Development of a Power Distribution Module for a Nanosatellite

by

MOTLOKWE MALEKA

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Supervisor: Mr. David Francois Visser
Co-supervisor: Prof. Robert Van Zyl

Bellville Campus
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DECLARATION

I, Motlokwe Maleka, declare that the contents of this thesis represent my own unaided work, and that the thesis has not previously been submitted for academic examination towards any qualification. Furthermore, it represents my own opinions and not necessarily those of the Cape Peninsula University of Technology.

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Signed   **Date**

ABSTRACT

The space environment is characterised by harsh radiation, extreme temperatures and vacuum. Electronics subsystems for satellite applications are designed to be fault tolerant and robust enough to survive this environment. A power distribution module (PDM) for a CubeSat nanosatellite application is developed here, with the aim to distribute power to CubeSat subsystems reliably. The PDM prototype is carefully designed with reference to an extensive literature study. The study dwells on the low Earth orbit (LEO) space environment, critically identifying radiation sources and temperature ranges in the LEO. The study further investigates traditional analogue techniques of logic circuit design using bipolar junction transistors (BJTs) which are known for their higher tolerance to radiation sources as compared to recent integrated circuits (ICs). Careful consideration is given to different ways of designing a fault tolerant system. The study specifically looks at redundant circuit design within the limitations of weight and space of a nanosatellite. Possible electrical faults in power systems are identified, which include over-currents, over-voltages, over-temperatures, inrush currents and latchup. This study shows that identified faults generally are over-currents. A power switch is included in each power distribution channel to trip the current in case a faulty condition is detected. The PDM is designed to have eight power output distribution channels to allow a subsystem load to connect to more than one channel, thereby meeting its power requirements. The PDM power channels are designed identically. Upon application, current limits are selected by a two-resistor divider circuit and connectors are used to connect to a required voltage bus at manufacturing time. The system's functionality is tested and verified using an Arduino development board interfaced to all I^2C devices as a master node, typically the on-board computer (OBC) in a real satellite mission. The system's functionality in a Gamma irradiated laboratory environment is verified to perform as required. The PDM system is further tested in a temperature cycled chamber from -31°C to 61°C. The system survived the entire eight hour test duration of two cycles. It is observed that the system is fault tolerant to radiation sources up to 10 krad and the temperature limits mentioned. The PDM system is recommended as an additional module to the CubeSat electrical power subsystem (EPS), thereby improving the reliability of the power subsystem.

Keywords: CubeSat, power channel, module, radiation, reliability, efficiency, I^2C, prototype.

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DEDICATION

I dedicate this thesis work to my late brother, Maputle Maleka, praise name "Moloto Mpepedi Morwa Kgoshi", an electromechanical engineer from UCT. He brought me to study in Cape Town, did all applications and inspired me to study further after he was impressed with my first semester results. Maputle taught me how to become self-independent away from home and strive to achieve greater in life.

I further dedicate this thesis work to my entire immediate family as a whole; namely my brother Katlego Mashoeu Harolad Maleka, my sister Refilwe Maleka CA(SA), my mother Rangoato Eunice Maleka and my father Mampone Colman Maleka. Proudly I can say you all contributed massively towards each day of this research work. I will forever be thankful for the countless opportunities you gave me in life and will be forever grateful for the compromises you made for me to study further.

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GLOSSARY

Acronyms and Abbreviations

ADC	Analogue to Digital Converter
ADCS	Attitude Determination and Control System
BCR	Battery Charge Regulator
Cal Poly	California Polytechnic State University
CPUT	Cape Peninsula University of Technology
ELaNa	Educational Launch of Nanosatellites
EPS	Electrical Power System
F'SATI	French South African Institute of Technology
GEVS	General Environmental Verification Standard
GSFC	Goddard Space Flight Centre
I^2C	Inter-Integrated Circuit
Mbps	Megabit per second
MC	Major Component
NASA	National Aeronautics and Space Administration
OBC	On-Board Computer
PCM	Power Conditioning Module
PDM	Power Distribution Module
TBD	To Be Determined
TCMD	Telecommand
TLM	Telemetry
TT&C	Telecommand, Telemetry and Control
UHF	Ultra High Frequency
VHF	Very High Frequency

CHAPTER 1: INTRODUCTION

1.1 INTRODUCTION

Subsequent to the 1957 first space launch of the Russian Sputnik 1 satellite, satellites were developed at a larger scale of mass and, hence, became more expensive to develop. The effects of changing world politics and military emphasis continuously put financial strain on the development of these large satellites in the space industry.

According to the National Aeronautics and Space Administration (NASA), micro- and nanosatellites are generally cheaper to produce and launch. NASA also believes that losing one nanosatellite within a constellation of small satellites is less of a financial risk as compared to losing one large satellite (Satter & Matousek, 2002:33). The advancing improvement and miniaturisation of micro-electronics have brought new ideas to develop smaller, cheaper and faster and more competent satellites.

Today, a number of small satellite constellations are proposed to provide global coverage, thereby providing real-time data to the global society. Recently, microsatellites have shown potential to effectively, rapidly and at a low cost execute civil and military missions such as communication services, Earth observation, technology demonstrators and educational training. To avoid confusion as to whether a satellite is large or small, a classification of satellites according to mass and typical cost is given in Table 1.1 (Rycroft & Crosby, 2002:2).

CubeSats are part of a category of satellites called nanosatellites. These were first developed and standardised in 1999 through the collaborative efforts of Prof. Jordi Puig-Suari at California Polytechnic State University (Cal Poly), San Luis Obispo, and Prof. Bob Twiggs at Stanford University's Space Systems Development Laboratory (SSDL). According to the CubeSat specification, a 1U CubeSat is a cubic satellite with dimensions of 10 x 10 x 10 cm^3 and a weight restricted to 1.33 kg[1]. This research project aims to develop a power distribution module (PDM) prototype for which the philosophy behind the design may be considered for future CubeSat missions.

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[1] http://www.cubesat.org/images/developers/cds_rev12.pdf

Table 1-1: Classification of satellites according to mass and typical cost (Rycroft & Crosby, 2002:2)

Class	Mass (kg)	Cost (US $million)
Large satellite	> 1000	> 140
Small satellite	500 - 1000	50 - 140
Mini-satellite	100 - 500	10 - 30
Micro-satellite	10 - 100	3 - 6
Nano-satellite	1 - 10	0.3 – 1.5
Pico-satellite	< 1	< 0.3

1.2 BACKGROUND TO RESEARCH PROBLEM

The French South African Institute of Technology (F'SATI) at the Cape Peninsula University of Technology (CPUT) offers a postgraduate programme in nanosatellite systems engineering where students are given the opportunity to be involved in the development of CubeSats. The first mission, a 1U CubeSat codenamed ZACUBE-1, has been completed and will be launched in 2013. The second mission, a 3U CubeSat codenamed ZACUBE-2, is currently under development by F'SATI students.

A satellite mission always has a payload, which is the mission-particular equipment. The payload dictates the top level satellite mission services intended for the satellite. The payload is supported by a satellite bus network, which is the combination of all other subsystems to provide the payload with housekeeping functions. The satellite bus consists of the communication subsystem, an on-board computer (OBC), a primary payload and where applicable a secondary payload, the attitude determination and control subsystem (ADCS), and a communication protocol interfacing all subsystem to communicate housekeeping telemetry and commands (Louis, 2008:37-38).

ZACUBE-1 is a CubeSat, as classified in Table 1-1; it therefore falls under the category of nanosatellites. A satellite system consists of a space segment and a ground segment. The space segment is represented by the CubeSat in space orbit and the ground segment consists of transmit and receive earth stations consisting of user network interfacing equipment, collectively known as the ground segment (Louis, 2008:37).

An example of the internal architecture of a CubeSat is shown in Figure 1-1, specifically showing the subsystems contained in ZACUBE-1. The internal subsystems depicted in Figure 1-1 are contained in almost all CubeSats. Although the functionality of each subsystem may differ according to various missions' requirements, the subsystems generally serve the same objectives to provide housekeeping functions. The payload is the only subsystem which serves a unique objective according to the specific mission objectives.
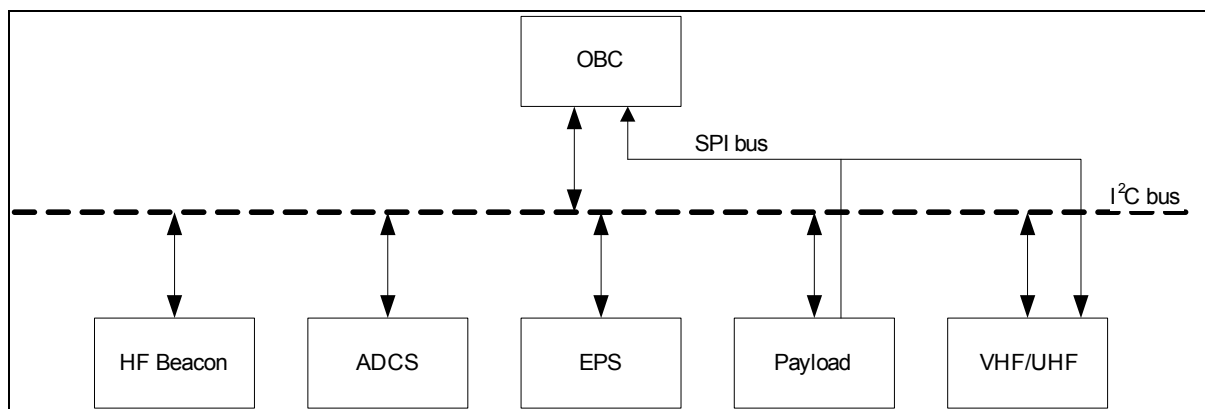
Figure 1-1: Block diagram showing F'SATI 1U CubeSat (ZACUBE-1) internal architecture

1.2.1 Satellite Subsystems

1.2.1.1 The Power Subsystem

The electrical power system (EPS), also simply referred to as the power subsystem, provides electrical power to all the other subsystems in the CubeSat. Herein, all other subsystems' power feeding from the EPS shall be referred to as subsystem loads.

The EPS comprises of the respective modules shown in Figure 1-5, namely the power source, power regulation and control, power storage and the power distribution module (PDM). This research project focusses on developing an optimised power distribution method which shall ensure reliable and efficient power distribution.
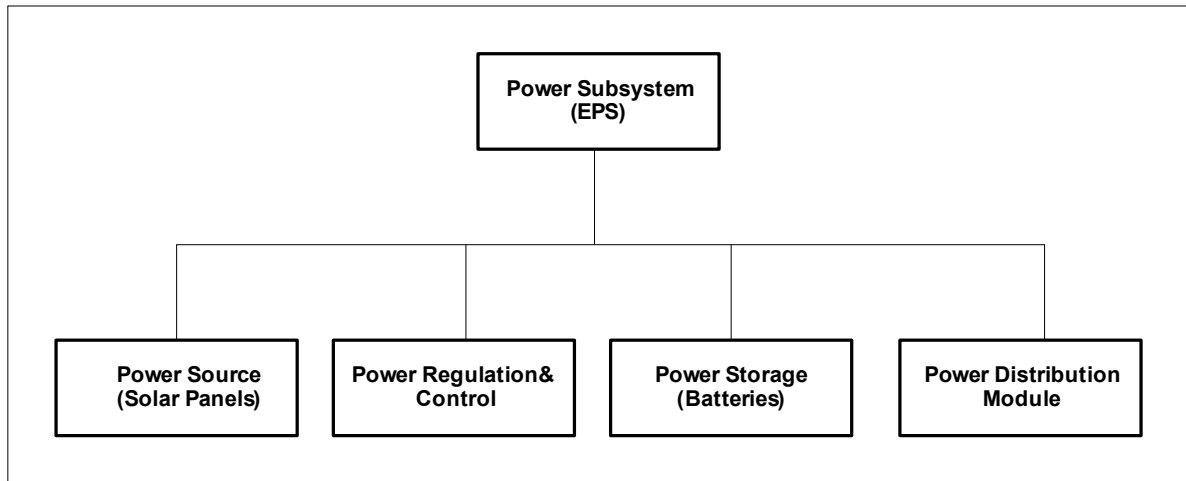
Figure 1-2: Components of a power subsystem

The primary power source in space orbit is solar energy from the Sun, extracted and converted into electrical energy by solar arrays (panels) which provide power to the EPS. The power regulation and control system may either be a direct-energy-transfer (DET) or maximum power-point tracking (MPPT) technique, which is used to efficiently draw maximum energy from the solar panels. The power storage devices are batteries, which store the electrical energy converted by the solar panels. The CPUT-F'SATI satellite programme currently does not have any PDM design, hence, is under investigation as part of this research project with a vision to add value to the CPUT-F'SATI satellite programme.

F'SATI uses the Clyde Space second generation EPS shown in Figure 1-6 (Clyde Space, 2010:6) which the PDM prototype is intended to complement. Clyde Space is a company located in Scotland, which has an online CubeSat shop where various CubeSat parts may be purchased. On the power side these include an EPS, spacecraft batteries, solar panels and space dc-dc converters[2]. To form a complete power system, the EPS needs to be integrated with solar arrays and suitable batteries, which are recommended to be 10Wh or 20Wh batteries for a 1-U CubeSat structure (Clyde Space, 2010: 6).

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[2]http://www.clyde-space.com/cubesat_shop/eps/8_1u-cubesat-eps
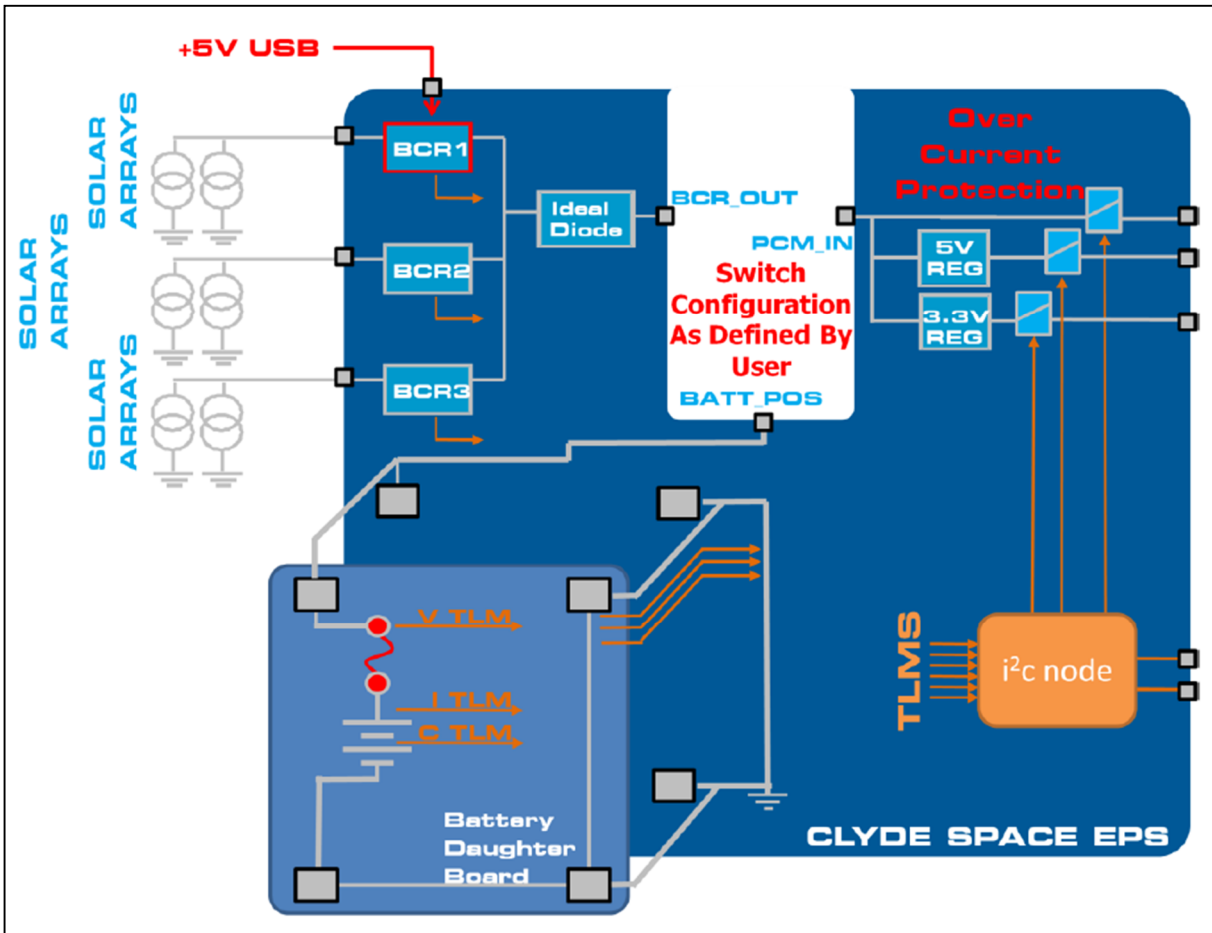
Figure 1-3: Clyde Space second generation EPS system diagram

(From Clyde Space, 2010:6)

The power supply in a CubeSat is limited and energy consumption should be managed efficiently throughout the mission lifetime. The solar cells and batteries used as part of the CubeSat power subsystem should be chosen to meet power consumption requirements from beginning-of-life (BOL) until end-of-life (EOL) of the CubeSat mission. In addition, the total energy requirement of all the electronic subsystems within the satellite must not exceed the limits of the energy supply capability of the power system (Larson & Wertz, 2005:303-304). In the following section, the problem statement is clearly defined for the reader to understand the need for an efficient and reliable power distribution method for a nanosatellite.

1.2.1.2 Communication Subsystem

A basic communication subsystem in the CubeSat consists of a receiver and a transmitter, collectively known as the transceiver. The very-high-frequency/ultra-high-frequency (VHF/UHF) transceiver is the communication subsystem which provides a link between the CubeSat and the ground station. During uplink, commands are received by the CubeSat's receiver, demodulated and executed by the OBC. During downlink, telemetry data is transmitted from the CubeSat to the ground station (Larson & Wertz, 2005:303).

1.2.1.3 On-Board-Computer

The OBC sends housekeeping instructions to the rest of the CubeSat subsystems. For ZACUBE-1, the OBC is based on the Pumpkin CubeSat OBC structure, part of the MSP430 instruments from Texas Instruments. Housekeeping functions include interpreting telemetry from subsystems and sending housekeeping commands.

1.2.1.4 Payload

A high frequency beacon (HF beacon) is the main payload for ZACUBE-1. The South African National Space Agency (SANSA) operates high frequency (HF) space weather radars at the South African National Antarctic Expedition (SANAE) base in Antarctica. A 14 MHz signal will be received by the radar on the ground station whenever the CubeSat passes over the radar's field-of-view. This signal will allow characterisation of the angle of arrival performance of the HF radar, thereby improving its scientific objectives. The radar is part of the global Dual Auroral Radar Network (DARN). The radars are collectively called SuperDARN, which is an international collaboration of HF radars in the Polar Regions that measure interactions between the solar wind and the Earth's magnetic field (Visser, 2011:1-3).

Besides the HF beacon, an additional payload for ZACUBE-1 is a camera, with the scientific objective to capture low resolution images of the Earth. For other satellite missions, experimental scientific payloads, such as charged particle sensors, are used to determine the electromagnetic field around the earth. A payload for a specific satellite mission will differ from the rest according to the scientific objectives the satellite mission is aimed to achieve. This will also determine the type of sensors, data rates, power budget, link budget, orbital characteristics, size and weight of the satellite as a whole.

1.2.1.5 Attitude Determination and Control Subsystem

The attitude determination and control subsystem (ADCS) receives measurement values from the different attitude sensors and, combined with a mathematical model, determine the orientation needed for the CubeSat to accurately stay in the correct orbit. Examples of the attitude sensors include orientation magnetometers, horizon sensors, sun sensors and star sensors.

Reaction wheels, magneto coils and thrusters are examples of actuators used to orientate the satellite. Common orientation techniques deployed on satellites are either spin-stabilised or three-axis stabilised. Reaction wheels may also be used to orientate the CubeSat in different directions without the need of thrusters. Typically, three reaction wheels are mounted on the three orthogonal axes of the satellite, namely yaw, roll and pitch. In order to rotate the satellite in a desired direction, the reaction wheel is spun in the opposite direction.

1.2.2 Communication Protocols

1.2.2.1 I^2C Communication Protocol

The inter-integrated circuit (I^2C) communication protocol is a widely used two wire synchronous serial data bus, commonly used in the electronic and embedded systems industry. ZACUBE-1 uses the I^2C communication protocol, whereby the OBC is the master device and all other I^2C devices in the CubeSat are coordinated as slave devices. The I^2C communication protocol has the option of synchronous speeds of up to 100 kbit/s, 400 kbit/s and 3.4 Mbit/s, respectively referred to as standard mode, fast mode and high-speed mode (Bruce, Gray, & Follett, 2003:1).

Traditionally, slave devices were connected to a microcontroller via individual address and data lines. This caused large numbers of wires, printed circuit board (PCB) tracks and more master devices to interface slave devices. In the 1980's, the I^2C low-bandwidth and short communication bus protocol was introduced by Philips, where all slave devices can now be connected via two serial wires, namely serial data (SDA) and serial clock (SCL). This is illustrated in Figure 1-2 (Total Phase, 2011:2).
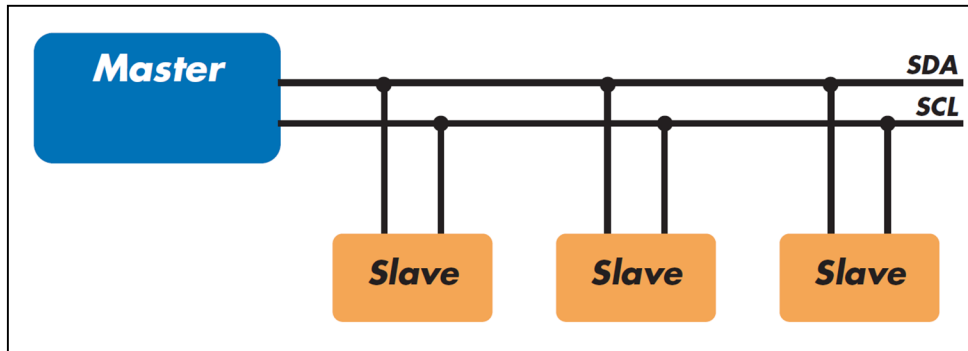
Figure 1-4: Sample I²C master/slave implementation

(From Total Phase, 2011:2)

The I²C master/slave theory of operation is illustrated in Figure 1-3 (Total Phase, 2011:2-3) and is explained as follows:

- The master device initiates communication by a start signal (START) to inform all slave devices to acknowledge the serial data line according to their respective addresses.

- The master then sends a slave address to the intended slave device that it wants to communicate to, followed by a read/write flag to read from or write to the device, respectively.

- The slave device acknowledges the sent address by responding with an acknowledgement (ACK) signal.

- Communication between the master and slave continues on the data bus with 8 data bits sent or received at a time.
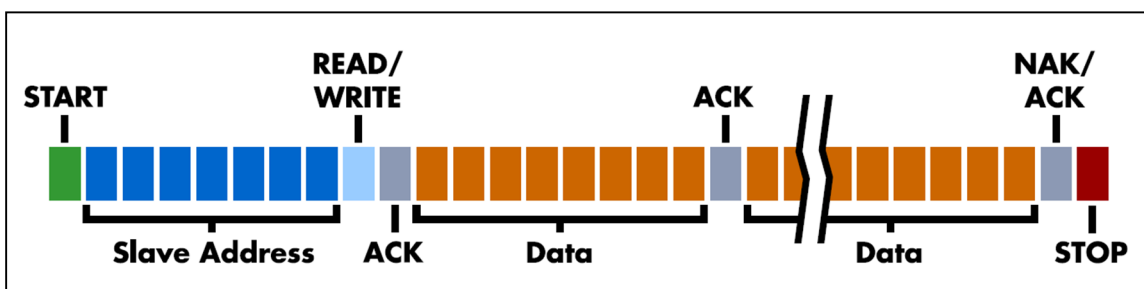
Figure 1-5: A sample bitstream of the I²C protocol

(From Total Phase, 2011:3)

1.2.2.2   SPI Communication Protocol

The serial peripheral interface (SPI) serial communication protocol is a full-duplex communication protocol developed by Motorola. SPI uses four bus lines as shown in Figure 4-4 (Total Phase, 2011:4-5), namely clock (SCLK), master output/slave input (MOSI), master input/slave output (MISO) and slave select (SS). SPI has the advantages that it is fairly easy to implement and supports high data rate transfer. Using SPI, the SS port of each slave device requires its own track and as a result a large number of tracks on the PCB are required. The I^{2}C communication protocol would be a much better solution for many serial devices on one board, where all devices' addresses are tied to the SDA bus (Total Phase, 2011:4-5).
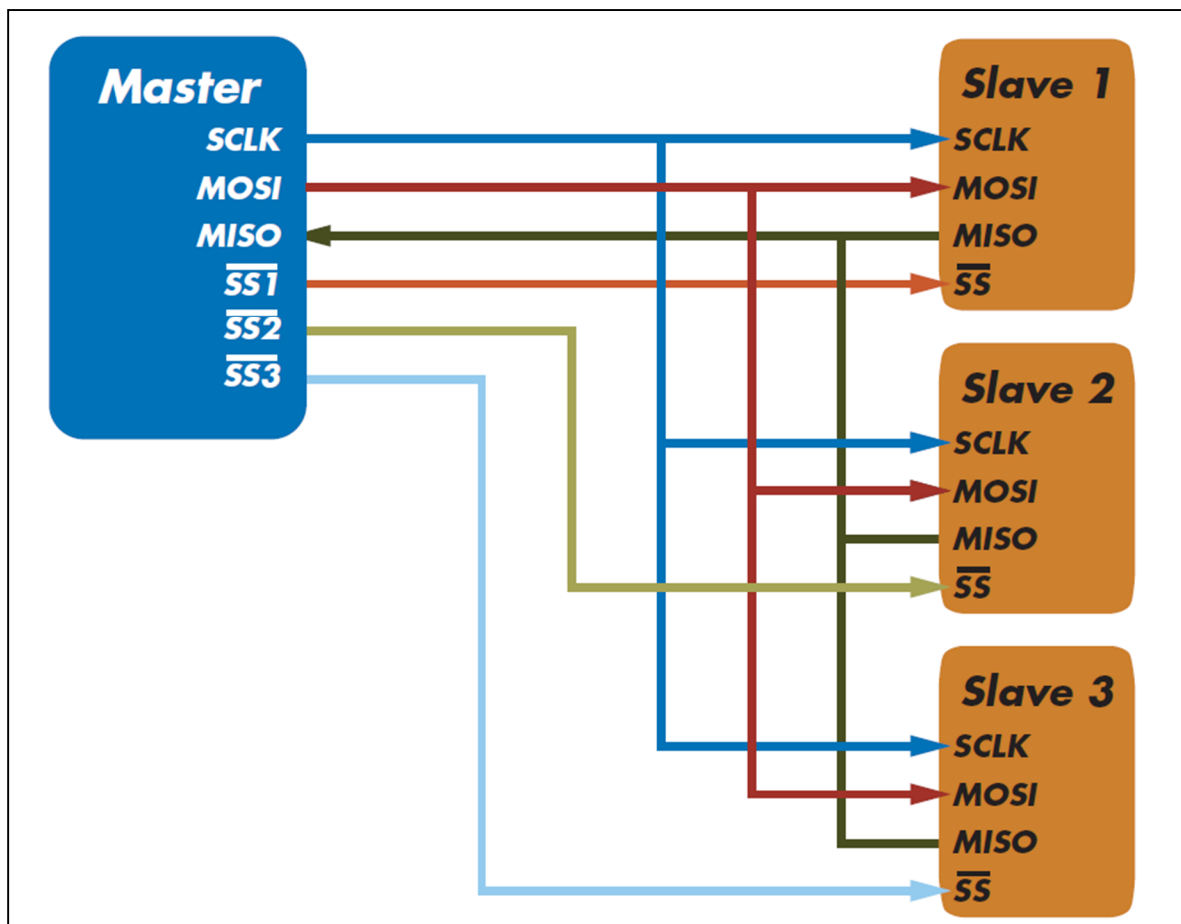
Figure 1-6: Sample SPI master/slave implementation

(From Total Phase, 2011:4-5)

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1.3 RESEARCH PROBLEM STATEMENT

The EPS provides voltage regulated output power channels to subsystem loads. Subsystem loads may completely fail due to possible electrical faults, such as latchup, inrush currents, over-voltages, over-temperature and over-currents which could occur while the nanosatellite is in orbit. Should a subsystem load, such as the communication subsystem or the OBC, fails due to one of the abovementioned faults, the nanosatellite may be totally lost in space due to a communication failure with the ground station.

In order to avoid total loss of a nanosatellite, it is vital to implement a reliable power distribution method which can ensure that subsystem loads are protected from possible power related faults such as those mentioned herein.

CubeSats are too small to employ complete redundancy in all subsystems. Therefore, by making a critical component such as a power supply more reliable, the overall reliability of the CubeSat may be improved. An efficient and highly reliable power distribution method is necessary for space power systems to massively reduce the high risk of satellite loss.

In addition to the problem statement, subsystem loads are restricted to be connected to one of three power outputs provided by the Clyde Space power subsystem, namely the battery bus (8.3V), 5V and 3V power busses. To allow subsystem loads the flexibility to connect to more than one power output channel, thereby allowing the subsystem load to meet its power requirement, it is necessary to investigate an alternative method to make available an increased number of efficient and reliable power output channels.

1.4 RESEARCH QUESTIONS

- Which technology and circuit design would be best suitable for a reliable PDM design?
- What are the required power ratings for CubeSat power systems?
- Which test procedures should be followed to test the developed prototype?
- Which environmental tests would be meaningful to verify reliability of the final prototype?
- What contribution will the research outputs provide to future nano-satellite missions?

1.5   RESEARCH OBJECTIVES

The research objectives define the broad goals the PDM subsystem is expected to achieve. The objectives are qualitatively drawn from the research problem statement defined in the previous section. Although objectives may be slightly modified during development of the power distribution concept exploration, it is essential to ensure that the main objective is met. Sub-objectives are not top level goals required to be reached. These are usually defined to utilise possible extra features which may be added to the subsystem design.

1.5.1   Main Objectives

- The main objective is to develop a PDM as an additional module to the power subsystem. The PDM should automatically, efficiently and safely distribute power to subsystem loads in a CubeSat feeding from the power subsystem, thereby detecting power faults, monitoring power measurements and controlling power distribution in the utmost reliable manner. The PDM should communicate trip and reset conditions to the OBC when electrical faults occur.
- The PDM must provide the OBC with continuous voltage, temperature and current telemetry for each power output channel so that this data may be known by the nanosatellite mission operators on the ground station.

1.5.2   Sub-objective

- The PDM prototype will be subjected to radiation and thermal environmental conditions similar to that in space, thereby predetermining the system's robustness to the space environment.

1.6   PDM MODULE FUNCTIONAL REQUIREMENTS

To meet the main and sub-objectives presented in the previous section, the PDM functionality requirements are divided into three main categories, namely power monitoring, power control and power switching. Power monitoring functions are intended to provide some form of power measurement data. Power control functions intend to command some form of housekeeping circuitry and power switching functions allow switching from one channel to another. These are all defined in more detail in the following subsections.

1.6.1   Power Monitoring Functions

Power monitoring functions entail power measuring devices which should provide the OBC with instantaneous telemetry of power distribution in the CubeSat, thereby allowing the OBC to accurately execute housekeeping commands to other subsystems. Telemetry to be monitored should include current, voltage and temperature measurements.

1.6.2   Power Control Functions

It is required to isolate subsystem loads from the power source in cases of fault conditions, which may result in damage to other subsystem loads. Power isolation may be achieved by trip commands controlling a low voltage drop power switch between the input and output channels of the PDM. A very low voltage drop (mV) power switch would ensure each subsystem load receiving precisely the voltage specified from the EPS. Trip commands would enable safe operating modes of the EPS as a complete system interfaced to the PDM under development. Isolation of subsystem loads via a power switch is a load protection method which aims to ensure that subsystem loads are protected when possible faults occur.

Through control circuitry, autonomous trip functions should automatically interrupt (isolation power trip) the current in a distribution channel if predetermined monitored thresholds are exceeded. The OBC should reset the trip function when the monitored fault conditions have cleared. The OBC should also be enabled to override the trip function.

1.6.3   Power Distribution and Switching Functions

The Clyde Space EPS features only three output power channels, with maximum ratings of 3.3V/4A, 5V/4A and 8.4V/6A. From these voltage/current ratings, the maximum power ratings are 13.2 W, 20 W and 50.4 W, respectively.

By distributing more than three output power channels, power delivered to subsystem loads could be increased by switching channels in parallel, such that a subsystem load may be physically connected to more than one output channel in order to suit its load requirements, otherwise limited to the maximum rated current of the EPS. A user should be able to physically switch a channel to a specified input voltage bus and output load at build-time as required.

1.7   PDM MODULE DESIGN SPECIFICATIONS

The PDM to be developed is for an operational application. The PDM design should be applicable to all CubeSat structures which use the standardised PC/104 PCB size and stacking arrangement. In this section, the reliability and characteristic specifications of the PDM prototype are discussed.

The prototype's reliability needs to be verified for expected environmental conditions in space orbit. Therefore, it is vital to dwell on a discussion about the various environmental tests aimed to be performed on the final prototype. All possible interfaces to the PDM prototype are presented herein, namely electrical, mechanical and software interfaces.

1.7.1   Reliability of Module

Subsections of an EPS design for space applications are generally required to be as robust, reliable and as efficient as possible. This requirement arises because failure of the power subsystem whilst the nanosatellite is in space orbit may result in total failure of the nanosatellite, such that all subsystems loads are shut down and communication to the nanosatellite is lost. As an additional module to the EPS, the PDM is generally required to be highly reliable so that the probability of power failure is significantly reduced.

1.7.2   Physical Characteristics

The PDM prototype will consist of electronic components mounted and soldered on a standard sized PC/104 PCB. The final PCB prototype shall be stacked with other subsystem boards as shown in Figure 1-7 (PC/104 specification version 2.6, 2008:3). The mounted components on the PCB shall be limited to a height restriction of 15.24 mm to allow for other PC/104 modules to be stacked on top or below that module as illustrated in Figure 1-7, unless it is otherwise not required to place other modules on top.
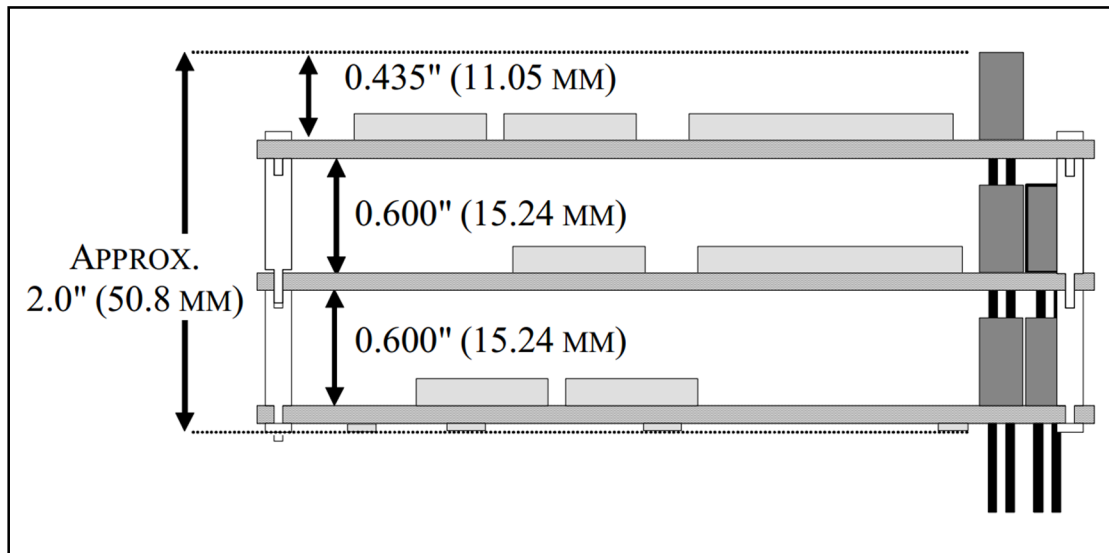
Figure 1-7: Typical PC-104 stack arrangement

(From PC/104 specification version 2.6, 2008:3)

The PC/104 PCB standard from factor has the following physical size characteristics[3]:

- 90 x 96 mm module dimensions;
- 15.24 mm spacing between individual vertically stacked modules;
- 8 or 16 bit (ISA) modules;
- 1.6 mm PCB thickness;
- Four mounting holes;
- Stack-through connectors to other PC/104 modules (Figure 1.7).

1.7.3 Environmental Tests

Environmental tests are divided into four categories, namely mechanical, thermal cycling, radiation and functional tests. Functional tests are normally performed in a laboratory environment and as part of other environmental tests. Mechanical tests depend on the respective mission launch vehicles to be used. Mechanical tests include vibration and shock testing, normally performed for the payload or the nanosatellite as a complete unit. Flight hardware is generally required by NASA to go through a random vibration and acoustic test regime to qualify the hardware for an expected mission launching environment. The test is performed to ensure that all electrical, electronic and mechanical devices are qualified to survive during launching of the nanosatellite.

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[3]http://www.pc104.org/specifications/PC104_Spec_v2_6.pdf

The other two tests are thermal cycling and irradiation tests. These tests are performed to qualify that the prototype will survive in space environments.

1.7.3.1 Vibration test

Vibration tests are not included as part of the verification process for in this research project. Vibration tests are performed only for a flight model, not for a research prototype model.

1.7.3.2 Thermal cycling

During thermal cycling tests, the temperature is cycled over the temperature limits that the nanosatellite is expected to operate under when in orbit. Although these limits are dependent on the mission orbital height, generally for low Earth orbit (LEO) nanosatellite missions, such as CubeSats, the temperature varies from -25 °C to 70 °C. The thermal chamber at Reutech Radar Systems (http://www.rrs.co.za) available for thermal tests gave a thermal profile from -31 °C to 61 °C.

1.7.3.3 Radiation tests

Radiation tests are performed to test the effects of radiation on a circuit. Electronic circuits in space are bombarded by radiation particles which may cause improper operation of the circuit, such as bit flips or memory corruption. Radiation tests are divided into two categories, namely total ionisation doze and single-event effects (SEE) radiation tests. During radiation tests, radiation sources illuminate the unit under test (UTT) for a certain period which corresponds to total radiation dose. The prototype that was developed, was exposed to a total of 9.8 krad of Gamma rays over a period of 210 minutes.

1.7.4 Electrical Interfaces

Module interfaces are divided into three categories, namely electrical, mechanical and software interfaces. Electrical interfaces may further be divided into digital, power inputs and power outputs. Software interfaces to a nanosatellite enable communication of received telemetry data and telecommands.

1.7.4.1 Digital interfaces

The current F'SATI-CPUT 1U and 3U CubeSats use an I^2C communication protocol for telemetry interface between subsystems. Therefore, it is essential to investigate a method of interfacing digital components on the PDM to the OBC via the I^2C communication protocol.

1.7.4.2 Power input interfaces

The PDM will need to accept the Clyde Space EPS three regulated voltage bus lines as power inputs. Although the PDM is intended to be configurable to accept a range of low voltage inputs in the typical nanosatellite range, power inputs are limited to those provided by the EPS. Power inputs are calculated by a straightforward multiplication of the maximum ratings of "input voltage" and "input current rating" listed in Table 1-2, which were taken from the Clyde Space EPS.

1.7.4.1 Power outputs

The PDM is required to have a minimum of eight switchable power outputs. No voltage regulation is required as it is already implemented on the EPS. Power outputs shall be differentiated by respective current limits such that a subsystem load may be configured to more than one output channel to increase its overall current requirements, thereby meeting its power needs. Table 1-2 (Clyde Space, 2010:8) lists values of expected voltage and current ranges as adopted from Clyde Space EPS manual.

Table 1-2: Expected electrical characteristics of PDM (Clyde Space, 2010:8)

PARAMETER	Symbol	Minimum	Typical	Maximum	Units
Input voltage busses	V_{IN}	--	3.3 bus 5 bus 7.2-8.4 bus 12 bus	--	V
Input current rating	I_{IN}	0		6	A
Output voltage busses	V_{OUT}	--	3.3 bus 5 bus 7.2-8.4 bus 12 bus	--	V
Output currents	I_{OUT}	0	--	12	A
Operating temperature	T_C	-40	60	80	°C
Storage temperature	T_S	-50	25	100	°C
Mass	M	60	70 - 80	100	g
PCB dimensions (PC/104)	--	--	90 x 96 x 1.6	--	mm^3

1.7.5   Mechanical Interfaces

The PDM prototype shall be supported in the CubeSat by four mounting holes as described by the standardised PC/104 PCB specifications listed earlier. The PC/104 board has four standard slots for insertion into the CubeSat, whereas the height between respective boards is 15.24 mm when boards are stacked on top of each other.

1.7.6   Software Interfaces

Software interfaces are divided into two main categories, namely telecommands and telemetry. Telecommands are housekeeping instructions from the OBC or ground station, received by the PDM to regain proper functionality when faults have occurred. Telemetry is the information sent from the PDM subsystem and received by the OBC or ground station. Telemetry is used for decision making when telecommands are sent to the PDM.

1.7.6.1   Telemetry

The OBC should receive the following telemetry information from the PDM:
- Power output channel current;
- Input voltage from the EPS;
- Temperature of the PDM board or individual power channels;
- The pre-set current trip level for the OBC to be aware of over-current conditions.

1.7.6.2   Telecommands

Telecommands to the PDM should be commanded by the OBC via the I^2C communication bus. Expected telecommands are:
- Trip power switch if any of the telemetry received (current, voltage or temperature) is beyond pre-set thresholds;
- Override all trip functions and force reset when channel trips continuously;
- Reset terminal power switch when fault is cleared.

1.8 PROPOSED POWER DISTRIBUTION MODULE

Functionally, the proposed PDM is divided into three subsections as shown in Figure 1-8, namely power distribution and switching, power monitoring and power control.
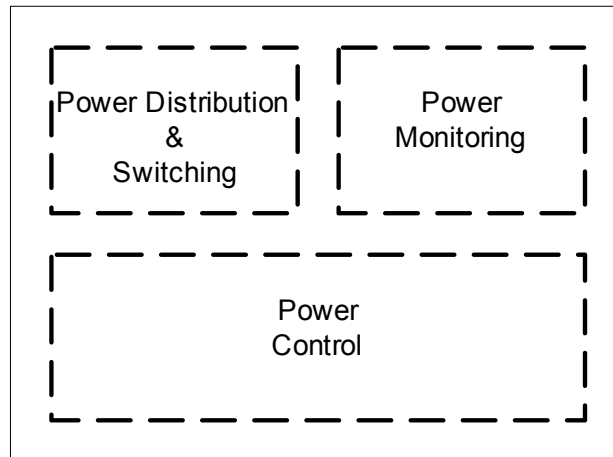
Figure 1-8: Definition of functional subsections to be contained within the PDM

At this stage, it is assumed that the control section will take up the larger part of the PDM board mainly due to the need for highly reliable and redundant electronic circuitry to accept housekeeping analogue and digital telecommands. For power monitoring, voltage and current sensors will be used to provide all required telemetry. The requirement for power distribution and switching will be governed by the PCB layout, in the sense that power output PCB tracks should be wide enough to handle maximum currents through the switching ports implemented as part of the design.

1.8.1 Power Distribution and Switching

With minimum voltage drop, the proposed PDM design primarily aims to distribute a limited number of power output channels due to the space constraint on a standard PC/104 board. However, it is required by the F'SATI technical team that a minimum of eight power outputs be available as shown in Figure 1-9. More power outputs may be added should there be space available on the final PCB design. In Figure 1-9, it is shown that a switching methodology will be investigated, which should provide all eight power outputs with the flexibility to be connected to any of the input voltage busses at manufacturing time. Referring to the Clyde Space EPS, the three voltage busses provided will act as inputs to the

PDM. An extra 12 V bus will be added, with a vision that ZACUBE-2 may have a higher power demand and a new four voltage bus EPS may be developed in future.
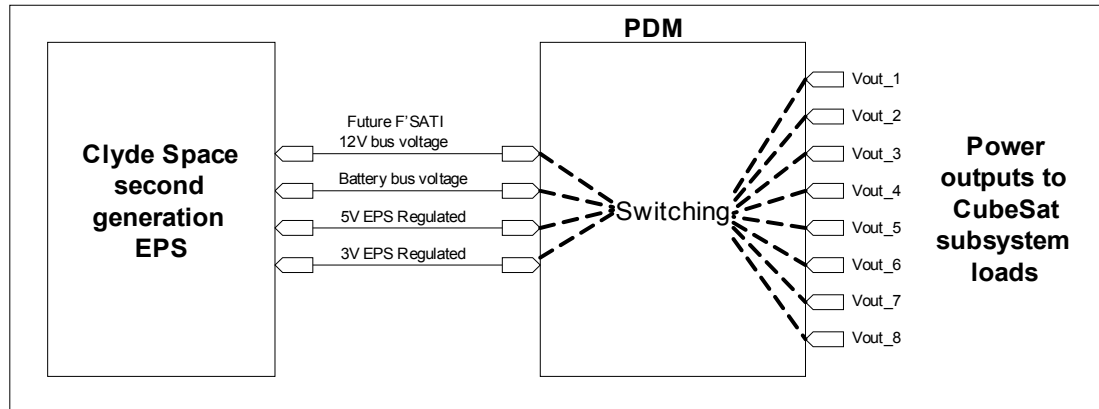
Figure 1-9: Interfacing PDM to Clyde Space second generation EPS

1.8.2   Power Monitoring Devices

The monitoring subsection of the PDM will consist of electronic sensors used to provide housekeeping telemetry to the OBC. In particular, current, voltage and temperature sensors are required. Current sensors will monitor the current flow in each power channel, thereby accurately informing the OBC of any faults due to threshold limits being exceeded. Although the Clyde Space EPS subsystem provides regulated voltage outputs, it is a research sub-objective to monitor those voltage output busses, which are voltage input busses to the PDM as depicted in Figure 1-9.

1.8.3   Power Control Circuits

The control circuitry will form part of the critical subsection of the PDM. A study of possible electrical faults in subsystem loads is presented in the next chapter, with the aim to guide the control circuitry design of the power switch control section. Control circuitry is expected to execute trip and override functions by receiving trip and override commands from the OBC, thereby controlling the power switch accordingly.

The PDM controls the power distribution to subsystems in a CubeSat, and enable diagnostics of fault conditions on the power supply network. Since it is of critical importance that a power supply of a satellite be reliable, the next chapter includes a literature study on space environmental effects which could possibly affect normal operation of the PDM.

1.9 SCOPE AND LIMITATIONS

The work presented in this thesis is for research purposes only, which is intended to verify the feasibility and functionality of a PDM prototype. Environmental verification testing will include functional tests during irradiation and thermal cycling. Test limits will conform to those stipulated by the F'SATI technical team, as the research project is a contribution to future F'SATI CubeSat missions. Therefore, to use the prototype for any other CubeSat satellite mission, verification tests on the prototype should be performed under that particular CubeSat mission's specification and not those to be determined in this document.

1.10 THESIS OUTLINE

Chapter 1 gives background of the research problem, and identifies the research objectives. Design specifications and requirements are outlined and a preliminary design concept is proposed.

Chapter 2 provides detailed studies of environmental conditions in space, leading to discussions on environmental testing. Trade studies of electronic device physics and possible faults in power systems are presented, subsequent to which a solution approach is proposed.

In chapter 3, the proposed design is expanded into circuit designs and simulations. Suitable electronic devices for the design are identified and a PCB layout is designed.

Chapter 4 develops a test bench to verify proper operation of the PDM prototype, whereby the prototype is interfaced to computer software to test telemetry and telecommand housekeeping functions. Functional and environmental tests are conducted and reported on.

Verification results are presented and analysed in Chapter 5. Laboratory functional tests results are compared to functional results captured during functional tests under radiated and thermal cycled environmental conditions.

Chapter 6 concludes with a critical review of the research outcomes. Possible future work and recommendations are identified.

1.11 SUMMARY

The F'SATI postgraduate satellite systems engineering programme currently running at CPUT was introduced in this chapter. Postgraduates are involved in research projects based on the development of nanosatellites. The background section provides an overall discussion of CubeSats and the involvement of F'SATI students in the research field of CubeSats. In particular, the subsystems contained in the current ZACUBE-1 CubeSat are presented to provide the reader basic understanding of the different subsystems contained in a typical nanosatellite. The project's main objective to have reliable control over power distribution in a nanosatellite is outlined. Prototype characteristic requirements and specifications are defined and a proposed design is presented. The chapter concludes with a thesis outline.

CHAPTER 2:   LITERATURE REVIEW STUDY

2.1   INTRODUCTION

This chapter introduces the space environment, thereby highlighting the effects of vacuum, temperature and radiation on spacecraft in the low Earth orbit (LEO). Radiation tests are performed to predict radiation tolerance of a device or subsystem. Total doze ionisation and single-event effects (SEE) are discussed in this chapter. Thermal cycling tests are also performed to determine the satellite's tolerance to the variation from high to low temperatures experienced on opposite sides of the Earth when a satellite is in orbit. Generally, circuit designs for satellite systems should be of high reliability and of increased fault tolerance to survive the harsh space environment. It is therefore of critical importance to study the different types of redundant circuit design techniques to increase a system's tolerance to fault conditions. It is also necessary to identify possible electrical faults a power subsystem such as the power distribution module (PDM) may encounter whilst in space orbit, so as to implement preventative measures during the design phase. Herein, trade studies on the abovementioned are described, subsequent to which a strategic solution approach is proposed.

2.2   THE SPACE ENVIRONMENT IN LEO

The hash space environment should be considered when designing satellite subsystems according to the mission altitude at which the satellite is designed to orbit. Nanosatellites are characterised by low power budgets which allow these small satellites to efficiently communicate only at LEOs, mainly due to lack of sufficient electrical power to transmit data at higher altitudes. LEO altitudes are ±450 km above the Earth surface, where a satellite would take about 90 minutes to complete one orbit around the Earth (Homeck & Rettberg, 2007:274).

A nanosatellite in the LEO space environment will be affected by physical space conditions such as "high vacuum, short-wave solar radiation (also known as electromagnetic waves),

ultraviolet X-rays, gamma radiation from the galactic background, high-energy particles (electrons, protons, neutrons and alpha particles), the cold background of space, microgravity, aerodynamic drag of the atmosphere at LEOs and influence of atomic oxygen" (Ley, Wittmann & Hallmann, 2008:33-35). Normal functionality of electronic devices in the space environment is mostly negatively affected by increased temperatures, pressure (vacuum) and different sources of radiation which are discussed in the following subsection.

2.2.1 Vacuum in LEO

In LEO the typical vacuum pressure is of the order 10^{-14} Pascal (Pa). This vacuum pressure is the environmental constitution of hydrogen, molecular oxygen, highly reactive nitrogen and oxygen atoms (Gargaud, 2011:1538).

2.2.2 Temperature in LEO

It is essential to know the temperature range in LEOs to estimate the temperature range electronic components used for the PDM prototype will be expected to survive when the satellite is in space orbit. Although the research project is not intended for a particular prescribed mission, thermal cycling tests will be performed to inform the F'SATI technical team, and generally all those interested in using the PDM system, of the environmental limits the PDM system can survive. Typical temperature variations in LEO range from -40°C to 70°C.

2.2.3 Space Induced Radiation

Different microelectronic technologies react differently to the effects of space radiation. Natural space radiation sources which may affect LEO satellites include galactic cosmic rays (GCR's), particles emitted by solar events and particles trapped in the Earth's radiation belts (Edmonds, Barnes & Scheick, 2000:3). According to Johnston (2000:6), LEO satellites in the 300-1400km altitude range are mostly affected by the trapped radiation belts which act as a steady source of radiation and solar flares from the sun. Johnston (2000:6) further states that trapped radiation belts occur in the South Atlantic Anomaly and contains approximately 2krad radiation dose of protons.

Space radiation is categorised into three sources of radiation. The first source which is important to consider at LEOs is the Earth's van Allen belts (VAB's), where charged particles of the Earth are trapped by the Earth's magnetic field. The second source of radiation is known as the galactic cosmic rays (GCRs), mostly important for higher altitudes satellite

missions. The third source of radiation is solar particle events (SPEs) caused by proton and electron emissions from the sun (Bevelacqua, 2008:253).

2.2.3.1 Van Allen Belts

Van Allen Belts (VABs), also known as trapped radiation around the earth, are constituted by charged particles trapped by the electromagnetic fields of the Earth. VABs exist as inner and outer belts. In terms of the Earth's radius ($R_C = 6.4 \times 10^3$ km), the inner radiation belt lies around 2.8 R_C and the outer radiation belt from 2.8 R_C to 12 R_C (Bevelacqua, 2008:253). The inner belt is characterised by even more energetic electrons (Novikov *et al.*, 2008:1).

2.2.3.2 Galactic Cosmic Radiation in LEO

Galactic Cosmic Radiation (GCR) is also referred to as Galactic Cosmic Rays (GCRs). GCRs are caused by extra-solar cataclysmic events such as supernovae. LEO missions are not affected to a large extent by GCRs and SPEs because the Earth's atmosphere shields them. The GCR intensity level is minimum at solar maximum conditions, and increases to maximum during solar minimum conditions (Bevelacqua, 2008:259).

2.2.3.3 Solar Cosmic Radiation in LEO

Solar Cosmic Radiation (SCR), also known as solar flare radiation, comprises of low-energy solar particles and high energy SPEs. Carbon, nitrogen and oxygen contribute to about 1% of the solar flare radiation emissions. Low-energy solar wind particles constantly flow from the Sun while highly energetic SPEs "are emitted from magnetically disturbed regions of the Sun in sporadic bursts" (Homeck & Rettberg, 2007:275).

According to Bevelacqua (2008:259-260), SPEs are ejections of matter from the Sun comprising of mostly protons and alpha particle. It has not yet been accurately predicted by solar physicists as to when SPEs will occur. It is therefore still extremely dangerous for astronauts to go on missions to other planets in outer space.

2.3 ENVIRONMENTAL VERIFICATION TESTS

Satellite hardware needs to be qualified before launch according to a general environmental verification standard (GEVS). A GEVS provides the basic requirements and processes to be followed for an environmental verification program. Goddard Space Flight Centre (GSFC) presently applies the GSFC-STD-7000 (NASA-GSFC-STD-7000, 2005:11) standard. For satellite missions, the launch provider's GEVS needs to be followed.

2.3.1 Types of Verification Testing

In the space manufacturing industry, manufactured products need to undergo production monitoring and acceptance testing to qualify the product for space applications.

A *production monitoring test* is performed to verify that the manufacturing process was properly implemented; thereby assuring that the product meets all quality specifications. This test is normally the responsibility of the product manufacturer.

Acceptance tests are performed to verify that the tested item is qualified to perform according to the item's prescribed documentation upon purchase. Also, acceptance tests demonstrate the quality assurance of the item upon delivery under the terms and conditions of that specific delivery contract (NASA-GSFC-STD-7000, 2005:14). Environmental acceptance tests are performed in environmental chambers. These tests demonstrate that an item is suitable to be used for flight or ground purposes (NASA-HDBK-8739.19-2, 2010:20).

Design qualification tests verify functionality of the tested item under a simulation platform with more severe conditions than those expected in the space environment. The primary purpose of a design qualification tests is to demonstrate the design can work and possible manufacturing techniques that could be considered. This test method is used to "prototype" or "protoflight" test levels (NASA-GSFC-STD-7000, 2005:15). The design qualification test would best suit the verification process for the PDM prototype, although environmental tests will be added to qualify the prototype.

Functional tests are those performed during the first stages of any system verification process. Functional tests are performed to verify that the item performs according to the design performance and functional specifications.

2.3.2   Radiation Testing

Three types of radiation sources are found, namely Alpha, Beta and Gamma rays. Commonly used for laboratory total ionising dose radiation tests are Gamma rays. Total ionising dose radiation tests are performed at a proton facility, where the common effects on microelectronics can be carefully monitored. These effects are collectively referred to as single-event effects (SEEs).

Various total ionising dose radiation test methods exist, such as specified by the MIL-SDT-883, TM1019 and ESA/SCC No. 22900 standards. Although different methods exist, the general goal is to measure the extent to which microelectronics under test can tolerate total ionising dose radiation. There are different configurations in which total ionising dose radiation tests may be implemented, which are briefly discussed below.

2.3.2.1   Enhanced Low-Dose-Rate Sensitivity

According to James *et al.* (2008:20), radiation induced charge that increasingly build up in bipolar devices, such that the oxides separating the base-emitter junction is negatively affected, results in degradation of the device's performance characteristic degrades.

Since the early 1990s, it was found that certain bipolar transistors and ICs (Integrated Circuits) exhibit enhanced low-dose-rate sensitivity (ELDRS), which means the total ionising dose has more effect at low dose rates than at higher dose rates.

Recently, however, it was found that the effects of ELDRS on circuits are small. It should not be of critical importance to focus on possible device failure which could be due to ELDRS during the radiation tests.

2.3.2.2   Pre-irradiation Elevated Temperature Stress Effects

Pre-irradiation elevated temperature stresses (PETS) in electronic devices are caused by exposure to thermal cycles during packaging and reliability tests of the device. PETS can increase the static leakage currents in a device during irradiation or negatively affect the proper functionality of the device. For one to accurately analyse the results from a device's total ionising radiation response, it is advantageous to know of PETS so that errors in devices may be correctly identified. It has also been observed that the total ionising dose response of integrated circuits (ICs) exposed to PETS is different to those ICs used for qualification testing only (James *et al.*, 2008:26).

2.3.2.3   Optimum Laboratory Radiation Sources

Total dose degradation of electronic components in space is caused by the high amount of electrons and protons in space to which the components are exposed to. For laboratory radiation tests, Co-60 gamma and X-ray sources are the most widely used options to test radiation tolerance of electronic devices, thereby creating a simulation platform of electrons and protons. X-ray sources are an optimum test solution for process development and control. This is because X-ray sources can function at higher dose rates than Co-60 sources. Although this is the case, Co-60 sources are optimum for device hardness assurance testing.

2.3.3   Single-Event Effects

Heavy ions and protons can cause single-event effects (SEEs) in ICs. These effects result in soft or hard errors. Soft errors do not cause permanent damage to a device. They are measured in errors/bit-day, and if the rate is too high it may results in poor performance of the unit under test (UUT). A good example of a soft error is a single-event functional interrupt (SEFI), which occurs when a device goes into its non-functional mode such as a test mode or a power-on reset mode.

Hard errors are those which cannot be corrected simply by reprogramming the device, hence may result in damage to the device. It is essential to study the different types of SEE tests. Different types of SEEs are briefly discussed below.

2.3.3.1   Single-Event Upsets

Information is stored at nodes in memory circuits. A heavy ion or proton particle that strikes a circuit node can result in incorrect data stored. This type of soft error failure mode is commonly known as a single-event upset (SEU). Digital ICs are mostly affected by SEUs due to an ion hit to a digital or analogue component in the IC. The ion hit changes the state of a digital component in the IC because of a voltage transient created in its analogue component (Edmonds *et al.*, 2000:47).

2.3.3.2   Single-Event Latchup

Single-event latchup (SEL) events cause latchup states. This type of SEE is the most dangerous because it threatens the reliability of a subsystem. To reduce the risk of system failure because of SEEs, current limiting and fast trip modes are incorporated in the design.

2.3.4 Thermal Cycling Verification Tests

According to NASA's GSFC-STD-7000 verification standard (NASA-GSFC-STD-7000, 2005:18), temperature cycling is well defined as follows; "a transition from some initial temperature condition to temperature stabilization at one extreme and then to temperature stabilization at the opposite extreme and returning to the initial temperature condition". In simpler terms, temperature cycling refers to a variation of temperature from minimum to maximum, thereby observing the item's behaviour under changing and extreme pre-set temperatures. The thermal cycling test, also known as thermal-vacuum testing, is generally performed to ensure that the system operates normally under expected in-orbit temperatures, but conservatively over a wider temperature range. For acceptance and qualification tests, the temperature limits are ±5 °C beyond expected temperature limits and for qualification tests the limits are ±10°C beyond expected temperature limits.

In the satellite production industry, thermal cycling tests are implemented to assure readiness of flight hardware, thereby assuring that the hardware is reliable enough to be operated in an expected space temperature cyclic environment. For example, printed circuit boards (PCBs) may experience solder joint cracks due to the thermal mismatch of materials.

2.3.4.1 Thermal Margins

The thermal extreme points, also known as thermal margins, are the minimum and maximum temperatures to be tested, which are beyond expected temperatures during the mission lifetime. These temperature margins are predetermined by the test facility program or a verified tested model of the subsystem. If neither party can provide test margins, it is advisable to consult with the thermal engineer for the project. For this research project, the F'SATI chief engineer responsible for the F'SATI CubeSat developments shall provide thresholds according to future F'SATI CubeSat mission requirements. Due to the unavailability of facilities, thermal cycling verification tests are performed at normal atmospheric pressure.

2.3.4.2 Temperature Cycles

Fully assembled subsystems in a satellite are expected to undergo a minimum of four (4) thermal-vacuum cycles whilst functionality of the subsystem is monitored. Individual components are expected to undergo a minimum of eight (8) thermal-vacuum temperature cycles before assembly for a protoflight. During the eight temperature cycles, the component is also operated to monitor its performance under the thermal cycled environment.

2.3.4.3 Test Duration

Payloads are expected to be exposed to extreme temperature points for at least twenty-four (24) hours per temperature cycle. Subsystems are exposed for a minimum of twelve (12) hours at extreme points per cycle and similarly for components only four (4) hours at extreme points per cycle (NASA-GSFC-STD-7000, 2005:119).

2.4 ELECTRONIC COMPONENTS SUITABLE FOR SATELLITES

Due to the limited mass, space and power budget for CubeSats, subsystems are generally required to be characterised by simple designs, low cost, low mass and low power consumption. Selection of electronic components for space applications also requires that the components be able to preserve their functionality under the effects of radiation in space. Radiation hardened electronic components, also known as space qualified components, are known to be too expensive. For short lifetime and low cost nanosatellite missions such as CubeSats, it becomes a compromise to use common off-the-shelf electronic components which are cheaper but non-space qualified. The balance in this compromise is that these non-qualified electronic components should still be able to tolerate the higher temperatures and radiation for a short lifetime nanosatellite mission.

2.4.1 Derating of Electronic Devices

Performance of electronic components can degrade due to operation in fluctuating or hash environments. In the space environment, a satellite orbiting at LEO will make a full rotation around the Earth in ±90 min; hence, will experience high temperatures when passing the Earth's side facing the Sun and low temperatures on the opposite side of the Earth not facing the Sun within that ±90 min time frame.

For example, the performance of a field-effect-transistor (FET) is known to decline due to self-heating effects which causes the junction temperature of the FET to increase. As a result, the power dissipation of the FET increases and electron transport degrades. This change in temperature is related to the dissipated power according to Equation 2.1 (Baca & Ashby, 2005:237-246) as:

$$\Delta T = R_{th} I_D V_{DS} = R_{th} P_D \hspace{5cm} \text{Equation 2.1}$$

where P_D is the dissipated power and R_{th} is the total thermal impedance thermal across the FET. Equation 2.1 shows that the junction temperature of a FET depends partly on the manner in which the power is thermally dissipated.

2.4.2   Surface Mount Technology

There are several printed circuit board (PCB) design software tools which offer a PCB designer better and faster design methods by automated rule checking for clearance between components, checking connection of all tracks, multilayer PCB designs and repeated multi-channel designs on a single PCB. A critical decision lies between using surface mount technology (SMT) components or traditional plated through-hole (PTH) components.

SMT, based on surface mount devices (SMD's), is structured as terminal surface area plates which are soldered on top of a PCB pad as shown in Figure 2-1 (a), rather than lead wires soldered through a hole in the PCB for PTH components as shown in Figure 2-1(b) (taken from Williams, 2005:58).
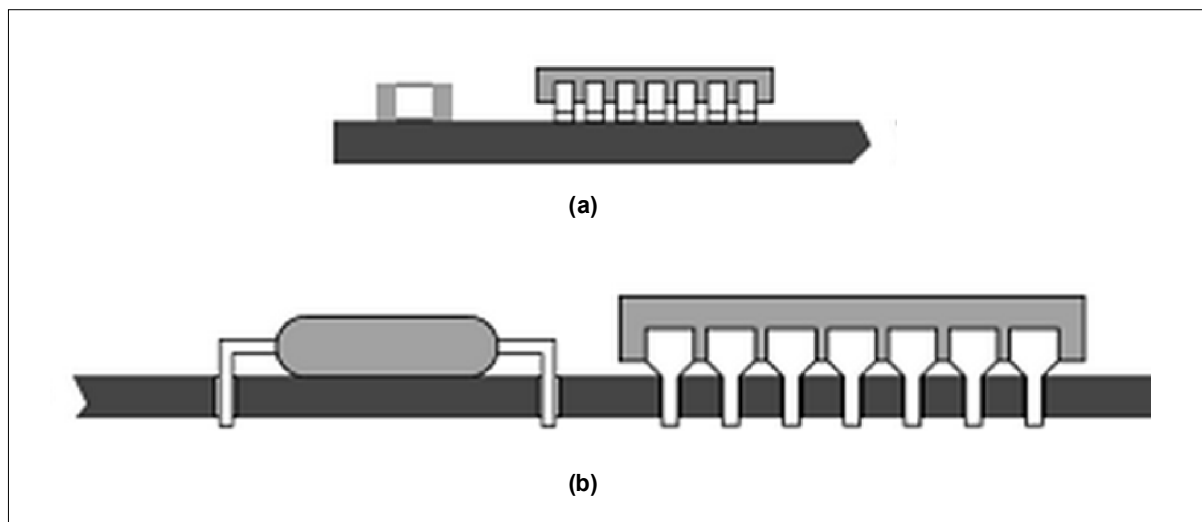
Figure 2-1: (a) Surface mount devices and (b) its equavalent PTH devices

(From Williams, 2005:58)

SMDs hold many more advantages than PTH components and in most designs currently SMDs can take up to 90% of the PCB assembly. Although this is the case, it is highly unlikely that PTH components will completely disappear. Table 2-1 lists the advantages and disadvantages of SMDs as compared to PHT components (Williams, 2005:58-59).

Table 2-1: SMT in comparison to PHT

Surface Mount Technology (SMT)		
	Advantages	**Disadvantages**
Size	Smaller sized components, small height and both sides PCB mounting offer increased circuit design density.	Difficult to test SMDs, increased chance of short circuits during tests due to components too close to each other. Easier to test and replace PTH components.
Electrical Performance	Higher speeds, higher accuracy, lower noise.	Not all components available in SMT.
Cost	Reduced product cost and fully automated assembly for cost effective large volume production.	Company needs to invest in special skills, techniques and production machinery in order to jump into SMT.

2.5 TRADE STUDY 1: CIRCUIT TOPOLOGY

Performance, voltage efficiency, switching speed, low power consumption and reliability characterise a suitable IC. This trade study aims to highlight possible control circuit design techniques and IC selection criteria to guide the design process in the next chapter. In addition, the study aims to show possible circuits which can be used to interface analogue control circuitry to digital I^2C commands from the on-board computer (OBC).

A design methodology needs to be chosen which shall provide a robust and reliable PDM design. The trade study presented here outlines the application of large-scale integrated circuits (ICs) as compared to using low-scale ICs combined and discrete components for nanosatellite applications. Using a single highly integrated IC which provides most, if not all, of the PDM functional requirements is one way of a design methodology. Another would be to use the combination of low-scale integrated ICs and discrete components to build the

PDM. Each design methodology is carefully studied for space applications. The critical components of the design are:

- Telemetry sensors;
  - A suitable current, voltage and temperature sensor to provide telemetry. The current sense resistors in the main current path are also critical.
- Decision making circuitry;
  - A suitable IC or circuitry design for decision making. This will provide the trip and override functions which should control a power switch.
- Power switch;
  - A power switch in the main current path needs to reliably switch the largest expected current, maximum of 6 A.

2.5.1 Large-scale Integration Circuits

Using the large-scale ICs such as the TPS2480/1 current monitor from Texas Instruments[4] can provide a suitable highly integrated solution. The IC provides current, voltage and power telemetry via an I^2C communication protocol. The IC further includes a gate-drive digital pin (pin 13 in Figure 2-2) which is used to control a field-effect transistor (FET) power switch, thereby executing trip commands.

2.5.1.1 Advantages: Space and Weight

Space and weight are major design limitations to subsystem designs for small satellite missions. For nanosatellite applications, using a single large-scale IC design approach occupies minimum space and weight. A single surface mount IC such as the TPS2480/1 current monitor occupies less space and weight than bulky circuits comprising of discrete components and less integrated ICs.

2.5.1.2 Disadvantages: Susceptibility to Space Radiation

The 20-pin TSP2480/1 IC is large-scale integrated IC, as seen from the functional block diagram in Figure 2-2. The IC is available in a 6x4 mm surface mount package and contains a large number of transistors. The likelihood of one of these transistors to be damaged by a radiation particle is much larger than would be in a device with simpler construction. Should a radiation particle affect half the IC's functionality, the PDM's performance will be largely compromised. To avoid such drawbacks, it is recommended to implement simpler integrated

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[4] http://www.ti.com/lit/ds/slus939b/slus939b.pdf

circuits that build up the same functionality combined with discrete components that are less susceptible to space radiation.
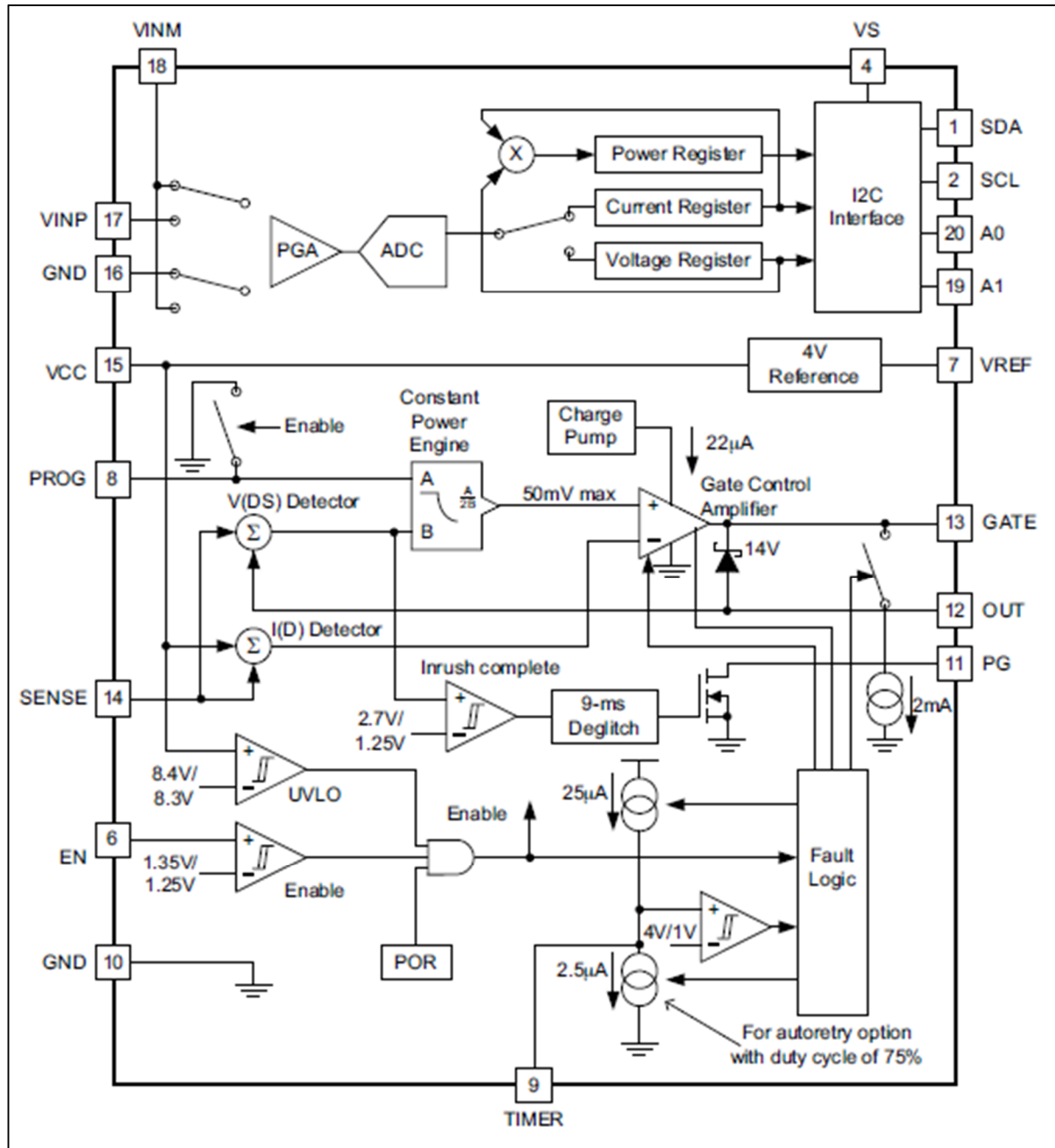
Figure 2-2: Functional block diagram of the TPS2480/1 current monitor

(Adapted from TPS2480/1 datasheet, 2010:7)

2.5.2 Low-Scale Integration Circuits

Examples of low-scale integration ICs that are relatively radiation tolerant are the LM324-N[5] operational amplifier (Op-Amp) and the LM139-N voltage comparators[6]. These low-scale ICs can be interfaced to discrete resistors and FETs to produce similar functionality as the large-scale integration application circuit of Figure 2-2. A typical application circuit using low-scale integration is depicted in Figure 2-3, where an Op-Amp and a voltage comparator are interfaced to a microcontroller (uC) for I^2C housekeeping.
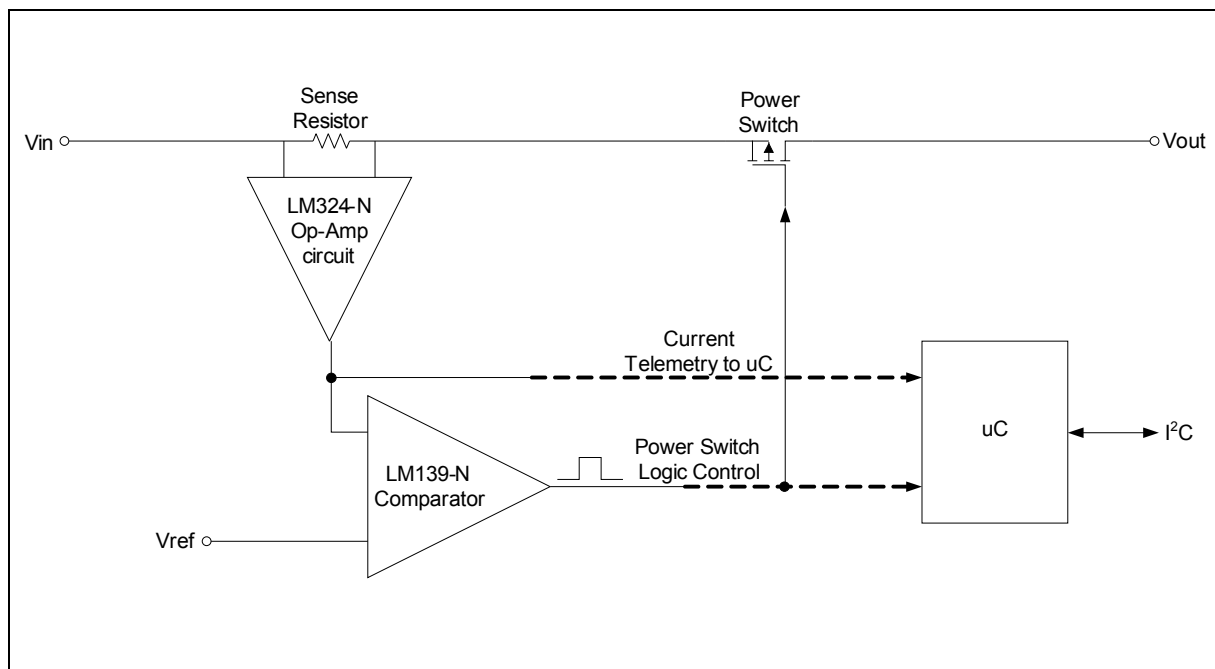
Figure 2-3: Application block diagram of low-scale integration circuit design for the PDM

2.5.2.1 Advantages: Reliability

Using a simplified circuit shown in Figure 2-3 is a more reliable design methodology. A single Op-Amp or comparator is less susceptible to space radiation than many incorporated into a single large-scale IC.

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[5] http://www.ti.com/lit/ds/symlink/lm124-n.pdf
[6] http://www.ti.com/lit/ds/symlink/lm339-n.pdf

2.5.2.2   Disadvantages: Bulky Circuitry

This design technique requires more components than using a single IC. As a result, the circuit design becomes bulky and heavier. However, the reliability and robustness of the PDM will be increased using this design methodology as compared to a single large-scale integrated component.

2.5.3   Logic Technology in Integrated Circuits

2.5.3.1   TTL Technology

TTL is a transistor dependent +5V logic family developed in 1965, rarely used in most recent logic ICs today (Godse & Bakshi, 2006:13). To cater for different environments, the TTL family was divided into two main series, namely the 54-series and the 74-series. The 54-series devices are qualified for a temperature range -55°C to +125°C, whereas the 74-series are qualified for a temperature range 0°C to +70°C (Maini, 2005:67).

2.5.3.2   CMOS Technology

The CMOS family is one of the families of logic circuits using metal–oxide–semiconductor field-effect transistors (MOSFETs). CMOS uses both n-channel and p-channel MOSFETS. CMOS ICs have the improved advantage of higher speeds, lower power dissipation and improved noise immunity over its TTL counterparts (Godse & Bakshi, 2006:43).

2.5.4   Optimum Circuit Topology

The design methodology for the PDM needs to be highly reliable as it will control the power supply to all the CubeSat subsystems. To optimise the reliability of the design, a combination of low-scale ICs and discrete components is a better solution as compared to a single large-scale IC. A single large-scale IC is more susceptible to radiation and a radiation attack on the IC could compromise functionality of the entire PDM.

However, low-scale ICs and discrete components need to be interfaced to a large-scale IC (microcontroller) for I^2C communication. As a suitable trade-off, using a combination of low-scale ICs rather than using a single TPS2480/1 high-scale IC is the optimum design solution. The 10-pin MAX9611[7] less integrated current monitor with 3 Op-Amps and one comparator is chosen. This is a CMOS device and the functional block diagram is shown in Figure 2-4, which internally features the Op-Amp and comparator circuits of Figure 2-3. The IC

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[7] http://datasheets.maximintegrated.com/en/ds/MAX9611-MAX9612.pdf

measures voltage, current and temperature. Furthermore, the IC features an internal analogue-to-digital converter (ADC) and an I²C interface for housekeeping commands from the OBC.
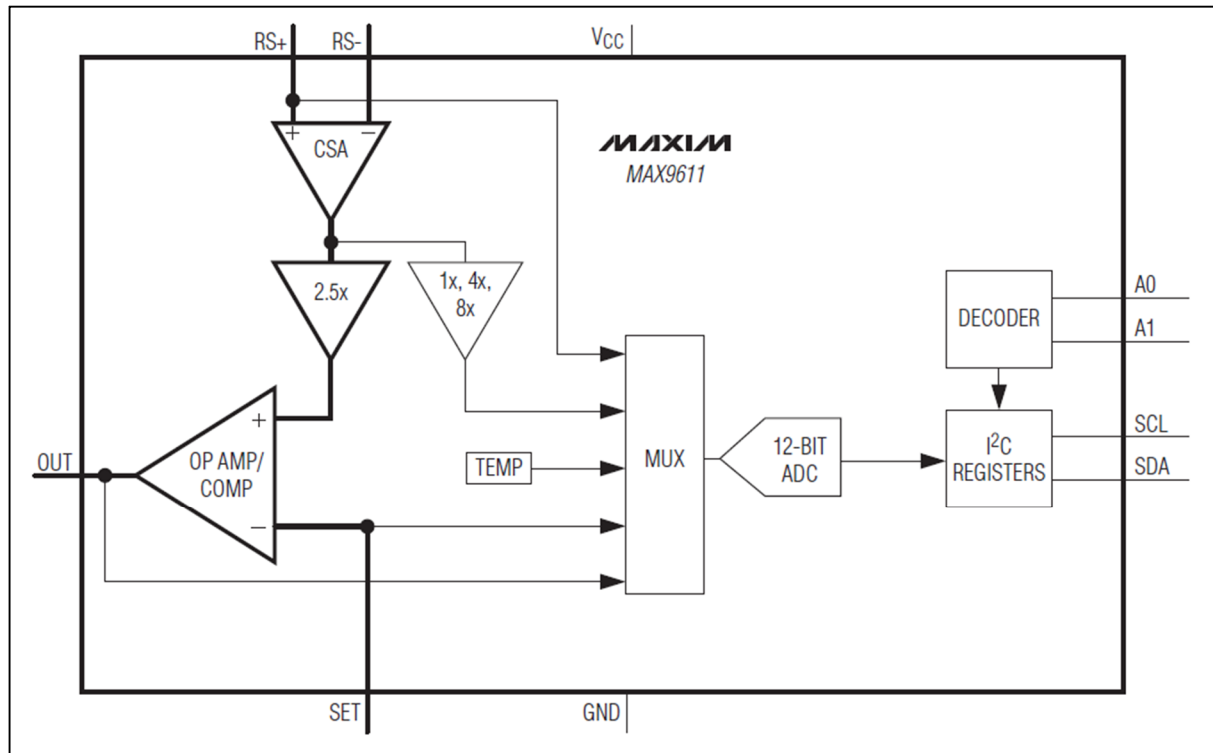
Figure 2-4: MAX9611 functional block diagram

(Adapted from MAX9611/2 datasheet, 2011:11)

2.6 TRADE STUDY 2: FAULT TOLERANCE AND REDUNDANCY

Fault tolerance is an important factor for satellites because failures occurring in space orbit cannot be directly fixed. Fault tolerance is considered to be a better technique than fault avoidance, as it has a wider failure mode spectrum, but more costly as more electronic components are required to build the electronic system (Larson & Wertz, 2005:777).

Redundancy is a technique used to build an electronic system to a certain level of fault tolerance, thereby defining the electronic system to have a predetermined scope of redundancy. Different techniques to implement redundancy are used to build a fault tolerant electronic system, which are precisely discussed in the next subsections.

2.6.1 Same Design Redundancy

Same design redundancy is used to protect the electronic system against random faults and possible components failures due to space radiation. For this technique, identical structures of the same circuit are built next to one another, with a switching circuit used to switch the normally inactive circuit on should the normally active circuit fail due to randomly unknown faults. Generally, same design redundancy refers to an increased number of the same design which can be interchanged to perform the same function for the same input and output (Laplante, 1999:538). For power distribution systems designs, inputs and outputs of identical distribution channels could be tied together to create a same design redundant system.

2.6.2 Diverse Design Redundancy

Diverse design redundancy is the cooperation of two or more different circuit designs which fulfil the same objective (output). Advantages of this redundancy technique is that it offers high system protection against random and design failures, whilst the disadvantages being addition of logistical costs of additional electronic components and test specifications required for each different design.

2.6.3 Functional Design Redundancy

Functional design redundancy is used for transient and intermittent failures. An example of this technique is using a gyro assembly for attitude determination and control of the CubeSat, and using a star sensor for navigation, such that if the gyro fails, it is still possible to simultaneously use the star sensor for attitude determination control and navigation. This type of redundancy may be seen as having a subsystem in the satellite performing its unique function whilst being a backup for another subsystem's function. An advantage of this type of redundancy is that the two subsystems are totally independent from each other, thereby limiting weight and costs of the satellite. One major disadvantage is that the backup system is usually less efficient as compared to the original system (Larson & Wertz, 2005:779).

2.6.4 Temporal Design Redundancy

Temporal redundancy is a retry technique used if the system in operation fails to give the required output. An advantage of this technique is the low cost implication involved, such that there is no need for another system to be built as backup. A disadvantage is that should

the active system be physically damaged due to radiation, heat or other harsh environmental conditions, the retry function will not solve the faulty condition (Larson & Wertz, 2005:779).

2.7 TRADE STUDY 3: POSSIBLE FAULTS IN POWER ELECTRONIC LOADS

Various electronic defects can be expected to cause faulty circuitry responses when the nanosatellite is in space orbit. This is primarily caused by the extreme temperature cycles and increased dose of radiation particles in the space environment. The final system prototype needs to be fault tolerant to a certain extent. Other environmental factors such as radiation can result in latchup conditions, over-currents, over-voltages and inrush currents to subsystem loads.

2.7.1 Inrush Currents

Inrush currents are very high instantaneous currents formed when a load circuit is powered. For example, the filament in a light bulb has very low "cold resistance" of ±9.5 Ω before being energised, and a "hot resistance" of about 144 Ω when operating at 100 % efficiency of its rated voltage (Mullin &Simmons, 2011:166).

2.7.2 Latchup

Latchup in CMOS devices is caused by latchup triggering faults, for example the radiation attack on the silicon controlled rectifier (SRC), resulting as a turn-on state or burn-out state of the device. When a latchup fault occurs, extremely high currents flow on that low resistance path, resulting in a malfunction or total damage of that current path (Ker & Hsu, 2009:1).

In satellite subsystems, latchup is commonly caused by radiation particles which strike a transistor in a CMOS device. The BJT becomes permanently turned-ON until a power reset state is triggered. If no reset condition is triggered, a large current flows through the transistor and as a result the circuit is damaged. It is therefore essential for the PDM design to include a current trip function to protect subsystem loads from inrush currents and faulty ON-states caused by latchup.

2.7.3 Over-currents, Over-voltages and Over-temperature Protection

The PDM is developed as a system to protect subsystem loads; therefore, it may also partially be referred to as a protection unit. It becomes essential for this protection system to be as robust and reliable as possible.

Power systems are designed to accommodate failure modes commonly referred to as electrical faults. A dead short circuit fault is a total fault and a metallic fault is a partial fault, where the entire load bypasses current through itself. The primary fault conditions in power systems are short circuit faults. Short circuit faults are due to failure of insulation, which amongst many other reasons may be caused by the following (Paithankar & Bhide, 2010:1-4):

- Over-voltages;
- High temperatures;
- Harsh environments.

To protect subsystem loads from over-currents, over-voltages and high temperatures, monitoring and protection circuits need to be implemented. The coordination of these circuits will together makeup a robust housekeeping segment within the distribution system. Good sensors are characterised by high-quality sensitivity, proper selectivity, fast response speed, reliability and dependability.

The PDM needs to be able to identify a certain fault correctly and isolate the corresponding circuit path. The PDM system also needs to have a fast response time to fault conditions. To prevent damage on the current path of that fault condition, the speed of isolation from fault is a critical criterion for power protection systems.

A protection system that is not reliable is generally useless. It has been found that simple, redundant systems which depend on local telemetry are more reliable and dependable than those depending on remote telemetry (Paithankar & Bhide, 2010:13-14). It is therefore recommended to apply simple engineering practices in the PDM design process to make the system more robust and dependable.

2.8   PROPOSED SOLUTION APPROACH

A power efficient, highly reliable and robust power distribution system is required. This solution should include fault protection circuitry to meet the main objective, which is to monitor and protect subsystem loads from power related faults. A power control technique is investigated, such that power switches may isolate subsystem loads from the power source in cases of over-voltages, latchup, over-currents or inrush currents to the subsystem loads. A proposed conceptual design is depicted in Figure 2-5, showing the input voltage busses from the EPS (12 V, 7.2-8.4 V battery bus, 5 V and 3.3 V), the I^2C bus from the OBC, power switches and the required minimum of eight power output channels.
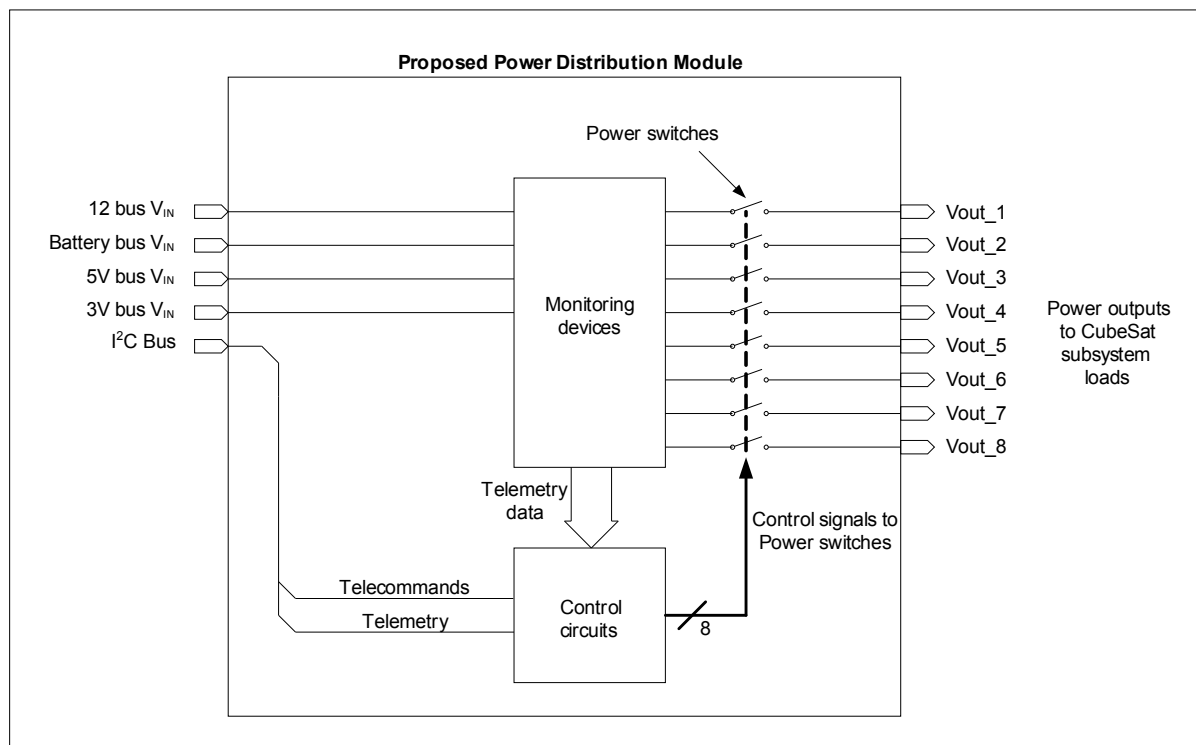
Figure 2-5: Conceptual design of the power distribution module

2.8.1   Power Monitoring Devices

The monitoring devices in Figure 2-5 are electronic sensors monitoring the instantaneous voltage, current and temperature measurements.

2.8.1.1 Current Sensor

A typical current sensor measures the voltage over a small sensing resistor. A low resistance value series (sense) resistor is selected to prevent undesirable loading effects. However, measurement accuracy may be compromised when using a very low resistance value in the sense that the voltage drop across the sense resistor becomes as low as the offset voltage of analogue conditioned circuits (Zhen, 2010:1-2). The MAX9611 current sensor from Maxim[8] is chosen for the PDM prototype development.

There are two common techniques of integrating a current sensor into a circuit with a load, namely high-side and low-side current sensing as shown in Figure 2.6(a) and Figure 2.6(b), respectively (as taken from Zhen, 2010:3). High-side current sensing has the advantages of no ground disturbances; the load is safely connected directly to ground and latchup can be detected. Disadvantages are that the circuits should handle very high common mode input voltages; more complex circuits and higher costs. Low-side current sensing has the advantages of low input common mode voltage; a ground referenced input and output; simplicity and low cost. Disadvantages are the load is no longer grounded; latchup and ground disturbances can damage the load (Zhen, 2010:2).

The current sensor should be chosen according to general electronic component characteristic requirements for CubeSat applications, which are low power consumption, small size, low mass and reliability. Considering the solution approach discussed in the previous chapter, the current sensor measurement data needs to be interfaced to an I^2C bus to send the telemetry to the OBC to enable housekeeping decisions that are made according to the telemetry received.

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[8] http://datasheets.maximintegrated.com/en/ds/MAX9611-MAX9612.pdf
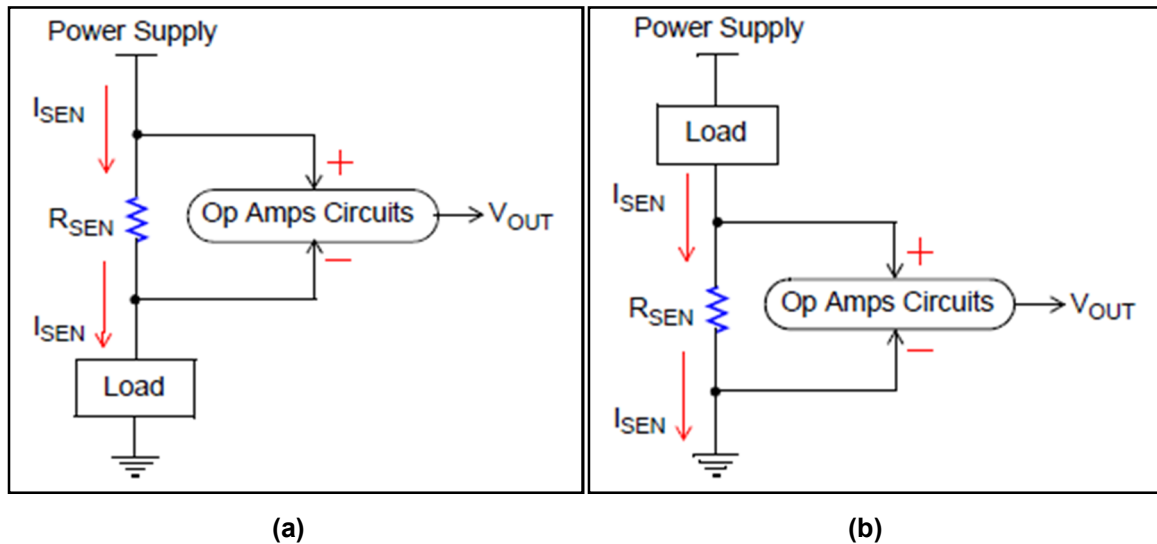
Figure 2-6: Current sensing using Op Amps (a) High-side current sensing, (b) Low-side current sensing

(From Zhen, 2010:3)

2.8.1.2 Voltage Sensor

Most sensors generally fall under two categories, namely reference voltage sensors or voltage generating sensors. Reference voltage sensors output a voltage signal equal to the change of voltage from a referenced voltage. Voltage generating sensors produce a varying voltage signal which corresponds to the change of condition being sensed (Erjavec, 2005:68). The simplest type of voltage sensor is a resistive divider which outputs a voltage that is proportional to the input. For voltage measurements, the MAX9611 current sensor is used as it features internally high-side voltage measurement.

2.8.1.3 Temperature Sensor

Temperature sensors, also known as temperature transducers, convert the measured temperature to a corresponding voltage (Richard & James, 2010:42-44). Temperature sensing is the process whereby a contact temperature sensor is fixed to an object and a small portion of the object's thermal energy flows to the sensor as heat. The signal from the sensor is processed and converted to the measured temperature (Fraden, 2010:519).

Two basic methods of signal processing are implemented on contact temperature sensors, namely equilibrium and predictive signal processing. With equilibrium signal processing, the contact temperature sensor and the object under temperature measurement reach an equilibrium thermal energy level, resulting in a rise or drop until equilibrium is reached. This may take a few seconds or minutes according to the rate of thermal coupling of that contact

sensor. Using the predictive signal processing method, "the equilibrium level is anticipated via a computation through the rate of the sensor's temperature change" (Fraden, 2010:519-520). For temperature measurements, the MAX9611 current sensor is used as it also features an internal temperature sensor.

2.8.2 Power Control Circuits

Power control circuits are generally required to control power isolation by tripping and resetting a power switch as shown in Figure 2-7. Three command signals are proposed, namely a hardware trip, software trip and a software override signal also shown in Figure 2-7. The hardware trip signal will execute an autonomous trip command. The software trip signal is a diverse design redundant circuit (discussed in section 2.6.2) to perform the same trip command from a different circuit. The software override command will override all trip commands and force a reset condition. This is a functional redundant design (discussed in section 2.6.3) which should ensure the PDM system is operational when faulty conditions within it cannot be cleared, such as continuous hardware tripping.
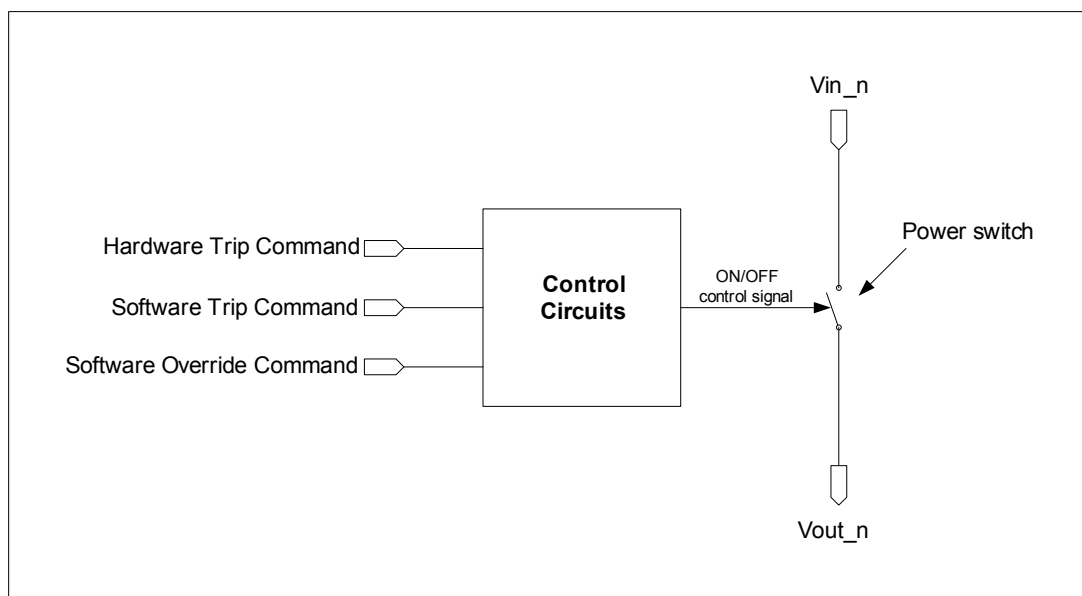
Figure 2-7: Proposed power switch control input signals to control circuits

The power switch on each power distribution channel plays a critical role such that failure of the power switch may result in a subsystem load permanently switched off. Electronic components used for power systems are generally designed for non-faulty operation, such that when faulty conditions occur it is essential to isolate the faulty sections of the power

network from the healthy sections in order to avoid faulty over-currents and over-voltages adversely affecting the healthy sections. A comparative survey of switches is presented here, critically focussed on switches characterised by low power demand, fast switching times, small size and low mass. The selected switch must further isolate power reliably, be self-maintainable in orbit, and have a minimum voltage drop across it.

2.8.2.1   BJT versus FET as Power Switch

Bipolar junction transistors (BJTs) and field-effect-transistors (FETs) are mostly used where fast and reliable switching applications are required, hence are considered for the PDM design. Table 2-2 (Salivahanan, Kumar & Vallavaraj, 2008:205-206) highlights a general comparison between the BJT and the FET, and provides a selection guideline to select the appropriate device for the PDM power switch implementation.

According to Table 2-2, BJTs are noisier than FETs. FET's are easier to control because they are voltage controlled, unlike BJTs which are current controlled. Suitable for space applications, FETs can tolerate higher levels of radiation and their performance is less affected by external temperature effects. Although BJTs are generally cheaper, FETs are more reliable in the space environment, require simpler drive circuits and can switch faster than BJTs. Subsequent to this argument, FETs are found to be more suitable than BJTs for the power switch application.

Table 2-2: Comparison of BJT vs FET for power switch selection

Characteristic	BJT	FET
Noise	Noisy.	Less noisy. FETs have no bi-polar junctions; conduction through only n-type or p-type semiconductor material.
Input impedance	Low input impedance because its input is forward biased.	Can act as an excellent buffer amplifier because of its high input impedance.
Device control	Current controlled device.	Voltage controlled device, can be easily monitored.
Space	Occupy more space.	Easier to fabricate & suitable for ICs, less space occupied.
Radiation	Performance degrades due to neutron radiation because of reduction in minority-carrier lifetime.	Not reliant on minority carriers for operation, hence can tolerate higher level of radiation.
Temperature	Has positive temperature coefficient at high current levels, leading to thermal breakdown.	Has negative temperature coefficient at high current levels, thus performance less affected by ambient temperature changes.
Speed & frequency	Lower switching speed and cut-off frequency; suffers from minority carrier storage effects.	Higher switching speed and cut-off frequencies because device does not suffer from minority carrier storage effects.
Distortion	Noisy characteristic can cause signal distortion.	Low gain bandwidth product produces more signal distortion except for small signal operation.
Cost	Cheaper to produce.	More expensive to produce than BJTs.
Drive circuits	Normally requires more circuitry.	Simpler drive circuits.

2.8.2.2 Comparison of FETs

The MOSFET and the junction field effect transistor (JFET) are widely used as switching devices for power control applications, and also in DC-DC converters in space power systems. Table 2-3 lists a comparison of the two types, highlighting advantages and disadvantages of each according to selective characteristics which can influence the PDM system operation (Salivahanan *et al.*, 2008:210-211).

Table 2-3: Comparison of JFET and MOSFET for power switch selection

Characteristic	JFET	MOSFET
Input impedance	Lower, of the order $10^8\,\Omega$.	Very high, of the order $10^{10}\,\Omega$ to $10^{15}\,\Omega$, hence can act as a better buffer.
Drain resistance	Higher, ranging from 0.1 Ω to 1 MΩ.	Lower, ranging from 1 Ω to 50 kΩ.
Operation mode	Can be operated in only depletion mode.	Can be operated in both depletion and enhancement modes.
Symmetry	Non-symmetrical device.	Symmetrical device, source and drain can be interchanged which makes this device good for analogue switching applications.
CMOS advantages	Not as widely used as MOSFETs.	Widely used in very-large-scale-integration (VLSI) digital circuits.
ON resistance	Higher as compared to MOSFETs.	Lower as compared to JFET.
Drive circuits	Require more circuit components.	Simpler input-drive circuits.
Failure mode	Open circuit.	Closed circuit.

MOSFETs have negative temperature coefficient of carrier mobility which reduces the risk of thermal runaway, destructive breakdown in the transistor and less power demand. MOSFETs further have a closed-circuit failure mode, which makes it highly reliable for the PDM application because this suggests that a subsystem load will not be power-cut in case the power MOSFET fails completely whilst in space orbit (Shenai, Galloway &Schrimpf, 2004:1-5).

With reference to the above advantages of the MOSFETs over JFETs and BJTs, the power MOSFETs would be best suitable for the PDM power switch application. Power MOSFETs show higher reliability based on the comparisons listed in this section. Therefore, an n-channel or p-channel MOSFET will be used in the PDM design in chapter three.

2.8.3   Power Distribution and Switching

The PDM will distribute eight power channels instead of only the three power channels provided by the Clyde Space EPS. A user of the PDM system will be able to select the current path rating, current trip point and voltage bus required. Voltage busses will flexibly be

changed at build time to switch an output channel to any of the available input voltage busses from the EPS.

2.9   SUMMARY

The space environment is characterised by harsh conditions, such as high temperatures, vacuum and radiation sources. Two categories of radiation tests are known to be performed on electronic devices to qualify a device for space applications, namely total ionising dose and single-event effects (SEEs) irradiation. Electronic devices used for nanosatellite applications are generally required to be small in size and mass due to the space and weight limitations on a small nanosatellite. In addition, the devices should be heat tolerant and have a slow derating factor to last longer in space orbit. Space electronic circuits are normally designed with redundancy because of the inability to repair circuits whilst the nanosatellite is in space orbit. Possible electrical faults in power electronics loads, such as inrush currents, latchup, over-currents, over-voltages and over temperatures should be considered when designing power systems for satellites because failure of the power subsystem may result in other subsystems permanently disabled. Subsequent to the research studies presented here, a solution approach towards the development of an efficient and highly reliable PDM is presented in this chapter, where all elements of the conceptual proposed system in chapter 1 are clearly identified. The design, simulations and prototype development follows in chapter 3.

CHAPTER 3:   MODULE DESIGN AND PROTOTYPING

3.1   INTRODUCTION

In this chapter, all elements of the power distribution module (PDM) proposed in the previous chapters are simulated using LT-Spice[9]. Accordingly, the design is divided into the three subsections, namely monitoring, control and switching. Each subsection of the design is simulated and components are selected for prototyping. The printed circuit board (PCB) design, prototyping and component population follow. A populated prototype of the PDM is tested and verified in chapter 4.

3.2   MODULE DESIGN OVERVIEW

The PDM system block diagram design is depicted in Figure 3-1. The PDM will comprise of eight trip circuits on each power channel, each having the option to connect to one of four input voltage busses at manufacturing time. The fourth input bus to the PDM is placed according to requirements by the F'SATI technical team, anticipating that an additional 12V bus will be created for future CubeSat electrical power supply (EPS) designs. The input voltage busses to the PDM are shown in Figure 3-1 as "12V bus V_{IN}", "Battery bus V_{IN}", "5V bus V_{IN}" and "3V bus V_{IN}". The design further shows the eight output power channels listed as "Vout_1" to "Vout_8". This design should allow subsystem loads to be configured to more than one output channel as required.

Current, temperature and voltage sensors are intended to provide telemetry to the OBC, thereby allowing the OBC to trigger power trip switch in cases of faulty conditions. A shown in Figure 3-1, the control circuitry will accept software trip and override signals to control the power switch. The current sensors will automatically generate a hardware trip signal when over-current conditions are measured.

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[9] http://www.linear.com/designtools/software/#LTspice
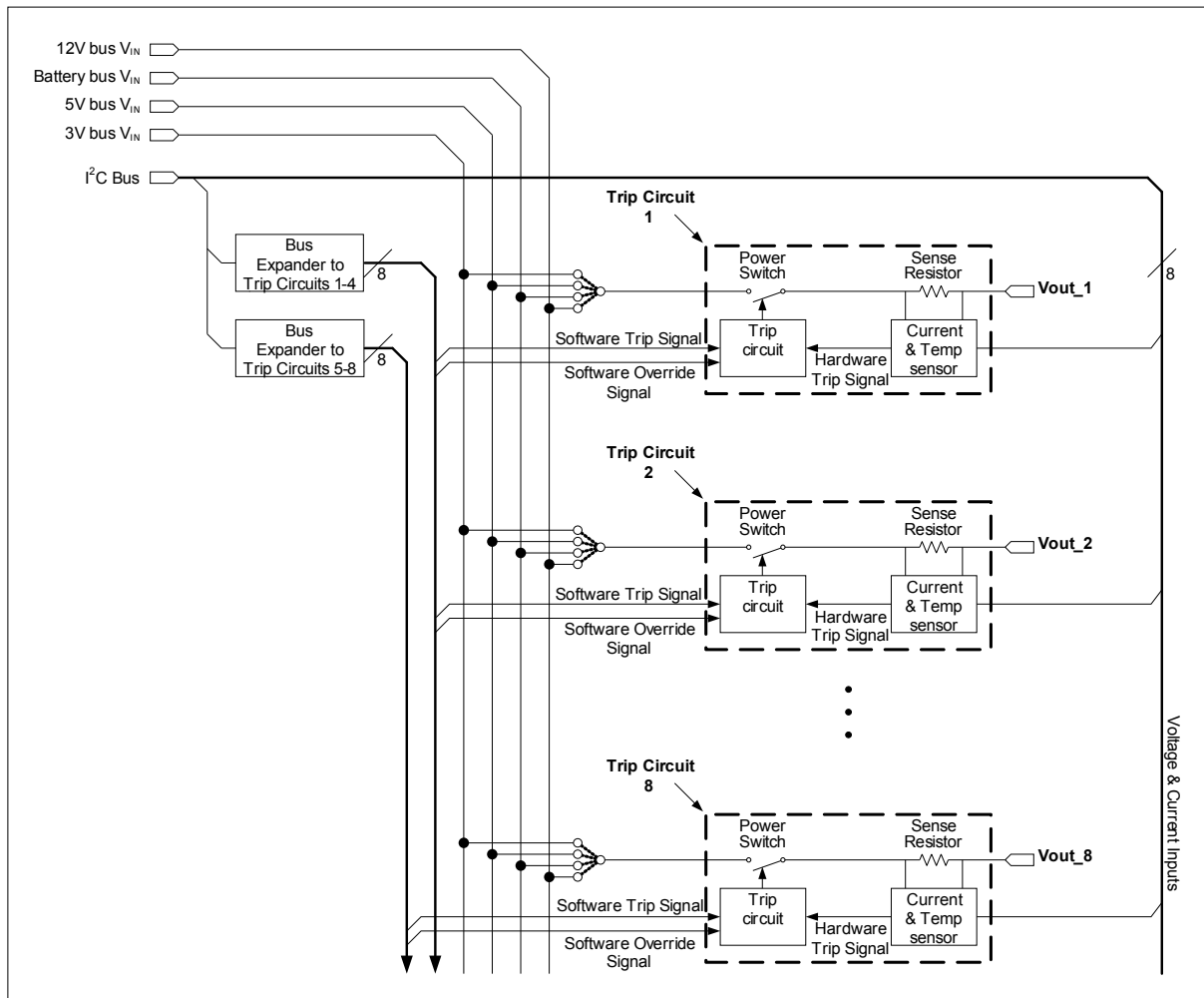
Figure 3-1: Block diagram showing overall layout of the PDM power channels

An I²C bus will interface with two I²C expanders as shown in Figure 3-1. The I²C expanders will carry out all software commands, namely software trip and software override. One I²C expander will carry out software commands to control circuits in power channels 1 to 4, and the second I²C expander to control circuits in power channels 5 to 8.

3.3   POWER MONITORING DESIGN

In this section, all suitable monitoring devices are selected. Components are also selected with reference to the trade studies carried out in chapter 2, which covered logic design physics, fault tolerance and devices suitable for satellite applications.

3.3.1 Current Monitoring

The MAX9611[10] current sensor from Maxim is selected. The current sensor was available since early 2011. The current sensor is a smart 10-pin IC, and is found to be most suitable for the PDM application. The current sensor has the following features that conform with the PDM application:

- Supports I²C communication protocol;
- 12 bit internal analogue to digital converter;
- Has a built in temperature sensor;
- Provides digital current, temperature and voltage telemetry via I²C;
- Allows up to 16 of these devices on the PDM board.

The selected current sensor is highly advantageous because it can easily be interfaced to the OBC via the I²C communication without the need for extra interfacing ADCs or microcontrollers. The sensor will also provide all required telemetry. A typical current monitoring circuit using the MAX9611 integrated circuit (IC) is shown in Figure 3-2 (taken from MAX9611 datasheet), where the IC is used to limit inrush currents to a load.
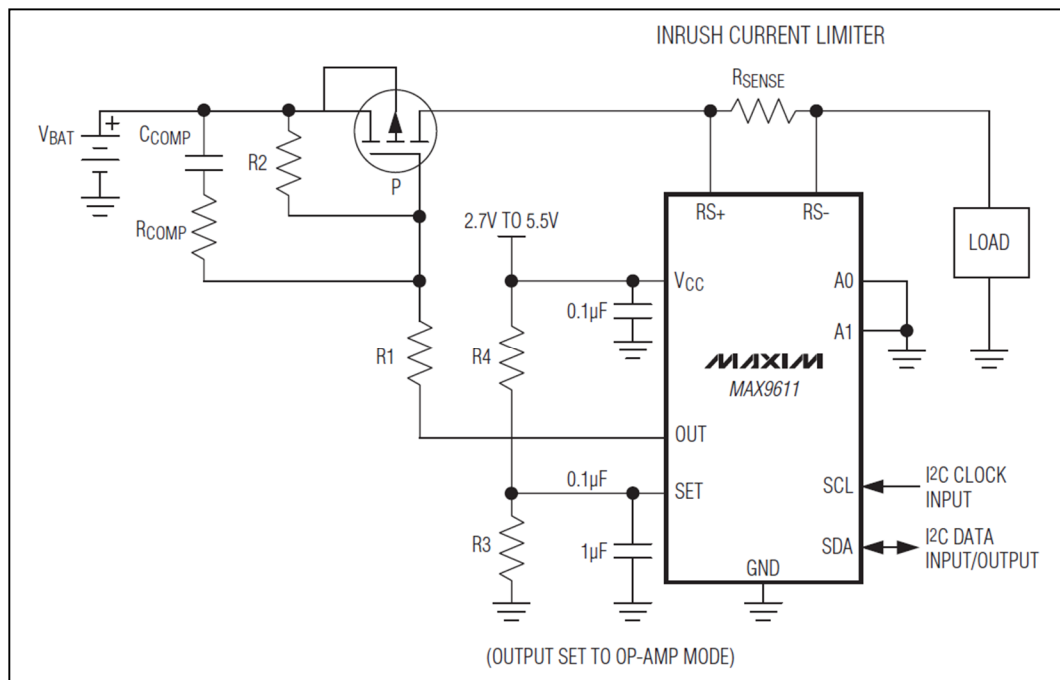
Figure 3-2: Current monitoring circuit where the inrush current limiter can easily be changed to a high-side relay disconnect circuit using the MAX9611 sensor set to comparator mode

(From MAX9611 datasheet, 2011:17)

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[10] http://datasheets.maximintegrated.com/en/ds/MAX9611-MAX9612.pdf

The inrush current limiter shown in Figure 3-2 can easily be coded to respond as a trip circuit when programmed to function in comparator mode. In this mode, the output pin (OUT in Figure 3-2) will latch high when the sensed current exceeds the current threshold (SET), pre-set by resistors R3 and R4 in Figure 3-2. Connecting this device in parallel with a sense resistor as shown by the "Current & Temp sensor" block in Figure 3-1, all telemetry will be achieved via I²C and a hardware trip command will be executed by the OUT pin in Figure 3-2. OUT latches high to trip a p-channel MOSFET. To recap from chapter 2 (section 2.8.2.1), it was shown that the best choice for the power switch application would be a power MOSFET. As to whether to use a p-channel or an n-channel MOSFET, the choice is guided by the best suitable design. Seeing that the circuit used in Figure 3-2 controls a p-channel MOSFET, the rest of the control circuitry will be designed to control a p-channel MOSFET.

An internal amplifier in the current sensor can be programmed to voltage gains of 1x, 4x or 8x which outputs a full-scale voltage proportional to the sensed voltage of 440mV, 110mV and 55mV, respectively. The R-0603 surface mount package resistors are already set as a standard package to be used by the F'SATI technical team. The smallest value for sense resistors which could be found from RS-components in the R-0603 package was 0.1Ω. Using two 0.1Ω resistors in parallel, the effective resistance of the sense resistor (R_{sense}) is 0.05Ω, thereby achieving lower voltage drop. To use the highest full-scale sensed voltage of 440mV for higher precision, the highest current that can be measured is:

$$I_{sense} = \frac{V}{R_{sense}} = \frac{0.44}{0.05} = 8.8 \, \text{A}$$

Equation 3.1

This value exceeds the expected maximum current from the power supply. The voltage drop across the effective sense resistance (V_{drop}) may be calculated according to the voltage bus connected to the input channel of the PDM. For example, if the input is connected to the 5 V bus (V_{in} = 5 V) with an expected 1 A current flow, the voltage drop is calculated using Equation 3.2:

$$V_{drop} = I_{sense} \times R_{sense} = 1 \times (0.05) = 50 \, \text{mV}$$

Equation 3.2

With a voltage drop of 50mV, the output voltage to a subsystem load connected to the 5 V bus will then be 4.95 V.

It is evident that the voltage drop across the sense resistor is very small. It could also be suggested that it is so small that it is worth the compromise to use a PDM system which drops the voltage by 0.05V but offers a very high level of reliability, power control and protection to subsystem loads.

3.3.2 Voltage and Temperature Monitoring

The MAX9611 current sensor also features an internal die temperature sensor, which can measure temperatures in the range -40°C to +125°C with a 0.5°C resolution. Die temperature from this sensor can be used for thermal monitoring (Maxim, 2011:12). The MAX9611 sensor is found suitable because temperature ranges fall within the expected temperature range for low Earth orbit mission, typically from -25°C to 70°C.

The MAX9611 also has an internal current-sense precision amplifier. The amplifier can tolerate 0 V to 60 V input common-mode voltage (Maxim, 2012:12). The input sense voltage (V_{in}), which is the input voltage from the electrical power supply (EPS) to the PDM, can be measured using this sensor.

3.4 POWER CONTROL DESIGN

The control subsection of the PDM is based on controlling the power switch to be ON or OFF. It was decided, with reference to the trip circuit shown in Figure 3-2, that a p-channel MOSFET shall be used because the MAX9611 OUT pin remains LOW and latches HIGH when over-current states are detected. A p-channel power MOSFET is ON when the gate voltage is LOW, and the switch is OFF when the gate voltage is HIGH. The p-channel power MOSFET is also known to be easier and cheaper to produce.

The IRF9328 p-channel MOSFET shown in Figure 3-3 is selected. The MOSFET is a small size SO-8 surface mount package. It is rated to 30 V which exceeds the EPS voltage range and the highest voltage in the PDM of 12 V.
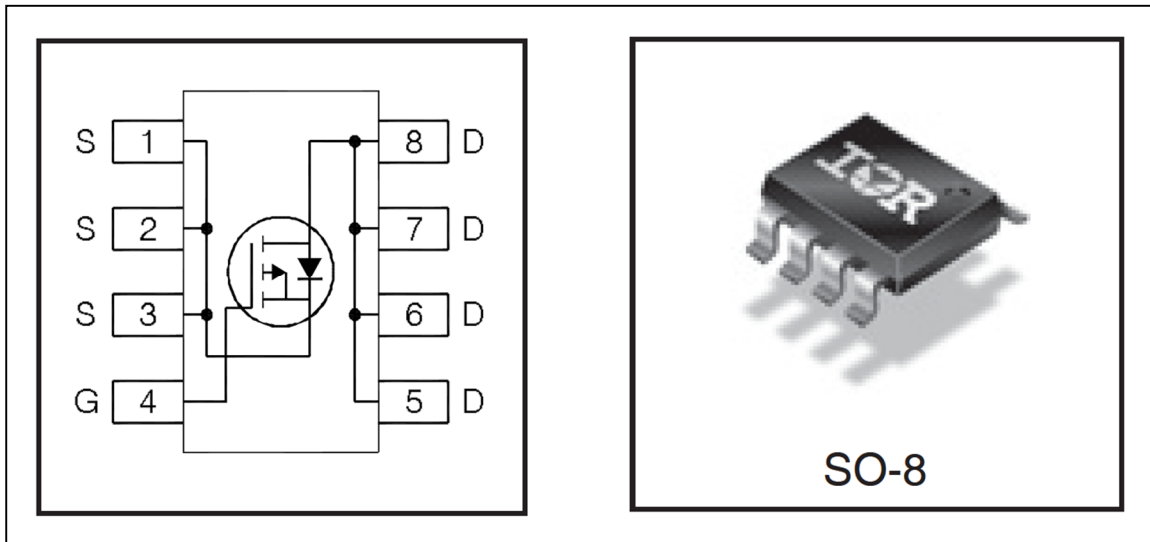
Figure 3-3: IRF9328 p-channel power MOSFET used as the power switch for each PDM power switch

(From International Rectifier, 2010:1)

The IRF9328 power MOSFET is a suitable choice for the power switch application of the PDM system. All electrical specifications listed in chapter one (section 1.6.4) can be tolerated by this power MOSFET.

The electrical characteristics of the IRF9328 are summarised in Table 3-1 (International Rectifier, 2010:1). The MOSFET has a very low on-resistance ($R_{DS(on)}$) of maximum 19.7 mΩ and a 12 A rating.

Table 3-1: Maximum ratings of the IRF9328 p-channel MOSFET

Parameter	Value	Unit
V_{DS}	-30	V
$R_{DS(on) max}$ (@V_{GS}= -10V)	11.9	mΩ
$R_{DS(on) max}$ (@V_{GS}= -4.5V)	19.7	mΩ
$Q_{g (typical)}$	18	nC
I_D (@ T_A = 25°C)	-12	A

3.4.1 Logical Flow of the Control Circuit Design

Command signals commanding the power switch (p-channel MOSFET switch) should be logic signals, where 5 V gives a logic-HIGH ("1") and 0 V gives a logic-LOW ("0"). An OR-gate provides a control signal to the MOSFET based on the input signals, software_trip and hardware_trip.

As shown in Table 3-2, if any of the trip signals are commanded (HIGH), the p-channel MOSFET gate voltage is pulled HIGH and the MOSFET switch is turned OFF, thereby tripping the current path.

Table 3-2: OR-gate truth table representation of trip commands to power switch

Input A (software_trip)	Input B (hardware_trip)	OUT (Gate Voltage)	P-channel MOSFET
0	0	0	**ON**
0	1	1	**OFF**
1	0	1	**OFF**
1	1	1	**OFF**

It is required that an override command (logic HIGH) forces the p-channel power switch to turn ON when required, thereby overriding all trip commands. The necessity to have an override command is to enable a forced reset condition, such that if the hardware trip malfunctions in such a way that it keeps tripping the power switch unnecessarily, a forced-ON state may be commanded by an override command.

The addition of extra logic to drive the power switch is necessary, herein referred to as "Drive Logic" in Figure 3-4. A complete logical flow showing all three commands is shown in Figure 3-4, where the output of the OR-gate will now be one of the inputs to the Drive Logic. The second input to the Drive Logic will be the override command, shown as software_override in Figure 3-4.
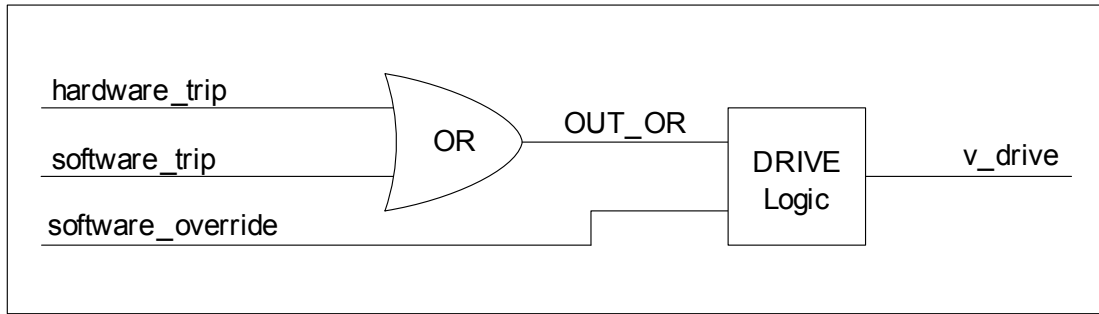
Figure 3-4: Logic gate representation of control signals driving the power switch

Table 3-3 defines the required combined logic of the complete control circuit. A single logic gate could not be found which can execute the output requirements of the Drive Logic, v_drive in Table 3-3. In the following subsections the complete Drive Logic is designed using BJT transistors to execute an output which corresponds to the v_drive output according to Table 3-3.

Table 3-3: Control logic configuration of an OR-gate trip output and an override signal

Drive Logic-gate			v_drive	P-channel MOSFET
State	OUT_OR	software_override		
1	0	0	0	**ON**
2	0	1	0	**ON**
3	1	0	1	**OFF**
4	1	1	0	**ON**

Table 3-3 is explained as follows:

- State 1: There are no trip signal commands (OUT_OR is LOW) and no override command (software_override is LOW). Therefore, no fault conditions are detected and the power channel is in normal operation, hence, the p-channel MOSFET switch is ON.

- Sate 2: OUT_OR remains unchanged compared to State 1, but software_override goes HIGH, which means the p-channel MOSFET is forced to be turned ON, hence, remains ON as before.

- State 3: OUT_OR switches HIGH, which means a fault condition has been detected and either hardware_trip or software_trip is tripping the MOSFET switch. Since software_override is LOW, the MOSFET switch tripped into an OFF state, thereby cutting the current path.
- State 4: OUT_OR remains unchanged compared to State 3, but software_override switches HIGH, meaning an override command is executed, thereby overriding all software trip commands and forcing the switch to turn ON.

3.4.2   Trip Control Circuit Design

The simplest solution would be to use an OR-gate IC to execute the trip commands. However, traditional switching circuits using bipolar junction transistors (BJTs) have shown to be highly reliable in previous satellite missions because BJTs have high tolerance to radiation sources which are likely to cause single event upsets (SEU) in ICs. The resistor-transistor logic (RTL) is considered here due to its primary advantage of using very few transistors to construct a digital logic circuit, as shown in Figure 3-5.
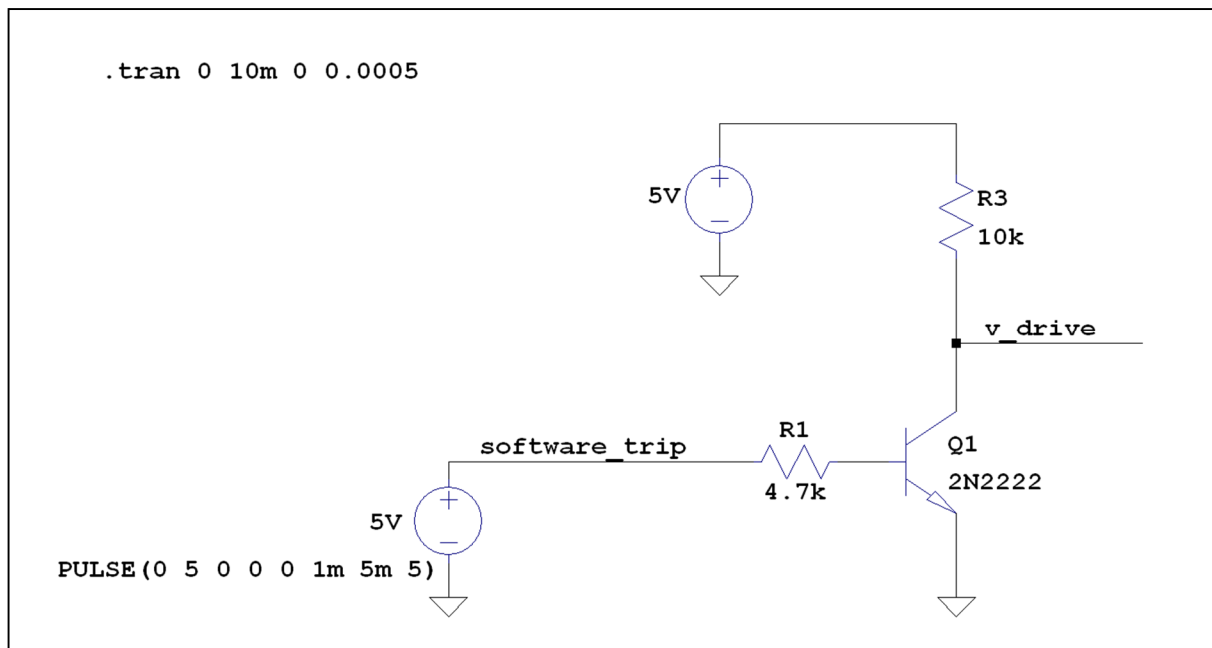
Figure 3-5: P-Spice circuit schematic of a single software_trip signal applied to the base of a BJT where the collector output (v_drive) will be used to drive a p-channel MOSFET

First, the switching control behaviour of a BJT transistor using RTL logic is studied. In the best case scenario, it is required that the logic signals be 0 V for a logic-LOW and 5 V for a logic-HIGH, so that the p-channel MOSFET may be switch hard ON and hard OFF. To achieve this, the collector of the BJT is pulled to the 5 V by R3 in Figure 3-5. A 5 V control signal (software_trip) is applied to the base of the transistor via the series resistor R1. Taking the output (v_drive) at the collector as an open collector configuration, it shall be observed that the output is HIGH (5 V) when the v_trip is LOW (0 V). Vice versa, the output (v_drive) will go LOW (0 V) when the software_trip is HIGH (5 V). The circuit in Figure 3-5 is simulated using LT-Space and the simulation plots are verified correct as shown in Figure 3-6
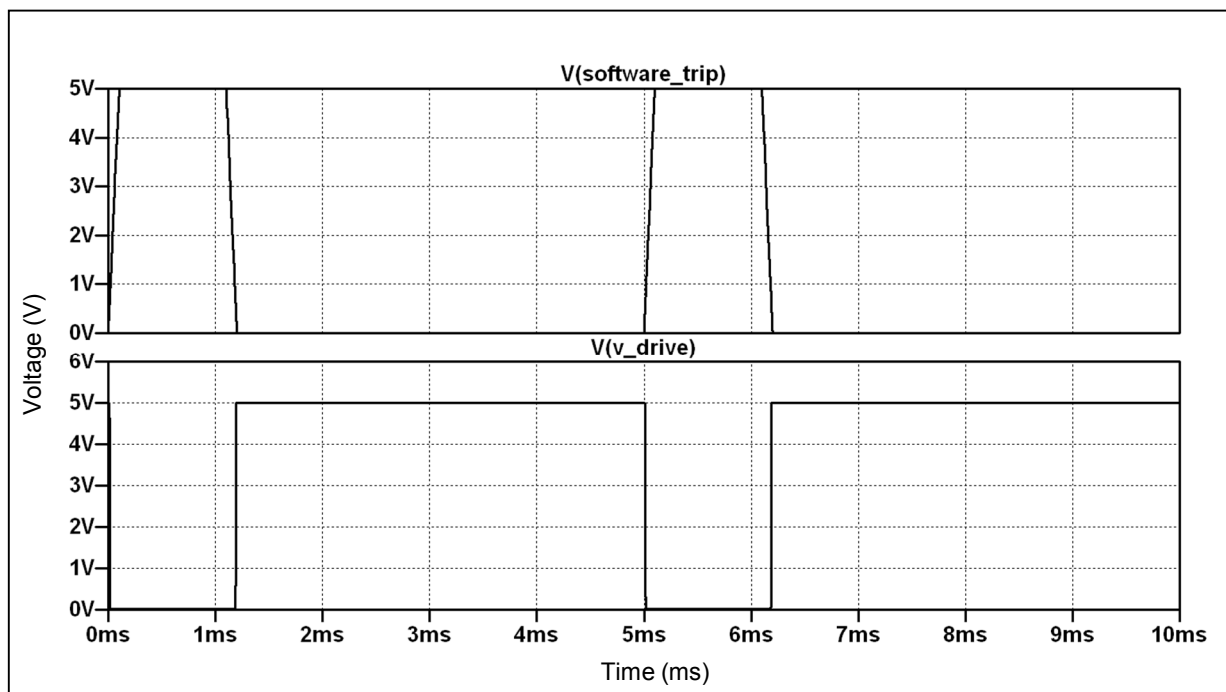
Figure 3-6: Simulated voltage waveform of the trip signal circuit applied to base of transistor for power switch control (Figure 3.5)

With reference to Table 3-3, where the logic drive functions are defined, it is required that the drive logic (v_drive) should switch to a logic HIGH when either trip signal switches HIGH. Therefore, with the configuration in Figure 3-5, this condition is not satisfied. To satisfy the drive logic requirements, the circuit shown in Figure 3.5 is modified by adding a pnp BJT (Q2 in Figure 3-7) to the circuit, which inverts v_drive. Both trip signals (software_trip and hardware_trip) are now added as inputs to the control circuit; v_drive remains the output as before. The configuration is shown in Figure 3-7.

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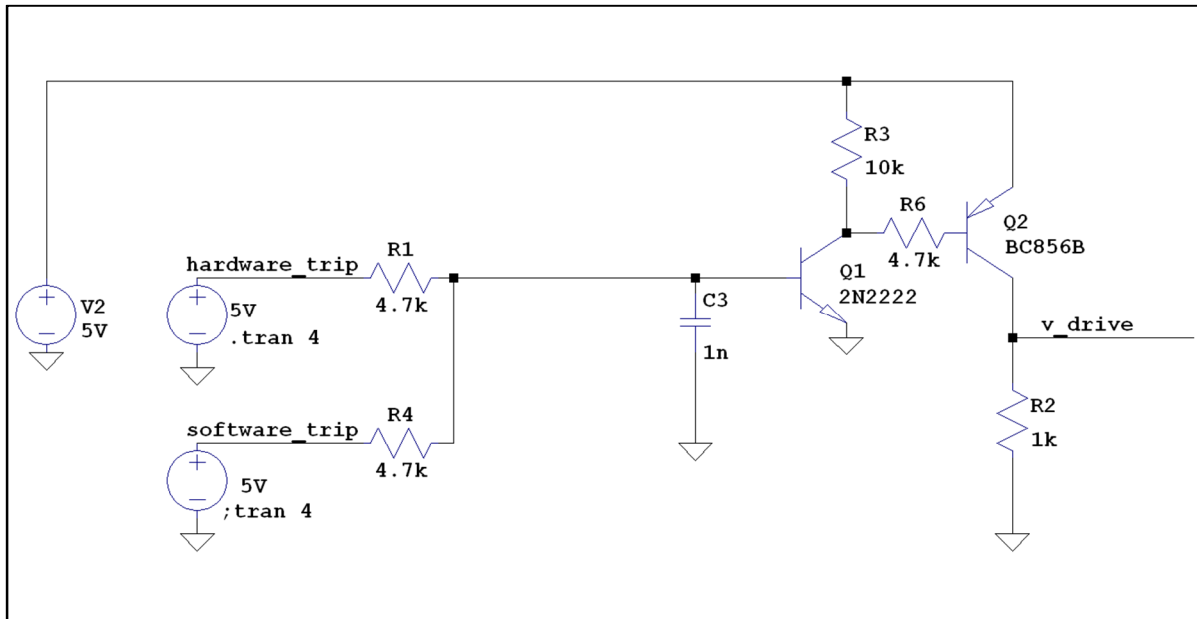
Figure 3-7: P-Spice trip-only circuit schematic showing input trip signals to the drive signal to control a p-channel MOSFET

The hardware_trip command will be the OUT pin from MAX9611 current sensor, which latches HIGH when an over-current condition is detected. The MAX9611 current sensor is a CMOS device; hence the logic HIGH and logic LOW voltage levels will be 5 V and 0 V, respectively, as required. The software_trip and software_override commands will be commanded from an I^2C controllable switch (ADG715), where one side of the switch is connected to 5 V and the other side is the control signals software_trip and software_override. This shall later be seen when the ADG715 I^2C controllable switch is introduced.

The control circuit diagram shown in Figure 3-7 is simulated using LT-Spice. The simulation plots are shown in Figure 3-8. From an initial time t = 0s, the plots are explained as follows:

- At time 0 s to 0.5 s, there are no trip signals and v_drive is at 0 V. Therefore, the p-channel MOSFET connected to v_drive will remain in the ON state.
- At time 0.5 s, hardware_trip is executed. As the hardware_trip signal rises above 0.7 V, npn transistor Q1 in Figure 3-7 turns ON, thereby turning ON pnp transistor Q2 through resistor R6, and v_drive is pulled HIGH to 5 V and a p-channel MOSFET connected to v_drive will be turned OFF.
- At time 0.9 s, hardware_trip signal is switched OFF. As the hardware_trip signal drops below 0.7 V, the npn transistor Q1 in Figure 3-7 turns OFF, thereby turning

OFF pnp transistor Q2 and pulling v_drive LOW to ground via resistor R2. As a result, a p-channel MOSFET connected to v_drive will be turned ON again.

- Software_trip command is executed between 1.5 s and 2 s. A p-channel MOSFET connected to v_drive will be switched OFF and ON again as before.

- Again Software_trip command is executed again between 2.5 s and 3.5 s; as a result v_drive goes HIGH.

- Between 3 s and 3.5 s, both trip signals are executed simultaneously and v_drive stays HIGH as required.
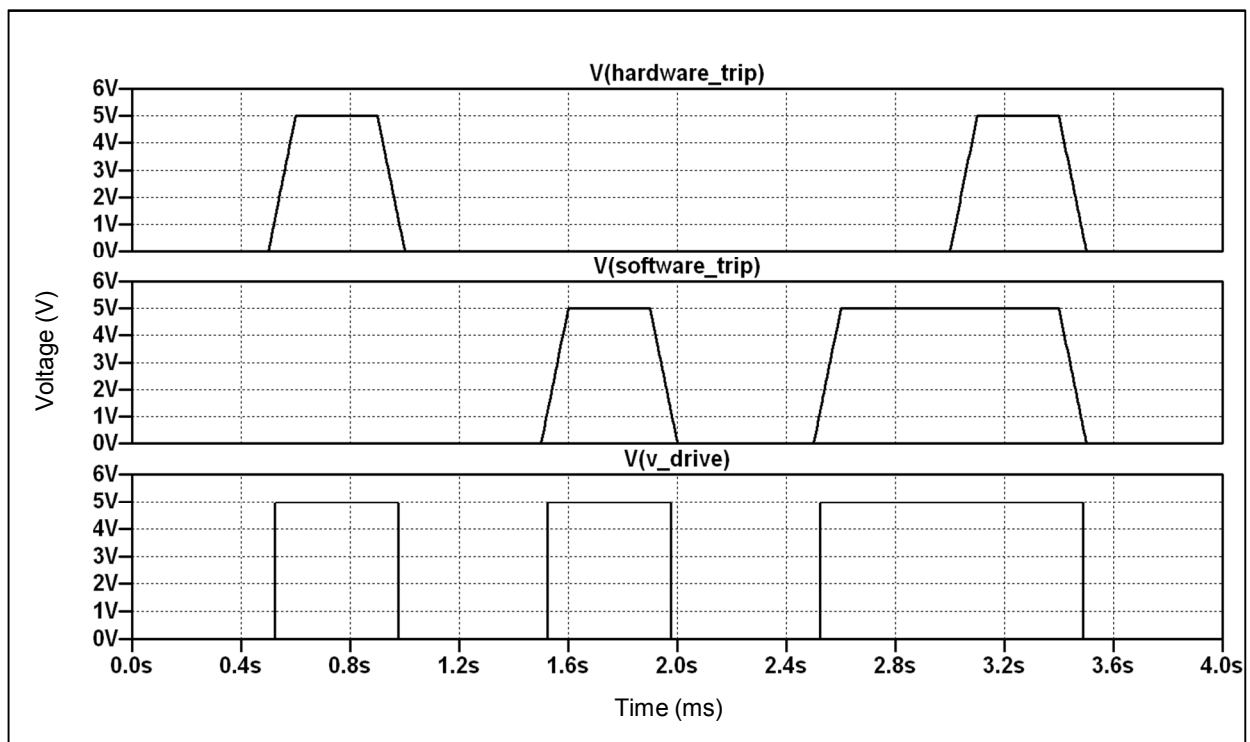
Figure 3-8: Voltage output waveforms for trip-only control circuit shown in Figure 3.7

At this stage it is observed that the trip control functions have been successfully designed and verified through simulation. Both hardware_trip and software_trip commands execute the desired v_drive output to drive the p-channel MOSFET power switch. However, the control circuit is not complete because the override command (software_override) has not been included in the design up to this stage. In the following subsection, extra logic circuitry for the software_override command is added to the control circuit design of Figure 3-7 and simulated in LT-Spice. A p-channel MOSFET switch is also added to the design. As a complete control circuit, the design is simulated.

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3.4.3 Combined Trip and Override Control Functions Design

The final complete and combined control circuit to be implemented on each PDM power channel is shown in Figure 3-9. As shown in Figure 3-9, for simulation verification purposes, a load resistance (R_LOAD) of 10 Ω is used in the simulation. The IRF9328 chosen for the PDM power switch channels is not a default P-Spice model, so the IRF7233 p-channel MOSFET is used for simulation as it matches the characteristics of the IRF9328 p-channel MOSFET. The addition of capacitor C1, resistor R10 and R9 help roll-off high-frequency gain of the MAX9611 current sensor feedback control system. R7 is a high impedance resistor (470 kΩ) used to pull-up v_drive as close to 5 V when a trip signal is commanded.
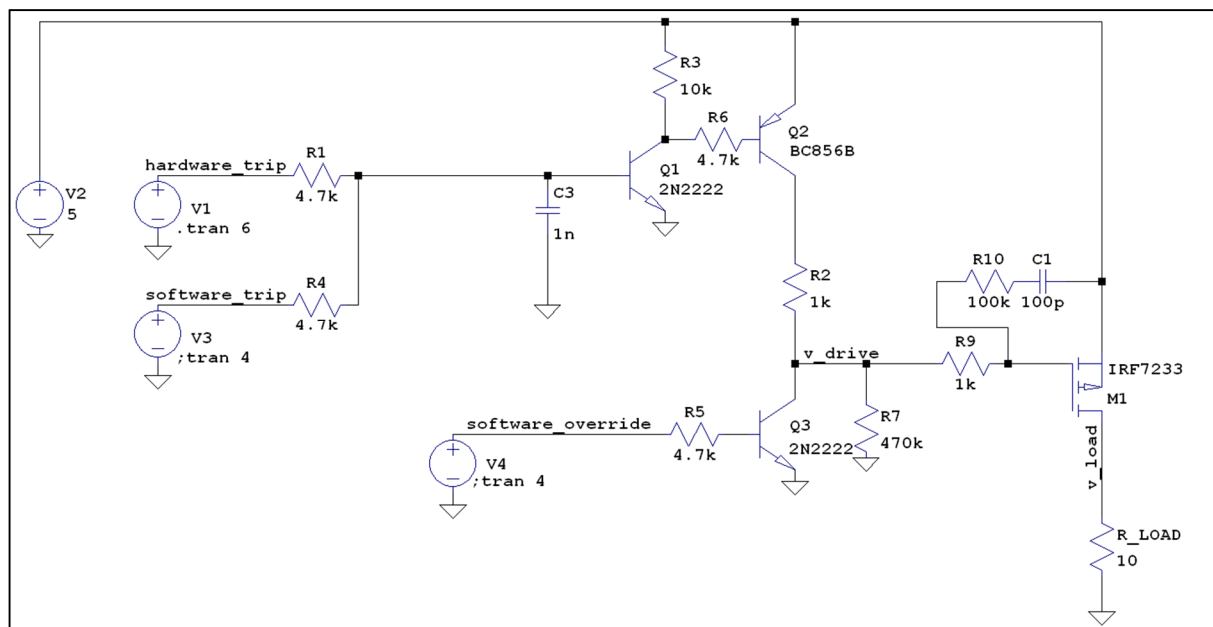
Figure 3-9: P-Spice circuit schematic showing the complete control circuit design to be used on each power distribution channel

Figure 3-10 shows the final output voltage waveform required for the complete control circuit. Looking at the bottom waveform, it is observed that the voltage across R_LOAD is zero whenever a trip signal is applied. At time 0.5 s, a hardware_trip signal is applied; thereby turning OFF the IRF7233 p-channel MOSFET power switch. The load voltage switches to 0 V. At time 0.9 s the hardware_trip signal is turned OFF. As it falls below 0.7 V, BJT Q1 switches to the OFF state and the load voltage instantly rises to 5 V. Similarly, at 2 s a software_trip signal is commanded and the same OFF to ON state is executed. At time 4 s, the software_override signal is applied, regardless of the hardware_trip and software_trip

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signals commanded at time 3 s and 3.5 s, respectively. All functionalities required from the control design of the PDM are successfully simulated. The next subsection introduces the ADG715 I^{2}C controllable switch which is used as an I^{2}C expander to execute all software commands.
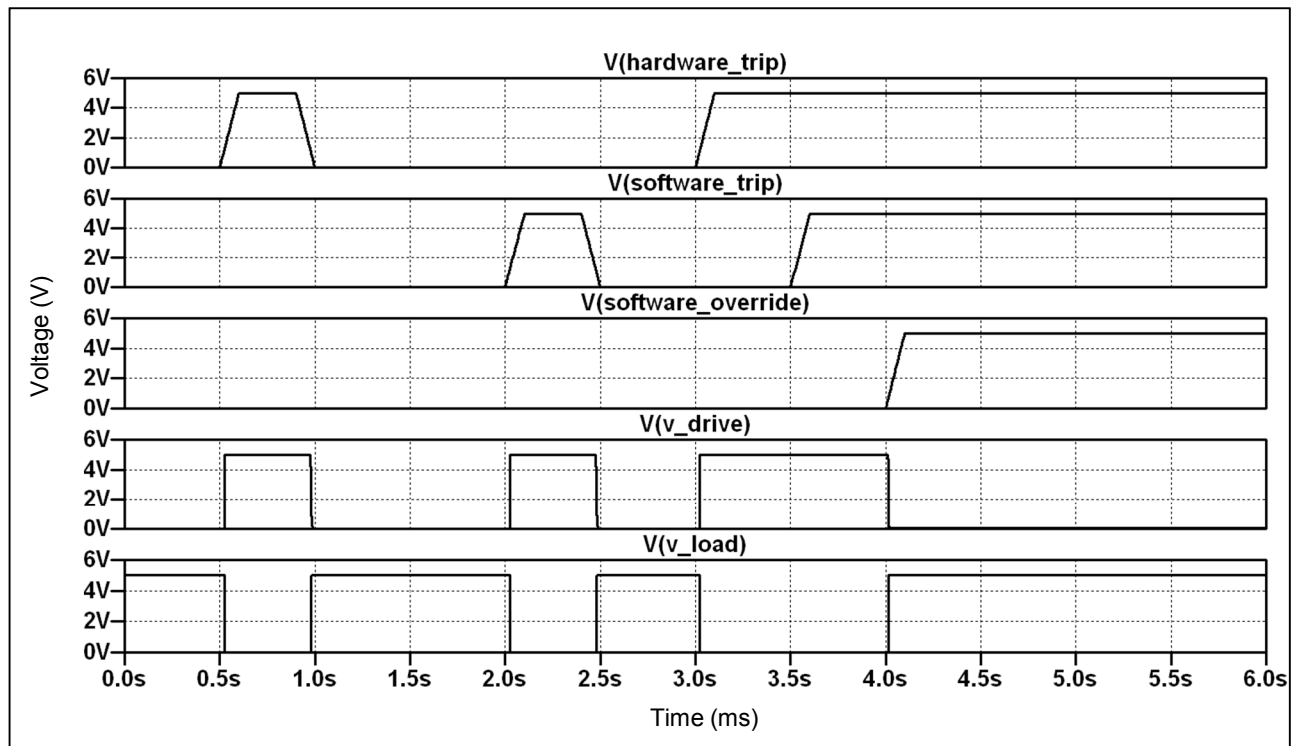
Figure 3-10: Output waveforms for control circuit shown in Figure 3-9

3.4.4 Software Signals Source

The ADG715 I^{2}C controllable switch with eight switch lines are shown in Figure 3.11, where each line is connected to the 5 V voltage bus on one end and software command signals executed on the other end of each switch. Each switch line has a low ON resistance of 0.6 Ω, and in the worst case may rise to 2.5 Ω. The device is found reliable because of its fast switching times of 130 ns turn-on and 115 ns turn-off, which is advantageous to instantaneously isolate a fault condition. The device is used for software_trip and software_override signals as configured in Figure 3-11. For eight channels, two ADG715 devices will be used to provide two software signals on each channel, as previously shown in Figure 3-1.

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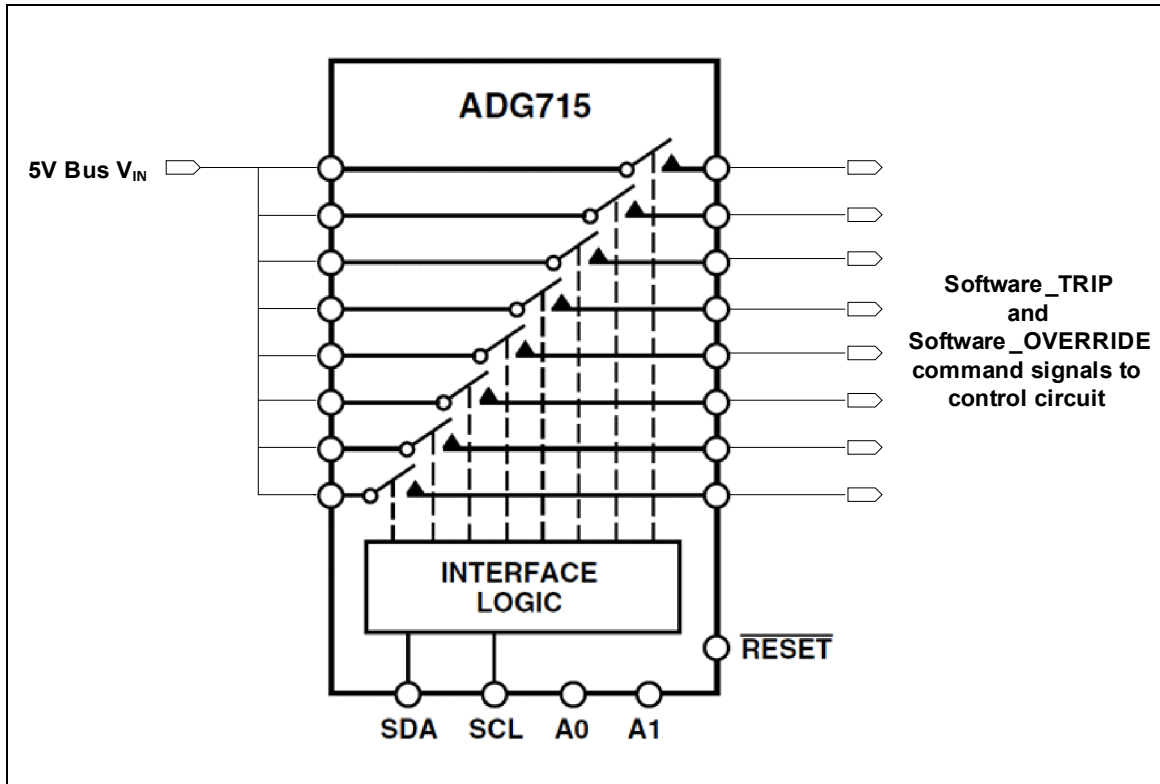
Figure 3-11: ADG175 I^{2}C controllable switch configuration for software commands

(Adapted from ADG714/ADG715 datasheet)

Up to four ADG715 devices can be connected to a single I^{2}C bus as shown in Figure 3-12 (taken from ADG715 datasheet). Each device has two I^{2}C pins, namely serial data (SDA) and serial clock (SCL). Each device further comprises of two addressing pins, A0 and A1 as shown in Figure 3-12.
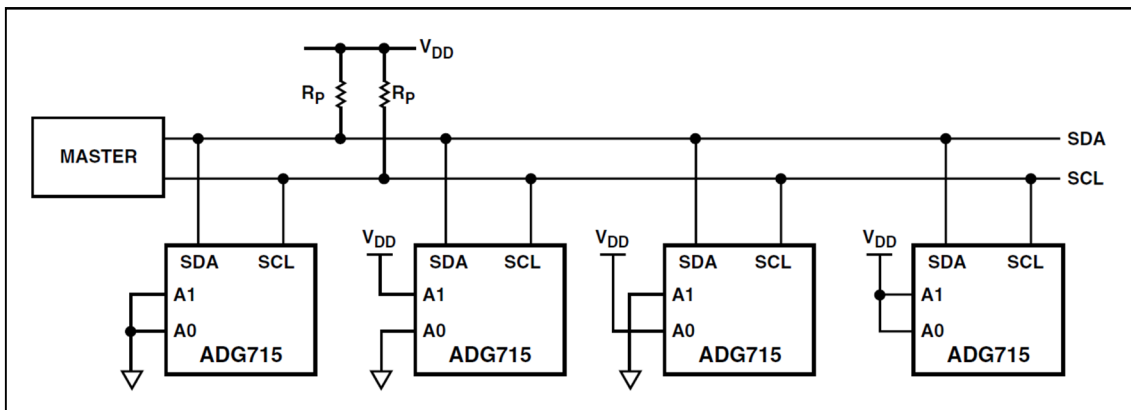
Figure 3-12: Circuit connection for addressing ADG715 devices on an I^{2}C bus

(From ADG714/ADG715 datasheet)

3.5 POWER DISTRIBUTION AND SWITCHING DESIGN

The switching flexibility design of each power channel is implemented as shown in Figure 3-13. A manual switch (connector) shall be used to physically connect the input voltage bus from the EPS to the input port of a single channel on the PDM as shown in Figure 3-13. In this manner, a power channel will not be restricted to be powered from one dedicated voltage bus but will rather have the flexibility to be physically powered to more than one voltage bus.
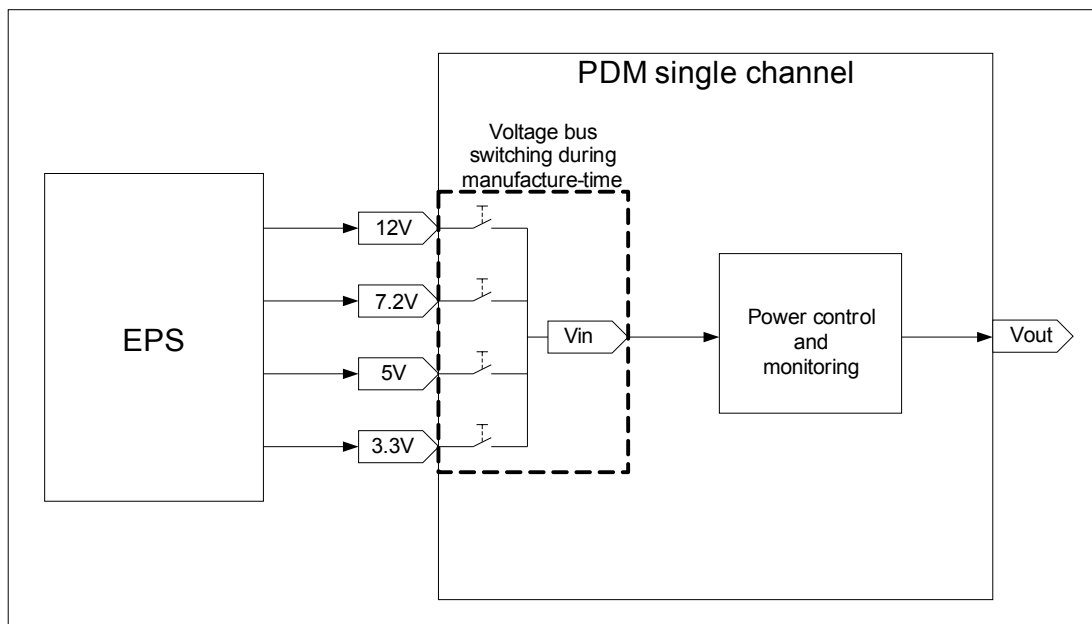
Figure 3-13: Manual switching of power channels at manufacturing time using a manual switch

3.6 PCB DESIGN AND PROTOTYPING

The PCB board design is implemented using Altium Design Explorer (DXP)[11] integration platform.

3.6.1 Control Circuit Schematic

The Altium control circuit schematic for a single power channel previously depicted in Figure 3-9, with the addition of the MAX9611 current sensor, is shown in Figure 3-14. The OUT pin of the current sensor is the hardware_trip signal, which is connected via resistor

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[11] http://wiki.altium.com/display/ADOH/The+Design+Explorer+(DXP)+Integration+Platform

R5. The software_trip and software_override signals are represented as TRIP and OVR in Figure 3-15. Using the diverse design redundancy technique studied in chapter two (section 2.6.2), instead of one sense resistor (R_{sense}), two sense resistors are connected in parallel to the RS+ and RS- pins of the current sensor. The input and output ports of the power channel are shown as Vin and Vo, respectively.
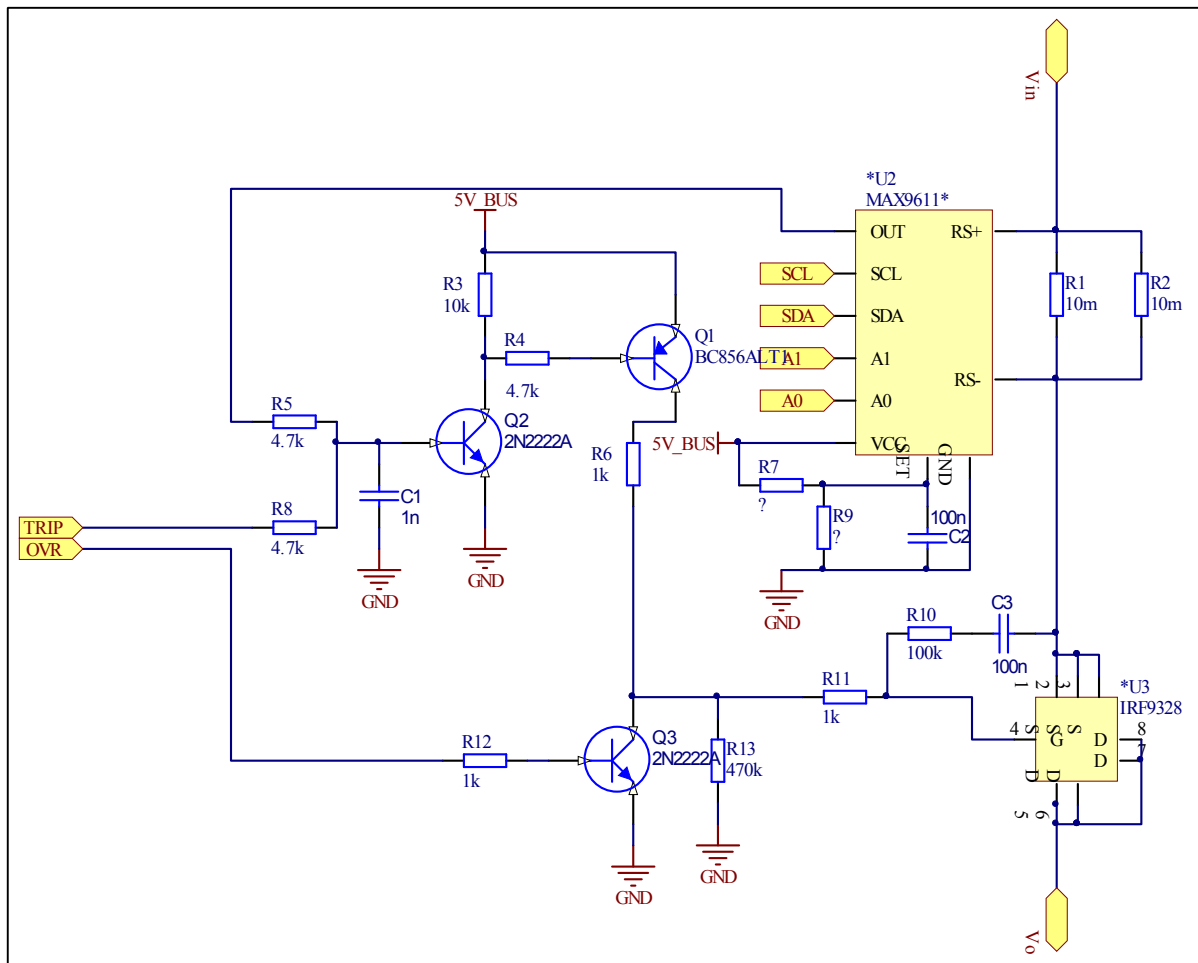
Figure 3-14: Altium control circuit schematic

3.6.2   Current Sensors Addressing

Eight power channels, each containing a single MAX9611 current sensor, are implemented. Each MAX9611 current sensor is required to have its unique device address as listed in Table 3.4. Up to 16 addresses are available, but only the simplest 8 addresses are used for the PDM design. The Arduino development board is used for all software configurations (Chapter 4). Using this board, all bits of the address are shifted to the right; as a result the

least significant bit (LSB) is eliminated. The address becomes a 7 bit address; hence, the write and read addresses are the same. The Arduino addresses are listed on the far right column.

Table 3-4: Address description for MAX9611 current sensors for each PDM power channel

Current Sensor for Channel No.	A1	A0	Device Write Address	Device Read Address	Address on Arduino
1	Vcc	Vcc	0xFE	0xFF	0x7F
2	0	Vcc	0xE6	0xE7	0x73
3	Vcc	2/3×Vcc	0xFC	0xFD	0x7E
4	0	2/3×Vcc	0xE4	0xE5	0x72
5	0	1/3×Vcc	0xE2	0xE3	0x71
6	Vcc	1/3×Vcc	0xFA	0xFB	0x7D
7	Vcc	0	0xF8	0xF9	0x7C
8	0	0	0xE0	0xE1	0x70

Vcc and ground (GND) are already available as part of the electrical power system (EPS). To achieve the 1/3 Vcc and 2/3 Vcc voltage levels, a 16x2 header is created where opposite pins (example shown by pin 1 and pin 17 in Figure 3-16) are connected via a 0 Ω resistor. This header is necessary for creating multi-channel designs discussed later in this section. Using three series connected 10 kΩ resistors between Vcc and GND, all four voltage levels (Vcc, 2/3 Vcc, 1/3 Vcc and GND) are achieved from the addressing header. The header is used to address all eight I²C compatible MAX9611current sensors.
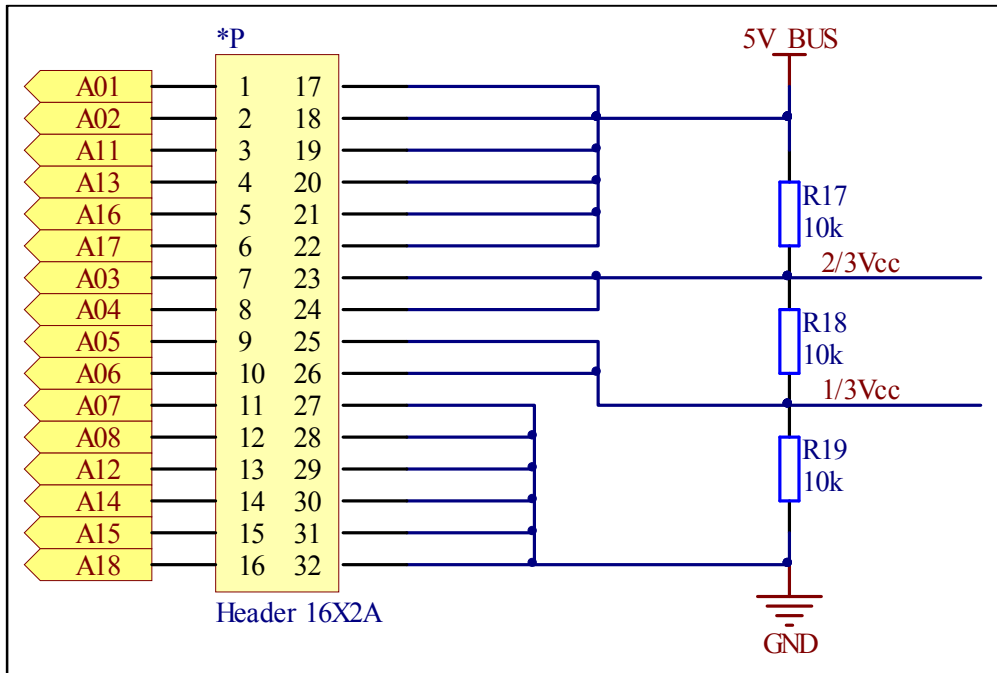
Figure 3-15: A 16x2 header created for addressing of current sensors

3.6.3 PC/104 Headers

Each subsystem in a CubeSat is built on a standard PC/104 board with two 26x2 headers, which are stacked on top of each other in the CubeSat to interface the subsystems. To avoid subsystem designers using the same pins for different purposes, dedicated pins are assigned as shown in Figure 3-16. The dedicated pins are the I^2C pins (SAD and SCL), 3V3_BUS, 5V_BUS, 7V2_BUS and GND. These pins conform to the F'SATI PC/104 pin allocations. The 12V_BUS and all output pins (Vo1 to Vo8) are randomly chosen for research purposes. These may be changed for a protoflight model development of the PDM.
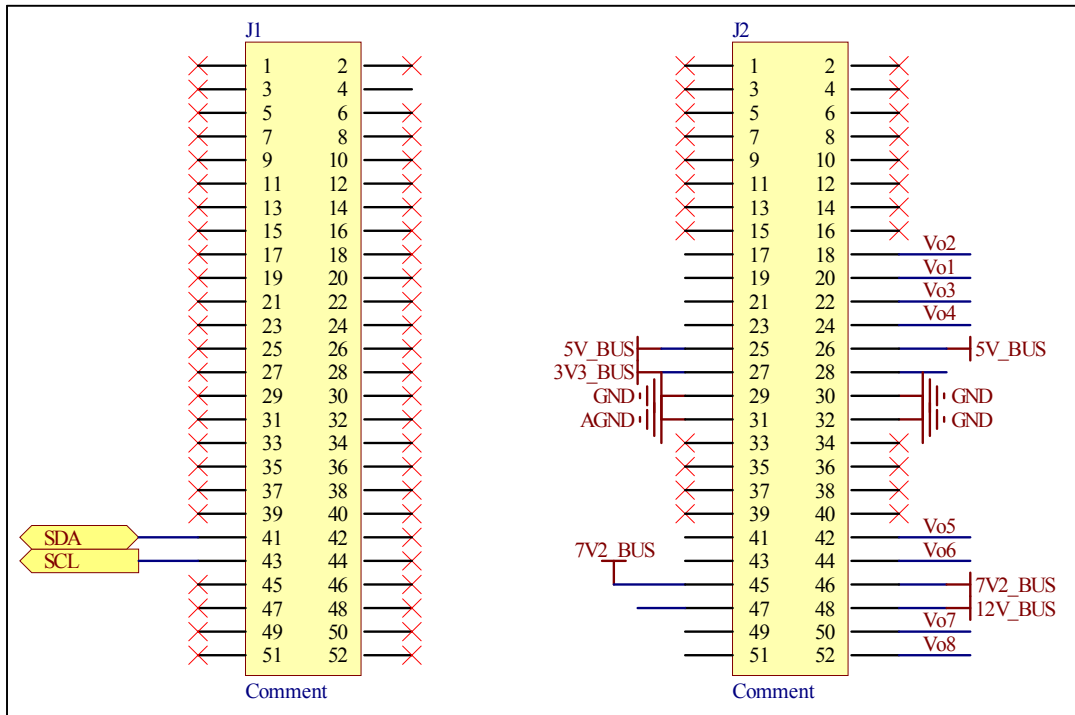
Figure 3-16: Pin definition of the two PC/104 26x2 headers for the PDM

3.6.4   I^{2}C Expanders

As discussed in section 3.4.4 (Figure 3-11), two ADG715 I^{2}C controllable switches are used to generate 5 V logic software signals. Circuit connections for these devices are shown in Figure 3-17, where *U1 is used for power channels 1 to 4 software signals and *U4 is used for power channels 5 to 8 software signals. The outputs (D1 to D8) of each ADG715 device connect to the control circuits. Circuit connections may be seen in the top level design given in Appendix A.
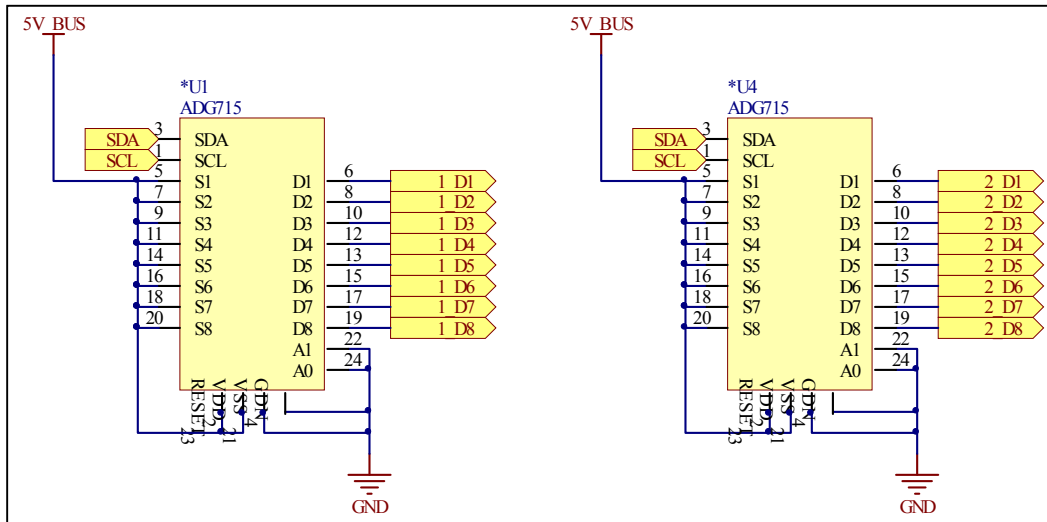
Figure 3-17: Implementation of an I^{2}C controllable switch to expand 5V logic software signals

3.6.5 Multi-Channel Design

Finally, all schematic documents created are combined into a single "top level design" included in Appendix A. The "Top Level Design" creates blocks representing each schematic page, where all connection points (SDA, SCL, A1 & A0, etc.) can be coordinated to the PC/104 headers seen on the top level design in Appendix A.

All power channels of the PDM are similar, and only differentiated by routing to the ADG715 devices and the addressing header from each MAX9611 I^{2}C device. It was found that Altium DXP has the option to create repeated PCB layouts of the same design. The process for creating repeated PCB layouts of the same channel is referred to as multi-channel design. The control circuit schematic (CS.SchDoc) is drawn once on the schematic sheet and routed once on the PCB board layout. To create a multi-channel design in DXP, the procedure is easily followed using the "Creating a Multi-channel Design" tutorial from Altium[12]. The eight repeated schematics are all represented by the "Repeat(CS,1,8)" block in Figure 3-18. Also shown in Figure 3-18 are all sixteen (16) software trip and override commands from the ADG715 devices. SCL and SDA are common to all devices and only need to be named and are automatically routed. All 8 inputs and outputs to each power channel are also visible in Figure 3-18, as well as the A0 and A1 pins to the I^{2}C addressing header created in section 3.6.3.

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[12]http://www.altium.com/files/Altiumdesigner6/LearningGuides/TU0112%20Creating%20a%20Multi-channel%20Design.PDF
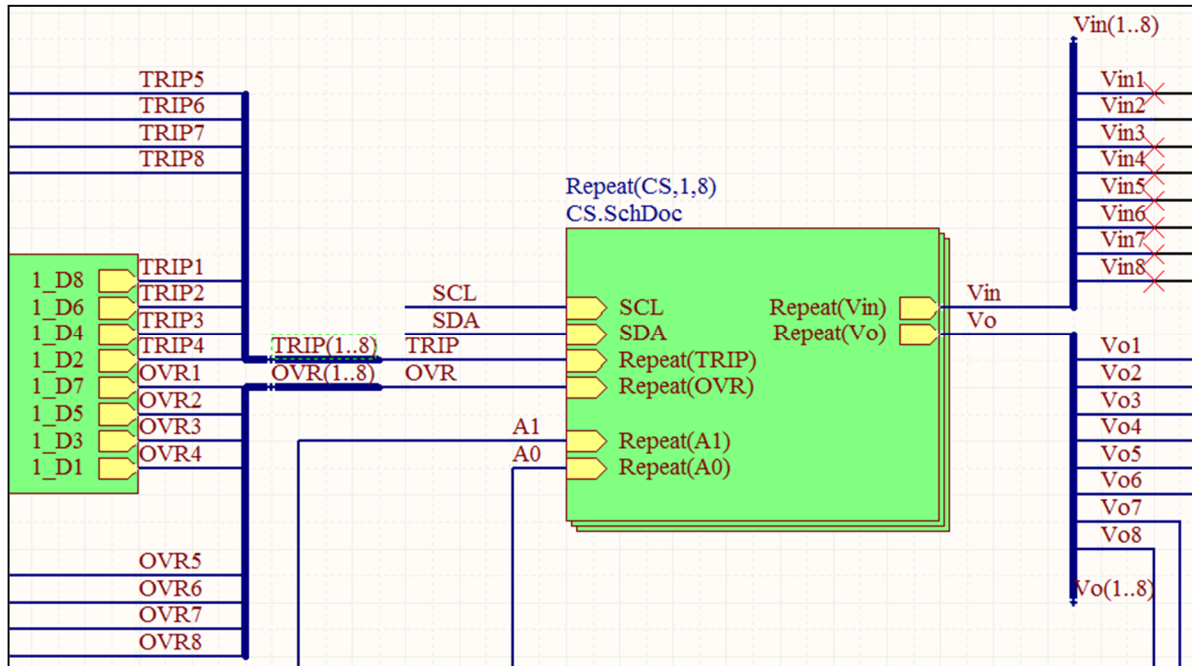
Figure 3-18: Repeated multi-channel design of the control circuit for each power distribution channel

3.6.6 PCB Prototyping

The final PCB layout is included in Appendix B. Figure B-1 shows the PCB layout with repeated channels (CS1 to CS8) enclosed in shaded rectangular blocks referred to as rooms when creating an Altium DXP multi-channel design. It will also be noted that power channels 1 to 4 are similar and power channels 5 to 8 are similar. The only difference between channels is the routing to the I^2C header and the ADG715 devices. Also, it should be noted that components belonging to power channel 1 (CS1) will end with a letter suffix "A". For example, resistor "R4" in power channel 1 (CS1) is named "R4A", "R4B" in power channel 2 (CS2) and "R4H" for power channel 8 (CS8). Figure B-2 in Appendix B is a clearer view of the final PCB layout without the multi-channel design rooms. The populated prototype is included in Appendix C, with power channels 1, 3, 7 and 8 populated. The two I^2C switches (ADG715) are also populated on the board in Appendix C.

3.6.7 PDM Populated Prototype

The PDM prototype is shown in Figure 3.19, with components populated and soldered on power channels 1, 3, 7 and 8. For simplicity, these power channels are referred to according to the hexadecimal I^2C address of the current sensor belonging to that power channel, previously described by the Arduino addresses in Table 3-4. The current sensor of each

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power channel is referenced by the hexadecimal I^{2}C address, namely 0x7F, 0x7E, 0x7C and 0x70 for power channels 1, 3, 7 and 8, respectively. The two I^{2}C controllable switches (ADG715) are also shown in Figure 3.19. They are used for software commands to each power channels. For power channel 1-4, ADG715 device with address 0x48 is used and for power channels 5-8, ADG715 device with address 0x48 is used. Extension wires seen in Figure 3-19 are used to interface the board to the power supply, load meter, load resistances and an Arduino development board for functional software implementation. The PDM system functionalities are verified in chapter 4.

Pull-up resistors

Power switches

Channel 1-4 I^2C switch
(0x48)

Channel 1 (0x7F) sensor

Channel 3 (0x7E) sensor

Voltage bus connectos

Channel 7 (0x7C) sensor

Channel 8 (0x70) sensor

Channel 5-8 I^2C switch
(0x49)
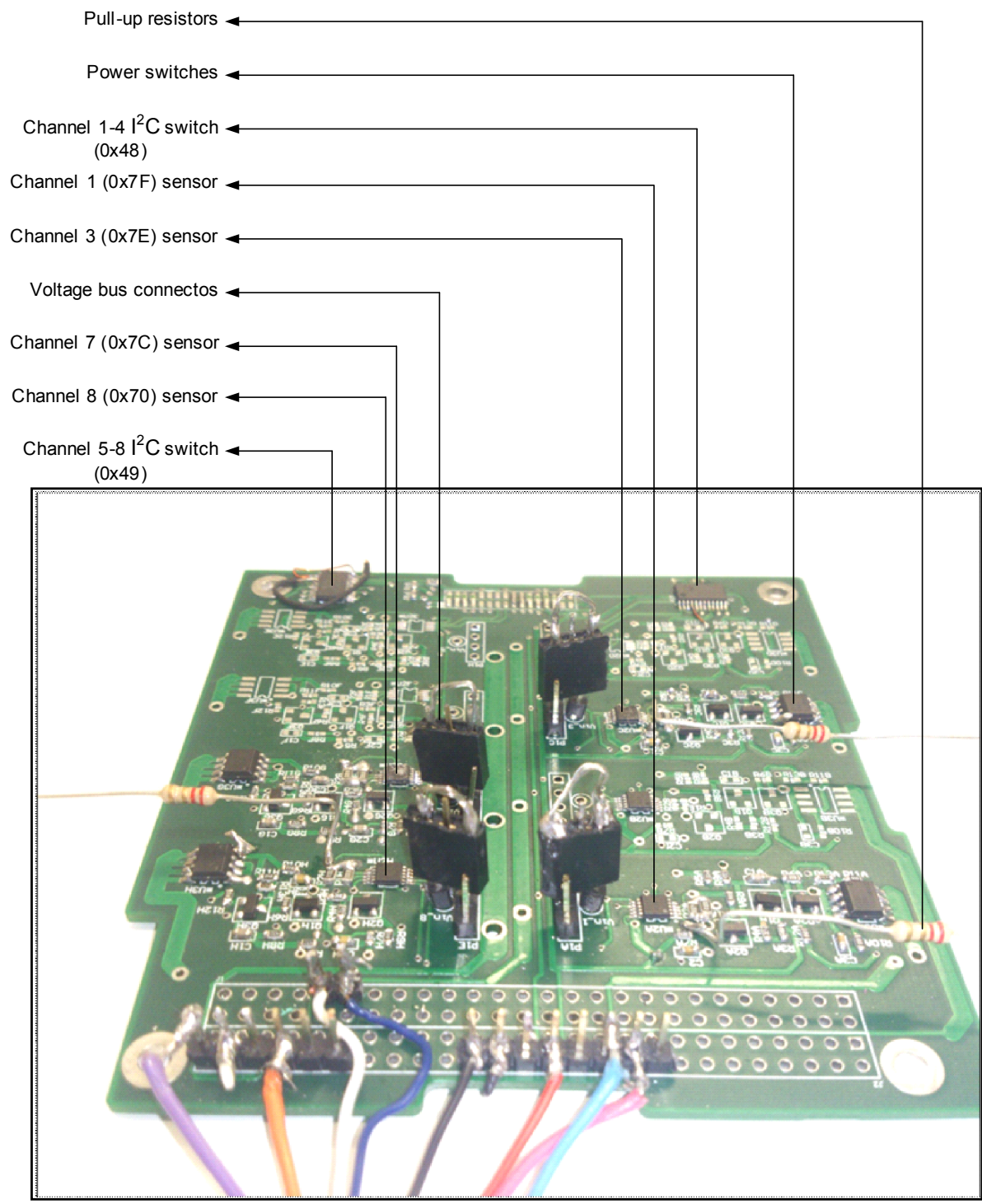
Figure 3-19: PDM prototype with four populated power channels

3.7 SUMMARY

This chapter discusses all steps followed from design and simulation phase to producing the PDM prototype. The PDM is designed according to the specifications and studies carried out in chapter 1 and chapter 2. The design is verified through simulation, using LT-Spice. Components for the design are carefully selected according to voltage and current thresholds. The PDM PCB design is implemented using Altium DXP, which has the advantage of creating multi-channel designs of the power distribution channels. The chapter concludes with the final PDM prototype, showing 4 populated channels. This prototype is tested in chapter 4.

CHAPTER 4: PROTOTYPE VERIFICATION

4.1 INTRODUCTION

In chapter one, two types of environmental tests were discussed to qualify the power distribution module (PDM) under "space like" environments, namely radiation and thermal testing. In chapter two, the different types of radiation sources in the space environment were discussed. Before environmental testing, functional tests need to be performed in the laboratory. Basic current flow (continuity) and voltage measurements on selected power channels are tested to verify functionality of the PDM system. Software implementation on an external master node is implemented to execute all software telemetry and commands on the PDM system.

To drive software coded functional tests, the PDM is interfaced to an Arduino development board (microprocessor) as a master node to read and write all I^2C telemetry and commands. In a real satellite mission, all software functions performed by the Arduino microprocessor will be executed by the on-board computer (OBC). Lastly, environmental verification tests are performed.

4.2 TEST PLATFORM SETUP

Since all power channels are identical, to verify proof of concept for this research project one power channel may be put under test to certify that all functional and performance specifications are met. For environmental tests, populating more power channels would be ideal to draw a statistical conclusion regarding failures detected on individual channels. Although testing all power channels may be the ideal case, populating all power channels is limited by the availability of electronic components since the project is a proof of conceptual research. Power channels 1 (0x7F), 3 (0x7E) and 8 (0x70) are populated with electronic components as shown in Figure 3.19 of chapter three to prepare the system for functional testing.

4.2.1 Analogue Measurements of Power Channels

Two 100 mΩ current-sensing resistors connected in parallel are used for each power channel current sense resistance. This yields an effective current sense resistance (R_{sense}) of 50 mΩ. Alternately for each channel test, the output port of the channel is connected in series to a load meter. There is an expected voltage drop across the sense resistors and along the connection wires to the power supply and load meter. Because all subsystems in a CubeSat are interconnected via the PC/104pin header, it is necessary to take voltage input measurements (V_{in}) and voltage output measurements (V_{out}) at the PC/104 pins using an accurate measurement meter in order to avoid voltage drops across the external connection wires which are not used in a typical real CubeSat mission.

To determine how efficient the PDM design is in terms of voltage drop, the voltage efficiency is calculated by taking the ratio of the input and output voltages of each tested power channel according to Equation 4.1 as:

$$\%V_{eff} = \frac{V_{out}}{V_{in}} \times 100\% \qquad\qquad \text{Equation 4.1}$$

For each channel, V_{in} is alternately connected to one of the four voltage busses using the voltage bus connector shown in Figure 3.19 of. V_{in} is measured at the PC/104 pin of the power channel under test using the high accuracy Agilent 34405A digital multimeter[13]. In the same manner, V_{out} is measured at the PC/104 output pin of that tested power channel. High voltage efficiency is associated with small voltage drops from input to output. The voltage drop is simply calculated using Equation 4.2:

$$V_{drop} = V_{out} - V_{in} \qquad\qquad \text{Equation 4.2}$$

Each bus voltage line is tested for current continuity and the voltage drop is measured across each tested power channel. The results are summarised in Table 4.1. It can be seen that all tested power channels prove to be highly efficient and that current continuity is indeed achieved. It should be noted that the series resistors have ±5% tolerance; hence, for the 3.3 V bus with 97.03% efficiency, the resistors may be slightly higher than 100 mΩ (range from 95 mΩ to 105 mΩ), thereby causing a slightly bigger voltage drop across the

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[13]http://cp.literature.agilent.com/litweb/pdf/34405-91000.pdf

sense resistors. The output of each power channel is connected to the load meter as a load (R_{load}).

Table 4-1: Measured voltage efficiency of selected power channels driven by the different voltage busses

Voltage bus (V)	Power Channel	I_{load} (mA)	R_{load} (Ω)	V_{IN} (V)	V_{OUT} (V)	V_{DROP} (mV)	V_{eff} (%)
3.3	1	289.4	11.02	3.299	3.202	97.9	97.0
5	3	270.4	18.01	4.874	4.837	36.9	99.2
7.2	8	224.2	31.75	7.162	7.145	17.4	99.8
12	1	170.9	69.71	11.957	11.945	12.0	99.9

4.2.2 Master Node

Software-operated electronic devices in F'SATI CubeSats communicate to a master node, the OBC, as slave devices via an inter-integrated circuit (I^2C) communication protocol previously discussed in chapter 1 (section 1.2.5). In the absence of the OBC, and to verify proof of concept, the PDM system is interfaced with the Arduino UNO[14] development tool; herein used as the master node. The Arduino UNO development tool is shown in Figure 4.1. The serial USB port is used to interface the development tool to a computer for software coding and viewing of results in real-time. The ground pin is connected to a common ground with the PDM board. A reset button is used to restart the code internally when required. Pins A4 and A5 are connections to the I^2C bus.

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[14]http://arduino.cc/en/Main/ArduinoBoardUno
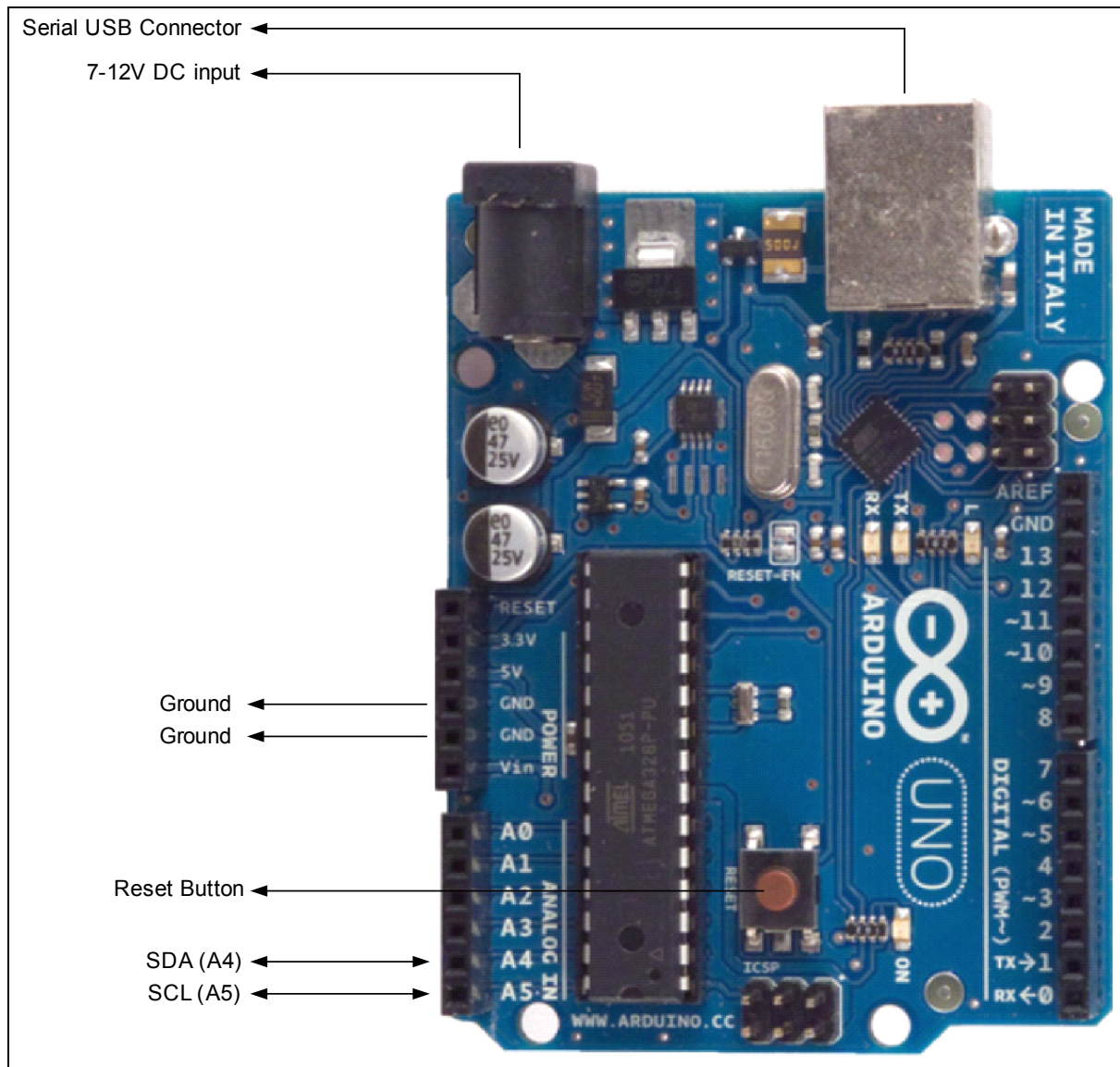
Figure 4-1: Arduino develepment tool used as a master node for functional test purposes

4.2.3 Equipment Setup

The equipment used is the BK Precision 8500 300 W programmable DC electronic load[15], the Agilent E3631A DC power supply, a breadboard for I^2C pull-up resistors (R_P=10 kΩ), constant resistive loads (R_L=150 Ω), and the Arduino UNO development board. The equipment setup is depicted in Figure 4-2, portraying the combination of equipment to the PDM board.

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[15]http://www.bkprecision.com/products/dc-electronic-loads/8500-300-w-programmable-dc-electronic-load.html
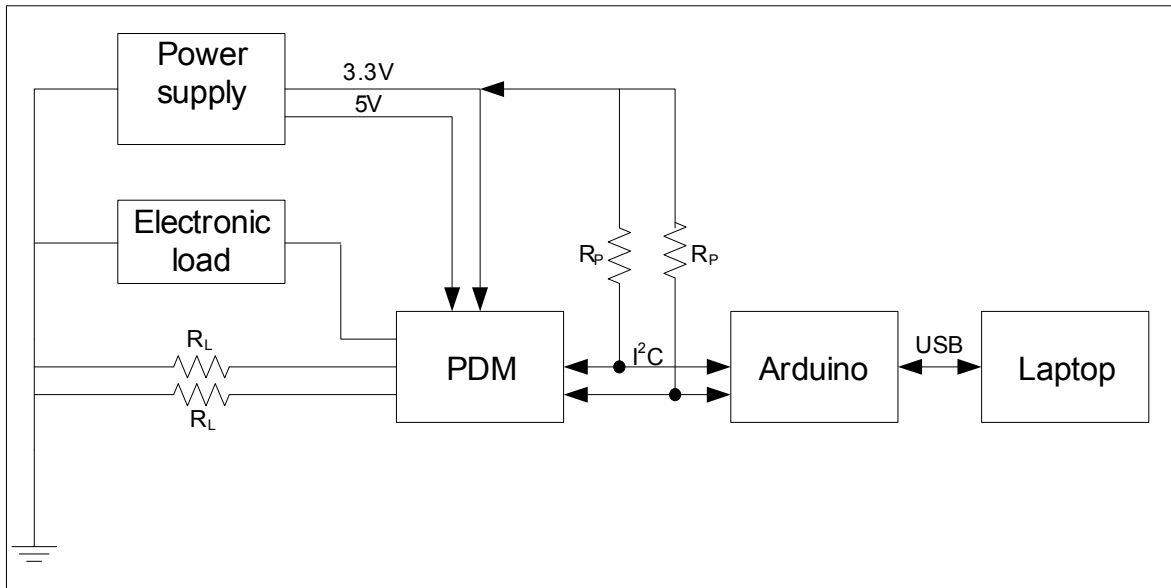
Figure 4-2: Equipment setup used for functional tests

4.2.4 I²C device scanner

Before the functional software code can be programmed onto the Arduino UNO board to read and command digital software signals, an I²C scanning code included in Appendix D (taken from Arduino Playground[16]) is run on the PDM board to scan and verify addresses of all I²C devices populated on the board. After running the I²C scanner code, the serial monitor display showed the devices found as shown in Figure 4-3. On every instant of pressing the "reset" button shown in Figure 4-1, all devices are found at the same addresses.

```
I2C scanner. Scanning ...
Found address : 72 (0x48)
Found address : 73 (0x49)
Found address : 112 (0x70)
Found address : 126 (0x7E)
Found address : 127 (0x7F)
Done.
Found  5 device(s).

I2C scanner. Scanning ...
Found address : 72 (0x48)
Found address : 73 (0x49)
Found address : 112 (0x70)
Found address : 126 (0x7E)
Found address : 127 (0x7F)
Done.
Found  5 device(s).
```

Figure 4-3: Serial monitor display of the I²C scanner code run on the PDM board

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[16] http://playground.arduino.cc/Main/I2cScanner

As shown in Figure 4-3, five devices were found with their addresses written in decimal and hexadecimal in brackets. The first two devices, 0x48 and 0x49, are the ADG715 I^{2}C controllable switches for software commands on channels 1 to 4 and channels 5 to 8, respectively. The last three devices, 0x70, 0x7E and 0x7F, are current sensors for channels 8, 3 and 1, respectively. Seeing that the devices are found, a functional code is designed and integrated in the next sub-subsection for I^{2}Ccommanding of the devices.

4.2.5 Functional Code Implementation

The PDM digital software interfaces are outlined in chapter one (section 1.6.6) in terms of telemetry and telecommands. The functional code needs to read voltage, current and temperature telemetry from all sensors. The code further needs to execute software trip and override commands for each power channel. The hardware trip command is set in control register 1 of the MAX9611 current sensor to MODE 111 (Maxim, 2011:16). This is the comparator mode, where the OUT pin will latch high if the sensed current threshold is exceeded, thereby automatically tripping the power switch. The functional code is described by the flowchart in Figure 4-4 and is summarised below:

- Initialisation: Three counters are initialised, namely x, row and var. The serial bus is set to a baud rate of 9600. All control registers for all I^{2}C devices are cleared. Headings are printed to the Excel page shown in Figure 4-6, namely Time, Volts 7F (V), etc.

- Trip commands are executed on all channels simultaneously at x = 50, 800. Similarly, override commands override the trip commands at x = 120, 870. On the first loop, x = var = 1 pre-set from the initialisation stage which sets current sensor 0x7F (channel 1) as the address.

- The MAX9611 current sensor of the selected address is set to read all telemetry every 2 ms and also set to comparator mode (MODE2), where the hardware trip signal should latch high if an over-current condition is detected, thereby autonomously tripping the power switch of that channel.

- Telemetry is read from the selected current sensor.

- Telemetry is exported to the active Excel spreadsheet of that address as shown in Figure 4-6.

- All counters are incremented, and if var = 4 it is reset to 1 to make address = 0x7F.

- A delay of 5 s is executed and all processes are looped except the initialisation process.
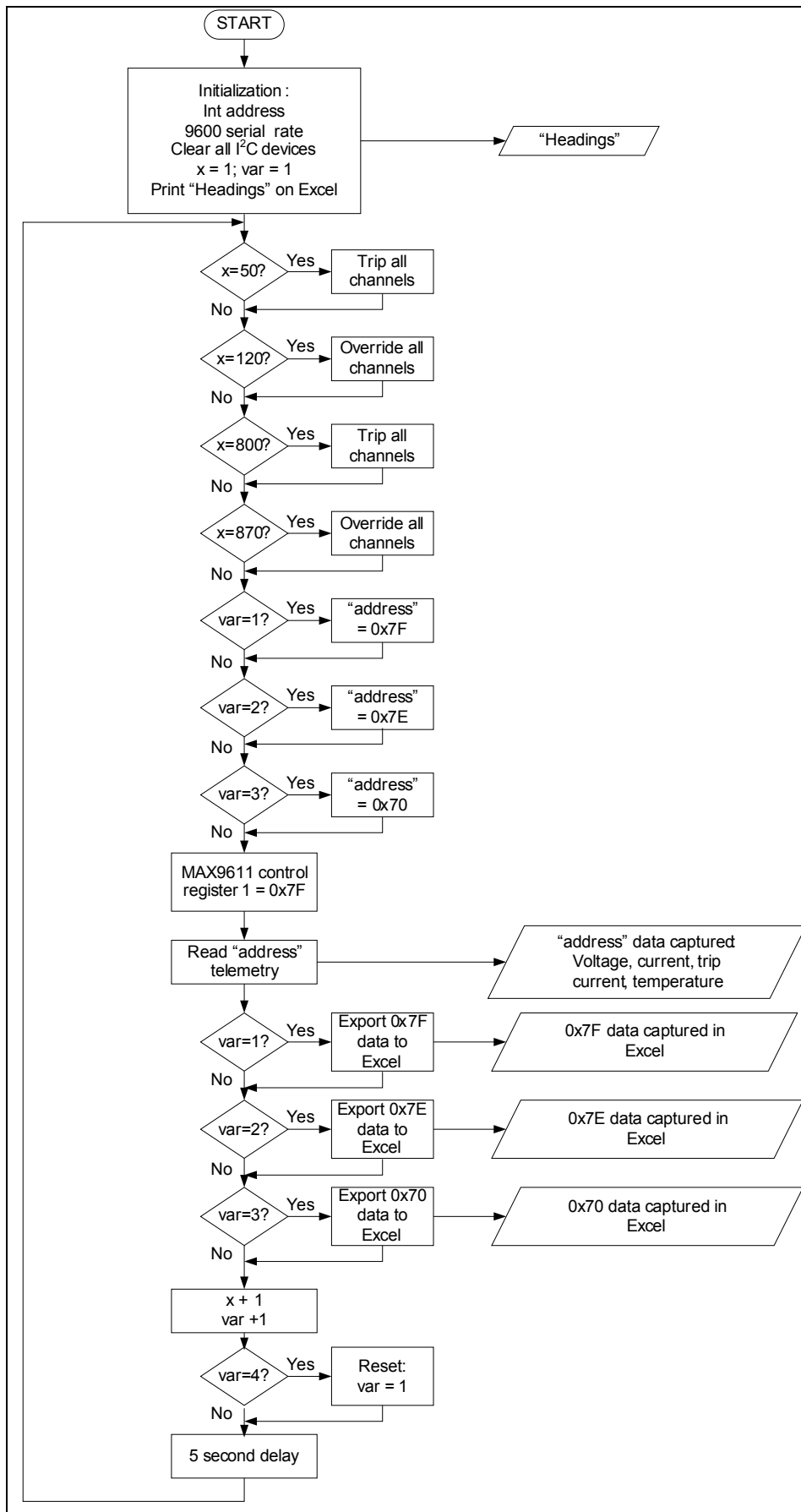
Figure 4-4: Functional code flowchart

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4.2.6 Software Digital Measurements

The MAX9611 current sensors are equipped with an internal analogue to digital converter (ADC) which enables the conversion of analogue measurements to digital format and transmission via the serial bus. All digital measurements are serially transferred to a computer and printed on the Arduino serial screen sequentially as shown in Figure 4-5. The first line, "CLEARDATA", clears and refreshes the serial monitor screen. Second to fourth prints the headings of the telemetry to follow. For example, the first value (4.84) is the voltage of power channel 0x7F, labelled "Volts 7F (V)" in the headings row. Although the power supply is set to 5 V, there will be a voltage drop across the connection wires to the PDM board from the power supply and load meter; hence, voltage reading drops by 160 mV to 4.84 V. It was observed that when voltage measurements were taken at the PC/104 pin header, the voltage drops were lower, in the range of ±30 mV. The Arduino serial monitor data is shown in Figure 4-5.

```
CLEARDATA
LABEL,Time,Volts 7F (V),Current 7F (mA),Power 7F (W),Temp 7F (deg C),Volts 7E (V),Current 7E
(mA),Trip Current 7E (mA),Temp 7E (deg C),Volts 70 (V),Current 70 (mA),Power 70 (W),Temp 70
(deg C),

DATA,TIME,4.84,8.77,0.04,31.68,4.90,35.08,683.03,24.00,4.78,539.30,2.58,24.96,
DATA,TIME,4.84,8.77,0.04,31.68,4.90,35.08,683.03,24.00,4.80,541.49,2.60,24.96,
DATA,TIME,4.84,8.77,0.04,32.64,4.90,35.08,683.03,24.00,4.80,528.34,2.54,24.96,
DATA,TIME,4.84,8.77,0.04,32.64,4.90,35.08,683.03,24.00,4.80,532.72,2.56,24.96,
DATA,TIME,4.84,8.77,0.04,32.64,4.90,35.08,683.03,24.00,4.80,532.72,2.56,24.96,
DATA,TIME,4.84,8.77,0.04,32.64,4.90,35.08,683.03,24.00,4.80,537.11,2.58,24.96,
DATA,TIME,4.84,8.77,0.04,32.64,4.90,35.08,683.03,24.96,4.80,543.69,2.61,24.96,
DATA,TIME,4.84,8.77,0.04,33.60,4.90,35.08,683.03,24.00,4.80,545.88,2.62,24.96,
DATA,TIME,4.84,8.77,0.04,32.64,
```

Figure 4-5: Arduino serial monitor showing power channels' telemetry in real-time

Although the data is readable as shown in Figure 4-5, it becomes very difficult to follow and spot a fault when the data line is displayed every second or every five seconds. A better solution to monitor all telemetry in real-time is by exporting it to Excel. By installing the Parallax PLX-DAQ data acquisition for Excel software[17], all power channel telemetry can be monitored and displayed in real-time in Microsoft Excel spreadsheets. In addition, any change in data may be detected easily from real-time graphs drawn in Microsoft Excel, as shown in Figure 4-6. The first column from the left displays the real-time. The following four

---

[17]http://www.parallax.com/tabid/393/default.aspx

columns display telemetry for channel 0x7F, followed by four columns of 0x7E telemetry and the last four columns telemetry for power channel 0x70. Graphs may be inserted on the Excel page to view the telemetry as it changes in real-time. As an example, a graph representing the voltage on channel 1 (0x7F) is included in the screen shot shown in Figure 4-6.
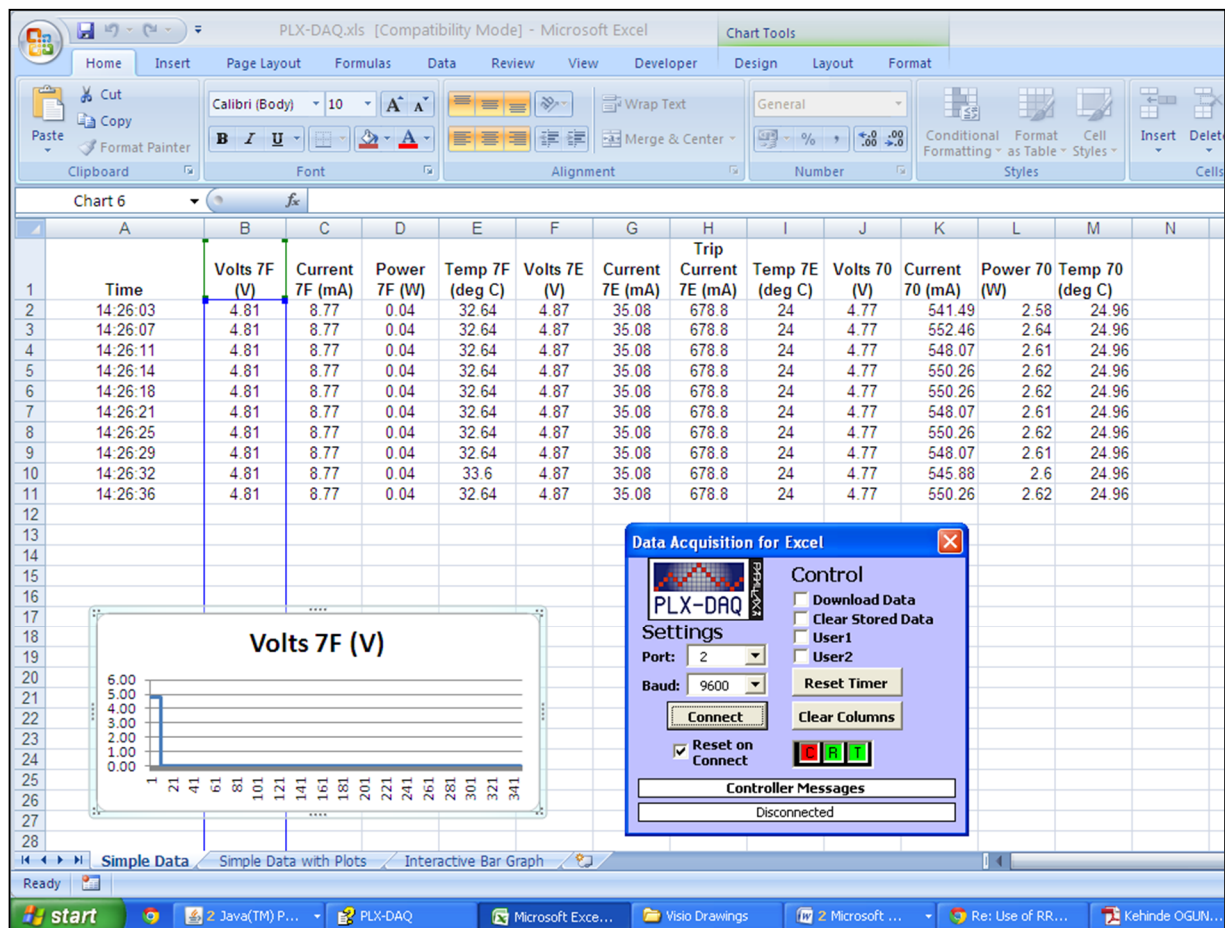
Figure 4-6: Parallax "Data Acquisition for Excel" software displaying telemetry from the power channels in real-time

4.3 FUNCTIONAL TESTS

All three channels (0x7F, 0x7E and 0x70) are put to test and monitored in real-time. Telemetry is captured using the Parallax Data Acquisition software for Excel. Due to only one load meter available in the F'SATI laboratory, only one power channel per test cycle can be connected to the variable load meter. All three channels are tested during each functional test cycle, during which one channel is connected to the load meter and the other two

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connected to constant resistive loads (150 Ω, 0.25 W tolerant resistors). This resistance value is selected to be equivalent to the power consumption consumed by the OBC and the attitude determination and control (ADSC) subsystems in a typical CubeSat mission.

4.3.1 Test Procedure

- Software_trip and software_override commands:

As coded in the functional code included in Appendix E, software commands (software_trip and software_override) are executed periodically by the two I^{2}C controllable switches. The commands are simultaneously executed on all power channels, thereby periodically verifying that all software trip circuits and the I^{2}C controllable switches executing these software commands are still working properly. Software command output plots are described in Figure 4-7(a).

- Autonomous hardware_trip command:

To create an over-current condition, the load resistance on the load meter is lowered until the current exceeds the trip level. With only one load meter available, three test cycles of 20 minutes per cycle are performed on each channel. Viewing real-time telemetry graphs, current trip points are observed as shown in Figure 4-7(a). The Autonomous hardware_trip command is executed automatically by a comparator internal to the MAX9611 current sensor when the current reaches the trip level of 600 mA as shown in Figure 4-7(a). The comparator output trips a p-channel MOSFET by latching high for 50 ms, then auto-retries by latching low.

- Autonomous Reset

The Autonomous Reset function automatically stops the comparator from latching when the current drops to about one third below the trip level, thereby stopping the autonomous trip function and allowing the power switch to reset as shown in Figure 4-7(a).

- Telemetry

Real-time graphs showing each channel's telemetry over time are acquired. Each channel's telemetry is as follows:

- Voltage telemetry from the input side of the power channel, drawn in Figure 4-7(b). This voltage varies according to the trip conditions due to the trip level

set resistor divider and the input voltage feeding from the same unregulated bus.

- – Current telemetry is shown in Figure 4-7(a).
- – Temperature telemetry is shown in Figure 4-7(c).
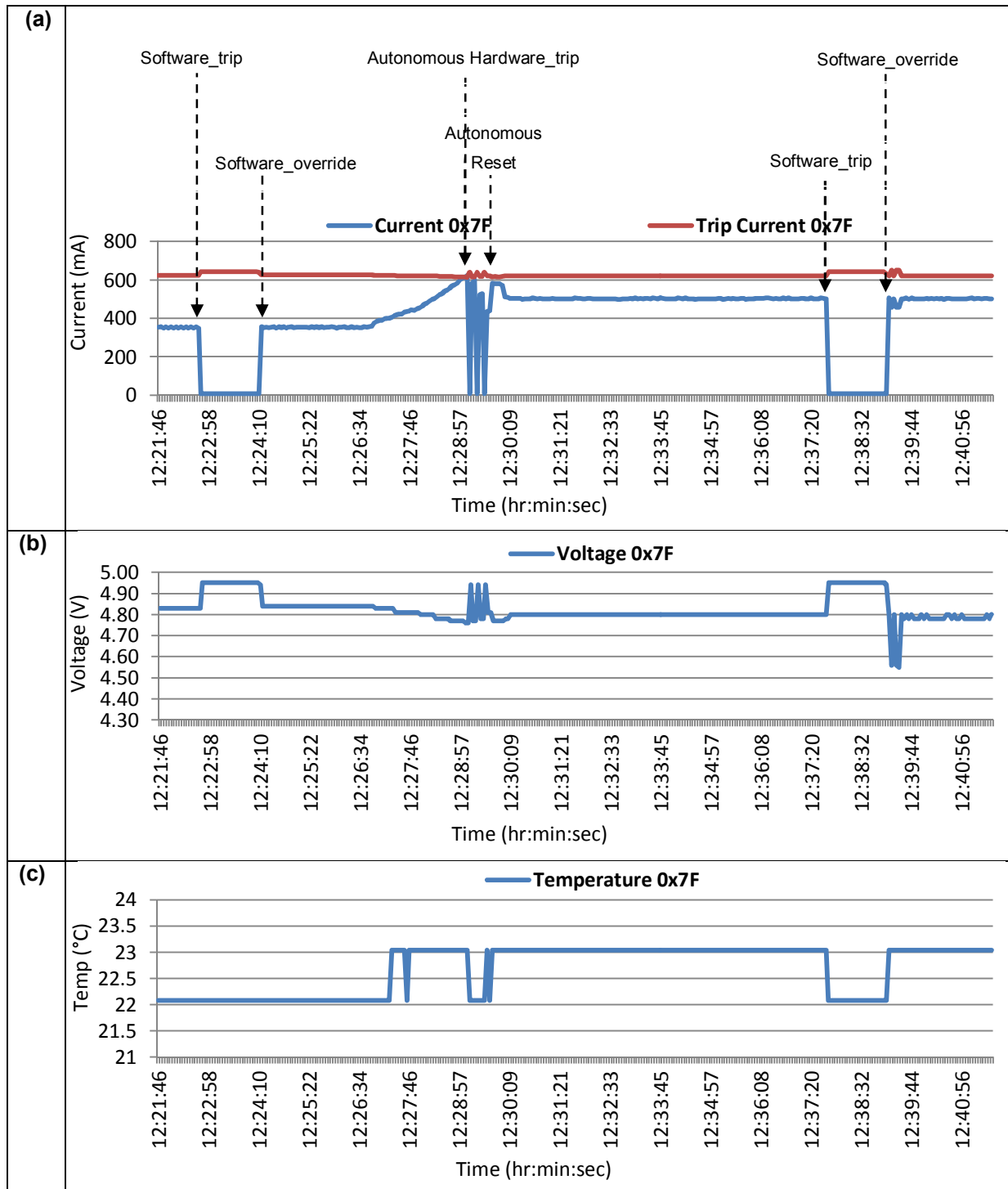
Figure 4-7: Functional test verification showing (a) load current telemetry and trip commands (b) voltage telemetry and (c) temperatute telemetry

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4.3.2 Functional Verification

The test procedure is followed and the module functionality is verified by the plots in Figure 4-7(a)-(c). Current, voltage and temperature telemetry of a single channel (0x7F) is shown. All trip and override commands are verified according to the module's functional requirements and design specifications presented in chapter one (refer to sections 1.6 and 1.7).

4.4 IRRADIATION FUNCTIONAL TESTS

Functional performance against specification was verified in the previous section. The next stage is to investigate functional performance under environmental conditions, namely irradiation and thermal cycling tests.

The primary purpose of the irradiation functional tests is to determine the level of radiation dosage the PDM can withstand without failure modes. Extension wires 7 m long are used to isolate the setup equipment from the radiation chamber room to avoid possible damage to the equipment.

4.4.1 Test Procedure

Irradiation tests are performed at iThemba LABS, South Africa. An AECL Medical Theratron 780-C is used to control a Cobalt-60 ($^{60}C_0$) Teletherapy machine (see Appendix G) that has the capability to generate irradiation Gamma rays. As discussed in chapter 2 (section 2.3.3.3), Co-60 gamma and X-ray sources are the most commonly used for laboratory irradiation tests.

The irradiation test procedure is as follows:
- Functional test process followed. All three power channels under test are functional and monitored in real-time.
- PDM board is 7 m away (inside irradiation chamber). All three channels provide real-time telemetry simultaneously as described in the functional test procedure.
- 20 minute test cycles are followed. The radiation chamber has to be reset every 20 minutes.
- Telemetry is displayed.
- Eleven test cycles are done, with the first ten cycles of 20 minutes each and the eleventh cycle of 10 minutes, yielding a total cycle time of 210 minutes.

- An irradiation dose rate of 0.47 Gy/min is generated for the total cycle time, thereby yielding a total irradiation dose of 98.7 Gy after 210 minutes, which is equivalent to 9.8 krad ($\approx$10 krad). Generally, a low Earth orbit (LEO) satellite mission lifetime of five years is exposed to a total radiation dose of 20 krad. Therefore, a total of 10 krad is equivalent to half the mission lifetime. A typical CubeSat operational lifetime is ±1 year; hence, a 10 krad dose of 2.5 years is sufficient for qualification purposes.

- The dosage level is noted whenever an unusual condition occurs.

4.4.2 Functional Verification

The hardware trip command tripped the power channel but also interrupted the I^2C communication bus; as a result the bus had to be reset every time the hardware trip was manually triggered by varying the load resistance. After a few attempts, the hardware trip testing was omitted to complete the radiation test. The module was controlled via a wire harnass with a length of approximately 7 m and it is believed that the switching of large currents in close proximity with the I^2C wiring caused upsets in the I^2C communication.

4.5 THERMAL CYCLING FUNCTIONAL TESTS

Thermal cycling functional tests are performed at Reutech, South Africa. A Tenney Environmental Test Chamber shown in Appendix G (Model No. C30RC2.0-A-RMC-NY) is used, purchased with chamber option of LN2/CO2 boost cooling. The chamber is used for environmental cycling reach-in tests, with the ability to simulate "Temperature-only" and "Temperature/Humidity" environmental conditions. A temperature button is placed underneath the PDM board (see Appendix G) to measure the temperature and log the data onto its own memory. After the test, all temperature data from the button (chamber temperature) can be compared to the set temperature as shown in the first row of Table 4-2. It can clearly be seen that the chamber temperature is exactly equal to the pre-set temperature, thereby concluding that a precisely accurate chamber was used.

Thermal cycling tests are performed under the same test setup described for irradiation tests. However, during thermal cycling functional tests, the chamber does not need to be reset at intervals; it runs for the entire test period. Two thermal cycles are tested as required by the F'SATI technical team.

4.5.1 Test Procedure

For real satellite missions, test durations are governed by the expected mission lifetime. The developed PDM is intended for future CPUT-F'SATI missions; hence, temperature margins and cycles are set by the F'SATI technical team. The test procedure is best described in Figure 4-8 according to test cycle periods and temperature limits, ranging between -31 °C to 61 °C.
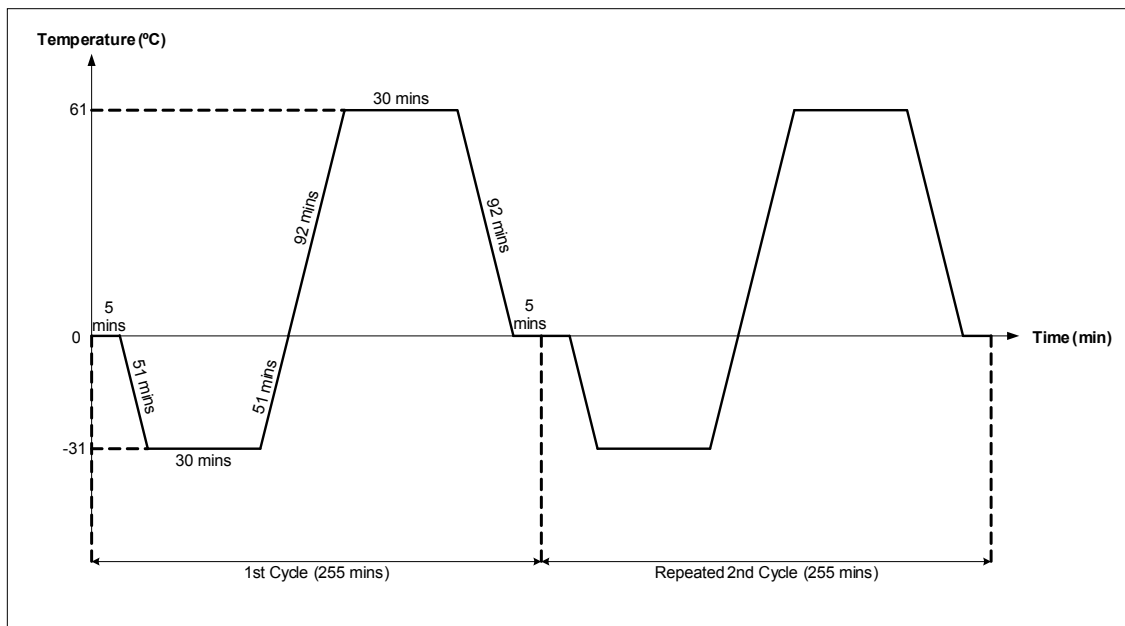
Figure 4-8: Temperature cycling test cycles and test periods

Figure 4-8 shows the temperature cycling test procedure adapted from F'SATI's required temperature profile. Presented in Figure 4-9 are the verification results from each sensor of the three power channels, which are described as follows:

- Minimum temperature: -31 ºC
- Maximum temperature: 61 ºC
- Temperature rise ramp: 1 ºC/min
- Temperature fall ramp: 1 ºC/min
- Dwell at maximum and minimum temperature: 30 minutes
- Total time: 520 minutes = 8.5 hours
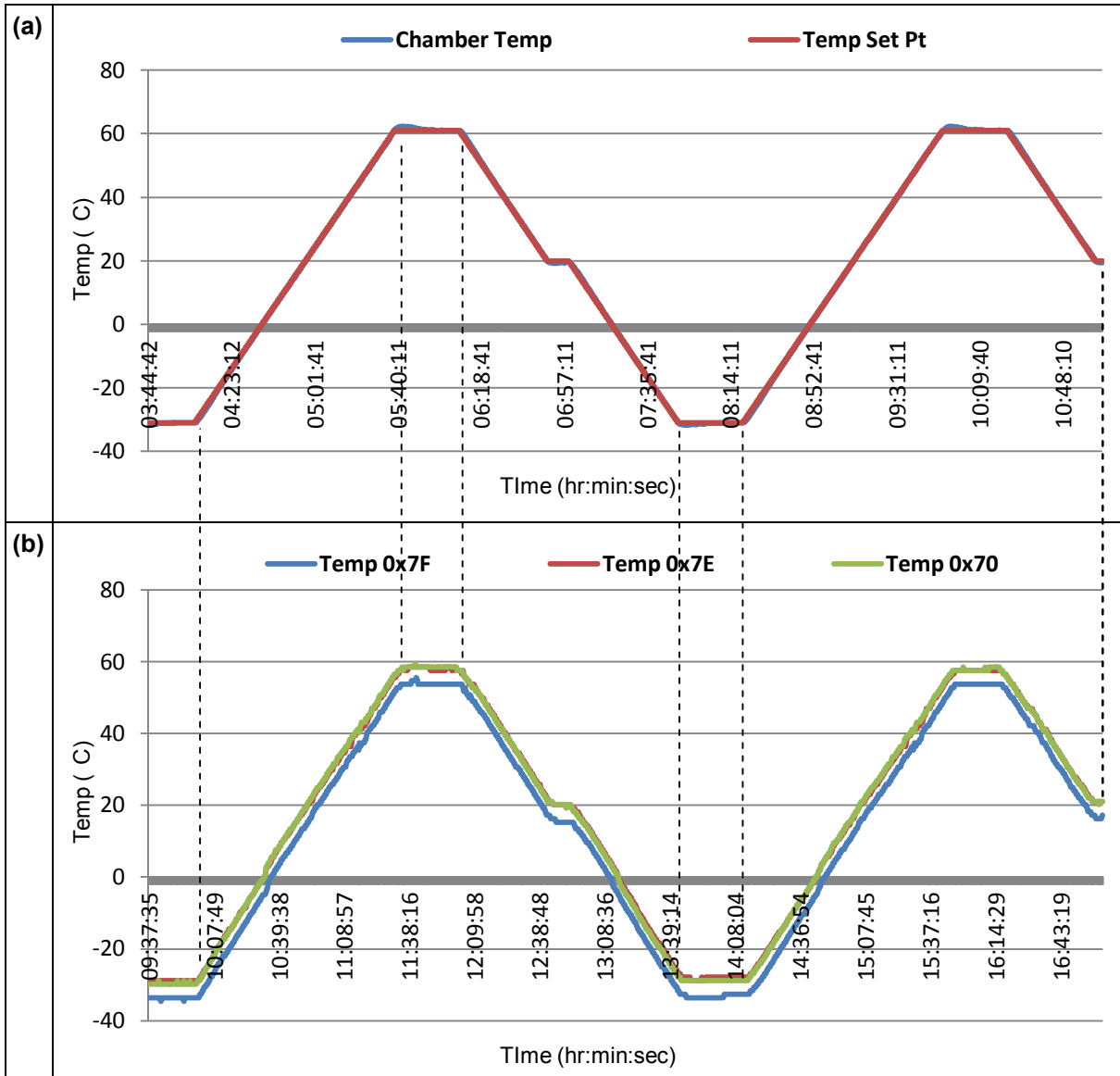
Figure 4-9: Verification comparison of (a) measured and pre-set chamber temperature vs. (b) temperature from PDM sensors

4.5.2 Functional Verification

Although only one power channel results are presented here to verify functionality of the PDM system, all three channels were tested and the results are presented in chapter five. Temperature variation profiles are presented in Figure 4-9 and follow the required profiles in Figure 4-8.

4.6   SUMMARY

In this chapter, all test procedures and verification methods are discussed. Firstly, a test platform is built, where the Arduino UNO development board, a power supply and an electronic load are interfaced as test equipment. All I^2C devices on the populated board are detected using an I^2C device scanning code programmed on the Arduino UNO board (see Appendix D). All functional requirements and specifications are verified to operate correctly. Similar functional tests are performed under environmental conditions and the results are presented in chapter five for all three tested channels.

CHAPTER 5:   RESULTS AND ANALYSIS

5.1   INTRODUCTION

The test setup, all test procedures and system verifications were covered in chapter 4. In this chapter, functional, irradiation and thermal cycling results are presented. Functional tests are done in an ideal laboratory environment as well as under environmental (irradiation and thermal) test conditions. The results are compared with the objective to analyse any abnormalities which may have occurred during environmental testing.

5.2   FUNCTIONAL TEST RESULTS

Current continuity and voltage efficiency measurements are verified in chapter 4. All four voltage busses are alternately loaded to verify their specified voltage ratings listed previously in chapter one (see Table 1-2). Herein, the functional results for all three power channels are presented in Figures 5-1(a) to (e), where all power channels (0x7F, 0x7E and 0x70) feed from the same power supply.

In Figures 5-1(a) shows the input voltage telemetry from each power channel. It is observed that the voltage of all three power channels varies by ±0.1 V every instant a trip or command is executed. This is due to the common power source connection.

In figures 5-1(b) - (d), the following trip conditions are verified to perform as required:
    A – software_trip command executed as coded;
    B – software_override command overrides trip condition as coded;
    C - Autonomous hardware_trip command executed when pre-set trip level is reached;
    D - Autonomous reset condition when load is varied until current is below trip level.

Figure 5-1(e) shows the temperature telemetry from each power channel sensor. Temperature telemetry from sensors in power channels 0x7E and 0x70 vary between 27 °C and 28 °C, which is the measured temperature in the laboratory. However, temperature telemetry from power channel 0x7F has an offset of about 5 °C.
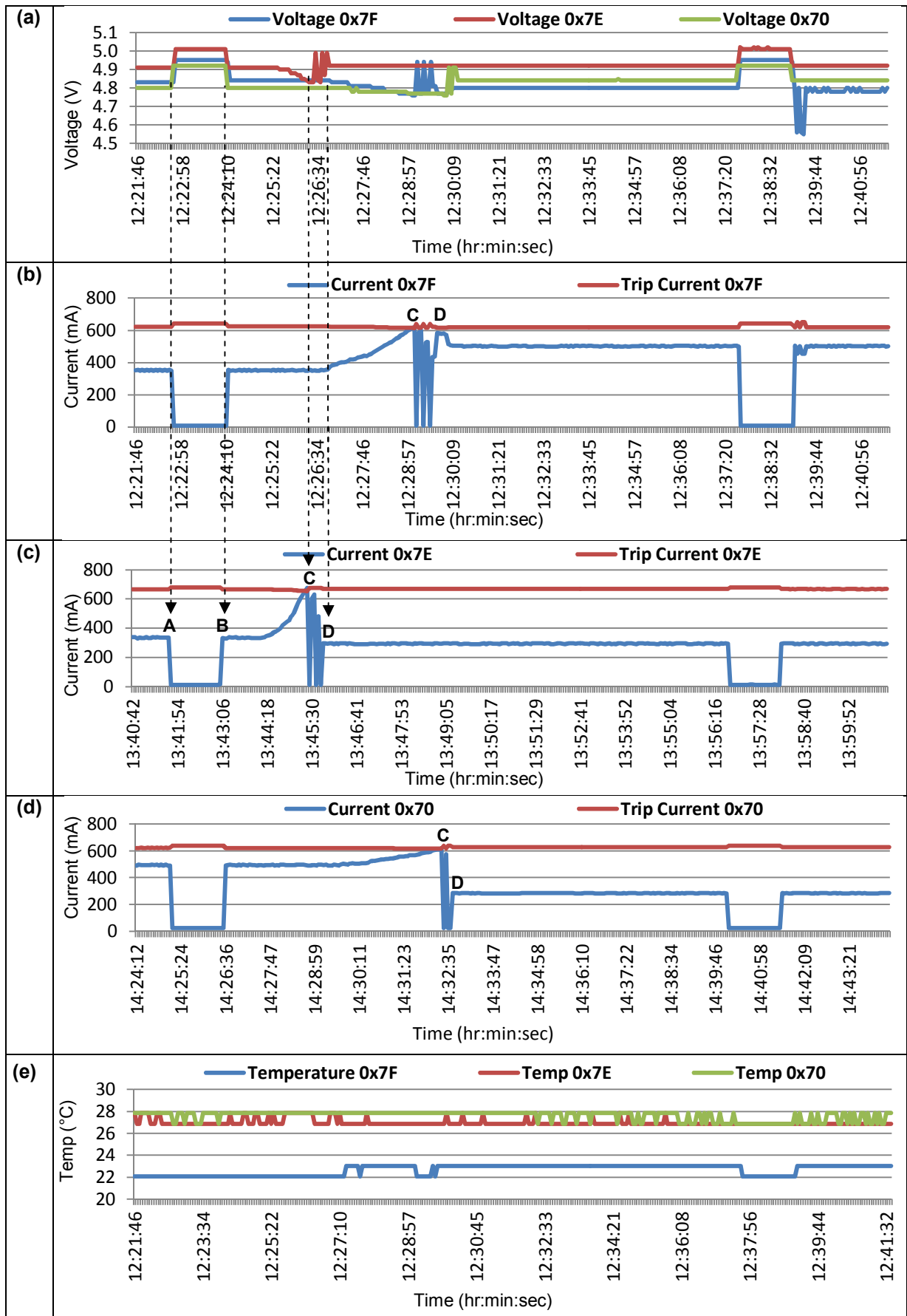
Figure 5-1: Functional test results showing (a) all channels' voltage telemetry, (b)-(d) load current telemetry and trip level of each channel and (e) all channels' temperature telemetry

It is suspected that this may be caused by manufacturing stresses because the sensor is received from a different distribution patch, which was given as free samples from the manufacturer. Later in this chapter, more accurate temperature measurements are verified when the PDM system performance is tested under an accurately monitored temperature cycled environment.

The test results shown in Figure 5-1 correspond to the verification results previously shown in chapter 4 (see Figure 4.7). Each channel is subjected to a 20 minute test cycle. All channels trip and reset accordingly, as required.

5.3   IRRADIATION TEST RESULTS

Irradiation test results are presented in Figure 5-2. The tests run from time 11:30:49 to 16:23:28 in 20 minute test cycles. More detailed irradiation test results are included in Appendix F (see Figure F-1 to Figure F-6). Critical points of abnormal functionality and telemetry received are concatenated and presented in Figures 5-2(a) - (c) using data used to plot the figures in Appendix F.

In Figures 5-2(a) - (c) the following activities are observed as labeled in the figures:

A – Voltage and temperature digital bit errors in the telemetry received from corresponding channels.

B – Software_trip command executed on all power channels.

C – Software_override command executed on all power channels.

D – Autonomous hardware_trip command executed on channel 0x7E which is connected to the variable load. At this point, the total irradiation dose is approximately **1.4 krad** (see Figure F-1 in Appendix F). This power channel's functional performance is nominal.

E – Autonomous reset condition executed.

F – Autonomous hardware_trip command executed on channel 0x70 connected to the variable load.

G – Autonomous reset condition executed.

H – Variable load resistance on channel 0x7E is varied.

I – Autonomous hardware_trip command **fails** to trip when current trip level is reached. At this point, the total irradiation dose is approximately **4.9 krad**.

J – With the system still failing to trip, and the total irradiation dose approaching **5.3 krad**, the current suddenly fluctuates between 400 mA and 1 A.
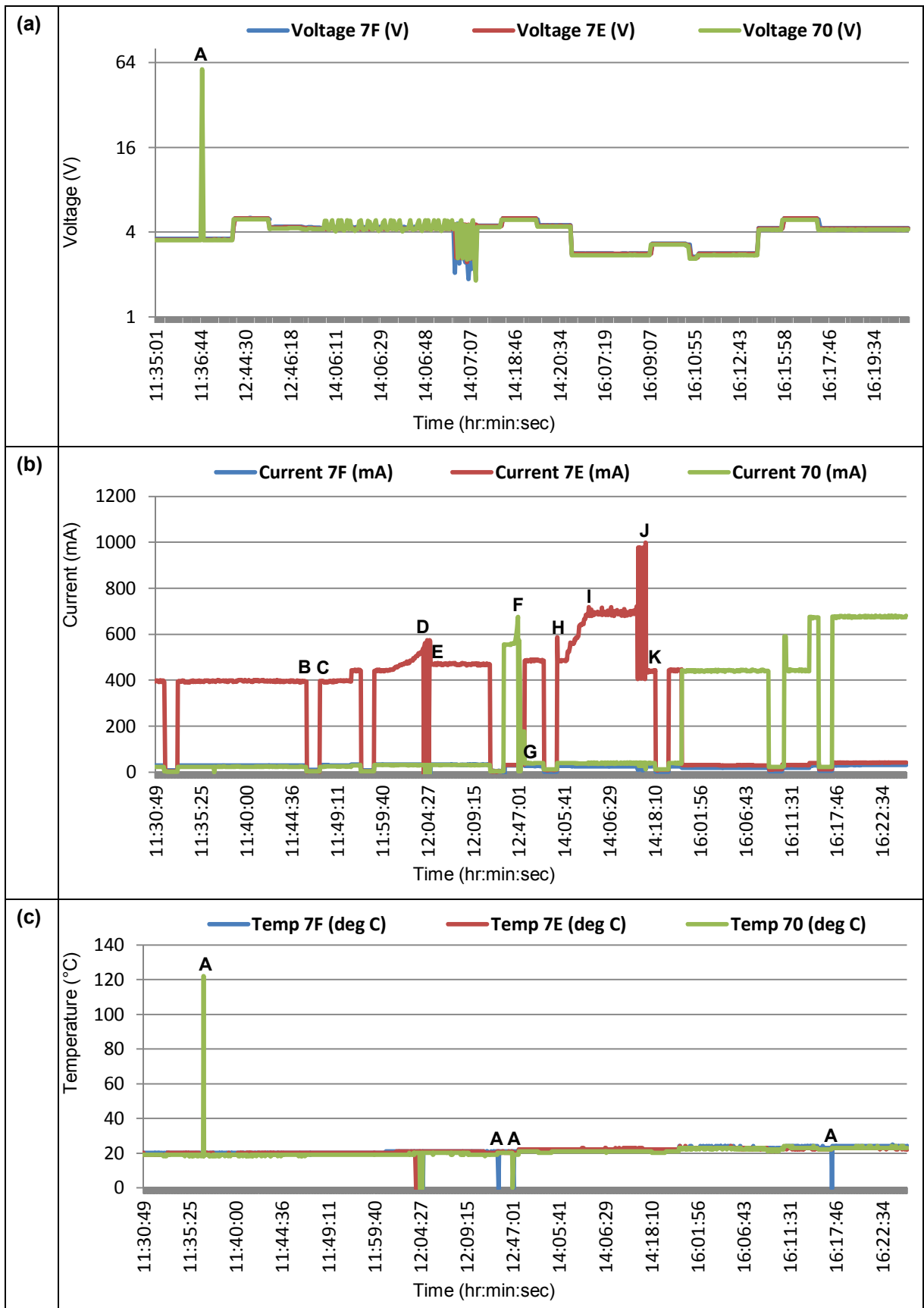
Figure 5-2: Irradiation test results showing (a) all channels voltage telemetry, (b) all channels' current telemetry and trip commands, (c) all channels' temeperature telemetry and (d) irradiation dose over the entire time interval

K – The current is decreased by varying the variable load and the irradiation test is continued with the observation noted that the internal amplifier in the MAX9611 current sensor failed to trip the current at 4.9 krad dose. It is therefore noted that the internal amplifier could have failed anywhere between 1.4 krad and 4.9 krad.

5.4 THERMAL CYCLING TEST RESULTS

Thermal cycling test results are shown in Figure 5-3(a) – (d). It should be noted that only one variable load meter was available. Therefore, because the thermal cycling tests cannot be interrupted, only power channel 0x7F is connected to the load meter. Results show that the PDM system meets all performance specifications similar to the functional test results. Voltage and current telemetry is nominal. Temperature variation is measured accurately. However, it is again noted that the sensor in power channel 0x7F has a temperature offset of about 5 °C.

The thermal cycling functional test results are interpreted according to the alphabetic labels in Figure 5-3(b) as follows:

A – Software_trip command executed on all power channels.

B – Software_override command executed on all power channels.

C – Autonomous hardware_trip command executed on channel 0x7F, which is connected to the variable load.

D – Autonomous reset condition executed.
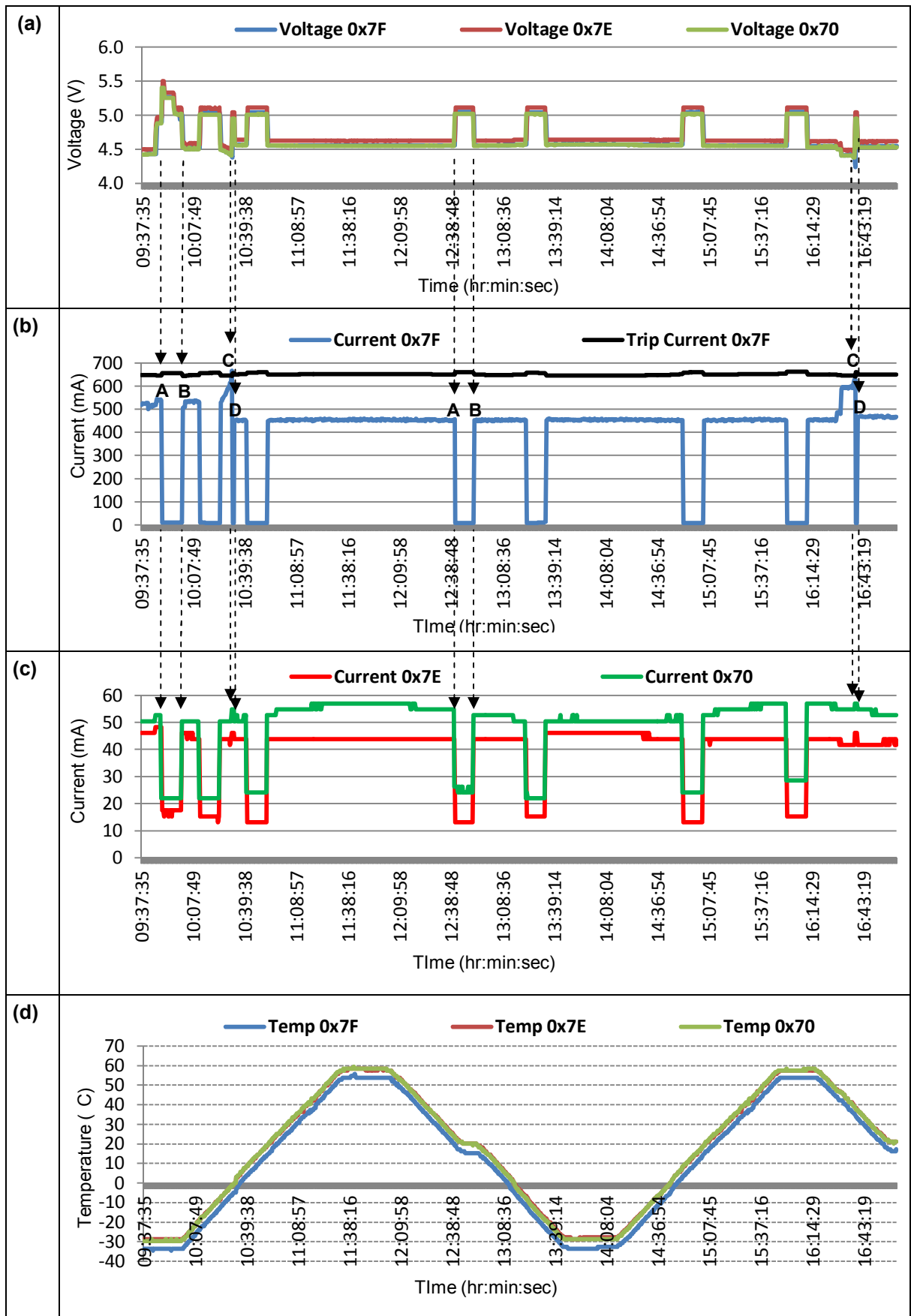
Figure 5-3: Thermal cycling test results showing (a) all channels' voltage telemetry, (b) channel 0x7F current telemtry and trip level, (c) channels 0x7E and 0x70 current telemetry and (d) all channels' temperature telemetry inside thermal chamber

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5.5 SUMMARY

Functional, irradiation and thermal cycling tests results were presented. Functional tests under laboratory conditions satisfied the specifications. Following similar functional test procedures, environmental irradiation and thermal cycling tests results were presented. Hardware trip commands interrupted the I^2C communication bus during irradiation tests; as a result the sensors gave random fluctuating readings. The hardware trip command was not triggered again and the PDM system survived the rest of the irradiation test up to 10 krad. Two thermal cycles were processed for the thermal cycling test and the PDM maintained proper functionality for the entire test duration.

CHAPTER 6: CONCLUSIONS AND RECOMMENDATIONS

6.1 INTRODUCTION

The electrical power subsystem (EPS) from Clyde Space currently used in the F'SATI satellite projects distributes three voltage busses; 3.3 V bus, 5 V bus and one unregulated battery bus of 6.2 V to 8.4 V. The power subsystem as one unit does not include a reliable fault tolerant power distribution module (PDM) to ensure subsystem loads are protected from over-currents, over-temperatures and over-voltage faults which can cause unexpected inrush currents or latchup conditions. To make the EPS reliable, a PDM system was researched and developed to be interfaced as an additional module to the EPS. The primary research objective was to develop a PDM prototype for a CubeSat application which can reliably distribute power to CubeSat subsystem loads.

6.2 CONCLUSIONS

A reliable power distribution module was developed considering space environmental effects on electronics, reliable logic design and fault tolerant system designs. Analogue logic circuits using bipolar junction transistors (BJTs) are known to be highly reliable in space due to their less susceptibility characteristic to space radiation. The PDM was designed using this technology to make the system highly reliable for space applications.

Standard low power busses are used in F'SATI CubeSats are a 3.3 V regulated bus; a 5 V regulated bus; and a 6.2-8.4 V unregulated bus. A 12 V regulated bus was added to the PDM design for future 3U CubeSat missions which may need higher voltage requirements than the highest unregulated battery bus.

The module was designed to have eight (8) identical power distribution channels, where each channel is operationally independent from all other channels. In this manner, any power channel that fails will not affect operation of the remaining power channels of the PDM. In addition, two or more power channels can be connected in parallel at manufacture time to create a same-design redundant system (refer to section 2.6.1).

Each power channel provides continuous current, voltage and temperature telemetry via an I^2C communication bus. This telemetry is intended for the on-board-computer (OBC), which shall use the telemetry to command housekeeping instructions to trip power switches and isolate subsystem loads when the received telemetry exceeds pre-set trip levels.

The module was designed to have an autonomous hardware trip function for each power channel. This is used to automatically trip a power switch when a fault condition is detected. As a diverse-design redundant technique (see section 2.6.2), a software controllable trip functionality is featured for each power channel as backup to the autonomous hardware trip functionality.

The module features a software controllable override function. The override function is a software-executed command that is used to override both trip commands and execute a forced reset condition in case a power channel is stuck in a continuous trip mode.

A meaningful functional test procedure was outlined. The functionality of the PDM prototype was tested in the F'SATI laboratory where three randomly selected power channels were tested. Only three power channels were tested due to limited availability of components and test equipment. The module's functional performance was verified to meet all functional specifications.

Irradiation functional tests and thermal functional tests assess the prototype's endurance in the expected space environment. The prototype's functionality was tested in a thermal cycling chamber and a Gamma irradiation source chamber. The prototype was found to meet all functional specifications similar to those defined for the functional tests. During thermal cycling tests, the PDM system was operated continuously for two thermal cycles between -31 °C and 61 °C. However, a temperature offset of approximately 5 °C was noted from the 0x7F power channel's current sensor. It was observed that temperature telemetry from the other two power channels' sensors, 0x7E and 0x70, were accurate. Soldering joints on the 0x7F sensor were critically checked to investigate if there was a better thermal connection on the 0x7E and 0x70 devices as compared to the 0x7F device. All solder joints were, however, properly soldered. The 0x7F sensor was distributed by the manufacturer as part of a free samples batch. It is possible that the device from the samples batch could have experienced pre-irradiation elevated temperature stresses (PETS) during the manufacturing process (refer to section 2.3.3.2).

During the irradiation tests it was found that the autonomous hardware trip function failed at some point between 1.4 krad and 4.9 krad. Nevertheless, the system was tested up to 9.8 krad. All other functional specifications were met. The current path could still be isolated by the software trip function.

The developed module is a fully redundant 8 power channel distribution system. The tested prototype tolerates beyond the expected low Earth orbit (LEO) temperature and radiation doses and could be a useful technology in future nanosatellite missions. The philosophy behind this design may also be useful for larger satellite missions in the implementation of redundant systems.

6.3 FUTURE WORK RECOMMENDATIONS

The objectives for this research project have been met. For those interested in future work related to this research project, it is recommended to determine the exact irradiation dose where the internal comparator of the MAX9611 current sensor failed to execute the autonomous trip function during the irradiation tests. This would give more accurate results as to the radiation levels the device can tolerate.

To achieve this, it is recommended to test the prototype using an active load instead of the variable load. One could consider a T0220 BJT interfaced as a load to the PDM power outputs as shown in Figure 6-1. In this configuration, the BJT is switched harder ON by a saw-tooth signal from a signal generator, thereby increasing the transistor's loading ability. However, further research needs to be done to determine the size from the power dissipated in the transistor.

This active loading technique could be designed and developed as a separate module which may later possibly be used for other load test applications. However, it is critical to design the active load to tolerate the high power that is expected to be dissipated in the transistor when the load resistance decreases towards zero ohm, and extreme heat is expected from the BJT.
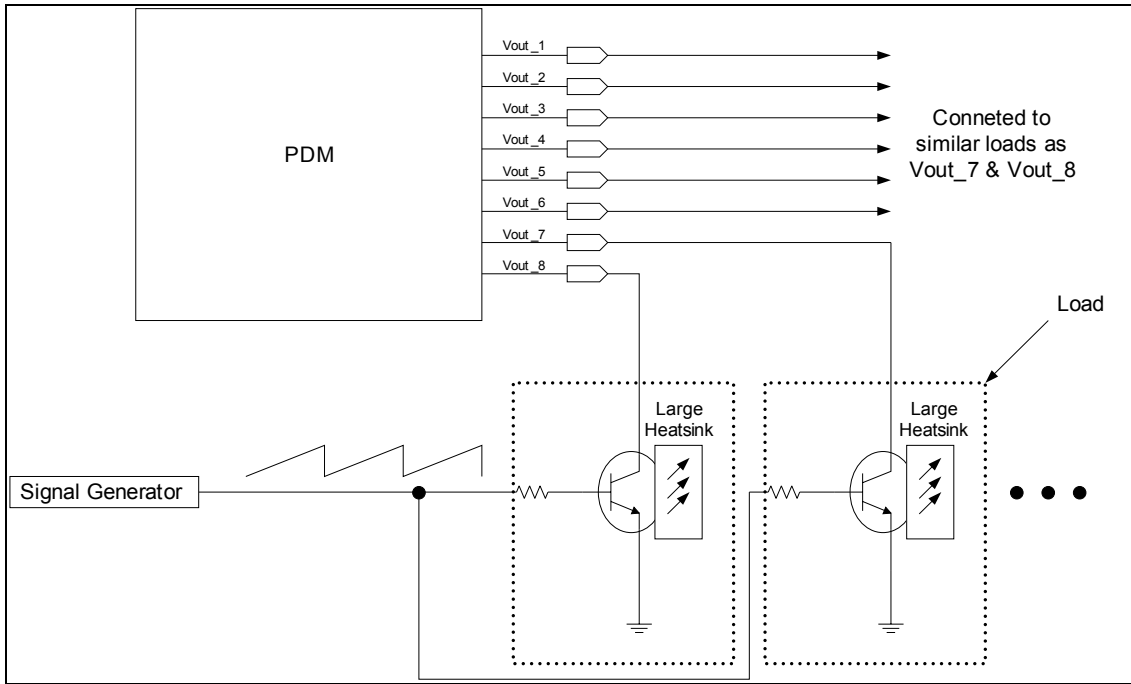
Figure 6-1: Variable active loading using a BJT mounted on a heatsink and switched harder ON by a varied sawtooth ramp current source from a signal generator

Using the active load configuration in Figure 6-1, the load current will increase slowly up to the required pre-set current trip level, thereby allowing the autonomous hardware trip (AHT in Figure 6-2) command to be executed by the internal comparator of the MAX9611 current sensor. The expected output waveform is shown in Figure 6-2, where the AHT and autonomous reset (AR) points can be identified accurately when failing to trip the power channel. The corresponding irradiation dose may then be captured.
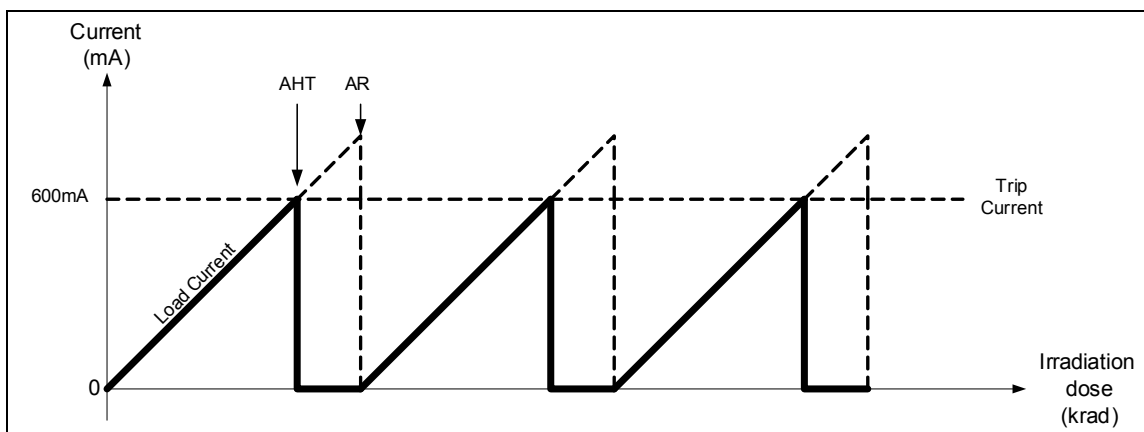
Figure 6-2: Expected output curve of load current for testing the autonomous trip functions using an active load

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APPENDIX A: ALTIUM DXP TOP LEVEL DESIGN
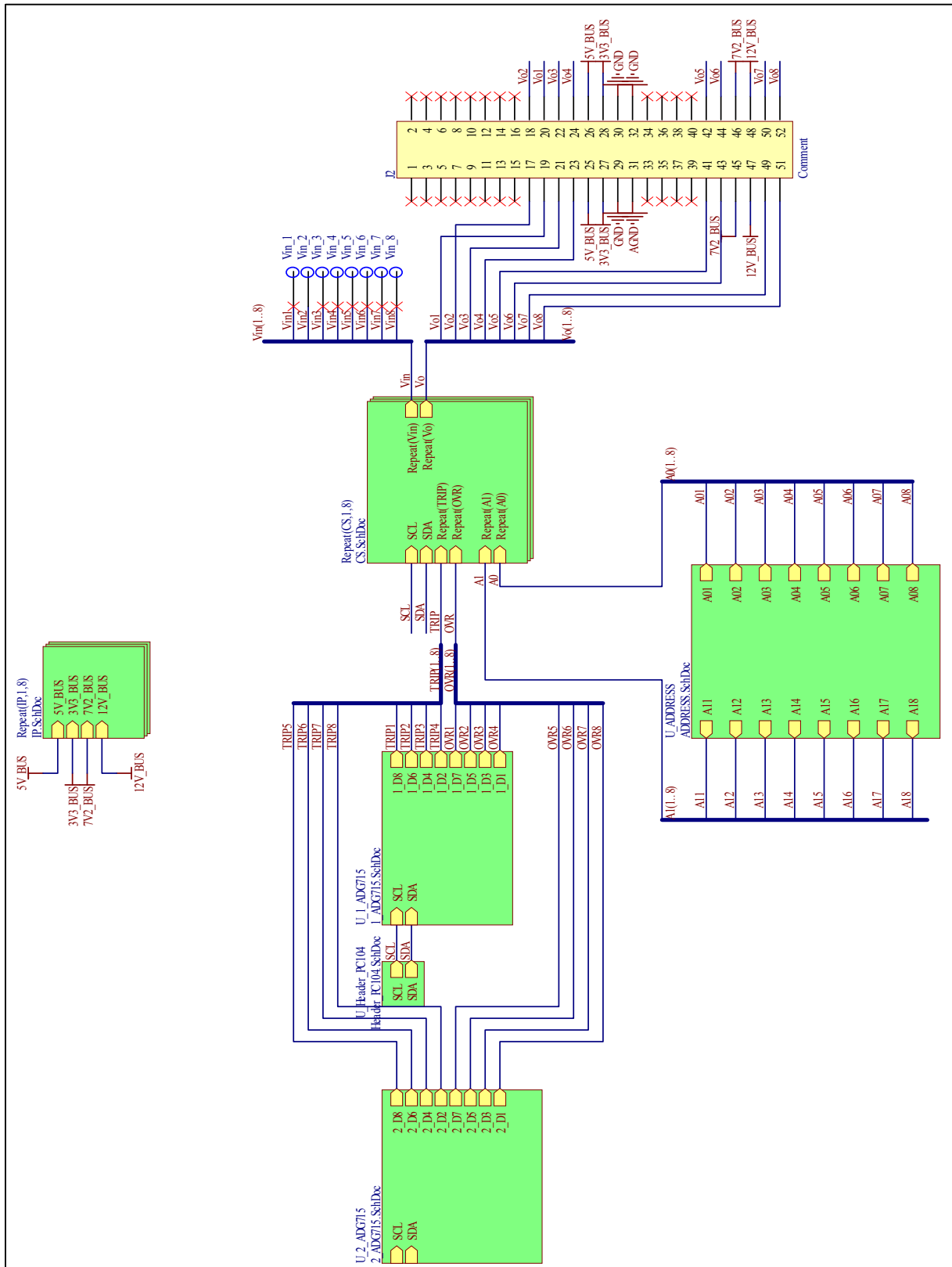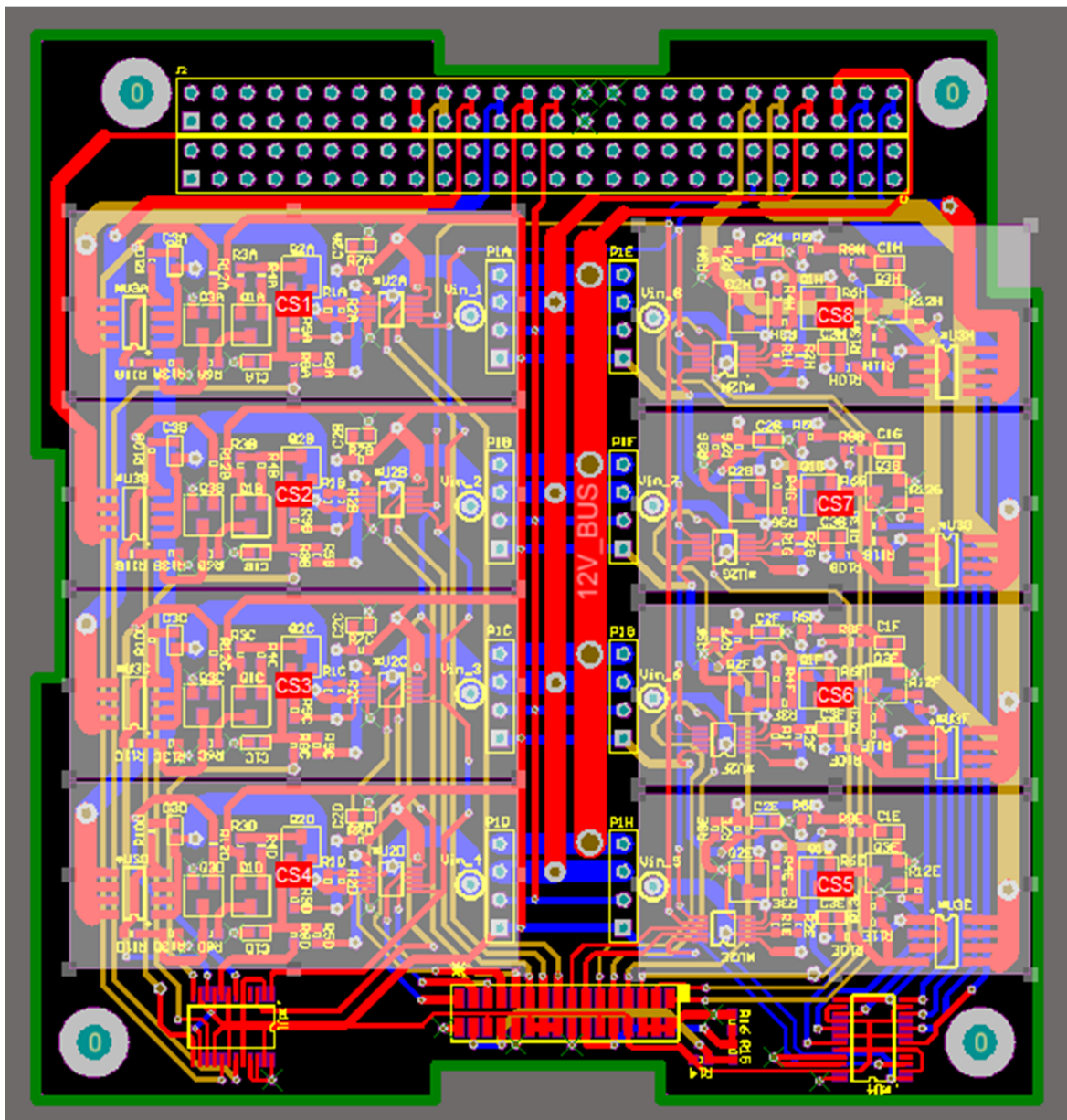
APPENDIX B: ALTIUM DXP MULTI-CHANNEL PCB LAYOUT

Figure B-1: Altium DXP final PCB layout showing repeated channels 1 to 4 and 5 to 8.
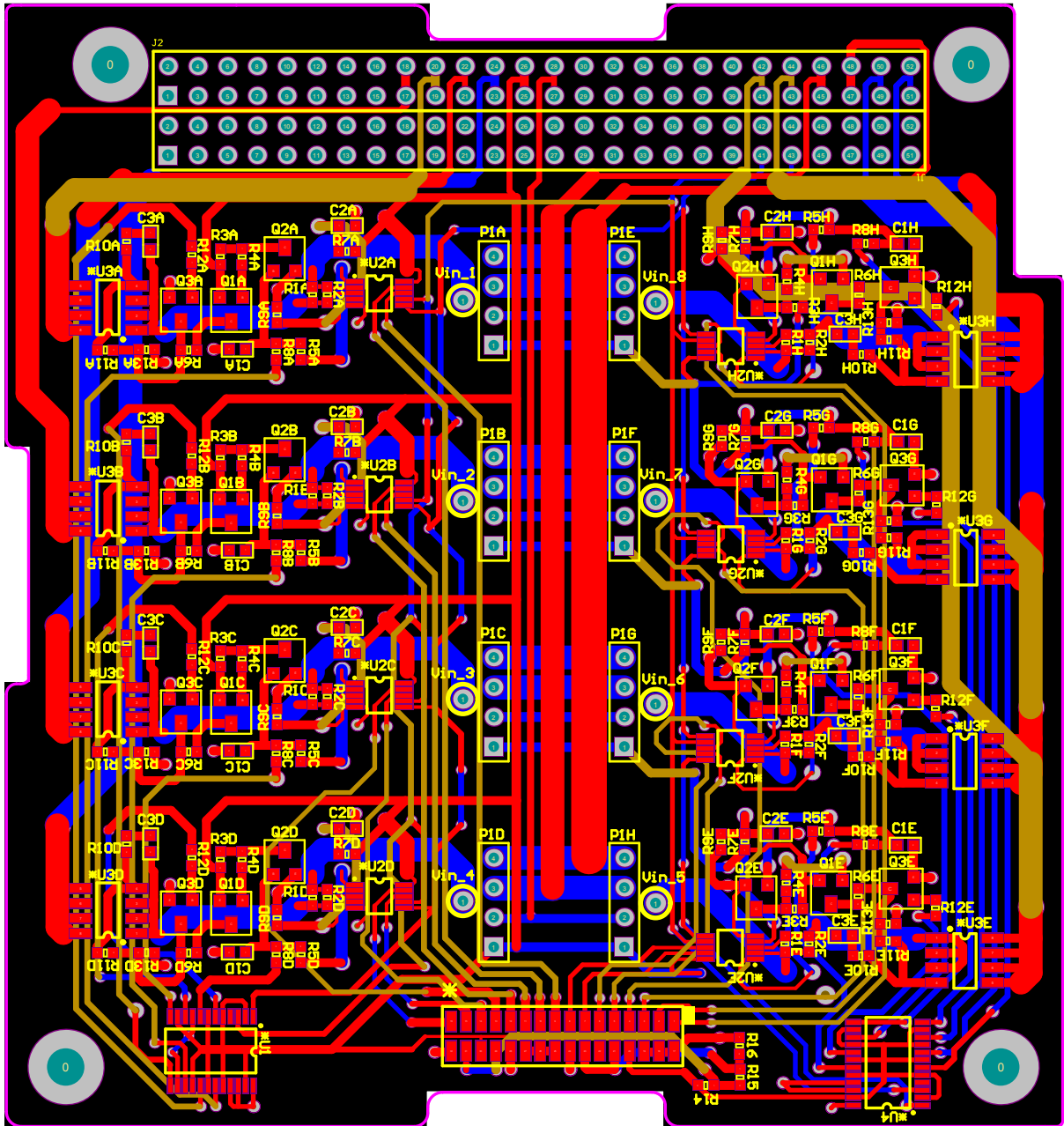
Figure B-2: Altium DXP final PCB layout of PDM sent to TRAX for prototyping.

APPENDIX C: PCB PROTOTYPE

ADG715 I^{2}C switch ◄
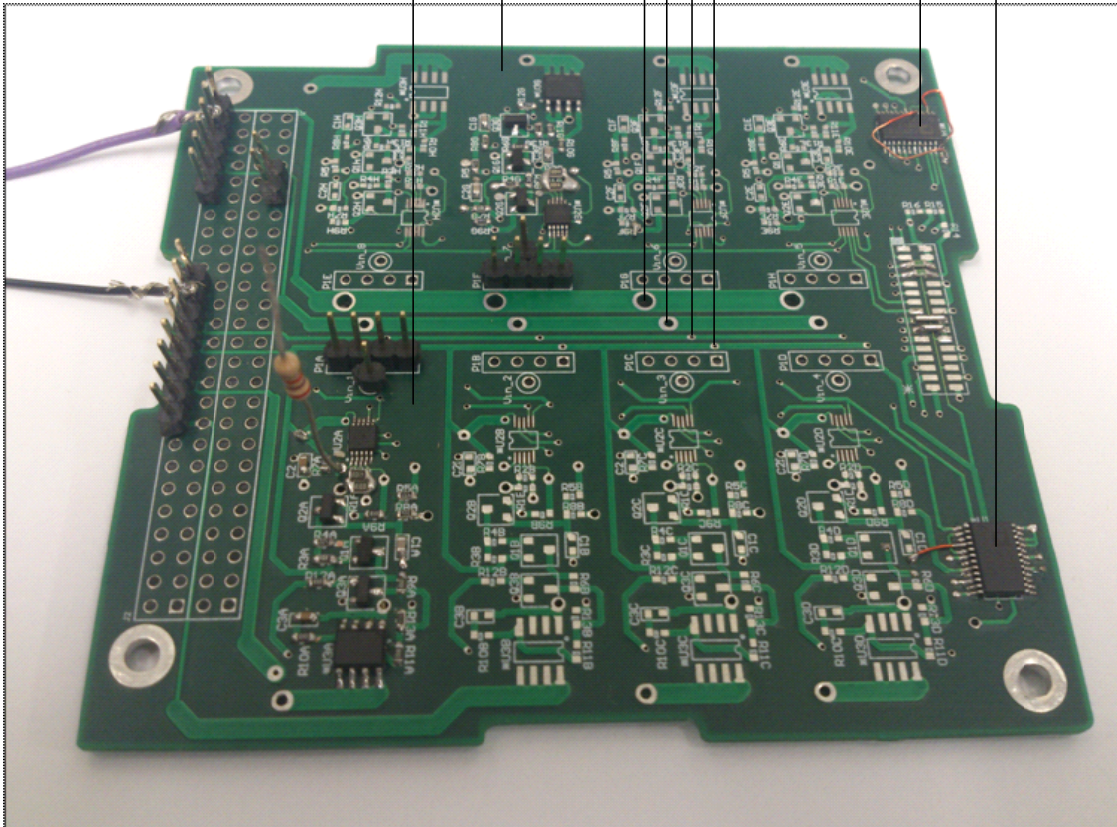
ADG715 I^{2}C switch ◄

5V bus ◄

3.3V bus ◄

7.2V bus ◄

12V bus ◄

Power channel 7 ◄

Power channel 1 ◄

APPENDIX D: I²C SCANNER CODE

```
#include <Wire.h>

void setup()
{
Serial.begin (9600);
  // Leonardo: wait for serial port to connect
while (!Serial)
   {

   }
Serial.println ();
Serial.println ("I2C scanner. Scanning ...");
byte count = 0;

Wire.begin();
for (byte i = 1; i < 128; i++)
 {
Wire.beginTransmission (i);
if (Wire.endTransmission () == 0)
    {
Serial.print ("Found address: ");
Serial.print (i, DEC);
Serial.print (" (0x");
Serial.print (i, HEX);
Serial.println (")");
count++;
delay (1);  // maybe unneeded?
   } // end of good response
 } // end of for loop
Serial.println ("Done.");
Serial.print ("Found ");
Serial.print (count, DEC);
Serial.println (" device(s).");
}  // end of setup

void loop()
{
}
```

APPENDIX E: FUNCTIONAL TESTING CODE

```
// Power Distribution Module Functional Code
// Written by Motlokwe Maleka
// Date: 16th May 2013

#include "Wire.h"

double MAX9611_voltage, MAX9611_current, MAX9611_temperarure, MAX9611_set, Load_power;
double volts, current, temp, set, power;
intmsb, lsb, temp_MSB, temp_LSB;
floati_set, ADG_data;
doubletempresolution = 0.48;
float x = 0, n = 0;
int address = 0x7F, time = 0;
int row = 0;
intvar = 1, z = 0;

void setup()
{
Serial.begin(9600);
Wire.begin();
Wire.beginTransmission(0x48);                    //I2C switch for power channel 1 to 4
Wire.write(0x00);                      //RESET IC
Wire.endTransmission();

Serial.println("CLEARDATA");
Serial.print("LABEL,Time,Volts 0x7F,Current 0x7F,Trip Current 0x7F,Temp 0x7F,Volts 0x7E,Current 0x7E,Trip
Current 0x7E,Temp 0x7E,");
Serial.println("Volts 0x70,Current 0x70,Trip Current 0x70,Temp 0x70,");

Wire.beginTransmission(address);
Wire.write(0x0A);        //Control register 1
Wire.write(0xF7);        //Comparator mode, LR Reset if latched, SHDN normal operation, read all channels every
2ms
Wire.endTransmission();

Wire.beginTransmission(0x48);  //I2C switch for power channel 1 to 4
Wire.write(0x00);            //set all switches to be OFF
Wire.endTransmission();

Wire.beginTransmission(0x49);  //I2C switch for power channel 1 to 4
Wire.write(0x00);            //set all switches to be OFF
Wire.endTransmission();
```

```
}


void loop()                    //loop function repeats itself
{
if(x==50)
   {
     SOFTWARE_TRIP();  //first trip point
   }


if(x==120)
   {
     SOFTWARE_OVERRIDE();  //override first trip condition
   }


if(x==800)
   {
     SOFTWARE_TRIP();  //second trip point
   }


if(x==870)
   {
     SOFTWARE_OVERRIDE();  //override second trip condition
   }


switch (var)
   {
case 1:
address = 0x7F;    //channel one sensor I2C address
break;
case 2:
address = 0x7E;    //channel three sensor I2C address
break;
case 3:
address = 0x70;    //channel eight sensor I2C address
break;
   }


Wire.beginTransmission(address);
Wire.write(0x0A);        //Control register 1
Wire.write(0xF7);          //Comparator mode, LR Reset if latched, SHDN normal operation, read all channels every
2ms
Wire.endTransmission();
delay(20);
```

```
volts = get_MAX9611_voltage();      //get voltage reading
delay(10);

current = get_MAX9611_current();    //get current reading
delay(20);

set = get_MAX9611_set();            //get set voltage reading
i_set = set/(2.5*0.052)*1000;       //calculate trip current according to set voltage
delay(10);

temp = get_MAX9611_temperarure();  //get temperature reading
delay(10);

power = get_MAX9611_power();     //calculate power accross the load
delay(10);


switch (var)
   {
case 1:
address = 0x7F;
printData7F();    //print data for power channel one
break;
case 2:
address = 0x7E;
printData7E();    //print data for power channel three
break;
case 3:
address = 0x70;
printData70();    //print data for power channel eight
break;
   }

row++;      //move to next row on Excel sheet
x++;
var++;
if(var==4)
   {
var=1;   //move back to print channel one data
   }
   //delay(100);     //approximately half a second sampling
//delay(1100);    //5 seconds sampling
delay(9500);    //30 seconds sampling

}
```

```
//******** This function prints data for power channel one **********
void printData7F(void)
{
Serial.print("DATA,TIME,");
Serial.print(volts);
Serial.print(",");
Serial.print(current);
Serial.print(",");
Serial.print(i_set);
Serial.print(",");
Serial.print(temp);
Serial.print(",");
  //Serial.print(power);
  //Serial.print(",");
delay(10);


}


//******** This function prints data for power channel three **********
void printData7E(void)
{
Serial.print(volts);
Serial.print(",");
Serial.print(current);
Serial.print(",");
Serial.print(i_set);
Serial.print(",");
Serial.print(temp);
Serial.print(",");
delay(10);


}


//******** This function prints data for power channel one **********
void printData70(void)
{
Serial.print(volts);
Serial.print(",");
Serial.print(current);
Serial.print(",");
Serial.print(i_set);
Serial.print(",");
Serial.print(temp);
```

```
Serial.print(",");
Serial.println(" ");
delay(10);
}



//******** This function reads and converts voltage from the MAX9611 current sensor ***********
double get_MAX9611_voltage(void)
{
Wire.beginTransmission(address);
Wire.write(0x02);
Wire.endTransmission();

Wire.requestFrom(address,2);
msb = Wire.read();
lsb = Wire.read();
Wire.endTransmission();

   MAX9611_voltage = ((msb)<<4)+(lsb>>4);
   MAX9611_voltage = ((MAX9611_voltage/4096)*57.3);

return MAX9611_voltage;
}



//******** This function reads and converts current from the MAX9611 current sensor ***********
double get_MAX9611_current(void)
{
Wire.beginTransmission(address);
Wire.write(0x00);
Wire.endTransmission();

Wire.requestFrom(address,2);
msb = Wire.read();
lsb = Wire.read();
Wire.endTransmission();

   MAX9611_current = ((msb)<<4)+(lsb>>4);
   MAX9611_current = (((.44/4096)*MAX9611_current)/.049)*1000;

return MAX9611_current;
}
```

```c
//******** This function reads and converts die temperature from the MAX9611 current sensor ***********
double get_MAX9611_temperarure(void)
{
int i, sign, temp1;            //added sign and temp1. JZ 05/21/2012
double temperature;

Wire.beginTransmission(address);
Wire.write(0x08);
Wire.endTransmission();

Wire.requestFrom(address,2);
temp_MSB = Wire.read();
temp_LSB = Wire.read();
Wire.endTransmission();

  // changed for MAX9611 internal temperature output (9 bits with sign). JZ 05/21/2012
sign = (temp_MSB>>8 & 0x1);            //extract sign bit
  temp1 = (((temp_MSB<<1) & 0xFE)|((temp_LSB>>8)&0x1));   //extract internal temperature ADC steps
if(sign)
   {
temperature = (-1)*((~temp1 & 0xFF) + 1)*tempresolution;        //sign bit=1, temperature is negative (two's
compliment)
   }
else
   {
temperature = temp1 * tempresolution;        //otherwise, the temperature is a positive number
   }

return temperature ;        //temp in Deg

}


//******** This function reads and converts the set voltage from the MAX9611 current sensor ***********
double get_MAX9611_set(void)
{
Wire.beginTransmission(address);
Wire.write(0x07);
Wire.endTransmission();

Wire.beginTransmission(address);
Wire.write(0x06);
Wire.endTransmission();

Wire.requestFrom(address,2);
```

```
msb = Wire.read();
lsb = Wire.read();
Wire.endTransmission();

    MAX9611_set = ((msb)<<4)+(lsb>>4);
    MAX9611_set = ((MAX9611_set/4096)*1.126);    //Vset max is 1.126V full-scale

return MAX9611_set;
}



//******** This function calculates the power in the load ***********
double get_MAX9611_power(void)
{
Load_power = (current/1000) * volts;
returnLoad_power;
}



//******** This function executes the software trip commands on all three channels ***********
void SOFTWARE_TRIP(void)
{
Wire.beginTransmission(0x48);  //I2C switch for power channel 5 to 8
Wire.write(0x88);            //Trip power channel 1 and 3
Wire.endTransmission();

Wire.beginTransmission(0x49);  //I2C switch for power channel 5 to 8
Wire.write(0x02);            //Trip power channel 7
Wire.endTransmission();
}



//******** This function executes the software override commands on all three channels ***********
void SOFTWARE_OVERRIDE(void)
{
Wire.beginTransmission(0x48);  //I2C switch for power channel 1 to 4
Wire.write(0x44);            //Trip channel 1
Wire.endTransmission();

Wire.beginTransmission(0x49);  //I2C switch for power channel 1 to 4
Wire.write(0x01);            //Trip channel 1
Wire.endTransmission();
}
```

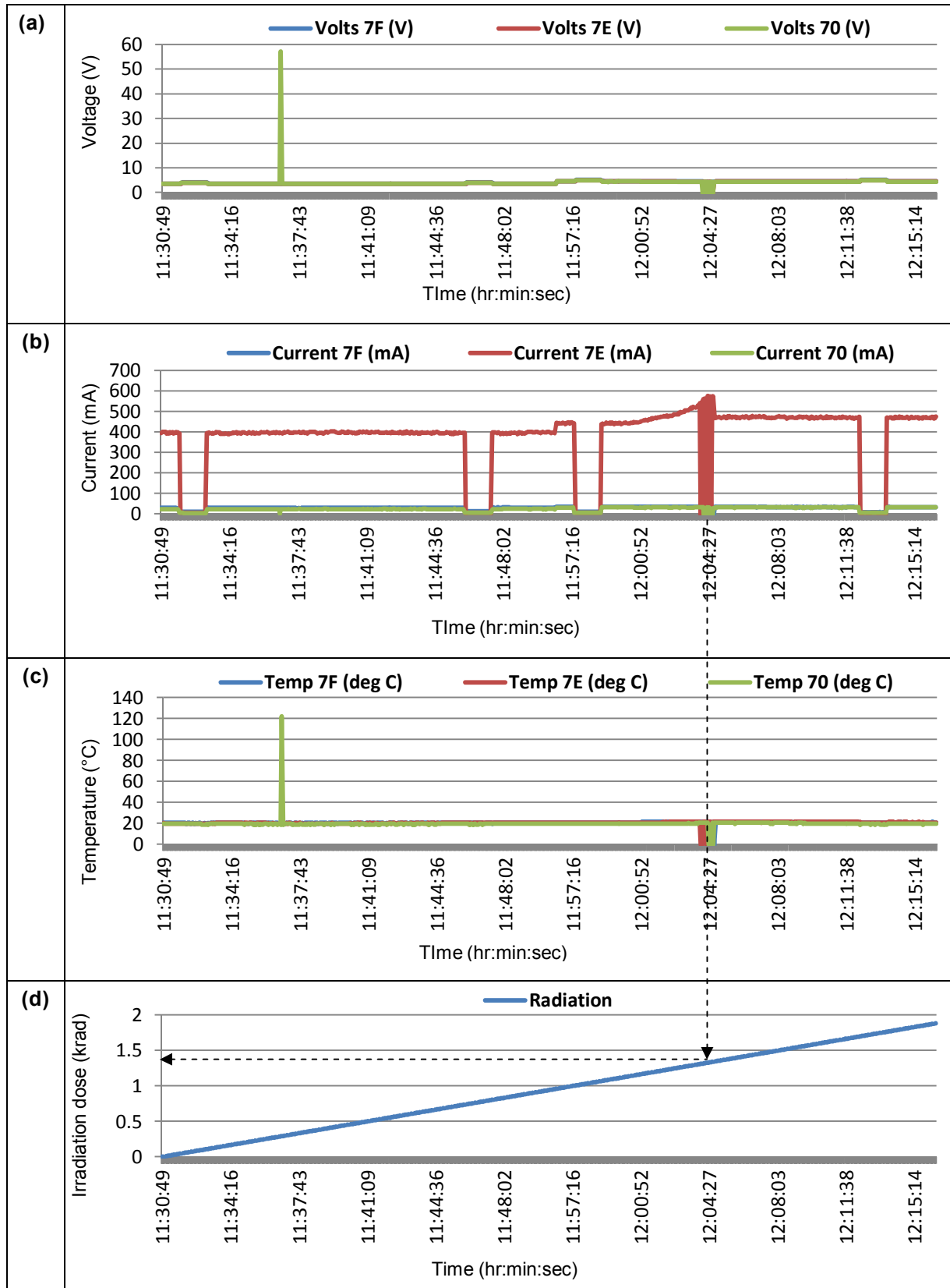# APPENDIX F: RADIATION TEST RESULTS

Figure F- 1: 0 – 1.88 krad irradiation dose test results with power channel 0x7E connected to the variable load and all channels' telemetry of (a) voltage, (b) current, (c) temperature and (d) the radiation dose over a 20 minutes timeframe
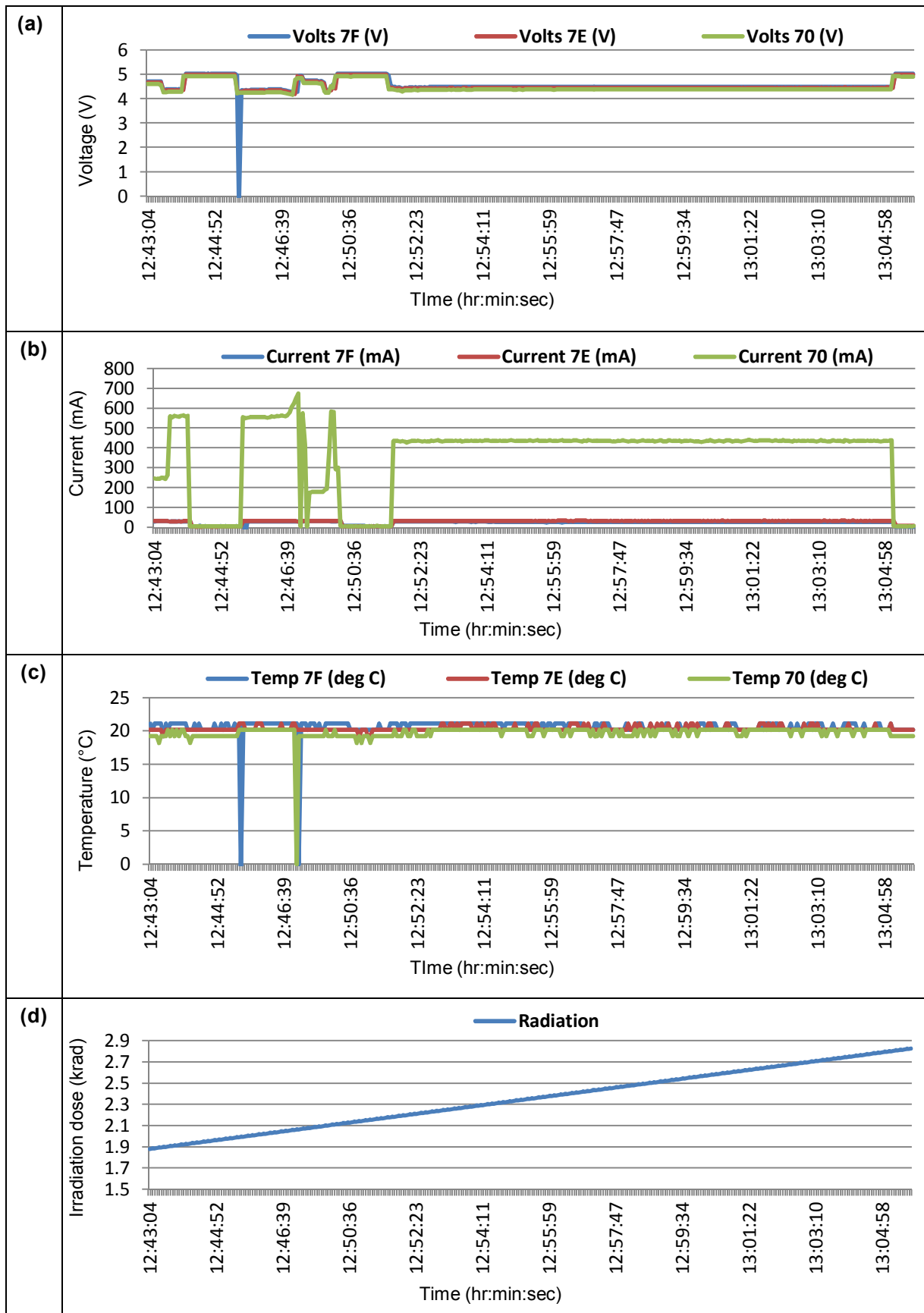
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Figure F- 2: 1.88 – 2.82 krad irradiation dose test results with power channel 0x70 connected to the variable load and all channels' telemetry of (a) voltage, (b) current, (c) temperature and (d) the radiation dose over a 20 minutes timeframe
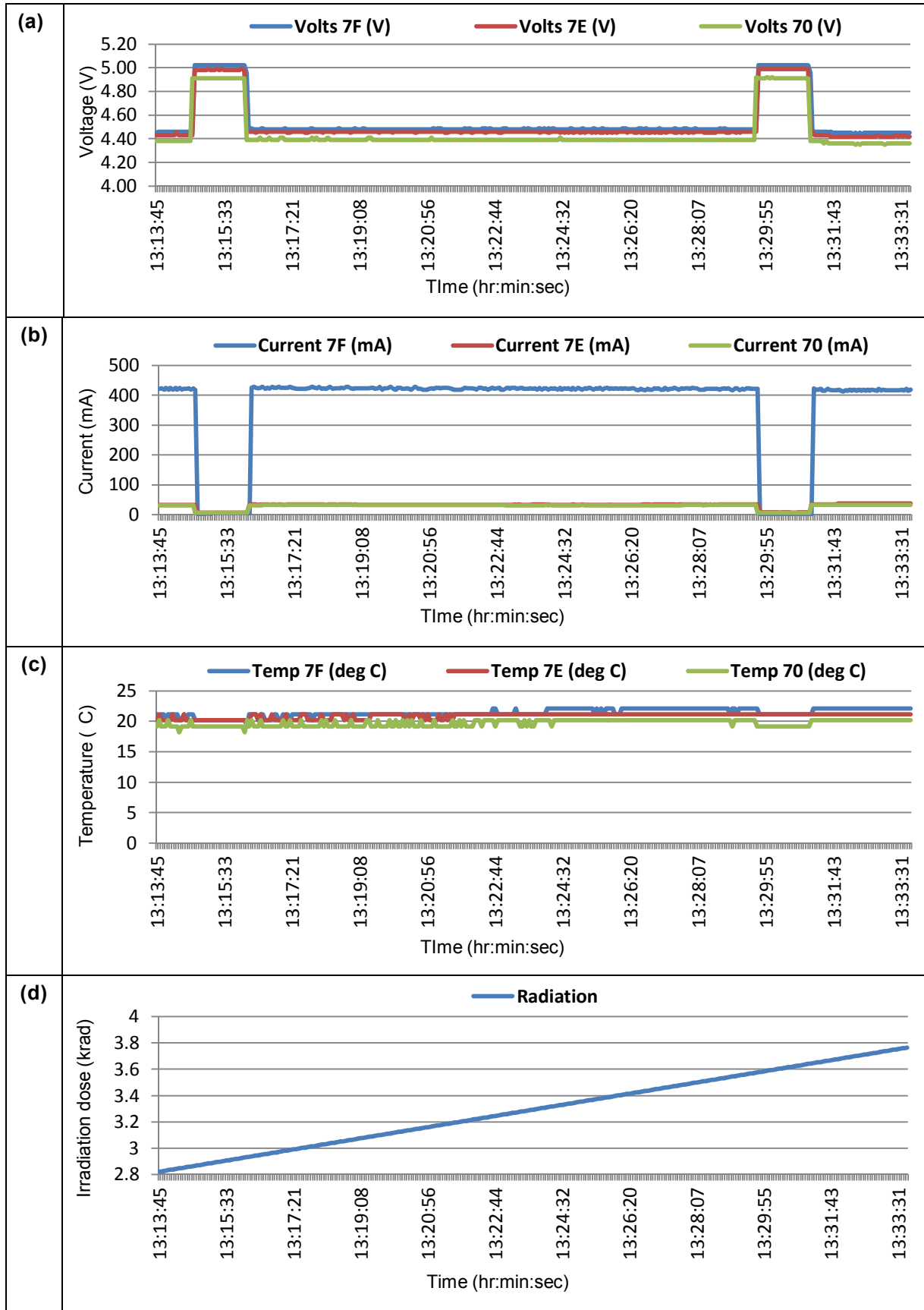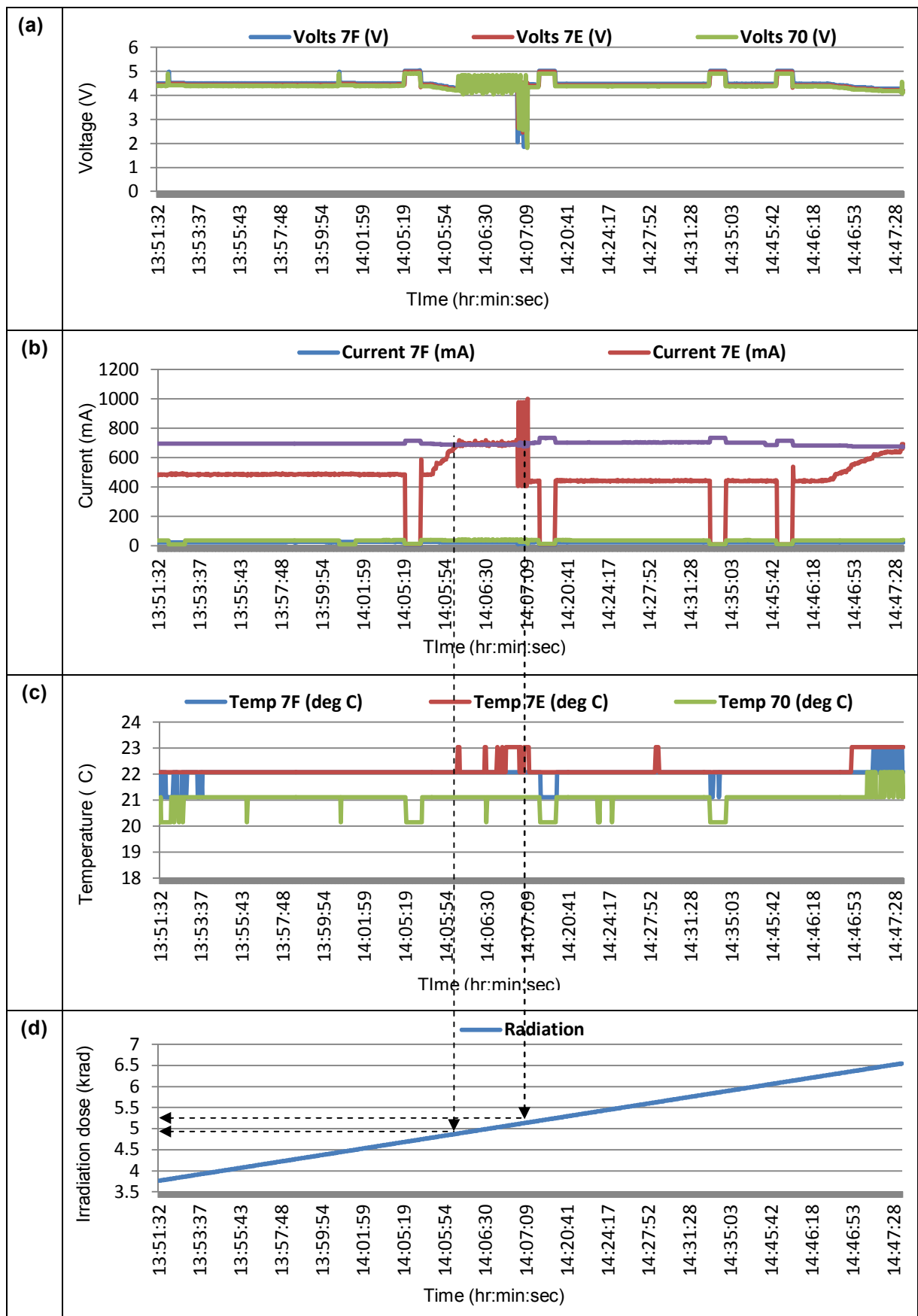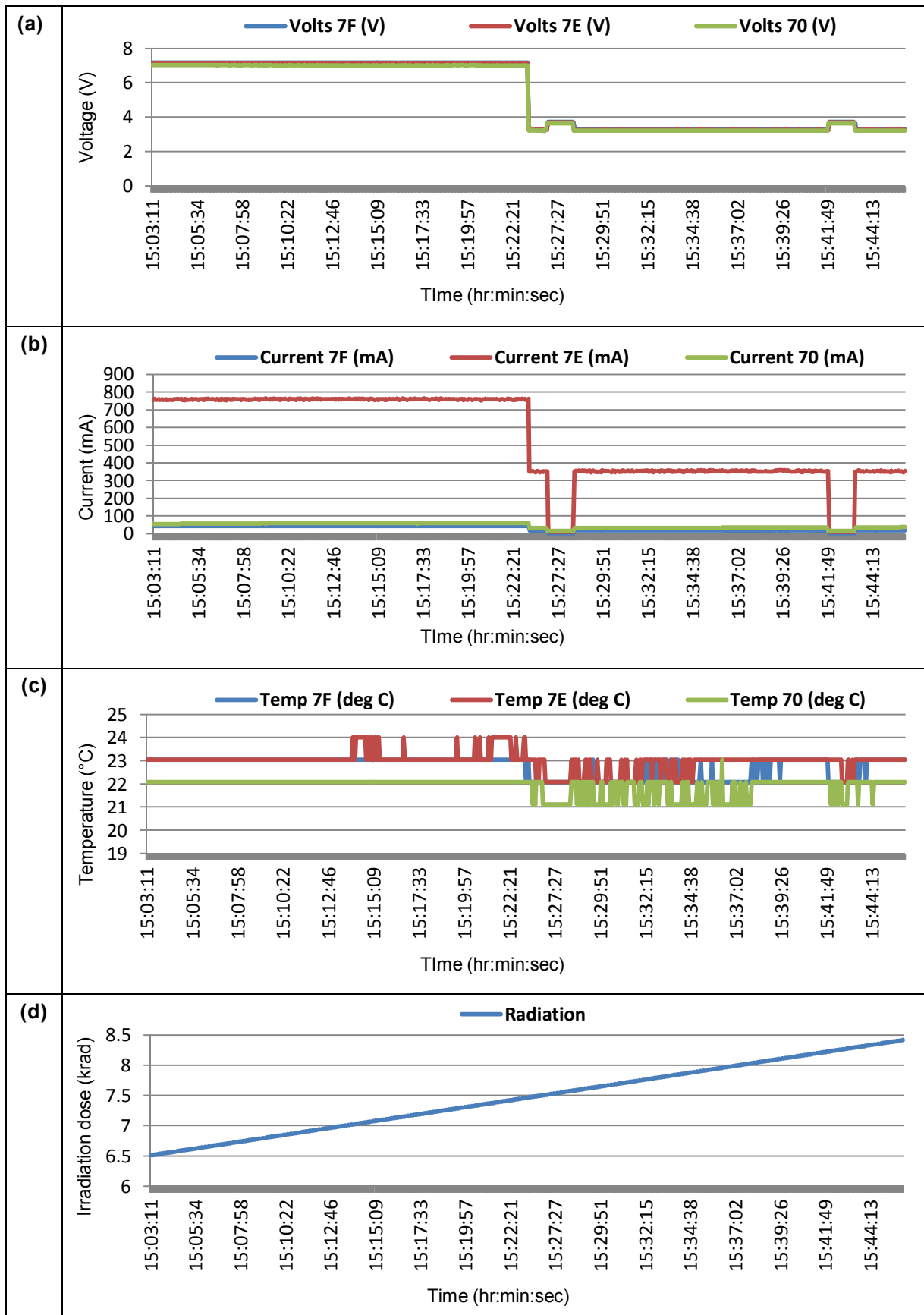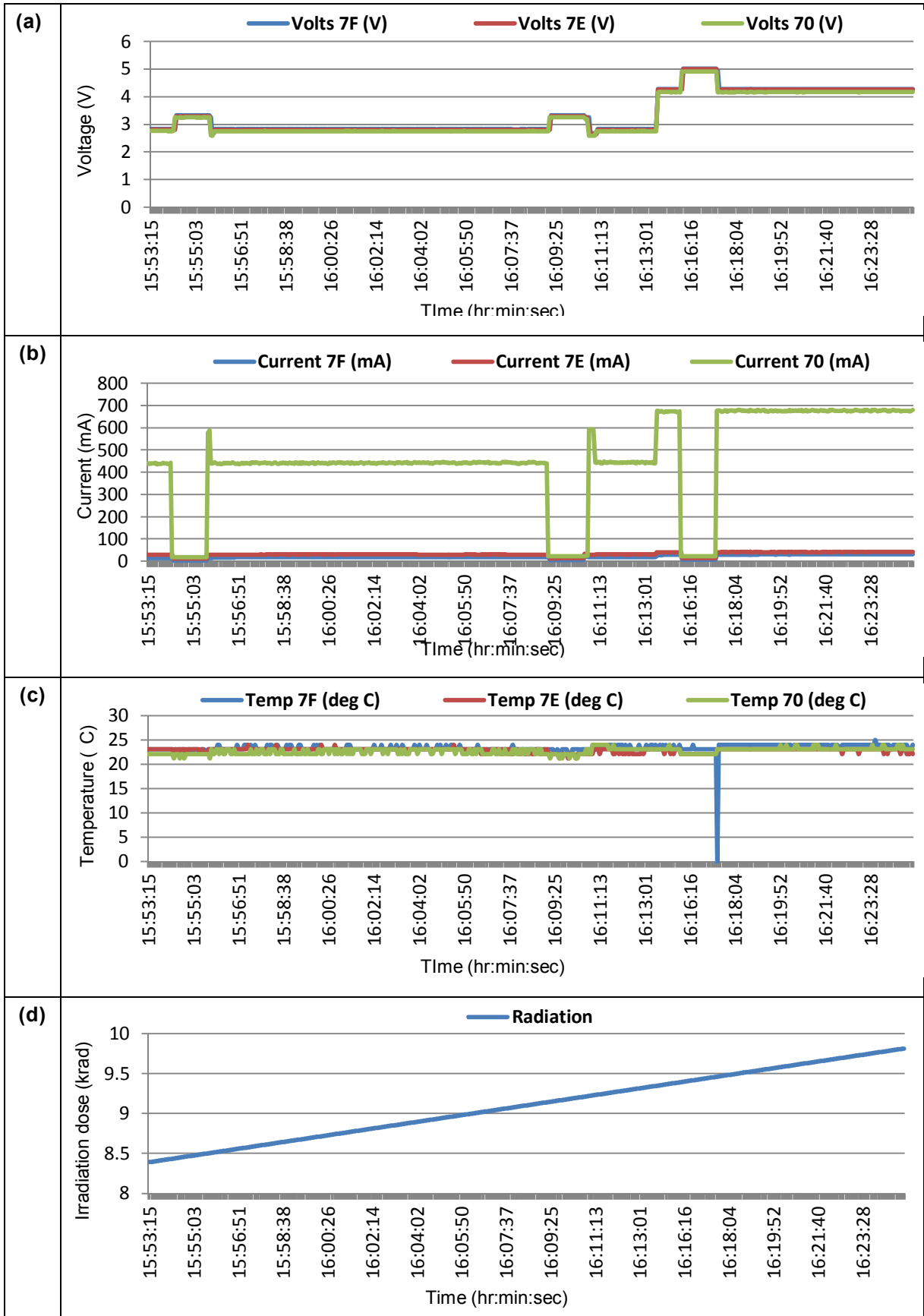
Figure F- 3: 2.82 – 3.76 krad irradiation dose test results with power channel 0x7F connected to the variable load and all channels' telemetry of (a) voltage, (b) current, (c) temperature and (d) the radiation dose over a 20 minutes timeframe

Figure F- 4: 3.76 – 6.51 krad irradiation dose test results with power channel 0x7E connected to the variable load and all channels' telemetry of (a) voltage, (b) current, (c) temperature and (d) the radiation dose over a 20 minutes timeframe

Figure F- 5: 6.51 – 8.39 krad irradiation dose test results with power channel 0x7E connected to the variable load and all channels' telemetry of (a) voltage, (b) current, (c) temperature and (d) the radiation dose over a 20 minutes timeframe

120

Figure F- 6: 8.39 – 9.8 krad irradiation dose test results with power channel 0x70 connected to the variable load and all channels' telemetry of (a) voltage, (b) current, (c) temperature and (d) the radiation dose over a 20 minutes timeframe
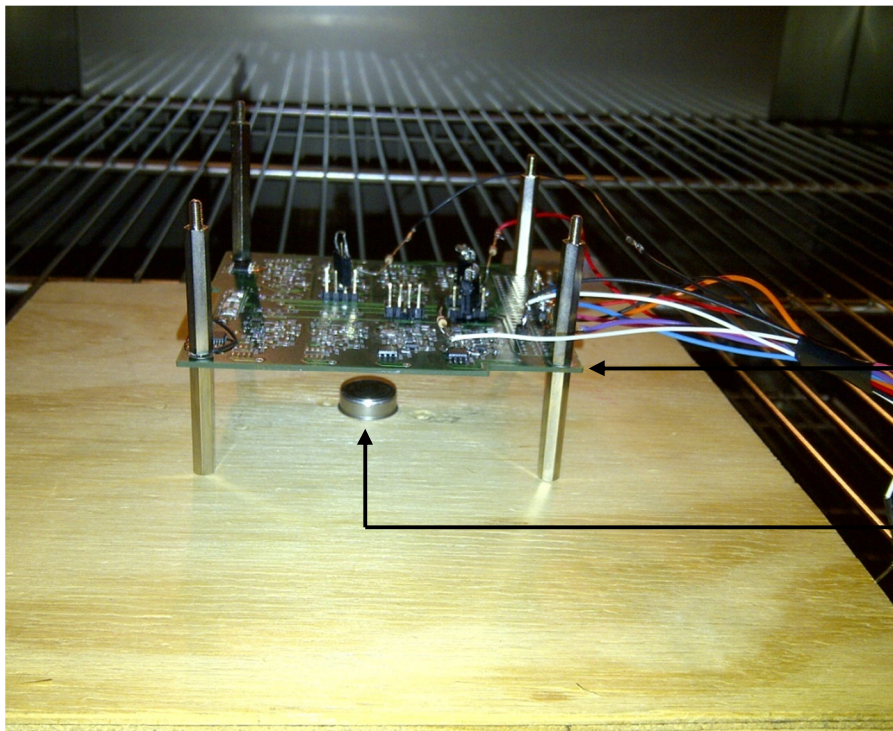
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APPENDIX G: TENNEY THERMAL CYCLING TEST CHAMBER

Settings and display board

PDM inside temperature chamber

Tenney temperature cycling test chamber

PDM inside temperature chamber

Temperature button to log chamber temperature data

APPENDIX H: RADIATION TEST EQUIPMENT

AECL Medical
Theratron 780-C

Time setting

Start button

PDM

Source of
Gamma Rays

Cobalt-60 ($^{60}C_0$)
Teletherapy
machine