## AUTOMATIC FREQUENCY CONTROL OF AN INDUCTION FURNACE

Presented by

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### SYNOPSIS

The development of an automatic frequency control system for a miniature high frequency induction furnace is described.

A background study into the fields of induction-heating, resonance, power electronic resonant converters and phase locked-loops are performed with relevance to this research. An analysis of the resonant load circuit is performed by means of a combination of measurement and numerical simulations. The study of the load behavior and power source is used as a cool to aid effective implementation of the automatic frequency control system. This simulation data is used to determine the operating frequency range of the RLL system.

A background study is performed in which several frequency-control schemes for power electronic converters are investigated. A brief summary, in which the basic requirements for a frequency control system with regards to this research are presented.

Two revisions of the Automatic Frequency Control system (RLL) were implemented, on the induction furnace. Experimental results on both systems (Rev1 and Rev2), illustrating the necessity for frequency control are also presented.

Future suggestions for optimizing the loop performance are presented. Further steps in the developmental process of the miniature high frequency induction furnace are also discussed.

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IR2	113 HIGH AND LOW SIDE MOSFET DRIVER	
AD	734 HIGH-SPEED ANALOG MULTIPLIER	
VC.	A 610 AUTOMATIC GAIN CONTROL IC	
CD-	4046 CMOS PLL IC	
DG	301 ANALOG SWITCH	

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### **CHAPTER 1**

#### **INTRODUCTION**

Induction heating is an important enabling technology in the platinum and gold jewellery manufacturing industry. This industry is the key to adding value to the mineral extraction industry of South Africa. Platinum jewellery has fast become a growing trend in South Africa, the United States and most of Europe<sup>1</sup>. The nature of this metal with its high melting point and difficulty in working however does not easily lend itself to usage by the average jeweller using oxy-gas torches and silica investment casts. The first reason for using this is that the high melting point of platinum alloys dissolves the usual refractory materials, causing contamination of the melt, and results in poor finished products. The second reason is the special mixture of oxy-gas and hydrogen required for melting platinum is often expensive and requires skilled labour to operate<sup>2</sup>.

This research is aimed at the jewellery manufacturing industry. Local jewellers seek a suitable alternative to the conventional blowtorch<sup>2</sup>. Induction-heating provides a faster and cleaner melt than the conventional blowtorch, producing a high purity homogenous alloy brought about by the inherent stirring action of the induced eddy currents. Commercially available large-scale induction furnaces do exist for the jewellery manufacturing industry most of which are imported from Germany, Italy and the USA. Price ranges of such systems vary between R75 000 and R245 000 per unit. The technology to work platinum has been limited to the few who have imported expensive units allowing them to monopolise the industry with the aid of these technological benefits.

The first aim of this research is therefore to provide the South African jewellery industry with a low cost induction furnace capable of melting and alloying small quantities of precious metal such as gold, silver and platinum.

The second aim of this research is to provide a laboratory standard induction furnace capable of electrically heating any metal for experimental purposes. This application would encourage research into the advancement of materials and metallurgical research at tertiary institutions<sup>3</sup>.

The advent of solid state power sources for induction heating has enabled conversion efficiencies of up to 93 % due to low switching losses and good high frequency coupling<sup>4</sup>. Solid state power sources used to drive induction-heating loads are usually very efficient, provided that the load is driven at its natural resonant frequency<sup>5</sup>. This allows zero voltage (ZVS) and or zero current (ZCS) switching of the converter, resulting in reduced power losses in the semiconductor switches<sup>5,6</sup>. Another advantage of driving a load at resonance is to enable an input power factor close to unity allowing minimal KVA consumption<sup>6</sup>. These parameters enable high conversion efficiencies due to reduced switching losses in the power source<sup>7,8,9</sup>.

The components of an induction furnace can be broken down into three main categories namely:

- 1) Load circuit,
- 2) Power source and
- 3) Frequency control circuit

The basic load circuit and power source has already been developed in part during a previous research project<sup>10</sup>. The current research project however, focuses on the development of a novel frequency control system for the induction furnace.

The induction-heating load forms part of a resonant tank circuit with a Q, which varies from 3 to 18. The power source is used to drive this tank circuit at its resonant frequency. The metal which is to be heated (work-p'cce), is situated inside a refractory crucible, which is placed inside the heating coil. When the coil is loaded a resulting shift in the resonant frequency of the tank circuit occurs. This shift in resonant frequency is directly related to the loading effect, which depends on the resistivity of the work-piece and the efficiency of coupling between the work-piece and the coil<sup>11</sup>. This shift is compensated for by manually adjusting the driving frequency of the power source to the new load resonant frequency. During a heating cycle, an increase in work-piece temperature causes an increase work-piece resistivity, which in turn also causes a shift in the resonant frequency of the tank circuit. When melting metals by induction, it is predicted that a further shift in

resonant frequency also occurs at the instant of melting. This phenomenon is attributed to the fact that the resistivity of a liquid metal differs from that of a solid metal. When dealing with magnetic metals, frequency shifts also occurs during a heating cycle<sup>12,5</sup>. When heating a ferromagnetic material (eg. steel), the relative permeability of that metal decreases with an increase in temperature, which causes a large shift in resonant frequency when the metal is heated through its Curie point. All of the factors mentioned above should be considered when heating and melting various metals by induction.

A problem therefore exists when different metals are placed in the heating coil, because it would require the operator of the induction furnace to manually tune the system for maximum power and efficiency throughout the process. This situation is undesirable because human intervention is not always as accurate and reliable as automatic control. An example of this situation occurs when heating a high melting point metal such as platinum. This process requires continuous maximum power transfer at all times. Incorrect manual tuning of the driving frequency could result in the freezing of the precious metal at the instant of pouring, due to insufficient heating above the metals melting point. The system also becomes less complicated to use, once automatic frequency control is implemented. The system proposed for this research is one that would automatically search for and operate at the natural load resonant frequency, and continuously track this resonant frequency during the heating cycle. This system will be referred to as the Automatic Frequency Control system (AFC) or the Resonant Locked Loop control circuit (RLL).

This thesis describes the actual implementation of a no el Automatic Frequency Control circuit to the existing prototype induction furnace. A brief study of previous frequency control systems are presented and used as design guidelines. The control circuit implementation is tested on the prototype induction furnace and results are presented to verify its stability under power conditions.

### **CHAPTER 2**

#### **PREVIOUS WORK**

#### 2.1 PREVIOUS INDUCTION HEATING RESEARCH

This project was first undertaken at the University of Cape Town in 1995 by Dave Dean, an engineer from the Materials Engineering Department. The project was unsuccessful due to an inadequate inverter circuit. The design was reported to cause continuous MOSFET destruction.<sup>11</sup> This was due to incorrect gating of the inverter switches which caused cross-conduction (MOSFET's switched on in the same inverter leg) resulting in large short-circuit currents in the inverter. The DC bus voltage for the inverter was then stepped down to about 40 volts resulting in far higher required MOSFET current ratings.

A second attempt was undertaken as a BTech project in 1996 by Leon Bardenhorst.<sup>12</sup> The gold work-piece could not be heated to more than 300°C due to device failure in the inverter circuit. It was found that this was due to incorrect gating of the MOSFET's and poor inverter layout. Another major problem encountered was matching transformer saturation due to incorrect design.

A third attempt was undertaken by Marcello Bartolini as a BTech project in 1997<sup>11</sup>. It was reported that a melting time of 30seconds was achieved for a gold work-piece. An input power of 4kW was used, and instability of the system during the heating cycle was reported. This problem was mainly due to poor esonant circuit design and inadequate load matching.

The previous three attempts all followed the same approach, which utilized a Voltage-Fed inverter driving a series resonant load. An extensive literature study was performed into the contemporary topologies used for modern induction heating, before a decision was made for this project. The Loughborough University Institute of Technology have performed extensive research into high frequency induction heating power sources employing power MOSFET's<sup>10,13</sup>. It was clearly pointed out in this publication that the Current-Fed topology driving a parallel resonant load circuit had proven to be far superior in performance and operation, than the three previous attempts, utilizing the Voltage-Fed inverter. It was at this point that a decision was made to employ a Current-Fed full-bridge load-resonant topology.

The fourth attempt was undertaken by the present author as a BTech project in 1998. A working prototype system using a Current-Fed inverter was developed and conclusive experimental results were presented<sup>4</sup>. It was found that the system operated efficiently off a single-phase supply, drawing less than 900W of input power to melt 30g of 24-karat gold in less than 26 seconds.

The development of the basic 1kW, 100 kHz switch-mode inverter (Current-Fed) employing power MOSFET's was described in the research dissertation. Some good design guidelines for the construction of the switch-mode inverter, which are crucial at elevated operating frequencies, were also presented<sup>4</sup>. The induction-heating load formed part of a parallel resonant circuit and the development of this load circuit was described. The achievement of these results, was mainly attributed to the sound construction of the power source and careful design of the induction-heating resonant load circuit.

The results and conclusions to the research described above have motivated research into further development of the miniature high frequency induction furnace. The initial system operated in open loop frequency control, which required the user to manually tune the operating frequency of the inverter to the natural resonant frequency of the load by monitoring the wave shape of the driving voltage across the load. The inverter switching frequency was manually tune. To achieve zero voltage transition (ZVT) switching in the power source. Failure to do so would result in a mismatch between the driving frequency and the natural resonance of the load. This would produce a fall off in inverter efficiency, and maximum power would not be transferred to the load. A temporary solution was provided by adjustment of the load circuit bandwidth to compensate for changes in load operating frequency. This proved to be disadvantageous because the system efficiency was not constant over the entire operating range. It was therefore apparent that closed loop frequency control was needed in order for the system to operate at maximum possible efficiency at all times.

The problem of frequency control is often encountered when driving loads of dynamic resonant nature, such as resonant induction heating loads.

Investigations into the operation of several frequency control schemes were therefore conducted as a basis for the current research. These various frequency control techniques were studied in detail and discussions are presented to analyse each system's overall performance. A conclusive summary is also presented, in which the fundamental requirements of a frequency control system are discussed as a basis for the current research.

#### 2.2 BACKGROUND STUDY

The work to be discussed concentrates on the frequency control of resonant loads for various induction-heating applications as well as a high power ultrasound application.

#### 2.2.1. Current Source Inverter using SIT's for Induction Heating Applications



Fig. 2.1. Simplified block diagram showing the layout of the induction billet neater and its control circuit

A control scheme was implemented for a 130 kHz, 7.5 kW full-bridge inverter for the induction heating of iron billets by Akagi, *et al* <sup>14</sup>. The simplified block diagram of the system is shown in figure 2.1. A current-fed topology was used to drive the induction-heating load, which formed part of a parallel resonant circuit. The frequency control scheme employed essentially the switching of the SITs (static

induction transistors) at zero voltage in order to maximize converter efficiency. This control was realized by employing two digital phase-locked loops. Optimal firing phase angle control values for the SITs which were a function of the average load current and the RMS load voltage, were pre-calculated and stored in a 64 kbyte ROM table. The average load output current and RMS output voltage were used as offset addresses for the ROM table, which then gave the optimal phase angle to be used. Loop1 controlled the ON timing of the SIT switches in order to maintain a fixed phase relationship between the load current and load voltage over the entire operating frequency range. Loop2 provided zero voltage switching by locking the off timing of the SIT switches to the load voltage.

#### 2.2.2 Discussion

The system was reported to have performed well with an estimated inverter efficiency of 95%. The response time of the system presented was limited by the following factors:

- Conversions of the output voltage and current from an analogue quantity to a digital value.
- Accessing data from the ROM table to produce the optimal phase angle value.
- Digital to analog conversion of the optimal phase angle value to be synthesised by the PLL circuit.

All conversions (D - A and A - D) had a resolution of only eight bits which limited the accuracy of the optimal phase angle control scheme. The EMI and induced noise generated by the switching of the power source could have an adverse effect on the operation of the frequency control scheme employed. The start-up sequence of this system was achieved by first manually tuning the inverter switching frequency (by adjusting the VCO) to the resonant frequency of the load. Once resonance was achieved, the user would then switch to automatic operation. Thus no automatic startup was achieved.



#### 2.3.1 High Power Ultrasound for Industrial applications

The research involved the driving of an ultrasonic transducer (Tonpiltz) at a power of approximately 1.5 kW by Veldhuizen<sup>15</sup>. A simplified block diagram is shown in figure 2.2. This project was aimed at ultrasonic cleaning applications. A half-bridge voltage fed inverter was employed to supply the necessary RF power to the transducer (load).

The transducer formed a complex high Q resonant circuit (predominantly series resonant) which required frequency control of the power source in order to lock to a specific resonant mode in the transducer, hence delivering maximum power to the load. This was achieved by locking the driving voltage and current to the load in phase over the specified operating frequency range of approximately 20 – 40 kHz. The frequency control system employed the monolithic 4046 PLL IC. Operating mode 2 of the PLL, which utilized the R-S latch phase detector, was employed.

#### 2.3.2 Discussion

The system was reported to be unstable due to poor loop filter design. The system was very susceptible to noise and EMI which cased the frequency control loop to lose lock at high power levels. Special noise shielding techniques were employed to ensure operation. The driving current signal to the load was embedded in noise due the measuring technique employed, and special filter circuitry was designed for signal conditioning purposes (filter A and filter B). The susceptibility of the loop to noise and EMI is characteristic of edge-triggered devices such as the R-S latch. The current filtering circuitry employed matched 2<sup>nd</sup> order passive filters on both the output

voltage ( $V_{LOAD}$ ) and output current ( $I_{LOAD}$ ) in order to minimize phase errors over the operating frequency range of the frequency control system. The signal conditioning circuitry proved to be a critical factor in the design of this frequency control circuit. It was therefore concluded that a frequency control circuit should have a low susceptibility to noise and EMI produced by the power source, if reliable operation was to be guaranteed.



#### 2.4.1 Half - Bridge Inverter for Induction Heating Applications

This research involved the development of a 6 kW, 50 – 150 kHz half – bridge IGBT inverter for the heating of carbon steel billets above Curie temperature (780°C) for industrial heating applications by Kamli<sup>7</sup>. A simplified block diagram is shown in figure 2.3. The frequency control circuit is shown in figure 2.4. The load circuit formed a combined series parallel configuration, which was driven by the inverter. A frequency control circuit was employed to track changes in the resonant load circuit. This was realized by employing the monolithic 4046 PLL IC in operation mode II. The control of the inverter was achieved by locking the control signals to the IGBT switches, in phase with the zero crossing points of the load voltage. A simple PLL control circuit was implemented to realize this control. A passive second order loop filter was employed to provide the error voltage proportional to the phase difference between the two input signals. The system was started up by manually adjusting the VCO to resonance before switching over to automatic lock operation.

#### 2.4.2 Discussion

The system operated well over the entire operating range and experimental results showing the tracking operation of the control circuit were presented. The passive second order loop filter employed does not provide for effective tracking and capture operation resulting in a finite static phase error due to its low loop gain<sup>16</sup>.



#### 2.5.1 PWM Inverter Control Circuitry for induction Heating

Fig. 2.5: SImplified block diagram showing the power source and frequency control circuit

The research involved the development of a frequency control circuit for a 4kW, 70kHz, full-bridge Voltage Source Inverter for induction heating applications by Ho<sup>8</sup>. The basic system is shown in figure 2.5. This system was used to heat carbon steel billets past their Curie temperature. A phase shifted PWM controller (UC 3825) was also employed to generate the switching signals for inverter with the necessary dead timings between transitions to prevent cross conduction of the power source. The 4046 PLL operating in mode II was employed to achieve zero voltage switching of the power source and ensure maximum power transfer to the load at all times. Frequency control of the power source was achieved by locking the measured output voltage and current to the load in phase, over the operating frequency range. The phase error produced by the type II phase detector was filtered by a first order passive low pass filter and provided the DC reference voltage for clocking the phase shifted PWM controller. The system was started up manually by varying the driving frequency of the clocking circuit until lock in operation occurred.

#### 2.6 SUMMARY

It can be concluded from the previous work discussed that the following problems exist with frequency control circuits in resonant mode power sources:

#### Signal Conditioning

All the types of frequency control methods studied thus far require some sort of current and or voltage measurement technique in order to detect resonance. This occurs when the load voltage and load current are in phase. A problem exists within high frequency converters when measuring output currents. This is due high frequency oscillations often being superimposed on the actual measured signal<sup>17</sup>. Special signal filtering techniques are often required to "clean up" the signal, making it compatible with standard analog and digital circuitry to be implemented for the control stage. Passive filtering circuits have a finite frequency and phase response over their operating range and often require a relatively narrow bandwidth to achieve optimal filtering at the fundamental frequency. These practicalities often limit the operating range of the system and produce phase shifts around its stable operating point.

#### <u>Stability</u>

High frequency power sources are generators of electromagnetic interference (EMI). The intense magnetic field produced in the induction-heating coil is also a generator of high frequency power radiation. These factors make operation of low-power analogue control-circuitry difficult due to noise EMI produced by the high power circuits. Special noise shielding techniques are usually required to make these low power circuits immune to EMI. Digital circuits are relatively immune to EMI and pose a feasible solution provided that the operating speed does not limit the performance of the system.

#### Speed

The natural resonant frequency of the load circuit is altered when the inductance of the heating-coil changes. This change occurs by virtue of the loading effect produced by the work-piece due to factors such as different conductivities, different coupling distances from the surface of the work-piece to the inner coil surface, and the changing relative permeability of the work-piece<sup>6</sup>. These changes occur whenever a different work-piece is inserted into the coil and so the resonance point can never be exactly the same. Another factor which alters the inductance of the coil, is when a ferromagnetic work-piece (such as steel) is heated through its Curie point. The Curie transition (approximately 780°C for steel) causes the material to lose its magnetic properties resulting in the relative permeability being reduced to unity from several hundred at room temperature. This transition results in a rapid increase in the penetration depth of the induced eddy currents. The work-piece is no longer a good conductor of magnetic flux (due to Curie  $u_r = 1$ ) and the amount of flux cutting the work-piece changes, resulting in a dramatic decrease in the inductance of the coil. This results in an increase in the natural resonant frequency of the tank circuit<sup>6</sup>. Frequency changes in the load circuit can also occur when heating non-ferrous metals past their melting points. A change in phase (from solid to liquid) in the metal results in a change in the metal's conductivity which influences the inductance of the coil by virtue of the magnetic field produced in it. The rate of change of frequency in the load is determined by the rate at which power is being delivered to the work-piece. Ideally for efficient melting systems the idea is to deposit energy into the work-piece at a rate faster than what can be dissipated by the work-piece by virtue of its thermal conductivity<sup>18</sup>. The control system to be implemented should therefore be able track fast changes in the load resonant frequency, maintaining lock at all times.

#### Protection

When operating the high frequency power source, a loss of lock in the frequency control system could produce catastrophic results. If the system loses lock and drives the inverter to a frequency away from the natural resonance of the load, the power losses in the semiconductor increase rapidly and semiconductor failure could result due to excessive power dissipation. These power losses are brought about by the loss of zero voltage transition switching and the conduction of the integral body-diodes in the switching elements, at operation away from resonance. A subsystem is therefore necessary to detect a loss of lock in the frequency control circuit. It should then attempt to force the system back into lock operation as quickly as possible or provide a trip signal to the DC bus or isolate the load from the inverter by shutting down the gate-drive signals to the inverter-bridge in the event of a malfunction occurring.

#### Initialization Procedure

All the induction heating frequency control systems studied thus far are started up manually by tuning the VCO to the resonant frequency before switching to automatic frequency control. This drawback is due to the limited capture range of the PLL control system employed, which makes automatic frequency control from start up problematic. The frequency control circuits studied thus far also all employ passive low-pass filtering techniques. Passive loop filters are undesirable in some systems because of the static phase error produced by low loop gain. Low loop gain also results in poor tracking operation<sup>16</sup>. Passive filters also have a limited capture range due to their large bandwidth. Two crucial parameters of first order loops viz.: loop-gain and loop bandwidth, cannot be independently adjusted and therefore do not allow for effective operation at all times<sup>16</sup>. Active loop filters (e.g. 2<sup>nd</sup> order PI controller) however provide much better tracking capability, capture range and minimal static phase error compared to the passive type. These factors are essential for automatic start up operation as well as good overall performance and will be investigated for this research.

### CHAPTER 3

## AN INTRODUCTION TO INDUCTION-HEATING AND PHASE LOCKED-LOOPS

#### 3.1 BACKGROUND

Electromagnetic induction, the basis of all induction heating, was first discovered by the "father" of induction, Michael Faraday in 1832. With his induced emf theory he proved that currents could be induced in a closed secondary circuit as a result of varying the current in a neighboring primary circuit. The essential feature was a change in the magnetic flux linkage with the closed secondary circuit, produced by an alternating current in the primary. In 1927, almost a century later, the first medium frequency induction furnace was developed by the Electric Furnace Company (EFCO) and since then, the number and size of heating installations have grown steadily<sup>19</sup>.

#### 3.2 BASICS OF INDUCTION HEATING

Induction heating utilizes three main effects: electromagnetic induction, skin effect and heat transfer. The heating is caused by the Joule heating effect when an electrically conductive object called the work-piece, is placed in an alternating magnetic field<sup>18</sup>. This alternating magnetic field is set up in the water-cooled induction coil. The induction heating coil and work-piece can be visualized as a transformer with primary turns (work-coil) and a short-circuited secondary turn (work-piece)<sup>19</sup>. When alternating current flows in the primary, voltages are induced in the secondary which cause currents to flow in it and these currents tend to cancel the flux that produces them, according to Lenz's law<sup>18</sup>. The frequency of these induced Eddy currents in the work-piece is determined by the frequency of 'he power source. These eddy currents are induced into a peripheral layer of the work-piece known as the skin-depth ( $\delta$ ) or penetration depth which is characteristic of current flow at high frequency due to skin effect is given by:

$$\delta = \sqrt{\frac{\rho}{\mu \pi f}}$$
(3.1)

#### Where:

 $\delta$  = penetration depth

 $\rho$  = resistivity of work-piece

f = frequency of eddy currents

 $\mu$  = permeability of work-piece which in this case is the same as free space, since the work-piece is non-magnetic.

The skin depth is roughly where the current density has fallen to about one third its surface value. The current density falls off from the surface to the center of the work-piece and the rate of decrease is higher at higher frequencies<sup>19</sup>. It is also dependent on two properties of the material, i.e., resistivity and relative permeability<sup>18</sup>. Both the penetration depth in the work-piece and the work-coil depend on the three parameters shown in equation 3.1. The ideal situation is to maintain a good efficiency of coupling between the coil and work-piece to ensure maximum power transfer. Coupling efficiency is a measure of the amount of power transferred between the coil and work-piece. The efficiency of coupling in this case is dependent on the resistivity of the coil and that of the work-piece and is given by equation 3.2.

$$\eta \approx \frac{1}{1 + \sqrt{\frac{\rho_c}{\rho_u \mu_u}}}$$
(3.2)

Where:

 $\eta$  = coupling efficiency between the coil and work-piece;

 $\rho_c$  = electrical resistivity of the heating coil (which is usually soft copper tubing)

 $\rho_w$  = electrical resistivity of the work-piece

 $\mu_w$  = relative permeability of the work-piece

When deviating from the idealized concept of equation 3.2, the concept of coupling efficiency is related to the term known as the coupling factor in conventional transformer theory. In both cases the idea is to keep the primary and the secondary closely wound or closely coupled to reduce flux leakage between the primary and secondary windings, hence improving the power transfer<sup>19</sup>. In induction heating, the heating coil is considered to be the primary, and the work-piece is considered to be a short-circuited secondary winding of a transformer.

Practical factors affecting coupling efficiency include:

- Geometry of work-piece, which improves for a tightly packed, solid work-piece and decreases for a loosely packed work-piece due to leakage flux.
- Geometry of the heating coil, which improves for a closely wound coil around the work-piece. Other factors also concerned with geometry are the length of the coil and the number of coil turns.
- The material used for the heating coil. The higher the coil conductivity, the lower the I<sup>2</sup>R losses in the coil, hence the more power transferred to the work-piece.

Another important factor to be considered is the fact that materials such as gold, copper and silver have relatively low resistivities at room temperature, which once again results in a low coupling efficiency at startup. Examples of coupling efficiencies at room temperature are:

Metal	Resistivity(p20°C)	Efficiency (η)
Platinum	0.106 uΩm	71.56 %
Gold	0.023 uΩm	53.97 %
Copper	0.01673 uΩm	50 %
Silver	0.016 uΩm	49.44 %

 Table 3.1: The coupling efficiencies for several metals are shown. In accordance to equation 2 it is evident that low resistivity metals result in poor coupling efficiencies at room temperature.

Equation 3.2 is the idealised condition and should be treated with care, but it gives a broad-brush idea of what controls the coupling efficiency. If for example, one considers a material with high resistivity and permeability such as steel, an efficiency

approaching 100% can be achieved, but copper with a low resistivity, where the root term (equation 3.2) approaches unity, has an efficiency of about 50%. This formula applies for simple coils and is not valid for multi-layer coils where the coil current is not limited to the skin depth<sup>19</sup>. The efficiency increases during the heating cycle due to fact that the resistivity of the work-piece increases with temperature as shown in equation 3.3. The resistivity of the coil is kept constant by passing cooling water through it thereby also keeping the losses in the coil to a minimum.

The heating of ferro-magnetic materials poses a special problem because of the Curie point. Above the Curie temperature the relative permeability of the material reduces to unity, which results in a large increase in sk.n depth.

$$\rho_{\theta} = \rho_{1} \left[ 1 + \alpha_{2\theta} \left( \theta - \theta_{1} \right) \right]$$
(3.3)

Where:

 $\rho_{\theta}$  = The resistivity at any temperature  $\theta$ ,

 $\alpha_{20}$  = the temperature coefficient of resistance at a temperature of 20°C,

 $\rho_1$  = the resistivity at temperature  $\theta_1$ .

#### 3.3 HYSTERESIS AND EDDY-CURRENT LOSS

In conventional induction heating of magnetic materials such as steel, the heating is caused by eddy-current losses that produce I<sup>2</sup>R heating and hysteresis losses. Hysteresis loss is defined as the friction between molecules when the material is magnetized first in one direction and then in the other. The molecules may be regarded as small magnets, which turn around with each reversal of direction of the magnetic field<sup>20</sup>. Therefore in ferro-magnetic materials hysteresis loss improves the induction heating efficiency. It is therefore concluded that for a material such as gold, the heat generated in the work-piece can only be due to eddy-current loss since these materials are non-magnetic.

#### 3.4 **POWER SOURCE**

Induction heating power supplies are frequency changers that convert utility line frequency (50Hz) power to the desired single-phase power at the frequency required by the induction heating process<sup>5</sup>. The rectifier portion of the power supply converts the single-phase line frequency input to DC, and the inverter portion changes the DC to single-phase high frequency (100kHz) AC. This is illustrated in figure 3.3:



Figure 3.3: Layout of the high frequency power source showing the converter, inverter and heating

Inverter circuits use solid switching devices such as thyristors (SCRs) and transistors. For high power and lower frequencies, large thyristors are commonly used. For low power or frequencies above 25kHz, transistors are used because of their ability to be turned on and off very fast with low switching losses<sup>9</sup>. Vacuum tube oscillators have been used extensively for many years at frequencies above 300kHz. However, tube oscillators have a low conversion efficiency of 55 to 60% compared to 85 to 93% for inverters using transistors. Power vacuum tubes have a limited life of typically 2000 to 4000 hours and are therefore a costly maintenance item<sup>9</sup>. The high voltage (over 10000 volts) required for tube operation is more dangerous than the 1000 volts or less present in typical transistorized inverters. These negative features of tube oscillators have brought about a dramatic move toward use of transistorized power supplies in heat treating applications that require a frequency of less than 1MHz<sup>9</sup>. Induction heating power supplies utilize various techniques to produce the high frequency alternating current. Various topologies are:

#### Initial Investigations

- Half-bridge voltage-fed inverter topology (Figure 3.4)
- Full-bridge voltage-fed inverter topology (Figure 3.5)
- Current-fed full-bridge inverter topology (Figure 3.6)
- Cycloconverter or AC AC converter (Figure 3.7)
- Current-fed chopper or quarter bridge (Figure 3.8)



Figure 3.4: Half-bridge voltage-fed inverter topology



Figure 3.6: Current-fed full-bridge inverter topology



Figure 3.8: Current-fed chopper or quarter bridge



Figure 3.5: Full-bridge voltage-fed inverter topology



Figure 3.7: Cycloconverter or AC = AC converter

#### 3.5 CHOICE OF FREQUENCY

Frequency is a very important parameter in induction heating because it is the primary control over the depth of current penetration and therefore the depth of heating<sup>5</sup>. Frequency is also important in the design of induction heating power supplies because the power components must be rated to operate at the specified frequency. Due to reduced switching losses at elevated switching frequencies (up to 1MHz), enhancement-mode power MOSFETs have become an important component in high frequency power sources for induction heating<sup>13</sup>. For effective induction heating, the frequency of the alternating magnetic field in the work-coil is of paramount importance and is given by:

$$f_c = \frac{6.45 \ \rho}{\mu \ d^{-2}} \tag{3.4}$$

Where:

 $f_c$  = critical frequency

 $\rho$  = the electrical resistivity of the work-piece ( $u\Omega m$ )

d = the diameter of the work-piece (m)

 $\mu$  = the permeability of the work-piece (Hm<sup>-1</sup>).

Equation 3.4 is defined as the critical frequency below which, a loss of heating would occur due to field cancellation in the work-piece. The critical frequency is calculated at a ratio of work-piece diameter to penetration depth  $(d/\delta) > 4.5$ . Where a free choice of frequency exists, it should be chosen greater than or equal to  $f_c$ .<sup>3</sup>

Equation 3.5 shows the power loss per unit area in the work-piece written in terms of current density  $(Js^2)$ . Equation 3.6 shows the power loss per unit area in terms of the applied field Hs<sup>2</sup> at the surface of the work-piece<sup>18</sup>. From equation 3.7 the relationship between the power density (P) and the penetration depth can be seen. Equation 3.8 shows the relationship between the penetration depth and the applied frequency, which is derived from equation 3.1. Equating equations 3.7 and 3.8 yields equation 3.9 which illustrates the relationship between the power density in the work-piece and the applied frequency. It is therefore concluded that for a given work-piece and a free choice of frequency, it is always advantageous to increase the frequency<sup>18</sup>.



The gold work-piece has the following parameters:

Diameter	0.01 m
Length	0.013 m
Resistivity ( $\rho_{20}^{\circ}C$ )	0.024 uΩm
Resistivity ( $\rho_{1064}^{\circ}C$ ) melting point	0.127 uΩm
Permeability (µ0)	$4\Pi x 10^{-7} \text{ Hm}^{-1}$

Table 3.2: Dimensions of the gold work-piece to be melted in the induction furnace



Figure 3.9: The variation in penetration depth in a gold work-piece over a frequency range of 100kHz.

In an induction heating application, the penetration depth ( $\delta$ ) of the induced current in the work-piece is inversely proportional to the applied frequency (equation 3.1 and figure 3.9). It is common practice in most induction heating applications to make the penetration depth ( $\delta$ ), much smaller than the diameter (d) of the work-piece<sup>18, 19, 20, 21</sup>. The gold work-piece diameter is determined by the inner diameter of the crucible, which in this application was chosen to be 10mm (table 3.2). The penetration depths in the gold work-piece at room temperature over a range of frequencies (50kHz-150kHz) are shown in figure 3.9.

#### 3.6 EDDY CURRENT STIRRING

A unique feature in induction heating is the automatic stirring of the molten metal. This movement is the result of the interaction of the magnet's fields of the currents in the coil and work-piece<sup>22</sup>. This effect is:

- Proportional to the square of the applied field (ampere-turns):
- Inversely proportional to the density of the molten metal;
- Inversely proportional to the applied frequency of the magnetic field;
- Important in the production of high-grade allovs<sup>18, 19, 21, 22</sup>.

#### 3.7 RESONANCE

Resonance is the study of the frequency response of a particular circuit. The resonant circuit is a combination of R, L and C elements having a frequency response characteristic similar to figure  $3.10^{23}$ .



Figure 3.10: Response curve of a resonant circuit

It is evident that at a certain frequency  $f_r$  the response of the circuit in figure 3.10 is a maximum. This behavior is classified as resonance. Resonance can be defined as the point at which maximum response occurs in a circuit. The response can be in terms of voltage (V) or current (I) depending on what type of resonance circuit is being analysed. The frequency  $f_r$  at which maximum response occurs is defined as the point at which the reactive components in the resonant circuit are equal and opposite (XL = XC)<sup>23, 24</sup>.  $f_r$  can be defined in terms of the circuit elements such as inductance and capacitance (L and C) and is given in equation 3.10. This project deals with characteristic response and basic analysis of a parallel resonant (tank) circuit.

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$
(3.10)

Where:

- $f_r$  = resonant frequency in Hz
- L = inductance in Henries
- C = capacitance in Farads.

#### 3.7.1 Parallel Resonance



Figure 3.11a: General representation

Figure 3.11b: Equivalent representation as seen by the source

The following analysis is based on the assumption that the quality factor (Q) > 10. Figure 3.11a shows the general representation of the parallel resonant circuit. The circuit is modeled with an ideal current source (I) and the source impedance is assumed to be infinite.  $Z_{TP}$  is defined as the input impedance to the tank circuit. Xc is defined as the capacitive reactance of the tank circuit and  $X_L$  is defined as the inductive reactance of the coil.  $R_L$  is defined as the resistance of the coil. In induction heating the work-coil and work-piece are modelled as a series R, L circuit as shown in figure 3.11a. The quality factor (Q) which exists in all resonance circuits, is defined as the ratio between the reactive power and real power present in the circuit. The Q is determined by the coil and is given by<sup>23</sup>:

$$Q_{L} = \frac{X_{IP}}{R_{I}}$$
 (3.11)

#### Where:

 $Q_L$  = Quality factor of the coil  $X_{LP}$  = inductive reactance of coil  $R_L$  = resistance of the coil

Figure 3.11b shows the equivalent representation of the tank circuit as seen by the source.  $X_{LP}$  is defined as the total inductive reactance of the coil at resonance. Xc is defined as the capacitive reactance of the tank circuit at resonance. At resonance the inductive and capacitive reactances cancel and the resistance of the coil is transformed from  $R_L$  to Rp by the ratio,  $Q_L^2 R_L$  as shown in figure 3.11b<sup>23</sup>. Rp is the impedance which the source sees at resonance. Assuming the tank circuit has a Q of 10 it can be seen that Rp is of the order of 100R<sub>L</sub>.

It is therefore evident that the Q acts as an impedance transformer and explains why parallel resonant circuits have maximum impedance at resonance, with an impedance response curve similar to that of figure 3.10. Since impedance transformation occurs in parallel resonance it follows that current transformation occurs in the reactive branches of the tank circuit. It can be seen from figure 3.11b that if  $I_T$  is the total current entering the tank circuit, the current in the reactive branches  $X_L$  and  $X_c$  are given by<sup>23</sup>:

$$I_L = Q_L I_T$$
 (3.12a)  $I_C = Q_L I_T$  (3.12b)

Where

 $I_L$  = current in the inductor  $I_C$  = current in the capacitor  $I_T$  = total current into the resonant circuit  $Q_L$  = quality factor of the resonant circuit

The bandwidth of the tank circuit is given  $by^{23}$ :

$$BW = \frac{f_r}{Q_p}$$
(3.13)

Where

BW = bandwidth of the tank circuit in Hz;

 $f_r$  = the resonant frequency, at which maximum impedance occurs in Hz;

 $Q_P$  = The quality factor of the tank circuit ( $Q_P = Q_L$ )

#### 3.7.2 Frequency characteristic of a parallel resonant circuit



**Figure 3.12:** Frequency characteristic of a parallel resonant circuit. At frequencies below resonance  $(\omega_0)$  the inductive reactance of the circuit shunts the circulating current, making the load inductive in nature. Likewise at frequencies above  $\omega_0$  the load becomes capacitively reactive.

Figure 3.12 shows the frequency characteristic of a parallel resonant circuit.  $\theta$  in figure 3.12 shows the phase relation between the voltage and current as a function of frequency. The voltage leads the current at frequencies below resonance ( $\omega_0$ ), where the inductor impedance is lower than the capacitor impedance, and hence the inductor current dominates<sup>25</sup>. At frequencies above resonance, the capacitor impedance is lower and the voltage lags the current, with the voltage phase angle approaching  $-90^{\circ}$ . It is therefore evident that a parallel resonant circuit has a lagging power factor at frequencies below resonance and a leading power factor at frequencies above resonance. At the resonant frequency  $(\omega_0)$ , both the voltage and current are in phase and the input power factor to the tank circuit is therefore unity. Most resonant converters in induction heating applications operate by driving the load circuit at its resonant frequency<sup>13, 7, 5, 9, 10</sup>. This has the advantage of providing reduced switching losses (due to zero voltage and or zero current switching) and thereby, a high operating efficiency in the power-source. The advent of solid state converters have therefore led to increasing interest in the development of RF power sources for induction heating. Unlike RF valves solid state switches cannot tolerate mismatched load circuits too well at high frequency making these supplies unstable and inefficient. Driving a mismatched load brings about the conduction of the integral

body diode within the MOSFET. This results in a conduction power loss as well as reverse recovery loss when the load current is commutated from one half-cycle to the next. Phase locked-loop circuits applied to solid state power sources ensures efficient switching by holding the load at resonance. This concept applied to induction heating has only recently been discovered. The earliest publication of PLL control for solid state power sources are dated back to 1985. Since then there have been only a few publications on this topic over the past one and a half decades making research into this field challenging and every contribution significant.

The implementation of the PLL control system was viewed from a power electronics perspective. A basic understanding of the operation of phase locked-loops from the telecommunications perspective are presented and the concepts then adapted for the power electronics discipline.

#### 3.8 PHASE LOCKED-LOOPS

A phase locked loop is a circuit, which synchronizes the signal from an oscillator with a second input signal, called the reference so that they operate at the same frequency with a fixed phase relationship between the two<sup>16</sup>. Phase-locked loops are often used because they provide filtering to the phase or frequency of a signal that is similar to what is provided to voltage or current waveforms by ordinary electronic filters<sup>16</sup>.

Phase locked-loops find wide application in the areas such as communications, wireless systems, digital circuit's etc. The first description of phase locked loops was published by de Bellescize in 1932 on work involving the synchronous reception of radio signals.

$$\theta_{i}(s) \xrightarrow{P.D}_{\langle s \rangle} \quad Loop Filter \quad VCO \quad \theta_{o}(s) \rightarrow \\
 \div N$$

Fig 3 13: Schematic block diagram of bisic PLL configuration

While the concept of phase locking has been in use for more than half a century, monolithic implementation of PLL's have become possible only in the last twenty years and popular in the last ten.

#### <u>3.8.1 Loop Fundamentals</u>

The basic loop consists of a phase detector (P.D), a loop filter and a voltagecontrolled oscillator (VCO). With the input signal to the loop having a phase of  $\theta_i(t)$ and an output of  $\theta_o(t)$ , the following assumptions are made:

- The loop is locked
- The phase detector has a linear characteristic

#### 3.8.2 Phase Detector

The ideal phase detector output voltage is proportional to the phase difference between its inputs, i.e.:

$$Vd = Kd \left(\phi_{i} - \phi_{o}\right) \tag{3.14}$$

where Kd is the phase detector gain factor with dimensions of volts per radian (V/rad).
Many different types of phase detectors exist, all performing essentially the function of multiplication in a typical PLL system. For the purposes of this project only the following three types will be discussed:

#### 3.8.2.1 4-Quadrant Multiplier

A multiplier acts as a phase detector (P.D) through the trigonometric identity:

$$\sin A \cos B = \frac{1}{2} \left[ \sin(A - B) + \sin(A + B) \right]$$
(3.15)

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The term "4-Quadrant" refers to the ability of the multiplier to handle both positive and negative values at both of its inputs<sup>26</sup>.

If the inputs to the multiplier are:

$$\mathbf{v}_i = V_i \sin(\omega_i t + \phi_i) \tag{3.16}$$

$$v_{o} = V_{o}\sin(\omega_{i}t + \phi_{o})$$
(3.17)

The P.D output is:

$$v_d = K_m v_i v_o \tag{3.18}$$

where  $K_m$  = multiplier constant resulting in:

$$\widetilde{v}_{d} = \frac{1}{2} K_{m} V_{i} V_{o} [\sin(\phi_{o} - \phi_{i}) + \sin(2\omega_{i}t - \phi_{o} + \phi_{i})]$$
(3.19)  
and  
 $\phi_{o} - \phi_{i} = \Delta \phi$   
yielding  
 $\widetilde{v}_{d} = \frac{1}{2} K_{m} V_{i} V_{o} [\sin \Delta \phi + \sin(2\omega_{i}t - \Delta \phi)]$ 
(3.20)

Equation 3.19 shows the two sinusoidal components of the phase detector output. For a constant  $\Delta \phi$  the output of the P.D should be constant according to equation 3.20. The second term however varies with a frequency  $2\omega i$  as shown in equation 3.20.

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Because the second term is removed by the loop-filter, the average dc equivalent of the output is given by:

$$\overline{v}_d = \frac{1}{2} k_m V_i V_o \Delta \phi \tag{3.21}$$

where  $k_m$  is a constant associated with the multiplier. For small values of  $\Delta \phi$ , sin  $\Delta \phi \approx \Delta \phi$  and the P.D gain is given by:

$$k_{d} = \frac{1}{2} k_{m} V_{e} V_{o}$$
(3.22)

It is therefore evident that the P.D gain  $(k_d)$  is a function of the input signal level. Therefore if the input signal amplitude varies,  $k_d$  and all loop parameters dependant on loop gain will also vary<sup>16</sup>. As  $\Delta \phi$  increases with time, the average component of V<sub>d</sub> varies sinusoidally, resulting in the P.D characteristic shown in fig (3.14).



Fig.3.14: Sinusoidal characteristic of analog phase detector (4-Quadrant multiplier).

#### 3.8.2.2 Switch type phase-detectors

Also a common type of P.D consisting of a switch. The switch could be anything from a transistor to a diode-quad or even an analog switch.



Drive Fig. 3.15. Basic Switch type P.D. configuration

Common types of switch-type phase detectors are:

- Gilbert Multiplier
- Double-Balanced Multiplier
- Half and full-wave transistor multiplier

These phase detectors also have a sinusoidal characteristic as shown in fig (3.14). The switch is driven synchronously with the input signal and on alternate half-cycles it allows the input either to pass or not to pass as shown in figure 3.16. Assuming the input signal to be *Es cos* ( $wt + \emptyset$ ) and the switch changes at the zero crossings of *sin wt*, the output will be *Es cos* ( $wt + \emptyset$ ) for  $0 < wt < \pi$  and zero for  $\pi < wt < 2\pi$ . The average d-c output of the P.D is:

$$E_{d} = \frac{E_{s}}{2\pi} \int_{0}^{\pi} \cos(\omega t + \phi) dwt \qquad (3.23)$$
$$= -\frac{E_{s}}{\pi} \sin \phi$$

Figure 3.16 illustrates the operation of a half-wave detector. A full-wave detector can also be used and the d-c output will be doubled, as well as the ripple frequency. This is an advantage in wide-band loops as it eliminates problems caused by low phase detector ripple getting to the VCO and causing phase jitter.



Fig.3.16. Switching waveforms illustrating phase detector operation

#### 3.8.2.3 Triangular phase detectors

Unlike sinusoidal characteristic phase detectors, linearity in triangular P.D's are near perfect for phase angles as large as 90°. Figure 3.17 and 3.18 show a comparison between sinusoidal and triangular P.D characteristics. A triangular characteristic is realized by driving the inputs to the multiplier with square waves. This operation gives the P.D an exclusive-OR characteristic<sup>27</sup>.



Fig.3.17: Sinusoidal characteristic of analog phase detector showing its limited linear operating region

Fig318 Triangular physicilization characteristic showing the extended linear operating range

Digital phase detectors are realized when using an XOR gate or an edge-triggered R-S flip-flop. These form part of the triangular family of P.D's but have a slightly different output characteristic as shown in fig (3.19) below:



#### 3.8.2.4 XOR Phase Detector

Operation from a single supply and a close examination of the XOR truth table yields the digital P.D characteristic. It should be observed that preferred operation of this device would be when the two input signals are phase shifted by 90°. This puts the P.D in the center of its linear region and ensures accurate lock operation over the range  $0 < \phi < \pi$ .

The XOR gate being a digital device is relatively immune to switching and input signal noise. The trade-off however, is that the input signal range is limited to a 50 % duty cycle in order to ensure correct operation of this device.

#### 3.8.2.5 <u>R-S LATCH</u>

The extended operating range of  $(0 < \phi < 2\pi)$  for the R-S latch makes it an attractive option for a P.D. This device is not duty-cycle limited like the XOR but has its disadvantages. Being an edge-triggered device makes it susceptible to noise effects and therefore the two input signals must be of a quality that will trigger the flip-flop reliably<sup>16</sup>. Also the input signal-to-noise ratio must be high and is of no value if a signal must be recovered from a larger noise.

Other types of Triangular P.D's are:

- 2 and 3 state P.D
- charge-pump P.D
- sample and hold P.D

#### 3.8.3 Loop filter

The output of the phase detector is filtered by the loop filter, which provides a phase error voltage to drive the VCO keeping the loop in lock. Since the P.D and the VCO designs are usually inflexible, the design of the loop filter provides more flexibility in controlling the PLL characteristics<sup>26, 27, 28</sup>. The desired PLL response will determine

the loop-order. The loop-order required therefore dictates the loop filter type. Loop filters are generally of 2-types namely, passive and active.

#### 3.8.3.1 Passive loop filter

Passive loop filters are of the low pass type or of the phase-lead-lag type. For simple phase-locked applications requiring low loop gain, marginal phase-accuracy and transient loop stability, passive loop filters provide a quick and easy solution.

#### 3.8.3.2 Active loop filter

For a passive loop filter the maximum dc ga.n achievable is 1. An active loop filter provides dc loop gains that are essentially infinite and provide better tracking performance. Many types of active loop filter configurations (such as the integrator, integrator and lead, lead-lag filter) are available in references<sup>16, 26, 28</sup>. The final loop filter configuration used for this research will be discussed briefly.

#### 3.8.3.2.1 Integrator and lead filter



The integrator plus lead filter forms a basic PI controller as nown in figure 3.21. The prime purpose of introducing an integral term into the controller is to remove any steady state phase error. At high frequency the ac gain (proportional term Kp) is formed by R2/R1. The ac amplifier is actually used as an attenuator to the high frequency ripple, providing a jitter free signal to the VCO. The dc gain of the filter is usually infinite as mentioned before. In many applications however, involving high order loops it is always desirable to control the dc loop gain to prevent instability. Rp/R1 controls the dc gain component of the loop filter and therefore also indirectly controls the entire loop gain.

Design of a PLL requires the ability to be able to control the natural loop frequency  $(w_n)$ , damping factor ( $\zeta$ ) and dc loop gain (K). Passive loop filters such as the singlepole low-pass and the two-pole low pass filter, do not allow for the control of  $w_n$ ,  $\zeta$ and K independently. The control of K ensures good tracking as mentioned before but a high gain loop (large K) also comes with a wide bandwidth. Therefore narrow bandwidth and good tracking are usually incompatible in first order loops. If it is necessary to have large gain and small bandwidth, the loop will be badly underdamped (low  $\zeta$ ) and transient response will be poor (low  $w_n$ ). The active integratorplus lead filter having two independent time constants ( $\tau 1$  and  $\tau 2$ ), draws on the concept of tachometer feedback which allows for the independent control of natural frequency (transient response), damping factor (overshoot) as well as the dc gain (good tracking).

#### 3.8.4 Voltage Controlled Oscillator (VCO)

The voltage-controlled oscillator provides an output frequency, which is controlled by the filtered error voltage it receives from the loop filter. Since frequency is the derivative of phase, the VCO operation may be described as:

$$\frac{d\phi_o}{dt} = K_o V_m \tag{3.24}$$

where 
$$K_o = VCO$$
 gain  
 $V_m = VCO$  input voltage  
 $d\phi_o = VCO$  output phase

It is therefore apparent that the phase of the VCO output will be proportional to the integral of the input voltage  $V_{in}$ . The VCO should be operated within its linear range to ensure a constant loop-gain parameter (Kvco). For the purposes of this research, a linear relationship between input control voltage and output frequency is assumed and is given by equation 3.25

$$k_{o} = \frac{\Delta f_{o}}{\Delta V_{o}} \tag{3.25}$$

The VCO's employed in the PLL system for this research were derived from two 4046 PLL integrated circuits.

# **CHAPTER 4**

# IMPLEMENTATION OF AUTOMATIC FREQUENCY CONTROL 4.1 SYSTEM DESCRIPTION AND OPERATION



Figure 4.1: Schematic layout of the induction furnace and all its components

The induction furnace comprises the following components, with reference to figure 4.1:

- A variable DC power source that is derived from rectified mains voltage. This
  feeds a rectifier bridge from a variac. The isolation transformer between the variac
  and the mains voltage (50Hz), serves to provide isolation for test purposes. By
  varying the DC bus voltage, the input power to the inverter is controlled thereby
  controlling the input power to the load;
- A filtering inductor or iron core reactor, which is situated in the positive DC bus rail. The iron core reactor serves to feed a constant current to the inverting stage. The iron core reactor also provides inherent short circuit protection because it restricts the rate of rise of current in the event of a short circuit occurring in the induction-heating coil. Because of the slow rate of rise of current under fault conditions in the iron core reactor, this topology is advantageous since it now gives the necessary protection circuitry some time to sense and operate under fault conditions. The result is that protection circuitry can be easily implemented to the system<sup>10</sup>,

- A 100kHz full-bridge load-resonant MOSFET inverter which operates at approximately 1kW. The inverter switches are operated in alternate pairs to generate the high frequency alternating current needed to produce strong eddy currents in the heating coil. The inverter operates at the resonant frequency of the load circuit thereby allowing zero voltage switching, hence no external high speed diodes are needed across the MOSFET switches to carry reactive freewheeling current. <sup>16</sup> The result being that the total switching losses in the inverter is greatly reduced, thereby increasing the inverter efficiency;
- The gating and gate drive circuitry which are used to convey the switching signals to the inverter switches;
- The load which consists of a water cooled induction heating work-coil in which the crucible and work-piece are situated;
- A water-cooled high frequency matching transformer which is used to step up the current in the work-coil to a high value, which is necessary for good induction heating and also serves to provide electrical isolation;
- A capacitor bank which is used to resonate with the reflected inductance of the load and matching transformer at a frequency of approximately 100kHz.
- To enable maximum power transfer to the load at all times the automatic frequency control system is included which forms the basis for the current research. This is given by the AFC block in figure 4.1.

#### 4.2 LOADING EFFECT

The placing of metal in the heating coil tends to change the frequency characteristic of the load circuit. This facilitates the need for frequency control to ensure maximum power transfer. Table 4.1 shows the resonant frequencies of the same load circuit with different metals placed inside the coil.

Metal	DIAMETER	MASS	FREQUENCY
	( <i>mm</i> )	(g)	(kHz)
Copper	12.5	27.8	195.5
Gold	10	20	160.4
Steel	12	18.5	126.1
Nickel	9	10.5	134.5
Lead	10	12	156.4
Brass	12	24.3	183.3

Table, 4.1: Resonant frequencies for various metals at room temperature, when placed in the prototype induction furnace

The resonant frequencies for different metals at room temperature were measured at low power levels using a function generator and oscilloscope to determine the frequencies at which zero phase shift between the driving voltage and current were observed in the load circuit.

The inner diameter of the heating coil was approximately 14mm. The natural resonant frequency of the tank circuit with the coil not loaded was 148kHz. It was observed that when a high conductivity, closely coupled metal (copper) is inserted into the coil, it causes the inductance of the tank circuit to decrease. This results in a shift in resonance, which means that the tank circuit must now be resonated at a higher frequency. When a steel work-piece is inserted into the coil its magnetic properties (permeability) tends to increase the inductance of the tank circuit, causing its resonant frequency to decrease.

This dynamic behavior of the load circuit (induction-heating load) is of major interest for the implementation of automatic frequency control. In a basic sense, automatic frequency control is implemented to compensate for changes, which occur in the load during the heating cycle. A basic understanding of the load behavior under various conditions is essential for the effective implementation of the RLL circuit.

## **4.3 LOAD CIRCUIT**

The induction-heating load forms part of a parallel resonant circuit, which is continuously driven at its natural resonant frequency by the inverter. The idealised equivalent circuit model for the induction-heating load is shown in figure 4.2.



Fig.4.2: Idealized equivalent circuit for induction heating load

The expression for the complex impedance of the parallel tuned circuit in figure 4.2 at any frequency (f) is given by equation  $4.1^{28}$ :

$$Z(f) = - - \frac{Rp}{1 + jQp} \left( \frac{f}{fo} - \frac{fo}{f} \right)$$
(4.1)

#### where:

Rp = Equivalent resistance of the tank circuit as seen by the source, Qp = Quality factor of the tank circuit and is given by Qp = Rp / XLp, fo = Natural resonant frequency of the tank circuit.

The equivalent circuit parameters were measured at low power with sinusoidal excitation from a signal generator. These tests were conducted in order to determine the load circuit parameters and calculations were performed where necessary. The load circuit was then simulated on ORCAD 9.1 using the measured and calculated values determined in the experiment. The simulated load circuit parameters transformed to the terminals of the source are discussed for three discrete conditions namely:

#### 4.3.1 Unloaded heating coil



Fig. 4.3: Equivalent load circuit parameters of induction heating load measured with an unloaded heating coil

Fig 4.4: Impedance characteristic of unloaded inductionheating coil. The circuit has 2 natural resonant frequency of 148 kHz and a Q of 18. The load circuit has a maximum impedance of 79  $\Omega$ .

The frequency response of the unloaded induction-heating coil is shown in figure 4.4. The resonant impedance is higher (79  $\Omega$ ) for unloaded conditions, which improves the systems no load performance<sup>30</sup> because of minimal current drawn from the supply (higher impedance at no-load). When the coil is loaded the load impedance is reduced and more current is drawn from the DC supply. The resonant frequency is approximately 148kHz with a Q of 18.

#### 4.3.2 Copper work-piece



Fig. 4.5: Equivalent load circuit parameters of induction heating load measured with a copper work-piece placed in the heating coil



The frequency response of the loaded induction-heating coil is shown in figure 4.6. The copper work-piece has the parameters as shown in table 4.1. The resonant impedance is lower (33  $\Omega$ ) for the loaded condition and more current is therefore drawn from the supply. The inductance of the coil (L2) is decreased due to the insertion of the copper work-piece resulting in an increase in the resonant frequency of the load circuit to approximately 195 kHz with a loaded Q of 10. The increase in resonant frequency results in a reduction in skin depth thereby increasing the equivalent resistance (R2) of the load circuit.





Fig. 4.7: Equivalent load circuit parameters of induction heating load measured with a steel work-piece placed in the heating coil



Fig 4.8: Impedance characteristic of inductionheating load with a steel work-piece placed in the heating coil. The circuit has a natural resonant frequency of 126 kHz and a Q of 3.5. The load

The frequency response of the loaded induction-heating coil is shown in figure 4.8. The steel work-piece has the parameters as shown in table 4.1. The resonant impedance is the lowest (18  $\Omega$ ) for this loaded condition and more current is drawn from the supply. The inductance of the coil is increased due to the insertion of the steel work-piece resulting in a decrease in the resonant frequency of the load circuit to approximately 126 kHz with a loaded Q of 3.5.

The Q acts as an impedance transformer in a parallel resonant circuit<sup>4</sup>. The lowering of the circuit Q as a result of inserting a steel work-piece, results in the reduction of the load circuit impedance. The steel work-piece is a better conductor of the magnetic flux in the coil than air is, which tends to increase the inductance of the coil (L3) as can be seen in figure 4.7. The equivalent resistance of the work-piece is also increased (R3) hence the power loss in the work-piece increases. This relationship is given by equation 4.2 for a relative permeability of several hundred in steel at room temperature<sup>18</sup>.

#### **4.2 CONCEPT OF RESONANCE LOCKING**

#### Phase Characteristic



Fig. 4.9: Phase relationship between driving voltage and driving current to tank circuit as a function of frequency. The characteristic illustrates the response for the three conditions discussed above. The respective resonant frequencies occur at the points of zero-phase displacement.

The analysis of the induction-heating load has shown that different resonant characteristics exist for different loading of the heating coil. It is clearly apparent that different loading changes all the parameters of the load circuit such as the natural resonant frequency, resonant impedance and inductance of the coil as well as the Q. It is evident that at a frequency f = fo, the impedance of the tank circuit is a maximum. At this frequency the phase displacement between the driving voltage and current to

the tank circuit is equal to zero. Figure 4.9 shows calculated phase characteristics for the three load conditions presented.

For a load circuit Q of greater than 10, this implies that maximum real power transfer is taking place at resonance as given by figure 4.9. This maximum operating point is where the induction furnace should operate at all times.

Figure 4.10 shows the combined complex impedance magnitude versus frequency plots for three conditions namely:

- 1. Coil unloaded (no work-piece)
- 2. Copper work-piece in coil
- 3. Steel work-piece in coil



Fig. 4.10: Frequency response for the induction heating tank circuit. The unloaded coil has a relatively high Q (approximately 18). When the coil is loaded the Q tends to decrease (8.25 for copper and 2.56 for steel). The resonance locked loop tracks the operating points  $f_{ir}$ ,  $f_1$  and  $f_2$  for different load conditions and therefore maintains maximum real power transfer to the load throughout the heating cycle.

Figure 4.10 shows the resonant frequencies,  $f_0$  for an unloaded coil,  $f_1$  for a copper work-piece and  $f_2$  for a steel work-piece placed in the coil. The unloaded coil resonates at approximately 148kHz, and has a Q of approximately 18.

When a steel work-piece is inserted into the coil, the inductance of the coil increases, changing the Q of the tank circuit as well as its resonant frequency. If the induction

furnace were to run in open loop, at frequency  $f_0$  with a steel work-piece, the system would be operating at point A on the steel work-piece curve. Operation at point A results in a reduction of power transfer to the load since point A is relatively close to the 3dB (1/2 power) point on this curve. When a copper work-piece is inserted into coil, the system operates at point B on the copper work-piece curve. With no frequency-tuning present, operation at point B would result in very little power transfer to the copper work-piece. Another drawback of operating at points A (steel) and B (copper) is that significant switching losses develop in the power source when driving a load off resonance<sup>4,7,8</sup>. The resonance locked loop therefore tracks the optimum operating points  $f_0$ ,  $f_1$  and  $f_2$  for different loading in the coil.

#### 4.3 RESONANCE LOCKING METHODOLOGY

The implementation of the resonance locked loop required the control of two distinct variables whose phase relationship was a function of the applied frequency of the power source. A simplified schematic of the current fed inverter (power source) is shown in figure 4.11.



Fig. 4.11: Basic current-fed inverter configuration employing power MOSFET's. Gate driver circuits have been omitted for



Fig. 4.12: Ideal waveforms of the driving voltage and current to the load circuit. It is apparent that the gate control signal (VGATE) is an approximate phase

The induction-heating load can be characterised by the equivalent circuit shown in figure 4.1. The load circuit is current supportive and is modeled with an ideal current source which warrants the use if the iron-core reactor in the inverter DC bus. The

switching elements in the inverter drive the load at a frequency determined by the switching rate of the control signals fed to the gate of the power MOSFETs. Switches S1, S2 and S3, S4 operate alternatively each to produce one half cycle of the RF power presented to the load terminals. Simulation results of the equivalent load circuit driven at resonance are shown in figure 4.12.  $V_{Load}$  is the driving voltage across the tank circuit and  $I_{Load}$  is the driving current through the load produced by the closure of switches S1, S2 and S3, S4 respectively.

Due to the principal of forced commutation<sup>30</sup> it is evident in figure 4.12 that the control voltage to the power MOSFET  $V_{gate}$ , is an actual phase representative of the driving current through the load. This concept is treated in the ideal sense and omits the propagation delay time taken to drive the MOSFET into the saturation mode of operation. This delay time is typically in the order of 200 – 300ns and is affected by the following factors:

- Rise and fall times of gate drive signal
- Value of gate resistor chosen for damping
- Input capacitance of the power MOSFET
- Stray inductance in the gate drive loop
- Characteristics of the load being switched by the power MOSFET (resistive or reactive)

This propagation delay results in a small offset phase error within the resonance locked loop. This phase error is encouraged as it has the effect of producing a nonzero output from the phase detector, which is required to maintain the control voltage at the VCO input, holding the system in lock<sup>16</sup>.

#### 4.3.1 Signal Measurement

In summary the control strategy employed utilized the following concepts:

- The inverter output voltage ( $V_{Load}$ ) was transformed to logic levels (900Vp-p to 25Vp-p) The voltage transformer was wound on an ETD29 ferrite core with a turns ratio of 40:1. This transformer is given by T4 in schematic 1 of Appendix B.
- Gate control signal fed to power MOSFET is used as a phase representative of the driving current. This factor eliminates the need for current measurement and simplifies the layout of the inverter, making it compact, and provides for stable operation.

Control of the inverter is achieved by continuously locking the gating control signal (V<sub>gate</sub>) to the inverter output voltage (V<sub>Load</sub>) over its entire operating range.

#### 4.4 CONTROL CIRCUIT IMPLEMENTATION

Research into the development of an Automatic Frequency Control system resulted in two final implementations. The implementation of the gate voltage locking method has eliminated the need for current measurement. Both systems were tested on the prototype induction furnace at full power where various work-pieces were heated. The systems (Rev1 and Rev2) proved to be stable over the entire operating range at both low and full power. A comparative discussion will be presented to summarize the individual system's performances.

#### 4.4.1 RLL revision 1

Automatic frequency control of the inverter was achieved by means of resonant mode locking. The control system, which is called a resonant locked loop (RLL) employed essentially two second-order phase locked loops. The basic system is shown below in figure 4.13.



Fig. 4.13: Simplified schematic representation of the resonance locked-loop comprising two phase locked-loops (Loop 1 and Loop 2). Loop 1 comprises an active filter which and is used to generate a 90° phase-shift in waveform B. Loop 2 comprises another active filter and is used generate a 90° phase-shift in waveform A. The AGC is used to supply a fixed amplitude signal to PD 2.

Phase detector 1 (PD1) is a type 1, exclusive-OR phase detector derived from the MC14046 PLL chip. Loop 1 operated as an active filter and was used to generate a  $90^{\circ}$  phase-shift in the current sample (waveform B). The  $90^{\circ}$  phase-shift is characteristic of the XOR gate PLL and was used to hold the phase detector in the center of its linear range (chapter 3). The phase-shifted current-sample waveform was

multiplied by the tank-circuit voltage (waveform A) in phase detector 2 (PD2). Phase detector 2 incorporated the AD734 4-quadrant analog multiplier. The analogue multiplier was used so that the transformed sinusoidal tank circuit voltage (waveform A) could be fed directly into the phase detector. PD 2 operated by locking the phase-shifted current sample 90° out of phase with the voltage waveform A. The 90° phase shift method was employed in order to ensure operation in the phase detector's (PD 1 and PD 2) linear region<sup>27</sup>. This operation locked waveforms A and C 180° out of phase. The result was a relative zero phase shift (anti-phase) between waveforms A and C. Inverting one of the waveforms initially resulted in a near zero phase shift when in locked operation. VCO 1 and VCO 2 were derived from two MC14046 PLL integrated circuit.

The automatic gain control stage (AGC) was used to convey a fixed amplitude signal to PD 2. It operates by amplifying or attenuating an incoming signal in order to maintain a fixed amplitude output signal. Under different load conditions the Q of the tank circuit changed, resulting in an amplitude change at a specific resonant frequency as shown in figure 4.10. Another reason for employing an AGC was to allow the induction furnace to operate at reduced power levels. It was found that by changing the amplitude of waveform A, an offset phase error was produced in phase detector 2 (analog multiplier) due to signal amplitude being below the minimum input offset voltage, which caused the loop to lock incorrectly. The AGC which incorporated the VCA610 was used to hold the amplitude of waveform A constant over the operating range of the induction furnace, hence produced no offset phase error in the multiplier.

The following derivation has proven the necessity for an AGC implementation in conjunction with an analog phase detector (PD2) in the system implemented. Assuming two uniformly time varying signals multiplied such that the multiplier output M is:

$$M = A\cos(\omega t + \phi_1) xB\cos(\omega t + \phi_2)$$
(4.3)  
$$= \frac{AB}{2}\cos(\phi_1 - \phi_2) + \frac{AB}{2}\cos(2\omega t + \phi_1 + \phi_2)$$
  
After low pass filtering Leaves :  
$$= \frac{AB}{2}\cos(\Delta\phi) \qquad \text{where } :\cos(\Delta\phi) = \cos(\phi_1 - \phi_2)$$
(4.4)

From the final expression of the output it can be seen that output phase of the multiplier ( $\cos \Delta \phi$ ) is dependent on the amplitude of the input signals (AB/2). It is therefore apparent that a fixed amplitude signal has to be fed to the multiplier in order to eliminate the problem of phase errors being produced over the operating range of the RLL. The actual circuit implementation of revision 1 is shown in appendix B2.

#### 4.4.2 RLL revision 2

The cost and complexity of RLL revision 1 has led to the development of a simpler, cheaper and more effective means of phase locking. Revision 2 introduced a similar system to the previously presented model, except for a few changes as shown in figure 4.13.



Fig. 4.14: Block diagram representation of the frequency control system. The system comprises two cascaded 2<sup>nd</sup> order PLL circuits, which lock at 90° phase-shift relative to its input. PD 1 and PD2 comprise XOR digital phase-detectors.

The frequency control system also comprises two 2<sup>nd</sup> order phase locked loops as shown in figure 4.14 but does not employ an AGC or an analog phase detector.

The two loops operate as 90° phase shifters maintaining lock over the entire operating range. Operation is also realised by comparison of the phase difference between the load voltage ( $V_{LOAD}$ ) and the switch gate voltage ( $V_{GATE}$ ). This phase difference is processed by loop 2 and a frequency change proportional to the phase difference is generated by VCO 2. This frequency difference is the clock signal, which is used to either drive the inverter to the new load resonant frequency, or hold it at the current resonant frequency.

The automatic frequency control system employed Type I Exclusive-Or phase detectors in both loops. Active 2<sup>nd</sup> order PI controllers where employed as the loop filters in LPF 1 and LPF 2. The use of active loop filters provided the necessary high gain to the loop and ensured good tracking performance with minimal static phase error. The total loop can be modelled as a 4<sup>th</sup> order PLL system and was found to be stable over the entire operating range. The actual circuit implementation is shown in appendix B3.

#### 4.4.3 Discussion

The following aspects were observed to be critical aspects in the design of the two RLL circuit implementations:

- Loop stability was greatly influenced by the bandwidth of the op-amps used in the phase shifter loop<sup>26,27</sup>. Op-amps with high gain bandwidth products were used.
- A second order PI controller was employed as part of the loop filter. Op-amps with very low input bias currents were used to avoid the integrator from charging in the wrong direction as well as drifting during normal operation<sup>31</sup>.
- Loop time constants were a critical factor in the design of a stable RLL system. Stable operation of the loop was achieved by making the time constant of LPF1 much faster than that of LPF2 (at least 10 times).
- No extra filtering circuitry was employed to condition signals before being fed to the RLL system. This factor simplifies the design and allows effective operation over a wide frequency range.
- The implementation of the zero-crossing detector ir revision 2 was a major contributing factor to the simplicity of the second design.
- Slew-rate limiting in the analog multiplier resulted in a phase error offset at the loop output.
- Employing active loop filters was a necessity because the low DC gain of passive loop filters did not enable lock in operation when the system was started up.
- Limiting the RLL lock range gives the system the properties of a highly selective filter. This feature gave the system extremely good noise rejection capability, which assisted in automatic start-up operation.

#### 4.4.4 Anti-Lock protection circuitry

An electronic protection circuit was incorporated to monitor the RLL operation during a heating cycle. The basic system is shown in figure 4.14.



Fig. 4.15: Block diagram representation of the frequency control system showing the anti-lock protection circuit. Operation of loop1 is monitored by a window comparator circuit. In the event of a loss of lock, the triggered timer deactivates the inverter PWM and operates the analog switch circuit, which simultaneously resets both loops, pulling the system back into lock operation.

The anti-lock or loss of lock protection circuit was developed as part of the electronic protection circuitry for to the induction furnace. The protection circuit section on figure 4.14 monitors loop1 status checking for an invalid operation. The input voltage to VCO 1 is fed to a window comparator circuit, which monitors the operating range of the VCO 1. If loss of lock occurs, the VCO driving voltage goes out of range and triggers the window comparator circuit. This circuit then triggers a CMOS timer configured as a monostable. Activation of the monostable deactivates the PWM signals to the inverter section and also activates analog switching circuit. The analog switch circuit simultaneously resets the loop-filters LPF1 and LPF2 by shorting out the integrating filter capacitor. This reset action pulls the RLL circuit to its center frequency, which is designed to be close to unloaded resonant frequency of the induction furnace. When the monostable has timed out the loop is reactivated and returns to normal lock operation.

The complete implementation of the anti-lock protection circuit is shown in appendix B3.

## **CHAPTER 5**

#### EXPERIMENTAL RESULTS

Two final circuit implementations resulted from the research into automatic frequency control of the induction furnace. Both systems were individually tested on the induction furnace at full power and at low power levels.

The AFC system was tested on the induction furnace where 50g slugs of steel and copper were heated respectively. The load circuit comprised a multi-turn induction-heating coil, which formed part of a high Q parallel resonant circuit. The system was driven in open loop and the frequency was adjusted to the natural resonance of the unloaded tank circuit. When a steel work-piece is placed inside the coil the inductance of the tank circuit increase. This effect makes the tank circuit capacitively reactive as shown in figure 6.



Fig. 5.1: Capacitively reactive tank circuit being driven by the inverter. Trace 1 shows the switching control signal fed to the MOSFET gate. Trace 2 shows the loss of zero voltage switching across the MOSFET's. Over voltage turn-on and turn-off spikes are also present, which could lead to the destruction of the switches at higher power levels.

The control-switching signal (VGATE) fed to the power MOSFET is shown in trace 1 of figure 5.1. Trace 2 shows the drain-source voltage (VDS) being switched by a MOSFET in the current-fed inverter. It is evident that the mismatch between the natural resonance and the current driving frequency has resulted in a loss of zero voltage switching as shown by trace 2. The loss of ZVS has also brought rise to over-voltage transients at both turn-on and turn-off of the switch. These transients increase dramatically in amplitude as the power is increased. This often results in the necessity to use special snubber circuitry to prevent MOSFET destruction. Driving the load off resonance also results in a reduction of load circuit impedance (as shown in figure 4.9) which resulting in excessive current being drawn from the DC supply.

#### 5.1 REVISION 1

The AGC circuit employed in revision 1 performed well over the entire operating range with no noticeable phase shift incurred by its operation. A high-speed (15Mhz) 4-quadrant analog multiplier (AD734) employed in PD2 was used to provide minimal phase error introduced by the multiplier at the operating frequency range in question (80kHz – 220kHz). A low speed (5Mhz) 4-quadrant multiplier (AD633) was initially incorporated as PD2 but slew rate limiting in the multiplier core produced offset phase errors in LOOP2.



Fig. 5.2: Gate voltage (trace 1) and transformed inverter midpoint voltage (trace 2) waveforms locked 90° out of phase by loop 1.

Figure 5.2 shows the loop in lock at an operating frequency of approximately 150kHz with a gold work-piece placed inside the crucible. The 90° phase shifted gate voltage (trace 1) and the transformed sinusoidal midpoint voltage (trace 2) are both fed to PD2 which locks the two incoming signals by phase displacing them a further 90°. The output of PD2 is shown in trace 2 of figure 5.3 with a copper work-piece placed inside the coil. Switching noise fed from the midpoint of the inverter to the RLL circuit causes the noise on the rising slope of the multiplier output (trace 2). The fast falling edge in the output of PD2 is the main factor which dictates the necessity for a high-speed (15 MHz) analog multiplier. Trace 1 shows the zero-voltage switching drain-source voltage (150Vpeak) across a power MOSFET in the inverter-bridge and is free of over-voltage transients.



Fig. 5.3: The inverter operating with RLL revision 1 in phase-lock. Trace 1 shows the zero-voltage switching drain-source voltage across a MOSFET in the bridge. The 90° phase shifted gate voltage and the transformed sinusoidal tank circuit voltage is multiplied together by the high-speed analog phase detector (AD734) PD2. The output of PD2 is shown in trace 2. The fast falling edges in the output waveform is the factor which dictates the use of a high slew-rate analog multiplier

Figure 5.4 shows the system in lock with the coil unloaded. Trace 1 is the transformed signal waveform A (figure 4.12) of a 400Vp-p voltage applied to the tank circuit at resonance. Trace 2 represents the 90° phase shifted current sample of loop 1, which is 180° out of phase with waveform A (figure 4.12) at 159kHz. When different loading occurs in the coil, the resonance locked-loop will change the driving frequency of the power source to maintain lock between the current sample (waveform A) and the tank circuit voltage waveform B (figure 4.12) over its full operating range (80kHz-220kHz).



Fig. 5.4: Gate voltage (trace 2) and transformed inverter midpoint voltage (trace 1) waveforms locked 180° out of phase to hold the tank circuit at resonance when operating the prototype induction furnace.

#### 5.2 REVISION 2

The following results are were taken from revision 2 of the automatic frequency control system implemented. This system was found to be the most feasible and cost effective solution of the two investigated for this research.

The resonance locked loop was tested on the prototype induction furnace, which was used to melt 30g of copper and 30g of gold at 1kW of DC input power with closed loop frequency control using revision 2. It was found that the system held the load at resonance throughout the heating cycle with no frequency drift or instability occurring over the operating frequency range (85k –220kHz).

The PLL system employed acts as a highly selective filter. This feature gives the system extremely good noise rejection capability, which assists in automatic start-up. With little power applied to the inverter, the zero-crossing detector generates random oscillations on its output. This acts as a noise input to the loop as shown in trace 1 of figure 5.5. This noise injected into loop occurs at a frequency, which is outside of the bandwidth of the AFC loop. The frequency control system therefore locks to the closest multiple of this noise within its bandwidth thereby holding the system in lock at start-up. Trace 2 of figure 5.5 shows one half cycle of the inverter output phase-locked to the 43<sup>rd</sup> harmonic of the noise injected into the loop.



Fig. 5.5: Trace 1 illustrates the zero crossing detector output as the automatic frequency control system acquires lock when the power is applied. The circuit acts as a selective filter extracting only the fundamental load resonant frequency component and rejects the high frequency noise injected into the loop. The drain- source voltage across a lower MOSFET in the bridge is given by trace 2.

Figure 5.6 shows the implementation of automatic frequency control to the induction furnace. It is evident that the ZVS is occurring in every cycle and no over-voltage transients are present as shown in trace 2. With the AFC system in operation the gate control signal (trace 1) is always phase-locked to the zero-crossing points of the tank circuit voltage (trace 2).



Fig. 5.6: Tank circuit driven at its natural resonant frequency by the power source. The AFC system is controlling the inverter switching frequency, thereby holding the load circuit in resonance at all times. ZVS can be observed in trace 2 with no overvoltage transients across the MOSFET switch.

Figure 5.7 shows the heating cycle of a steel work-piece. At room temperature the tank circuit resonates at 126kHz. As the work-piece is heated, its relative permeability decreases and approaches unity. This causes a decrease in the resonant frequency of the tank circuit. At the curie transition ( $\approx$ 710 °C to  $\approx$ 780°C) in figure 5.7, the relative permeability of the work-piece has fallen to unity and the steel loses its magnetic properties [4]. This results in a decrease in inductance of the tank circuit, resulting in a major shift in the resonant frequency (from 125k –175k) of the tank circuit. The work-piece was heated to 1180°C. After the transition through curie temperature, the resonant frequency increases slightly due to the change in resistivity of the steel work-piece. The temperature of the work-piece was measured by means of a radiation pyrometer, which was immune to the magnetic fields produced in the heating coil.



Fig. 5.7: Heating cycle of a steel work-piece in the prototype induction furnace, showing the frequency change as the metal is heated through its curie point.

# **CHAPTER 6**

# CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

#### 6.1 CONCLUSIONS

The automatic frequency control system has been successfully implemented by virtue of "gate-voltage locking" and the induction-furnace has been tested on a number of different metals. The rapid frequency changes that occurred when heating steel through curie temperature (figure 5.7) has proven that the resonance locked-loop can track changes and maintain lock at the natural resonant frequency of the tank circuit. The implementation of the resonance locked-loop eliminates the need for manual tuning and provides for a more accurate and effective means of closed loop frequency control, providing maximum power transfer to the load at all times.

The system proved to have the following advantages:

- 1. The implementation of the actual circuit utilized fewer and less expensive components than revision 1 and therefore provided a relatively cost effective approach for frequency control.
- 2. The implementation of AFC eliminates the need for manual open loop frequency control and has optimized the inverter performance.
- The continuous ZVS achieved has eliminated the need for snubber circuitry and also allows the MOSFET switches to be driven closer to their maximum voltage ratings.
- 4. No current measuring circuitry was needed for the approximation of the load current phase displacement. This technique of phase locking is simpler and only utilizes the measurement of the load voltage and gate control voltage to the inverter.

- 5. No special matched filtering circuitry was needed to filter the signals to be phaselocked. The AFC system performed an inherent filtering function as mentioned in chapter 5.
- 6. The high gain active loop filters employed, provided optimum tracking performance with reduced steady-state phase error.
- 7. Automatic start-up operation was achieved by virtue of the implementation of active loop filters. At startup, the smallest phase error signal fed to the loops from the phase detectors (PD1 and PD2) are integrated to zero. This feature holds the system in lock from the start, hence allowing automatic start-up operation of the induction furnace.
- The use of the XOR PD's provided good circuit immunity to the radiated EMI radiated by the magnetic field inside the coil and power source during a typical heating cycle
- 9. The system response to a step change in phase when a work-piece was inserted into the coil proved to be satisfactory. Tracking the curie-point transition of a steel work-piece during a typical heating cycle simulated the system response to a velocity change in phase, which also provides satisfactory results.
- 10. The basic electronic loss of lock protection was provided for the AFC system. It monitored the status of the control system and detected a loss of lock. The system then performed a corrective action by simultaneously resetting both loops and providing a trip signal for future auxiliary protection.

The resonance locked-loop was therefore found to be suitable for the application of automatic frequency control of the prototype miniature induction furnace. The successful implementation of AFC on this system has encouraged investigation into the application of this control strategy to other resonant-mode power electronic converters for induction heating. The concept of "gate-voltage locking" has provided a breakthrough for this research with regards to frequency control and possibilities of other forms of frequency control using this technique can be investigated.

#### 6.2 **RECOMMENDATIONS FOR FUTURE WORK**

Current research is underway to melt platinum slugs (20g), which would test the system's stability at higher output power levels (2kW). Further tests to investigate the effect of the phase transformation of a solid work-piece to its molten liquid state are to be conducted. These results will provide valuable information regarding the detection of the melting point of a metal by virtue of a frequency shift during the heating cycle. This method could save major costs invested in radiation pyrometers for temperature measurement.

A mathematical model of the load and frequercy control circuit will aid the designing of effective frequency control systems. The two working systems (Revision 1 and Revision 2) will provided the foundation on which the numerical model will be based. The aim of this study will be to provide a working model which can be applied to the designing any frequency control system for power electronic converters.

The following improvements could be implemented to the existing frequency control system:

- High bandwidth optical isolation between the AFC system and the inverter drivers could be implemented. This procedure would separate the control circuit ground from the inverter power ground thus providing better noise immunity to the system.
- PCB prototyping of Revision 2 is currently underway in preparation for the melting of platinum. The current prototypes (Revision 1 and Revision 2) were constructed on veraboard for testing.
- A theoretical model of the working systems (Revision 1 and Revision 2) will provide valuable information for the design procedure of future AFC systems at any operating frequency range for various induction heating applications.

- A frequency control system incorporating the use of the type II phase detector (in place of the XOR) and active loop filters could be investigated for future research. The noise immunity of the edge triggered PD (RS latch) in the new PLL system would have to be investigated further. Special noise shielding techniques could be employed to allow stable operation in this mode.
- A simpler lock-detection circuit incorporating an R-S latch could also be investigated. This system would eliminate the use of the window comparator circuit thereby simplifying the overall design.
- Application of "gate-voltage locking" to other resonant-mode power electronic converters for induction heating. A voltage-fed inverter is to be developed for induction heating and the control strategy employed in this research is to be implemented on the inverter, as a means of automatic frequency control.
- A self-oscillating resonant inverter incorporating "gate-voltage locking" is to be investigated. It is believed that the zero crossing points across the load circuit voltage in a present cycle of operation could be used to generate the switching transition signals for the next cycle of operation. This system could be implemented, but requires some thought with regards to start-up operation.

Future projects on the development of the induction-furnace include:

Temperature control

The temperature of the work-piece has to be monitored throughout the heating cycle to ensure that the work-piece temperature never exceeds the maximum temperature of the crucible. The work-piece is heated to its molten form, hence no contact measurement can be allowed as contamination of precious metal quickly occurs. A radiation pyrometer could be employed to monitor the temperature of the work-piece throughout the heating cycle. The output signal from a pyrometer can be used to feed a translator circuit, which would either advance or delay the firing angle of the controlled rectifier bridge, and accurate power control to the work-piece can be achieved. The implementation of temperature control would be advantageous because it would extend the applications of the induction furnace. The system could then be

used for special laboratory applications, which require precision heating of small quantities of metal. Examples of applications are silicon crystal growing, tungsten refining and special high-purity alloying with metals like titanium, ruthenium and platinum.

#### Protection circuitry

Overload and short circuit protection needs to be implemented to the system. This kind of protection could involve inserting a circuit breaker into the DC bus, which would operate when a fault was being sensed. Due to the presence of the iron core reactor in the DC bus, the protection circuitry will be given adequate time to respond to a fault condition.

#### Cooling water monitoring

The most common type of failure present in induction furnaces is cooling water failure. Dangerous consequences could result if no monitoring of the flow rate and temperature of cooling water was present. A temperature sensor such as the LM35 could be employed to monitor the temperature of the water. When the set point temperature of the water is reached, a signal could be fed to the cooling water pumps to increase the flow rate of the water, hence lowering the temperature of the cooling water. Differential pressure sensors could be employed to monitor the flow rate of the water. When an undesirable condition is reached, a signal could be fed to the protection circuitry to operate and trip the system.

#### • Front end power factor correction

Investigations need to be conducted to determine what kine of harmonics the system could be injecting back into the line frequency power source. If the need arises a front-end power factor correction system could be implemented, which would incorporate a DC-DC converter in place of the controlled rectifier. If the system is to be sold to foreign markets (e.g. Europe) it would have to comply with certain harmonic standards.

## • Microprocessor implementation

An embedded micro-controller could be implemented as the main unit which would monitor and control all of the above mentioned processes. A simple PIC or DSP could be employed for this application.

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## APPENDICES

## **APPENDIX A: LOOP DESIGN EQUATIONS**



Fig.1: Block diagram model of frequency control system.

The equivalent model for the frequency control circuit of revision 2 is given by figure 1. The system consists of two cascaded  $2^{nd}$  of der phase-locked loops which operate by tracking changes in the resonant frequency of the load circuit.

### LOOP COMPONENTS

Phase detector

The type 1 Phase detector (XOR) has a linear operating range of 180 degrees as shown in figure 3.19. The phase detector gain is therefore:

 $K\phi = Vdd/\pi$  (V/rad)

#### Loop filter

An active loop filter was used to provide optimum tracking and minimal static phase error. The loop filter consists of an integrator plus lead filter and its configuration is shown in figure 2




The loop transfer function K<sub>LF</sub> is represented in the frequency domain by:

$$F(s) = \frac{A(\tau_2 s + 1)}{(\tau_1 s + 1)}$$
<sup>[1]</sup>

#### where:

$$A = Rp/R1,$$
  

$$\tau_1 = (R2+Rp).C \text{ and}$$
  

$$\tau_2 = R2.C$$

```
• <u>VCO</u>
```

The transfer function of the VCO in the frequency domain is given by:

```
Ko =Kv/s (rad/s/V)
where
Kv = 2\pi (fmax - fmin)/Vdd-3.6V (rad/s/V)
```

#### Feedback

The feedback loop usually contains a gain, Kn which represents a counter module of value 1/N where N is the didviding ratio of the counter.

#### TRANSFER FUNCTION

The open loop transfer function of a second order loop is given by:

$$GH(s) = \frac{K(\tau_{2}s+1)}{s(\tau_{1}s+1)}$$
[2]

where: K = A.  $K\phi$ .Kv.Kn

The open loop transfer function yields a type 1, second order system which should produce zero steady state phase error for a step phase input.

The characteristic equation for the loop is given by:

$$C.E: s^{2} + \frac{(K\tau_{2} + 1)}{\tau_{1}}s + \frac{K}{\tau_{1}} = 0$$
[3]

Appendices

This allows for the formulation of the expressions for  $\omega_n$  and  $\zeta$  :

and

$$\omega_n = \sqrt{\frac{K}{\tau_1}}$$
 [4]

$$\zeta = \frac{(K\tau_2 + 1)}{2\omega_n \tau_1}$$
 [5]

This allows for the design of a desired loop response. It is evidant that  $\omega_n$  can be controlled by adjusting the value of  $\tau_1$ . It is also evident that the damping factor  $\zeta$  can be controlled by adjusting  $\tau_2$ .

#### **APPENDIX B: SCHEMATICS**

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#### 1. SCHEMATIC LAYOUT OF INDUCTION FURNACE



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# APPENDIX B: SCHEMATICS

# 1. SCHEMATIC LAYOUT OF INDUCTION FURNACE





#### 2. AUTOMATIC FREQUENCY CONTROL SYSTEM REVISION 1



#### 3. AUTOMATIC FREQUENCY CONTROL SYSTEM REVISION 2

#### APPENDIX C: TECHNICAL DATA

IRFF460 ENHANCEMENT-MODE POWER MOSFET

**IR2113 HIGH AND LOW SIDE MOSFET DRIVER** 

AD734 HIGH-SPEED ANALOG MULTIPLIER

VCA 610 AUTOMATIC GAIN CONTROL IC

CD4046 CMOS PLL IC

**DG301 ANALOG SWITCH** 

# International IOR Rectifier

HEXFET<sup>®</sup> Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- · Ease of Paralleling
- Simple Drive Requirements

#### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications



PD-9.512B

**IRFP460** 



DATA Sheets

#### **Absolute Maximum Ratings**

	Parameter	Max	Units
ID @ Tc = 25°C	Continuous Drain Current, VG5 @ 10 V	20	
lo @ Tc = 100°C	Continuous Drain Current, VGS @ 10 V	13	A
IDM	Pulsed Drain Current	60	
PD @ Tc = 25°C	Power Dissipation	280	W
	Linear Derating Factor	22	Ū W Č
Vgs	Gate-to-Source Voltage	220	r v
Eas	Single Pulse Avalanche Energy 2	960	- mJ
lan .	Avalanche Current @		Â
EAR	Repetitive Avalanche Energy 1	28	mJ
dv/dt	Peak Diode Recovery dv/dt 12	3.5	Vins
 Tu	Operating Junction and	-55 to + 150	
TSIG	Storage Temperature Range		^C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 fbf+n (1 i N+m)	

#### **Thermal Resistance**

	Parameter	_ <u>Nn</u>	Тур	Max Units
Rwc	Junction-to-Case		<i>–</i> .	0 45
Racs	Case-to-Sink, Flat, Greased Surface		0.24	: "CW "
Reja	Junction-to-Ambient			40

# International **ICR** Rectifier

Data Sheet No. PD601471

# IR2110/IR2113

## HIGH AND LOW SIDE DRIVER

#### Features

- Floating channel designed for bootstrap operation Fully operational to +500V or +600V Tolerant to negative transient voltage dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- Separate logic supply range from 5 to 20V Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- · Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

#### Description

The IR2110/IR2113 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 or 600 volts.

#### **Typical Connection**

#### Product Summary

Vof	FSET (IR2110) (IR2113)	500V max. 600V max.
	I <sub>O</sub> +/-	2A / 2A
Vout		10 - 20V
t <sub>on/off</sub> (typ.)		120 & 94 ns
De	lay Matching	10 ns

#### Packages





# ANALOG DEVICES

# 10 MHz, 4-Quadrant Multiplier/Divider

# AD734

#### CONNECTION DIAGRAM

14-Lead DIP (Q Package and N Package)



#### FEATURES

High Accuracy 0.1% Typical Error High Speed 10 MHz Full-Power Bandwidth 450 V/µs Slew Rate 200 ns Settling to 0.1% at Full Power Low Distortion -80 dBc from Any Input Third-Order IMD Typically -75 dBc at 10 MHz Low Noise 94 dB SNR, 10 Hz to 20 kHz 70 dB SNR, 10 Hz to 20 kHz Direct Division Mode 2 MHz BW at Gain of 100

#### APPLICATIONS

High Performance Replacement for AD534 Multiply, Divide, Square, Square Root Modulator, Demodulator Wideband Gain Control, RMS-DC Conversion Voltage-Controlled Amplifiers, Oscillators, and Filters Demodulator with 40 MHz Input Bandwidth

#### PRODUCT DESCRIPTION

The AD734 is an accurate high speed, four-quadrant analog multiplier that is pin-compatible with the industry-standard AD534 and provides the transfer function W = XY/U. The AD734 provides a low-impedance voltage output with a full-power (20 V pk-pk) bandwidth of 10 MHz. Total static error (scaling, offsets, and nonlinearities combined) is 0.1% of full scale. Distortion is typically less than -80 dBc and guaranteed. The low capacitance X, Y and Z inputs are fully differential. In most applications, no external components are required to define the function.

The internal scaling (denominator) voltage U is 10 V, derived from a buried-Zener voltage reference. A new feature provides the option of substituting an external denominator voltage, allowing the use of the AD734 as a two-quadrant divider with a 1000:1 denominator range and a signal bandwidth that remains 10 MHz to a gain of 20 dB, 2 MHz at a gain of 40 dB and 200 kHz at a gain of 60 dB, for a gain-bandwidth product of 200 MHz.

The advanced performance of the AD734 is achieved by a combination of new circuit techniques, the use of a high speed complementary bipolar process and a novel approach to laser-trimming based on ac signals rather than the customary de methods. The wide bandwidth (>40 MHz) of the AD734's input stages and the 200 MHz gain-bandwidth product of the multiplier core allow the AD734 to be used as a low distortion.

#### REV. C

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demodulator with input frequencies as high as 40 MHz as long as the desired output frequency is less than 10 MHz

The AD734AQ and AD734BQ are specified for the industrial temperature range of -40°C to +85°C and come in a 14-lead ceramic DIP. The AD734SQ 883B, available processed to MIL-STD-883B for the military range of -55°C to +125°C, is available in a 14-lead ceramic DIP.

#### PRODUCT HIGHLIGHTS

The AD734 embodies more than two decades of experience in the design and manufacture of analog multiphers, to provide:

- A new output amplifier design with more than twenty times the slew-rate of the AD534 (450 V.us versus 20 V(µs) for a full power (20 V pk-pk) bandwidth of 10 MHz
- Very low distortion, even at full power, through the use of circuit and trimming techniques that virtually eliminate all of the spurious nonlinearities found in earlier designs.
- 3. Direct control of the denominator, resulting in higher multiplier accuilley and a gain-bandwidth product at small denominator values that is typically 200 times greater than that of the AD 534 in divider modes.
- 4. Very clean transient response, achieved through the use of a novel input stage design and wide-band output amplifier, which also ensure that distortion remains low even at high frequencies
- 5 Superior noise performance by careful choice of device geometries and operating conditions, which provide a guaranteed 58 dB of dynamic range in a 20 kHz bandwidth

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## VCA610

# WIDEBAND VOLTAGE CONTROLLED AMPLIFIER

#### FEATURES

- WIDE GAIN CONTROL RANGE: 80dB
- SMALL PACKAGE: 8-pin SOIC or DIP
- WIDE BANDWIDTH: 30MHz
- LOW VOLTAGE NOISE: 2.2nV/√Hz
- FAST GAIN SLEW RATE: 300dB/μs
- EASY TO USE

#### DESCRIPTION

The VCA610 is a wideband, continuously variable, voltage controlled gain amplifier. It provides lineardB gain control with high impedance inputs. It is designed to be used as a flexible gain control element in a variety of electronic systems.

The VCA610 has a gain control range of 80dB (-40dB to +40dB) providing both gain and attenuation for maximum flexibility in a small 8-lead SO-8 or plastic dual-in-line package. The broad attenuation range can be used for gradual or controlled channel turn-on and turn-off for applications in which abrupt gain changes can create artifacts or other errors. In addition, the output can be disabled to provide -80dB of attenuation. Group delay variation with gain is typically less than  $\pm 2$ ns across a bandwidth of 1 to 15MHz.

The VCA610 has a noise figure of 3.5dB (with an  $R_s$  of 200 $\Omega$ ) including the effects of both current and voltage noise. Instantaneous output dynamic range is 70dB for gains of 0dB to  $\pm$ 40dB with 1MHz noise bandwidth. The output is capable of driving 100 $\Omega$  The high speed, 300dB  $\mu$ s, gain control signal is a unipolar (0 to  $\pm$ 2V) voltage that varies the gain linearly in dB V.

#### **APPLICATIONS**

- OPTICAL DISTANCE MEASUREMENT
- AGC AMPLIFIER
- ULTRASOUND
- SONAR
- ACTIVE FILTERS
- LOG AMPLIFIER
- IF CIRCUITS
- CCD CAMERAS

The VCA610 is designed with a very fast overload recovery time of only 200ns. This allows a large signal transient to overload the output at high gam, without obscuring low-level signals following closely behind. The excellent overload recovery time and distortion specifications optimize this device for lowlevel doppler measurements.



International Auroport Industrial Park + Mailing Address, PO Box 11400, Tucson, AZ 85734 + Street Address, 6730 S. Tucson, Bivd., Tucson, AZ 85755 + Tel. (520) 746-1111 + Twx, 910-952-1111 Internet: http://www.burr/brown.com/ + FAXLine (800) 548-6133 (US:Canada Oniyi + Cable, BBRCORP + Telex, 066-6491 + FAX (520) 889-1510 + Immediate Product Info. (800) 548-6132

C1992 Burr-Brown Corporation

#### FAIRCHILD

SEMICONDUCTORIM

#### CD4046BC Micropower Phase-Locked Loop

#### **General Description**

The CD4046BC micropower phase-locked loop (PLL) consists of a low power, linear, voltage-controlled oscillator (VCO), a source follower, a zener diode, and two phase comparators. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal.

Phase comparator I, an exclusive OR gate, provides a digital error signal (phase comp I Out) and maintains 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle), it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency.

Phase comparator II is an edge-controlled digital memory network. It provides a digital error signal (phase comp. It Out) and lock-in signal (phase pulses) to indicate a locked condition and maintains a 0° phase shift between signal input and comparator input

The linear voltage-controlled oscillator (VCO) produces an output signal (VCO Out) whose frequency is determined by the voltage at the VCO<sub>IN</sub> input, and the capacitor and resis tors connected to pin C1<sub>A</sub>, C1<sub>B</sub>, R1 and R2

The source follower output of the VCO<sub>R4</sub> (demodulator Out) is used with an external resistor of 10 k $\Omega$  or more

. \_ \_ \_

The INHIBIT input, when high disables the VCO and source follower to minimize standby power consumption. The zener diode is provided for power supply regulation, if necessary.

October 1987

Revised January 1999

#### Features

- Wide supply voltage range: 3 0V to 18V
- Low dynamic power consumption: 70  $\mu$ W (typ.) at f<sub>c</sub> = \*0 kHz, V<sub>DD</sub> = 5V
- VCO frequency 1.3 MHz (typ ) at V<sub>DD</sub> = 10V
- Low frequency drift = 0.06%/°C at V<sub>DD</sub> > 10V with temperature
- High VCO linearity 1% (typ)

#### Applications

- FM demodulator and modulator
- · Frequency synthesis and multiplication
- Frequency discrimination
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Tone decoding
- FSK modulation

....

Motor speed control

\_ . .

#### Ordering Code:

Order Number	Package Number	Package Description
CD4046BCM	M16A	16-Lead Small Outline integrated Circuit (SOIC), JEDEC MS-012, 0 150" Narrow Body
CD4046BCN	N16E	16-Lead Plastic Dual In-Line Package (PDIP), JEDEC MS-001, 0 300" Wide
Devices also avadable	in Tape and Reel Specify	by appending the suff ix letter 1X1 to the ordering clude

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#### **Connection Diagram**





#### DG300A, DG301A, DG303A

#### File Number 3119.2

#### TTL-Compatible, CMOS Analog Switches

The DG300A through DG303A family of monolithic CMOS switches are truly compatible second source of the original manufacturer. The switches are latch-proof and are designed to block signals up to 30V<sub>P.P</sub> when OFF. Featuring low leakage and low power consumption, these switches are ideally suited for precision application in instrumentation, communication, data acquisition and battery powered applications. Other key features include Break-Before-Make switching, TTL and CMOS compatibility, and low ON resistance. Single supply operation (for positive switch voltages) is possible by connecting V- to 0V.

#### Features

- Low Power Consumption
- Break-Before-Make Switching
   ton
   150ns
- TTL, CMOS Compatible
- Single Supply Operation
- True Second Source

#### Ordering Information

PART NUMBER	TEMP.   RANGE ( <sup>o</sup> C)	PACKAGE	PKG. NO.
DG300ABK	-25 to 85	14 Ld CERDIP	F14 3
DG301ACJ	0 to 70	14 Lo PDIP	E14 3
DG303AAK	-55 to 125	14 Ld CERDIP	F 14 3
DG303ABK	-25 to 85	14 Ld CERDIP	F14 3
DG303ACJ	0 to 70	14 Ld PDIP	E14 3
DG303ACY	0 to 70	16 Ld SMIC	M16-3

Functional Diagrams and Pinouts (Switches shown for a logic "1" input)



	DG300A TRUTH TABLE		
	LOGIC	SWITCH	
) D <sub>1</sub>	0	OFF	
	. 1	011	
	Logic "0" ≤ 0.8V Logic "1" ≥ 4.0V		

DG301A TRUTH TABLE

SWITCH 1

OFF

ON

Logic 01 < 0.8V Logic 1 24.6V

LOGIC

0

1

SWITCH 2

011

OFF







DG301A (SPDT)



CAUTION: These devices are sensitive to electrostatic discharge, folicik proper IC Handling Procedures http://www.intersil.com/or.407-727.92427 -> Copytight 5 Intersil Corporation, 1999

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