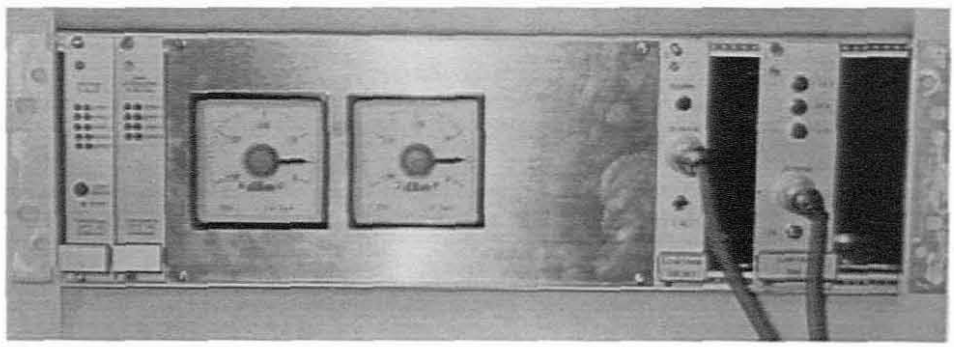
Microprocessor Controlled Communication Line Level Meter



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Statements and Acknowledgements

I Pierre Delport state hereby that the contents of this thesis is my own work and that the opinions contained herein are my own and not necessarily those of the Technikon.

This thesis has not previously been submitted for academic examination towards any qualification.

Thanks to ESKOM for allowing me to do the project and for the use of a computer, word-processor and printer.

Thanks to Pierre de Vos for the help on programming the micro-controller.

All data-sheets were taken from National Semiconductor, Intel and Analogue Devices data books.

Synopsis

ESKOM control a massive power grid in a vast geographical area in the R.S.A.. This power originates at the power stations, from where it is distributed to the users. All the power generated is pumped into a National Power Grid. The backbone of the network consists of the following supply voltages:

- 765 kV
- 400 kV
- 132 kV

These voltages are stepped down locally at substations to lower voltages for the customers. Bigger customers (e.g. Municipalities, Mines, etc.) are bulk users and use high voltages. Lower voltages range from 220V up to 66kV.

In order to ensure a good service to all power user customers ESKOM must be able to identify power failures and other abnormal conditions as quickly as possible and react fast to restore power again.

When supervising a power grid good communication systems are essential. Communications systems serve as links between the following functional systems:

- Contacting personnel with radio (Mobile or Handheld)
- Contacting personnel with pagers (Digital or Analogue)

- Receiving up to date information on the SCADA network
- Protection on power lines and transformers (Fault conditions)

Without good telecommunication ESKOM will not be able to control the national grid efficiently. The Telecommunication Department fulfil a vital role ensuring that the National Grid functions at its optimum.

It is normally impossible to do an accurate measurement of the power level in dBm or dBv on a communication line while an RTU is communicating to the MASTER.

This is mainly because the duration of the data burst on the communication line is less than the sample time required by the level meters available. The time duration on a TELKOR PUTU general poll is 250ms. With the available digital meters (e.g. W &G SPM33A) it is totally impossible to get a power level reading because the sampling time of the instrument is 1 second. With the analogue meters available (e.g. W&G SPM09, SPM31) it is possible to get a reading, but this normally between 2 dBm and 4 dBm low, because of the dynamic behaviour of the moving coil. Thus before the pointer of the meter has reached the correct level, the burst of data has stopped This is characterised by three quantities:

1. The inertia (J) of the moving coil about its axis of rotation.
2. The opposing torque (S) developed by the coil suspension
3. The damping constant (D)

A solution is to sample the receive and transmit levels during polling with an electronic circuit and feed it into an ADC connected to a Microcontroller (e.g. 8031 family). The Microcontroller will do all the converting and mathematical functions and will output a value through a DAC. This output value will be a current(mA) value directly proportional to the input level (e.g. -20dBm to 0dBm = 0 to 5mA). These RX and TX level values can be fed into analogue inputs of the RTU. This real-time measurement of the levels on communication lines will be available at the SCADA master. These values can then be trended and if a downward trend is observed, maintenance can be done on the line before a failure. This should result in higher availability of the SCADA network.

Synopsis

ESKOM beheer 'n massiewe elektriese krag netwerk oor 'n groot geografiese gebied in the R.S.A. Hierdie elektriese krag het sy oorsprong by die kragstasies, vanwaar dit versprei word na die verbruikers. Alle elektriese krag wat opgewek word, word aan die Nasionale Netwerk gelewer. Die ruggraat van die netwerk bestaan uit die volgende spannings:

- 765kV
- 400kV
- 132kV

Hierdie spannings word verminder by plaaslike substasies vir die verbruikers. Groter verbruikers (b.v. Munisiepaliteite, Myne, ens.) gebruik hoë spannings. Lae spannings wissel van 220V tot 66kV.

Om te verseker dat 'n uitstekende diens aan al die verbruikers gelewer word, moet ESKOM vinnig kragonderbrekings en abnormale toestande op die netwerk kan identifiseer en vinnig kan reageer om die onderbreking te herstel.

Om 'n kragnetwerk effektief te beheer, is 'n goeie kommunikasie stelsel nodig. Dit word gebruik vir die volgende:

- Om personeel te kontak in die veld (Radio)

- Om Toesigbeheer op die apparaat in die veld te hê (SCADA).
- Beveiliging van kraglyne en transformators

Sonder goeie telekommunikasie sal dit onmoontlik wees om die elektriese netwerk effektief te beheer. Die telekommunikasie departement vervul hier 'n belangrike rol om te verseker dat die Nasionale Netwerk maksimaal benut word.

Dit is normaalweg onmoontlik om 'n akkurate spanningsvlak meeting te doen in dBm of dBv op 'n kommunikasie lyn terwyl 'n Slaaf stasie in 'n afstandbeheerde sisteem met die Meester stasie kommunikeer.

Die hoofrede hiervoor is dat die tydsduur van die data korter is as die monstertyd wat nodig is vir die beskikbare meetinstumente om die data te verwerk. Die tyd vir 'n TELKOR PUTU (Slaaf stasie) se kortste boodskap is 250ms. Met die beskikbare digitale drywing meters (bv. W&G SPM33) is dit totaal onmoontlik, omdat die verwerkingstydperk van die meter 1 sekonde is. Met die analoog meters beskikbaar (bv. W&G SPM09 ann SPM31) is dit moontlik, maar die lesings is gewoonlik tussen 2 dBm en 4 dBm laag, as gevolg van die dinamiese eienskappe van die bewegende spoel van die meter. Met ander woorde voor die meter se naald die korrekte waarde bereik, het die data gestop. Die volgende drie kwantiteite bepaal die bewegende meter se karakter:

1. Die traagheid (J) van die bewegende spoel om sy eie as.

2. Die oponerende wringkrag (S) onwikkel deur die spoel se suspensie.

3. Die dempings konstante (D)

Die beste oplossing is om die ontvang en send seine te probeer monster met 'n elektroniese baan en dit te voer na 'n ADO wat gekoppel is aan 'n mikro verwerker (bv. 8031 familie). Die mikro verwerker doen dan al die omskakelings en wiskundige verwerkings en verskaf 'n analoog uittreewaarde deur 'n DAO. Hierdie uittreewaarde moet in mA wees en direk eweredig aan die intreewaarde (bv. -20dBm tot 0dBm = 0 tot 5mA). Die ontvang en send waardes kan dan gebruik word vir 'n slaaf stasie se analoog intree poorte. Hierdie sal 'n akkurate en onmiddelike lesing wees van die drywing en beskikbaar wees by die meester stasie. Hierdie waardes kan gestoor word in 'n data basis en 'n daar sal onmiddelik waargeneem word indien die waardes besig is om te dryf. Vinnige optrede deur tegniese personeel is dan moontlik om the kommunikasie lyn weer in te stel voordat 'n onderbreking plaasvind. Dit sal 'n hoër beskikbaarheid van die stelsel meebring.

Contents

Appendix C

1. Introduction

With a Company like ESKOM it is essential to have good quality communication circuits out to the Substations in the field. At each Substation is a RTU (Remote Terminal Unit), which must communicate with a Mainframe Computer System at our Control Centre. This is called a SCADA system(Supervisory Control and Data Acquisition)

A RTU is defined as a computer with I/O ports, which communicates with a master computer system. The RTU performs the following functions:

- Accept alarm inputs or conditions (Input device).
- Does controls (Output device).
- Accept analogue inputs with an ADC (Input device)

An RTU must be able to accept raw data from the plant, process it and transmit this information to the SCADA Master. It must also be able to receive messages from the SCADA Master, process the information and utilize it (e.g. do a control).

A SCADA network normally use polling RTU's. A polling RTU is defined as an RTU that will only react when it receives a message from a SCADA master containing it's own address and which will request a reply (e.g. TELKOR PUTU, IST ERTU, L&N SCALD). The reason why poling RTU's are used is that more than one RTU can be on one communication line, each with its own address. If a single remote/master system is used (every remote has it's own master), FDM or TDM must be used to put more than one system on one

communication line. This is due to thefact that each RTU and MASTER use a unique frequency. This will limit the amount of RTU's on the line (e.g. TIC 2P/2C systems).

This message can be a general poll, analogue update, one shot control, two shot control, etc. For a reliable telecontrol system it is essential to have good communication lines from the SCADA master to the RTU's in the field. It is therefore necessary to do periodic routine maintenance on the systems and testing of the communication lines. This also involves the measurement of the power levels on the transmit as well as receive lines.

The SCADA system is used to do the following:

1. Notify the Control personnel at the control centre of any abnormal condition out at the substation, e.g. Voltages out of limit, alarms, breaker trips, etc.

2. Enable the Controllers to do Remote Controls at the substations, e.g. Reset abnormal conditions and open or close breakers remotely.

3. Supply trends on analogue values, e.g. MW, Mvar, Amp, kV, Frequency, etc.

As you can see without a reliable SCADA system it is impossible to control an electrical network efficiently. Without a reliable communication network it is impossible to have a reliable SCADA system.

A communication system will function properly only when it is set up properly. This means that the signal levels on the system are set up to the manufacturer's specifications or the CCITT recommended levels.

If the levels that are connected into the system (TX or transmit levels) are too high it can overload the system and if it is too low, noise can corrupt the data on the system. If the levels coming out of the system (RX or receive levels) are too high it can damage the equipment it is connected to and if it is too low, noise will also corrupt the data.

Most of the data on the systems is FSK modulated which are sinusoidal wave type modulation. If the levels are to high the waveform will "clip" and thus will be distorted and data corruption will occur. When levels are too low, noise can be at the same level as the data, which will result in corruption of the waveform.

It is therefore important to have a good maintenance programme to continuously test the communication links. The following procedure is being used:

1. One technician goes to one end of the link with his test equipment. This can be far, some of our substations are 600km from the control centre.

2. Another technician goes to the other side of the link with his test equipment.

3. The communication line to be tested is taken out of service, thus disconnecting it from the communication system.

4. The communication line at the one end is looped back (The Receive and Transmit lines are disconnected from the RTU and connected together).

5. A test signal is injected at the other end at an certain level, looped back and received again. The Transmit signal is then compared with the Received signal enabling the technician to see if there was a loss of data (Bit Error Rate) or a change in level(dBm) between the RX and TX.

This method is however time consuming and not very productive, because two persons are required to drive to the two sites, of which one can be 6 hours drive and at least two technicians are needed for the test. We therefore need a better solution that will enable us to do tests automatically and warn us if the quality of the line is deteriorating.

A good system must be able to monitor the lines automatically and indicate in advance of a failure in order for preventative maintenance to be carried out.

Fault Statistics

The following table is a summary of Telecommunication Faults handled by Telecomms and Control Western Cape during the time 30 June 1995 to 30 June 1996.

Section	Total Outage Hours	Mean Down Time in Hours	Mean Repair Time in Hours	Total Faults Cleared
Broadband	1939	14	1.8	162
Radios	7875	30	1.2	315
Power Line Carrier	406	11	2.2	40
Repeater	1542	16	1.9	151
Switches	7418	23	1.1	393
Telecontrol	2868	20	1.3	217
Telephones	7295	21	0.6	386

With the aid of a good preventative system the total faults as well as the down time of the faults should be less.

This should result in a higher availability for the telecomms system.

2 Measuring levels on Transmission Lines

Power Measurement in Decibels

With faultfinding as well as commissioning of equipment it is essential for all technical personnel to know how to use level meters as well as signal generators.

Before we can start on how to use the test equipment, we must understand what levels are and what the unit of measure is.

The DECIBEL

Let's start by looking at the word ***decibel*** itself. It is a combination of "deci" and "bel". Bel comes from Bell. It was chosen to honour Alexander Graham Bell, the inventor of the telephone. Deci is a prefix meaning one-tenth. To get more realistic numerical values it was decided to use one tenth of the "bel" value, thus the term decibel.

$$N_B \text{ (number of bels)} = \log \frac{P1}{P2}$$

$$N_{dB} \text{ (number of decibels)} = 10 \log \frac{P1}{P2}$$

The factors P1 and P2 represent the values of any two power levels that are to be compared. In general, power levels can be of any type: electrical, mechanical, thermal, etc. We are however concerned primarily with the power levels of communication signals at various points in the communication system. Power level comparisons are most meaningful when the

power levels are related in some way. For example, the power gain in an electronic amplifier (a comparison of the output power to the input power) is often expressed in decibels:

$$\text{gain (dB)} = 10 \log \frac{P_{out}}{P_{in}}$$

Why do we use the logarithm of the power ratio and not just the simple ratio of P1 and P2 ? The answer is that human physiological response to sensory stimuli such as light and sound is approximately power logarithmic. This means that, for example, if the sound power at your ear of an aeroplane flying overhead is 10 000 times the power , at your ear, of a person clapping hands close by, you do not perceive the aeroplane sound as being 10 000 times as loud. Your perception is more like 40 times since 10 log 10 000 = 40. Thus power ratios expressed in decibels provide information which is more closely related to real-life effects than do simple direct ratios.

We will mainly use two types of decibel readings:

- dBm (Related to 1mW in 600Ω termination)
- dBv (Related to Volt)

We will use the following formulas for electrical power:

- $P = VI$
- $P = V^2/R$
- $P = I^2/R$

dBV:

Decibel values can be measured with a voltmeter by using the following formulas:

$$P1 = (V1)^2 / R1 \qquad P2 = (V2)^2 / R2$$

$$N_{dBV} = 10 \log \frac{P1}{P2}$$

$$= 10 \log \frac{(V1)^2/R1}{(V2)^2/R2}$$

$$= 10 \log [(V1/V2)^2 \times (R2/R1)]$$

$$= 20 \log \frac{V1}{V2} + 10 \log \frac{R2}{R1}$$

If the resistance is the same at the two points where power is being considered, that is if R1 = R2, the second term becomes zero, thus:

$$N_{dBV} = 20 \log \frac{V1}{V2}$$

The practical significance of the above equation is that only a voltmeter is needed to determine decibel values if the resistance at the points of measurement are the same. Many multimeters manufactured primarily for the use of field technicians have a scale calibrated in decibels (e.g. Fluke 8060A). This scale is used when the meter is measuring ac voltage. With such meters the scale is accurate only for measurement across 600Ω loads. If the resistances

are not the same, the decibel value obtained by voltage measurement must be corrected by the use of the second term, 10 log R2/R1.

dBm:

Because the decibel formula contains a ratio (a comparison of two power levels), the decibel is said to be a relative unit. A relative unit is to be distinguished from an absolute unit. Examples of absolute units are amperes, volts, ohms, etc. However, absolute decibel units can be created with the use of set reference power levels against which to compare any other power level. The reference for the dBm unit is 1mW, thus:

$$N_{dBm} = 10 \log \frac{P1}{1mW}$$

Before we can start measuring levels we must still look at the following concepts:

- Bandwidth
- Impedance Matching
- Through reading
- Terminated reading

Bandwidth

Measurement of power on communication lines can be measured as ***"Wideband"*** or over a certain ***"Bandwidth"*** at a certain centre frequency. With wideband the measurement is taken over the whole frequency spectrum that the instrument can handle. In other words levels of all frequencies on the communication line will be added and the total level will be displayed. When only a certain signal must be measured, this signal must be filtered out and then measured. This is done by selecting the centre frequency of the signal and the bandwidth the signal operate in. The portion of the frequency spectrum utilised by the signal being measured is the bandwidth of the signal.

$$\text{Bandwidth} = f_{\text{highest}} - f_{\text{lowest}}$$

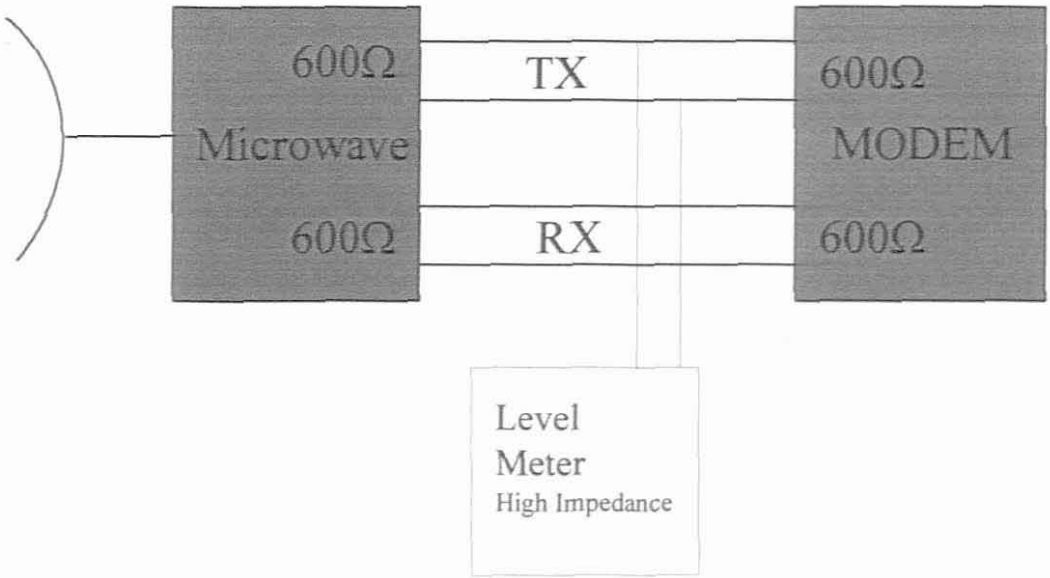
$$\text{Centre Frequency } f_{\text{centre}} = f_{\text{lowest}} + (f_{\text{highest}} - f_{\text{lowest}})/2$$

Impedance Matching

All communication lines have a working characteristic impedance. This may vary from 75Ω up to 600Ω. When the line is connected to other equipment (e.g. a MODEM), the impedance of both must be the same (matched) to have minimum power loss on the circuit. If the impedance on both are the same, it is said to be balanced. Level meters also have an impedance at their input when measuring and will influence the reading. Care must thus be taken when using level meters to select the correct impedance.

Through reading (High Impedance)

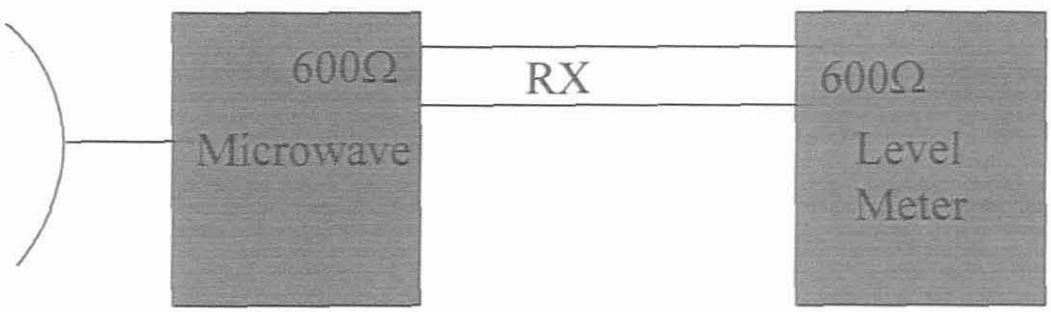
With a through measurement, you are measuring over the line, while it is "live" (Communicating), with nothing connected to the circuit.



When a level meter is used to measure, for example the level on the TX line in the above diagram, the meter must be selected to high impedance. This normally is higher than 12kΩ which, when connected in parallel to the TX, will not influence the impedance of the circuit. When the meter is selected say to 75Ω, the impedance of the circuit will be 75Ωin parallel to 600Ω, which will drastically influence the reading. The meter is calibrated to correct the error introduced with mismatching on the circuit.

Terminated reading

With a terminated measurement, you are measuring power on a circuit that has no other equipment terminated on it.



When the TX level coming from a microwave must be measured and it is not connected to any other equipment, the level meter must also be selected to the same impedance as that of the equipment which would eventually be connected to it. The impedance of the terminated equipment is always matched to that of the bearer equipment in order to effect maximum power transfer.

One last important thing to remember : ***Always calibrate the meter before a measurement is taken***.

The following is thus important when taking power level measurements on communication lines:

- Is the meter calibrated ?
- Is the battery charged ?
- Are we measuring dBm or dBv ?
- Is the Bandwidth selected correctly ?
- Is the Impedance selected correctly ?

3. IDF Background

The IDF (Intermediate Distribution Frame) at a Telecommunication site is the backbone where equipment are physically connected to each other with cables and wires. This makes it easier when changes have to be made later.

When parts of equipment are connected directly to each other by cables, it would be a massive job to make connection changes, because the cables will have to be disconnected and connected again. This can be a massive job if 100 pair (200 wires) cables are involved. The IDF was therefore introduced. The cables are made off separately on the frame and are connected by cross connection wires (jumper wires). In case of a change it will only be is necessarily to change the jumper wires.

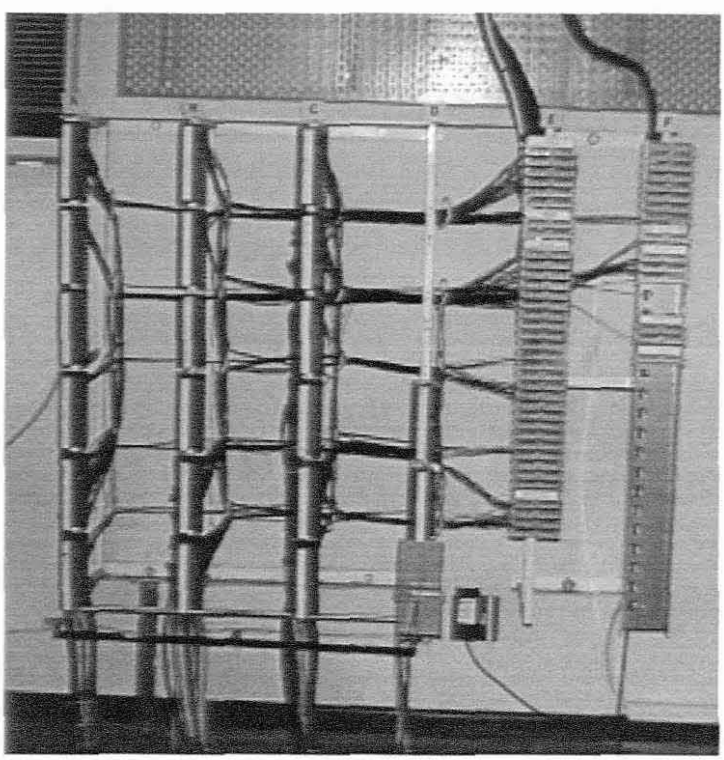


Figure 3.1. IDF with Tagblocks on first 4 verticals and Krone on last 2 verticals

Different connection blocks on the IDF are used:

- Krone 10 pair
- Krone 8 pair
- Poyet 10 Pair
- 6 x 25 tagblocks
- 10 x 20 tagblocks

The Krone and Poyet blocks are "push in" blocks and do not require soldering. A special tool is used to connect the wire to the block. The 6 x 25 and 10 x 20 blocks require the jumper wires to be soldered onto the tags. The Poyet and Krone blocks are faster to wire, but can take only a limited amount of jumper wires (2) per connection.

The IDF makes use of a specific numbering scheme enabling the user to find any point on the IDF quickly and accurately. Without this it will be virtually impossible to install new functions on the IDF or finding old functions quickly.

4. Suggested Solution

As mentioned in the introduction, there is a routine maintenance program to test the communication links on a regular basis. This is however hampered by the following factors:

- Staff shortage

  This due to the problem that ESKOM is not allowed to expand personnel.

- Expansion of the current network

  This is due to new services demanded by internal ESKOM customers

- Refurbishment of old equipment

  Old equipment must be replaced because of age, unavailability of spares and because of new technology that is demanded by customers

To relieve the pressure on the telecommunication personnel, we must look at other means of testing the communication lines automatically.

A solution to the current problem is to feed the TX and RX levels at the substation back to the control centre as an analogue value. This value will be displayed continuously on the screens of the SCADA system. The SCADA system will also continuously log and trend the values in a database. This can then be printed out and a trend can be observed.

If the trending graph shows a deterioration in line quality, the technicians can go out and realign the communication line. This procedure will save on the amount of maintenance tests on the communication lines.

All the RTU's that ESKOM uses have analogue inputs, which are supplied with a current range between -5 and +5mA by a transducer. The scaling is normally as follows:

Example 4.1.:

0 to 5 mA = 0 to 400 kV

Example 4.2.:

- 5 mA to + 5 mA = - 480 to + 480 MVar

Example 4.3.:

0 to 5mA = 0 to 800A

Therefore we can use the analogue inputs of the RTU's to send an analogue value of the power of the FSK signal to the SCADA master. We only have to supply a value that ranges from 0 to 5 mA and is directly proportional to the power of the FSK signal..

This level meter unit must have to the following specifications:

1. Standalone, connected to a RTU and fit into a standard 3U rack.

2. It must measure the RX and TX levels of the RTU and supply the RTU with a analogue value that is directly proportional to power of the incoming level (-20dBm to 0dBm) = 0 to 5mA).

3. Work from a 50V substation supply

5. RMS to DC Conversion Theory

Definition of RMS

RMS or Root Mean Square is a fundamental measurement of the magnitude of an ac signal. Its definition can both be practical and mathematical. Defined practically: the RMS value assigned to an ac signal is the amount of dc required to produce an equivalent amount of heat in the same load. For example: an ac signal of 1 volt RMS will produce the same amount of heat as in a resistor as a 1 volt dc signal. Defined Mathematically: the RMS value of a voltage is defined as:

$$E_{rms} = \sqrt{V_{avg}^2}$$

The above is a simplified formula-equivalent to the standard deviation of a zero average statistical signal. This involves squaring the signal, taking the average, and obtaining the square root. The averaging time must be sufficient long to allow filtering at the lowest frequencies of operation desired.

Methods of True RMS to DC Conversion

Thermal RMS to dc Conversion

Thermal conversion is the simplest method in theory, yet in practice, it is the most difficult and expensive to implement. This method involves comparing the heating value of a unknown ac signal to the heating value of a known calibrated dc reference voltage (see Figure 5.1.). When the calibrated voltage reference is adjusted to null the temperature difference between the reference resistor (R2) and the signal resistor (R1), the power dissipated in these

two matched resistors will be equal. Therefore, by the basic definition of RMS, the value of the dc reference voltage will be equal to the RMS value of the unknown signal voltage.

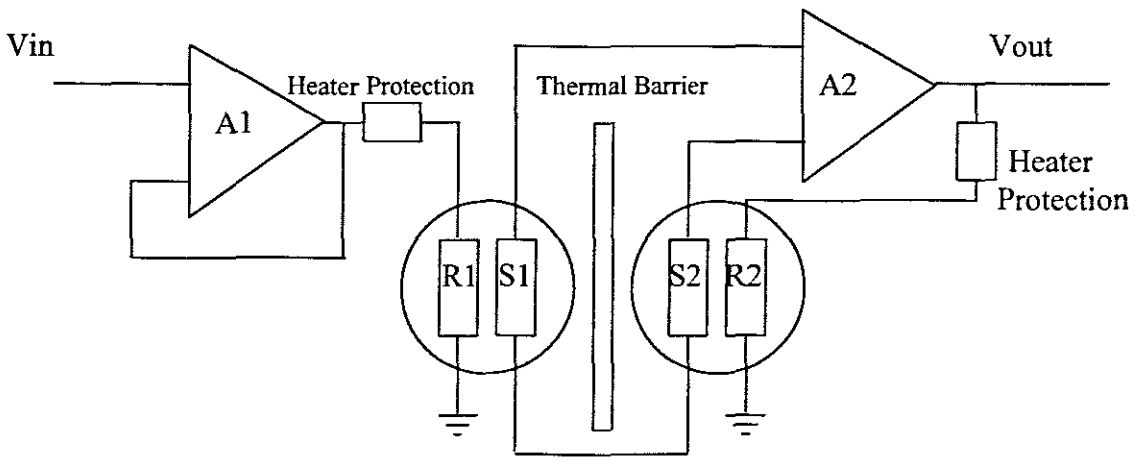


Figure 5.1. A Thermal RMS to dc Converter

Each thermal unit contains a stable, low-TC resistor (R1, R2) which is in contact with an linear temperature to voltage converter (S1, S2), an example of which would be a thermocouple. The output voltage of S1 (S2) varies in proportion to the mean square of Vin, the first order temperature/voltage ratio will vary as K Vin/R1.

The circuit of Figure 5.1 typically has very low error (approximately 0.1%) as well as wide bandwidth. However, the fixed time constant of the thermal unit (R1 S1, R2 S2) limits the low frequencies effectiveness of this RMS computational scheme.

In addition to the basic types discussed, there are also variable gain thermal converters available which can overcome the dynamic range limitations of fixed gain converters at the expense of increased complexity and cost.

Direct or Explicit Computation

The most obvious method of computing RMS value is to perform the functions of squaring, averaging, and square rooting in a straight-forward manner using multipliers and operational amplifiers. The direct or explicit method of computation (Figure 5.2) has a limited dynamic range because the stages following the squarer must try to deal with a signal that varies enormously in amplitude. For example, an input signal that varies over a 100 to 1 dynamic range (10mV to 1V) would have a dynamic range 10 000 to 1 at the output of the squarer (squarer output = 1mV to 10volts).

These practical limitations restrict this methods to inputs which have a maximum of approximately 10 : 1 dynamic range. System error can be as little as ± 0.1% of full scale using a high quality multiplier and square rooter. Excellent bandwidth and high speed can also be achieved using this method.

Indirect or Implicit Computation

A generally better computing scheme uses feedback to perform the square root function implicitly or indirectly at the input of the circuit as shown in Figure 5.3. Divided by the average of the output, the average signal levels now vary linearly (instead of as the square) with the RMS level of the input. This considerably increases the dynamic range of the implicit circuit, as compared to explicit RMS circuits.

Some advantages of implicit RMS computation over other methods are fewer components, greater dynamic range, and generally lower cost. A disadvantage of this method is that it generally has less bandwidth than either thermal or explicit computation. An implicit computing scheme may use direct multiplication and division (by multipliers), or it may use any of several log-antilog circuit techniques.

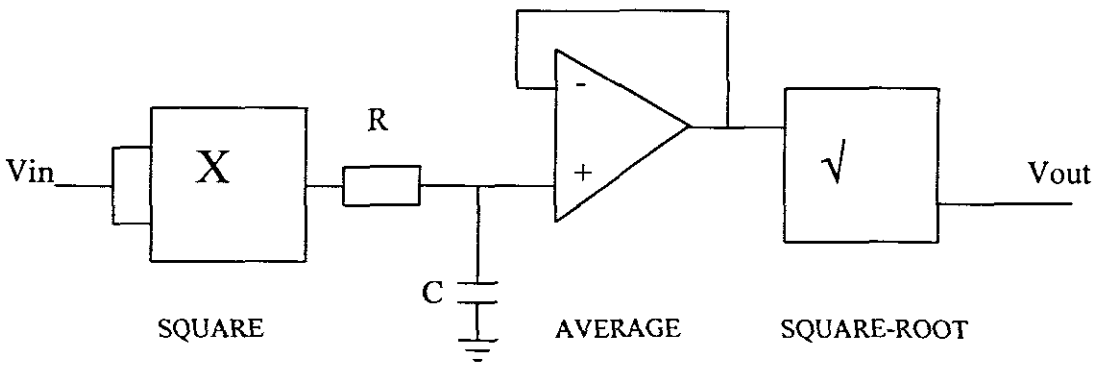


Figure 5.2. The Explicit Computation Method

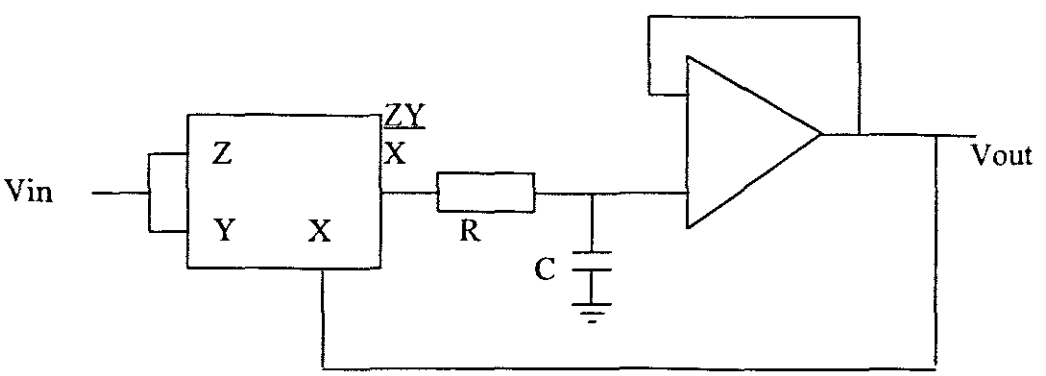


Figure 5.3. The Implicit Computation Method

The RMS to dc converter used in the final design (AD536A) is an example of the implicit computation method.

6. Circuit Description

The final design of the unit consists of the following blocks (see Figure 6.1):

1. Power Supply

2. FSK Analogue input circuit (as in diagram 6.1). This in turn consists of:

   2.1. Isolation Transformer

   2.2. Amplifier.

   2.3. Full wave full wave rectifier (RMS to DC converter)

   2.4. Amplifier

   2.5. Trigger Circuit (Voltage Comparator with TTL output)

3. Analogue to Digital Converter

4. Microprocessor

5. Digital to Analogue Converter

6. Current Source.

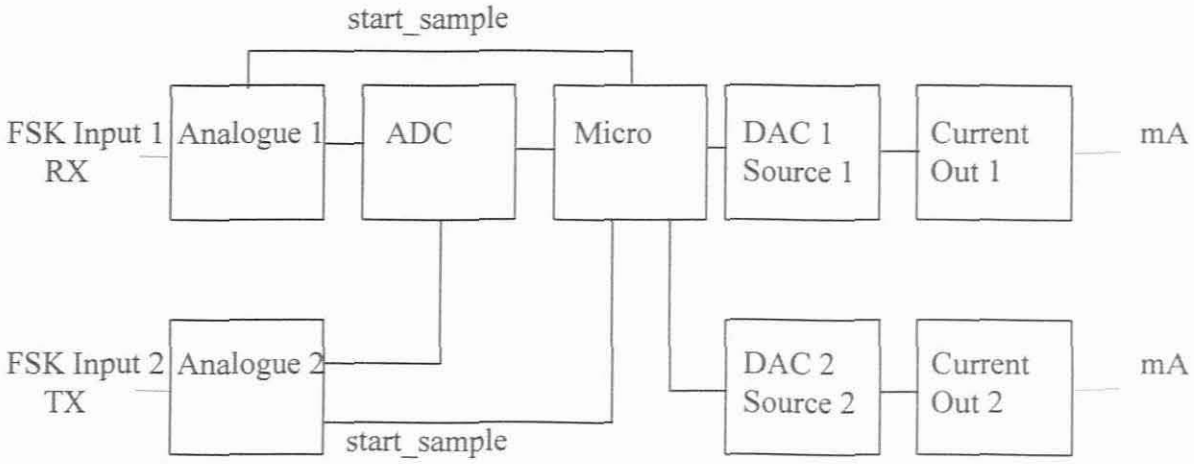


Figure 6.1 Block Diagram Level Meter

The FSK signals are detected by the analogue modules. The FSK signal is amplified, converted to DC and a start_sample signal is generated by the module (Figure 6.3.). The voltage comparator will generate a TTL logic high signal (start_ sample) when the level of the FSK input rise above - 20dBm. The microprocessor will start the sampling of the DC signal through the ADC, the moment the start_sample signal is detected by the microprocessor (Figure 6.1).

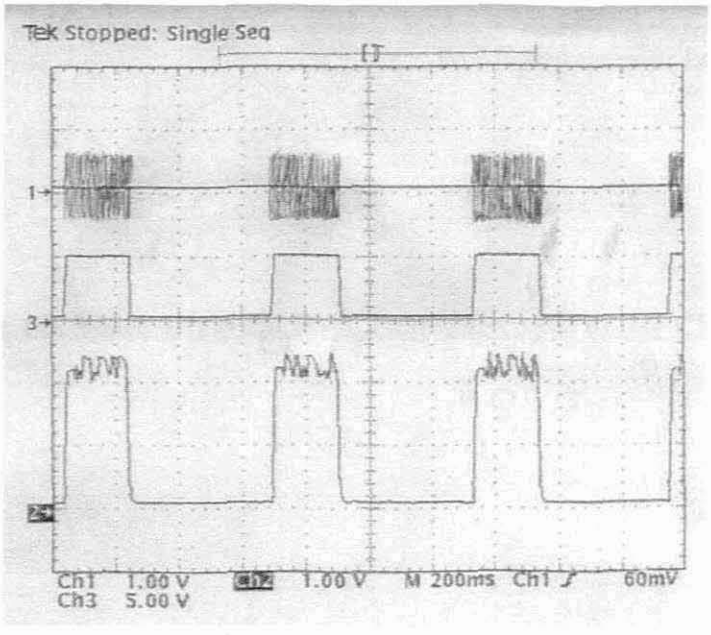


Figure 6.2.

The microprocessor will switch between the two analogue modules (RX and TX inputs). The sampled value will be converted to a linear value and converted to a 8 bit value by the microprocessor. The microprocessor will output this calculated value to the DAC. The DAC will feed a constant current source which will produce a current directly proportional to the voltage input from the DAC.

This current produced by the constant current source will be directly proportional to the power of the FSK signal at the analogue input.

Figure 6.2. shows the relationship between the FSK signal (Channel 1), the rectified signal (Channel 2) and the start_sample pulses (Channel 3).

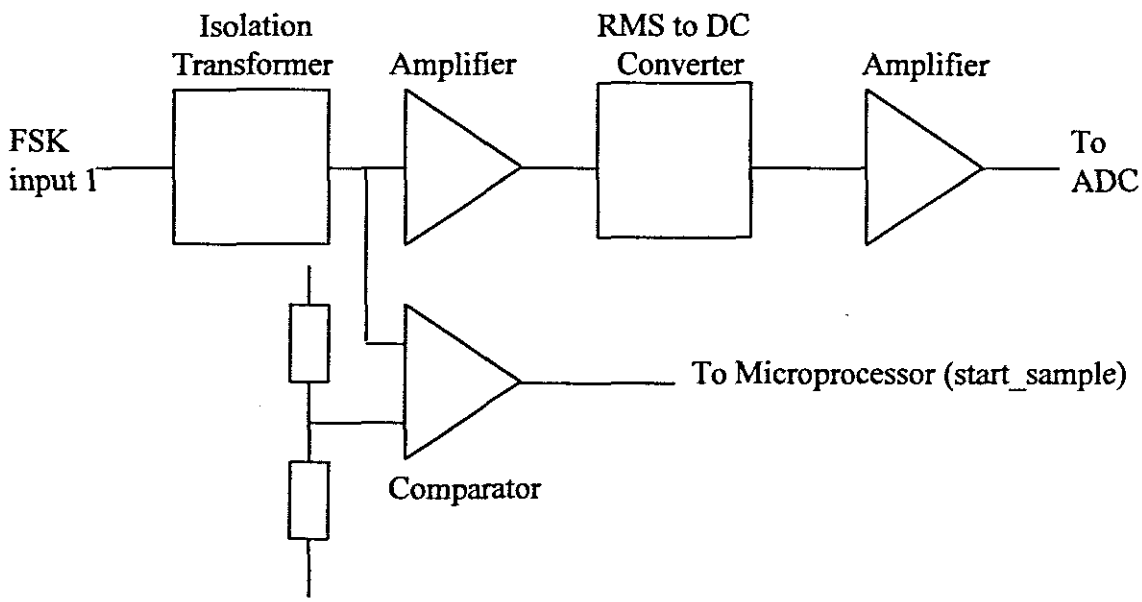


Figure 6.3. Block Diagram FSK Analogue Input of one Channel

Figure 6.4. shows the timing between the FSK signal (Channel 1), the rectified signal (Channel 2) and the start_sample pulse (Channel 3). Note the first part of the rectified signal is constant. The reason for the non-linearity of the rest of the signal is that the RMS to DC converter also reflects the value of the signal when it change over from a logic "1" to a logic "0". The "dips" in the signal is when there is a changeover from one FSK frequency to the other. During the constant part of the signal the MODEM transmits a logic "1" constantly to act as a wakeup (PTT) for the other MODEM. It is during this constant part that the samples are taken by the ADC.

The software is written that the microcontroller will wait 10ms after the start_sample signal goes high and will then take ten samples while the level is constant. The average of the ten samples will then be used for the conversion to get amore accurate and constant value.

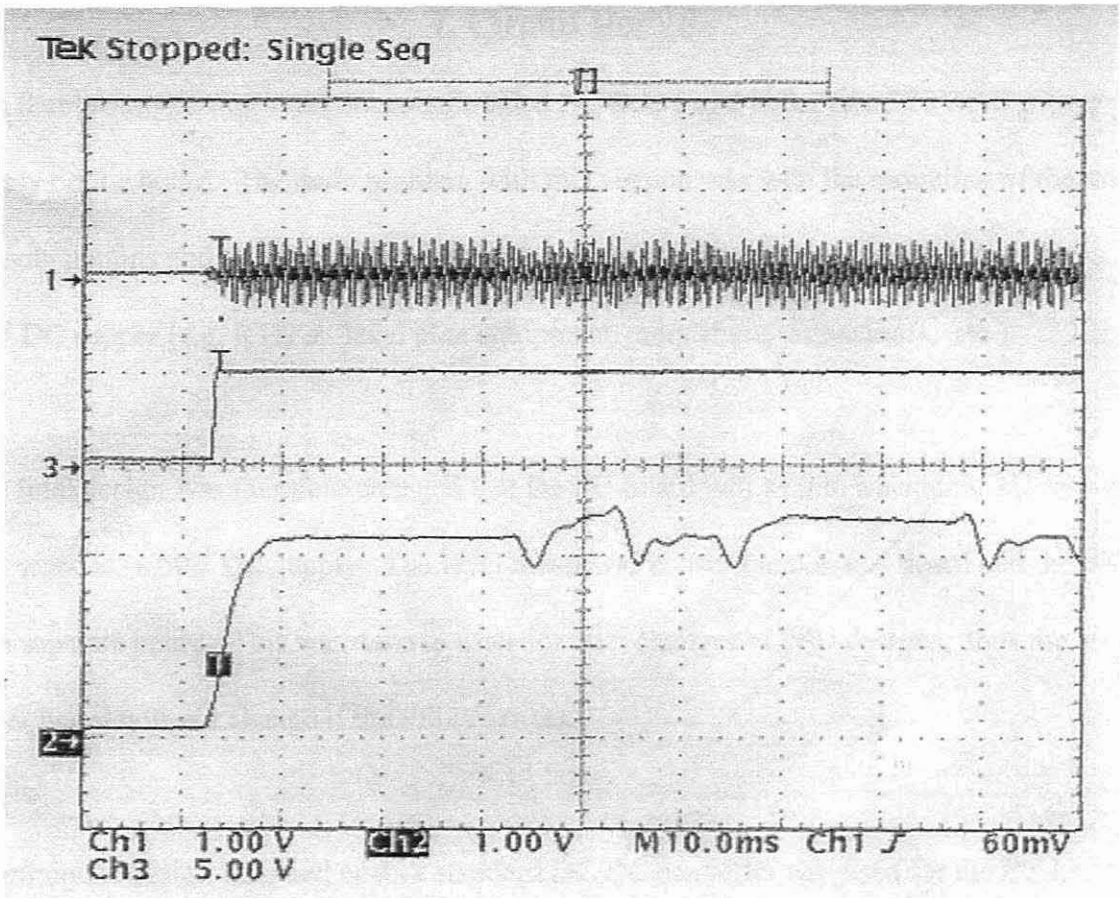

Tek Stopped: Single Seq
1→
3→
Ch1 1.00 V
Ch3 5.00 V
Ch2 1.00 V
M10.0ms Ch1 ƒ 60mV

Figure 6.4.

7. Circuit Design

The first prototype was build on a single sided PC-Board and included a 220V AC power supply on the board. The main problem with this version was with the mounting of the unit in the sub-stations and the availability of AC power. Most telecommunication devices use a 50V DC supply (e.g. RTU's, level plan equipment, amplifiers, attenuators, etc.).

The final design was therefore changed that the PC-board will fit into a standard 3U rack and will work off a 50V DC supply. The level meter was constructed on one board and the PSU on a separate board. This was done to cater for later changes in PSU designs, thus the level meter board will not change if the PSU changes.

To minimise design time and costs a standard DC/DC converter was used for the PSU, instead of designing switchmode PSU from scratch. The design of such a unit is a massive project on its own. The unit used (CALEX 48T5.15UW), takes a 48V DC supply and converts it to 5V and +/_15V DC with the following specifications :

- 5V DC output 800mA
- +15V DC output 150 mA
- -15V DC output 150 mA

FSK Analogue input design (Diagram 7.1).

Note : Only one channel is shown here, because both channels are exactly the same.

The FSK signal is connected to a high impedance isolation transformer with a 1:1 ratio, to decouple the circuit from the signal that has to be measured. A 600Ω resistor is connected to the secondary side of the transformer to provide a 600Ω load to the source. This is done to match the impedance on the communication line, without the loss of power.

The DC offset in the FSK signal is then blocked with a 0.1μF capacitor C1. The signal is then amplified with a LM351 operational amplifier connected as a non-inverting amplifier.

A gain of 100 was chosen

$$\text{Gain} = \frac{R2}{R3} = 100$$

choose R3 = 1kΩ

thus R2 = 100kΩ

A variable resistor is chosen for R2, for calibration later.

The amplified signal is again fed through a DC-blocking capacitor (C2, 0.1μF) and fed to the RMS to DC converter (AD536A). The AD536A is connected in a standard connection as described in Appendix B5. To minimise ripple on the supply rails, two 0.1μF capacitors (C4 and C5) are used to bypass both supplies (+15V and -15V) to ground as near the device as possible. A 0.1μF capacitor was chosen for the filter capacitor (C3).

The output of the AD536 is split to an operational amplifier (LM351) in non-inverting mode, which supplies the analogue to digital converter and a voltage comparater, which supply the micro-controller with the start_sample pulse.

Amplifier design:

A gain of 100 was chosen

$$\text{Gain} = \frac{R4}{R5} = 100$$

choose R4 = 100kΩ

thus R5 = 1kΩ

A variable resistor is chosen for R4, for calibration later.

Voltage Comparater design:

The voltage comparator must supply a start_sample pulse to the micro controller when it detects a signal higher that -20dBm. The LM311 voltage comparator was chosen. The output is open-collector and is taken to +5V with a pull-up 1kΩ resistor (R8).

Resistor ratio:

$$\frac{R7}{R6 + R7} = \frac{x}{5}$$

Were x is the compared voltage.

R7 was chosen as 22kΩ and R6 as 470kΩ.

thus x = 224mV

The output from the AD536 must be adjusted to 224mV (R2) with a -20dBm FSK input.

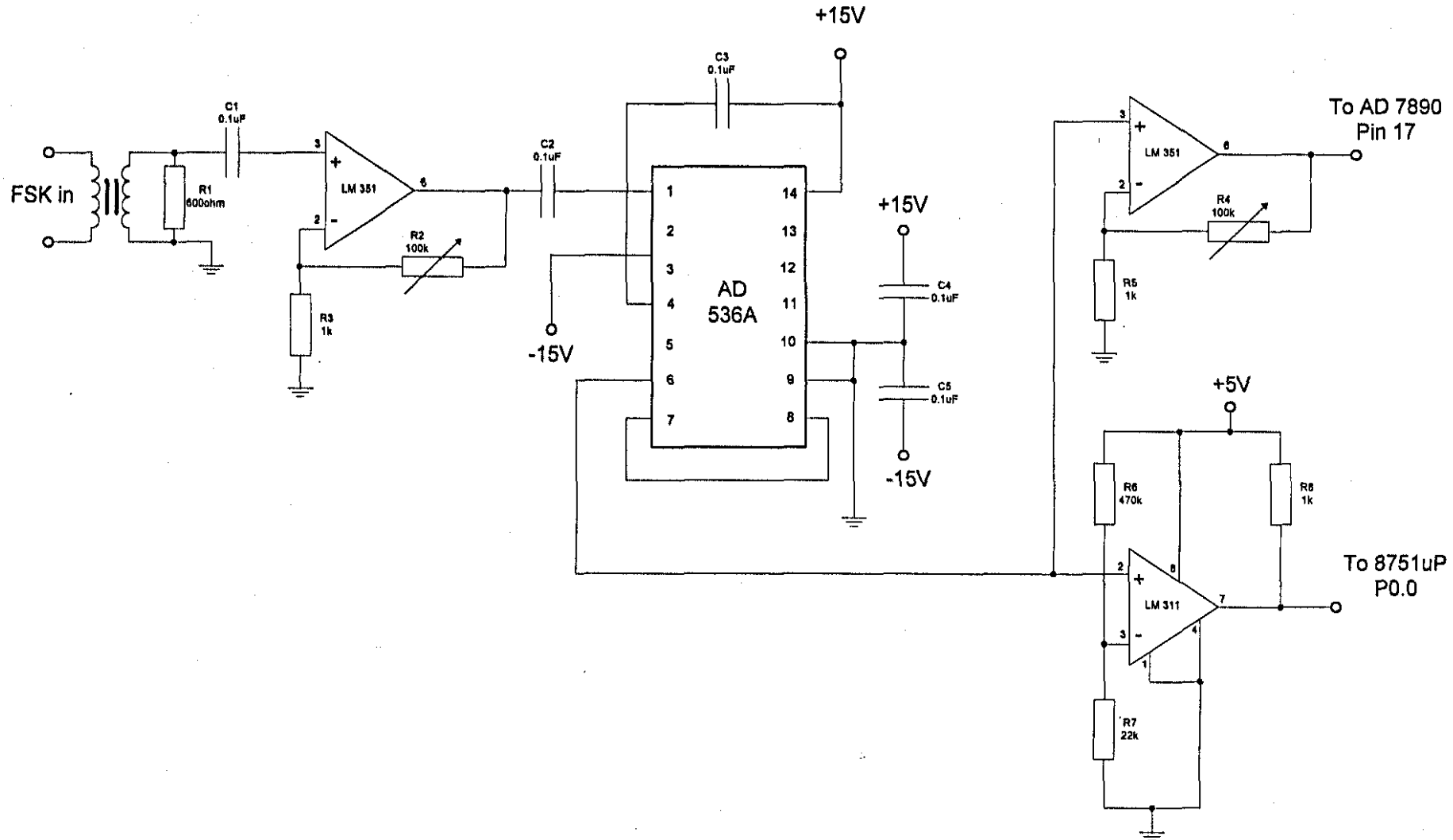


Diagram 7.1. FSK Analogue Input Channel One

ADC and Micro-controller design

The ADC (AD7890) is connected in a standard connection (Diagram 7.2) as described in Appendix B2. The AD7890 is used, because of its fast conversion time (5.9 us), it is a 12 bit ADC with high accuracy and it has eight analogue inputs. Only analogue inputs 1 and 2 were used for the two input signals, but later models can utilise all eight, supplying eight input and output channels for the level meter.

With a bigger model of eight input channels, it is suggested that the analogue inputs be separated from the level meter board and constructed on a separate PC-board. This will make the unit modular and user definable. More than one type of analogue board can be constructed ranging from one to eight inputs available for the user.

The control signals and digital data input / output signals were connected directly to the one port (P1) of the micro-controller.

The micro controller (8751) was chosen, because it has on board RAM and ROM available for the user, which eliminates external ROM and RAM devices, thus simplifying the design and making the PC-board smaller.

The 8751 was connected in a standard connection (Diagram 7.2) as described an Appendix B4. An 4 MHz crystal was used for the oscillator with two capacitors(47 pF) as shown in Figure 6.1 in Appendix B4.

The 8751 controls the ADC and serially reads the data from the ADC. The output ports P2 and P3 are connected directly to the DAC, which in turn supplies the output current to the current source. A calibration switch SW1 is used to calibrate the output of the DAC. When the switch is "on", the 8751 will output logic "1"'s on all the bits of port P2 and P3. This will enable the user to adjust the output of the current source to full scale (5mA), with a full scale input to the DAC.

Port 0 , bit 0 and 1 are used to detect the start_sample signals from the analogue input module and will activate the sampling of the data via the ADC.

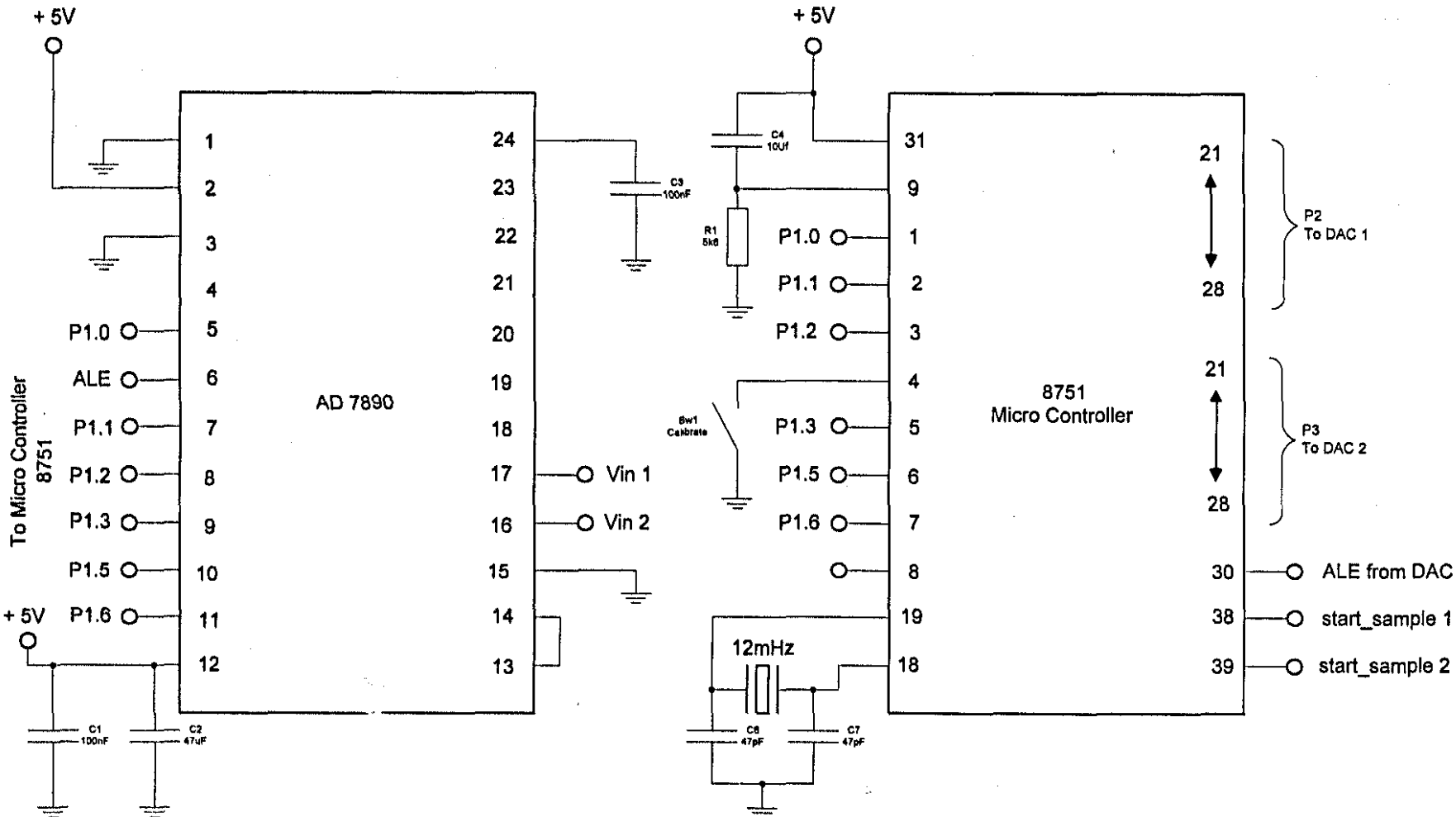


Diagram 7.2. Analogue to digital Converter and Micro Controller

Digital to Analogue Converter and Current Source Design

Note : Only one channel is shown here, because both channels are exactly the same.

The DAC800 was chosen for a DAC because of it's low cost and simple configuration. The DAC is connected to a LM3999 precision voltage reference Zener (Diagram 7.3), to supply a constant reference voltage to the DAC800. The output of the DAC is connected to a LF351 operational amplifier, connected as a current source, of which the output current is proportional to the output of the DAC.

- $+V_{ref}$ = Voltage at Pin 14
- I_{ref} = Current through R2
- R_{ref} = R2
- I_{FS} = Output Current at pin 4
- V_{out} = Output voltage of DAC at pin 4

Voltage Reference Design

The temperature stabiliser pin 3 in connected directly to the 15V supply line and consume typically 12 mA.

Zener forward current = 100μA

Zener voltage = 6.95V

Assume maximum supply current through R1 = 1.5 mA

$$R1 = \frac{15 - 6.95}{0.0015}$$

$$= 5.3k\Omega$$

Choose 4.7kΩ

Thus maximum current = 1.7 mA

Digital to Analogue Converter Design

The DAC800 is connected in a basic positive reference operation connection. (Figure 15 in Appendix B3)

Choose R2 = 3.8kΩ

$$I_{FS} = \frac{V_{ref}}{R2}$$

$$= \frac{6.95}{3800}$$

$$= 1.829mA$$

Choose $V_{out} = 5V$

$$R_{out} = \frac{V_{ref}}{I_{FS}}$$

$$= \frac{5}{0.001829}$$

$$= 2.73k\Omega$$

Choose a 2.2kΩ (R4) resistor in series with a 2kΩ variable resistor(VR1). The variable resistor is then the calibration point for full scale calibration.

Current Source Design

The LM351 operational amplifier is connected as a current source (Diagram 7.3), of which the output current is directly proportional to the input voltage.

Non - Inverting Voltage (MAX.) = 5V

Inverting Voltage (MAX.) = 5V

Iout(max.) = 5mA

$$R_6 = \frac{V-}{I_{out}}$$

$$= \frac{5}{0.005}$$

$$= 1k\Omega$$

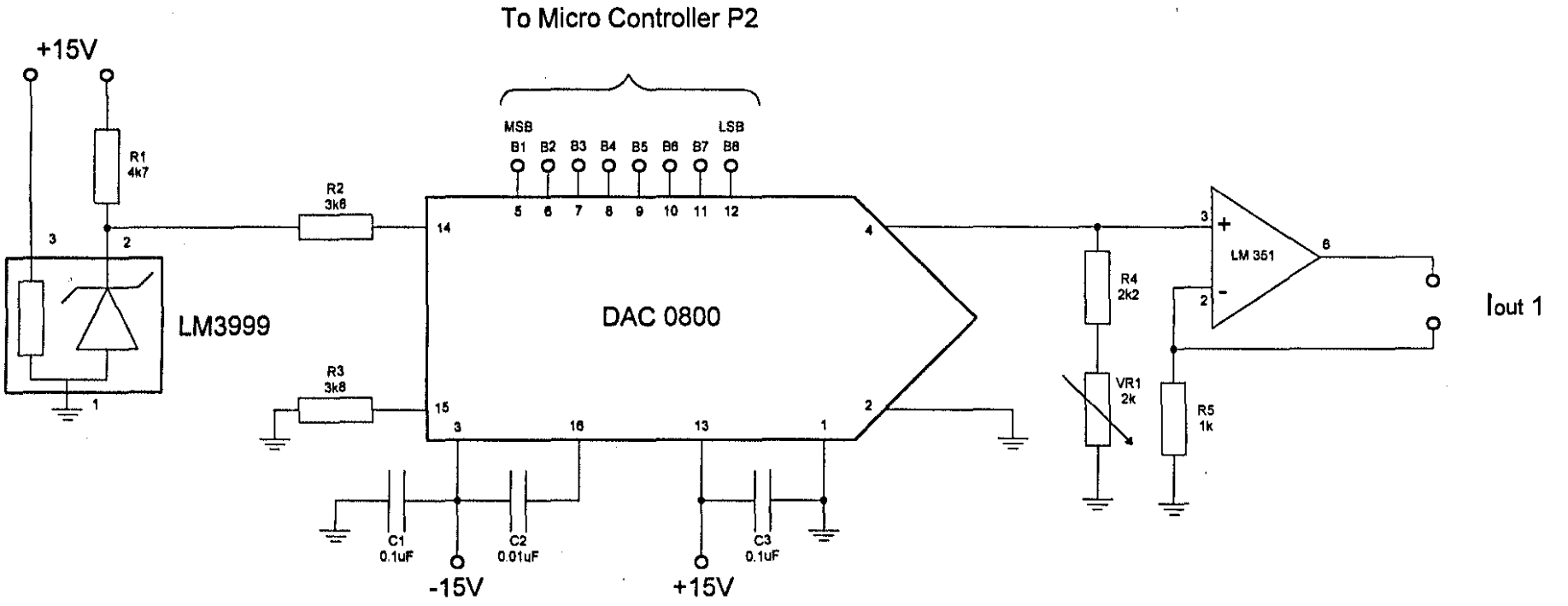


Diagram 7.3. Digital to Analogue Converter and Current Source

Power Supply Design

The initial PSU was a simple 220V AC to +5/+15/-15V DC design.

Standard bridge rectifiers, regulators, capacitors and transformer were used in the design as shown in Diagram 7.4.

As mentioned this design was not used in the final version, because of the 50V DC supply voltage used in ESKOM sub-stations.

A Calex 48T5.15UW DC/DC converter (Figure 7.5) was used in the final design and was mounted on a separate PC-board, acting as the PSU. An on/off switch, fuse and diagnostic LED's were added to the circuit. This unit supplies the main PCB with power, which contains the rest of the circuit.

PSU Design:

Fuse (F1)

$$I = \frac{P}{V}$$

$$= \frac{8.5}{48}$$

$$= 0.177 \text{ A}$$

Chose 150mA

$$\mathbf{R\,1} = \frac{15 - 1.5}{.02}$$

$$= 675\ \Omega$$

$$\mathbf{R\,2} = \frac{15 - 1.5}{.02}$$
$$= 675\ \Omega$$

$$\mathbf{R\,3} = \frac{5 - 1.5}{.02}$$
$$= 175\ \Omega$$

Chose resistor values:

- R 1 = 680 Ω
- R 2 = 680 Ω
- R 3 = 180 Ω

All LED's 3mm RED

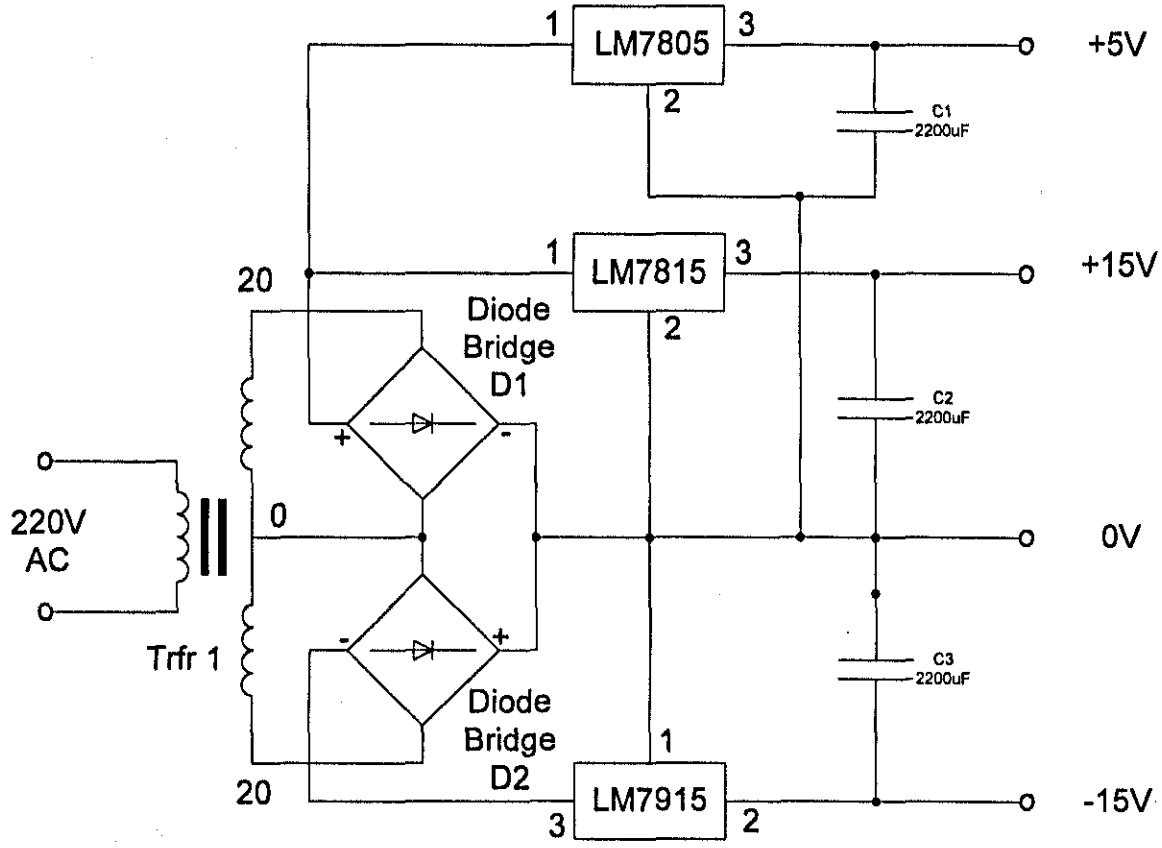


Diagram 7.4. PSU

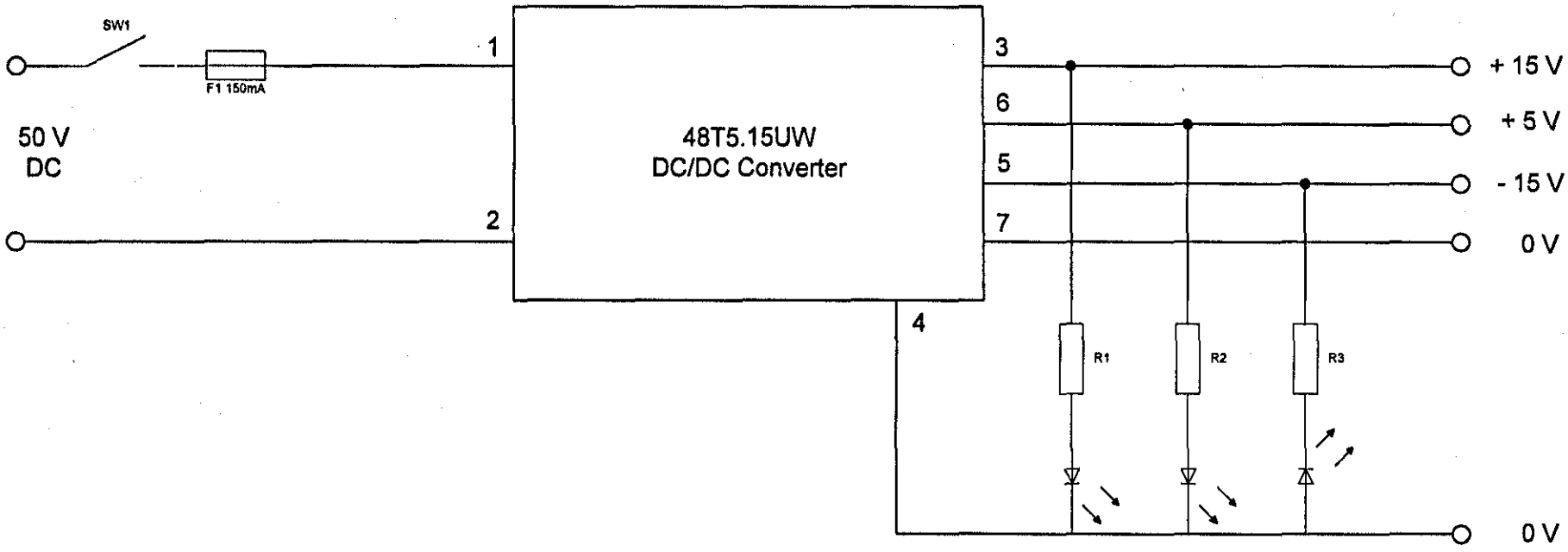


Diagram 7.5. PSU Final Design

8. Calibration and Testing of the Unit

The following calibration must be done on the unit for accurate operation:

1. Calibration of input circuits:

1.1 Switch the unit off.

1.2 Connect a Voltmeter to Test Point 1 (TP1)

1.3. Connect a Signal Generator to FSK input 1

1.4. Select the output of generator to 600Ω terminated and 0dBm power

1.5. Select centre frequency of 3000Hz and bandwidth of 240Hz

1.6. Switch the unit on

1.7 Adjust VR3 that meter reads 1.1V

1.8. Connect voltmeter to Pin 6 U9 and adjust VR4 that meter displays 10V

1.9 Repeat procedure with Input 2, VR1 and VR2

2. Calibration of the output circuits:

2.1. Switch the unit off

2.2 Connect a Ammeter to Output 1 (Full Scale as near as possible to 5mA)

2.3 Switch the unit on

2.4 Switch the calibrate switch on

2.5 Adjust VR6 that meter reads 5mA

2.6 Switch of Calibrate switch

2.7 Repeat procedure with Output 2 and VR5.

3. Testing of unit:

3.1 Use a calibrated MODEM (e.g. -9dBm output) for the test

3.2 Connect a poling signal to input 1 of the unit (from the MODEM)

3.3 Connect a Ammeter to output 2

3.4 Take the reading on the meter and use the following mathematical equation to calculate the dBm reading:

0 to 5mA = -20dBm to 0dBm

Thus

$$\text{dBm output} = \frac{(\text{mA reading} * 20)}{5} - 20$$

Compare dBm output value with the calibrated value of the MODEM. If the two values are the same the circuit is working properly. Repeat with Input 2 and Output 2.

The following results are from calibration tests done on the unit..

Channel 1:

dBm Input From Source	mA output	Calculated dBm Output	% Error
-20	0.015	-19.94	0.3
-18	0.49	-18.04	0.2
-16	0.96	-16.16	1
-14	1.46	-14.16	1.1
-12	1.96	-12.16	1.3
-10	2.47	-10.12	1.2
-8	2.98	-8.08	1
-6	3.48	-6.08	1.3
-4	4.01	-3.96	1
-2	4.5	-2	0
0	5	0	0

Channel 2:

dBm Input From Source	mA output	Calculated dBm Output	% Error
-20	0.02	-19.92	0.4
-18	0.4	-18.4	2.2
-16	0.94	-16.16	1
-14	1.47	-14.12	0.8
-12	1.96	-12.16	1.3
-10	2.49	-10.04	0.4
-8	3	-8	0
-6	3.51	-5.96	0.6
-4	4.02	-3.92	2
-2	4.5	-2	0
0	5	0	0

See also National Calibration Certificate in Appendix A.4

9. Problems encountered and earlier versions

The only difference between the versions was with the analogue input circuit.

Version 1.0.

Basic description:

The input circuit consisted of an active full-wave rectifier and an amplifier as in Diagram 9.1. In order to keep the rise-time of the rectified signal as low as possible, the signal was first rectified and then amplified. An active rectifier was used because the voltage drop over the diodes in a diode bridge (±1.4V) is higher than the input signal (220mV).

Problems encountered:

The circuit proved to be very accurate with constant level signals, but unusable with polling signals. The duration of a poll is 260ms and the rise time of the rectified signal was 1sec with a 1.8% ripple (4mV with a 220mV peak to peak signal).

With a low rise time of 10ms, the ripple on the rectified signal was unacceptably high at 18% (40mV with a 220mV peak to peak signal).

Practical Results:

The different ripple/rise-time values are displayed in Table 9.1.

Capacitor C3 (μf)	Ripple (mV)	Input Signal (Vpp)	Rise Time (ms)
10	4	220	1000
4.7	5	220	300
1	7	220	100
0.68	8	220	60
0.47	11	220	50
0.1	40	220	10

Table 9.1.

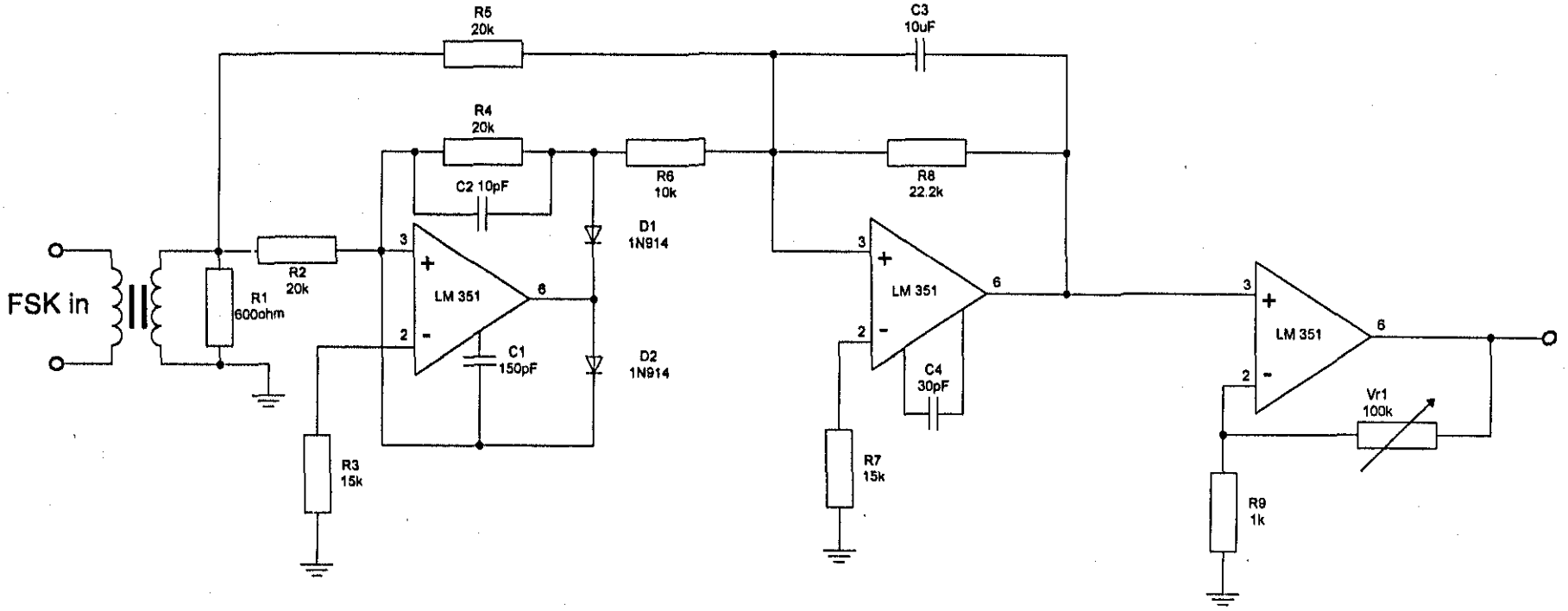


Diagram 9.1.: Version 1

Version 2.0.

Basic description:

The active full-wave rectifier was changed to a peak detector and an amplifier as in Diagram 9.2.

An 4.7 μf capacitor with a 180kΩ resistor was connected to the output to get a smoother rectified signal. The resistor was used to discharge the capacitor.

Problems encountered:

The rise-time of the rectified signal was acceptable at 4mV, but the percentage ripple was 15.

The other big problem was that the capacitor did not discharge to 0 V between polls. The voltage only dropped down to 1V (Figure 9.1.), which was too high.

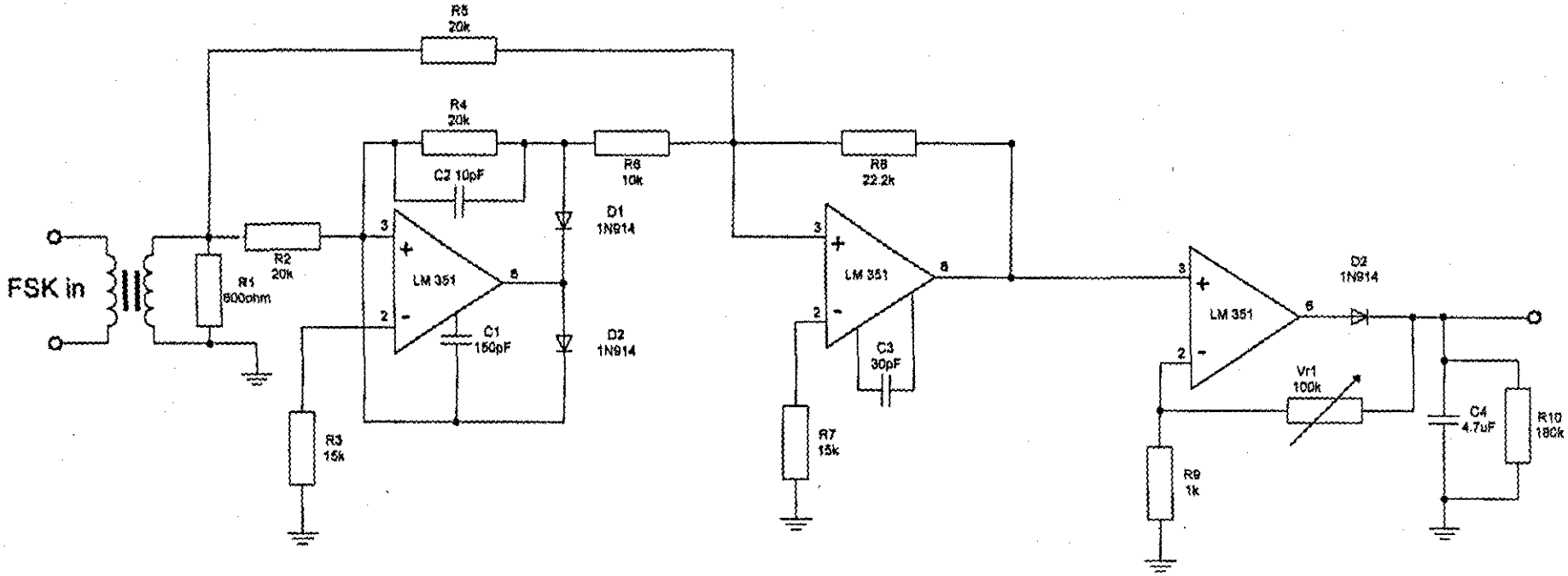


Diagram 9.2.: Version 2

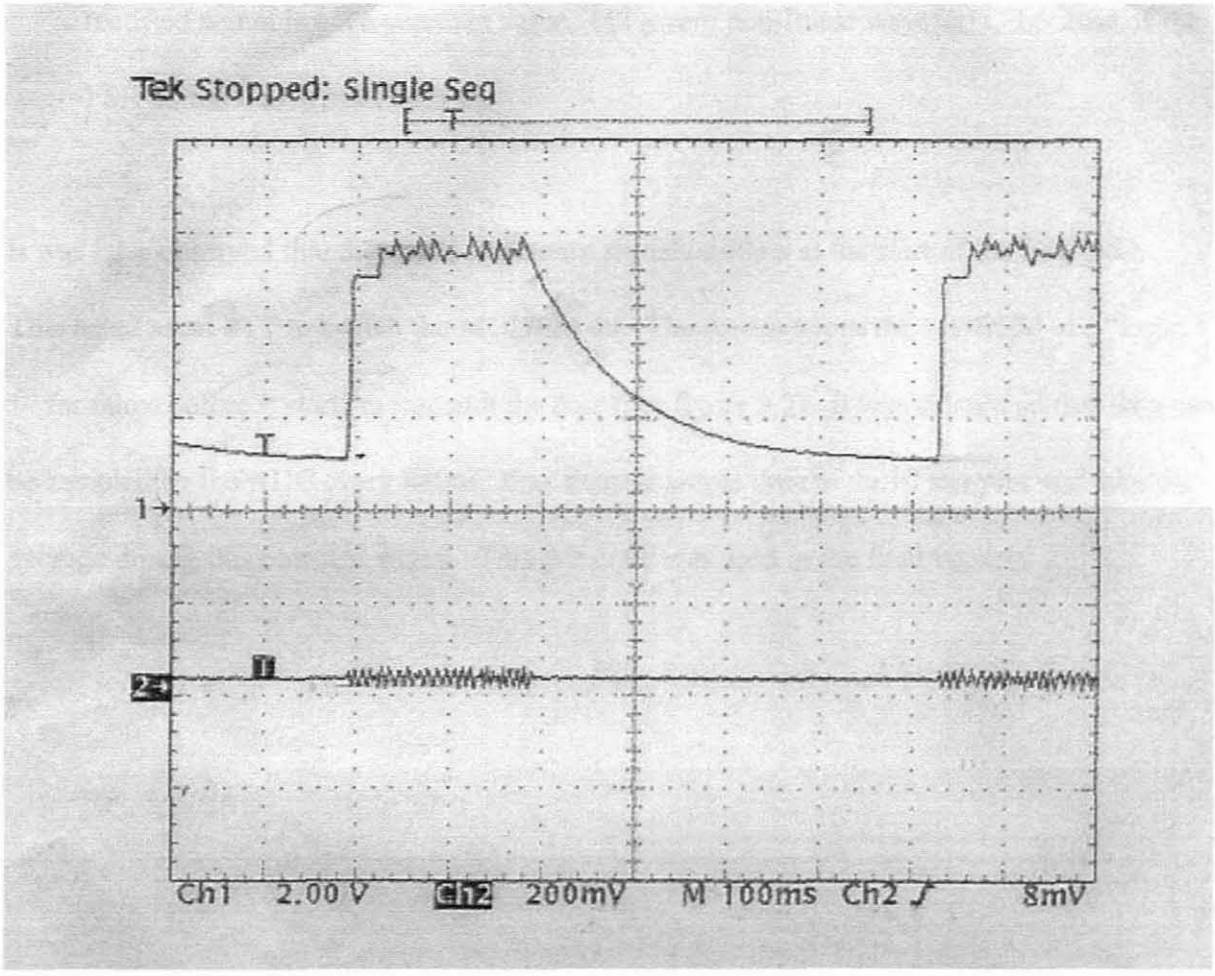


Figure 9.1

The waveform of the FSK data bursts is captured on channel 2 and the rectified signal on channel 1.

Another big problem was that the samples from the ADC were not constant. It depends on when during the poll it was sampled. The output of the DAC and constant current source varied between 3.7 mA and 5 mA with a full scale input of 0dBm. The result should have been a constant 5mA output. The reason for this behaviour is that the

rectified signal is not a constant value, but a very non-linear waveform, because of the FSK signal that is peak detected.

It was later observed that there was a constant signal of 60ms at the start of the FSK poll. This acted as an PTT to switch the MODEM on. The master keeps the MODEM at a "logic 1" for 60ms before it starts to transmit the data (see figure 9.2). It was calculated that data can be sampled by the ADC every 880ns, thus there is ample time to do 10 samples and take the average during this constant signal. This principle was used in the final version.

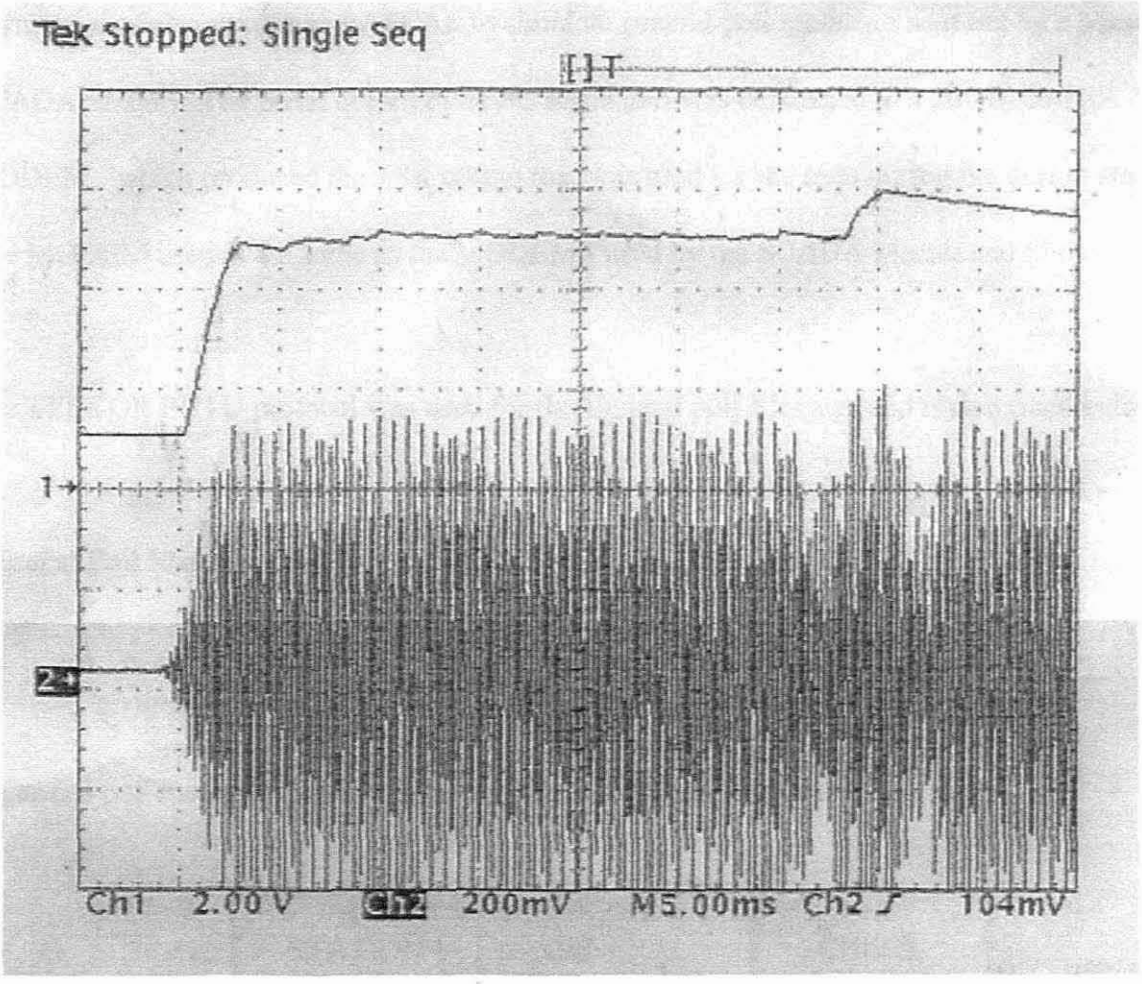


Figure 9.2.

10. Software

The software for the 8751 microcontroller was written in C and compiled to 8751 assembly language. The reason for this is that C supply us with excellent mathematical functions, which would be cumbersome in assembly language directly.

Software was written for single channel and double channel sampling. The reason for single channel was more for testing purposes. It was difficult to simulate two FSK data channels with the initial versions. The reason for this is that two MODEMS must be used and the timing between the two signals must be correct.

Software was also written in PASCAL to simulate general poll massages sent out by a Master SCADA Station. The serial output of an PC serial port was connected to a 200 Baud FSK MODEM, which produced the FSK output that was used for the tests during the design stage. The MODEM used is the same as the MODEMS used by the SCADA Master and Slaves.

The TELKOR PUTU protocol was used for the General poll Message and is described below:

General Poll Message

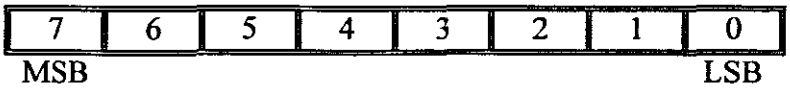
A general poll message consists of three bytes and looks as follows:

Byte 1 STATION ADDRESS	Byte 2 GENERAL MESSAGE	Byte 3 CHECK SUM

10.1. The first byte consists of the station address.

Example: 2E (Hex) = RTU 46 (Decimal)

10.2. The second byte defines the general poll number as well as the type of poll, a general poll discard or a general poll retransmit. Bit 7 (MSB) of the 8 bits shows if it is a general poll re-transmit or a general poll discard. Bit 0 and 1 shows which number general poll it is.



10.2.1. Bit 7:

Binary Value	Meaning
1	General Poll re-transmit
0	General Poll discard

10.2.2. Bit 0 and 1

	HEX	Binary	General Poll number
1	0	00	GP0
2	1	01	GP1
3	2	10	GP2
4	3	11	GP3

Where :

GP0 = Request priority 0 information only

GP0 = Request priority 0 and 1 information

GP0 = Request priority 0, 1 and 2 information

GP0 = Request information on all priorities

Examples:

Data : 2E 03 2D

03 = 0000 0011

Thus it is a general poll number 3 discard

Data : 2E 83 2D

83 = 1000 0011

Thus it is a general poll number 3 re-transmit

10.2.3. The last byte is the checksum of the message and is the XOR value of the first two bytes.

Source Code for General Poll Message.

```
Program RS232;

USES
  DOS,CRT;


Var
  COM      : Word;       (* RS 232 Comms Port *)
  Mesbyte  : Byte;       (* Number of Bytes in TX Message *)
  Check    : Byte;       (* PUTU Message Checksum *)
  PutuAddr : Byte;       (* PUTU Address *)
  Genpole  : Array [1..3] of Byte; (*General Pole Message*)
  ClockStart : Longint;

(*************************************************************************)

Procedure init8250;          (* Initialize RS232 Port *)

  (*       Putu RS232 Communication        *)
  (*                                       *)
  (* Baud-rate  = 200                      *)
  (* Data Bits  =  8                       *)
  (* Start Bits =  1                       *)
  (* Stop Bits  =  1                       *)
  (* Parity     = Odd                      *)
  (* Baud Rate Devisor = 115200 / Baud-rate *)

Begin

  PORT[COM+3] := $80;        (* Initialize Baud-rate devisor *)
  PORT[COM] := $40;          (* Output LSB Baud-rate devisor *)
  PORT[COM+1] := $02;        (* Output MSB Baud-rate devisor *)
  PORT[COM+3] := $0B;        (* Set up Line Control Register *)
  PORT[COM+4] := $0B;        (* Set up Modem Control Reg     *)
  PORT[COM+1] := $01;        (* Set up Interrupt-enable Reg  *)

End;

(*************************************************************************)

Function GettimeVal : Longint;

Var
  Hour, Minute, Second, Sec100 : Word;
  Time : Longint;
```

```
Begin
  Gettime(Hour,Minute,Second,Sec100);
  Time := ((Hour * 360000) + (Minute * 6000) + (Second * 100) + (Sec100));
  GettimeVal := Time;
End;

(*************************************************************************)

Procedure Startclock;              (* Get Time *)

Begin
  Clockstart := Gettimeval;
End;

(*************************************************************************)

Procedure Senddata(Mesbyte : integer);     (* Send Data To Comms Port *)
 Var
   n : Integer;

Begin
   For n := 1 to Mesbyte do
   Begin
    While ((Port[COM+5] AND $20) = 0) DO    (* Check Line Status Register *)
    begin
    end;
    PORT [COM] := MESSAGE[n];
   End;
End;

(*************************************************************************)

Procedure Genpolpr;            (* General Pole Procedure *)

Var
  i : integer;
Begin

  Check := Putuaddr XOR $03;              (* Checksum *)
  Genpole[1] := Putuaddr;                (* Address Byte *)
  Genpole[2] := $03;                    (* General Pole Byte *)
  Genpole[3] := Check;                   (* Checksum Byte *)
  Mesbyte := 3;                         (* Message Length *)
  Move (Genpole,Message,3);
  Senddata(3);

End;
```

```
(*****************************************************************************)

Begin                    (* Begin Main Program *)
   Com := $3F8;
   Init8250;
   Putuaddr:= $1;


End.
```

Source Code for single channel sampling:

```
#pragma code debug objectextend small
#include <reg51.h>                    /* define 8051 registers */
#include <math.h>

bit do_sample;
sbit CONVST = 0x90;
sbit SCLK = 0x91;
sbit TFS = 0x92;
sbit CAL_SWITCH = 0x93;
sbit RFS = 0x94;
sbit DATA_OUT = 0x95;
sbit DATA_IN = 0x96;
sbit START_SAMPLE = 0x97;
#define DAC1 P2


void set_channel(unsigned char channel) {
bit adr_bit;
int I;

 TFS = 1;
 SCLK = 1;
 TFS = 0;
 channel = (channel << 3) & 0x38;
 for(I = 0;I <= 5;I++) {
  SCLK = 1;
  if ((channel >> (5 - I) & 1) == 1) adr_bit = 1;
  else adr_bit = 0;
  DATA_IN = adr_bit;
  SCLK = 0;
 }
 SCLK = 1;
 TFS = 1;
}


int get_sample(unsigned char channel) {
int I;
int data_in;
unsigned char data_in_A;
unsigned char data_in_B;

 set_channel(channel);
 CONVST = 1;
 RFS = 1;
 SCLK = 1;
```

```
  CONVST = 0;
  DATA_OUT = 1;
  CONVST = 1;
  data_in = 0;
  data_in_A = 0;
  data_in_B = 0;

  for(I = 0;I <= 2;I++);
  RFS = 0;
  for(I = 0;I <= 3;I++) {
    SCLK = 1;
    SCLK = 0;
  }
  for(I = 0;I <= 3;I++) {
    SCLK = 1;
    SCLK = 0;
    if (DATA_OUT) {
      data_in_A = data_in_A | (1 << (3 - I));
    }
  }
  for(I = 0;I <= 7;I++) {
    SCLK = 1;
    SCLK = 0;
    if (DATA_OUT) {
      data_in_B = data_in_B | (1 << (7 - I));
    }
  }
  RFS = 1;
  SCLK = 1;
  data_in = ((int)((int)data_in_A * (int)256) + (int)data_in_B);

  return(data_in);
}

long total_sample;
int i;
float volt;
float dBm;
unsigned char ma_out;

void delay (int n){

      int i;
      for (i = 0; i<= n; i++)
        {
        }
}
```

```
main () {                /* main program */

 while(1) {
  if(CAL_SWITCH) {
   DAC1 = 0xFF;
  }
  else {
     while (!do_sample){          /* check for trigger pulse */
       while (START_SAMPLE);      /* must be 10ms long */
       while (!START_SAMPLE);
          delay (500);            /* 10ms delay */
       if (START_SAMPLE) do_sample = 1;
       else do_sample = 0;
       }
     total_sample = 0;
     for (i = 0; i < 10 ; i++){
          total_sample += get_sample(1);
          }
     }

   volt = (((float)total_sample/10.0) / 2048.0) * 10.0;
   dbm = 20.0 * log10(98.9e-3 * volt);
   ma_out = (unsigned char)(((20 + dbm) / 20) * 256.0);
   DAC1 = ma_out;
   do_sample = 0;

 }
}
```

Source Code for double channel sampling:

```
#pragma code debug objectextend small
#include <reg51.h>                    /* define 8051 registers */
#include <math.h>

sbit CONVST = 0x90;
sbit SCLK = 0x91;
sbit TFS = 0x92;
sbit CAL_SWITCH = 0x94;
sbit RFS = 0x93;
sbit DATA_OUT = 0x95;
sbit DATA_IN = 0x96;
sbit START_SAMPLE = 0x97;
sbit START0 = 0x80;
sbit START1 = 0x81;
#define DAC1 P2
#define DAC2 P3


void set_channel(unsigned char channel) {
bit adr_bit;
int I;

 TFS = 1;
 SCLK = 1;
 TFS = 0;
 channel = (channel << 3) & 0x38;
 for(I = 0;I <= 5;I++) {
  SCLK = 1;
  if ((channel >> (5 - I) & 1) == 1) adr_bit = 1;
  else adr_bit = 0;
  DATA_IN = adr_bit;
  SCLK = 0;
 }
 SCLK = 1;
 TFS = 1;
}


int get_sample(unsigned char channel) {
int I;
int data_in;
unsigned char data_in_A;
unsigned char data_in_B;

 set_channel(channel);
 CONVST = 1;
```

```
  RFS = 1;
  SCLK = 1;
  CONVST = 0;
  DATA_OUT = 1;
  CONVST = 1;
  data_in = 0;
  data_in_A = 0;
  data_in_B = 0;

  for(I = 0;I <= 2;I++);
  RFS = 0;
  for(I = 0;I <= 3;I++) {
   SCLK = 1;
   SCLK = 0;
  }
  for(I = 0;I <= 3;I++) {
   SCLK = 1;
   SCLK = 0;
   if (DATA_OUT) {
    data_in_A = data_in_A | (1 << (3 - I));
   }
  }
  for(I = 0;I <= 7;I++) {
   SCLK = 1;
   SCLK = 0;
   if (DATA_OUT) {
    data_in_B = data_in_B | (1 << (7 - I));
   }
  }
  RFS = 1;
  SCLK = 1;
  data_in = ((int)((int)data_in_A * (int)256) + (int)data_in_B);

  return(data_in);
}


void delay (int timeout){

      int i;
      for (i = 0; i<= timeout; i++)
        {
        }
}



bit wait_trigger(unsigned char channel, int timeout)
```

```
{
bit saved_state;
int ms5;

 ms5 = 0;
 switch(channel)
 {
  case 0x00:
   saved_state = START0;
   while(1)
   {
    if ((START0 != saved_state) && (saved_state == 0))  /* 0 to 1 trans */
    {
     delay(500);        /* wait 10 ms */
     if (START0)        /* still high ? */
     {
      return(1);
     }
    }
    else
    {
     saved_state = START0;
     delay(250);       /* wait 5 ms */
     ms5++;
     if (ms5 > timeout)
     {
      return(0);
     }
    }
   }
   break;
  case 0x01:
   saved_state = START1;
   while(1)
   {
    if ((START1 != saved_state) && (saved_state == 0))  /* 0 to 1 trans */
    {
     delay(500);        /* wait 10 ms */
     if (START1)        /* still high ? */
     {
      return(1);
     }
    }
    else
    {
     saved_state = START1;
     delay(250);       /* wait 5 ms */
     ms5++;
```

```
        if (ms5 > timeout)
        {
         return(0);
        }
       }
      }
      break;
  }
}

void do_conversion(unsigned char channel)
{
long total_sample;
int i;
float volt, dbm;
unsigned char ma_out;

 total_sample = 0;
 for (i = 0; i < 10; i++)              /* acquire 10 samples */
 {
  total_sample += get_sample(channel);
 }
 volt = (((float)total_sample/10.0) / 2048) * 10;
 dbm = 20.0 * log10(98.9e-3 * volt);
 ma_out = (unsigned char)(((20 + dbm) / 20) * 256.0);
 switch (channel)
 {
  case 0x00:
    DAC1 = ma_out;
    break;
  case 0x01:
    DAC2 = ma_out;
    break;
 }
}

main ()
{
  while(1)
 {
     if (CAL_SWITCH)
  {
  DAC1 = 0xff;
  DAC2 = 0xff;
  }
      else
      {
      if (wait_trigger(1, 2000))       /* timeout in 5ms intervals */
```

```
        {
        do_conversion(1);
        }
        if (wait_trigger(0, 2000))
        {
        do_conversion(0);
        }
    }
  }
}
```

11. Synthesis and recommendations

The final version of the level meter proved to work perfectly, despite initial setbacks. The unit is a valuable instrument with high accuracy.

Further enhancements to the unit will be to add the following to it. These additions will change it into a micro RTU.

- Dial-up MODEM
- Alarm Inputs
- Control Outputs

The MODEM will enable personnel to dial in to a site and do remote diagnostics. This will be useful when the RTU at the site is not responding to the master station. The following remote diagnostics will be available:

- RX and TX levels
- Alarm condition of the RTU power supply
- Remote control to reset the RTU, in case of a crash

With the above changes it must be stressed that a suitable communication protocol must be designed. Examples of messages from the master to the micro RTU will be:

- Update TX and RX levels

- Update alarm condition
- Sent remote control
- Test

Each message will have to get a unique structure and the structure will have to be of such a nature that it will not limit later enhancements or changes to the micro-RTU. It must be stressed that a communication protocol must be as simple as possible. This normally called the KISS (Keep It Straight and Simple) principle. The shorter the transmit message, the shorter the "air" time will be. This will cause less errors, and a higher availability of the system.

Possible applications will be to market the unit as a low cost hand-held level meter for technicians. Portable level meters (e.g. W&G SPM31) are bulky and heavy and normally not all the functionality is used by technicians. Although they are excellent test equipment and very accurate, they are also very high in price.

One possible problem with the unit is that it is a wide band meter, thus it measure the full frequency spectrum on the communication line. In some cases it will be necessary to do selective measurement, thus a certain frequency range needs to be measured. In this case a range of band-pass filters will have to be fitted to the unit.

The unit can also be made more intelligent, i.e. it can be fitted with a MODEM that will decode messages of the RX and TX lines, looking for data corruption. The problem here will

be that different makes of RTU's use different message protocols. Different units will have to be designed for each type of RTU, which will make it non standard.

The price of the power supply used in the project is however very high (±R600) and in order to produce a low cost module, a low cost DC/DC converter must be designed. This can be done with the proposed further enhancements.

A low cost DC/DC converter should bring the total price down to such a level that it will prove to be cost-effective to install the unit in all sub-stations equipped with RTU's. The unit will prove it's worth as a vital diagnostics tool, when it is changed to the proposed micro-RTU.

Appendix A

A.1. Installation Procedure

A.2 Glossary of Terms

A.3 Bibliography

A.4. Test Equipment used

A.5. Calibration Certificates

A.1. Installation Procedure

The level meter must be connected to a communication line without interfering with the communication between the RTU and the communication equipment.

The way to do this is to introduce splitters in the RX and TX lines. An splitter take one 600Ω signal and split this into four 600 Ω signals with the same power. The reason for this is that you can connect more than one 600 Ω terminated device onto a 600 Ω terminated communication line without changing the impedance and power on the communication line.

The connections between the communication equipment, splitters, RTU and level meter is shown in Diagram 12.1.

The level meter consists of two 3U cards that are fitted into a 3U rack that is connected with cables to the local IDF at the sub-station. These cables are connected to the backplane of the 3U rack. An short 4-wire cable connects the PSU board and the micro-controller board on the front panels of the two cards. This is used to supply the power to the micro-controller card. The 50V supply voltage for the PSU card is on the backplane of the 3U rack.

Normally the splitters are also housed in the 3U rack and connected to the IDF via cables from the backplane of the 3U rack. The communication equipment and RTU are also connected with cables to the IDF. The wire connections between the communication equipment, splitters, RTU and level meter are made with jumper wires on the IDF as in diagram 12.1.

After the jumper connections are made, the levels on all the equipment must be checked with a portable level meter (e.g. SPM31), to verify that the connections were made correctly.

The RTU must now be programmed to accept the two new analogue inputs and the SCADA master must be programmed to accept two new analogue values with the scaling factor of 0 to 5mA = -20dBm to 0dBm.

If the level meter was calibrated correctly before installation and the programming was done correctly the unit should work.

Fault finding:

If the unit is not working check the following:

12.1. Check if the unit is switched on

12.2 Measure for the 50V supply voltage

If it is absent, check the 50V cable connection between the backplane and 50V DC supply from the batteries.

12.3. Measure for the +5V, -15V and +15V supplies

If it is absent, check the fuse on the PSU card and the cable connection between the PSU card and the micro-controller card.

12.4. Measure if the TX and RX signals at the level meter

If this is absent or the incorrect level, check all jumper wire connections on the IDF and all cable connections between equipment and IDF

12.5. Measure if there is an current output at the analogue outputs of the level meter.

If the FSK input level at the level meter and the supply voltages are right, but the analogue outputs are absent, the unit is faulty.

If the analogue outputs to the RTU are present and the correct value, the problem is either with the RTU or the SCADA master.

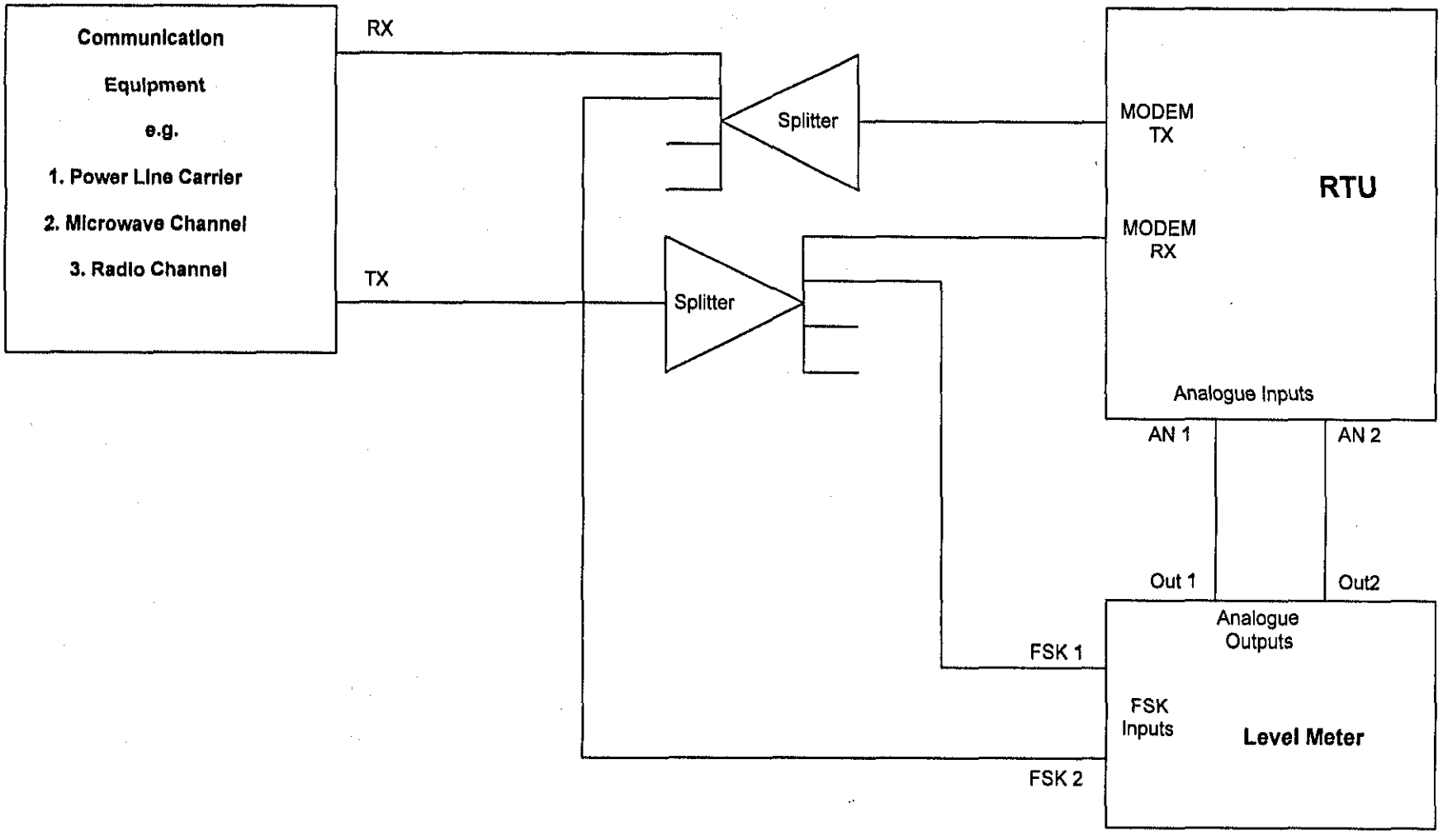


Diagram 12.1. Level Meter Connection to Communication Equipment

A.2 Glossary of Terms

Abbreviation	Meaning
AC	Alternating Current
ADC	Analogue to Digital Converter
DAC	Digital to Analogue Converter
DC	Direct Current
FDM	Frequency division multiplexing
FSK	Frequency Shift Key
I/O Port	Input / Output Port
kV	Kilo Volts
mA	Mili Ampere
MODEM	Modulator Demodulator
Mvar	Mega Var.
MW	Mega watt
PC	Personnel Computer
PSU	Power Supply Unit
RAM	Random Access Memory
ROM	Read Only Memory
RTU	Remote Terminal Unit
RX	Receive
SCADA	Supervisory, Control and Data acquisition
TDM	Time division multiplexing
TX	Transmit

A.3. Bibliography

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Analogue Devices data sheets. Analogue Devices. Norwood. U.S.A.

A.4. Test Equipment used

Equipment	Make	Serial Number	Specifications
Oscilloscope	Tektronix TDS 420	B012122	See calibration setificate
Oscilloscope probe 1 Oscilloscope probe 2 Oscilloscope probe 3 Oscilloscope probe 4	P6138 P6138 P6138 P6138	None	350MHz 10pF 10MΩ 10 : 1
Multimeter	Fluke 8060A	ESK44	See calibration sertificate
Level Meter	Wandel u Goltermann SPM - 9	406274 K	See Calibration Sertificate
Power Supply	Phillips PE 1542	WB 9230	Input : 220 V AC Outputs: 0 - 20 V 0 - 1 A 0 - 20 V 0 - 1A 0 - 7 V 0 - 3A
MODEM	TELKOR FAM 200	6 I 0428	0 - -20dBm output 600Ω termination

A.5. Calibration Certificates

Appendix B

B.1. Level Meter Circuit Diagram

B.2. PCB layout

B.3. Component Layout

B.4. Component List

Appendix C

C.1. LF 351 OP Amp

C.2. AD7890A ADC

C.3. DAC 0800

C.4. 8751 Microcontroller

C.5. AD536A True RMS-to-DC Converter

C.6. LM 311 Voltage Comparator

C.7. LM3999 Precision Reference

C.8. LM 7915 Regulator

C.9. LM 7805 / LM 7815 Regulator

C.10. Calex 48T5 DC/DC Converter

ESKOM

ESKOM CALIBRATION SERVICE

ESKOM DISTRIBUTOR GROUP CAPE DIVISION

METROLOGY STANDARDS LABORATORY

CERTIFICATE OF CALIBRATION

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SYSTEM PERFORMANCE
Telephone no : X 3366

It complies in full with the conditions of the approval granted by the Eskom Calibration Service. It is a correct record of the measurements made. This certificate may not be reproduced other than in full except with written approval of the issuing laboratory.

CERTIFICATE No: SL10154/ 01

DATE OF ISSUE : 12-04-96

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HEAD OF LABORATORY: ZW DE WITT

BRACKENFELL PO Box 222, BRACKENFELL, 7560 : TEL (021) 980-3294

ESKOM

CALIBRATION OF OSCILLOSCOPE

MAKE	: TEKTRONIX
MODEL/TYPE	: TDS420
INSTRUMENT NUMBER	: 12122
CALIBRATED FOR	: ESCOM
CALIBRATION PROCEDURE No	: SEE PAGE 3
CALIBRATION EQUIPMENT	: MSL 078

The laboratory is environmentally controlled at a Temperature of 23°C +/- 2°C and a Relative Humidity between 35% and 60%.

Uncertainties of measurements are quoted in terms of a 95 % Confidence Level.

The values in this certificate are correct at the time of calibration. Subsequently the accuracy will depend on such factors as the care exercised in handling and use of the instrument, and the frequency of use. Recalibration should be performed after a period which has been chosen to ensure that the instrument's accuracy remains within the prescribed limits.

Recommended due date :12-04-97

CERTIFICATE No: SL10154/ 01

DATE OF ISSUE : 12-04-96

PAGE 2 OF 4 PAGES

CALIBRATED BY:ZW DE WITT

ESKOM

1. PROCEDURE

The instrument was calibrated in terms of laboratory standards, the accuracies of which were traceable to national measuring standards maintained at the CSIR.

2. RESULTS

2.1 TIMEBASE CALIBRATION

Setting (S)	(%) Error CH 1
2 n	0,0
5 n	0,0
10 n	0,0
20 n	0,0
50 n	0,0
0,1 µ	0,0
0,2 µ	0,0
0,5 µ	0,0
1,0 µ	0,0
2,0 µ	0,0
5 µ	0,0
10 µ	0,0
20 µ	0,0
50 µ	0,0
0,1 m	0,0
0,2 m	0,0
0,5 m	0,0
1,0 m	0,0
2,0 m	0,0
5,0 m	0,0
10 m	0,0
20 m	0,0
50 m	0,0
0,1	0,0
0,2	0,0
0,5	0,0

Uncertainty of measurements: ± 0,5 %

CERTIFICATE No: SL10154/01

DATE OF ISSUE : 12-04-96

PAGE 3 OF 4 PAGES

CALIBRATED BY: ZW DE WITT

ESKOM

2.2 AMPLITUDE CALIBRATION

Applied (V)	Setting (V)	(%) Error Chan 1	Chan 2	Chan 3	Chan 4
10 m	2 m	0,0	- 0,2	- 0,1	0,0
20 m	5 m	- 0,4	0,0	0,0	0,0
50 m	10 m	- 0,1	- 0,2	0,0	0,0
0,1	20 m	- 0,3	- 0,4	0,0	- 0,1
0,2	50 m	- 0,3	- 0,4	0,0	- 0,2
0,5	0,1	- 0,2	- 0,2	0,0	0,0
1	0,2	- 0,1	- 0,4	- 0,1	0,0
2	0,5	- 0,1	- 0,2	0,0	0,0
5	1	- 0,1	0,0	- 0,1	0,0
10	2	0,0	0,0	- 0,2	+ 0,1
20	5	0,0	0,0	- 0,1	+ 0,2
50	10	0,0	0,0	- 0,2	0,0

Uncertainty of measurement: ± 1 %

2.3 BANDWIDTH VERIFICATION (100 mV)

The - 3 dB point of Chan 1 = > 234 MHz
Chan 2 = > 230 MHz
Chan 3 = > 239 MHz
Chan 4 = > 239 MHz

Uncertainty of measurement: ± 5 %

3. REMARKS

3.1 Tests were done to confirm correct operation of all functions, on all ranges, of the instrument.

3.2 The instrument performed to within the manufacturers accuracy specification.

CERTIFICATE No: SL10154/01

DATE OF ISSUE : 12-04-96

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CERTIFICATE No: SL10155/ 01

DATE OF ISSUE : 26-04-96

PAGE 1 OF 4 PAGES

HEAD OF LABORATORY: ZW DE WITT

BRACKENFELL PO Box 222, BRACKENFELL, 7560 : TEL (021) 980-3294

ESKOM

CALIBRATION OF SELECTIVE LEVEL METER

MAKE	: W&G
MODEL/TYPE	: SPM9
INSTRUMENT NUMBER	: 406274
CALIBRATED FOR	: ESCOM
CALIBRATION PROCEDURE No	: SEE PAGE 3
CALIBRATION EQUIPMENT	: MSL 136, 076 & 104,M

The laboratory is environmentally controlled at a Temperature of 23°C +/- 2°C and a Relative Humidity between 35% and 60%.

Uncertainties of measurements are quoted in terms of a 95 % Confidence Level.

The values in this certificate are correct at the time of calibration. Subsequently the accuracy will depend on such factors as the care exercised in handling and use of the instrument, and the frequency of use. Recalibration should be performed after a period which has been chosen to ensure that the instrument's accuracy remains within the prescribed limits.

Recommended due date :26-04-97

CERTIFICATE No: SLi0155/ 01

DATE OF ISSUE : 26-04-96

PAGE 2 OF 4 PAGES

CALIBRATED BY:ZW DE WITT

ESKOM

1. PROCEDURE

The instrument was calibrated in terms of laboratory standards, the accuracies of which were traceable to national measuring standards maintained at the CSIR.

2. RESULTS

2.1 RECEIVER RESPONCE VERIFICATION

RX SCALE LINEARITY CHECK (Coax)

2.1.1 Instrument Range setting: 1 dB

Applied frequencies: 10 kHz, 100 kHz

Applied dBm	Indicated dBm 600Ω (Bal)	150Ω (Bal)
- 0,50	- 0,48	- 0,46
0,00	+ 0.02	+ 0,05
+ 0,10	+ 0,12	+ 0,13
+ 0,20	+ 0,23	+ 0,22
+ 0,30	+ 0,32	+ 0,34
+ 0,40	+ 0,39	+ 0,41
+ 0,50	+ 0,50	+ 0,52
+ 1,00	+ 1,02	+ 1,03

Uncertainty of measurement: + 0,01 dB

2.1.2 Range verification

Applied frequencies: 10 kHz, 100 kHz

Applied dBm	Indicated dBm 600Ω (Bal)	150Ω (Bal)
+ 10,00	+ 10,08	+ 10,06
0.00	+ 0,02	+ 0,05
- 10.00	- 10,96	- 9,94
- 20.00	- 20,97	- 19,95
- 30.00	- 30,97	- 29,96
- 40.00	- 40,01	- 40,94

Uncertainty of measurement: ± 0,1 dB

CERTIFICATE No: SL10155/01

DATE OF ISSUE : 26-04-96

PAGE 3 OF 4 PAGES

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2.2 RX INPUT FREQUENCY CHECK

Instrument settings (Selective :60 Hz)

Applied Frequency (Hz)	DUT Indicated frequency (Hz)
1,0000 k	1,00 k
3,0000 k	3,00 k
5,0000 k	5,00 k
10,0000 k	10,00 k
12,5000 k	12,50 k
15,0000 k	15,00 k
17,5000 k	17,50 k
20,0000 k	20,00 k
100,0000 k	100,00 k

Uncertainty of measurement: ± 1 in 10^{-3} ·f ± 1 Hz

3 REMARKS

None.

CERTIFICATE No: SL10155/01

DATE OF ISSUE : 26-04-96

PAGE 4 OF 4 PAGES

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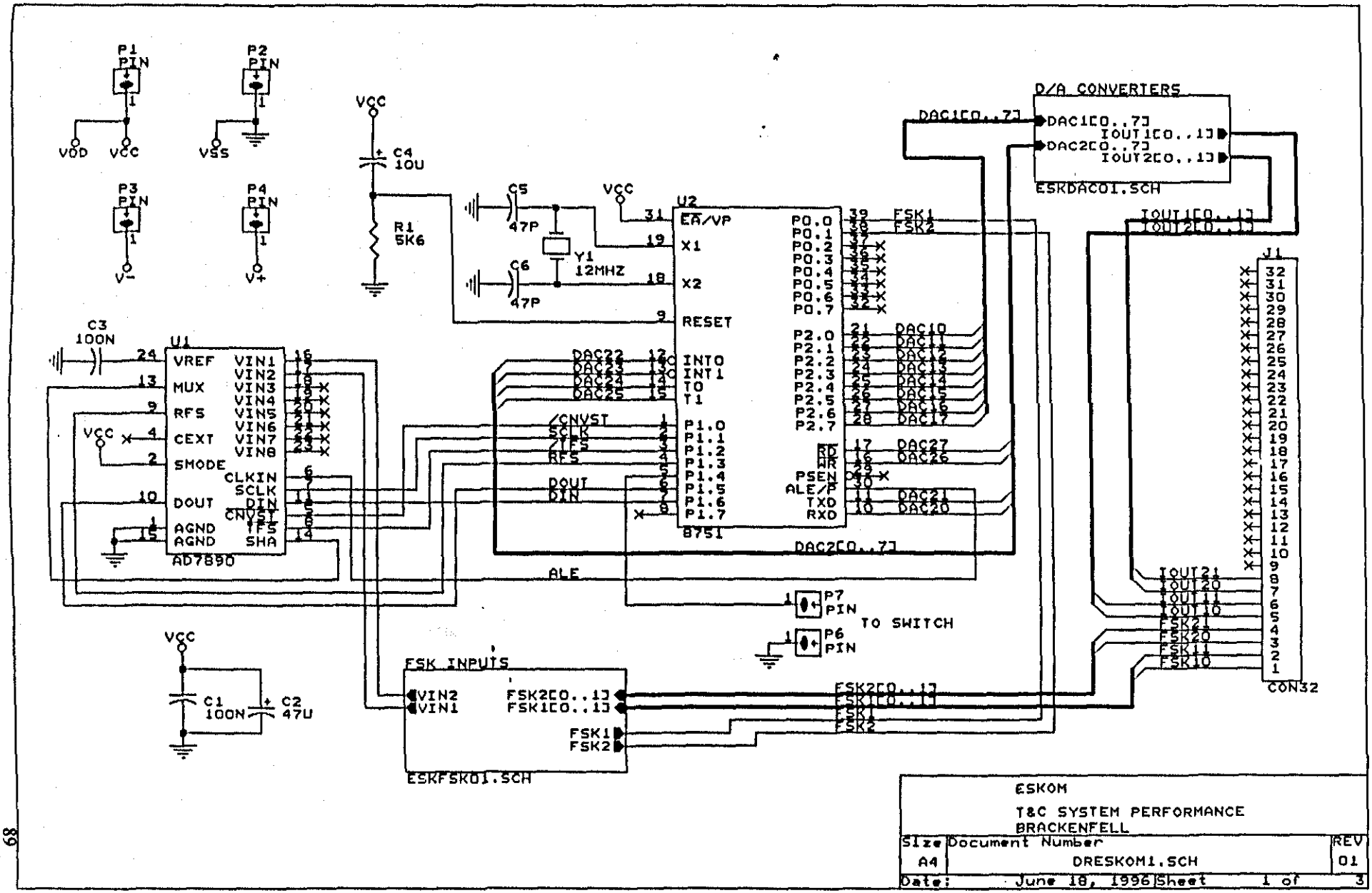
Appendix B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P2 PIN
P3 PIN
P4 PIN
VDD
VCC
VSS
V-
V+
C4 10U
R1 5K6
C5 47P
C6 47P
Y1 12MHZ
C3 100N
U1
AD7890
VREF
MUX
RFS
CEXT
SMODE
DOUT
AGND
CLKIN
SCLK
DIN
CNVST
SHA
VIN1
VIN2
VIN3
VIN4
VIN5
VIN6
VIN7
VIN8
U2
8751
EA/VP
X1
X2
RESET
INT0
INT1
T0
T1
TXD
RXD
PSEN
ALE/P
D/A CONVERTERS
DAC1D0..7
DAC2D0..7
IOUT1D0..11
IOUT2D0..11
ESKDAC01.SCH
J1
CON32
P7 PIN
TO SWITCH
P6 PIN
ALE
C1 100N
C2 47U
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FSK1D0..11
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Size A4
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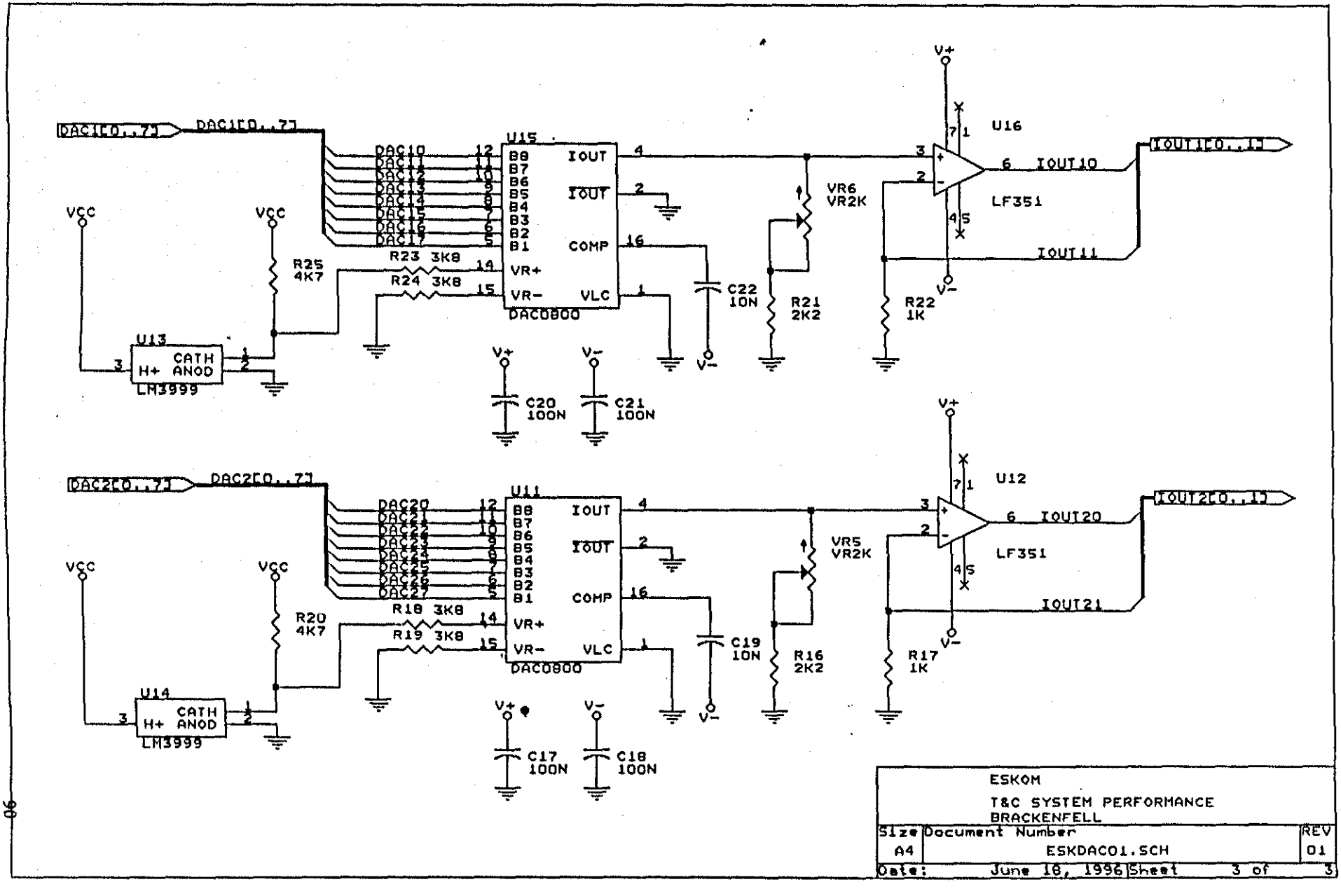
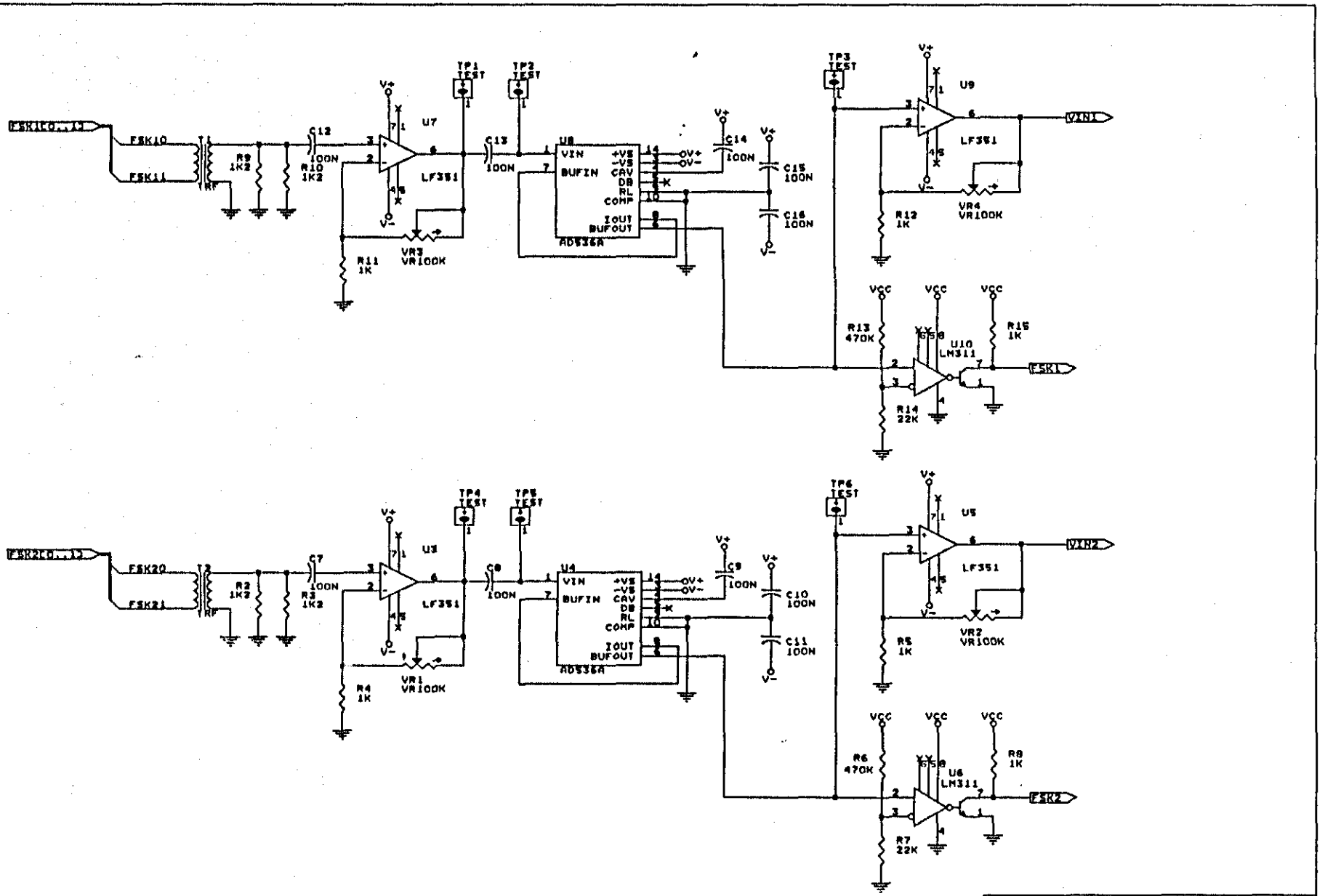
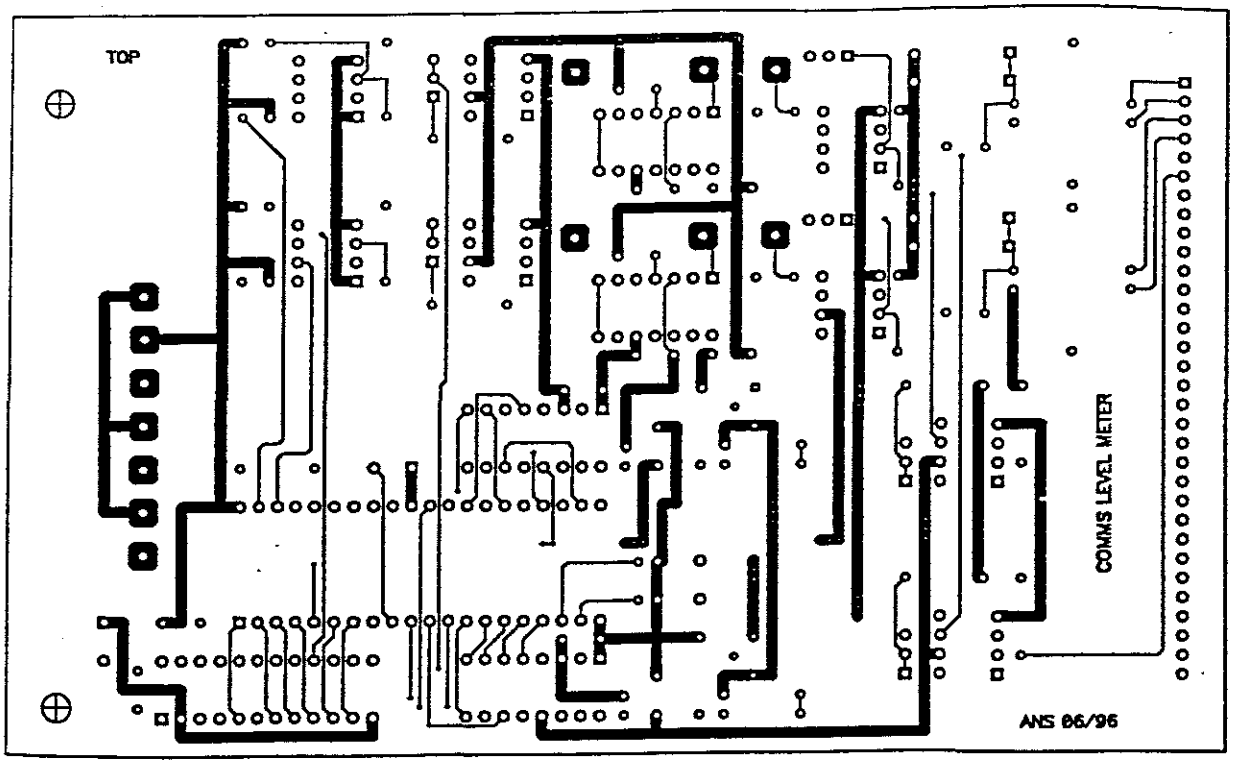
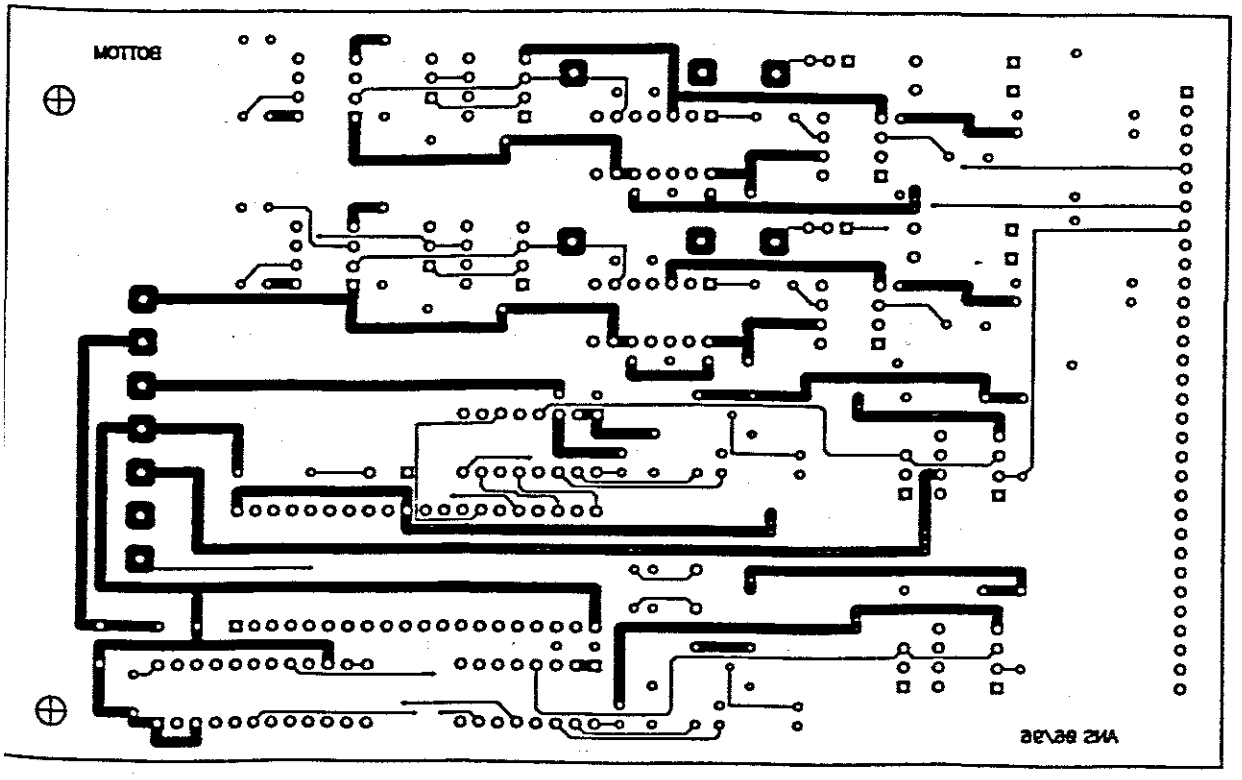
REV 01
Date: June 18, 1996
Sheet 1 of 3

68


DAC1[0..7]
DAC1[0..7]
U15
DAC10
DAC11
DAC12
DAC13
DAC14
DAC15
DAC16
DAC17
B8
B7
B6
B5
B4
B3
B2
B1
IOUT
IOUT
COMP
VR+
VR-
VLC
DAC0800
R23 3K8
R24 3K8
R25 4K7
VCC
VCC
U13
CATH
H+ ANOD
LM3999
C22 10N
C20 100N
C21 100N
V+
V-
VR6 VR2K
R21 2K2
R22 1K
U16
LF351
IOUT10
IOUT11
IOUT1[0..1]
DAC2[0..7]
DAC2[0..7]
U11
DAC20
DAC21
DAC22
DAC23
DAC24
DAC25
DAC26
DAC27
R18 3K8
R19 3K8
R20 4K7
U14
C19 10N
C17 100N
C18 100N
VR5 VR2K
R16 2K2
R17 1K
U12
IOUT20
IOUT21
IOUT2[0..1]
ESKOM
T&C SYSTEM PERFORMANCE
BRACKENFELL
Size A4
Document Number ESKDAC01.SCH
REV 01
Date: June 18, 1996
Sheet 3 of 3


FSK1[0..1]
FSK10
FSK11
R9 1K2
R10 1K2
C12 100N
U7
LF351
C13 100N
U8
VIN
BUFIN
+VS
-VS
CAV
DB
RL
COMP
IOUT
BUFOUT
AD536A
C14 100N
C15 100N
C16 100N
R11 1K
VR3 VR100K
TP1 TEST
TP2 TEST
TP3 TEST
U9
LF351
VR4 VR100K
R12 1K
VIN1
VCC
R13 470K
U10 LM311
R15 1K
R14 22K
FSK1
FSK2[0..1]
FSK20
FSK21
R2 1K2
R3 1K2
C7 100N
U3
LF351
C8 100N
U4
AD536A
C9 100N
C10 100N
C11 100N
R4 1K
VR1 VR100K
TP4 TEST
TP5 TEST
TP6 TEST
U5
LF351
VR2 VR100K
R5 1K
VIN2
R6 470K
U6 LM311
R8 1K
R7 22K
FSK2
ESKOM
T&C SYSTEM PERFORMANCE
BRACKENFELL
Size A3
Document Number ESKFSK01.SCH
REV 01
Date: June 18, 1996 Sheet 2 of 3


TOP
COMMS LEVEL METER
ANS 86/96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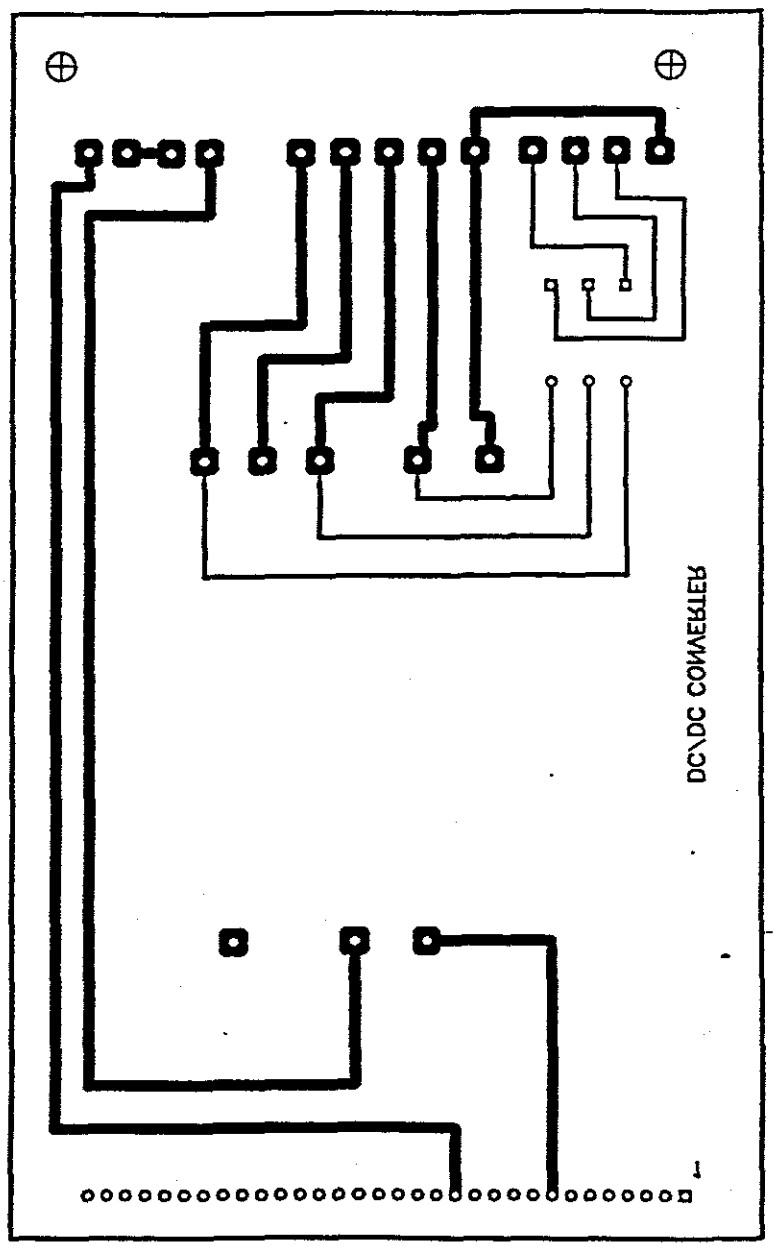
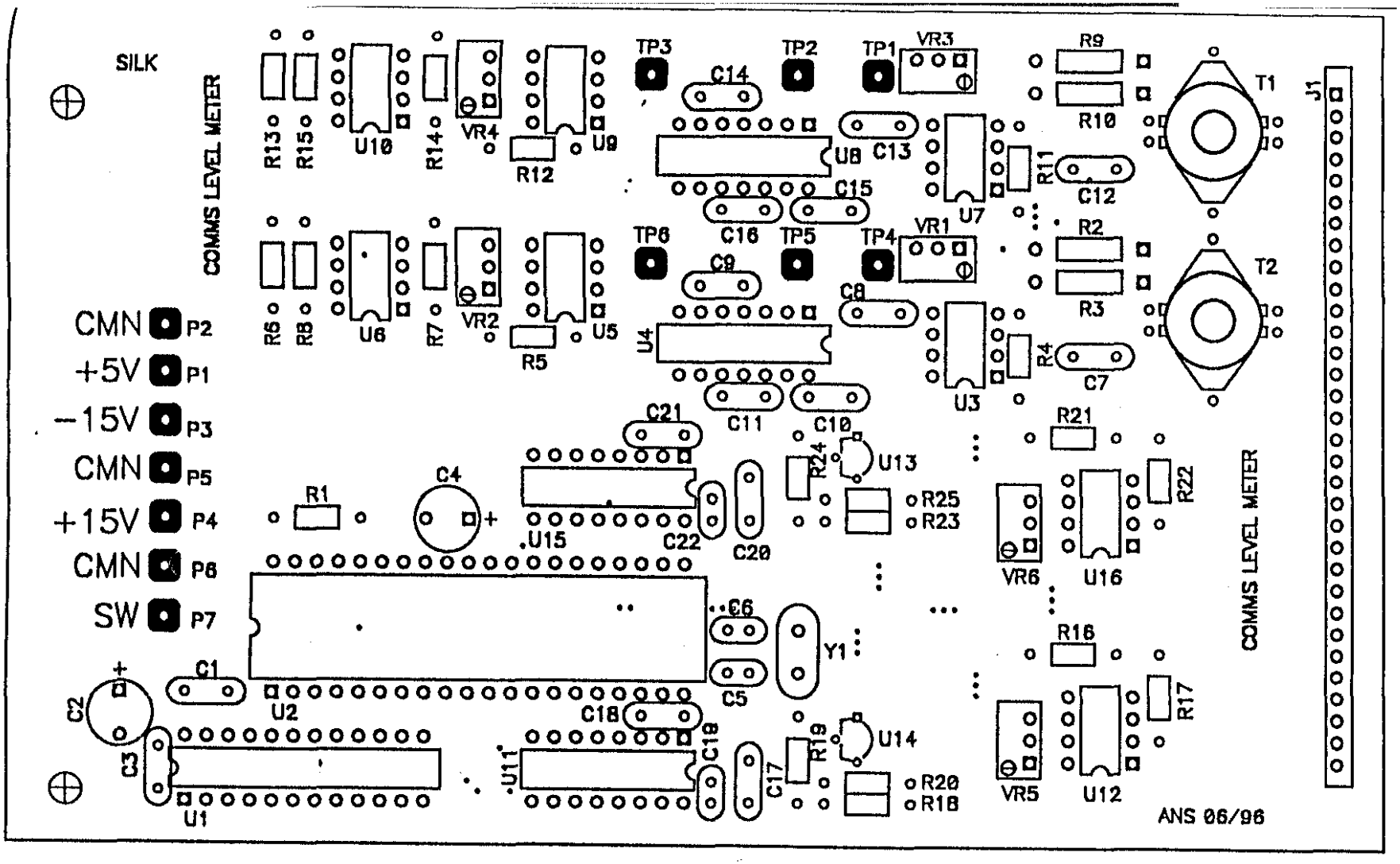
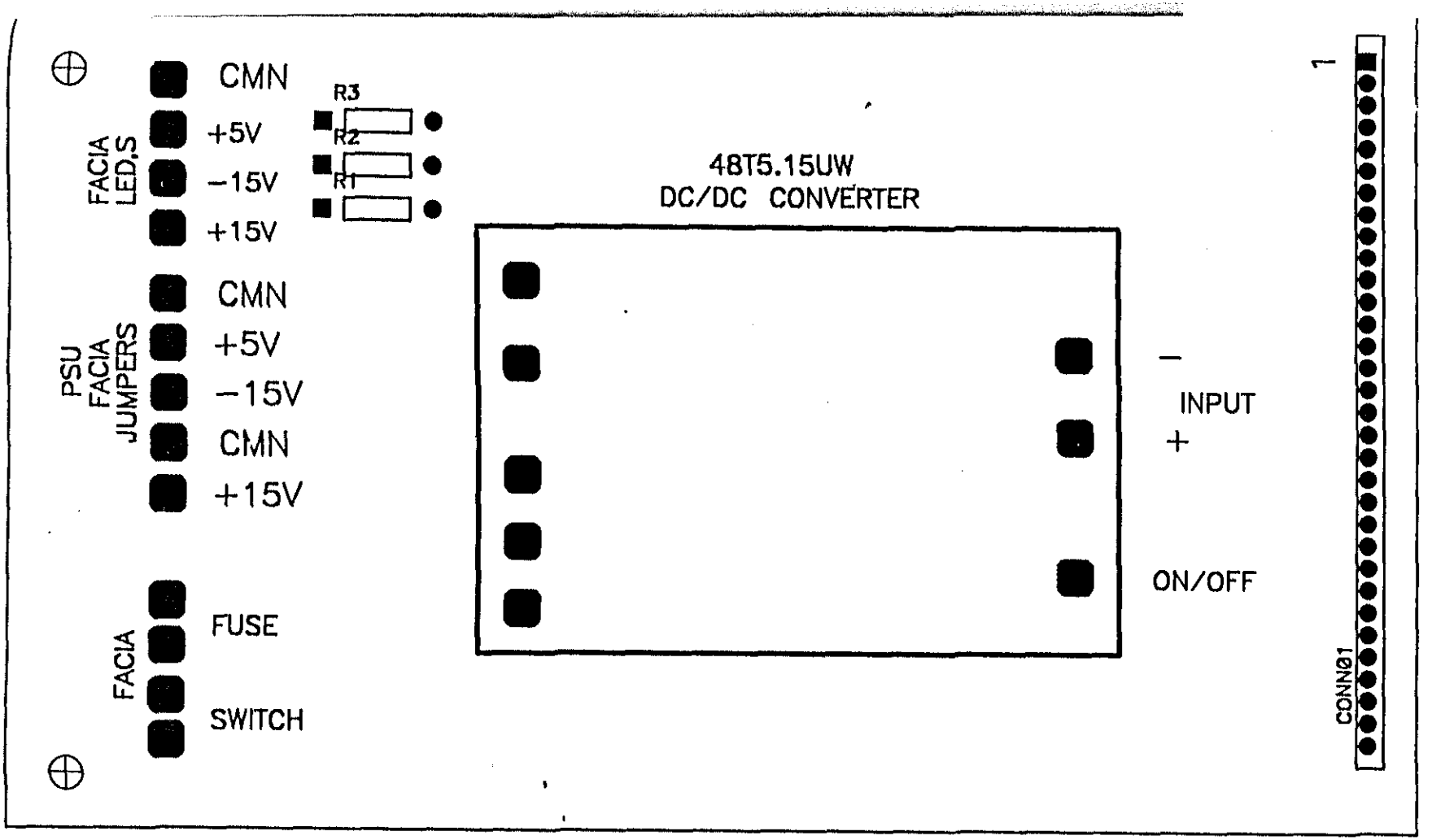

DC\DC CONVERTER


SILK
COMMS LEVEL METER
CMN P2
+5V P1
−15V P3
CMN P5
+15V P4
CMN P6
SW P7
TP3
TP2
TP1
VR3
R9
T1
J1
C14
R10
U10
R13
R15
VR4
R14
U9
R12
U8
C13
C15
U7
R11
C12
TP6
TP5
TP4
VR1
R2
T2
C16
C9
C8
R3
U6
R6
R8
VR2
R7
U5
R5
U4
R4
C7
U3
C11
C10
C21
R21
R24
U13
R1
C4
R25
R23
R22
U15
C22
C20
VR6
U16
C6
R16
Y1
C1
C5
C2
U2
C18
R19
U14
C3
C17
R20
R18
VR5
U12
R17
U11
U1
ANS 06/96
COMMS LEVEL METER


CMN
+5V
−15V
+15V
FACIA LED,S
R3
R2
R1
CMN
+5V
−15V
CMN
+15V
PSU FACIA JUMPERS
48T5.15UW
DC/DC CONVERTER
−
INPUT
+
ON/OFF
FUSE
SWITCH
FACIA
1
CONN01

B.4. Component List

Power Supply

Resistors

R1	680 Ω / ¼ W
R2	680 Ω / ¼ W
R3	180 Ω / ¼ W

Semiconductors

LED 1	RED 3mm
LED 2	RED 3mm
LED 3	RED 3mm
Calex 48T5.15W DC/DC Converter	

Miscellaneous

SW1	SPST Miniature Toggle Switch
F1	20mm Panel Mount Fuse Holder + 150mA Fuse
CONN01	32Pin PC MOUNT EDGE Connector
3 X 3mm LD Holders	
PC Board / Front Pannel	

Level Meter

Resistors

R1	5k6 / ¼ W
R2, R3, R9, R10	1k2 / ¼ W
R6, R13	470K / ¼ W
R4, R5, R8, R11, R12, R15, R17, R22	1K / ¼ W
R7, R14	22K / ¼ W
R16, R21	2K2 / ¼ W
R18, R19, R23, R24	3K8 / ¼ W
R20, R25	4K7 / ¼ W

Variable Resistors

VR1, VR2, VR3, VR4,	100K Multiturn 20T / Top
VR5, VR6	2K Multiturn 20T / Top

Capacitors

C1, C3, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C20, C21	100nF
C2	47uF Elec
C4	10uF Elec
C5, C6	47pF
C19, C22	10nF

Semiconductors

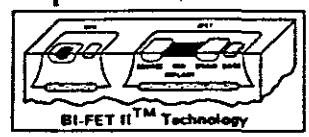
U1	AD7890
U2	8751
U3, U5, U7, U9, U12, U16	LF351
U4, U8	AD536A
U6, U10	LM311
U11, U15	DAC0800
U13, U14	LM3999

Miscellaneous

TP1, TP2, TP3, TP4, TP5, TP6	Test Pins
T1, T2	1 : 1 Isolation Tranformer 251 - AG0
CON32	32Pin PC MOUNT EDGE Connector
Y1	12mhz Crystal
8 PIN IC Socket X 8	
14 PIN IC Socket X 2	
16 PIN IC Socket X 2	
24 PIN IC Socket X 1	
40 PIN IC Socket X 1	
PC Board / Front Pannel	

Appendix C

National Semiconductor



LF351 Wide Bandwidth JFET Input Operational Amplifier

General Description

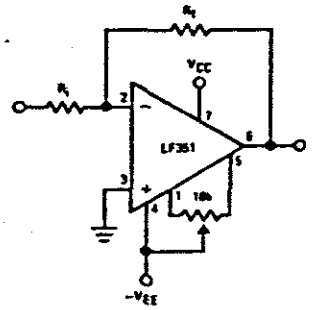
The LF351 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF351 is pin compatible with the standard LM741 and uses the same *offset voltage adjustment circuitry. This feature allows* designers to immediately upgrade the overall performance of existing LM741 designs.

The LF351 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the LF351 is the better choice.

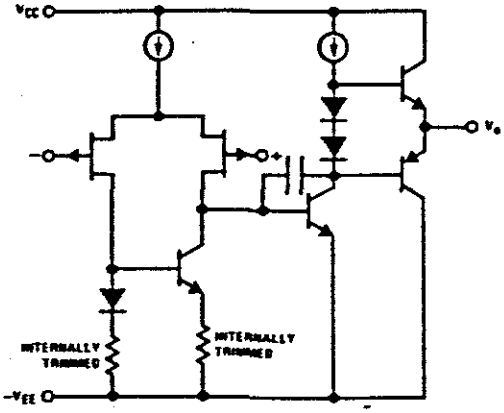
Features

■ Internally trimmed offset voltage	10 mV
■ Low input bias current	50 pA
■ Low input noise voltage	16 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	1.8 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20\ V_{p-p}$, BW = 20 Hz-20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection

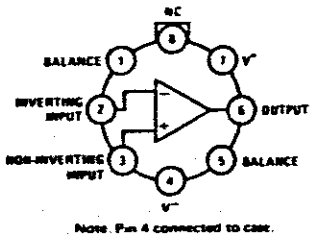


Simplified Schematic



Connection Diagrams (Top Views)

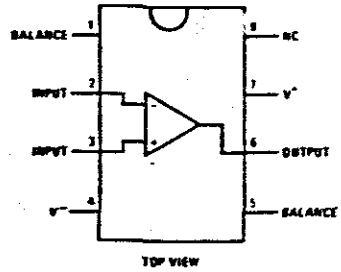
Metal Can Package



Note: Pin 4 connected to case.

Order Number LF351H
See NS Package H08C

Dual-In-Line Package



Order Number LF351N
See NS Package N08A

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF351			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S = 10k\Omega$, $T_A = 25°C$ Over Temperature		5	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10k\Omega$		10		µV/°C
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 4) $T_j \leq 70°C$		25	100 4	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 3, 4) $T_j \leq 70°C$		50	200 8	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 2k\Omega$	25	100		V/mV
		Over Temperature	15			V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	70	100		dB
I_S	Supply Current			1.8	3.4	mA

AC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF351			UNITS
			MIN	TYP	MAX	
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$		13		V/µs
GBW	Gain Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, $f = 1000Hz$		16		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$, $f = 1000Hz$		0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

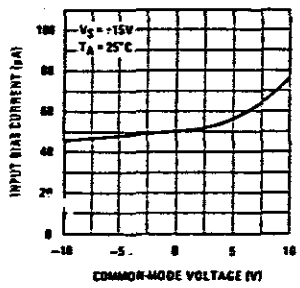
Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

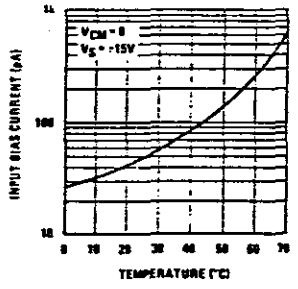
Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

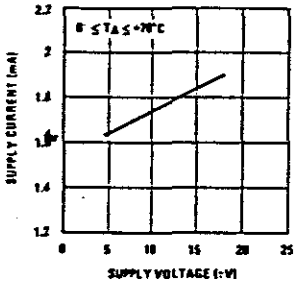
Input Bias Current



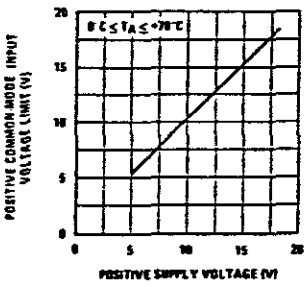
Input Bias Current



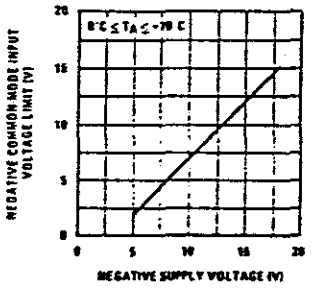
Supply Current



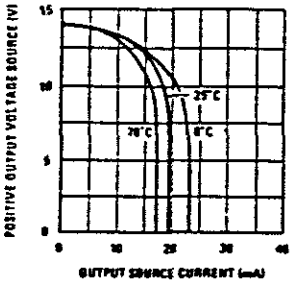
Positive Common-Mode Input Voltage Limit



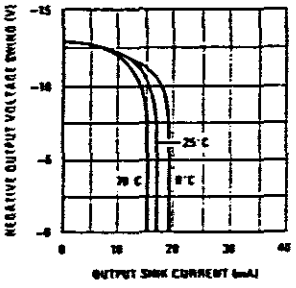
Negative Common-Mode Input Voltage Limit



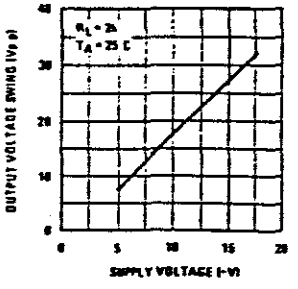
Positive Current Limit



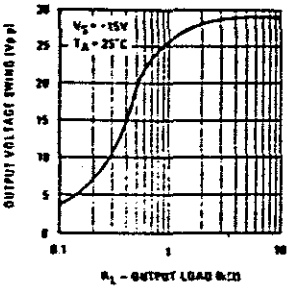
Negative Current Limit



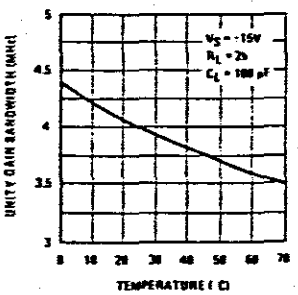
Voltage Swing



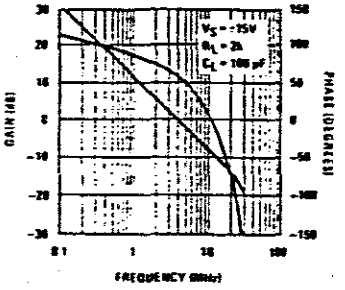
Output Voltage Swing



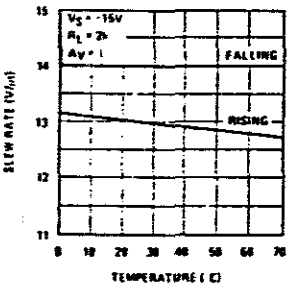
Gain Bandwidth



Bode Plot

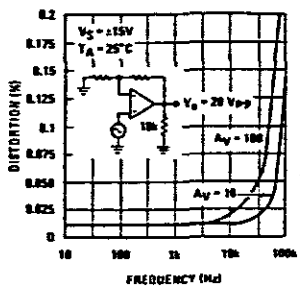


Slew Rate

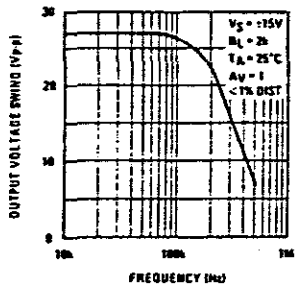


Typical Performance Characteristics (Continued)

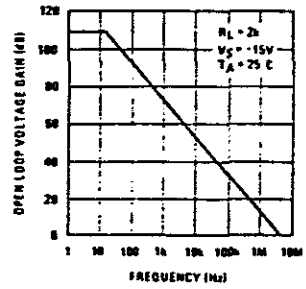
Distortion vs Frequency



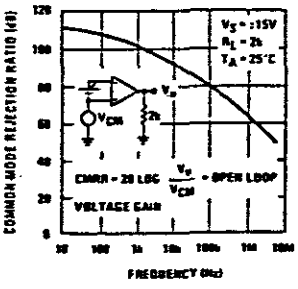
Undistorted Output Voltage Swing



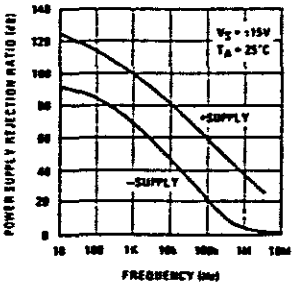
Open Loop Frequency Response



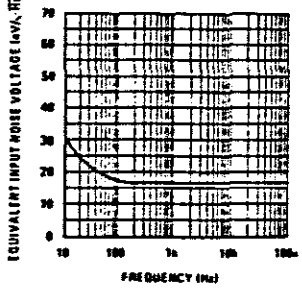
Common-Mode Rejection Ratio



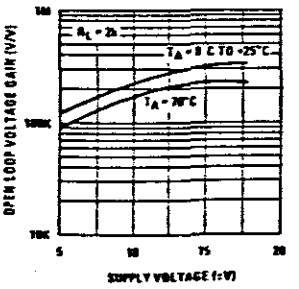
Power Supply Rejection Ratio



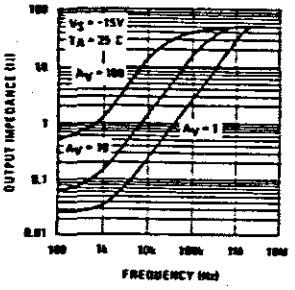
Equivalent Input Noise Voltage



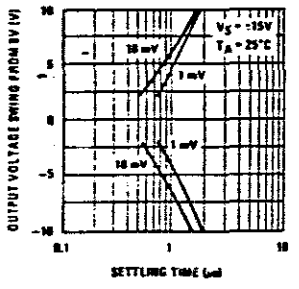
Open Loop Voltage Gain (V/V)



Output Impedance

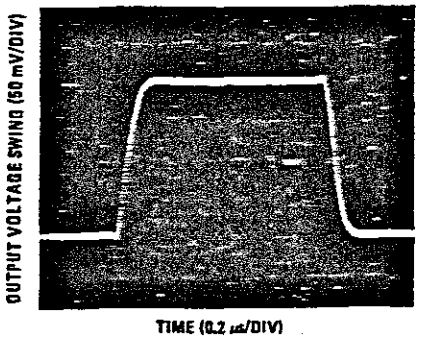


Inverter Settling Time

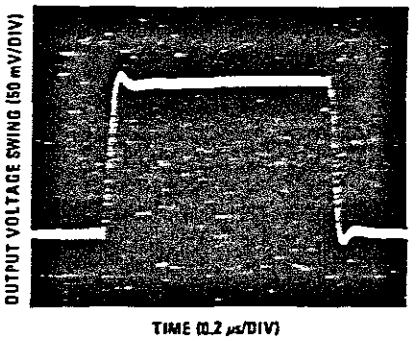


Pulse Response

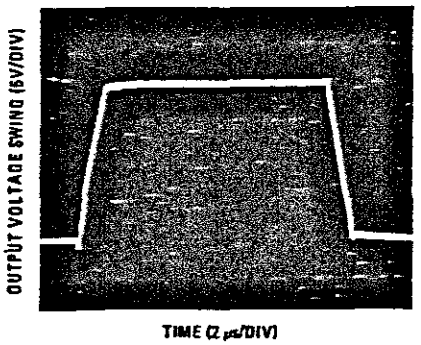
Small Signal Inverting



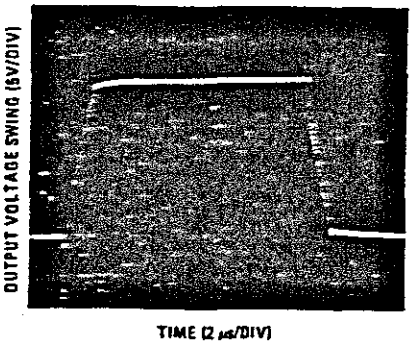
Small Signal Non-Inverting



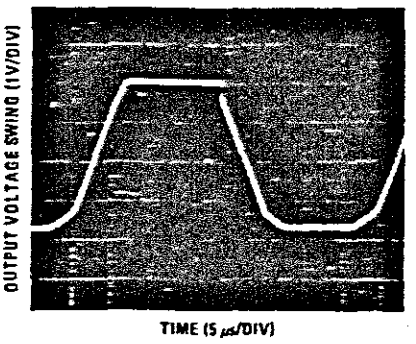
Large Signal Inverting



Large Signal Non-Inverting



Current Limit (R_L = 100Ω)



Application Hints

The LF351 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a

Application Hints (Continued)

high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF351 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF351 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

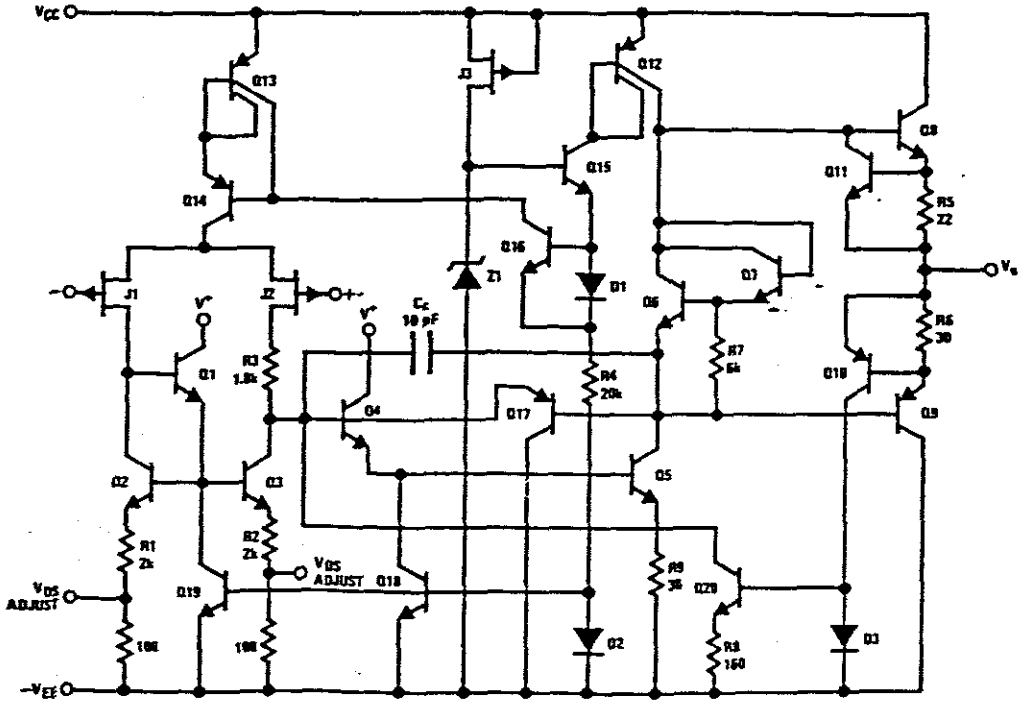
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

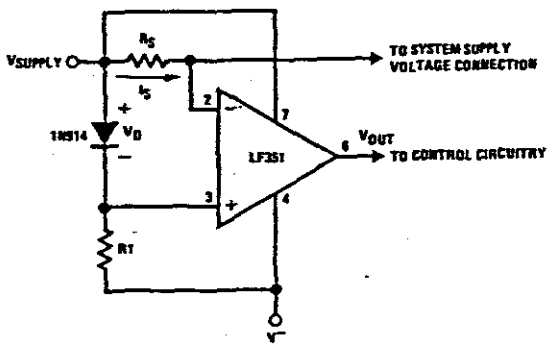
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



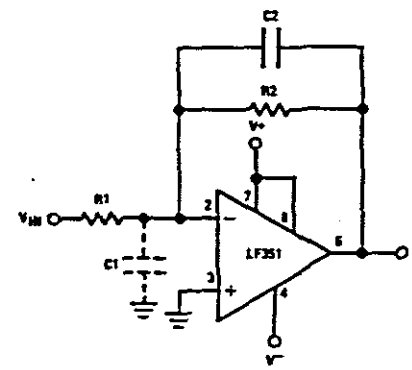
Typical Applications

Supply Current Indicator/Limiter



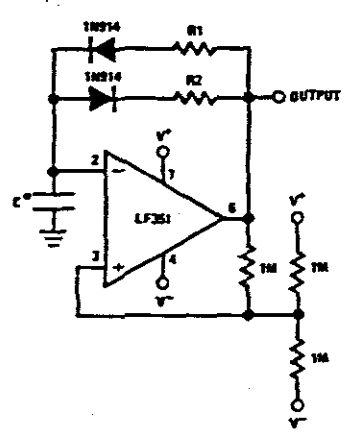
- V_{OUT} switches high when $R_S I_S > V_D$

Hi-Z_{IN} Inverting Amplifier



Parasitic input capacitance C1 ≈ 13 pF for LF351 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 = R1C1.

Ultra-Low (or High) Duty Cycle Pulse Generator

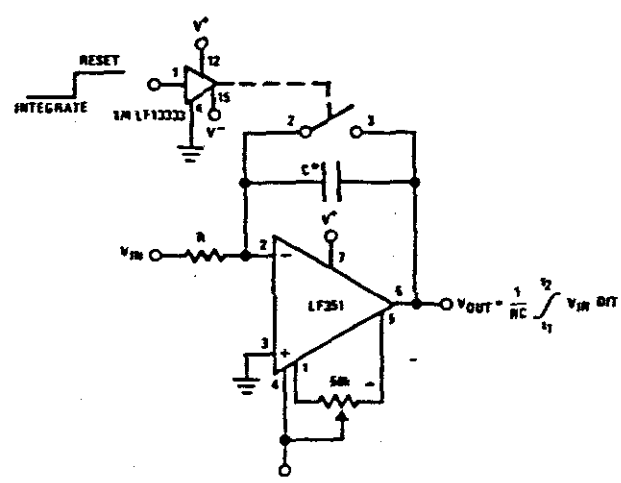


- $t_{OUTPUT\ HIGH} \approx R1C\ \ln \frac{4.8 - 2V_S}{4.8 - V_S}$
- $t_{OUTPUT\ LOW} \approx R2C\ \ln \frac{2V_S - 7.8}{V_S - 7.8}$

where $V_S = V^+ + |V^-|$

*low leakage capacitor

Long Time Integrator



*Low leakage capacitor

- 50k pot used for less sensitive V_{OS} adjust

National Semiconductor

ADC0800 8-Bit A/D Converter

General Description

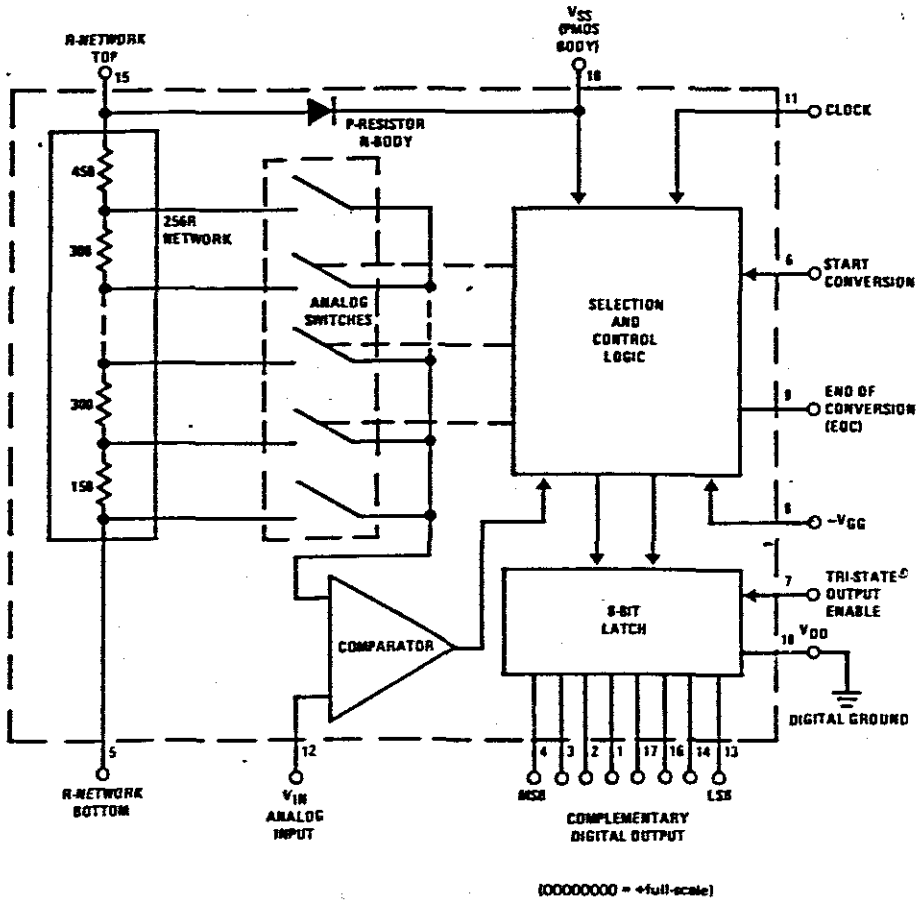
The ADC0800 is an 8-bit monolithic A/D converter using P-channel ion-implanted MOS technology. It contains a high input impedance comparator, 256 series resistors and analog switches, control logic and output latches. Conversion is performed using a successive approximation technique where the unknown analog voltage is compared to the resistor tie points using analog switches. When the appropriate tie point voltage matches the unknown voltage, conversion is complete and the digital outputs contain an 8-bit complementary binary word corresponding to the unknown. The binary output is TRI-STATE® to permit bussing on common data lines.

The ADC0800PD is specified over −55°C to +125°C and the ADC0800PCD is specified over 0°C to 70°C.

Features

- Low cost
- ±5V, 10V input ranges
- No missing codes
- Ratiometric conversion
- TRI-STATE outputs
- Fast — T_C = 50 μs
- Contains output latches
- TTL compatible
- Supply voltages — 5 V_{DC} and −12 V_{DC}
- Resolution — 8 bits
- Linearity — ±1 LSB
- Conversion speed — 40 clock periods
- Clock range — 50 to 800 kHz

Block Diagram



Absolute Maximum Ratings

Supply Voltage (V_{DD})	V_{SS}–22V
Supply Voltage (V_{GG})	V_{SS}–22V
Voltage at Any Input	V_{SS} + 0.3V to V_{SS}–22V
Storage Temperature	150°C
Operating Temperature	
ADC0800PD	–55°C to +125°C
ADC0800PCD	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C

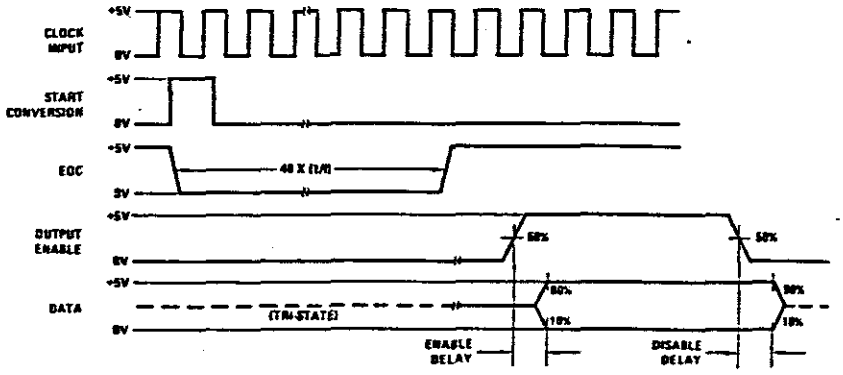
Electrical Characteristics

These specifications apply for V_{SS} = 5.0 V_{DC}, V_{GG} = –12.0 V_{DC}, V_{DD} = 0 V_{DC}, a reference voltage of 10.000 V_{DC} across the on-chip R-network ($V_{R\text{-}NETWORK\ TOP}$ = 5.000 V_{DC} and $V_{R\text{-}NETWORK\ BOTTOM}$ = –5.000 V_{DC}), and a clock frequency of 800 kHz. For all tests, a 475Ω resistor is used from pin 5 to ground. Unless otherwise noted, these specifications apply over an ambient temperature range of –55°C to +125°C for the ADC0800PD and 0°C to +70°C for the ADC0800PCD.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Non-Linearity	T_A = 25°C, *(Note 1)*			±1	LSB
	Over Temperature, (Note 1)			±2	LSB
Differential Non-Linearity				±1/2	LSB
Zero Error				±2	LSB
Zero Error Temperature Coefficient	(Note 2)			0.01	%/°C
Full-Scale Error				±2	LSB
Full-Scale Error Temperature Coefficient	(Note 2)			0.01	%/°C
Input Leakage				1	μA
Logical "1" Input Voltage	All Inputs	V_{SS}–1.0		V_{SS}	V
Logical "0" Input Voltage	All Inputs	V_{GG}		V_{SS}–4.2	V
Logical Input Leakage	T_A = 25°C, All Inputs, V_{IL} = V_{SS} – 10V			1	μA
Logical "1" Output Voltage	All Outputs, I_{OH} = 100 μA	2.4			V
Logical "0" Output Voltage	All Outputs, I_{OL} = 1.6 mA			0.4	V
Disabled Output Leakage	T_A = 25°C, All Outputs, V_{OL} = V_{SS} @ 10V			2	μA
Clock Frequency	0°C ≤ T_A ≤ +70°C	50		800	kHz
	–55°C ≤ T_A ≤ +125°C	100		500	kHz
Clock Pulse Duty Cycle		40		60	%
TRI-STATE Enable/Disable Time				1	μs
Start Conversion Pulse	(Note 3)	1		3 1/2	Clock Periods
Power Supply Current	T_A = 25°C			20	mA

Note 1: Non-linearity specifications are based on best straight line.
Note 2: Guaranteed by design only.
Note 3: Start conversion pulse duration greater than 3 1/2 clock periods will cause conversion errors.

Timing Diagram



Data is complementary binary (full scale is all "0's" output).

Application Hints

OPERATION

The ADC0800 contains a network with 256-300Ω resistors in series. Analog switch taps are made at the junction of each resistor and at each end of the network. In operation, a reference (10.00V) is applied across this network of 256 resistors. An analog input (V_{IN}) is first compared to the center point of the ladder via the appropriate switch. If V_{IN} is larger than $V_{REF}/2$, the internal logic changes the switch points and now compares V_{IN} and 3/4 V_{REF}. This process, known as successive approximation, continues until the best match of V_{IN} and V_{REF}/N is made. N now defines a specific tap on the resistor network. When the conversion is complete, the logic loads a binary word corresponding to this tap into the output latch and an end of conversion (EOC) logic level appears. The output latches hold this data valid until a new conversion is completed and new data is loaded into the latches. The data transfer occurs in about 200 ns so that valid data is present virtually all the time. Conversion requires 40 clock periods. The device may be operated in the free running mode by connecting the Start Conversion line to the End of Conversion line. However, to ensure start-up under all possible conditions, an external Start Conversion pulse is required during power up conditions.

REFERENCE

The reference applied across the 256 resistor network determines the analog input range. V_{REF} = 10.00V with the top of the R-network connected to 5V and the bottom connected to −5V gives a ±5V range. The reference can be level shifted between V_{SS} and VGG. However, the voltage, which is applied to the top of the R-network (pin 15), must not exceed V_{SS} to prevent forward biasing the on-chip parasitic silicon diode which exists between the P-diffused resistors (pin 15) and the N-type body (pin 10, V_{SS}). Use of a standard logic power supply for V_{SS} can cause problems, both due to initial voltage tolerance and changes over temperature. A solution is to power the V_{SS} line (15 mA max drain) from the output of the op amp which is used to bias the top of the R-network (pin 15). The analog input voltage and the voltage which is applied to the bottom of the R-network (pin 5) must be at least 7V above the $-V_{DD}$ supply voltage to insure adequate voltage drive to the analog switches.

Other reference voltages may be used (such as 10.24V). If a 5V reference is used, the analog range will be 5V and accuracy will be reduced by a factor of 2. Thus, for maximum accuracy, it is desirable to operate with at least a 10V reference. For TTL logic levels, this requires 5V and −5V for the R-network. CMOS can operate at the 10 V_{DC} V_{SS} level and a single 10 V_{DC} reference can be used. All digital voltage levels for both inputs and outputs will be from ground to V_{SS}.

ANALOG INPUT AND SOURCE RESISTANCE CONSIDERATIONS

The lead to the analog input (pin 12) should be kept as short as possible. Both noise and digital clock coupling to this input can cause conversion errors. To minimize any input errors, the following source resistance considerations should be noted:

For $R_s \leq 5k$	No analog input bypass capacitor required, although a 0.1 μF input bypass capacitor will prevent pick-up due to unavoidable series lead inductance.
For $5k < R_s \leq 20k$	A 0.1 μF capacitor from the input (pin 12) to ground should be used.
For $R_s > 20k$	Input buffering is necessary.

If the overall converter system requires lowpass filtering of the analog input signal, use a 20 kΩ or less series resistor for a passive RC section or add an op amp RC active lowpass filter (with its inherent low output resistance) to insure accurate conversions.

CLOCK COUPLING

The clock lead should be kept away from the analog input line to reduce coupling.

LOGIC INPUTS

The logical "1" input voltage swing for the Clock, Start Conversion and Output Enable should be (V_{SS} − 1.0V).

Application Hints (Continued)

CMOS will satisfy this requirement but a pull-up resistor should be used for TTL logic inputs.

RE-START AND DATA VALID AFTER EOC

The EOC line (pin 9) will be in the low state for a maximum of 40 clock periods to indicate "busy". A START pulse which occurs while the A/D is BUSY will reset the SAR and start a new conversion with the EOC signal remaining in the low state until the end of this new conversion. When the conversion is complete, the EOC line will go to the high voltage state. An additional 4 clock periods must be allowed to elapse after EOC goes high, before a new conversion cycle is requested. Start Conversion pulses which occur during this last 4 clock period interval may be ignored (see *Figures 1 and 2* for high speed operation). This is only a problem for high conversion rates and keeping the number of conversions per second less than $(1/44) \times f_{CLOCK}$ automatically guarantees proper operation. For example, for an 800 kHz clock, 18,000 conversions per second are allowed. The transfer of the new digital data to the output is initiated when EOC goes to the high voltage state.

POWER SUPPLIES

Standard supplies are V_{SS} = 5V, V_{GG} = −12V and V_{DD} = 0V. Device accuracy is dependent on stability of the reference voltage and has slight sensitivity to $V_{SS} - V_{GG}$. V_{DD} has no effect on accuracy. Noise spikes on the V_{SS} and V_{GG} supplies can cause improper conversion; therefore, filtering each supply with a 4.7 μF tantalum capacitor is recommended.

CONTINUOUS CONVERSIONS AND LOGIC CONTROL

Simply tying the EOC output to the Start Conversion input will allow continuous conversions, but an oscillation on this line will exist during the first 4 clock periods after EOC goes high. Adding a D flip-flop between EOC (D input) to Start Conversion (Q output) will prevent the oscillation and will allow a stop/continuous control via the "clear" input.

To prevent missing a start pulse which may occur after EOC goes high and prior to the required 4 clock period time interval, the circuit of *Figure 1* can be used. The RS latch can be set at any time and the 4-stage shift register delays the application of the start pulse to the A/D by 4 clock periods. The RS latch is reset 1 clock period after the A/D EOC signal goes to the low voltage state. This circuit also provides a Start Conversion pulse to the A/D which is 1 clock period wide.

A second control logic application circuit is shown in *Figure 2*. This allows an asynchronous start pulse of arbitrary length less than T_C, continuously converts for a fixed high level and provides a single clock period start pulse to the A/D. The binary counter is loaded with a count of 11 when the start pulse to the A/D appears. Counting is inhibited until the EOC signal from the A/D goes high. A carry pulse is then generated 4 clock periods after EOC goes high and is used to reset the input RS latch. This carry pulse can be used to indicate that the conversion is complete, the data has transferred to the output buffers and the system is ready for a new conversion cycle.

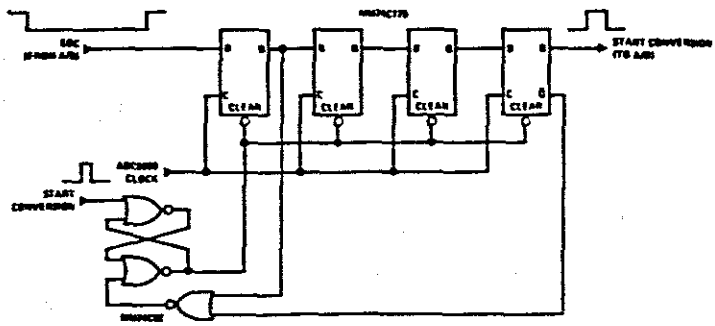


FIGURE 1. Delaying an Asynchronous Start Pulse

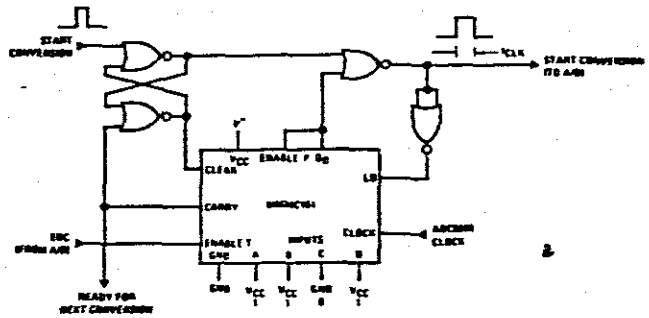


FIGURE 2. A/D Control Logic

Application Hints (Continued)

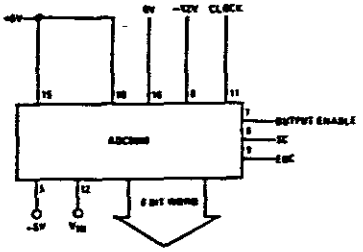
ZERO AND FULL-SCALE ADJUSTMENT

Zero Adjustment: This is the offset voltage required at the bottom of the R-network (pin 5) to make the 11111111 to 11111110 transition when the input voltage is 1/2 LSB (20 mV for a 10.24V scale). In most cases, this can be accomplished by having a 1 kΩ pot on pin 5. A resistor of 475Ω can be used as a non-adjustable best approximation from pin 5 to ground.

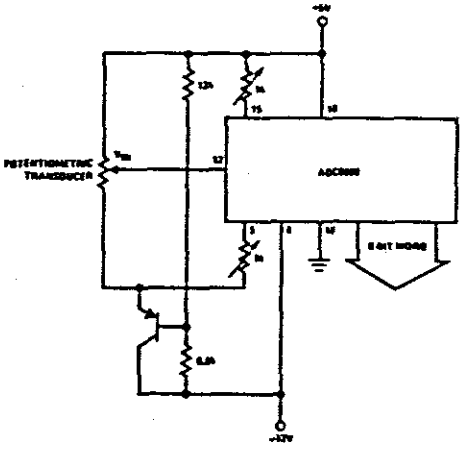
Full-Scale Adjustment: This is the offset voltage required at the top of the R-network (pin 15) to make the 00000001 to 00000000 transition when the input voltage is 1 1/2 LSB from full-scale (60 mV less than full-scale for a 10.24V scale). This voltage is guaranteed to be within 2 LSB for the ADC0800. In most cases, this can be accomplished by having a 1 kΩ pot on pin 15.

Typical Applications

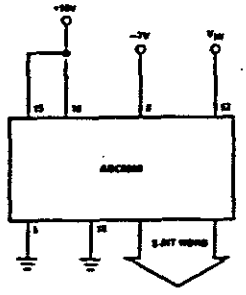
General Connection



Ratiometric Input Signal with Tracking Reference



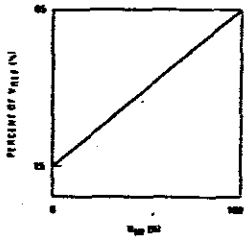
Hi-Voltage CMOS Output Levels

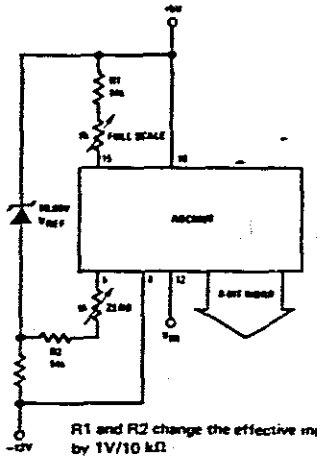


0V to 10V V_{IN} range
0V to 10V output levels

Level Shifted Zero and Full-Scale for Transducers

Level Shifted Input Signal Range

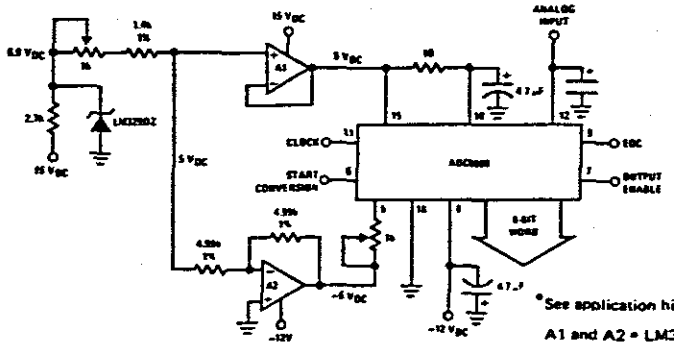




R1 and R2 change the effective input range by 1V/10 kΩ

Typical Applications (Continued)

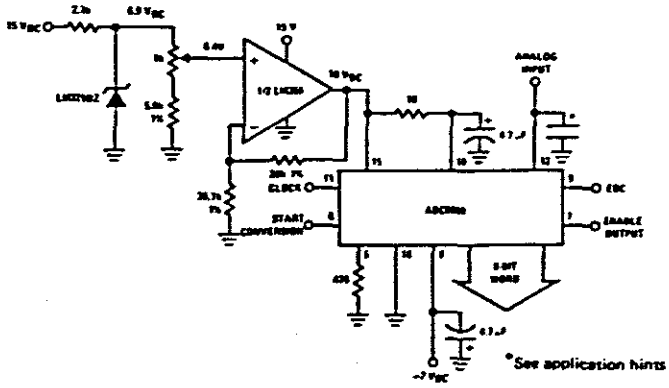
V_{REF} = 10 V_{DC} With TTL Logic Levels



*See application hints

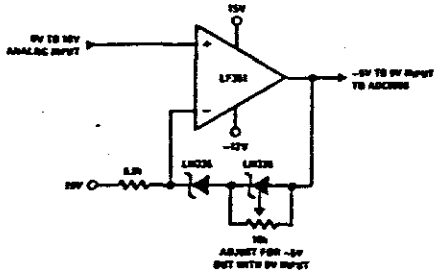
A1 and A2 = LM358N dual op amp

V_{REF} = 10 V_{DC} With 10V CMOS Logic Levels



*See application hints

Input Level Shifting



- Permits TTL compatible outputs with 0V to 10V input range (0V to −10V input range achieved by reversing polarity of zener diodes and returning the 6.8k resistor to V⁻).

MICROPROCESSOR INTERFACE

Figure 3 and the following sample program are included to illustrate both hardware and software requirements to allow output data from the ADC0800 to be loaded into the memory of a microprocessor system. For this example, National's INS8060, SC/MP II, microprocessor has been used.

The sample program, as shown, will start the converter, load the converter's output data into the accumulator, keep track of the number of data bytes entered, complement the data and store this data into sequential memory locations. After 256 bytes have been entered, the control jumps to the user's program where proces-

Typical Applications (Continued)

sing of the data entered will be implemented. A more practical program whereby each data byte entered will be processed before another entry is made can easily be done by jumping back to the user's program at the end of the interrupt routine (where the data is loaded into the accumulator and stored in memory). The end of the user's program should provide a jump back to the INITIALIZE statement to start a new conversion and generate a new data entry.

The following arbitrarily chosen addresses and pointer assignments are used in this example:

Pointer 1 — WORD COUNT (ADDR:0100)
Also used to point to the A/D converter at address 0500 for this example when data is to be entered.

Pointer 2 — ENTERED DATA (ADDR's: 0200→ 02FF)
Data is stored in 2's complement binary form, i.e, 01111111 → +full-scale and 10000000→ — full-scale.

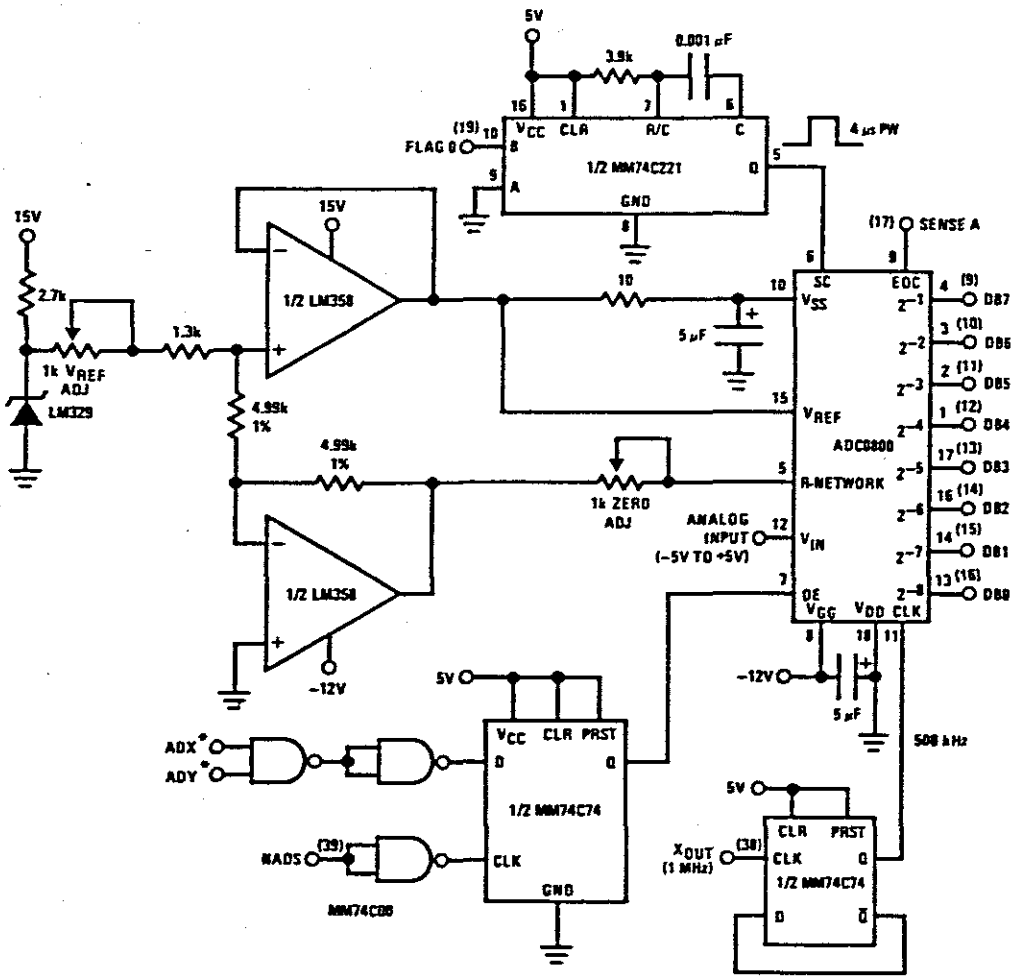
Pointer 3 — LOAD DATA SUBROUTINE (starts at ADDR:0300)
Executed when an EOC signal generates an interrupt request via sense A after an IEN (interrupt enable) instruction.

The address for the converter (0500) is unique for this particular sample program but may not be in a user's system so a different converter address must be used. Note that in *Figure 3* ADX and ADY for the address decode circuitry would be address bits ADB10 and ADB8 (pins 35 and 33 on the SC/MP II package) for converter address 0500.

SAMPLE PROGRAM TO LOAD DATA INTO MEMORY WITH SC/MP II.

```
0001  08      START:      NOP
0002  C4 01                LDIX'01
0004  35                  XPAH 1
0005  C4 00                LDIX'00
0007  31                  XPAL 1      ;P1 = 0100
0008  C4 02                LDIX'02
000A  36                  XPAH 2
000B  C4 00                LDIX'00
000D  C9 00                ST(P1)      ;Zero word count (P1)
000F  32                  XPAL 2      ;P2 = 0200
0010  C4 03                LDIX'03
0012  37                  XPAH 3
0013  08      INITIALIZE: NOP
0014  C4 00                LDIX'00
0016  33                  XPAL 3      ;P3 = 0300
0017  C4 01                LDIX'01
0019  07                  CAS         ;Starts converter via flag 0
001A  C1 00                LD (P1)
001C  F4 FF                XRIX'FF
001E  98 05                JZ DTA IN   ;Test to see if word count is FF,
                                        if so, jump to DTA IN
0020  05                  IEN         ;Enables INTERRUPT
0021  08      LOOP:       NOP
0022  90 FE                JMP LOOP    ;Loop until EOC
0024  08      DTA IN:     NOP
                          .
                          .
                          .           ;User program to process data
                          .
                          .
                          .
   ;DATA ENTRY SUBROUTINE
0300  08      DATA IN SR: NOP
0301  A9 00                ILD (P1)    ;Increment word count
0303  C4 05                LDIX'05
0305  35                  XPAH 1      ;P1 will point to converter
0306  C1 00                LD (P1)     ;Converter data loaded into
                                        accumulator
0308  F4 7F                XRIX'7F     ;Put data in 2's complement form
030A  CE 01                ST @ 1(P2)  ;Store data
030C  C4 00                LDIX'00
030E  07                  CAS         ;Resets flag 0
030F  C4 01                LDIX'01
0311  35                  XPAH 1      ;Resets P1 to point at word count
0312  C4 13                LDIX'13
0314  33                  XPAL 3
0315  3F                  XPPC 3      ;Return to INITIALIZE to start a
                                        new conversion
```

Typical Applications (Continued)



- Setting flag 0 (FLG0 = 1) with software, starts conversion (FLG0 must be cleared before another conversion can be initiated)
- With interrupt enabled an EOC will force an interrupt. Interrupt subroutine should load converter data into the accumulator.
- Output data is in complementary offset binary form
- Numbers in parentheses denote pin numbers of SC/MP chip

*ADX and ADY can be any of the address lines but they must be high *only* at the time the converter output data is to be put on the data bus (i.e., the converter must have its own unique address)

FIGURE 3. Interfacing to the SC/MP II Microprocessor

Typical Applications (Continued)

TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LED's to display the resulting digital output code as shown in *Figure 4*. Note that the LED drivers invert the digital output of the A/D converter to provide a binary display. A lab DVM can be used if a precision voltage source is not available. After adjusting the zero and full-scale, any number of points can be checked, as desired.

For ease of testing, a 10.24 V_{DC} reference is recommended for the A/D converter. This provides an LSB of 40 mV (10.240/256). To adjust the zero of the A/D, an analog input voltage of 1/2 LSB or 20 mV should be applied and the zero adjust potentiometer should be set to provide a flicker on the LSB LED readout with all the other display LEDs OFF.

To adjust the full-scale adjust potentiometer, an analog input which is 1 1/2 LSB less than the reference (10.240–0.060 or 10.180 V_{DC}) should be applied to the analog input and the full-scale adjusted for a flicker on the LSB LED, but this time with all the other LEDs ON.

A complete circuit for a simple A/D tester is shown in *Figure 5*. Note that the clock input voltage swing and the digital output voltage swings are from 0V to 10.24V. The MM74C901 provides a voltage translation to 5V operation and also the logic inversion so the readout LEDs are in binary.

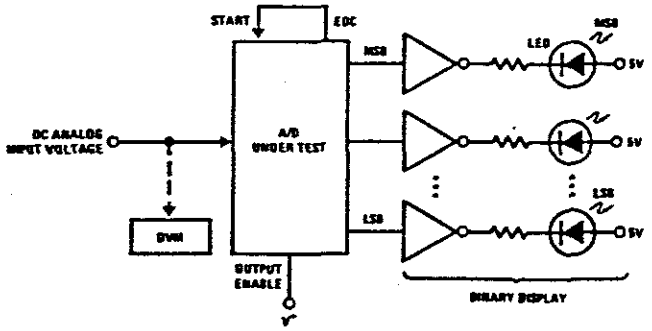


FIGURE 4. Basic A/D Tester

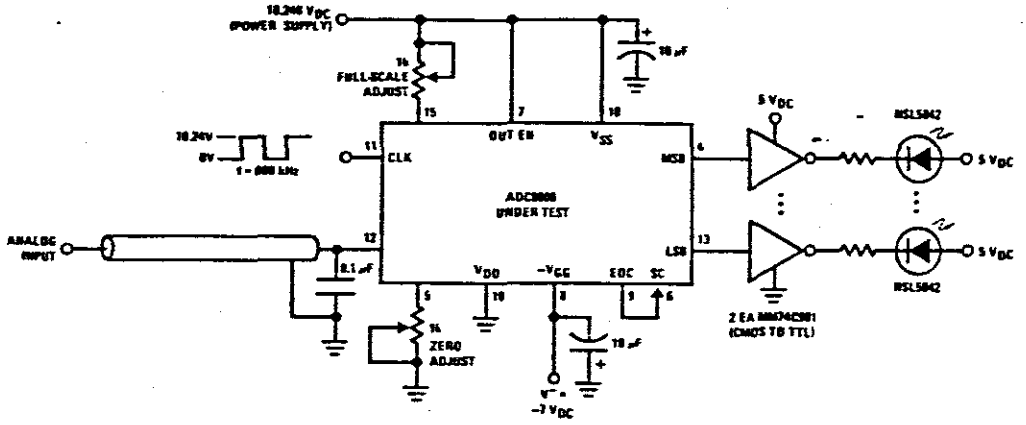


FIGURE 5. Complete Basic Tester Circuit

Typical Applications (Continued)

The digital output LED display can be decoded by dividing the 8 bits into the 4 most significant bits and 4 least significant bits. Table I shows the fractional binary equivalent of these two 8-bit groups. By adding the decoded voltages which are obtained from the column: "Input Voltage Value with a 10.240 V_{REF}" of both the MS and LS groups, the value of the digital display can be determined. For example, for an output LED display of "1011 0110" or "B6" (in hex) the voltage values from the table are 7.04 + 0.24 or 7.280 V_{DC}. These voltage values represent the center values of a perfect A/D converter. The input voltage has to change by ±1/2 LSB (±20 mV), the "quantization uncertainty" of an A/D, to obtain an output digital code change. The effects of this quantization error have to be accounted for in the interpretation of the test results. A plot of this natural error source is shown in *Figure 6* where, for clarity, both the analog input voltage and the error voltage are normalized to LSBs.

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY	FRACTIONAL BINARY VALUE FOR		INPUT VOLTAGE VALUE WITH 10.24 V_{REF}	
		MS GROUP	LS GROUP	MS GROUP	LS GROUP
F	1 1 1 1	15/16	15/256	9.600	0.600
E	1 1 1 0	7/8	7/128	8.960	0.560
D	1 1 0 1	13/16	13/256	8.320	0.520
C	1 1 0 0	3/4	3/64	7.680	0.480
B	1 0 1 1	11/16	11/256	7.040	0.440
A	1 0 1 0	5/8	5/128	6.400	0.400
9	1 0 0 1	9/16	9/256	5.760	0.360
8	1 0 0 0	1/2	1/32	5.120	0.320
7	0 1 1 1	7/16	7/256	4.480	0.280
6	0 1 1 0	3/8	3/128	3.840	0.240
5	0 1 0 1	5/16	5/256	3.200	0.200
4	0 1 0 0	1/4	1/64	2.560	0.160
3	0 0 1 1	3/16	3/256	1.920	0.120
2	0 0 1 0	1/8	1/128	1.280	0.080
1	0 0 0 1	1/16	1/256	0.640	0.040
0	0 0 0 0			0	0

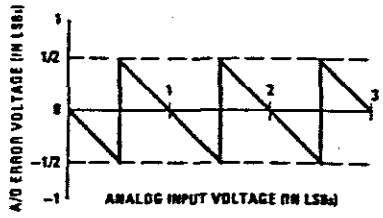


FIGURE 6. Error Plot of a Perfect A/D Showing Effects of Quantization Error

Typical Applications (Continued)

A low speed ramp generator can also be used to sweep the analog input voltage and the LED outputs will provide a binary counting sequence from zero to full-scale.

The techniques described so far are suitable for an engineering evaluation or a quick check on performance. For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be provided as either analog voltages or differences in two digital words.

A basic A/D tester which uses a DAC and provides the error as an analog output voltage is shown in *Figure 7*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to directly readout the difference voltage, "A–C". The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis). The construction details of a tester of this type are provided in the NSC application note AN-179, "Analog-to-Digital Converter Testing".

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 8* where the output code transitions can be detected as the 10-bit DAC is incremented. This provides 1/4 LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

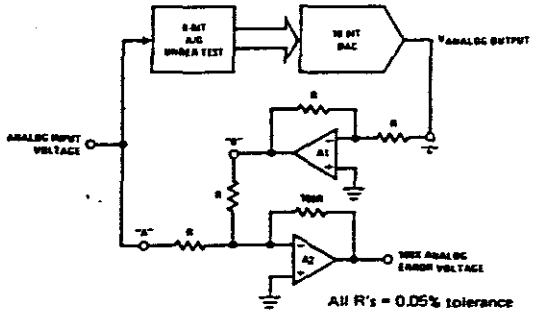


FIGURE 7. A/D Tester with Analog Error Output

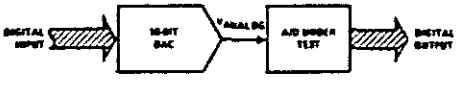
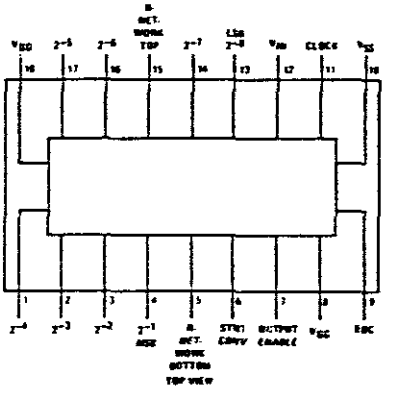


FIGURE 8. Basic "Digital" A/D Tester

Connection Diagram

Dual-In-Line Package



Order Number ADC0800PD (–55°C to +125°C)
or ADC0800PCD (0°C to +70°C)
See NS Package D18A

CHAPTER 6
MCS®-51 ARCHITECTURE

The major features of the 8051 are:

- 8-bit CPU
- on-chip oscillator
- 4K bytes of ROM
- 128 bytes of RAM
- 21 Special Function Registers
- 32 I/O lines
- 64K address space for external Data Memory
- 64K address space for external Program Memory
- two 16-bit timer/counters
- a five-source interrupt structure with two priority levels
- a full duplex serial port
- bit addressability for Boolean processing

The term "8051" is often used generically to refer to the 8051, the 8031, and the 8751. The 8031 is a ROM-less 8051; it fetches all instructions from external memory. The 8751 is an 8051 with EPROM instead of ROM.

A block diagram of the 8051 is shown in Figure 6-1. The pin-out is on the inside of the front cover of this manual.

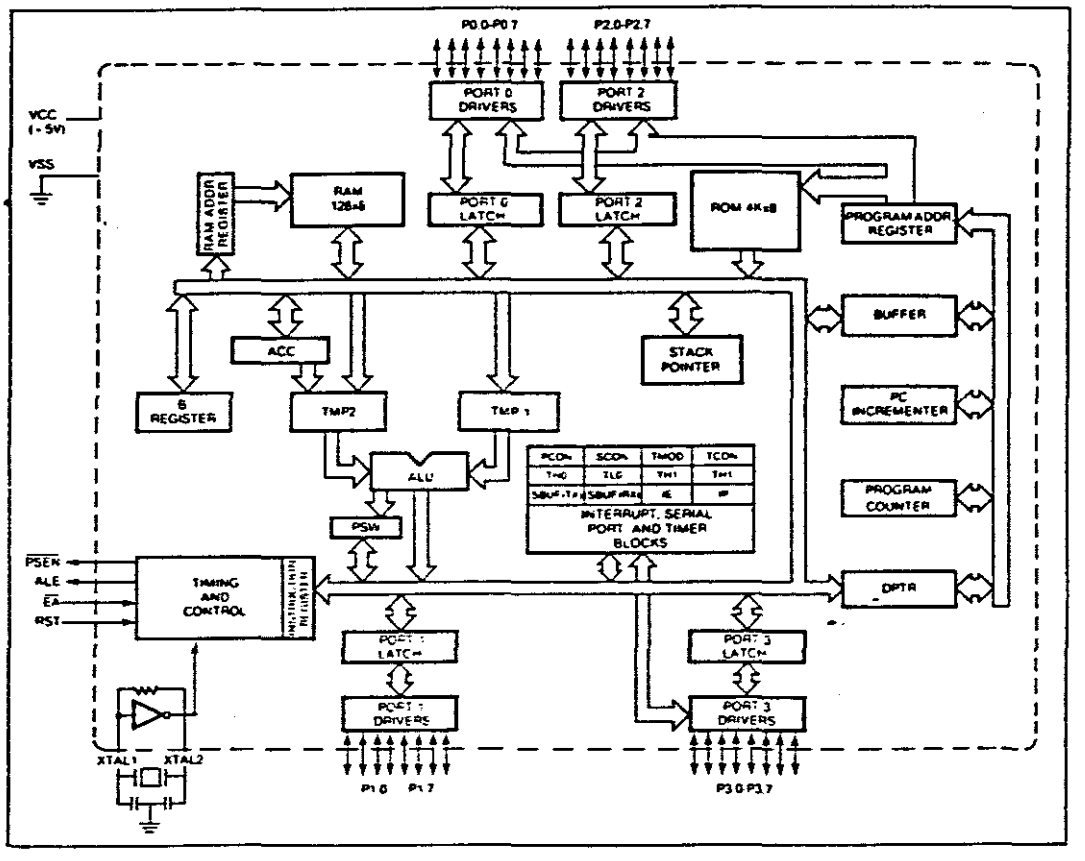


Figure 6-1. Block Diagram of the 8051

6.0 MEMORY ORGANIZATION

The 8051 maintains separate address spaces for Program Memory and Data Memory. The Program Memory can be up to 64K bytes long, of which the lowest 4K bytes are in the on-chip ROM.

If the $\overline{EA}$ pin is held high, the 8051 executes out of internal ROM unless the Program Counter exceeds 0FFFH. Fetches from locations 1000H through FFFFH are directed to external Program Memory.

If the $\overline{EA}$ pin is held low, the 8051 fetches all instructions from external Program Memory.

The Data Memory consists of 128 bytes of on-chip RAM, plus 21 Special Function Registers, in addition to which the device is capable of accessing up to 64K bytes of external data memory.

The Program Memory uses 16-bit addresses. The external Data Memory can use either 8-bit or 16-bit addresses. The internal Data Memory uses 8-bit addresses, which provide a 256-location address space. The lower 128 addresses access the on-chip RAM. The Special Function Registers occupy various locations in the upper 128 bytes of the same address space.

The lowest 32 bytes in the internal RAM (locations 00 through 1FH) are divided into 4 banks of registers, each bank consisting of 8 bytes. Any one of these banks can be selected to be the "working registers" of the CPU, and can be accessed by a 3-bit address in the same byte as the opcode of an instruction. Thus, a large number of instructions are one-byte instructions.

The next higher 16 bytes of the internal RAM (locations 20H through 2FH) have individually addressable bits. These are provided for use as software flags or for one-bit (Boolean) processing. This bit-addressing capability is an important feature of the 8051. In addition to the 128 individually addressable bits in RAM, eleven of the Special Function Registers also have individually addressable bits.

A memory map is shown in Figure 6-2.

6.1 SPECIAL FUNCTION REGISTERS

The Special Function Registers are as follows:

*	ACC	Accumulator
*	B	B Register
*	PSW	Program Status Word
	SP	Stack Pointer
	DPTR	Data Pointer (consisting of DPH AND DPL)
*	P0	Port 0
*	P1	Port 1
*	P2	Port 2
*	P3	Port 3
*	IP	Interrupt Priority
*	IE	Interrupt Enable
	TMOD	Timer/Counter Mode
*	TCON	Timer/Counter Control
	TH0	Timer/Counter 0 (high byte)
	TL0	Timer/Counter 0 (low byte)
	TH1	Timer/Counter 1 (high byte)
	TL1	Timer/Counter 1 (low byte)
*	SCON	Serial Control
	SBUF	Serial Data Buffer
	PCON	Power Control

The registers marked with * are both byte- and bit-addressable.

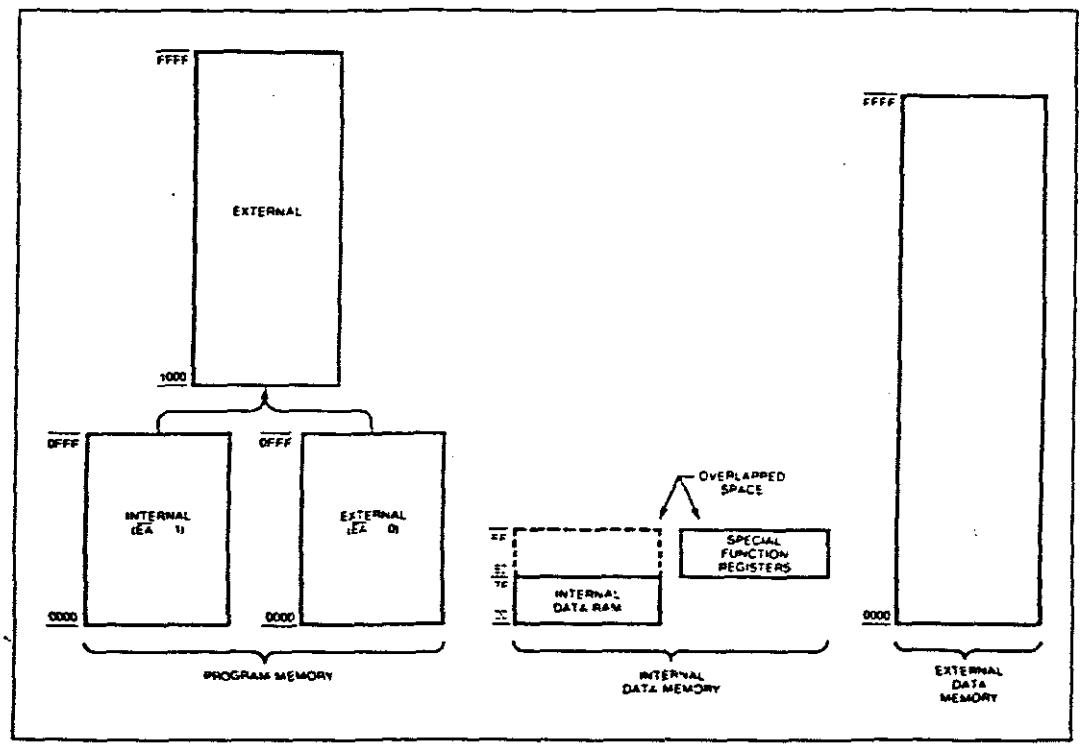


Figure 6-2. 8051 Memory Map

Accumulator

ACC is the Accumulator. The mnemonics for accumulator-specific instructions refer to the accumulator simply as A, but the register itself is named ACC.

B Register

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch register.

Stack Pointer

The Stack Pointer is 8 bits wide. The stack can reside anywhere in the 128 bytes of on-chip RAM. When the 8051 is reset, the stack pointer is initialized to 07H. When executing a PUSH or a CALL, the stack pointer is incremented before data is stored, so the stack would begin at location 08H.

Data Pointer

The Data Pointer (DPTR) is a 16-bit register, consisting of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address.

Ports 0 through 3

These four parallel ports provide the 32 I/O

lines. Each port consists of a latch (Special Function Registers P0 through P3), an output driver, and an input buffer.

The output drivers of Ports 0 and 2 and the input buffers of Port 0 are used in accesses to external memory. In this application, Port 0 outputs the low byte of the external memory address, time-multiplexed with the byte being written or read. Port 2, meanwhile, outputs the high byte of the external memory address.

The output drivers and input buffers of Port 3 are also multifunctional, as listed below:

Port Pin	*Alternate Function*
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt)
P3.3	$\overline{\text{INT1}}$ (external interrupt)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external Data Memory write strobe)
P3.7	$\overline{\text{RD}}$ (external Data Memory read strobe)

Serial Data Buffer

The Serial Buffer is actually two separate registers. When data is moved to SBUF, it goes to the transmit buffer where it is held for serial transmission. (Moving a byte to SBUF is what initiates the transmission.) When data is moved from SBUF, it comes from the receive buffer.

During serial reception the incoming bits are clocked into a separate shift register. When reception of a frame is complete, and if various other conditions are satisfied, 8 received data bits are transferred from the shift register to the receive buffer. The shift register is then ready to commence reception of a second frame, while the frame already received awaits servicing.

Control and Status Registers

Special Function Registers IP, IE, TMOD, TCON, SCON, and PCON contain control and status bits for the interrupt system, the timers, and the serial port. They will be fully described in the remaining sections of this chapter.

6.2 OSCILLATOR AND CLOCK CIRCUIT

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which is intended for use as a crystal oscillator, in the Pierce configuration, in the frequency range of 1.2MHz to 12MHz. XTAL2 is also the input to the internal clock generator.

To drive the chip with an external oscillator, one would ground XTAL1 and drive XTAL2. Since the input to the clock generator is a divide-by-two flip-flop, there are no requirements on the duty cycle of the external oscillator signal. However, minimum high and low times must be observed.

The clock generator divides the oscillator frequency by 2, and provides a two-phase clock signal to the chip. The Phase 1 signal is active during the first half of each clock period, and the Phase 2 signal is active during the second half of each clock period.

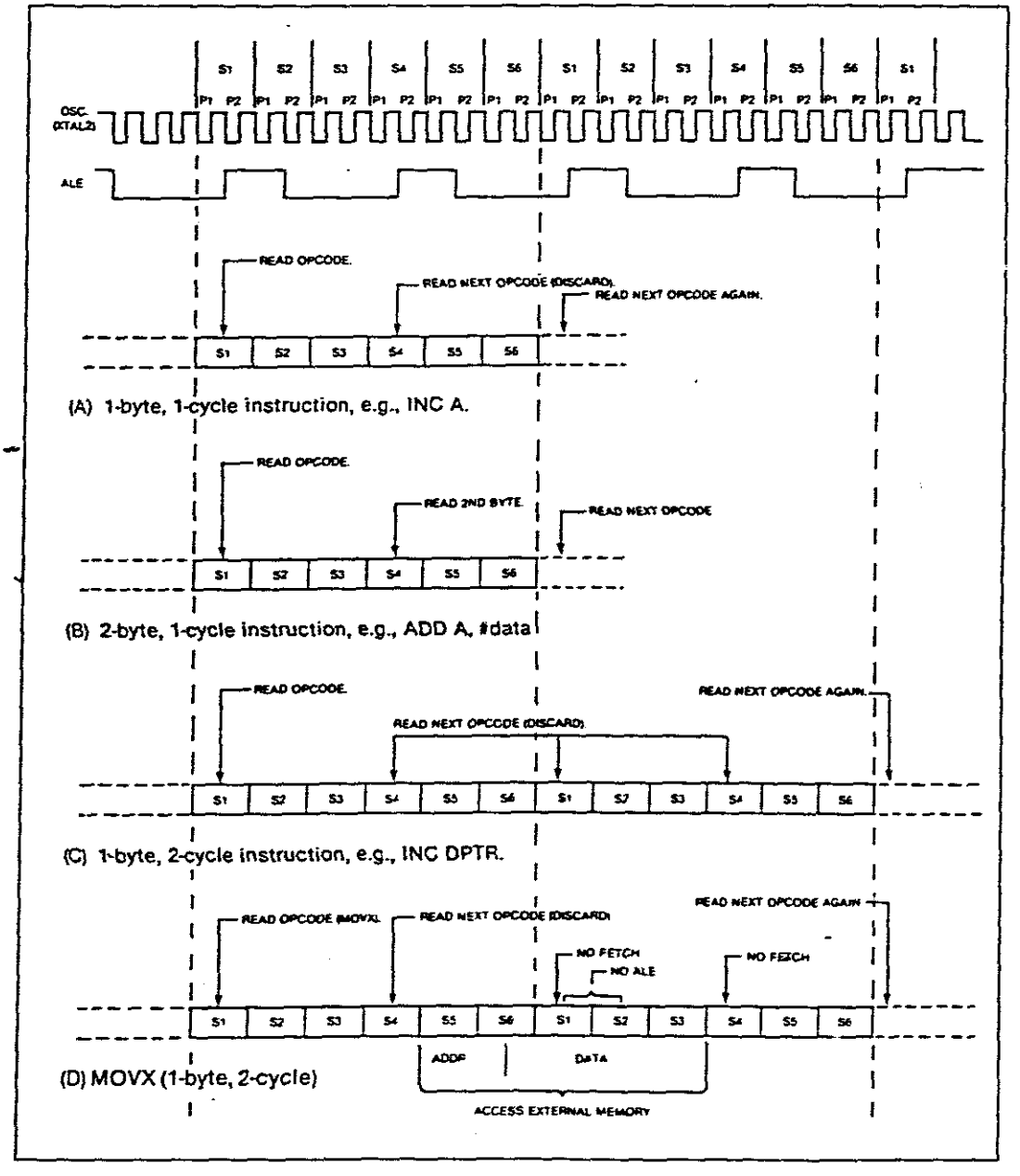


Figure 8.3. Fetch/Execute Sequences in the 8051

6.3 CPU TIMING

A machine cycle consists of 6 states (12 oscillator periods). Each state is divided into a Phase 1 half, during which the Phase 1 clock is active, and a Phase 2 half, during which the Phase 2 clock is active. Normally, arithmetic and logical operations take place during Phase 1 and internal register-to-register transfers take place during Phase 2.

The diagrams in Figure 6-3 show the fetch/execute timing referred to the internal states and phases. Since these internal clock signals are not externally observable, the XTAL2 oscillator signal and the ALE (Address Latch Enable) signal are shown for external reference. Thus a machine cycle consists of 12 oscillator periods, numbered S1P1 (State 1 Phase 1) through S6P2 (State 6 Phase 2). Each phase lasts for one oscillator period. Each state lasts for two oscillator periods. ALE is normally activated twice during each machine cycle: once during S1P2 and S2P1, and again during S4P2 and S5P1.

Execution of a one-cycle instruction begins at S1P2, when the opcode is latched into the Instruction Register. If it is a two-byte instruction, the second byte is read during S4 of the same machine cycle. If it is a one-byte instruction, there is still a read at S4, but the byte read (which would be the next opcode) is ignored, and the Program Counter is not incremented. In any case, execution is complete at the end of S6P2. Figures 6-3A and 6-3B show the timing for a 1-byte, 1-cycle instruction and for a 2-byte, 1-cycle instruction.

Most 8051 instructions execute in one cycle. MUL (multiply) and DIV (divide) are the only instructions that take more than two cycles to complete. They take four cycles.

Normally, two code bytes are fetched from Program Memory during every machine cycle. The only exception to that is when a MOVX instruction is executed. MOVX is a 1-byte, 2-cycle instruction that accesses external Data Memory. During a MOVX, two fetches are skipped while the external Data Memory is being addressed and strobed. Figures 6-3C and 6-3D show the timing for a normal 1-byte, 2-cycle instruction and for a MOVX instruction.

6.4 PORT OPERATION

All four ports in the 8051 are bidirectional. Ports 1, 2, and 3 have internal pull-ups. Port 0 has open-drain outputs. Figure 6-4 shows a functional diagram of a typical bit in each of the four ports.

Each I/O line can be independently used as an input or an output. For a line to be used as an input, the port latch must contain a 1, which turns off the output driver FET. Then, for Ports 1, 2, and 3, the pin is pulled high by the internal pull-up, but can be pulled low by an external source. For Port 0, a 1 in the port latch causes the output pin to float. All the port latches in the 8051 have 1s written to them by the reset function. If a 0 is subseqently written to a port latch, it can be reconfigured as an input if desired by writing a 1 to it.

Because Ports 1, 2, and 3 are pulled high when configured as inputs, they are sometimes called "quasi-bidirectional" ports. As inputs they can be driven in a normal manner by any TTL or MOS circuit. Because they do have the internal pull-ups, however, they can also be driven by open-collector or open-drain outputs without the need for additional external pull-ups.

Port 0 differs in not having internal pull-ups. The upper FET in the P0 output driver (see Figure 6-4A) is turned off except when the port is being used as an ADDR/DATA bus in accesses to external memory. Consequently, P0 lines that are being used as output ports have open-drain outputs. Writing a 1 to a P0 latch results in both output FETs being turned off, so the pin floats. In that condition it can be used as a high-impedance input.

Notice in Figure 6-4 that there are two ways to read a port: an instruction reads either the latch or the pin. In the 8051, some instructions read the latch and some read the pin. The instructions that read the latch rather than the pin are the ones that read a value, possibly change it, and then rewrite it to the latch. These are called "read-modify-write" instructions. The instructions listed below are read-modify-write instructions. When the destination operand is a port or a port bit, these instructions read the latch rather than the pin:

ANL	(logical AND, e.g., ANL P1, A)
ORL	(logical OR, e.g., ORL P2,A)
XRL	(logical EX-OR, e.g., XRL P3, A)

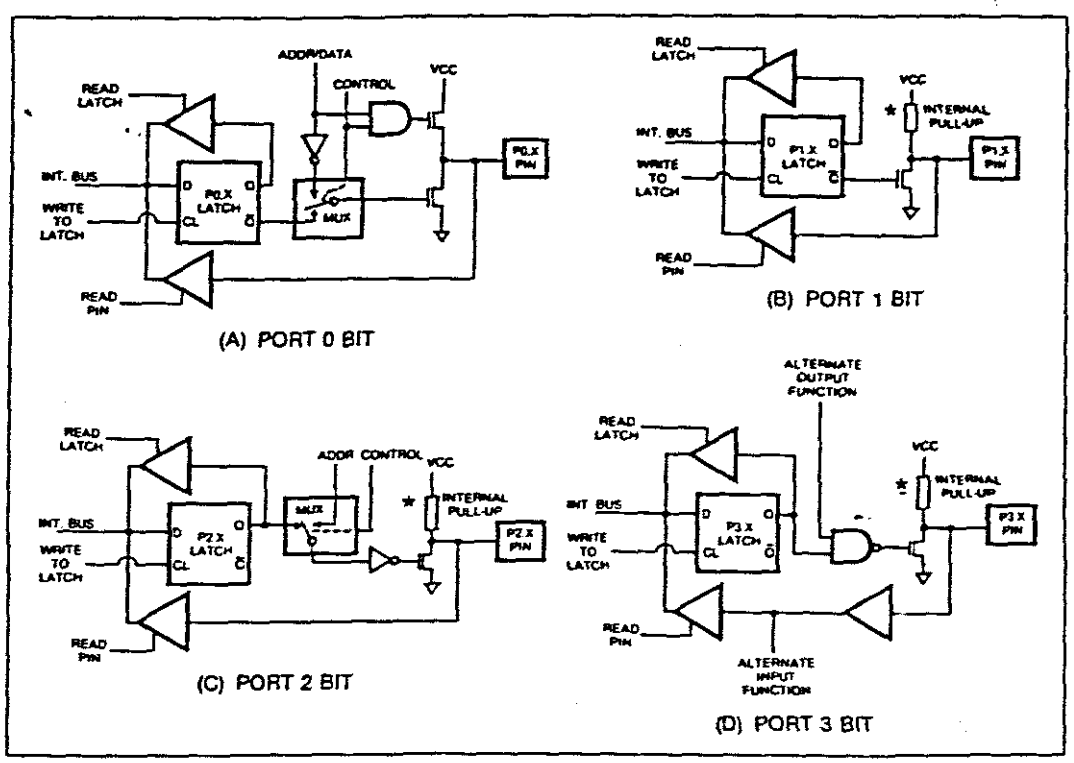


Figure 6-4. Port Latches and Buffers (*See Figure 6-5 for details of internal pullup).

JBC	(jump if bit = 1 and clear bit, e.g., JBC P1.1, LABEL)
CPL	(complement bit, e.g., CPL P3.0)
INC	(increment, e.g., INC P2)
DEC	(decrement, e.g., DEC P2)
DJNZ	(decrement and jump if not zero, e.g., DJNZ P3, LABEL)
MOV PX.Y,C	(move carry bit to bit Y of Port X)
CLR PX.Y	(clear bit Y of Port X)
SET PX.Y	(set bit Y of Port X)

It is not obvious that the last three instructions in this list are read-modify-write instructions, but they are. What they do is read the port byte, all 8 bits, modify the addressed bit, then write the new byte back to the latch.

The reason that read-modify-write instructions are directed to the latch rather than the pin is to avoid a possible misinterpretation of the voltage level at the pin. For example, a port bit might be used to drive the base of a transistor. One might write a 1 to it in order to turn the transistor on. If the CPU now reads the same port bit at the pin rather than the latch, it will read the base voltage of the transistor and interpret it as a 0. Reading the latch rather than the pin will return the correct value of 1. It is to avoid this type of problem that the 8051 directs read-modify-write instructions to the port latch rather than the port pin.

It can be seen in Figure 6-4D that each line in Port 3 is capable of performing an alternate input function and an alternate output function, not related to the port function. The bit latch must contain a 1, or else the port pin will be stuck at 0 regardless of which alternate function is trying to do what with it. The alternate functions that are implemented have already been listed, but the list is repeated here for convenience:

Port Pin	*Alternate Function*
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt)
P3.3	$\overline{\text{INT1}}$ (external interrupt)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external Data Memory write strobe)
P3.7	$\overline{\text{RD}}$ (external Data Memory read strobe)

6.4.1 Writing to a Port

In the execution of an instruction that changes the value in a port latch, the new value arrives at the latch during S6P2 of the final cycle of the instruction. However, port latches are in fact sampled by their output buffers only during Phase 1 of any clock period. (During Phase 2 the output buffer holds the value it saw during the previous Phase 1.) Consequently, the new value in the port latch won't actually appear at the output pin until the next Phase 1, which will be at S1P1 of the next machine cycle.

If the change requires a 0-to-1 transition in Port 1, 2, or 3, an additional pull-up is turned on during S1P1 and S1P2 of the cycle in which the transition occurs. This is done to increase the transition speed. The extra pull-up can source about 100 times the current that the normal pull-up can.

It should be noted that the internal pull-ups are field-effect transistors, not linear resistors. The pull-up arrangement is shown in Figure 6-5. The fixed part of the pull-up is a depletion-mode transistor with the gate wired to the source. If the port pin is shorted to ground, this transistor will allow about 0.25 mA (typical) to exit the pin. In parallel with the fixed pull-up is an enhancement-mode transistor which is activated during S1 whenever the port bit does a 0-to-1 transition. During this interval, if the port pin is shorted to ground, this extra transistor will allow an additional 30 mA (typical) to exit the pin.

6.4.2 Port Loading

The output buffers of Ports 1, 2, and 3 can drive 3 LS TTL inputs. The output buffers of Port 0 can each drive 8 LS TTL inputs.

Ports 1, 2, and 3 can drive any MOS input without the need for external pull-ups. Port 0 needs external pull-ups to drive MOS inputs, except when it's being used as an ADDRESS/DATA bus, in which case it can drive MOS inputs without external pull-ups.

6.5 ACCESSING EXTERNAL MEMORY

Accesses to external memory are of two types: accesses to external Program Memory and accesses to external Data Memory. Accesses to external Program Memory use signal $\overline{PSEN}$ (program store enable) as the read strobe. Accesses to external Data Memory use $\overline{RD}$ or $\overline{WR}$ (alternate functions of P3.7 and P3.6) to strobe the memory.

Fetches from external Program Memory always use a 16-bit address. Accesses to external Data Memory can use either a 16-bit address (MOVX @DPTR) or an 8-bit address (MOVX @Ri).

Whenever a 16-bit address is used, the high byte of the address comes out on Port 2, where it is held for the duration of the read or write cycle. During this time the Port 2 latch (the

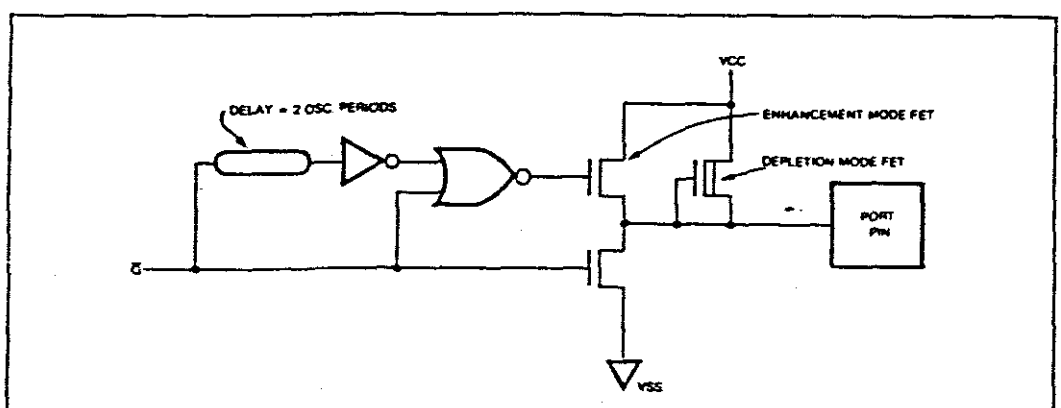


Figure 6-5. Internal Pull-Ups. The enhancement mode transistor is turned on for 2 osc. periods whenever $\overline{Q}$ makes a 1-to-0 transition.

Special Function Register) does not have to contain 1s, and the contents of the Port 2 SFR are not modified. If the external memory cycle is not immediately followed by another external memory cycle, the undisturbed contents of the Port 2 SFR will reappear shortly after the read or write strobe is deactivated.

If an 8-bit address is being used (MOVX @Ri), the contents of the Port 2 SFR remain at the Port 2 pins throughout the external memory cycle. This will facilitate paging.

In any case, the low byte of the address is time-multiplexed with the data byte on Port 0. The ADDR/DATA signal drives both FETs in the Port 0 output buffers. Thus in this application the Port 0 pins are not open-drain outputs, and they don't need external pull-ups. Signal ALE (address latch enable) should be used to capture the address byte into an external latch. The address byte is valid at the negative transition of ALE. Then, in a write cycle, the data byte to be written appears on Port 0 just before $\overline{WR}$ is activated, and remains there until after $\overline{WR}$ is deactivated. In a read cycle, the incoming byte is accepted at Port 0 just before the read strobe is deactivated.

During any access to external memory, the CPU writes 0FFH to the Port 0 latch (the Special Function Register), thus obliterating whatever information the Port 0 SFR may have been holding.

MORE ABOUT ACCESSING EXTERNAL PROGRAM MEMORY

External Program Memory is accessed under two conditions:

1) Whenever the program counter (PC) contains a number that is larger than 0FFFH;
2) Whenever signal $\overline{EA}$ is active, regardless of the contents of PC.

The 8031 is an 8051 that doesn't have internal Program Memory. $\overline{EA}$ must be externally wired to low on the 8031 to enable it to fetch the lower 4K program bytes from external memory.

When the CPU is executing out of external Program Memory, all 8 bits of Port 2 are dedicated to an output function: During external program fetches they output the high byte of the PC, and during accesses to external Data Memory they output either DPH or the Port 2 SFR (depending on whether the external Data Memory access is a MOVX @DPTR or a MOVX @Ri).

The read strobe for external fetches is $\overline{PSEN}$. $\overline{PSEN}$ is not activated for internal fetches. When the CPU is accessing external Program Memory, $\overline{PSEN}$ is activated twice every cycle (except during a MOVX instruction) whether or not the byte fetched is actually needed for the current instruction. When $\overline{PSEN}$ is activated its timing is not the same as $\overline{RD}$. A complete $\overline{RD}$ cycle, including activation and deactivation of ALE and $\overline{RD}$, takes 12 oscillator periods. A complete $\overline{PSEN}$ cycle, including activation and deactivation of ALE and $\overline{PSEN}$, takes 6 oscillator periods. The execution sequence for these two types of read cycles are shown in Figure 6-6 for comparison.

OVERLAPPING PROGRAM AND DATA MEMORY SPACES

In some applications it is desirable to execute a program from the same physical memory that is being used to store data. In the 8051 the external Program and Data Memory spaces can

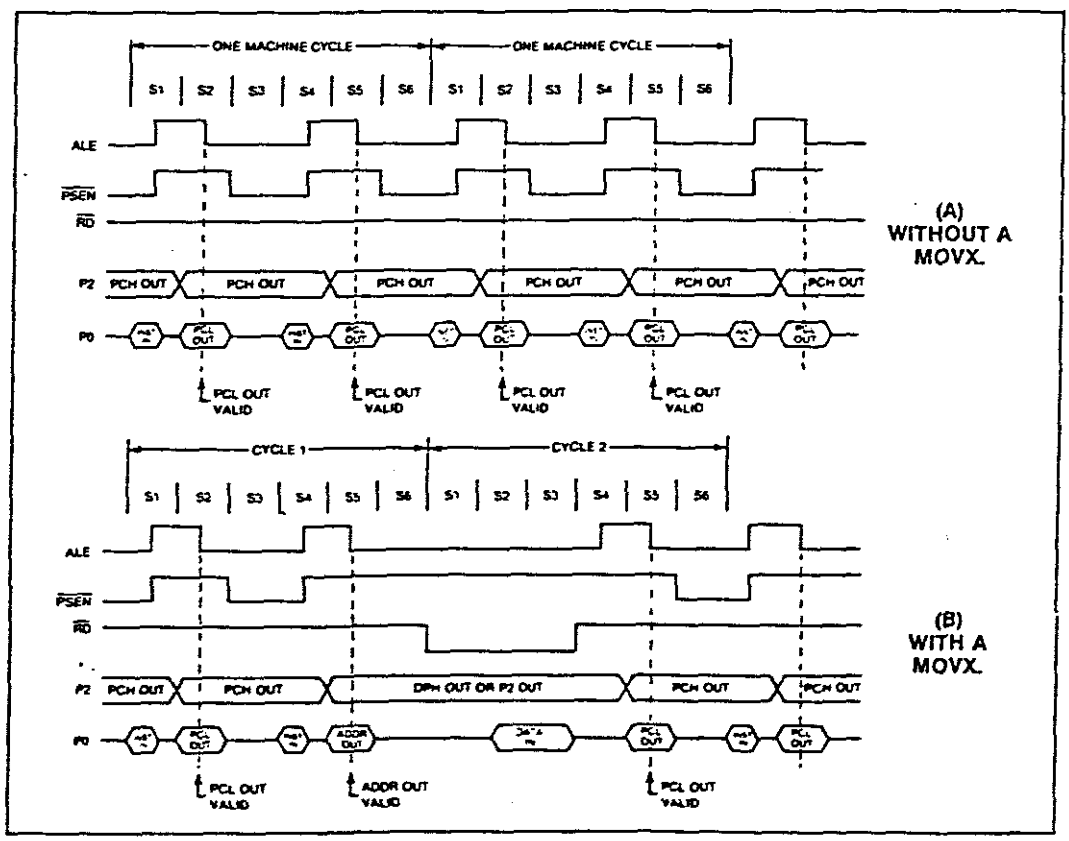


Figure 6-6. Executing Out of External Program Memory (Detailed timing diagrams are in the data sheets.)

be combined by ANDing $\overline{PSEN}$ and $\overline{RD}$. A positive-logic AND of these two signals produces an active-low read strobe that can be used for the combined physical memory. Since the $\overline{PSEN}$ cycle is faster than the $\overline{RD}$ cycle, the external memory needs to be fast enough to accommodate the $\overline{PSEN}$ cycle.

MORE ABOUT ALE

The main function of ALE is to provide a properly timed signal to latch the low byte of an address from P0 to an external latch during fetches from external Program Memory. For that purpose ALE is activated twice every machine cycle. This activation takes place even when the cycle involves no external fetch. The only time an ALE pulse doesn't come out is during an access to external Data Memory. The first ALE of the second cycle of a MOVX instruction is missing (see Figure 6-6). Consequently, in any system that does not use external Data Memory, ALE is activated at a constant rate of 1/6 the oscillator freqency, and can be used for external clocking or timing purposes.

6.6 TIMERS

The 8051 provides two 16-bit registers, Timer 0 and Timer 1, that can be used as timers or event counters. For each timer/counter register there is a control bit in Special Function Register TMOD that selects the timer/counter function to be "timer" or "counter."

In the "timer" function the register is incremented every machine cycle. Thus one can think of it as counting machine cycles. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the "counter" function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should hold for at least one full machine cycle.

In addition to the "timer" or "counter" selection, each timer/counter has four operating modes from which to select. These modes are functionally illustrated in Figure 6-7. Operating modes 0, 1, and 2 are the same for both timer/counters. Mode 3 is different. The four operating modes are described below.

MODE 0

Putting either Timer into mode 0 makes it look like an 8048 Timer, which is an 8-bit counter with a divide-by-32 prescaler. Figure 6-7A shows the mode 0 operation as it applies to Timer 1.

In this mode the Timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the Timer interrupt flag TF1. The counted input is enabled to the Timer when TR1 = 1 and either GATE = 0 or $\overline{INT1}$ = 1. (Setting GATE = 1 allows the Timer to be controlled by external input $\overline{INT1}$, to facilitate pulse width measurements.) TR1 is a control bit in Special Function Register TCON. GATE is a control bit in Special Function Register TMOD.

The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate and should be ignored. Setting the run flag (TR1) does not clear the registers.

Mode 0 operation is the same for Timer 0 as for Timer 1. Substitute TR0, TF0, and $\overline{INT0}$ for the corresponding Timer 1 signals in Figure 6-7A. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

MODE 1

Mode 1 is the same as Mode 0, except that the Timer register is being run with all 16 bits.

MODE 2

Mode 2 configures the Timer register as an 8-bit counter (TL1) with automatic reload. Overflow from TL1 not only sets TF1 but also reloads TL1 with the contents of TH1, which is preset by software to any desired one-byte

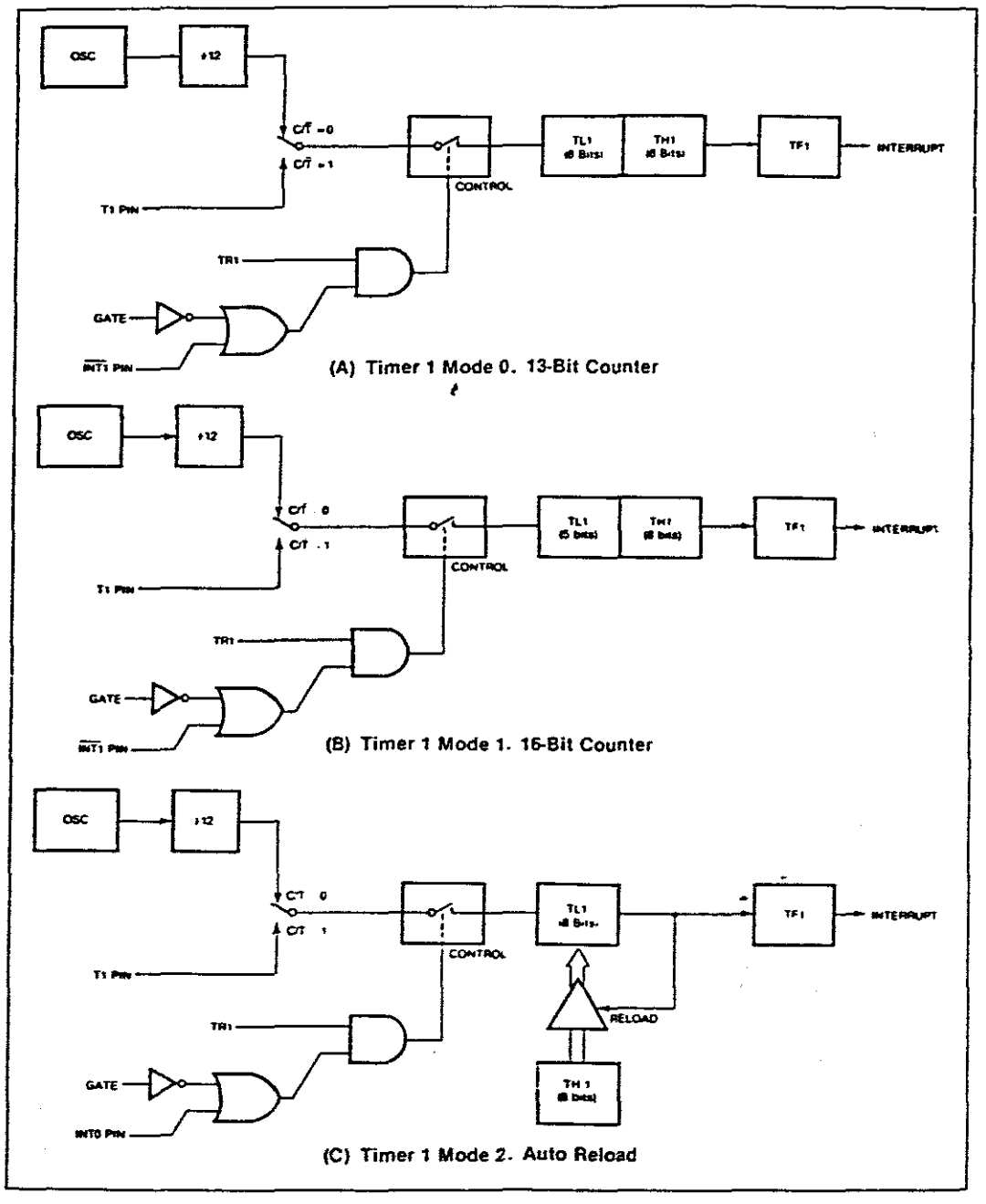
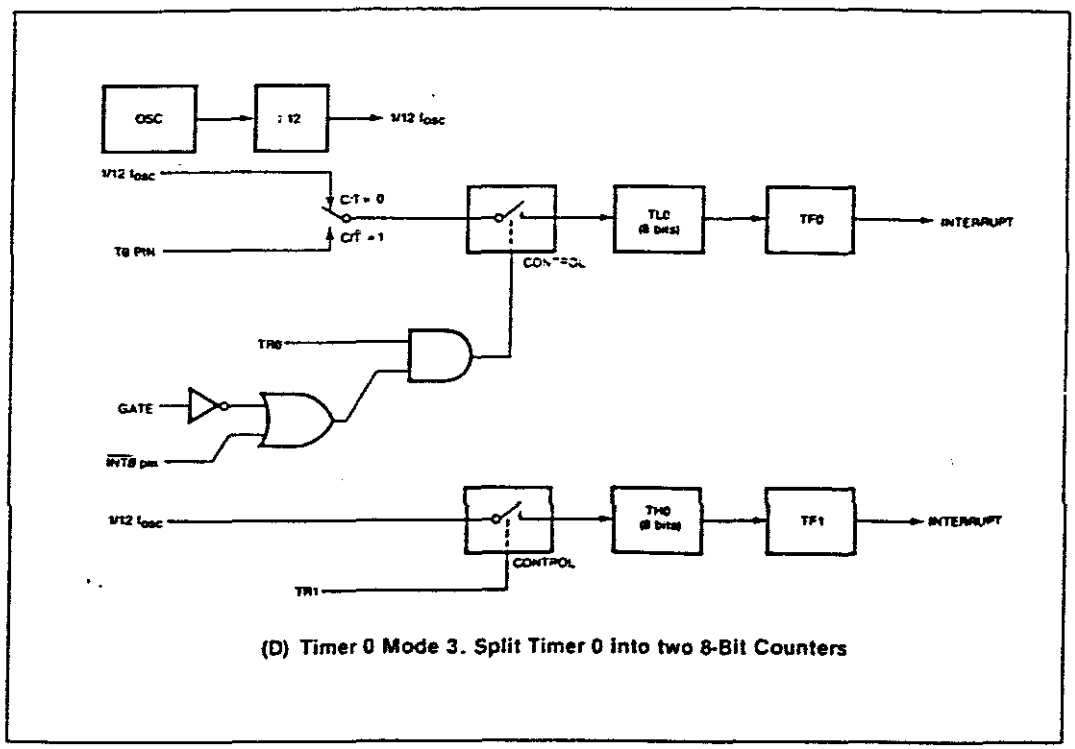

OSC
÷12
C/T = 0
C/T = 1
T1 PIN
CONTROL
TL1
8 Bits
TH1
8 Bits
TF1
INTERRUPT
TR1
GATE
INT1 PIN
(A) Timer 1 Mode 0. 13-Bit Counter
OSC
÷12
C/T 0
C/T 1
T1 PIN
CONTROL
TL1
(8 bits)
TH1
(8 bits)
TF1
INTERRUPT
TR1
GATE
INT1 PIN
(B) Timer 1 Mode 1. 16-Bit Counter
OSC
÷12
C/T 0
C/T 1
T1 PIN
CONTROL
TL1
8 Bits
TF1
INTERRUPT
RELOAD
TR1
GATE
INT0 PIN
TH 1
8 bits
(C) Timer 1 Mode 2. Auto Reload

Figure 6-7



(D) Timer 0 Mode 3. Split Timer 0 into two 8-Bit Counters

Figure 6-7 (continued)

value. The reload leaves TH1 unchanged.

Mode 2 operation is the same for Timer 0.

MODE 3

If you put Timer 1 into Mode 3, it holds its count. The effect is the same as setting TR1 = 0.

If you put Timer 0 into Mode 3, TL0 and TH0 become two separate counters. The logic for Mode 3 on Timer 0 is shown in Figure 6-7D. Note that TL0 is using all of the Timer 0 control bits: C/$\overline{T}$, GATE, TR0, $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and has taken over the use of TR1 and TF1 from Timer 1. (Thus TH0 now controls the "Timer 1" interrupt.)

Normally one would not put Timer 0 into Mode 3 unless Timer 1 were already in use as a baud rate generator for the serial port. Mode 3 is provided specifically for applications in which two independent timer/counters plus the serial port are required. One would set up Timer 1 as the baud rate generator (Mode 2), and operate Timer 0 in Mode 3.

6.6.1 Timer Control and Status Registers

Two Special Function Registers, TMOD and

TCON, are used to define the operating modes and control the functions of the timer/counters. When an instruction changes the content of TMOD or TCON, the change is latched into the SFR and takes effect at S1P1 of the next instruction's first cycle. The registers are shown below.

TMOD: Timer Mode Control Register

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
	/---- Timer 1 ----/				/------ Timer 0 ------/			

where M1, M0 specify the Mode, as follows:

M1	*M0*	*Mode*	*Description*
0	0	0	13-bit counter
0	1	1	16-bit counter
1	0	2	8-bit counter with auto reload
1	1	3	split Timer 0 into two 8-bit counters or stop Timer 1

- C/T selects "counter" or "timer" function. Set for "counter" function (count negative transitions at T0 or T1 pin). Clear for "timer" function (count machine cycles).
- GATE is Gating Control. When set, Timer "x" is enabled only while $\overline{INTx}$ pin is high and TRx bit is set. When cleared, Timer "x" is enabled whenever TRx bit is set.

Note: All bits of TMOD are cleared by reset.

TCON: Timer Control Register

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

where

- TF1 is the Timer 1 overflow interrupt flag. Set by hardware when Timer 1 overflows. Cleared by hardware when the processor transfers control to the interrupt service routine.
- TR1 is the Timer 1 run control bit. Set/cleared by software to turn Timer 1 on/off.
- TF0 is the Timer 0 overflow interrupt flag. Set by hardware when Timer 0 overflows. Cleared by hardware when the processor transfers control to the interrupt service routine.
- TR0 is the Timer 0 run control bit. Set/cleared by software to turn Timer 0 on/off.
- IE1 is the external interrupt 1 edge flag. If IT1 = 1, this bit is set by hardware when $\overline{INT1}$ is detected to have made a 1-to-0 transition. Cleared by hardware when the processor transfers control to the interrupt service routine.
- IT1 determines whether external interrupt 1 is edge-triggered or level-triggered. If IT1 = 1, external interrupt 1 is edge-triggered. If IT1 = 0, external interrupt is triggered by a detected low at $\overline{INT1}$ rather than a 1 in IE1.
- IE0 is the external interrupt 0 edge flag. If IT0 = 1, this bit is set by hardware when $\overline{INT0}$ is detected to

have made a 1-to-0 transition. Cleared by hardware when the processor transfers control to the interrupt service routine.

- IT0 determines whether external interrupt 0 is edge-triggered or level-triggered. If IT0 = 1, external interrupt 0 is edge-triggered. If IT0 = 0, external interrupt 0 is triggered by a detected low at $\overline{INT0}$ rather than a 1 in IE0.

Bits IE1 through IT0 have to do with the external interrupts, and are more fully discussed in the section dealing with the interrupt structure.

Note: All bits of TCON are cleared by reset.

6.7 SERIAL INTERFACE

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. (However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost.) The serial port registers are both accessed at Special Function Register SBUF. A write to SBUF loads the transmit register, and a read accesses a physically separate receive register.

The serial port can operate in 4 modes:

Mode 0: Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/12 the oscillator frequency.

Mode 1: 10 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in Special Function Register SCON. The baud rate is variable.

Mode 2: 11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8) can be assigned the value of 0 or 1. With nominal software overhead, TB8 can be made a parity bit, as shown in Figure 6-8. On receive, the 9th data bit goes into RB8 in Special Function Register SCON, and the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency.

```
MOV C,P      ; Parity moved to carry (byte
               already in A)
MOV TB8, C   ; Put carry into Transmit
               Bit 8
MOV SBUF, A  ; Load Transmit Register
```

Figure 6-8. Generating Parity and Initiating a Transmission

Mode 3: 11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except the baud rate. The baud rate in Mode 3 is variable.

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes 9 data bits are received. The 9th one goes into RB8. Then comes a stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. The way to use this feature in multiprocessor systems is as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. The slaves that weren't addressed leave their SM2s set and go on about their business, ignoring the coming data bytes.

SM2 should be cleared for operation in Mode 0 or 1.

6.7.1 Baud Rates

The baud rate in Mode 0 is fixed at 1/12 the oscillator frequency. The baud rate in Mode 2 is either 1/64 or 1/32 of the oscillator frequency, depending on the value of bit SMOD in Special Function Register PCON. If SMOD = 0 (which is its value on reset), the baud rate is 1/64 the oscillator frequency. If SMOD = 1, the baud rate is 1/32 of the oscillator frequency.

Baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate, as shown below:

Baud Rate = (Timer 1 overflow rate) /n

where n is an integer whose value is either 32 or 16, depending on the value of bit SMOD in Special Function Register PCON. If SMOD = 0 (which is its value on reset), n = 32. If SMOD = 1, n = 16. Timer 1 can be configured in any mode. The Timer 1 overflow rate is determined by its count rate and how many counts it takes to reach overflow.

For example, Timer 1 can be configured in the auto reload mode (TMOD.5 = 1, TMOD.4 = 0). The Timer must be running (TCON.6 = 1), and to keep the overflows from generating unnecessary interrupts the Timer 1 interrupt should be disabled (IE.3 = 0). Then the overflow rate depends on the reload value in TH1, as follows:

Overflow Rate = (count rate)/[256-(TH1)]

For very low baud rates one might select the 16-bit Timer 1 mode (TMOD.5 = 0, TMOD.4 = 1), and use the Timer 1 interrupt to do a software reload. In this case one would want to have the Timer 1 interrupt enabled (IE.3 = 1).

In any case, if Timer 1 is running with bit $C/\overline{T}$ = 0, the count rate is 1/12 the oscillator frequency. If the timer is running with $C/\overline{T}$ = 1, the count rate is the external input frequency, whose maximum usable value is 1/24 the oscillator frequency.

Figure 6-9 lists various commonly used baud rates and how they can be obtained in the 8051.

			TIMER 1		
BAUD RATE	f_{OSC}	SMOD	C/T	MODE	RELOAD VALUE
MODE 0 MAX: 1MHZ	12 MHZ	X	X	X	X
MODE 2 MAX: 375K	12 MHZ	1	X	X	X
MODES 1,3: 62.5K	12 MHZ	1	0	2	FFH
19.2K	11.059 MHZ	1	0	2	FDH
9.6K	11.059 MHZ	0	0	2	FDH
4.8K	11.059 MHZ	0	0	2	FAH
2.4K	11.059 MHZ	0	0	2	F4H
1.2K	11.059 MHZ	0	0	2	E8H
137.5	11.986 MHZ	0	0	2	1DH
110	6MHZ	0	0	2	72H
110	12 MHZ	0	0	1	FEEBH

Figure 6-9. Commonly Used Baud Rates

6.7.2 Baud Rate Bit in PCON

PCON is a Special Function Register (address = 87H) which has been added to the 8051 to implement certain Power Control options in the CMOS version of the chip. In the HMOS chip all the bits in PCON are dummy except bit 7, which is SMOD. SMOD is used in both the HMOS and CMOS versions to double the baud rate in modes 1, 2, and 3. PCON is not bit-addressable.

The reset value of SMOD is 0. Writing a 1 to SMOD (MOV PCON, #80H or MOV 87H, #80H) doubles the baud rate in modes 1, 2, and 3.

6.7.3 Serial Port Control Register

Special Function Register SCON is used to define the operating mode and control certain functions of the serial port. It also receives the 9th data bit (RB8), and contains the transmit and receive interrupt flags (TI and RI). The register is as shown below:

SCON: Serial Port Control Register

Bit:	7	6	5	4	3	2	1	0
	SM0	SM1	SM2	REN	TB8	RB8	TI	RI

where SM0, SM1 specify the serial port mode, as follows:

SM0	*SM1*	*Mode*	*Description*	*Baud Rate*
0	0	0	shift register	$f_{osc.}/12$
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	$f_{osc.}/64$ or $f_{osc.}/32$
1	1	3	9-bit UART	variable

- SM2 enables the multiprocessor communication feature in modes 2 and 3. In mode 2 or 3, if SM2 is set to 1 then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1 then RI will not be activated if a valid stop bit was not received. In mode 0, SM2 should be 0.
- REN enables serial reception. Set by software to enable reception. Clear by software to disable reception.
- TB8 is the 9th data bit that will be transmitted in modes 2 and 3. Set or clear by software as desired.
- RB8 in modes 2 and 3, is the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0, RB8 is not used.
- TI is transmit interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
- RI is receive interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Note: All bits of SCON are cleared by reset.

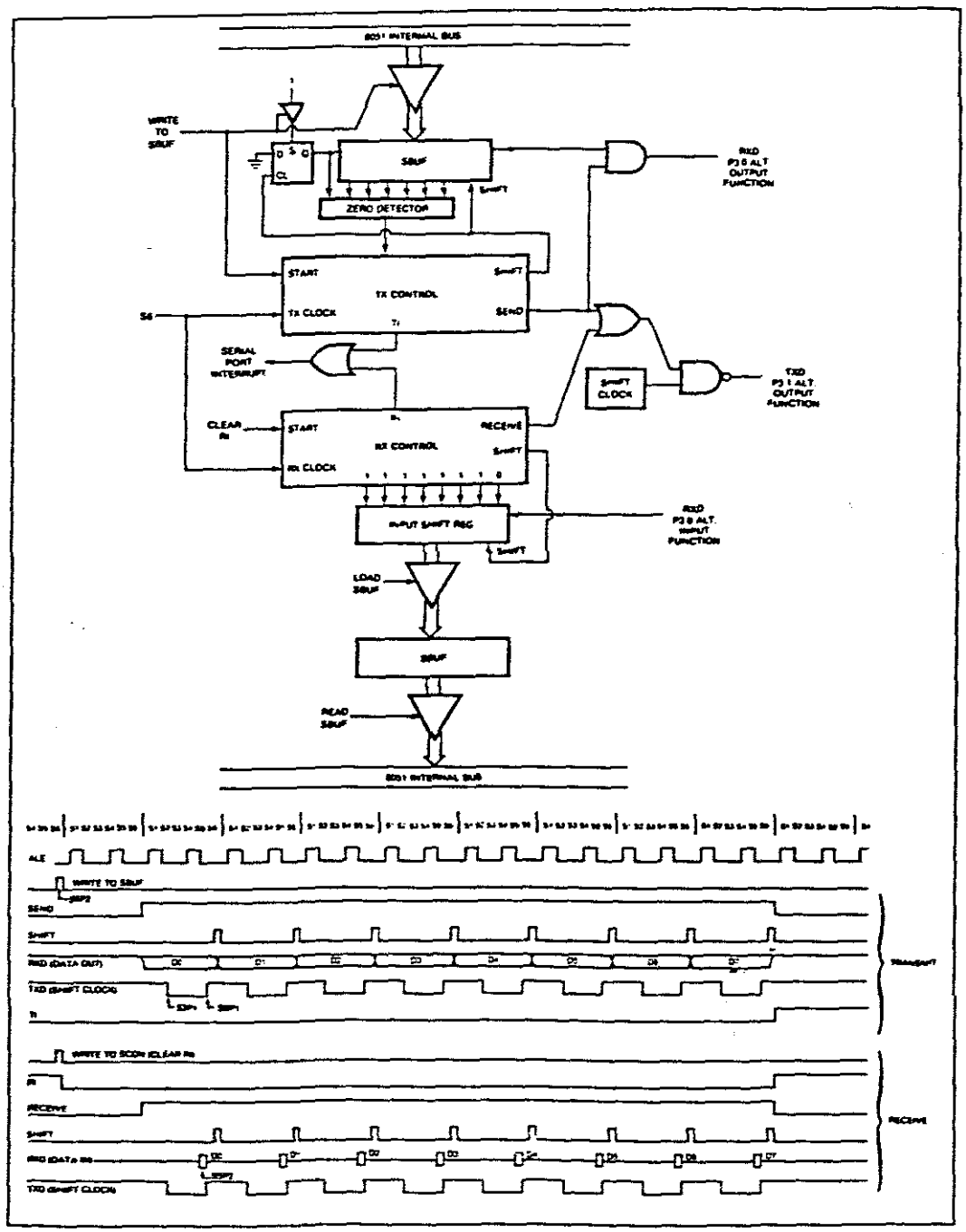


Figure 6-10. Serial Port in Mode 0

register, then the 1 that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain zeroes. This condition flags the TX Control block to do one last shift and then deactivate SEND and set TI. Both of these actions occur at S1P1 of the 10th machine cycle after "write to SBUF."

Reception is initiated by clearing RI, provided REN = 1. At S6P2 of the next machine cycle the RX Control unit writes the bits 11111110 to the receive shift register, and in the next clock phase activates RECEIVE.

RECEIVE enables SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK makes transitions at S3P1 and S6P1 of every machine cycle. At S6P2 of every machine cycle in which RECEIVE is active, the contents of the receive shift register are shifted to the left one position. The value that comes in from the right is the value that was sampled at the P3.0 pin at S5P2 of the same machine cycle.

As data bits come in from the right, 1s shift out to the left. When the 0 that was initially loaded into the rightmost position arrives at the leftmost position in the shift register, it flags the RX Control block to do one last shift and load SBUF. At S1P1 of the 10th machine cycle after the write to SCON that cleared RI, RECEIVE is cleared and RI is set.

Mode 0 Applications: Mode 0 was intended primarily for I/O expansion using CMOS or TTL shift registers, as shown in Figure 6-11.

6.7.6 More About Mode 1

Ten bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in SCON. The baud rate is determined by the Timer 1 overflow rate.

Figure 6-12 shows a somewhat simplified functional diagram of the serial port in Mode 1, and associated timing diagrams for transmit and receive.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal also loads a 1 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission actually commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus the bit times are synchronized to the divide-by-16 counter, not to the "write to SBUF" signal.)

The transmission begins with activation of $\overline{\text{SEND}}$, which puts the start bit at TXD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TXD. The first shift pulse occurs one bit time after that.

As data bits shift out to the right, zeroes are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain zeroes. This condition flags the TX Control unit to do one last shift and then deactivate $\overline{\text{SEND}}$ and set TI. This occurs at the 10th divide-by-16 rollover after "write to SBUF."

Reception is initiated by a detected 1-to-0 transition at RXD. For this purpose RXD is sam-

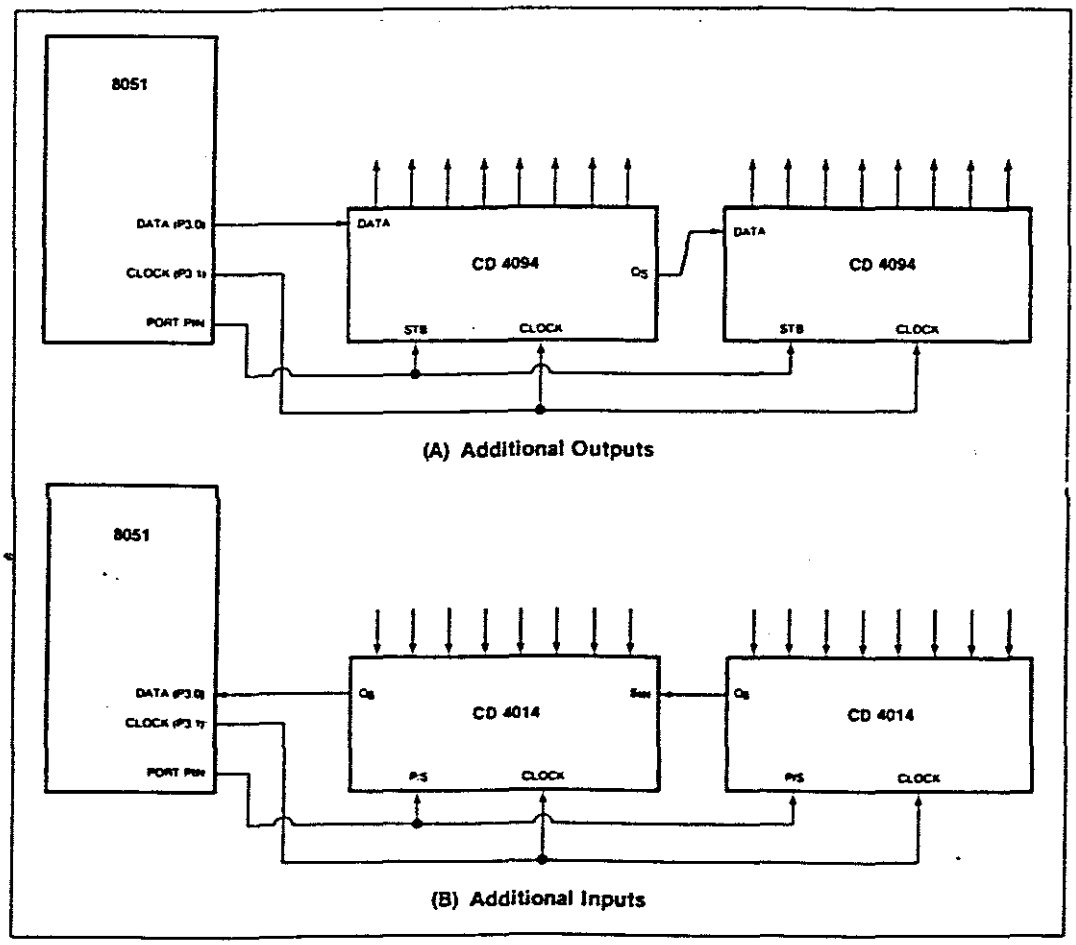


Figure 6-11. Mode 0 Applications

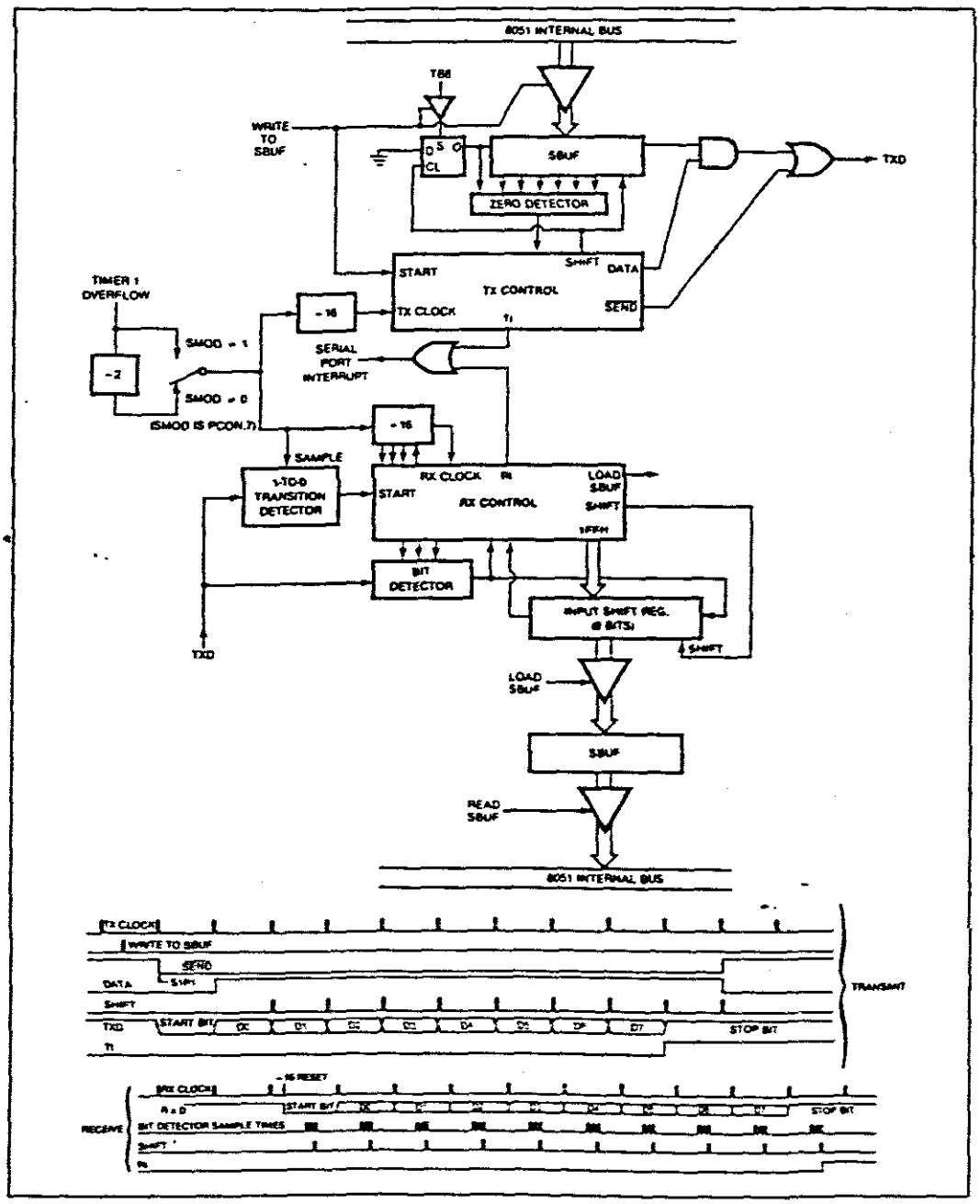


Figure 6-12. Serial Port in Mode 1

pled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written into the input shift register. Resetting the divide-by-16 counter aligns its rollovers with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in mode 1 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8, and to set RI, will be generated if and only if the following conditions are met at the time the final shift pulse is generated:

1) RI = 0, and
2) Either SM2 = 0 or the received stop bit = 1

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated. At this time, whether the above conditions are met or not, the unit goes back to looking for a 1-to-0 transition in RXD.

6.7.7 More About Modes 2 and 3

Eleven bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8) can be assigned the value of 0 or 1. On receive, the 9th data bit goes into RB8 in SCON. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency in mode 2 and is variable in mode 3.

Figure 6-13 shows a simplified functional diagram of the serial port in modes 2 and 3. The receive portion is exactly the same as in mode 1. The transmit portion differs from mode 1 only in the 9th bit of the transmit shift register.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal also loads TB8 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus the bit times are synchronized to the divide-by-16 counter, not to the "write to SBUF" signal.)

The transmission begins with activation of $\overline{\text{SEND}}$, which puts the start bit at TXD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TXD. The first shift pulse occurs one bit time after that. The first shift clocks a 1 (the stop bit) into the 9th bit position of the shift register. Thereafter, only zeroes are clocked in.

Thus as data bits shift out to the right, zeroes are clocked in from the left. When TB8 is at the output position of the shift register, then

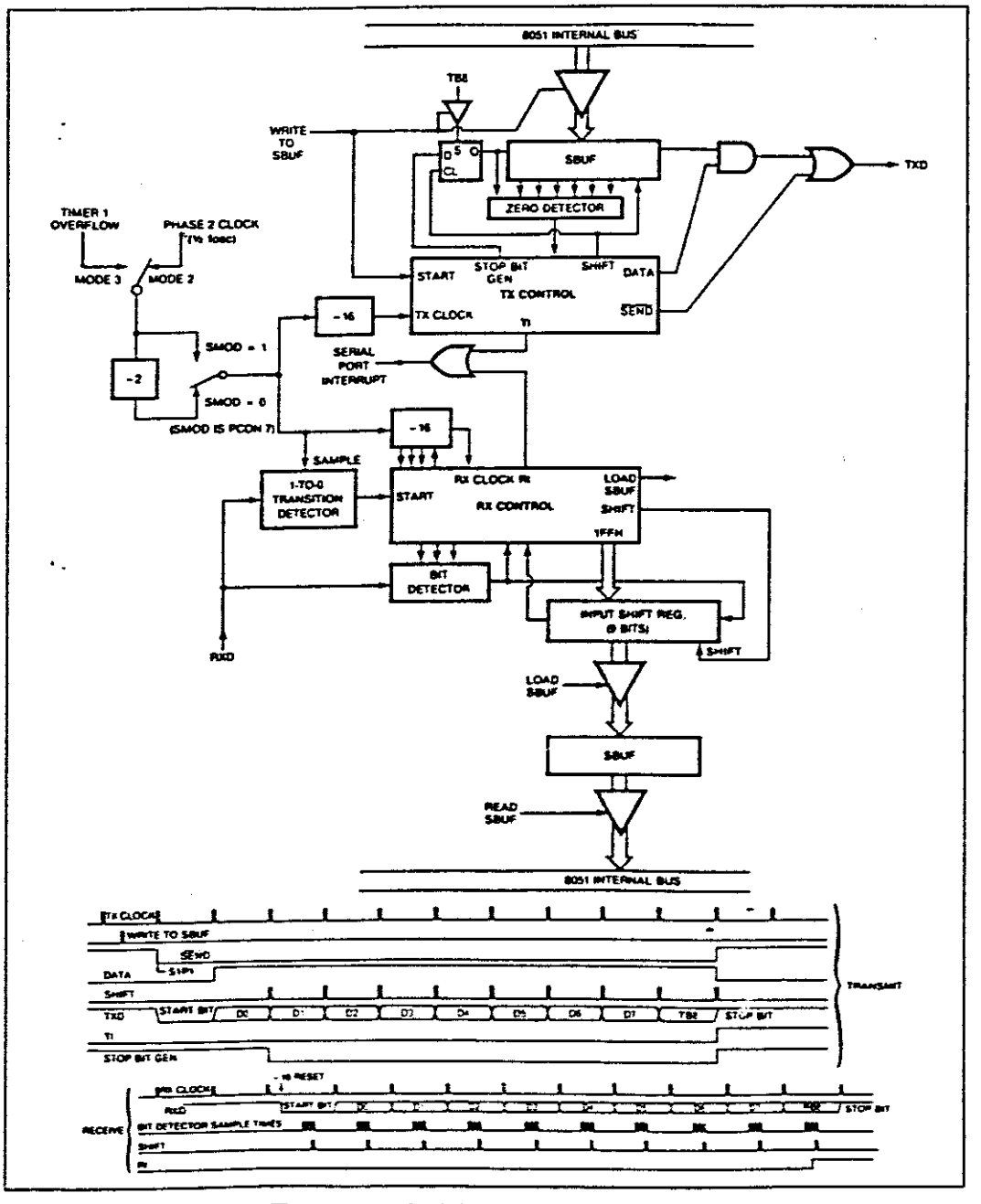


Figure 6-13. Serial Port in Modes 2 and 3

the stop bit is just to the left of TB8, and all positions to the left of that contain zeroes. This condition flags the TX Control unit to do one last shift and then deactivate $\overline{SEND}$ and set TI. This occurs at the 11th divide-by-16 rollover after "write to SBUF."

Reception is initiated by a detected 1-to-0 transition at RXD. For this purpose RXD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written to the input shift register.

At the 7th, 8th and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in modes 2 and 3 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8, and to set RI, will be generated if and only if the following conditions are met at the time the final shift pulse is generated:

1) RI = 0, and
2) Either SM2 = 0 or the received 9th data bit = 1

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF. One bit time later, whether the above conditions were met or not, the unit goes back to looking for a 1-to-0 transition at the RXD input.

Note that the value of the received stop bit is irrelevant to SBUF, RB8, or RI.

6.8 INTERRUPTS

The 8051 provides five interrupt sources, each of which can be programmed to one of two priority levels. The five interrupt sources are listed below:

Source	*Description*
$\overline{INT0}$	External request from P3.2 pin (sampled at S5P2 of every machine cycle).
Timer 0	Overflow from Timer 0 activates interrupt request flag TF0.
$\overline{INT1}$	External request from P3.3 pin (sampled at S5P2 of every machine cycle).
Timer 1	Overflow from Timer 1 activates interrupt request flag TF1.
Serial Port	Completion of transmission or reception of one serial frame activates request flag TI (on transmission) or RI (on reception).

Each source can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE.

Each source can be programmed to a high-priority level or a low-priority level by setting or clearing a bit in Register IP. A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted. To implement these rules, the Interrupt System contains two non-addressable "priority level active" flip-flops. One indicates that a high-priority interrupt is being serviced, and blocks all further interrupts. The other indicates that a low-priority interrupt is being serviced, and blocks all but high-priority interrupts.

In the event that requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence, as follows:

Source	*Priority within Level*
External Interrupt 0	(highest)
Timer 0 Overflow	
External Interrupt 1	
Timer 1 Overflow	
Serial Port	(lowest)

All the interrupt sources are examined sequentially during each cycle, such that by S6 of any cycle all active interrupt requests have been found and prioritized. Response to the active request of highest priority will commence with state 1 of the next machine cycle, provided the response is not blocked by any of the following conditions:

1) An interrupt of equal or higher priority level is already in progress.
2) The current machine cycle is not the final cycle in the execution of the instruction in progress. (In other words, no interrupt request will be responded to until the instruction in progress is completed.)
3) The instruction in progress is RETI or an access to Special Function Registers IE or IP. (In other words an interrupt request will not be responded to after RETI or after a read or write to IE or IP until at least one other instruction has been executed.)

If any of the above conditions exists, the result of the interrupt poll is discarded. If none of the above conditions exists, the result of the interrupt poll is acted on with the very next machine cycle.

The processor acknowledges a request by first setting the appropriate "priority level active" flip-flop. Then it executes a hardware subroutine call to the servicing routine. It also clears the flag that requested the interrupt (with exceptions: it doesn't clear $\overline{\text{INT0}}$ or $\overline{\text{INT1}}$, since it has no control over the sources of these signals, and it doesn't clear TI or RI). The hardware subroutine call pushes the contents of the Program Counter onto the stack (but it does not save the PSW) and reloads the PC with an address that depends on the source of the interrupt request, as shown below:

Source	*Address*
External Interrupt 0	0003H
Timer 0 Overflow	000BH
External Interrupt 1	0013H
Timer 1 Overflow	001BH
Serial Port	0023H

Execution proceeds from that address until the RETI instruction is encountered.

The RETI instruction clears the "priority level

until at least one other instruction has been executed. Thus, once an interrupt routine has been entered, it cannot be re-entered until at least one instruction of the interrupted program is executed.

There are a number of ways that this feature can be used to single-step the 8051. One way is to program one of the external interrupts (say, $\overline{INT0}$) to be level-activated. The service routine for this interrupt then will terminate with

```
JNB     P3.2,$      ;WAIT HERE TILL
                    INT0 GOES HIGH
JB      P3.2,$      ;NOW WAIT HERE
                    TILL IT GOES LOW
RETI                ;GO BACK AND
                    EXECUTE ONE
                    INSTRUCTION.
```

Now if the $\overline{INT0}$ pin, which is also the P3.2 pin, is held normally low, the CPU will go right into the External Interrupt 0 routine and stay there until $\overline{INT0}$ is pulsed (from low to high to low). Then it will execute RETI, go back to the task program, execute one instruction, and immediately re-enter the External Interrupt 0 routine to await the next pulsing of P3.2. One step of the task program is executed each time P3.2 is pulsed.

6.8.4 Interrupt Control Registers

The Interrupt Request Flags are in two different registers and two port pins, as listed below:

Source	*Request Flag*	*Location*
External Interrupt 0	$\overline{INT0}$, if IT0 = 0	P3.2
	IE0, if IT0 = 1	TCON.1
Timer 0 Overflow	TF0	TCON.5
External Interrupt 1	$\overline{INT1}$, if IT1 = 0	P3.3
	IE1, if IT1 = 1	TCON.3
Timer 1 Overflow	TF1	TCON.7
Serial Port	TI (on transmission)	SCON.1
	RI (on reception)	SCON.0

External Interrupt control bits IT0 and IT1 are in TCON.0 and TCON.2, respectively. Reset leaves all flags inactive, with IT0 and IT1 cleared.

All the interrupt flags can be set or cleared by software, with the same effect as by hardware.

The Enable and Priority Control Registers are shown below. All of these control bits are set or cleared by software. All are cleared by reset.

IE: Interrupt Enable Register

Bit:	7	6	5	4	3	2	1	0
	EA	X	X	ES	ET1	EX1	ET0	EX0

where

- EA disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
- ES enables or disables the Serial Port interrupt. If ES = 0, the Serial Port interrupt is disabled.
- ET1 enables or disables the Timer 1 Overflow interrupt. If ET1 = 0, the Timer 1 interrupt is disabled.
- EX1 enables or disables External Interrupt 1. If EX1 = 0, External Interrupt 1 is disabled.
- ET0 enables or disables the Timer 0 Overflow interrupt. If ET0 = 0, the Timer 0 interrupt is disabled.

IP: Interrupt Priority Register

Bit:	7	6	5	4	3	2	1	0
	X	X	X	PS	PT1	PX1	PT0	PX0

where

- PS defines the Serial Port interrupt priority level. PS = 1 programs it to the higher priority level.
- PT1 defines the Timer 1 interrupt priority level. PT1 = 1 programs it to the higher priority level.
- PX1 defines the External Interrupt 1 priority level. PX1 = 1 programs it to the higher priority level.
- PT0 defines the Timer 0 interrupt priority level. PT0 = 1 programs it to the higher priority level.
- PX0 defines the External Interrupt 0 priority level. PX0 = 1 programs it to the higher priority level.

6.9 RST/VPD PIN

The circuitry connected to the RST/VPD pin is shown in Figure 6-14. A Schmitt Trigger is used at the input to the reset circuitry for noise rejection. The output of the Schmitt Trigger is sampled by the reset circuitry at S5P2 of every machine cycle. At least two consecutive samples must show a high in order to effect a complete reset and initialization.

6.9.1 Reset

Reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods) while the oscillator is running. The CPU responds by executing an internal reset. It also configures the ALE and $\overline{PSEN}$ pins as inputs. (They are quasi-bidirectional.) The internal reset is executed during the second cycle in which RST is high and is repeated every cycle until RST goes low. It leaves the internal registers as follows:

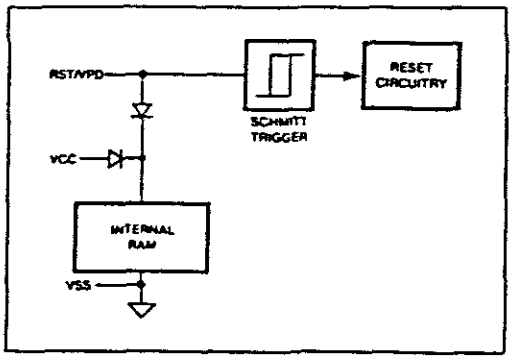


Figure 6-14. RST/VPD Circuitry

Register	*Content*
PC	0000H
A	00H
B	00H
PSW	00H
SP	07H
DPTR	0000H
P0 - P3	0FFH
IP	(XXX00000)
IE	(0XX00000)
TMOD	00H
TCON	00H
TH0	00H
TL0	00H
TH1	00H
TL1	00H
SCON	00H
SBUF	Indeterminate
PCON	(0XXXXXXX)

The internal RAM is not affected by reset. When VCC is turned on, the RAM content is indeterminate unless VPD was applied prior to VCC being turned off (see Power Down Operation).

POWER-ON RESET

An automatic reset can be obtained when VCC is turned on by connecting the RST pin to VCC through a 10 μf capacitor, providing the VCC risetime doesn't exceed a millisecond or so. A power-on reset circuit is shown in Figure 6-15. When power comes on the current drawn by RST commences to charge the capacitor. The voltage at RST is the difference between VCC and the capacitor voltage, and decreases from VCC as the cap charges. The larger the capacitor is, the more slowly VRST decreases. VRST must remain above the lower threshold of the Schmitt Trigger long enough to effect a complete reset. The time required is the oscillator start-up time plus 2 machine cycles. If the VCC risetime is less than 1 msec and the oscillator start-up time doesn't exceed 10 msec, a 10 μf capacitor will provide a reliable power-on reset.

6.9.2 Power Down Operation

During normal operation the internal RAM draws its power from VCC. However, as can be seen in Figure 6-14, if the voltage at RST/VPD exceeds VCC it becomes the source of power for the RAM. This allows a backup power supply to be used to hold RAM data in the event of a power failure.

To take advantage of this feature, the user's system, upon detecting that a power failure is imminent, would interrupt the processor via $\overline{\text{INT0}}$ or $\overline{\text{INT1}}$ to transfer relevant data to the RAM and enable the backup power supply to

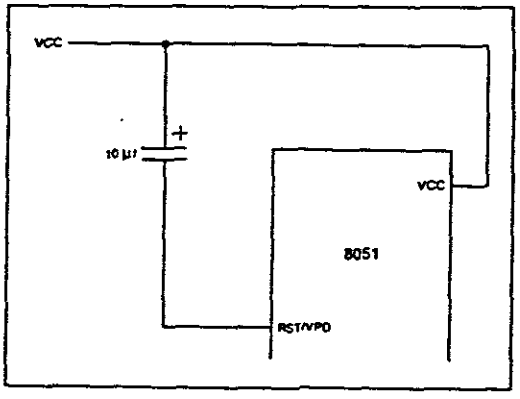


Figure 6-15. Power-On Reset

the RST/VPD pin before VCC falls below its operating limit. When power returns, VPD needs to stay on long enough to effect a reset (oscillator start-up time plus two machine cycles), and normal operation can resume.

Figure 6-16 suggests one possible implementation of the power-down feature. Assuming a detected imminent power failure interrupts the processor via $\overline{\text{INT0}}$, the External Interrupt 0 service routine transfers relevant data to the RAM and then writes a 0 to P1.0. The low at P1.0 triggers the 555, which is configured as a one-shot whose output pulse width depends on R, C, and the presence of VCC. If VCC is still present when the 555 times out, it is assumed that the "imminent power failure" was a false alarm, and operation resumes from reset. If VCC does in fact go down before the 555 times out, the 555 will hold power to RST/VPD during the outage, and will continue to hold it after VCC comes back, for a time determined by R and C. R and C should be selected so as to obtain a reliable power-on reset.

6.10 8751

The 8751 is the EPROM version of the 8051,

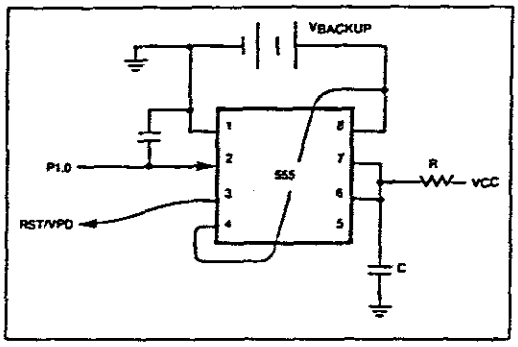


Figure 6-16. Power Down Circuit

that is, the on-chip Program Memory in the 8751 can be electrically programmed, and can be erased by exposure to ultraviolet light. Erasure leaves the array in an all 1s state.

6.10.1 Erasure Characteristics

Erasure of the 8751 Program Memory begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, constant exposure to these light sources over an extended period of time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause unintentional erasure. If an application subjects the 8751 to this type of exposure, it is suggested that an opaque label be placed over the window. (Suitable labels are available from Intel.)

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the 8751 to an ultraviolet lamp of 12000 μW/cm^2 rating for 20 to 30 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

6.10.2 Programming the EPROM

To be programmed, the 8751 must be running with a 4 to 6 MHz oscillator. The address of an EPROM location to be programmed is applied to Port 1 and pins P2.0-P2.3 of Port 2, while the data byte is applied to Port 0. Pins P2.4-P2.6 and $\overline{\text{PSEN}}$ should be held low, and P2.7 and RST high. (These are TTL levels, except RST which requires 2.5V for a high.) $\overline{\text{EA}}$ is held normally at TTL high, and is pulsed to +21V. While $\overline{\text{EA}}$ is at 21V, the ALE pin, which is normally being held at TTL high, is pulsed low for 50 msec. Then $\overline{\text{EA}}$ is returned to TTL high. This is illustrated in Figure 6-17. Detailed timing specifications are given in the data sheets.

Note: The $\overline{\text{EA}}$ pin must not be allowed to go above the maximum specified VPP level of 21.5 V, even instantaneously. Even a narrow glitch above that voltage level can cause permanent damage. It is suggested that the VPP source be well regulated and free of glitches.

6.10.3 Program Verification

Refer to Figure 6-18 for the Program Verification setup for the 8751 or the 8051. To read the Program Memory of either the 8751 or the 8051, the following procedure can be used. The unit must be running with a 4 to 6 MHz oscillator. The address of a Program Memory location to be read is applied to Port 1 and pins P2.0-P2.3 of Port 2. Pins P2.4-P2.6 and $\overline{\text{PSEN}}$ are held low, while the ALE, RST, and $\overline{\text{EA}}$ pins are held high. (These are TTL levels except RST, which requires 2.5V for a high.) Port 0 will be the data output lines. P2.7 can be used as a read strobe. While P2.7 is held at TTL high, the Port 0 pins float. When P2.7 is strobed low, the contents of the addressed location will appear at Port 0. External pull-

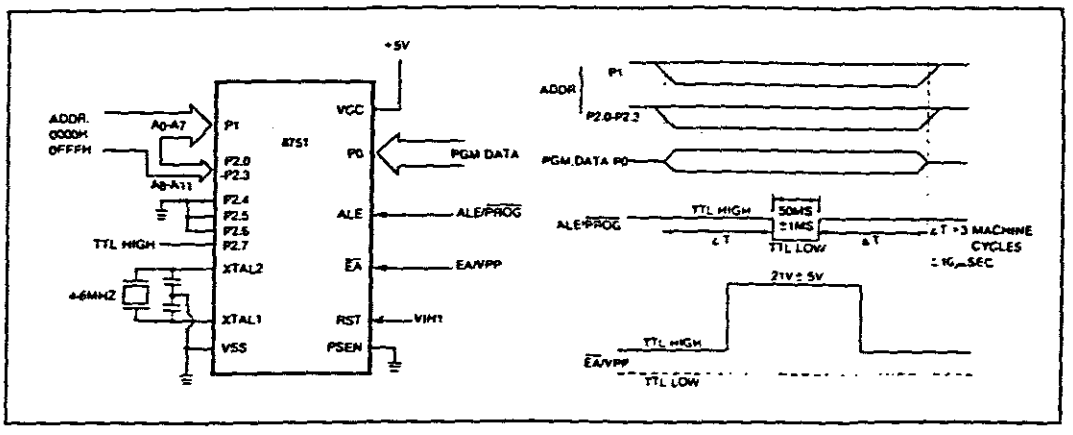


Figure 6-17. Programming the 8751

ups (e.g., 10K) are required on Port 0 during this operation.

6.11 8051 FAMILY PIN DESCRIPTION

VSS: Circuit ground potential.

VCC: Supply voltage during programming (of the 8751), verification (of the 8051 or 8751), and normal operation.

Port 0: Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus during accesses to external memory (during which accesses it activates internal pullups). It also outputs instruction bytes during program verification. (External pullups are required during program verification.) Port 0 can sink eight LS TTL inputs.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. It receives the low-order address byte during program verification in the 8051 or 8751. Port 1 can sink/source three LS TTL inputs. It can drive MOS inputs without external pullups.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. It emits the high-order address byte during accesses to external memory. It also receives the high-order address bits and control signals during program verification in the 8051 or 8751. Port 2 can sink/source three LS TTL inputs. It can drive MOS inputs without external pullups.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. It also serves the functions of various special features of the MCS-51 Family, as listed below:

Port Pin	*Alternate Function*
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt)
P3.3	$\overline{INT1}$ (external interrupt)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external Data Memory write strobe)
P3.7	$\overline{RD}$ (external Data Memory read strobe)

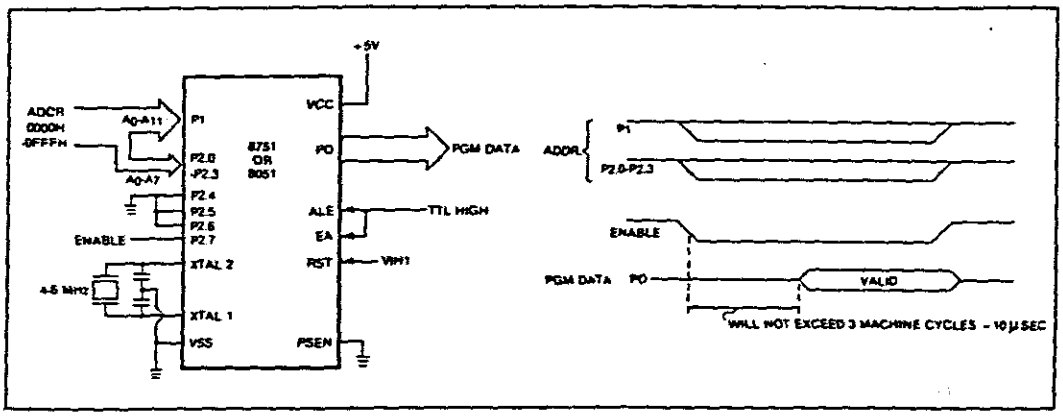


Figure 6-18. Program Verification

Port 3 can sink/source three LS TTL inputs. It can drive MOS inputs without external pullups.

RST/VPD: A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal pulldown permits Power-On reset using only a capacitor connected to VCC.

ALE/PROG: Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated though for this purpose at a constant rate of 1/6 the oscillator frequency even when external memory is not being accessed. Consequently it can be used for external clocking or timing purposes. (However, one ALE pulse is skipped during each access to external *Data* Memory.) This pin is also the program pulse input (PROG) durin EPROM programming.

PSEN: Program Store Enable output is the read strobe to external Program Memory PSEN is activated twice each machine cycle during fetches from external Program Memory. (However, when executing out of external Program Memory two activations of PSEN are skipped during each access to external *Data* Memory.) PSEN is not activated during fetches from internal Program Memory.

$\overline{EA}$/VPP: When EA is held high the CPU executes out of internal Program Memory (unless the Program Counter exceeds 0FFFH). When $\overline{EA}$ is held low the CPU executes only out of external Program Memory. In the 8031, $\overline{EA}$ must be externally wired low. In the 8751, this pin also receives the 21V programming supply voltage (VPP) during EPROM programming.

XTAL1: Input to the inverting amplifier that forms the oscillator. Should be grounded when an external oscillator is used.

XTAL2: Output of the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external oscillator signal when an external oscillator is used.

CHAPTER 7
MCS®-51 MEMORY, ORGANIZATION, ADDRESSING MODES AND DATA MANIPULATION

7.0 MEMORY ORGANIZATION

In the 8051 family the memory is organized over three address spaces and the program counter. The memory spaces shown in Figure 6-2 (page 6-3) are the:

- 64K-byte Program Memory address space
- 64K-byte External Data Memory address space
- 384-byte Internal Data Memory address space

The 16-bit Program Counter register provides the 8051 with its 64K addressing capabilities. The Program Counter allows the user to execute calls and branches to any location within the Program Memory space. There are no instructions that permit program execution to move from the Program Memory space to any of the data memory spaces.

In the 8051 and 8751 the lower 4K of the 64K Program Memory address space is filled by internal ROM and EPROM, respectively. By tying the $\overline{EA}$ pin high, the processor can be forced to fetch from the internal ROM/EPROM for Program Memory addresses 0 through 4K. Bus expansion for accessing Program Memory beyond 4K is automatic since external instruction fetches occur automatically when the Program Counter increases above 4095. If the $\overline{EA}$ pin is tied low all Program Memory fetches are from external memory. The execution speed of the 8051 is the same regardless of whether fetches are from internal or external Program Memory. If all program storage is on-chip, byte location 4095 should be left vacant to prevent an undesired prefetch from external Program Memory address 4096.

Certain locations in Program Memory are reserved for specific programs. Locations 0000 through 0002 are reserved for the initialization program. Following reset, the CPU always begins execution at location 0000. Locations 0003 through 0042 are reserved for the five interrupt-request service programs. Each resource that can request an interrupt requires that its service program be stored at its reserved location.

The 64K-byte External Data Memory address space is automatically accessed when the MOVX instruction is executed.

Functionally the Internal Data Memory is the most flexible of the address spaces. The Internal Data Memory space is subdivided into a 256-byte Internal Data RAM address space and a 128-byte Special Function Register address space as shown in Figure 7-1.

The Internal Data RAM address space is 0 to 255. Four 8-Register Banks occupy locations 0 through 31. The stack can be located anywhere in the Internal Data RAM address space. In addition, 128 bit locations of the on-chip RAM are accessible through Direct Addressing. These bits reside in Internal Data RAM at byte locations 32 through 47. Currently locations 0 through 127 of the Internal Data RAM address space are filled with on-chip RAM.

The stack depth is limited only by the available Internal Data RAM, thanks to an 8-bit reloadable Stack Pointer. The stack is used for storing the Program Counter during subroutine calls and may be used for passing parameters. Any byte of Internal Data RAM or Special Function Register accessible through Direct Addressing can be pushed/popped.

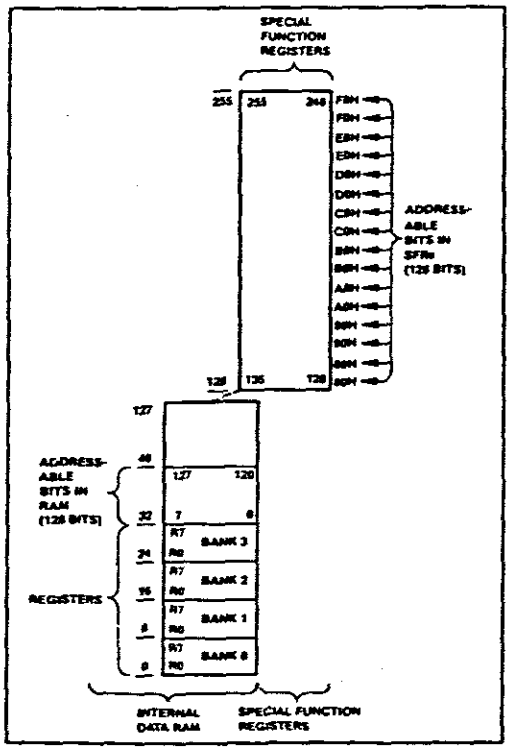


Figure 7-1. Internal Data Memory Address Space

The Special Function Register address space is 128 to 255. All registers except the Program Counter and the four 8-Register Banks reside here. Memory mapping the Special Function Registers allows them to be accessed as easily as internal RAM. As such, they can be operated on by most instructions. In addition, 128 bit locations within the Special Function Register address space can be accessed using Direct Addressing. These bits reside in the Special Function Register byte locations divisible by eight. The twenty Special Function Registers are listed in Figure 7-2. Their mapping in the Special Function Register address space is shown in Figures 7-3 and 7-4.

Performing a read from a location of the Internal Data memory where neither a byte of Internal Data RAM (i.e., RAM addresses 128-255) nor a Special Function Register exists will access data of indeterminable value.

Architecturally, each memory space is a linear sequence of 8-bit wide bytes. By Intel convention the storage of multi-byte address and data operands in program and data memories is the least significant byte at the low-order address and the most significant byte at the high-order address. Within byte X, the most significant bit is represented by X.7 while the least significant bit is X.0. Any deviation from these conventions will be explicitly stated in the text.

ARITHMETIC REGISTERS:
ACCumulator*, B register*,
Program Status Word*
POINTERS:
Stack Pointer, Data Pointer (high & low)
PARALLEL I/O PORTS:
Port 3*, Port 2*, Port 1*, Port 0*
INTERRUPT SYSTEM:
Interrupt Priority Control*,
Interrupt Enable Control*
TIMERS:
Timer MODe, Timer CONtrol*, Timer 1 (high & low), Timer 0 (high & low)
SERIAL I/O PORT:
Serial CONtrol*, Serial data BUFfer, PCON
*Bits in these registers are bit addressable

Figure 7-2. Special Function Registers

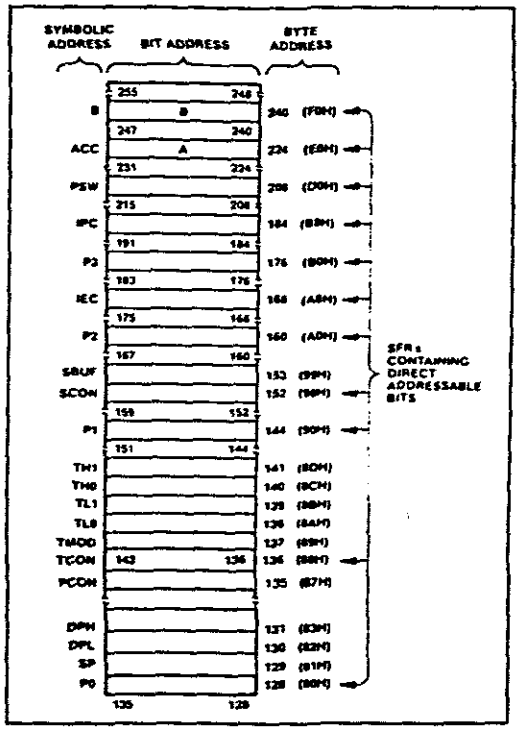


Figure 7-3. Mapping of Special Function Registers

7.1 OPERAND ADDRESSING

There are five methods of addressing source operands. They are Register Addressing, Direct Addressing, Register-Indirect Addressing, Immediate Addressing and Base-Register-plus Index-Register-Indirect Addressing. The first three of these methods can also be used to address a destination operand. Since operations in the 8051 require 0 (NOP only), 1, 2, 3 or 4 operands, these five addressing methods are used in combinations to provide the 8051 with its 21 addressing modes.

Most instructions have a "destination, source" field that specifies the data type, addressing methods and operands involved. For operations other than moves, the destination operand is also a source operand. For example, in "subtract-with-borrow A,#5" the A register receives the result of the value in register A minus 5, minus C.

Most operations involve operands that are located in Internal Data Memory. The selection of the Program Memory space or External Data Memory space for a second operand is determined by the operation mnemonic unless it is an immediate operand. The subset of the Internal Data Memory being addressed is determined by the addressing method and address value. For example, the Special Function Registers can be accessed only through Direct Addressing with an address of 128-255. A summary of the operand addressing methods is shown in Figure 7-5. The following paragraphs describe the five addressing methods.

7.1.1 Register Addressing

Register Addressing permits access to the eight registers (R7-R0) of the selected Register Bank (RB). One of the four 8-Register Banks is selected by a two-bit field in the PSW. The registers may also be accessed through Direct Addressing and Register-Indirect Addressing, since the four Register Banks are mapped into the lowest 32 bytes of Internal Data RAM as shown in Figures 7-6 and 7-7. Other Internal Data Memory locations that are addressed as registers are A, B, C, AB and DPTR.

7.1.2 Direct Addressing

Direct Addressing provides the only means of accessing the memory-mapped byte-wide Special Function Registers and memory mapped bits within the Special Function Registers and Internal Data RAM. Direct Addressing of bytes may also be used to access the lower 128 bytes of Internal Data RAM. Direct Addressing of bits gains access to a 128 bit subset of the Internal Data RAM and 128 bit subset of the Special Function Registers as shown in Figures 7-3, 7-4, 7-6, and 7-7.

Register-Indirect Addressing using the content of R1 or R0 in the selected Register Bank, or

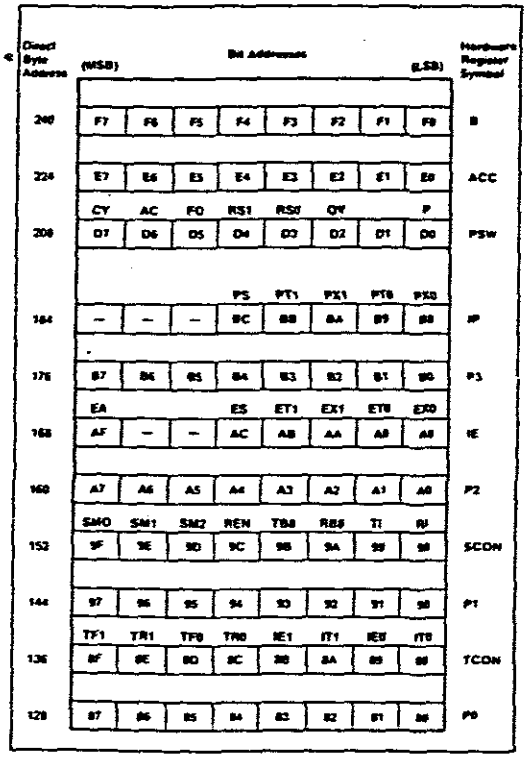


Figure 7-4. Special Function Register Bit Address

- Register Addressing
  - R7-R0
  - A,B,C (bit), AB (two bytes), DPTR (double byte)
- Direct Addressing
  - Lower 128 bytes of Internal Data RAM
  - Special Function Registers
  - 128 bits in subset of Internal Data RAM address space
  - 128 bits in subset of Special Function Register address space
- Register-Indirect Addressing
  - Internal Data RAM [@R1, @R0, @SP (PUSH and POP only)]
  - Least Significant Nibbles in Internal Data RAM (@R1, @R0)
  - External Data Memory (@R1, @R0, @DPTR)
- Immediate Addressing
  - Program Memory (in-code constant)
- Base-Register- plus Index-Register-Indirect Addressing
  - Program Memory (@ DPTR + A, @ PC + A)

Figure 7-5. Operand Addressing Methods

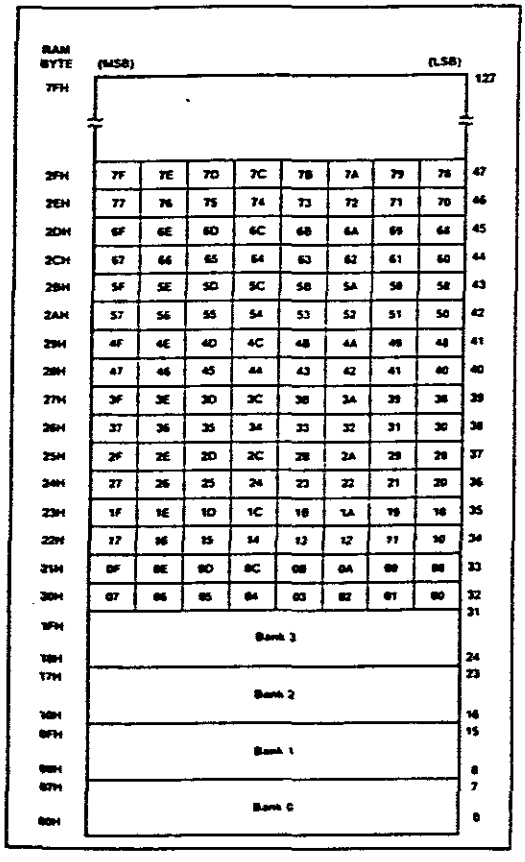


Figure 7-6. RAM Bit Addresses

using the content of the Stack Pointer (PUSH and POP only), addresses the Internal Data RAM. Register-Indirect Addressing is also used for accessing the External Data Memory. In this case, either R1 or R0 in the selected Register Bank may be used for accessing locations within a 256-byte block. The block number can be preselected by the contents of a port. The 16-bit Data Pointer may be used for accessing any location within the full 64K external address space.

7.1.3 Immediate Addressing

Immediate Addressing allows constants which

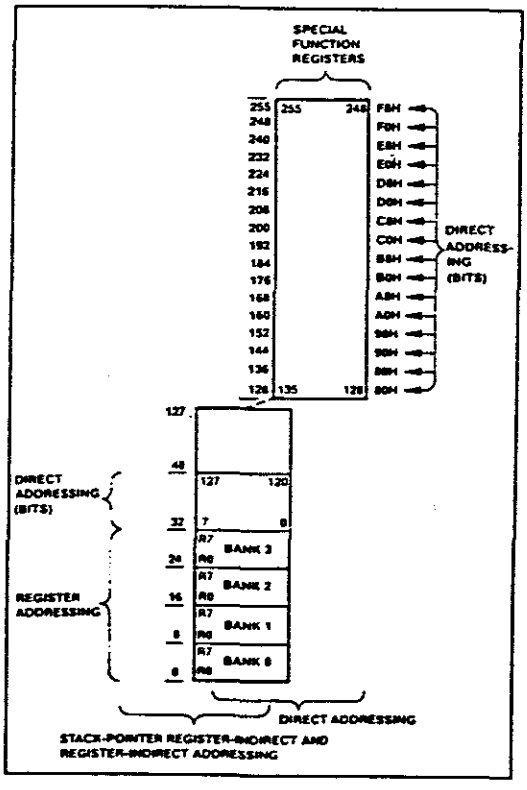


Figure 7-7. Addressing Operands in Internal Data Memory

are part of the instruction to be accessed from the Program Memory.

7.1.4 Base-Register- plus Index-Register- Indirect Addressing

Base-Register- plus Index-Register- Indirect Addressing simplifies accessing look-up-tables (LUT) resident in Program memory. A byte may be accessed from a LUT via an indirect move from a location whose address is the sum of a base register (the DPTR or PC) and the index register (A).

7.2 DATA MANIPULATION

The 8051 microcomputer is efficient both as an arithmetic processor and as a controller. In ad-

dition to the capabilities of its 8048 predecessor, the 8051 was enhanced with improved data transfer, logic manipulation, arithmetic processing, and real-time control capabilities. The 8051 performs operations on bit, nibble (4-bit), byte (8-bit) and double-byte (16-bit) data types. It is classified as an 8-bit machine since the internal ROM, RAM, Special Function Registers, Arithmetic/Logic Unit (ALU) and the external data bus are each 8-bits wide. The double-byte data type is used only by the Data Pointer and the Program Counter. The Data Pointer can be manipulated as a single double-byte register (DPTR) or as two locations in Internal Data Memory (DPH & DPL). The Program Counter is always manipulated as a single double-byte register.

7.3 BOOLEAN PROCESSOR

Although the Boolean processor is an integral part of the 8051's architecture, it may be considered an independent bit processor since it has its own instruction set, its own accumulator (the carry flag), and its own bit-addressable RAM and I/O.

The bit-manipulation instructions allow the Direct Addressing of 128 bits within the Internal Data RAM and 128 bits within the Special Function Registers. The Special Function Registers with an address evenly divisable by eight (P0, TCON, P1, SCON, P2, IEC, P3, IPC, PSW, A, and B) contain Direct Addressable bits. On any addressable bit, the Boolean processor can perform the bit operations of set, clear, complement, jump-if-set, jump-if-not-set, jump-if-set-then-clear and move to/from carry. Between any addressable bit (or its complement) and the carry flag it can perform the bit operation of logical and or logical or with the result returned to the carry flag.

The bit-manipulation instructions provide optimum code and speed efficiency in "bit-banging" applications such as the control of the 8051's on-chip peripherals. The Boolean processor also provides a straightforward means of converting logic equations (like those used in random logic design) directly into software. Complex cominatorial-logic functions can be resolved without extensive data movement, byte masking and test-and-branch trees.

7.4 DATA TRANSFER OPERATIONS

Look-up-tables resident in Program Memory can be accessed by indirect moves. A byte constant can be transferred to the A register (i.e., accumulator) from the Program memory location whose address is the sum of a base register (the PC or DPTR) and the index register (A). This provides a convenient means for programming translation algorithms such as ASCII to seven segment conversions. The Program Memory move operations are shown diagrammatically in Figure 7-8.

A byte location within a 256-byte block of External Data Memory can be accessed using R1 or R0 in Register-Indirect Addressing. Any location within the full 64K External Data Memory address space can be accessed through Register-Indirect Addressing using a 16-bit base register (i.e., the Data Pointer). These moves are shown in Figure 7-9.

The byte in-code-constant (immediate) moves and byte variable moves within the 8051 are highly orthogonal as detailed in Figure 7-10. When one considers that the accumulator and the registers in the Register Banks can be Direct Addressed, the two-operand data transfer operations allow a byte to be moved between any two of the RB registers, Internal

Data RAM, accumulator and Special Function Registers. Also, immediate operands can be moved to any of these locations. Of particular interest is the Direct Address to Direct Address move which permits the value in a port to be moved to the Internal Data RAM without using any RB registers or the accumulator. The Data Pointer register can be loaded with a double-byte immediate value. Also, the 8051's Boolean Processor can move any Direct Addressed bit to or from the carry register.

The A register can be exchanged with a register in the selected Register Bank, with a Register-Indirect Addressed byte in the Internal Data RAM or with a Direct Addressed byte in the Internal Data RAM or Special Function Register. The least significant nibble of the A register can also be exchanged with the least

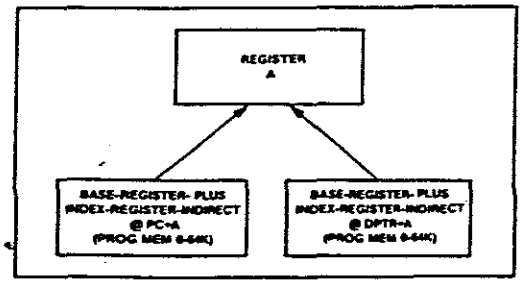


Figure 7-8. Program Memory Move Operations

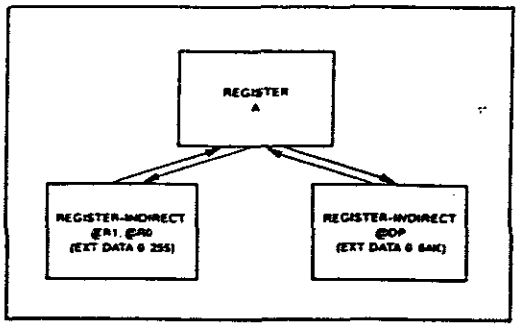


Figure 7-9. External Data Memory Move Operations

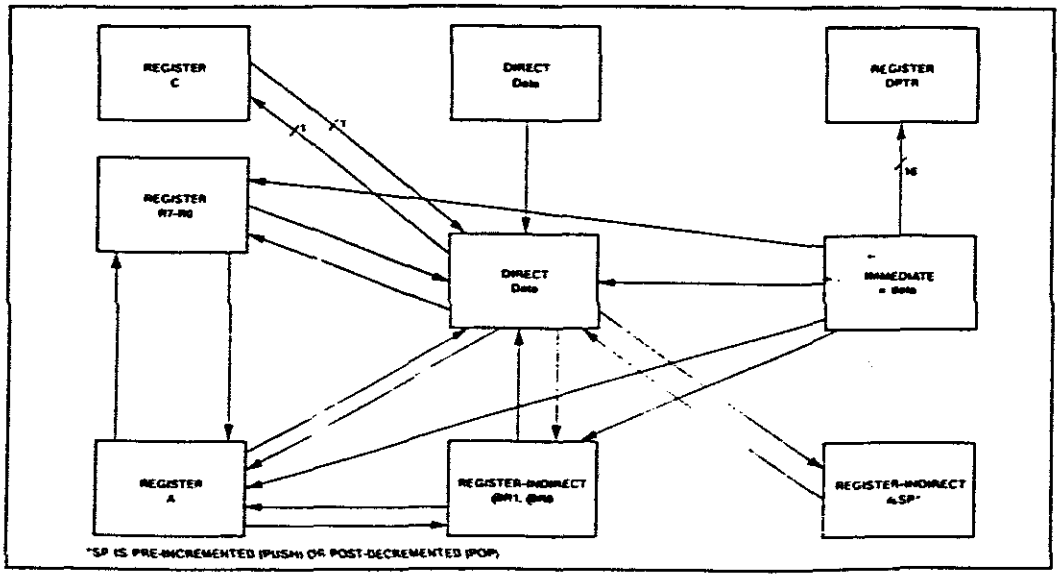


Figure 7-10. Internal Data Memory Move Operations

significant nibble of a Register-Indirect Addressed byte in the Internal Data RAM. The exchange operation is shown in Figure 7-11.

7.5 LOGIC OPERATIONS

The 8051 permits the logic operations of and, or, and exclusive-or to be performed on the A register by a second operand which can be immediate value, a register in the selected Register Bank, a Register-Indirect Addressed byte of Internal Data RAM or a Direct Addressed byte of Internal Data RAM or Special Function Register. In addition, these logic operations can be performed on a Direct Addressed byte of the Internal Data RAM or Special Function Register using the A register as the second operand. Also, use of Immediate Addressing with Direct Addressing permits these logic operations to set, clear or complement any bit anywhere in the Internal Data RAM or Special Function Registers without affecting the PSW, RB registers or accumulator. When one takes into account that registers R7-R0 and the accumulator can be Direct Addressed, the two-operand logic operations allow the destination (first operand) to be a byte in the Internal Data RAM, a Special Function Register, RB registers (R7-R0) or the accumulator while the choice of the second operand can be any of the aforementioned or an immediate value. The 8051 can also perform a logical or, or a logical and, between the Boolean accumulator (i.e, the carry flag) and any bit, or its complement, that can be accessed through Direct Addressing. The and, or, and exclusive-or logic operations are summarized in Figure 7-12.

In addition to the logic operations that are performed on Internal Data Memory as shown in Figure 7-12, there are also logic operations that are performed specifically on the A register. These are summarized in Figure 7-13.

In addition to the and and or bit logical shown in Figure 7-12, there are logicals that can operate exclusively on a Direct Addressed bit.

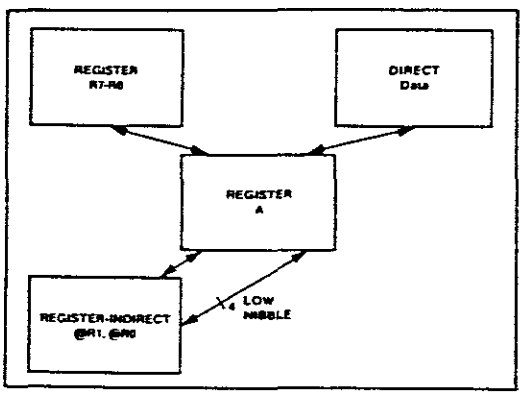


Figure 7-11. Internal Data Memory Exchange Operations

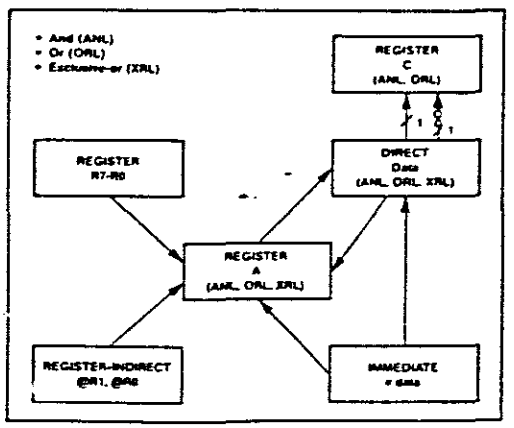


Figure 7-12. Internal Data Memory Logic Operations

These operations are listed in Figure 7-14. The carry flag is also addressed as a register and can be set, cleared or complemented with one-byte instructions.

7.6 ARITHMETIC OPERATIONS

Along with the existing 8048 arithmetic operations of add, increment, decrement, compare-to-zero, decrement-and-compare-to-zero, and decimal-add-adjust, the 8051 implemented subtract-with-borrow, compare, multiply and divide.

Only unsigned binary integer arithmetic is performed in the Arithmetic/Logic Unit. In the two-operand operations of add, add-with-carry and subtract-with-borrow, the A register is the first operand and receives the result of the operation. The second operand can be an immediate byte, a register in the selected Register Bank, a Register-Indirect Addressed byte or a Direct Addressed byte. These instructions affect the overflow, carry, auxiliary-carry and parity flag in the Program Status Word (PSW). The carry flag facilitates non-signed integer and multi-precision addition and subtraction and multi-precision rotation. Handling two's-complement-integer (signed) addition and subtraction can easily be accommodated with software's monitoring of the PSW's overflow flag. The auxiliary-carry flag simplifies BCD arithmetic. An operation that has an arithmetic aspect similar to a subtract is the compare-and-jump-if-not-equal operation. This operation performs a conditional branch if a register in the selected Register Bank, or an Indirect Addressed byte of Internal Data RAM, does not equal an immediate value; or if the A register does not equal a byte in the Direct Addressable Internal Data RAM, or a Special Function Register. While the destination operand is not updated and neither source operand is affected by the compare operation, the carry flag is. A summary of the two-operand add/subtract operations is shown in Figure 7-15.

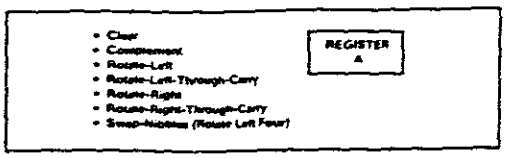


Figure 7-13. Internal Data Memory Logic Operations (Register A Specific)

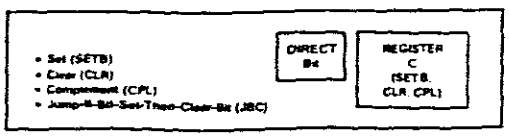


Figure 7-14. Internal Data Memory Logic Operations (Bit-Specific)

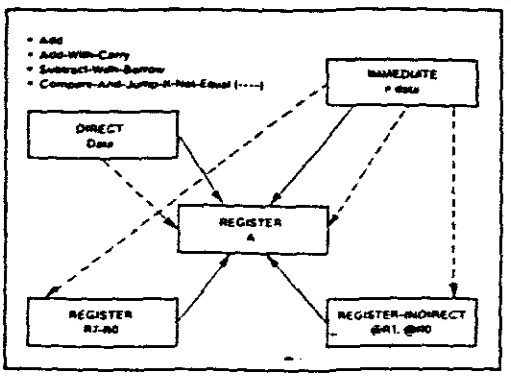


Figure 7-15. Internal Data Memory Arithmetic Operations

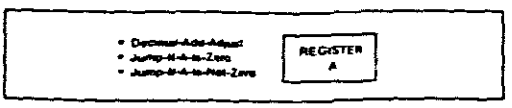


Figure 7-16. Internal Data Memory Arithmetic Operations (Register A Specific)

There are three arithmetic operations that operate exclusively on the A register. These are the decimal-adjust for BCD addition and the two test conditions shown in Figure 7-16. The decimal-adjust operation converts the result from a binary addition to two two-digit BCD values to yield the correct two-digit BDC result. During this operation the auxiliary-carry flag helps effect the proper adjustment. Conditional branches may be taken based on the value in the A register being zero or not zero.

The 8051 simplifies the implementation of software counters since the increment and decrement operations can be performed on the A register, a register in the selected Register Bank, an Indirect Addressed byte in the Internal Data RAM or a byte in the Direct Addressed Internal Data RAM or Special Function Register. The 16-bit Data Pointer can be incremented. For efficient loop control the decrement-and-jump-if-not-zero operation is provided. This operation can test a register in the selected Register Bank, any Special Function Register or any byte of Internal Data RAM accessible through Direct Addressing and force a branch if it is not zero. The increment/decrement operations are summarized in Figure 7-17.

The multiply operation multiplies the one-byte A register by the one-byte B register and returns a double-byte result (MSB in B, LSB in A). The divide operation divides the one-byte A register by the one-byte B register and returns a byte quotient to the A register and a byte remainder to the B register. These are shown in Figure 7-18.

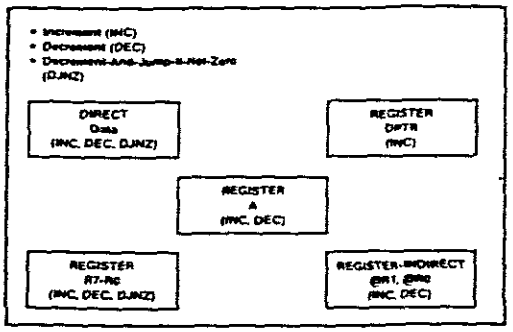


Figure 7-17. Internal Data Memory Arithmetic Operations

Figure 7-18. Internal Data Memory Arithmetic Operations (Register A with B Specific)

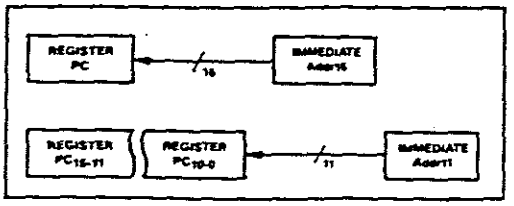


Figure 7-19. Unconditional Branch Operations

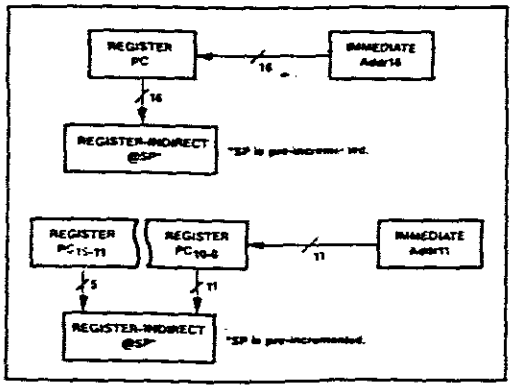


Figure 7-20. Call Operations

7.7 CONTROL TRANSFER

The 8051 has a non-paged Program Memory to accommodate relocatable code. The advantage of a non-paged memory is that a minor change to a program that causes a shift of the code's position in memory will not cause page boundary readjustments to be necessary. This also makes relocation possible. Relocation is desirable since it permits several programmers to write relocatable modules in various assembly and high-level languages which can later be linked together to form the machine object code.

Sixteen-bit jumps and calls are provided to allow branching to any location in the contiguous 64K Program Memory address space and preempt the need for Program Memory bank switching. Eleven-bit jumps and calls are also provided to maintain compatibility with the 8048 and to provide an efficient jump within a 2K program module. Unlike the 8048, the 8051's call operations do not push the Program Status Word (PSW) to the stack along with the Program Counter, since many subroutines written for the 8051 do not affect the PSW. Hence the 8051 return operations pop only the Program Counter. The 8051's branch, call and return operations are shown diagrammatically in Figures 7-19, 7-20, and 7-21, respectively.

The 8051 also provides a method for performing conditional and unconditional branching relative to the starting address of the next instruction (PC - 128 to PC + 127). The bit test operations allow a conditional branch to be taken on the condition of a Direct Addressed bit being set or not set. The accumulator test operations allow a conditional branch based on the accumulator being zero or non-zero. Also provided are compare-and-jump-if-not-equal and decrement-and-compare-to-zero. These are shown in Figure 7-22.

The register-indirect jump in the 8051 permits branching relative to a base register (DPTR) with an offset provided by the non-signed integer value in the index register (A). This accommodates N-way branching. The indirect jump is shown in Figure 7-23.

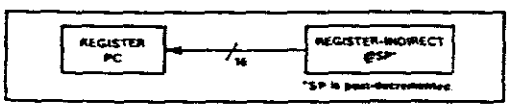


Figure 7-21. Return Operation

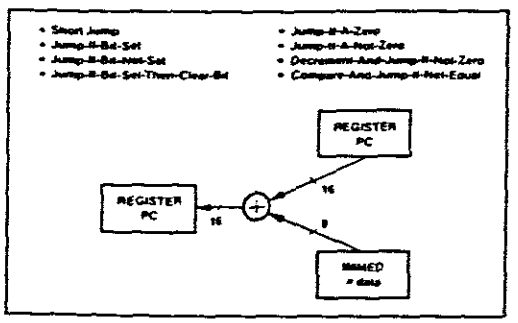


Figure 7-22. Unconditional Short Branch and Conditional Branch Operations

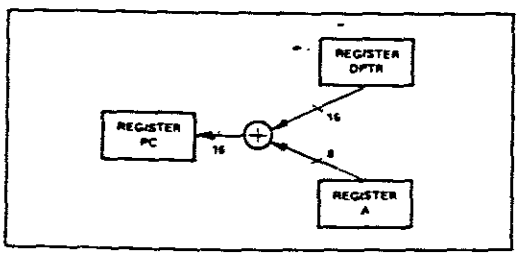


Figure 7-23. Unconditional Branch (Indirect) Operation

CHAPTER 8
MCS®-51 INSTRUCTION SET

8.0 WHAT THE INSTRUCTION SET IS

An instruction set is a set of codes that directs a computer to perform its operations. The ease of understanding the instruction set does not depend upon the structure of the machine codes that the computer recognizes, so much as it depends upon the structure of the symbolic language that is used to describe the machine codes.

The 8051 assembly language needs only forty-two mnemonics to specify the 8051's thirty-three functions. A function may have several mnemonics (e.g., MOV, MOVX, MOVC) since the function mnemonic specifies when the Program Memory or External Data Memory is used in conjunction with the Internal Data Memory. When the function mnemonics are combined with unique address combinations specified in the "destination, source" field, 111 instructions are possible. The "destination, source" field specifies the data type and the combination of addressing methods to be used to address the destination and source operands. A summary of the 8051 instruction set is provided in Table 8-1.

The syntax of most 8051 assembly language instructions consists of a function mnemonic followed by a "destination, source" operand field. Thus "MOV @R0, Data" may be interpreted as "The content of the Internal Data Memory location addressed by the content of Register 0 receives the content of the Internal Data Memory location addressed by Data." In two operand instructions, the destination address also serves as the address of the first source. As an example of this, "ANL Data, #5" may be interpreted as "The content of the Internal Data Memory location addressed by Data receives the result of the operation when the content of the memory location specified by Data is and-ed with the immediate 5."

The 8051's instruction set is an enhancement of the instruction set familiar to MCS-48 users. It is enhanced to allow expansion of on-chip CPU peripherals and to optimize byte efficiency and execution speed. Efficient use of program memory results from an instruction set consisting of 49 single-byte, 45 two-byte and 17 three-byte instructions. Most arithmetic, logical and branching operations can be performed using an instruction that appends either a short address or a long address. For example, Register Addressing allows a two-byte equivalent of the three byte Direct Addressing instructions. Also, short branches are more code efficient than long branches. 64 instructions execute in twelve oscillator periods, 45 instructions execute in twenty-four oscillator periods, and multiply and divide take only forty-eight oscillator periods. The number of bytes in each instruction and the number of oscillator periods required for execution are listed in Table 8-1.

8.1 ORGANIZATION OF THE INSTRUCTION SET

Instructions are described here in four functional groups:

- Data Transfer
- Arithmetic
- Logic
- Control Transfer

The Data Transfer, Arithmetic and Logic groups mentioned in the preceding list are further subdivided into an array of codes that specify whether the operation is to act upon immediate, RB register, accumulator, SFR or memory locations; whether bits, nibbles, bytes or double-bytes are to be processed; and what addressing methods are to be employed.

8.1.1 Data Transfer

Data transfer operations are divided into three classes:

- General Purpose
- Accumulator-Specific
- Address-Object

None affect the flag settings except a POP or MOV into the PSW.

General-Purpose Transfers

Three general-purpose data transfer operations are provided. These may be applied to most operands, though there are specific exceptions.

- MOV performs a bit or a byte transfer from the source operand to the destination operand.
- PUSH increments the SP register and then transfers a byte from the source operand to the stack element currently addressed by SP.
- POP transfers a byte operand from the stack element addressed by the SP register to the destination operand and then decrements SP.

Accumulator-Specific Transfers

Four accumulator-specific transfer operations are provided:

- XCH exchanges the byte source operand with register A (accumulator).
- XCHD exchanges the low-order nibble of the byte source operand with the low-order nibble of register A.
- MOVX performs a byte move between the External Data Memory and the A register. The external address can be specified by the DPTR register (16-bit) or the R1 or R0 register (8-bit).
- MOVC performs the move of a byte from the Program Memory to register A as follows. The operand in the A register is used as an index into a 256-byte table pointed to by the base register (DPTR or PC). The byte operand accessed is transferred to A. MOVC is used for table-look-up byte translation and for accessing operands from code-in-line tables.

Address-Object Transfer

- MOV DPTR,#data loads 16-bits of immediate data into a pair of destination registers, DPH and DPL (DHP from low-order address, DPL from high-order address).

8.1.2 Logic

The 8051 performs the basic logic operations on both bit and byte operands.

Single-Operand Operations

Seven single-operand logical operations are provided:

- CLR is used to set either the A register, the C register, or any Direct Addressed bit to zero (0).

- SETB sets either the C register or any Direct Addressed bit to one (1).
- CPL either forms the one's complement of the operand in the A register and returns the result to the A register without affecting flags or forms the one's complement of the C register or any Direct Addressed bit.
- RL, RLC, RR, RRC, SWAP. Five rotate operations can be performed on the A register; RL (rotate left), RR (rotate right), RLC (rotate left through C), RRC (rotate right through C), and SWAP (rotate left four). For RLC and RRC the C flag becomes equal to the last bit rotated out. SWAP rotates the A register left four places to exchange bits 3 through 0 with bits 7 through 4.

Two-Operand Operations

Three two-operand logical operations are provided:

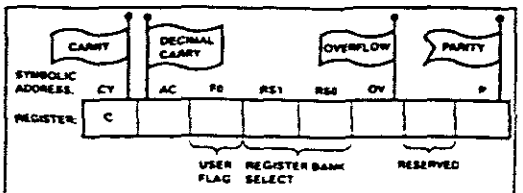
- ANL peforms the bitwise logical conjunction of two source operands (for both bit and byte operands) and returns the result to the location of the first operand.
- ORL performs the bitwise logical inclusive disjunction of two source operands (for both bit and byte operands) and returns the result of the location of the first operand.
- XRL performs the bitwise logical exclusive disjunction of the two source operands (byte operands) and returns the result to the location of the first operand.

8.1.3 Arithmetic

The 8051 provides the four basic mathematical operations. Only 8-bit operations using unsigned arithmetic are supported directly. The overflow flag permits the addition and subtraction operation to serve for both unsigned and signed binary integers. A correction operation is also provided to allow arithmetic to be performed directly on packed decimal (BCD) representations.

Flag Register Settings

Three one-bit flag registers are set or cleared by arithmetic operations to reflect certain properties of the result of the operation. These flags are not affected by the increment and decrement instructions. A fourth flag (P) denotes the parity of the eight accumulator bits. These flag registers are located in the Program Status Word (PSW) register. Their bit assignment are shown below. A list of the instructions that affect these flags is provided in the "8051 Instruction Set Summary" in Table 8-1.



Function	Flag	Bit Location
Carry Flag (also the C register)	CY:	PSW.7:
Auxiliary-Carry Flag	AC:	PSW.6:
Overflow Flag	OV:	PSW.2:
Parity Flag	P:	PSW.0:
User Flag 0	F0:	PSW.5:
reserved	—:	PSW.1:
Register Select MSb	RS1:	PSW.4:
Register Select LSb	RS0:	PSW.3:

Unless otherwise stated, the instructions obey these rules:

- CY is set if the operation result in a carry out of (during addition) or a borrow into (during subtraction) the high-order bit of the result; otherwise CY is cleared.
- AC is set if the operation results in a carry out of the low-order four bits of the result (during addition) or a borrow from the high-order bits into the low-order 4 bits (during subtraction); otherwise AC is cleared.
- OV is set if the operation results in a carry into the high-order bit of the result but not a carry out of the high-order bit, or vice versa; otherwise OV is cleared. OV is of use to two's-complement arithmetic, since it becomes set when the signed result cannot be represented in 8 bits.
- P is set if the module 2 sum of the eight bits in the accumulator is 1 (odd parity); otherwise P is cleared (even parity). When a value is written to the PSW register, the P bit remains unchanged, as it always reflects the parity of A.

Addition

Four addition operations are provided:

- INC (increment) performs an addition of the source operand and one (1) and returns the result to the operand.
- ADD performs an addition between the A register and the second source operand and returns the result to the A register.
- ADDC (add with Carry) performs an addition between the A register and the second source operand; adds one (1) if the C flag is found previously set and returns the result to register A.
- DA (decimal-add-adjust for BCD addition) performs a correction to the sum which resulted from the binary addition of two two-digit decimal operands. The packed decimal sum formed by DA is returned to A. The carry flag is set if the BCD result is greater than 99; or else it is cleared.

Subtraction

Two subtraction operations are provided:

- SUBB (subtract with borrow) performs a subtraction of the second source operand from the first operand (the accumulator), subtracts one (1) if the C flag is found previously set and returns the result to the A register.
- DEC (decrement) performs a subtraction of one (1) from the source operand and returns the results to the operand.

Multiplication

- MUL performs an unsigned multiplication of the A register by the B register, returning a double-byte result. Register A receives the low-order byte, B receives the high-order byte. OV is cleared if the top half of the result is zero and is set if it is non-zero. C is cleared. AC remains unaltered.

Division

- DIV performs an unsigned division of the A register by the B register and returns the integer quotient to register A and returns the fractional remainder to the B register. Division by zero leaves indeterminate data in registers A and B and sets OV, otherwise OV is cleared. C is cleared. AC remains unaltered.

8.1.4 Control Transfer

There are three classes of control transfer operations: unconditional calls, returns and jumps; conditional jumps; and interrupts. All control transfer operations cause, some upon a specific condition, the program execution to continue at a non-sequential location in program memory.

Unconditional Calls, Returns and Jumps

Unconditional calls, returns and jumps transfer control from the current value of the Program Counter to the target address. Both direct and indirect transfers are supported. The three transfer operations are described below.

- ACALL and LCALL push the address of the next instruction onto the stack (PCL to low-order address, PCH to high-order address) and then transfer control to the target address. Absolute Call is a 2-byte instruction used when the target address is in the current 2K page. Long Call is a 3-byte instruction that addresses the full 64K program space. In ACALL, immediate data (i.e. and 11 bit address field) is concatenated to the five most significant bits of the PC (which is pointing to the next instruction). If ACALL is in the last 2 bytes of a 2K page then the call will be made to the next page since the PC will have been incremented to the next instruction prior to execution.
- RET transfers control to the return address saved on the stack by a previous call operation and decrements the SP register by two (2) to adjust the SP for the popped address.
- AJMP, LJMP and SJMP transfer control to the target operand. The operation of AJMP and LJMP are analogous to ACALL and LCALL. The SJMP (short jump) instruction provides for transfers within a 256 byte range centered about the starting address of the next instruction (-128 to +127). The PC-relative short jump facilitates relocatable code.
- JMP @ A+DPTR performs a jump relative to the DPTR register. The operand in the A register is used as the offset (0-255) to the address in the DPTR register. Thus, the effective destination for a jump can be anywhere in the Program Memory space. This indirect jump is also useful for implementing N-way branches.

Conditional Jumps

In the control transfer group, the conditional jumps perform a jump contingent upon a specific condition. The destination will be within a 256-byte range centered about the starting address of the next instruction (-128 to +127).

- JZ performs a jump if the accumulator is zero.
- JNZ performs a jump if the accumulator is not zero.
- JC performs a jump if the carry flag is set.
- JNC performs a jump if the carry flag is not set.
- JB peforms a jump if the Direct Addressed bit is set.
- JNB performs a jump if the Direct Addressed bit is not set.
- JBC performs a jump if the Direct Addressed bit is set and then clears the Direct Addressed bit.

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Unconditional Calls, Returns and Jumps

Unconditional calls, returns and jumps transfer control from the current value of the Program Counter to the target address. Both direct and indirect transfers are supported. The three transfer operations are described below.

- ACALL and LCALL push the address of the next instruction onto the stack (PCL to low-order address, PCH to high-order address) and then transfer control to the target address. Absolute Call is a 2-byte instruction used when the target address is in the current 2K page. Long Call is a 3-byte instruction that addresses the full 64K program space. In ACALL, immediate data (i.e. and 11 bit address field) is concatenated to the five most significant bits of the PC (which is pointing to the next instruction). If ACALL is in the last 2 bytes of a 2K page then the call will be made to the next page since the PC will have been incremented to the next instruction prior to execution.
- RET transfers control to the return address saved on the stack by a previous call operation and decrements the SP register by two (2) to adjust the SP for the popped address.
- AJMP, LJMP and SJMP transfer control to the target operand. The operation of AJMP and LJMP are analogous to ACALL and LCALL. The SJMP (short jump) instruction provides for transfers within a 256 byte range centered about the starting address of the next instruction (-128 to +127). The PC-relative short jump facilitates relocatable code.
- JMP @ A+DPTR performs a jump relative to the DPTR register. The operand in the A register is used as the offset (0-255) to the address in the DPTR register. Thus, the effective destination for a jump can be anywhere in the Program Memory space. This indirect jump is also useful for implementing N-way branches.

Conditional Jumps

In the control transfer group, the conditional jumps perform a jump contingent upon a specific condition. The destination will be within a 256-byte range centered about the starting address of the next instruction (-128 to +127).

- JZ performs a jump if the accumulator is zero.
- JNZ performs a jump if the accumulator is not zero.
- JC performs a jump if the carry flag is set.
- JNC performs a jump if the carry flag is not set.
- JB peforms a jump if the Direct Addressed bit is set.
- JNB performs a jump if the Direct Addressed bit is not set.
- JBC performs a jump if the Direct Addressed bit is set and then clears the Direct Addressed bit.

Table 8-1. 8051 Instruction Set Summary

Interrupt Response Time: To finish execution of current instruction, respond to the interrupt request, push the PC and to vector to the first instruction of the interrupt service program requires 38 to 81 oscillator periods (3 to 7μs @ 12 MHz).

INSTRUCTIONS THAT AFFECT FLAG SETTINGS'

INSTRUCTION	FLAG			INSTRUCTION	FLAG		
	C	OV	AC		C	OV	AC
ADD	X	X	X	CLR C	0		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C,bit	X		
MUL	0	X		ANL C,/bit	X		
DIV	0	X		ORL C,bit	X		
DA	X			ORL C,bit	X		
RRC	X			MOV C,bit	X		
RLC	X			CJNE	X		
SETB C	1						

'Note that operations on SFR byte address 208 or bit addresses 209-215 (i.e. the PSW or bits in the PSW) will also affect flag settings.

Notes on instruction set and addressing modes:

- **Rn** — Register R7-R0 of the currently selected Register Bank.
- **data** — 8-bit internal data location's address. This could be an Internal Data RAM location (0-127) or a SFR [i.e. I/O port, control register, status register, etc. (128-255)].
- **@Ri** — 8-bit internal data RAM location (0-255) addressed indirectly through register R1 or R0.
- **#data** — 8-bit constant included in instruction.
- **#data 16** — 16-bit constant included in instruction
- **addr16** — 16-bit destination address. Used by LCALL & LJMP. A branch can be anywhere within the 64K-byte Program Memory address space.
- **addr11** — 11-bit destination address. Used by ACALL & AJMP. The branch will be within the same 2K-byte page of program memory as the first byte of the following instruction.
- **rel** — Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is -128 to +127 bytes relative to first byte of the following instruction.
- **bit** — Direct Addressed bit in Internal Data RAM or Special Function Register.
- ***** — New operation not provided by 8048/8049.

ARITHMETIC OPERATIONS

	Mnemonic	Description	Byte	Oscillator Period
ADD	A,Rn	Add register to Accumulator	1	12
ADD	A,direct	Add direct byte to Accumulator	2	12
ADD	A,@Ri	Add indirect Ram to Accumulator	1	12
ADD	A,#data	Add immediate data to Accumulator	2	12
ADDC	A,Rn	Add register to Accumulator with Carry	1	12
ADDC	A,direct	Add direct byte to Accumulator with Carry	2	12
ADDC	A,@Ri	Add indirect RAM to Accumulator with Carry	1	12
ADDC	A,#data	Add immediate data to Acc with Carry	2	12
SUBB	A,Rn	Subtract register from Acc with borrow	1	12

ARITHMETIC OPERATIONS Cont.

	Mnemonic	Description	Byte	Oscillator Period
SUBB	A,direct	Subtract direct byte from Acc with borrow	2	12
SUBB	A,@Ri	Subtract indirect RAM from Acc with borrow	1	12
SUBB	A,#data	Subtract immediate data from Acc with borrow	2	12
INC	A	Increment Accumulator	1	12
INC	Rn	Increment register	1	12
INC	direct	Increment direct byte	2	12
INC	@Ri	Increment indirect RAM	1	12
DEC	A	Decrement Accumulator	1	12
DEC	Rn	Decrement Register	1	12
DEC	direct	Decrement direct byte	2	12
DEC	@Ri	Decrement indirect RAM	1	12

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Table 8-1. Instruction Set Summary (continued)

ARITHMETIC OPERATIONS Cont.

Mnemonic		Description	Byte	Oscillator Period
INC	DPTR	Increment Data Pointer	1	24
MUL	AB	Multiply A & B	1	48
DIV	AB	Divide A by B	1	48
DA	A	Decimal Adjust Accumulator	1	12

LOGICAL OPERATIONS

Mnemonic		Description	Byte	Oscillator Period
ANL	A,Rn	AND register Accumulator	1	12
ANL	A,direct	AND direct byte to Accumulator	2	12
ANL	A,@Ri	AND indirect RAM to Accumulator	1	12
ANL	A,#data	AND immediate data to Accumulator	2	12
ANL	direct,A	AND Accumulator to direct byte	2	12
ANL	direct,#data	AND immediate data to direct byte	3	24
ORL	A,Rn	OR register to Accumulator	1	12
ORL	A,direct	OR direct byte to Accumulator	2	12
ORL	A,@Ri	OR indirect RAM to Accumulator	1	12
ORL	A,#data	OR immediate data to Accumulator	2	12
ORL	direct,A	OR Accumulator to direct byte	2	12
ORL	direct,#data	OR immediate data to direct byte	3	24
XRL	A,Rn	Exclusive-OR register to Accumulator	1	12
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	12
XRL	A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	12
XRL	A,#data	Exclusive-OR immediate data to Accumulator	2	12

LOGICAL OPERATIONS Cont.

Mnemonic		Description	Byte	Oscillator Period
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	12
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	24
CLR	A	Clear Accumulator	1	12
CPL	A	Complement Accumulator	1	12
RL	A	Rotate Accumulator Left	1	12
RLC	A	Rotate Accumulator Left through the Carry	1	12
RR	A	Rotate Accumulator Right	1	12
RRC	A	Rotate Accumulator Right through the Carry	1	12
SWAP	A	Swap nibbles within the Accumulator	1	12

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Table 8-1. Instruction Set Summary (continued)

DATA TRANSFER

Mnemonic		Description	Byte	Oscillator Period
MOV	A,Rn	Move register to Accumulator	1	12
MOV	A,direct	Move direct byte to Accumulator	2	12
MOV	A,@Ri	Move indirect RAM to Accumulator	1	12
MOV	A,#data	Move immediate data to Accumulator	2	12
MOV	Rn,A	Move Accumulator to register	1	12
MOV	Rn,direct	Move direct byte to register	2	24
MOV	Rn,#data	Move immediate data to register	2	12
MOV	direct,A	Move Accumulator to direct byte	2	12
MOV	direct,Rn	Move register to direct byte	2	24
MOV	direct,direct	Move direct byte to direct	3	24
MOV	direct,@Ri	Move indirect RAM to direct byte	2	24
MOV	direct,#data	Move immediate data to direct byte	3	24
MOV	@Ri,A	Move Accumulator to indirect RAM	1	12
MOV	@Ri,direct	Move direct byte to indirect RAM	2	24
MOV	@Ri,#data	Move immediate data to indirect RAM	2	12
MOV	DPTR,#data16	Load Data Pointer with a 16-bit constant	3	24
MOVC	A,@A + DPTR	Move Code byte relative to DPTR to Acc	1	24
MOVC	A,@A + PC	Move Code byte relative to PC and Acc	1	24
MOVX	A,@Ri	Move External RAM (8-bit addr) to Acc	1	24
MOVX	A,@DPTR	Move External RAM (16-bit addr) to Acc	1	24

DATA TRANSFER Cont.

Mnemonic		Description	Byte	Oscillator Period
MOVX	@Ri,A	Move Acc to External RAM (8-bit addr)	1	24
MOVX	@DPTR,A	Move Acc to External Ram (16-bit addr)	1	24
PUSH	direct	Push direct byte onto stack	2	24
POP	direct	Pop direct byte from stack	2	24
XCH	A,Rn	Exchange register with Accumulator	1	12
XCH	A,direct	Exchange direct byte with Accumulator	2	12
XCH	A,@Ri	Exchange indirect RAM with Accumulator	1	12
XCHD	A,@Ri	Exchange low-order Digit indirect RAM with Acc	1	12

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Table 8-1. Instruction Set Summary (continued)

BOOLEAN VARIABLE MANIPULATION

Mnemonic		Description	Byte	Oscillator Period
CLR	C	Clear Carry	1	12
CLR	bit	Clear direct bit	2	12
SETB	C	Set Carry	1	12
SETB	bit	Set direct bit	2	12
CPL	C	Complement Carry	1	12
CPL	bit	Complement direct bit	2	12
ANL	C,bit	AND direct bit to Carry	2	24
ANL	C,/bit	AND complement of direct bit to Carry	2	24
ORL	C,bit	OR direct bit to Carry	2	24
ORL	C,/bit	OR complement of direct bit to Carry	2	24
MOV	C,bit	Move direct bit to Carry	2	12
MOV	bit,C	Move Carry to direct bit	2	24
JC	rel	Jump if Carry is set	2	24
JNC	rel	Jump if Carry not set	2	24
JB	bit,rel	Jump if direct Bit is set	3	24
JNB	bit,rel	Jump if direct Bit is Not set	3	24
JBC	bit,rel	Jump if direct Bit is set & clear bit	3	24

PROGRAMING BRANCHING

Mnemonic		Description	Byte	Oscillator Period
ACALL	addr11	Absolute Subroutine Call	2	24
LCALL	addr16	Long Subroutine Call	3	24
RET		Return for Subroutine	1	24
RETI		Return for interrupt	1	24
AJMP	addr11	Absolute Jump	2	24
LJMP	addr16	Long Jump	3	24
SJMP	rel	Short Jump (relative addr)	2	24
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	24
JZ	rel	Jump if Accumulator is Zero	2	24

PROGRAM BRANCHING Cont.

Mnemonic		Description	Byte	Oscillator Period
JNZ	rel	Jump if Accumulator is Not Zero	2	24
CJNE	A,direct,rel	Compare direct byte to Acc and Jump if Not Equal	3	24
CJNE	A,#data,rel	Comare immediate to Acc and Jump if Not Equal	3	24
CJNE	RN,#data,rel	Compare immediate to register and Jump if Not Equal	3	24
CJNE	@Ri,#data,rel	Compare immediate to indirect and Jump if Not Equal	3	24
DJNZ	Rn,rel	Decrement register and Jump if Not Zero	3	24
DJNZ	direct,rel	Decrement direct byte and Jump if Not Zero	3	24
NOP		No Operation	1	12

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- CJNE compares the first operand to the second operand and performs a jump if they are not equal. *C* is set if the first operand is less than the second operand; else it is cleared. Comparisons can be made between the A register and Direct Addressable bytes in the Internal Data Memory or between an immediate value and either the A register, an RB register in the selected Register Bank, or a Register-Indirect addressed byte of the Internal Data RAM.
- DJNZ decrements the source operand and returns the result to the operand. A jump is performed if the result is not zero. The DJNZ instruction makes a RAM location efficient for use as a program loop counter by allowing the programmer to decrement and test the counter in a single instruction. The source operand of the DJNZ instruction may be any byte in the Internal Data Memory. Either Direct or Register Addressing may be used to address the source operand.

Interrupts

Program execution control may be transferred by means of internal and external interrupts. All interrupts perform a transfer by pushing the Program Counter onto the stack and then branching to programs located at absolute locations 3, 11, 19, 27 and 35 in the Program Memory. The programmer must push all registers that will be altered by his interrupt service program onto the stack to avoid corruption. Only one interrupt transfer operation is necessary:

- RETI transfers control in a manner identical to RET. In addition, RETI reenables interrupts for the current priority level.

See section 2.3.1 for further details on the operation and control of the interrupt system.

8.2 Instruction Definitions

The rest of this chapter defines all the instructions and operations which the MCS-51 CPU can perform. There is a separate section for each of the 51 basic operations, ordered alphabetically according to the operation mnemonic.

When an operation may apply to more than one data type (generally bit and byte data), the MCS-51 assembly language uses the same mnemonic for each, reducing the number of mnemonics the programmer must remember. The assembler determines which instruction is appropriate from the operands specified. Thus, the mnemonic "CLR" can operate on the eight-bit accumulator ("CLR A"), or on one-bit variables ("CLR F0"). The mnemonics ANL, ORL, CPL, and MOV can relate to more than one data type as well. These operations present each data type in a separate section.

Each section then describes the action taken by the operation, the flags and registers affected, and shows a short example of how an instruction might be used in a program. Next comes the number of bytes and machine cycles required, the corresponding binary machine-language encoding, and a symbolic description or restatement of the function implemented.

Note: Only the carry, auxiliary-carry, and overflow flags are discussed in these instruction descriptions. Since the parity bit (PSW.0) is recomputed *after every instruction cycle* any instruction that alters the accumulator — either inherently or as a special function

register — could affect the parity flag. Similarly, instructions which alter directly addressed registers could affect the other status flags if the instruction is applied to the PSW. Status flags can also be modified by the generalized bit-manipulation instructions.

Nineteen operations allow more than one addressing mode for the source and/or destination operand. The headings for these sections show the instruction format with such operands enclosed in angle brackets (for example, MOV <dest-byte>, <src-byte>). The operation description tells what modes (or combinations of modes) are allowed, and gives the assembly language notation, byte and cycle counts, encoding format, and a symbolic description for each.

The information in this chapter is directed towards defining the capabilities of the MCS-51 architecture and hardware. For details on the assembly language or ASM51 capabilities refer to the *MCS-51 Macro Assembler User's Guide,* publication number 9800937.

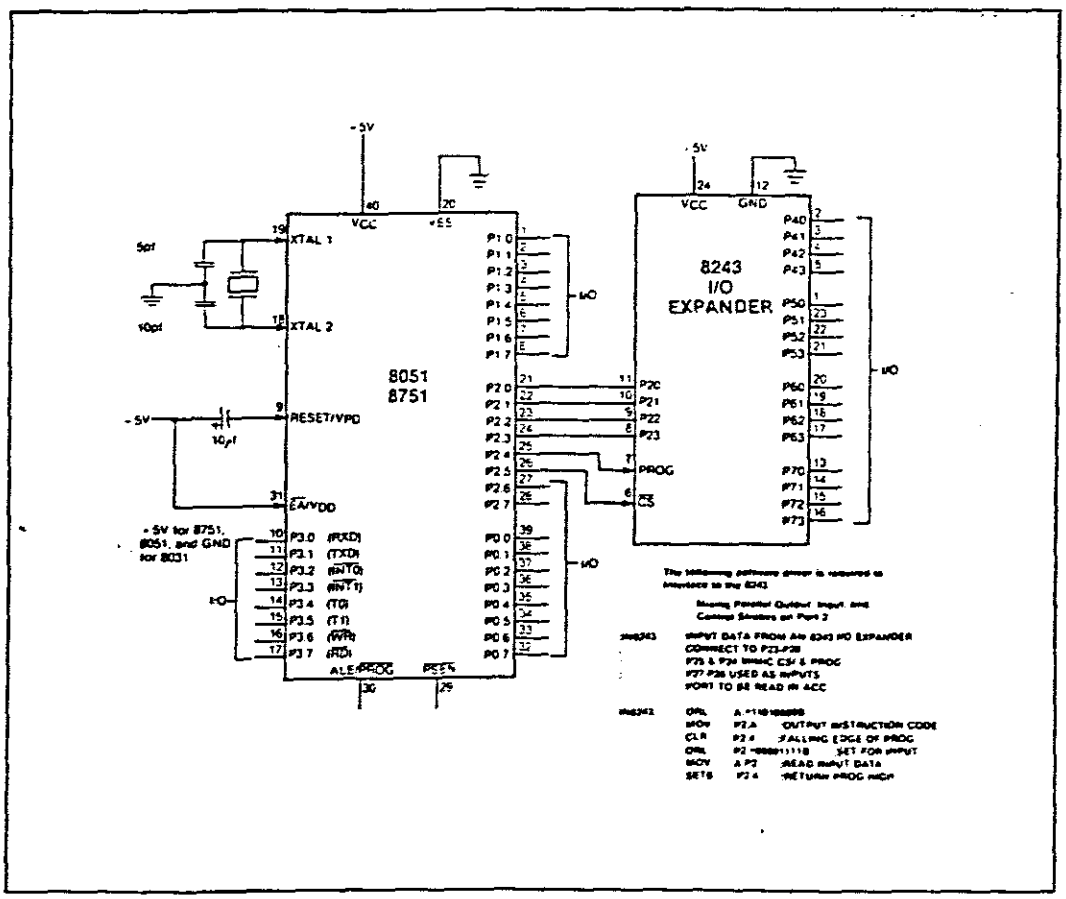


Figure 9-3. I/O Expansion Using an 8243

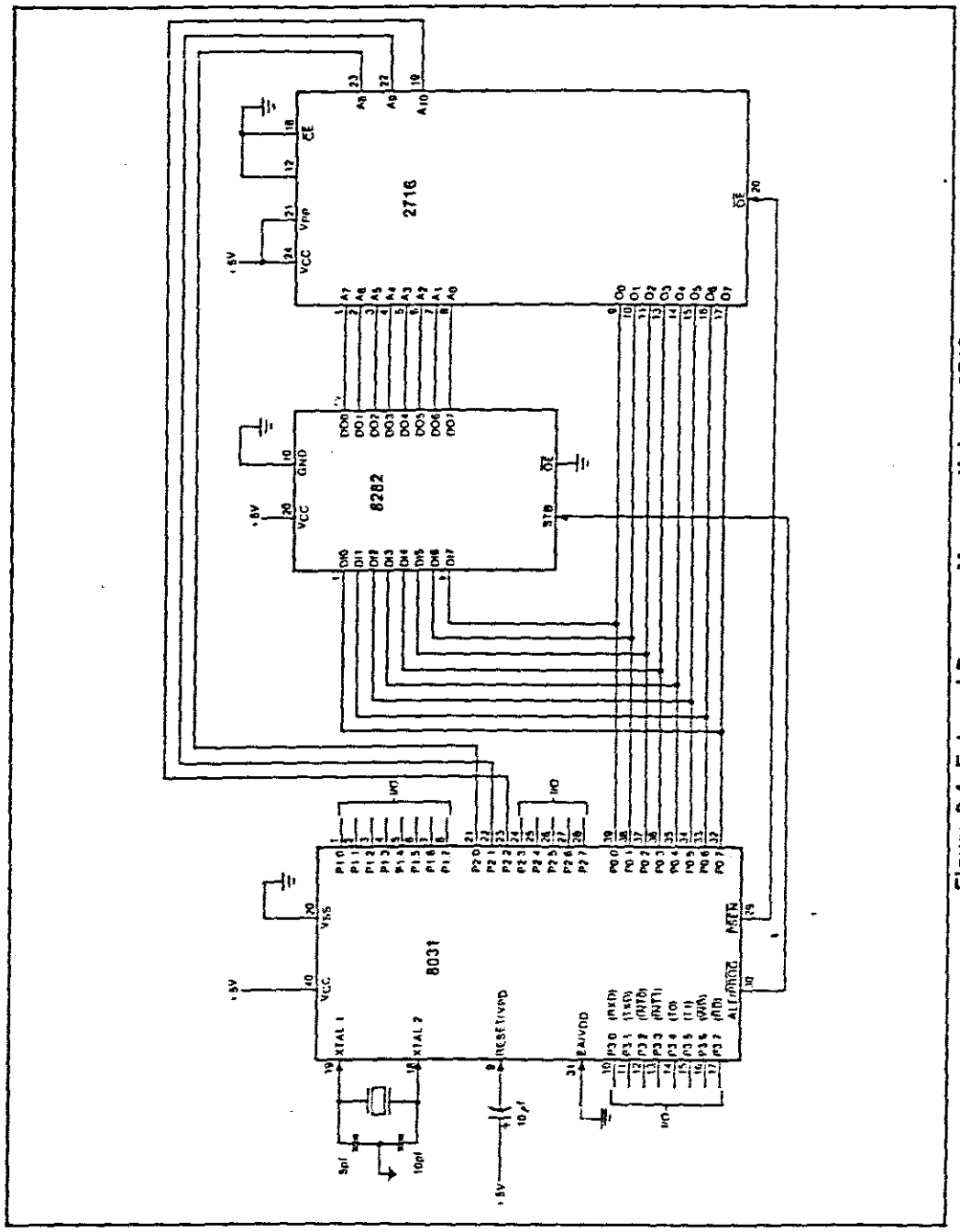


Figure 8-4. External Program Memory Using a 2716

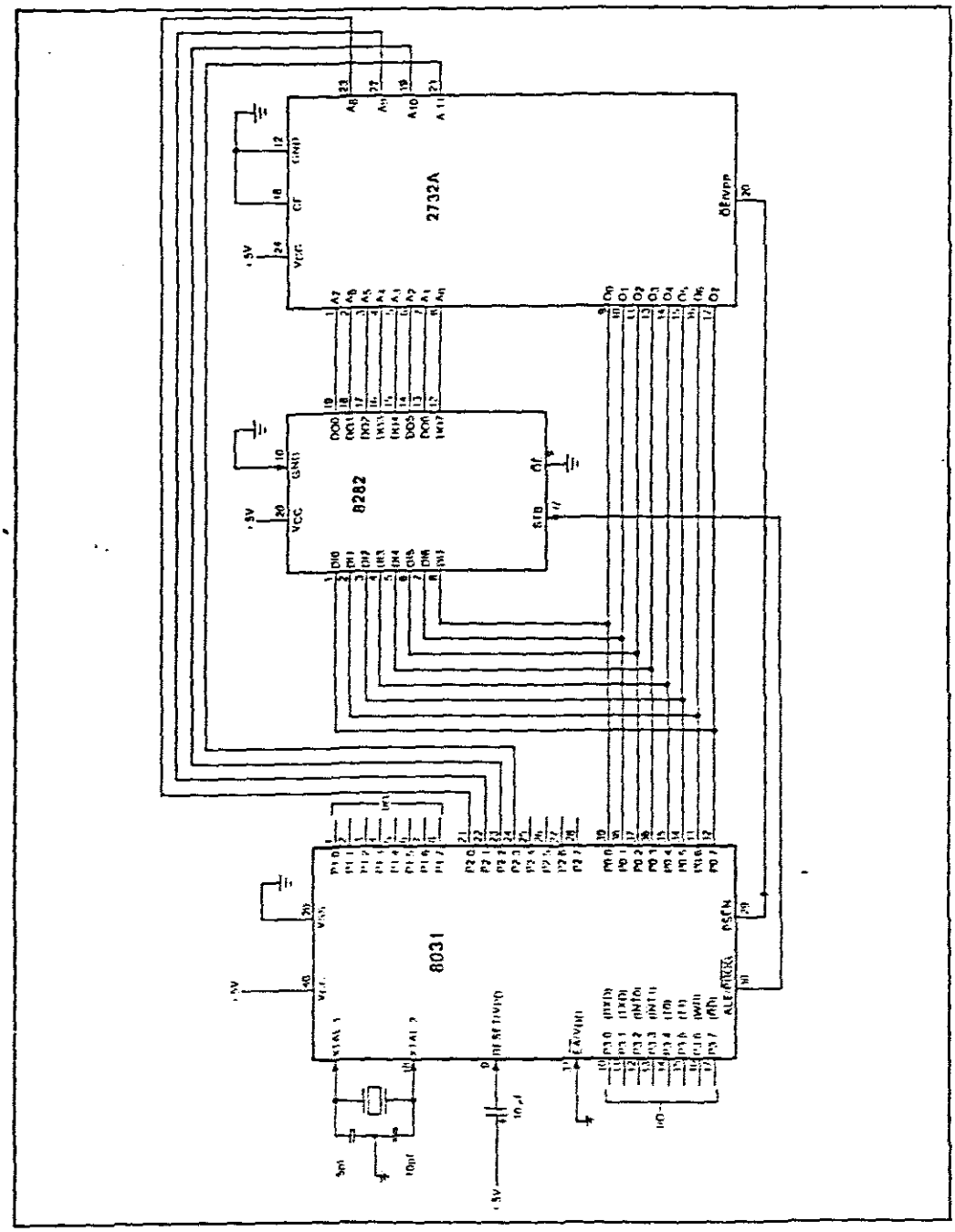


Figure 9-5. External Program Memory Using a 2732

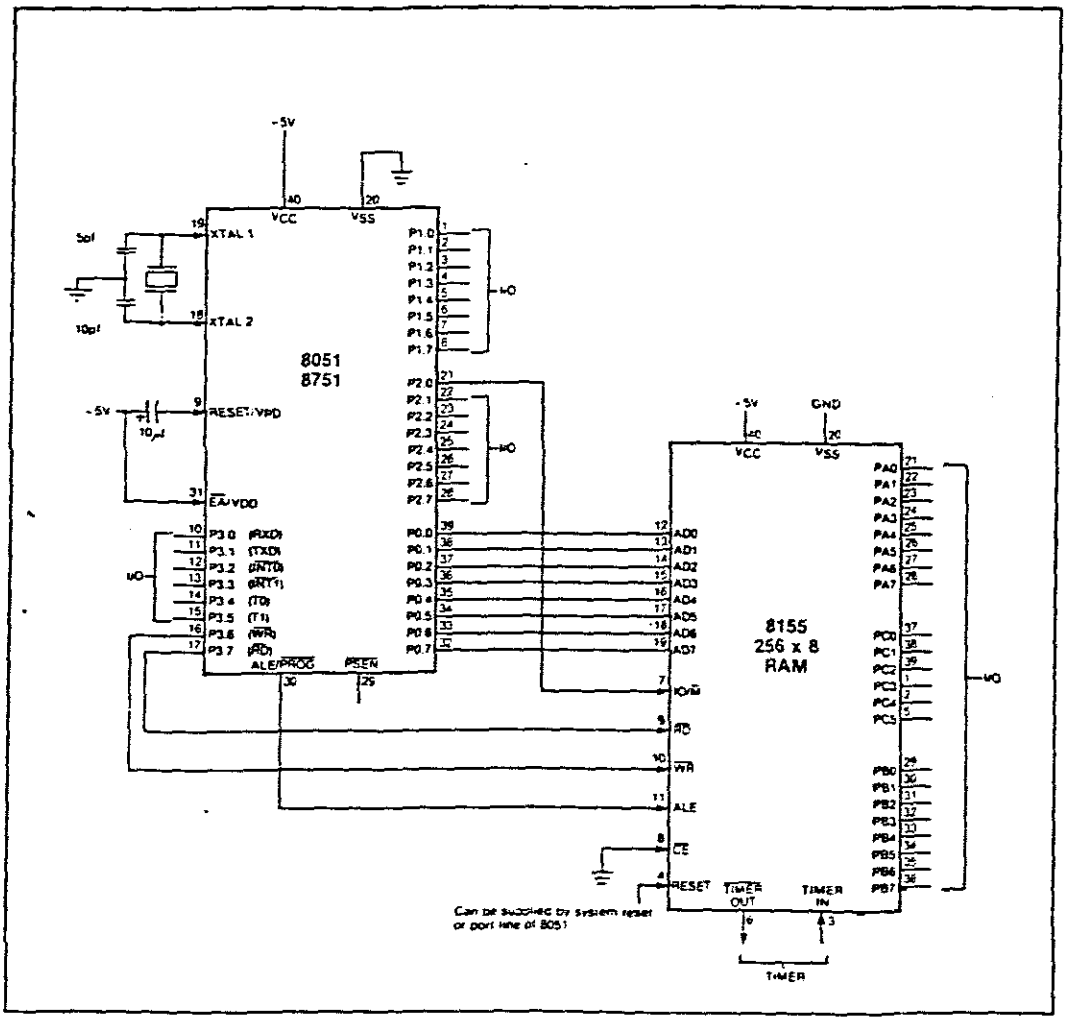


Figure 9-6. Adding a Data Memory and I/O Expander

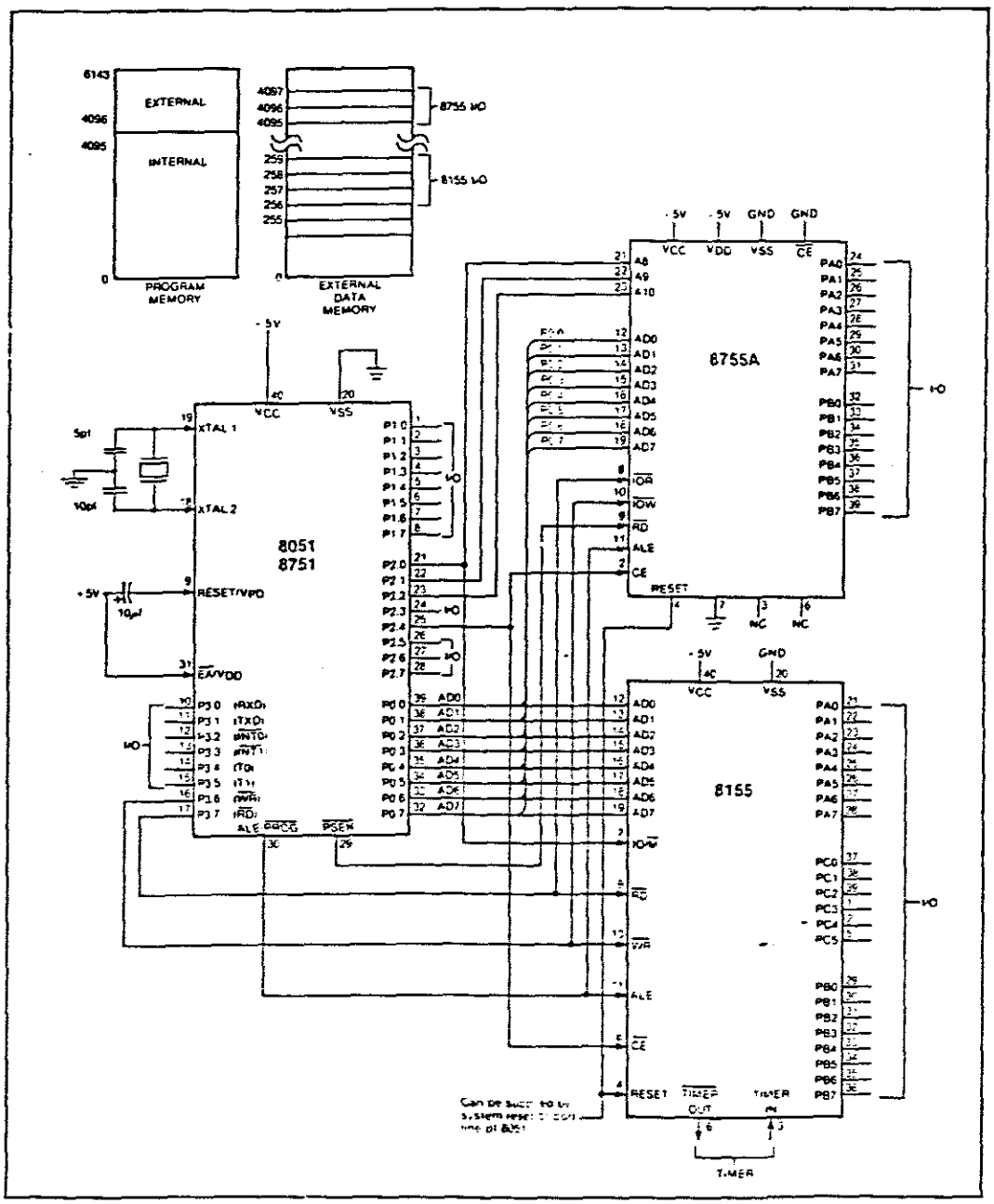


Figure 9-7. The Three-Chip System

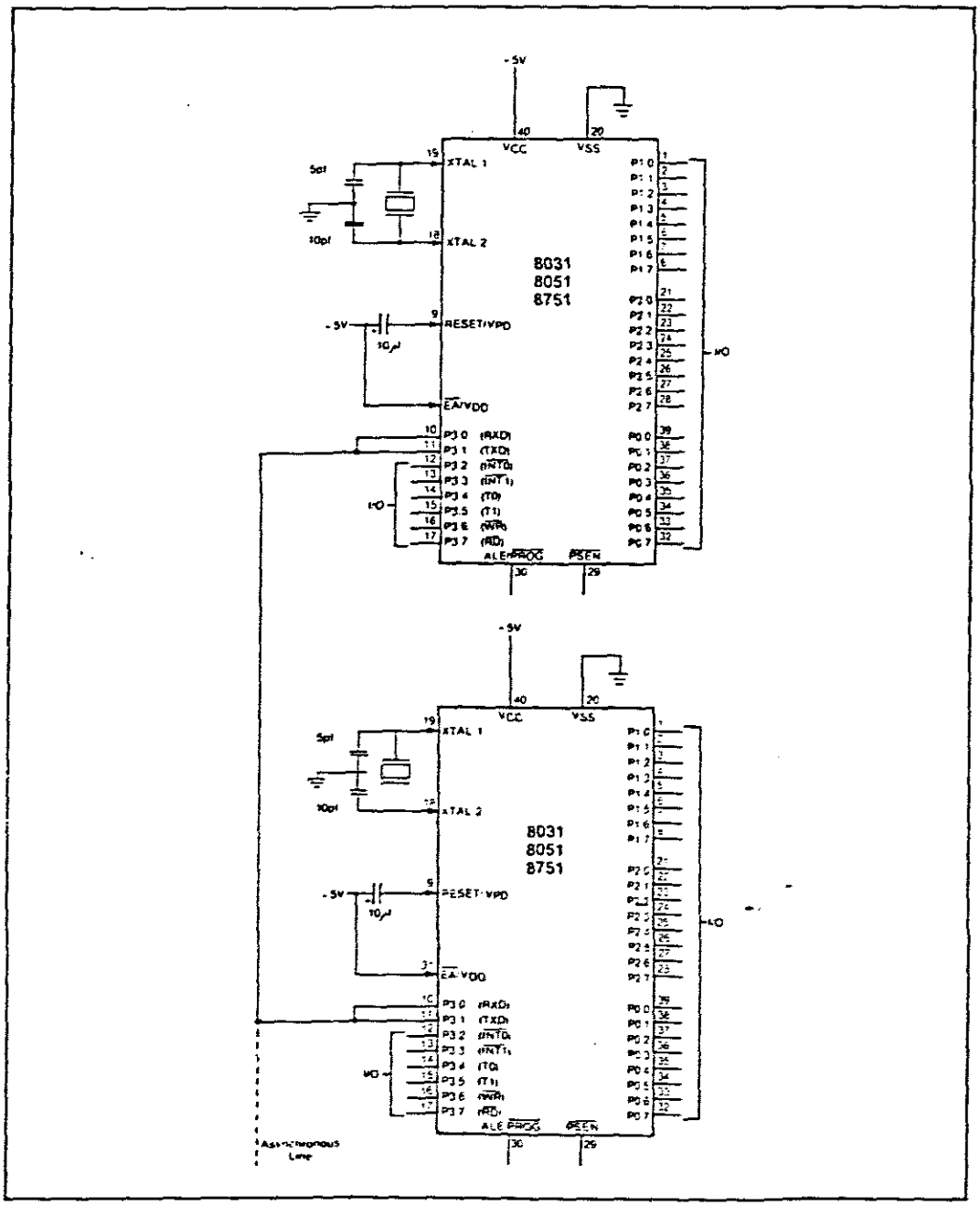


Figure 9-8. Multiple 8051's Using Half-Duplex Serial Communication

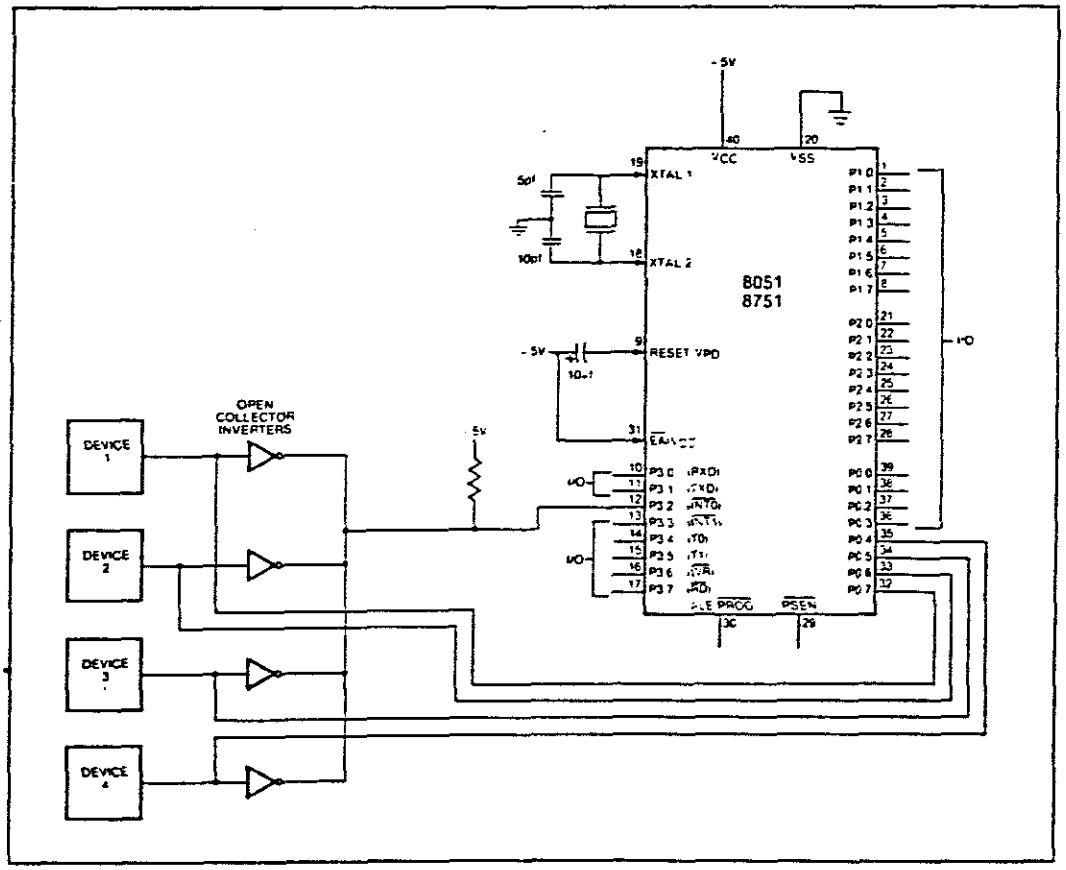
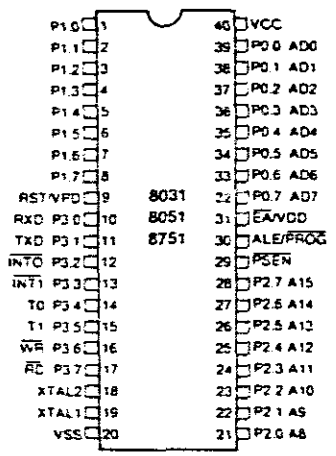


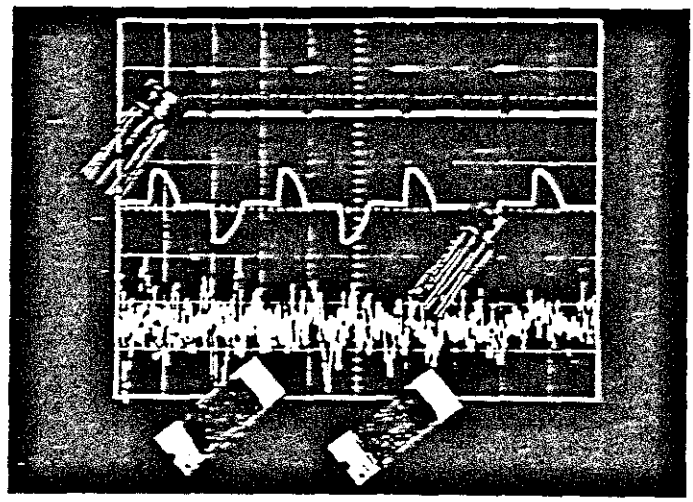
Figure 9-9. Multiple Interrupt Sources



ANALOG DEVICES

Integrated Circuit True rms-to-dc Converter

AD536A



FEATURES

True rms-to-dc Conversion
Laser-Trimmed to High Accuracy
  0.2% max Error (AD536AK)
  0.5% max Error (AD536AJ)
Wide Response Capability:
  Computes rms of ac and dc Signals
  450kHz Bandwidth: $V_{rms} > 100mV$
  2MHz Bandwidth: $V_{rms} > 1V$
  Signal Crest Factor of 7 for 1% Error
dB Output with 60dB Range
Low Power: 1.2mA Quiescent Current
Single or Dual Supply Operation
Monolithic Integrated Circuit
-55°C to +125°C Operation (AD536AS)
Low Cost

ODUCT DESCRIPTION

e AD536A is a complete monolithic integrated circuit which forms true rms-to-dc conversion. It offers performance ich is comparable or superior to that of hybrid or modular s costing much more. The AD536A directly computes the e rms value of any complex input waveform containing ac dc components. It has a crest factor compensation scheme ch allows measurements with 1% error at crest factors up 7. The wide bandwidth of the device extends the measure- t capability to 300kHz with 3dB error for signal levels ve 100mV.

important feature of the AD536A not previously available ms converters is an auxiliary dB output. The logarithm of rms output signal is brought out to a separate pin to allow dB conversion, with a useful dynamic range of 60dB. Using xternally supplied reference current, the 0dB level can be veniently set by the user to correspond to any input level n 0.1 to 2 volts rms.

e AD536A is laser trimmed at the wafer level for input and put offset, positive and negative waveform symmetry (dc rsal error), and full scale accuracy at 7V rms. As a result, xternal trims are required to achieve the rated accuracy e unit.

re is full protection for both inputs and outputs. The input uitry can take overload voltages well beyond the supply ls. Loss of supply voltage with inputs connected will not se unit failure. The output is short-circuit protected.

e AD536A is available in two accuracy grades (J, K) for mercial temperature range (0 to +70°C) applications, and grade (S) rated for the -55°C to +125°C extended range. e AD536AK offers a maximum total error of ±2mV ±0.2% of reading and the AD536AJ and AD536AS have maximum errors of ±5mV ±0.5% of reading. All three versions are available in either a hermetically sealed 14-pin DIP or 10-pin TO-100 metal can.

PRODUCT HIGHLIGHTS

1. The AD536A computes the true root-mean-square level of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it relates directly to the power of the signal. The rms value of a statistical signal also relates to its standard deviation.
2. The crest factor of a waveform is the ratio of the peak signal swing to the rms value. The crest factor compensation scheme of the AD536A allows measurement of highly complex signals with wide dynamic range.
3. The only external component required to perform measurements to the fully specified accuracy is the capacitor which sets the averaging period. The value of this capacitor determines the low frequency ac accuracy, ripple level and settling time.
4. The AD536A will operate equally well from split supplies or a single supply with total supply levels from 5 to 36 volts. The one milliampere quiescent supply current makes the device well-suited for a wide variety of remote controllers and battery powered instruments.
5. The AD536A directly replaces the AD536, and provides improved bandwidth and temperature drift specifications.

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Telex: 924491 Cables: ANALOG NORWOODMASS

PECIFICATIONS (@ +25°C, and ±15V dc unless otherwise noted)

del	AD536AJ Min	AD536AJ Typ	AD536AJ Max	AD536AK Min	AD536AK Typ	AD536AK Max	AD536AS Min	AD536AS Typ	AD536AS Max	Units
NSFER FUNCTION		$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$		
VERSION ACCURACY										
ial Error, Internal Trim[1] (Figure 1)			±5 ±0.5			±2 ±0.2			±5 ±0.5	mV ± % of Reading
vs. Temperature, T_{min} to +70°C			±0.1 ±0.01			±0.05 ±0.005			±0.1 ±0.005	mV ± % of Reading/°C
+70°C to +125°C									±0.3 ±0.005	mV ± % of Reading/°C
vs. Supply Voltage		±0.1 ±0.01			±0.1 ±0.01			±0.1 ±0.01		mV ± % of Reading/V
dc Reversal Error		±0.2			±0.1			±0.2		± % of Reading
al Error, External Trim[1] (Figure 2)		±3 ±0.3			±2 ±0.1			±3 ±0.3		mV ± % of Reading
OR VS. CREST FACTOR[2]										
s: Factor 1 to 2		Specified Accuracy			Specified Accuracy			Specified Accuracy		
s: Factor = 3		−0.1			−0.1			−0.1		% of Reading
s: Factor = 7		−1.0			−1.0			−1.0		% of Reading
UENCY RESPONSE[3]										
dwidth for 1% additional error (0.09dB)										
V_{IN} = 10mV		5			5			5		kHz
V_{IN} = 100mV		45			45			45		kHz
V_{IN} = 1V		120			120			120		kHz
3dB Bandwidth										
V_{IN} = 10mV		90			90			90		kHz
V_{IN} = 100mV		450			450			450		kHz
V_{IN} = 1V		2.3			2.3			2.3		MHz
ERAGING TIME CONSTANT (Figure 5)		25			25			25		ms/μF CAV
PUT CHARACTERISTICS										
gnal Range, ±15V Supplies										
Continuous rms Level		0 to 7			0 to 7			0 to 7		V rms
Peak Transient Input			±20			±20			±20	V peak
Continuous rms Level, ±5V Supplies		0 to 2			0 to 2			0 to 2		V rms
Peak Transient Input, ±5V Supplies			±7			±7			±7	V peak
aximum Continuous Nondestructive										
Input Level (All Supply Voltages)			±25			±25			±25	V peak
put Resistance	13.33	16.67	20	13.33	16.67	20	13.33	16.67	20	kΩ
put Offset Voltage		0.8	±2		0.5	±1		0.8	±2	mV
PUT CHARACTERISTICS										
set Voltage, V_{IN} = COM (Figure 1)		±1	±2		±0.5	±1			±2	mV
vs. Temperature		±0.1			±0.1				±0.2	mV/°C
vs. Supply Voltage		±0.1			±0.1			±0.2		mV/V
tage Swing, ±15V Supplies	0 to +11	+12.5		0 to +11	+12.5		0 to +11	+12.5		V
5V Supply	0 to +2			0 to +2			0 to +2			V
UTPUT (Figure 12,										
ror, V_{IN} 7mV to 7V rms, 0dB = 1V rms		±0.4	±0.6		±0.2	±0.3		±0.5	±0.6	dB
ale Factor		−3			−3			−3		mV/dB
ale Factor TC (Uncompensated, see Fig- re 12 for Temperature Compensation)		−0.033 +0.33			−0.033 +0.33			−0.033 +0.33		dB/°C % of Reading/°C
ge for 0dB = 1V rms	5	20	80	5	20	80	5	20	80	μA
ge Range	1		100	1		100	1		100	μA
TERMINAL										
Scale Factor		40			40			40		μA/V rms
Scale Factor Tolerance		±10	±20		±10	±20		±10	±20	%
put Resistance	20	25	30	20	25	30	20	25	30	kΩ
tage Compliance		$-V_S$ to ($+V_S$ −2.5V)			$-V_S$ to ($+V_S$ −2.5V)			$-V_S$ to ($+V_S$ −2.5V)		V
ER AMPLIFIER										
ut and Output Voltage Range		$-V_S$ to ($+V_S$ −2.5V)			$-V_S$ to ($+V_S$ −2.5V)			$-V_S$ to ($+V_S$ −2.5V)		V
Offset Voltage, R_S = 25k		±0.5	±4		±0.5	±4		±0.5	±4	mV
Bias Current		20	60		20	60		20	60	nA
Resistance		10^9			10^9			10^9		Ω
put Current		(+5mA, −130μA)			(+5mA, −130μA)			(+5mA, −130μA)		
Circuit Current		20			20			20		mA
put Resistance			0.5			0.5			0.5	Ω
Signal Bandwidth		1			1			1		MHz
Rate[4]		5			5			5		V/μs
ER SUPPLY										
ge Rated Performance		±15			±15			±15		V
Supply	±3.0		±18	±3.0		±18	±3.0		±18	V
ge Supply	+5		+36	+5		+36	+5		+36	V
escent Current										
V_S = 5V to 36V, T_{min} to T_{max}		1.2	2		1.2	2		1.2	2	mA
PERATURE RANGE										
ed Performance	0		+70	0		+70	−55		+125	°C
age	−55		+150	−55		+150	−55		+150	°C

[1] Error is specified for 0 to 7V rms, dc or 1kHz sinewave input with the AD536A connected as in the figure referenced.
[2] Additional crest factor is specified as an additional error for 1V rms rectangular pulse input, pulse width 200μs.
[3] Voltages are expressed in volts rms, and error is percent of reading.
[4] External pulldown resistor.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

STANDARD CONNECTION

The AD536A is simple to connect for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 1. In this configuration, the AD536A will measure the rms of the ac and dc level present at the input, but will show an error for low frequency inputs as a function of the filter capacitor, C_{AV}, as shown in Figure 5. Thus, if a 4μF capacitor is used, the additional average error at 10Hz will be 0.1%, at 3Hz it will be 1%. The accuracy at higher frequencies will be according to specification. If it is desired to reject the dc input, a capacitor is added in series with with the input, as shown in Figure 3; the capacitor must be non-polar. If the AD536A is driven with power supplies with a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground with 0.1μF ceramic discs as near the device as possible.

The input and output signal ranges are a function of the supply voltages; these ranges are shown in Figure 16. The AD536A can also be used in an unbuffered voltage output mode by disconnecting the input to the buffer. The output then appears unbuffered across the 25k resistor. The buffer amplifier can then be used for other purposes. Further the AD536A can be used in a current output mode by disconnecting the 25k resistor from ground. The output current is available at pin 8 (pin 10 on the "H" package) with a nominal scale of 40μA per volt rms input, positive out.

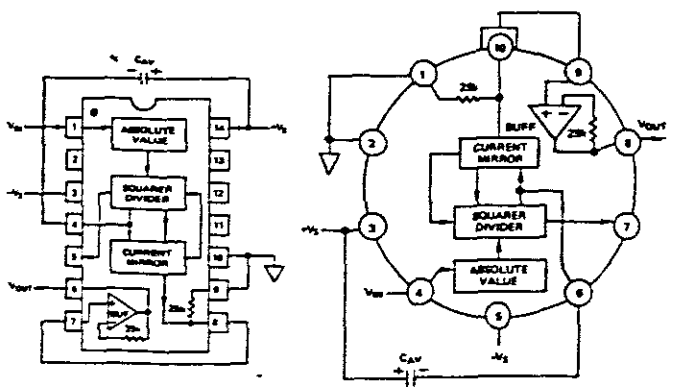


Figure 1. Standard rms Connection

OPTIONAL EXTERNAL TRIMS FOR HIGH ACCURACY

If it is desired to improve the accuracy of the AD536A, the external trims shown in Figure 2 can be added. R_4 is used to trim the offset. Note that the offset trim circuit adds 365Ω in series with the internal 25kΩ resistor. This will cause a 1.5% increase in scale factor, which is trimmed out by using R_1 as shown. Range of scale factor adjustment is ±1.5%.

The trimming procedure is as follows:

1. Ground the input signal, V_{IN}, and adjust R_4 to give zero volts output from pin 6. Alternatively, R_4 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input level to V_{IN}, either dc or a calibrated ac signal (1kHz is the optimum frequency); then trim R_1 to give the correct output from pin 6, i.e., 1.000V dc input should give 1.000V dc output. Of course, a ±1.000V peak-to-peak sinewave should give a 0.707V dc output. The remaining errors, as given in the specifications, are due to the nonlinearity.

The major advantage of external trimming is to optimize device performance for a reduced signal range; the AD536A is internally trimmed for a 7V rms full scale range.

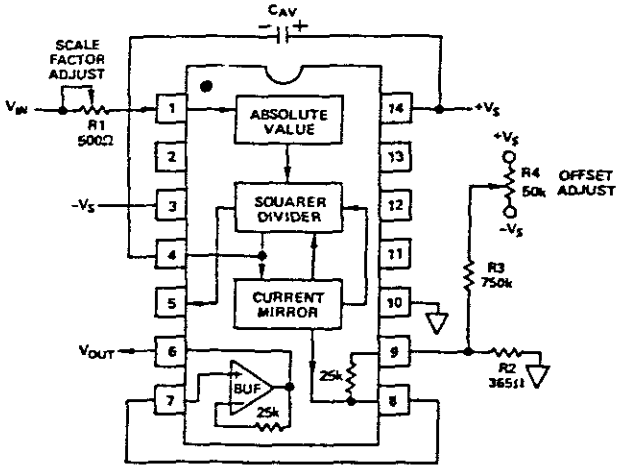


Figure 2. Optional External Gain and Output Offset Trims

SINGLE SUPPLY CONNECTION

The applications in Figures 1 and 2 require the use of approximately symmetrical dual supplies. The AD536A can also be used with only a single positive supply down to +5 volts, as shown in Figure 3. The major limitation of this connection is that only ac signals can be measured since the differential input stage must be biased off ground for proper operation. This biasing is done at pin 10; thus it is critical that no extraneous signals be coupled into this point. Biasing can be accomplished by using a resistive divider between $+V_S$ and ground. The values of the resistors can be increased in the interest of lowered power consumption, since only 5 microamps of current flows into pin 10 (pin 2 on the "H" package). AC input coupling requires only capacitor C_2 as shown; a dc return is not necessary as it is provided internally. C_2 is selected for the proper low frequency break point with the input resistance of 16.7kΩ; for a cut-off at 10Hz, C_2 should be 1μF. The signal ranges in this connection are slightly more restricted than in the dual supply connection. The input and output signal ranges are shown in Figure 16. The load resistor, R_L, is necessary to provide output sink current.

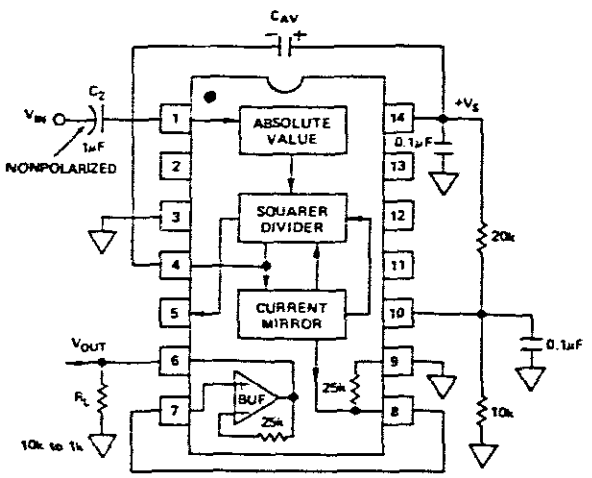


Figure 3. Single Supply Connection

CHOOSING THE AVERAGING TIME CONSTANT

The AD536A will compute the rms of both ac and dc signals. If the input is a slowly-varying dc, the output of the AD536A will track the input exactly. At higher frequencies, the average output of the AD536A will approach the rms value of the input signal. The actual output of the AD536A will differ from the ideal output by a dc (or average) error and some amount of ripple, as demonstrated in Figure 4.

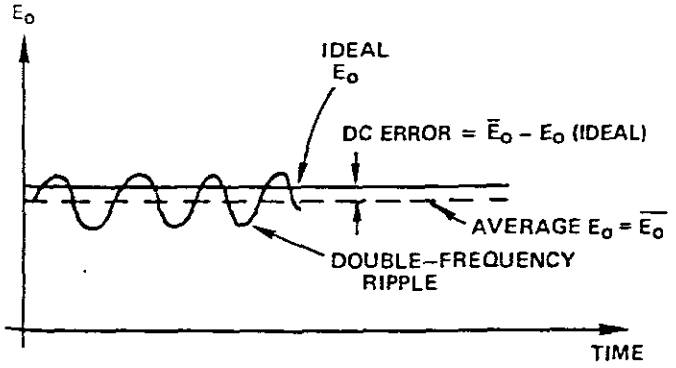


Figure 4. Typical Output Waveform for Sinusoidal Input

The dc error is dependent on the input signal frequency and the value of C_{AV}. Figure 5 can be used to determine the minimum value of C_{AV} which will yield a given percent dc error above a given frequency using the standard rms connection.

The ac component of the output signal is the ripple. There are two ways to reduce the ripple. The first method involves using a large value of C_{AV}. Since the ripple is inversely proportional to C_{AV}, a tenfold increase in this capacitance will effect a tenfold reduction in ripple. When measuring waveforms with high crest factors, (such as low duty cycle pulse trains), the averaging time constant should be at least ten times the signal period. For example, a 100Hz pulse rate requires a 100ms time constant, which corresponds to a 4μF capacitor (time constant = 25ms per μF).

The primary disadvantage in using a large C_{AV} to remove ripple is that the settling time for a step change in input level is increased proportionately. Figure 5 shows that the relationship between C_{AV} and 1% settling time is 115 milliseconds for each microfarad of C_{AV}. The settling time is twice as great for decreasing signals as for increasing signals (the values in Figure 5 are for decreasing signals). Settling time also increases for low signal levels, as shown in Figure 6.

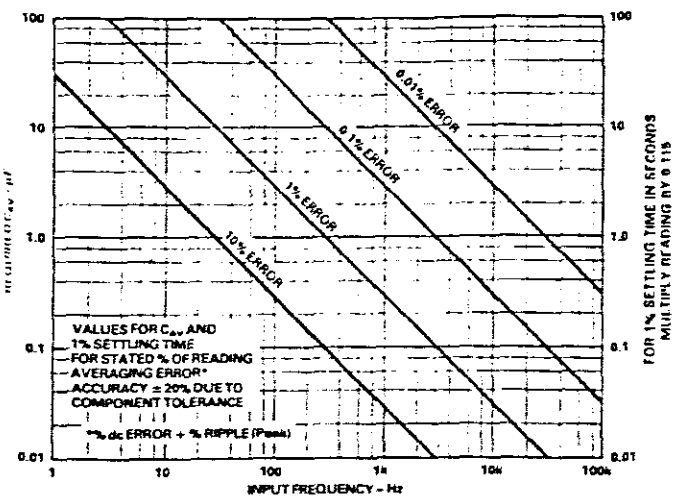


Figure 5. Error/Settling Time Graph for Use with the Standard rms Connection in Figure 1

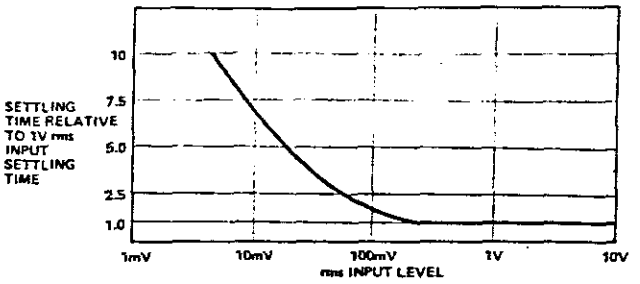


Figure 6. Settling Time vs Input Level

A better method for reducing output ripple is the use of a "post-filter". Figure 7 shows a suggested circuit. If a single-pole filter is used (C_3 removed, R_X shorted), and C_2 is approximately twice the value of C_{AV}, the ripple is reduced as shown in Figure 8, and settling time is increased. For example, with $C_{AV} = 1\mu F$ and $C_2 = 2.2\mu F$, the ripple for a 60Hz input is reduced from 10% of reading to approximately 0.3% of reading. The settling time, however, is increased by approximately a factor of 3. The values of C_{AV} and C_2 can therefore be reduced to permit faster settling times while still providing substantial ripple reduction.

The two-pole post-filter uses an active filter stage to provide even greater ripple reduction without substantially increasing the settling times over a circuit with a one-pole filter. The values of C_{AV}, C_2, and C_3 can then be reduced to allow extremely fast settling times for a constant amount of ripple. Caution should be exercised in choosing the value of C_{AV}, since the dc error is dependent upon this value and is independent of the post filter.

For a more detailed explanation of these topics refer to the *RMS to DC Conversion Application Guide 2nd Edition*, available from Analog Devices.

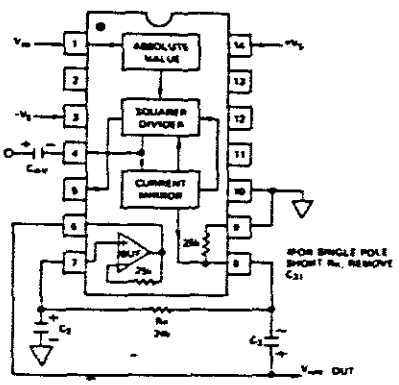


Figure 7. 2 Pole "Post" Filter

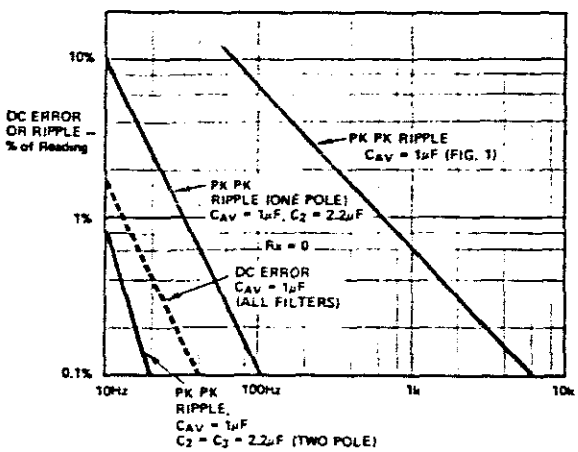


Figure 8. Performance Features of Various Filter Types

AD536A PRINCIPLE OF OPERATION

The AD536A embodies an implicit solution of the rms equation that overcomes the dynamic range as well as other limitations inherent in a straight-forward computation of rms. The actual computation performed by the AD536A follows the equation:

$$V_{rms} = \text{Avg.} \left[\frac{V_{IN}^2}{V_{rms}} \right]$$

Figure 9 is a simplified schematic of the AD536A; it is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage, V_{IN}, which can be ac or dc, is converted to a unipolar current I_1, by the active rectifier A_1, A_2. I_1 drives one input of the squarer/divider, which has the transfer function:

$$I_4 = I_1^2 / I_3$$

The output current, I_4, of the squarer/divider drives the current mirror through a low pass filter formed by R_1 and the externally connected capacitor, C_{AV}. If the R_1, C_{AV} time constant is much greater than the longest period of the input signal, then I_4 is effectively averaged. The current mirror returns a current I_3, which equals Avg. $[I_4]$, back to the squarer/divider to complete the implicit rms computation. Thus:

$$I_4 = \text{Avg.}\ [I_1^2/I_4] = I_1\ \text{rms}$$

The current mirror also produces the output current, I_{OUT}, which equals $2I_4$. I_{OUT} can be used directly or converted to a voltage with R_2 and buffered by A_4 to provide a low impedance voltage output. The transfer function of the AD536A thus results:

$$V_{OUT} = 2R_2\ I_{rms} = V_{IN\ rms}$$

The dB output is derived from the emitter of Q_3, since the voltage at this point is proportional to –log V_{IN}. Emitter follower, Q_5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current (I_{REF}) to Q_5 approximates I_3.

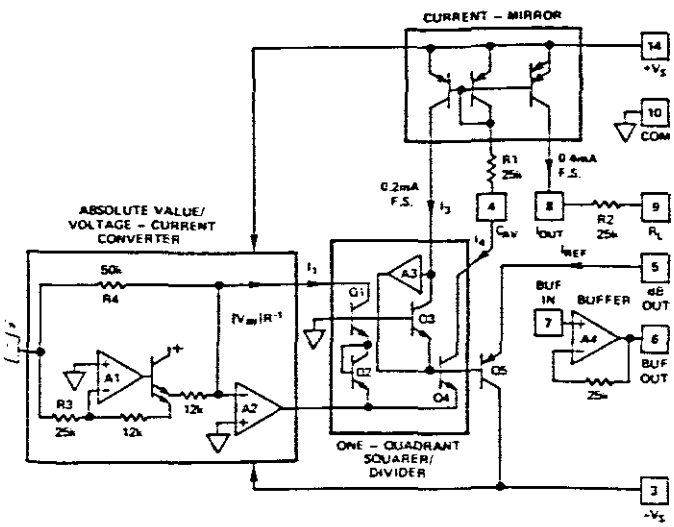
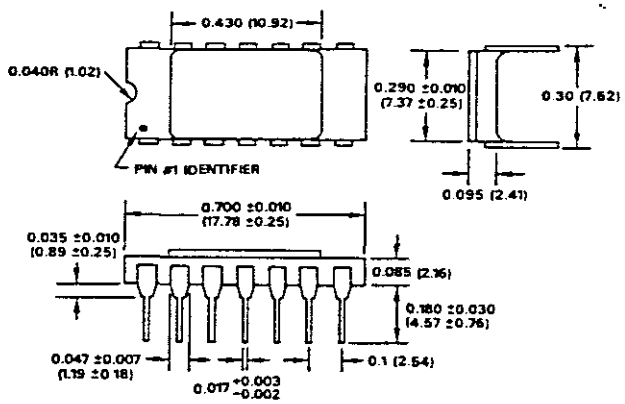


Figure 9. Simplified Schematic

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

"D" PACKAGE (TO-116)



"H" PACKAGE (TO-100)

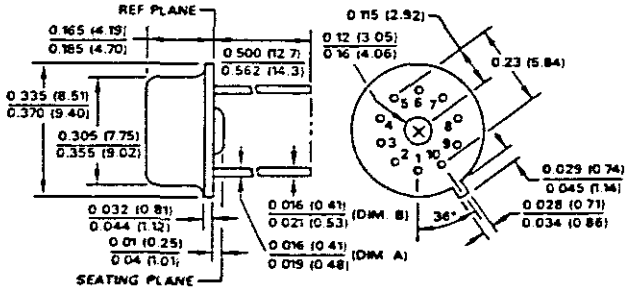


Figure 10. Physical Dimensions
Dimensions shown in inches and (mm).

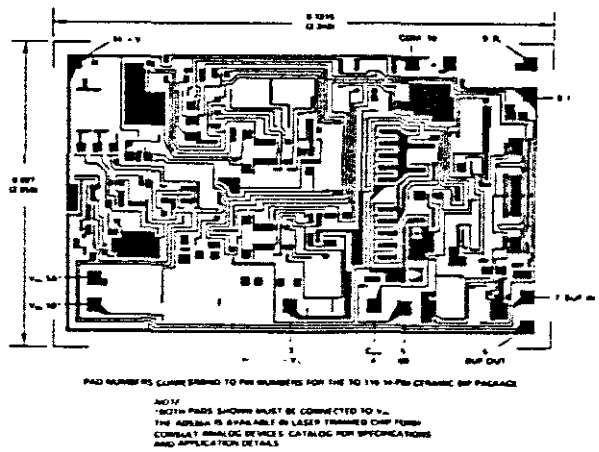


Figure 11. Chip Dimensions and Pad Layout.
Dimensions shown in inches and (mm).

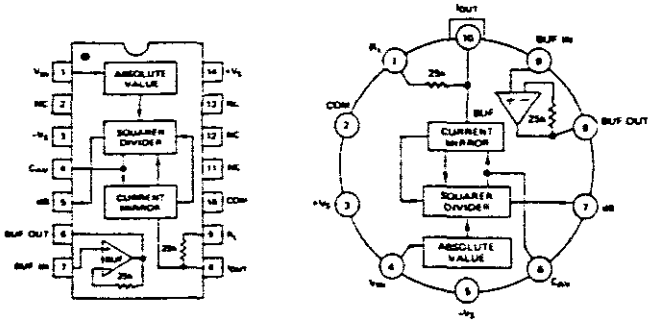


Figure 12. AD536A Pin Connections and Functional Diagram

National Semiconductor

LM311 Voltage Comparator

General Description

The LM311 is a voltage comparator that has input currents more than a hundred times lower than devices like the LM306 or LM710C. It is also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Its output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 40V at currents as high as 50 mA.

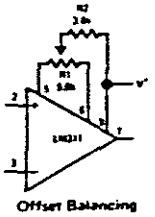
Features

- Operates from single 5V supply
- Maximum input current: 250 nA
- Maximum offset current: 50 nA
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

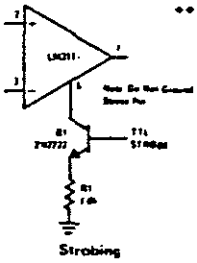
Both the input and the output of the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM306 and LM710C (200 ns response time vs 40 ns) the device is also much less prone to spurious oscillations. The LM311 has the same pin configuration as the LM306 and LM710C. See the "application hints" of the LM311 for application help.

Auxiliary Circuits**

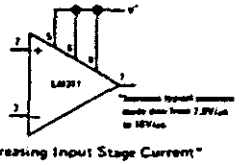
**Note: Pin connections shown on schematic diagram and typical applications are for TO-5 package.



Offset Balancing

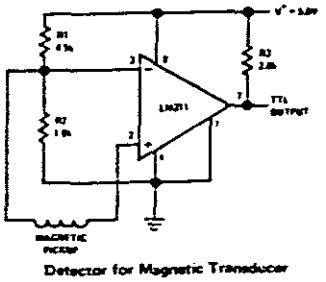


Strobing

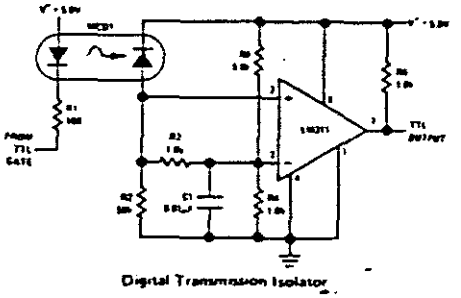


Increasing Input Stage Current*

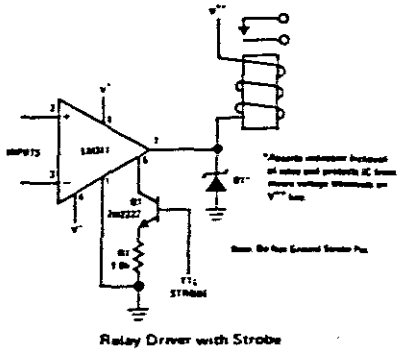
Typical Applications**



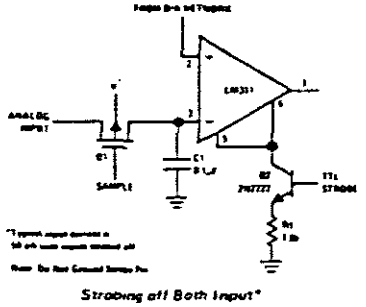
Detector for Magnetic Transducer



Digital Transmission Isolator



Relay Driver with Strobe



Strobing off Both Input* and Output Stages

Absolute Maximum Ratings

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	40V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 sec)	300°C
Voltage at Strobe Pin	V^+−5V

Electrical Characteristics *(Note 3)*

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		6.0	50	nA
Input Bias Current	$T_A = 25°C$		100	250	nA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe ON Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$ $T_A = 25°C$, $I_{STROBE} = 3$ mA		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k$			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range		−14.5	13.8,−14.7	13.0	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for V_S = ±15V and the Ground pin at ground, and 0°C < T_A < +70°C, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

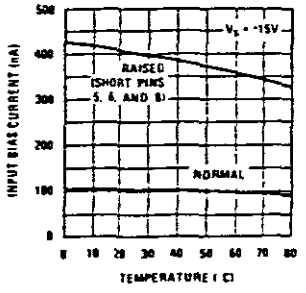
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

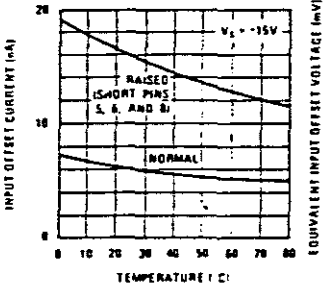
Note 6: Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Typical Performance Characteristics

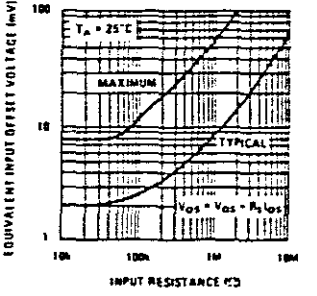
Input Bias Current



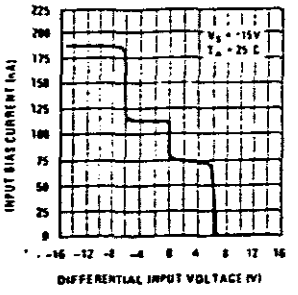
Input Offset Current



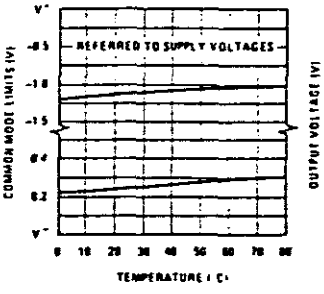
Offset Error



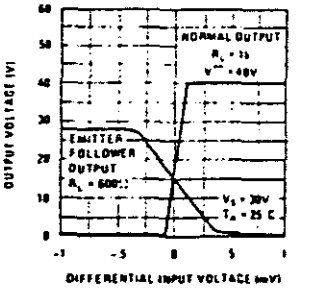
Input Characteristics



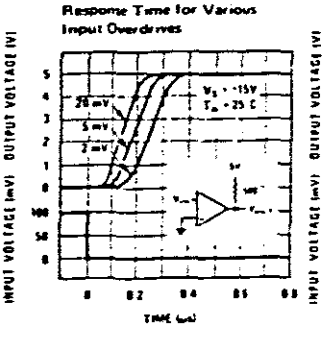
Common Mode Limits



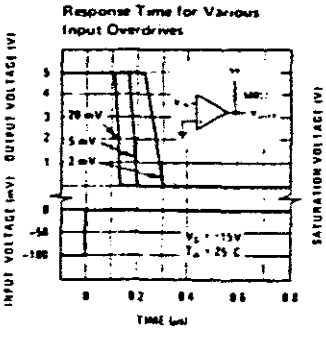
Transfer Function



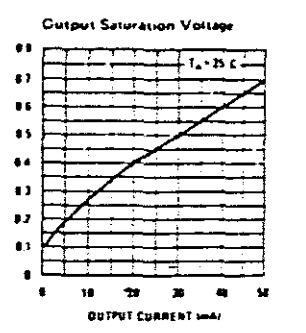
Response Time for Various Input Overdrives



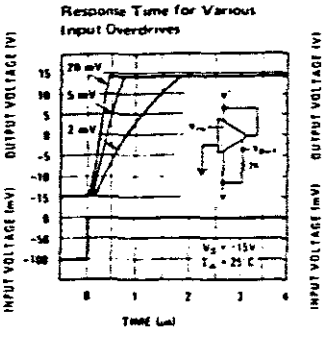
Response Time for Various Input Overdrives



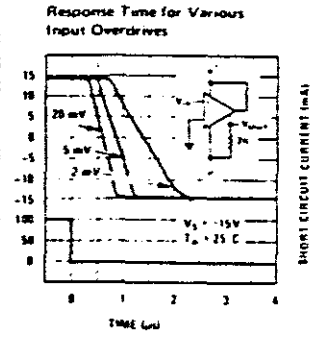
Output Saturation Voltage



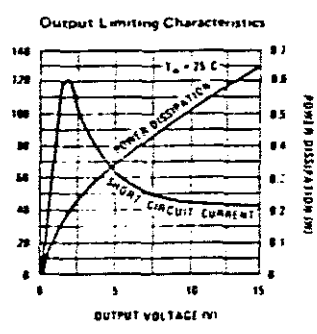
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives

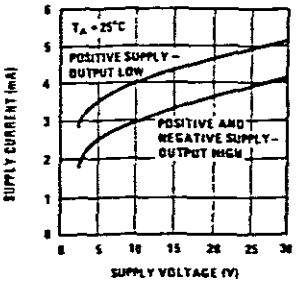


Output Limiting Characteristics

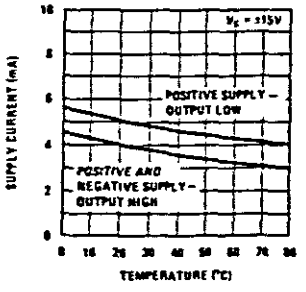


Typical Performance Characteristics (Continued)

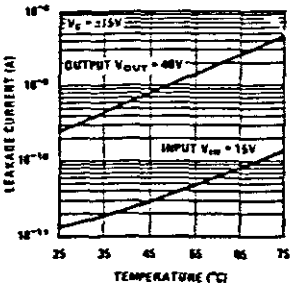
Supply Current



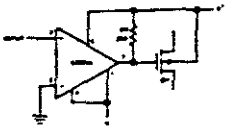
Supply Current



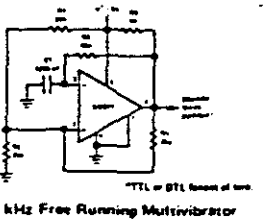
Leakage Currents



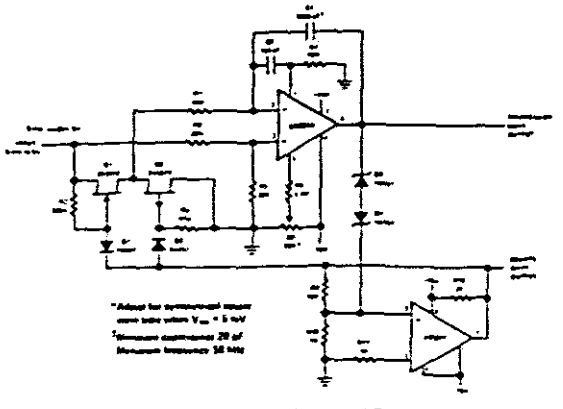
Typical Applications



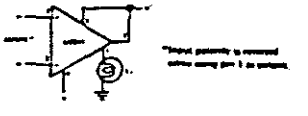
Zero Crossing Detector Driving MOS Switch



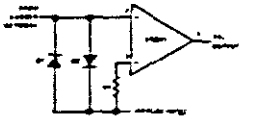
100 kHz Free Running Multivibrator



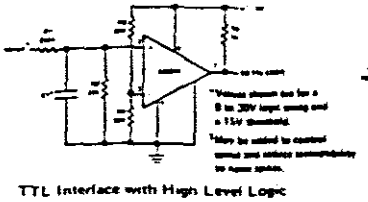
10 Hz to 10 kHz Voltage Controlled Oscillator



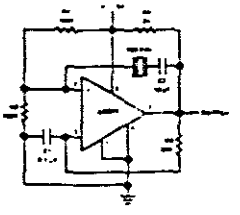
Driving Ground-Referred Load



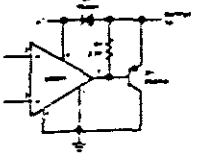
Using Clamp Diodes to Improve Response



TTL Interface with High Level Logic

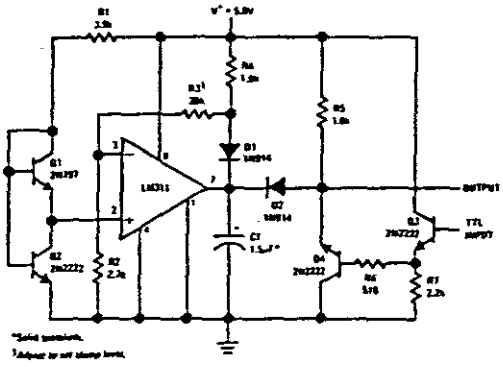


Crystal Oscillator

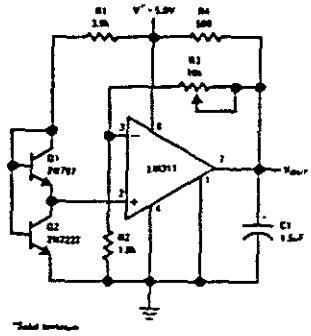


Comparator and Solenoid Driver

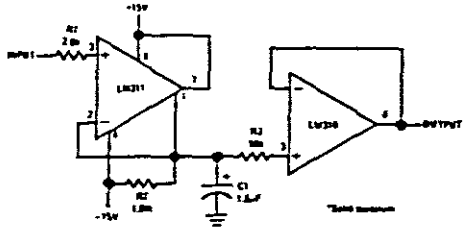
Typical Applications (Continued)



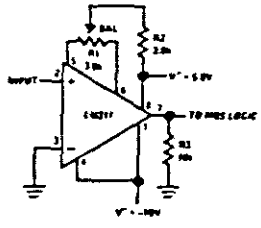
Precision Squarer



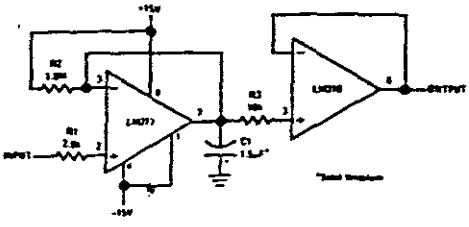
Low Voltage Adjustable Reference Supply



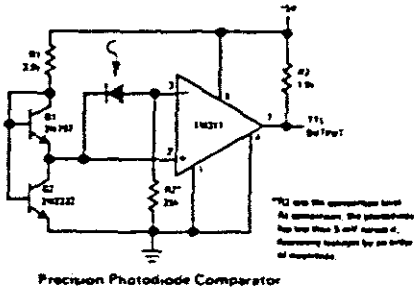
Positive Peak Detector



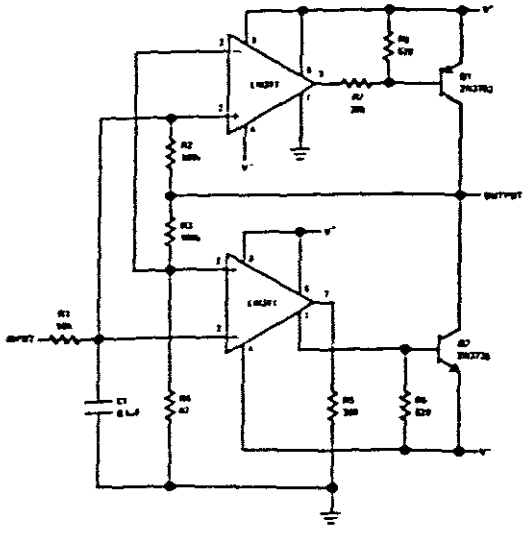
Zero Crossing Detector driving MOS logic



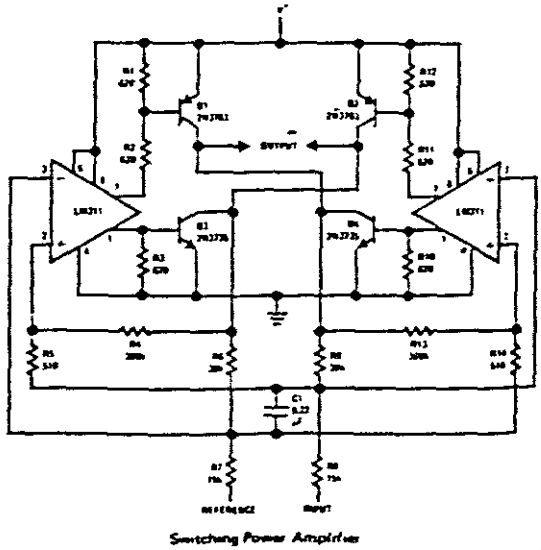
Negative Peak Detector



Precision Photodiode Comparator

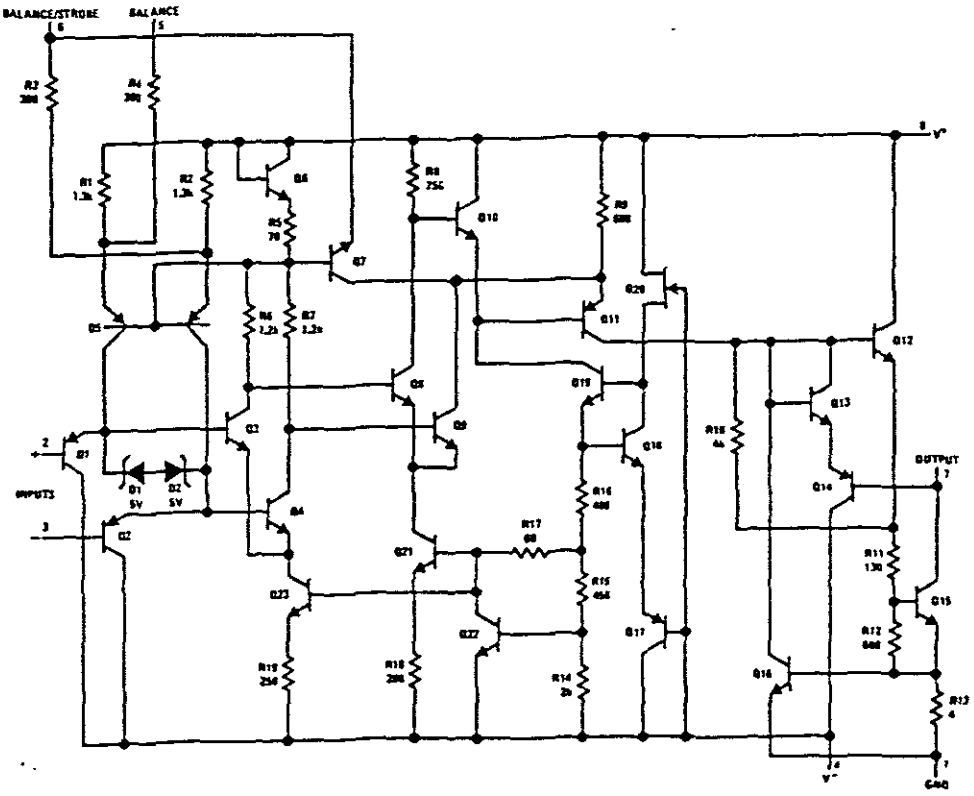


Switching Power Amplifier



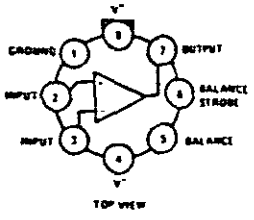
Switching Power Amplifier

Schematic Diagram



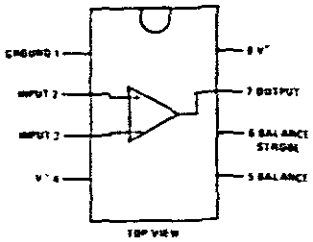
Connection Diagrams

Metal Can Package



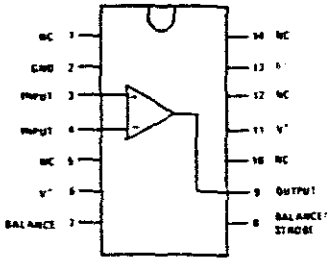
Order Number LM311H
See NS Package H08C

Dual-In-Line Package



Order Number LM311N
See NS Package N08B
Order Number LM311J-8
See NS Package J08A

Dual-In-Line Package



Order Number LM311N-14
See NS Package N14A
Order Number LM311J
See NS Package J14A

*Pin connections shown on schematic diagram and typical applications are for TO-5 package.

Application Hints

CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high-speed comparator such as the LM111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 μF disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in *Figure 1* below.

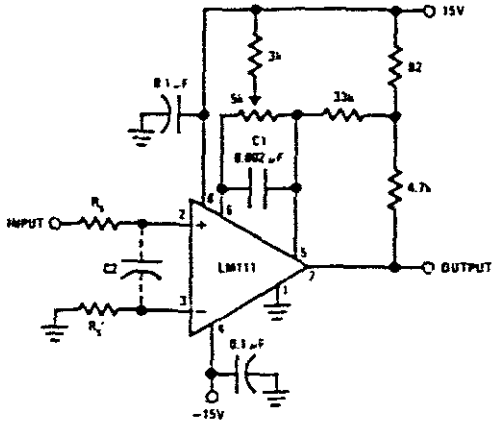
1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 μA capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in *Figure 1*.

2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.

3. When the signal source is applied through a resistive network, R_S, it is usually advantageous to choose an R_S' of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wirewound resistors are not suitable.

4. When comparator circuits use input resistors (eg. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if $R_S = 10\ k\Omega$, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.

5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the LM111, and the 0.01 μF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)



Pin connections shown are for LM111H in 8-lead TO-5 hermetic package

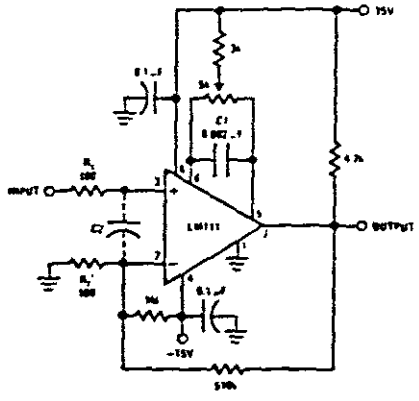
FIGURE 1. Improved Positive Feedback

Application Hints (Continued)

6. It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of *Figure 2*, the feedback from the output to the positive input will cause about 3 mV of hysteresis. However, if R_S is larger than 100Ω, such as 50 kΩ, it would not be reasonable to simply increase the value of the positive feedback resistor above 510 kΩ. The circuit of *Figure 3* could be used, but it is rather awkward. See the notes in paragraph 7 below.

7. When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of *Figure 1* is ideal. The positive feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the V_{OS} of the comparator. As much as 8 mV of V_{OS} can be trimmed out, using the 5 kΩ pot and 3 kΩ resistor as shown.

8. These application notes apply specifically to the LM111, LM211, LM311, and LF111 families of comparators, and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).



Pin connections shown are for LM111H in 8-lead TO-5 hermetic package

FIGURE 2. Conventional Positive Feedback

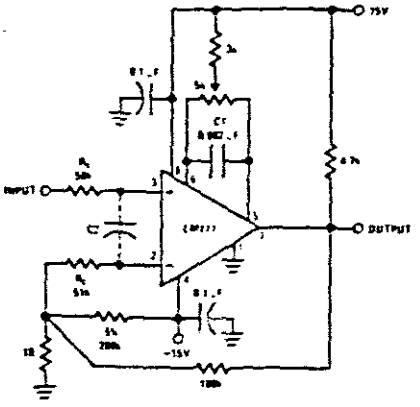


FIGURE 3. Positive Feedback With High Source Resistance

National Semiconductor

LM3999 Precision Reference

General Description

The LM3999 is a precision, temperature-stabilized monolithic zener offering temperature coefficients a factor of ten better than high quality reference zeners. Constructed on a single monolithic chip is a temperature stabilizer circuit and an active reference zener. The active circuitry reduces the dynamic impedance of the zener to about 0.5Ω and allows the zener to operate over 0.5 mA to 10 mA current range with essentially no change in voltage or temperature coefficient. Further, a new subsurface zener structure gives low noise and excellent long term stability compared to ordinary monolithic zeners.

The LM3999 reference is exceptionally easy to use and free of the problems that are often experienced with ordinary zeners. There is virtually no hysteresis in reference voltage with temperature cycling. Also, the LM3999 is free of voltage shifts due to stress on the leads. Finally, since the unit is temperature stabilized, warm up time is fast.

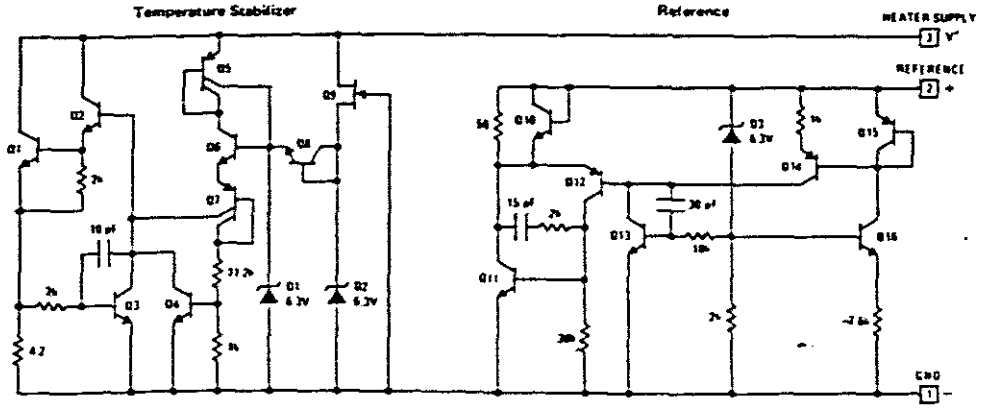
The LM3999 can be used in almost any application in place of ordinary zeners with improved performance. Some ideal applications are analog to digital converters, precision voltage or current sources or precision power supplies. Further, in many cases, the LM3999 can replace references in existing equipment with a minimum of wiring changes.

The LM3999 is packaged in a standard TO-92 package and is rated from 0°C to +70°C.

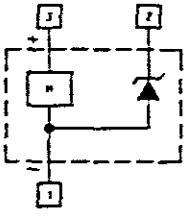
Features

- Guaranteed 0.0005%/°C temperature coefficient
- Low dynamic impedance – 0.5Ω
- Initial tolerance on breakdown voltage – 5%
- Sharp breakdown at 400μA
- Wide operating current – 500μA to 10 mA
- Wide supply range for temperature stabilizer
- Low power for stabilization – 400 mW at 25°C
- Long term stability – 20 ppm

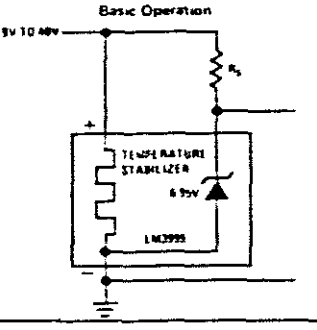
Schematic Diagram



Functional Block Diagram

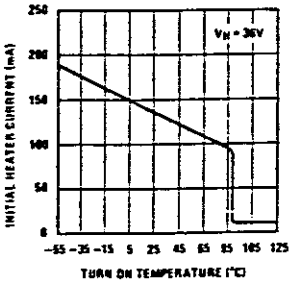


Typical Applications

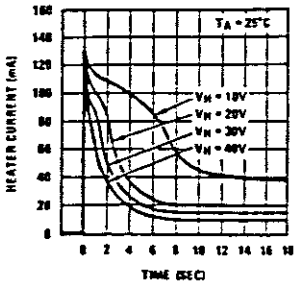


Typical Performance Characteristics (Continued)

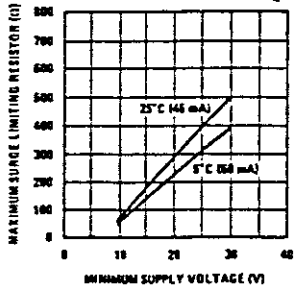
Initial Heater Current



Heater Current (To Limit This Surge, See Next Graph)

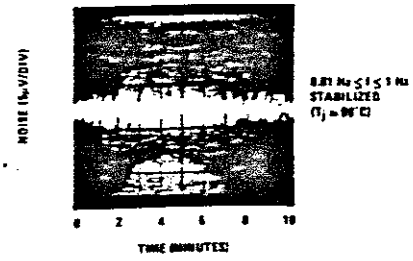


Heater Surge Limit Resistor vs Minimum Supply Voltage at Various Minimum Temperatures

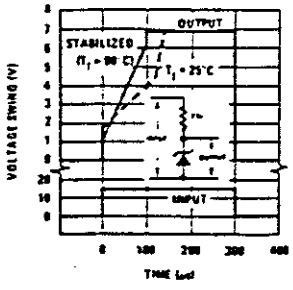


*Heater must be bypassed with a 2 μF tantalum capacitor if resistors are used.

Low Frequency Noise Voltage

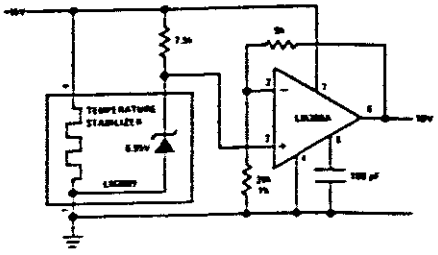


Response Time

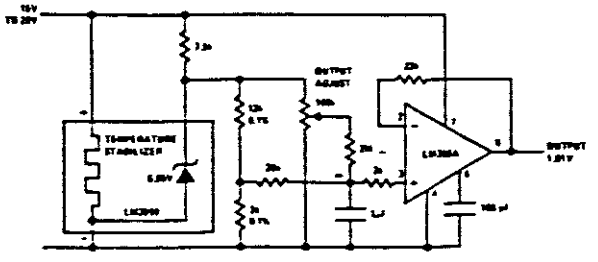


Typical Applications (Continued)

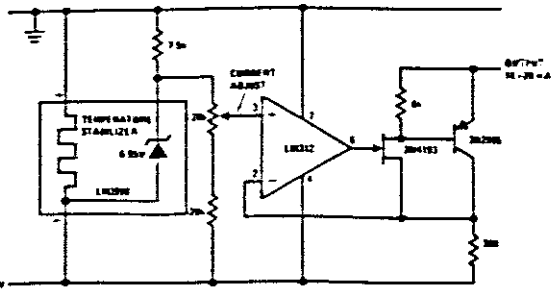
Buffered Reference With Single Supply



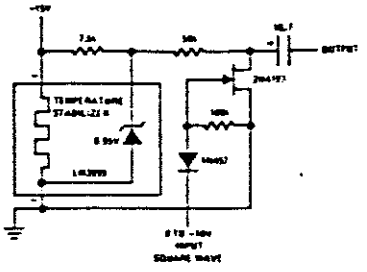
Voltage Reference



Negative Current Source



Square Wave Voltage Reference



Absolute Maximum Ratings

Temperature Stabilizer Voltage	36V
Reverse Breakdown Current	20 mA
Forward Current	0.1 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	*300°C*

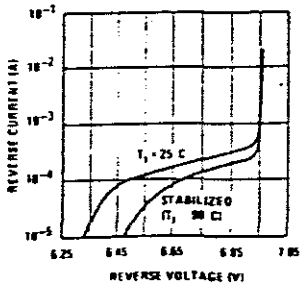
Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage	0.6 mA ≤ I_R ≤ 10 mA	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change With Current	0.6 mA ≤ I ≤ 10 mA		6	20	mV
Reverse Dynamic Impedance	I_R = 1 mA		0.6	2.2	Ω
Reverse Breakdown Temperature Coefficient	0°C ≤ T_A ≤ 70°C		0.0002	0.0005	%/°C
RMS Noise	10 Hz ≤ f ≤ 10 kHz		7		μV
Long Term Stability	Stabilized, 22°C ≤ T_A ≤ 28°C, 1000 Hours, I_R = 1 mA ±0.1%		20		ppm
Temperature Stabilizer	T_A = 25°C, Still Air, V_S = 30V		12	18	mA
Temperature Stabilizer Supply Voltage				36	V
Warm-Up Time to 0.05%	V_S = 30V, T_A = 25°C		5		Seconds
Initial Turn-on Current	9 ≤ V_S ≤ 40, T_A = 25°C		140	200	mA

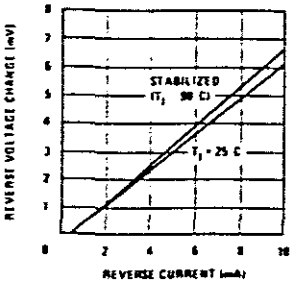
Note 1: These specifications apply for 30V applied to the temperature stabilizer and 0°C ≤ T_A ≤ +70°C.

Typical Performance Characteristics

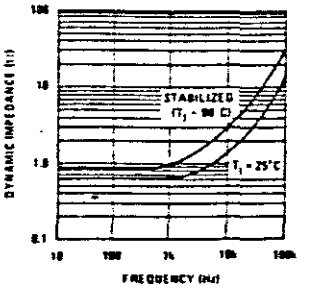
Reverse Characteristics



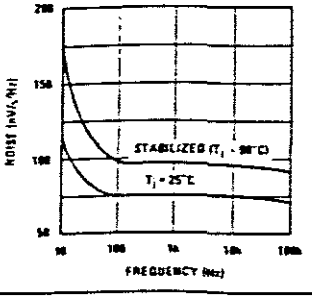
Reverse Voltage Change



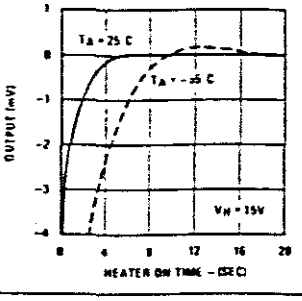
Dynamic Impedance



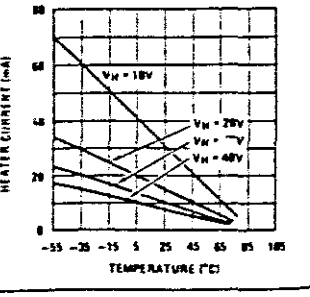
Zener Noise Voltage



Stabilization Time

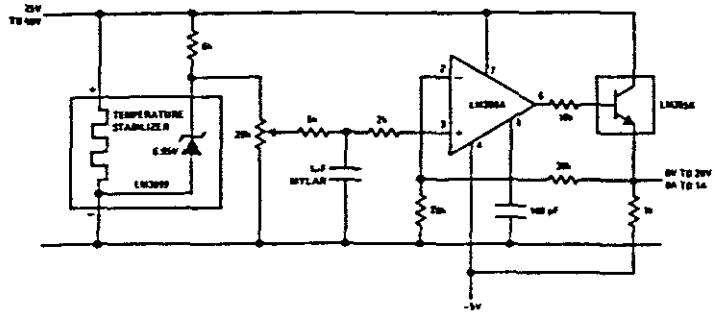


Heater Current

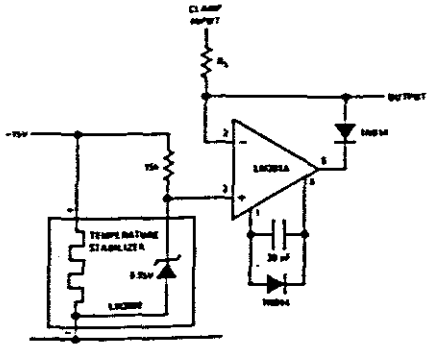


Typical Applications (Continued)

0V to 20V Power Reference

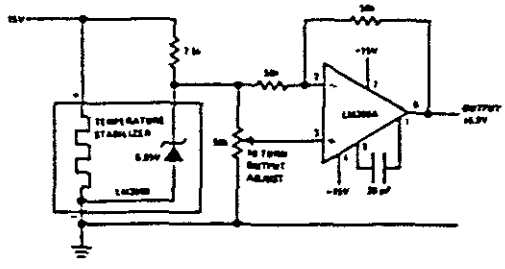


Precision Clamp*

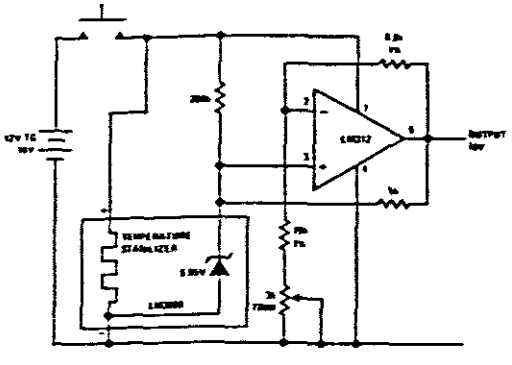


*Clamp will sink 5 mA when input goes more positive than reference.

Bipolar Output Reference



Portable Calibrator*



*Warm-up time 10 seconds; intermittent operation does not degrade long term stability.

Connection Diagram

Plastic Package

BOTTOM VIEW

Order Number LM399Z
See NS Package Z03A

LM79XX Series 3-Terminal Negative Regulators

General Description

The LM79XX series of 3-terminal regulators is available with fixed output voltages of −5V, −12V, and −15V. These devices need only one external component—a compensation capacitor at the output. The LM79XX series is packaged in the TO-220 power package and is capable of supplying 1.5A of output current.

These regulators employ internal current limiting safe area protection and thermal shutdown for protection against virtually all overload conditions.

Low ground pin current of the LM79XX series allows output voltage to be easily boosted above the preset value with a resistor divider. The low quiescent current drain of these devices with a specified maximum change with line and load ensures good regulation in the voltage boosted mode.

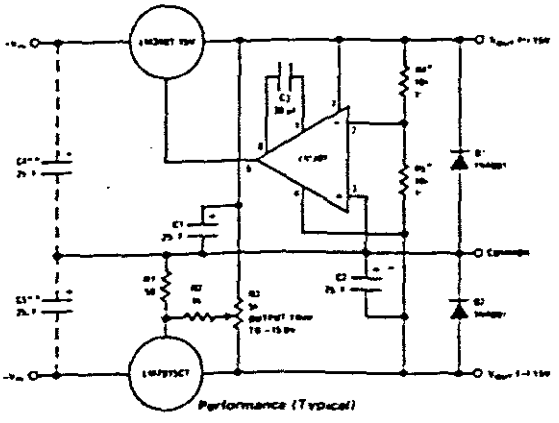
For applications requiring other voltages, see LM137 data sheet.

Features

- Thermal, short circuit and safe area protection
- High ripple rejection
- 1.5A output current
- 4% preset output voltage

Typical Applications

±15V, 1 Amp Tracking Regulators



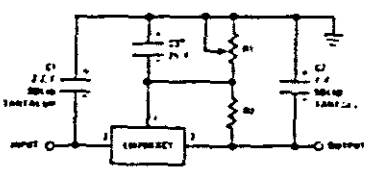
Performance (Typical)

	(−15)	(+15)
Load Regulation at ΔI_L = 1A	40 mV	2 mV
Output Ripple, C_{IN} = 3000μF, I_L = 1A	100μVrms	100μVrms
Temperature Stability	50 mV	50 mV
Output Noise 10 Hz ≤ f ≤ 10 kHz	150μVrms	150μVrms

*Resistor tolerance of R4 and R5 determine matching of (+) and (−) outputs

**Necessary only if raw supply filter capacitors are more than 3" from regulators

Variable Output



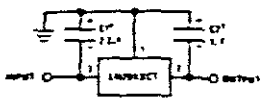
*Improves transient response and ripple rejection. Do not increase beyond 50μF

$$V_{OUT} = V_{SET}\left(\frac{R1 + R2}{R2}\right)$$

Select R2 as follows:

LM7905CT	300Ω
LM7912CT	750Ω
LM7915CT	1k

Fixed Regulator

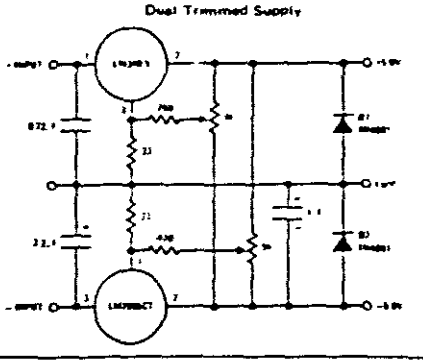


*Required if regulator is separated from filter capacitor by more than 3". For value given, capacitor must be solid tantalum. 25μF aluminum electrolytic may be substituted.

†Required for stability. For value given, capacitor must be solid tantalum. 25μF aluminum electrolytic may be substituted. Values given may be increased without limit.

For output capacitance in excess of 100μF, a high current diode from input to output (1N4001, etc.) will protect the regulator from momentary input shorts.

Dual Trimmed Supply



Absolute Maximum Ratings

Input Voltage	
(V_O = 5V)	−35V
(V_O = 12V and 15V)	−40V
Input-Output Differential	
(V_O = 5V)	25V
(V_O = 12V and 15V)	30V
Power Dissipation	Internally Limited
Operating Junction Temperature Range	0°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	230°C

Electrical Characteristics

Conditions unless otherwise noted: I_{OUT} = 500 mA, C_{IN} = 2.2μF, C_{OUT} = 1μF, 0°C ≤ T_J ≤ +125°C, Power Dissipation ≤ 15W.

PART NUMBER			LM7905C			UNITS
OUTPUT VOLTAGE			5V			
INPUT VOLTAGE (unless otherwise specified)			−10V			
PARAMETER		CONDITIONS	MIN	TYP	MAX	
V_O	Output Voltage	T_J = 25°C	-4.8	-5.0	-5.2	V
		5 mA ≤ I_{OUT} ≤ 1A,	-4.75		-5.25	V
		P ≤ 15W	(−20 ≤ V_{IN} ≤ −7)			V
ΔV_O	Line Regulation	T_J = 25°C, (Note 2)		8	50	mV
			(−25 ≤ V_{IN} ≤ −7)			V
				2	15	mV
			(−12 ≤ V_{IN} ≤ −8)			V
ΔV_O	Load Regulation	T_J = 25°C, (Note 2)				mV
		5 mA ≤ I_{OUT} ≤ 1.5A		15	100	mV
		250 mA ≤ I_{OUT} ≤ 750 mA		5	50	mV
I_Q	Quiescent Current	T_J = 25°C		1	2	mA
ΔI_Q	Quiescent Current	With Line			0.5	mA
	Change		(−25 ≤ V_{IN} ≤ −7)			V
		With Load, 5 mA ≤ I_{OUT} ≤ 1A			0.5	mA
V_n	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 Hz		125		μV
	Ripple Rejection	f = 120 Hz	54	66		dB
			(−18 ≤ V_{IN} ≤ −8)			V
	Dropout Voltage	T_J = 25°C, I_{OUT} = 1A		1.1		V
I_{OMAX}	Peak Output Current	T_J = 25°C		-2.2		A
	Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 100°C		0.4		mV/°C

Electrical Characteristics (Continued) Conditions unless otherwise noted: I_{OUT} = 500 mA, C_{IN} = 2.2µF, C_{OUT} = 1µF, 0°C ≤ T_J ≤ +125°C, Power Dissipation = 1.5W.

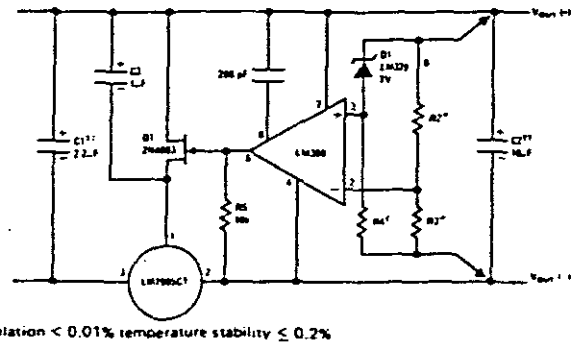
PART NUMBER			LM7912C			LM7915C			UNITS
OUTPUT VOLTAGE			12V			15V			
INPUT VOLTAGE (unless otherwise specified)			−19V			−23V			
	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	T_J = 25°C	-11.5	-12.0	-12.5	-14.4	-15.0	-15.6	V
		5 mA ≤ I_{OUT} ≤ 1A,	-11.4		12.6	-14.25		15.75	V
		P ≤ 15W	(-27 ≤ V_{IN} ≤ -14.5)			(30 ≤ V_{IN} ≤ 17.5)			V
ΔV_O	Line Regulation	T_J = 25°C, (Note 2)		5	80		5	100	mV
			(-30 ≤ V_{IN} ≤ -14.5)			(-30 ≤ V_{IN} ≤ 17.5)			V
				3	30		3	50	mV
			(-22 ≤ V_{IN} ≤ -16)			(-26 ≤ V_{IN} ≤ 20)			V
ΔV_O	Load Regulation	T_J = 25°C, (Note 2)		15	200		15	200	mV
		5 mA ≤ I_{OUT} ≤ 1.5A		15	200		15	200	mV
		250 mA ≤ I_{OUT} ≤ 750 mA		5	75		5	75	mV
I_Q	Quiescent Current	T_J = 25°C		1.5	3		1.5	3	mA
ΔI_Q	Quiescent Current Change	With Line			0.5			0.5	mA
			(-30 ≤ V_{IN} ≤ -14.5)			(-30 ≤ V_{IN} ≤ 17.5)			V
		With Load, 5 mA ≤ I_{OUT} ≤ 1A			0.5			0.5	mA
V_n	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 Hz		300			375		µV
	Ripple Rejection	f = 120 Hz	54	70		54	70		dB
			(-25 ≤ V_{IN} ≤ -15)			(-30 ≤ V_{IN} ≤ -17.5)			V
	Dropout Voltage	T_J = 25°C, I_{OUT} = 1A		1.1			1.1		V
I_{OMAX}	Peak Output Current	T_J = 25°C		2.2			2.2		A
	Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 100°C		-0.8			-1.0		mV/°C

Note 1: For calculations of junction temperature rise due to power dissipation, thermal resistance junction to ambient (θ_{JA}) is 50°C/W (no heat sink) and 5°C/W (infinite heat sink).

Note 2: Regulation is measured at a constant junction temperature by pulse testing with a low duty cycle. Changes in output voltage due to heating effects must be taken into account.

Typical Applications *(Continued)*

High Stability 1 Amp Regulator



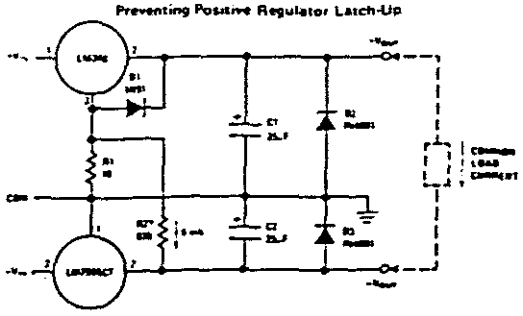
Load and line regulation < 0.01% temperature stability ≤ 0.2%

†Determines Zener current

††Solid tantalum

*Select resistors to set output voltage. 2 ppm/°C tracking suggested

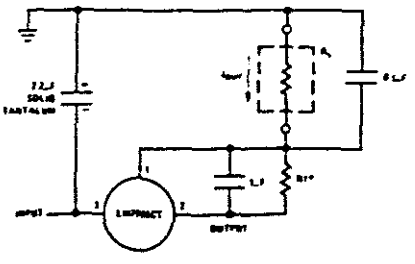
Preventing Positive Regulator Latch-Up



R1 and D1 allow the positive regulator to "start-up" when $+V_{IN}$ is delayed relative to $-V_{IN}$ and a heavy load is drawn between the outputs. Without R1 and D1, most three-terminal regulators will not start with heavy (0.1A–1A) load current flowing to the negative regulator, even though the positive output is clamped by D2.

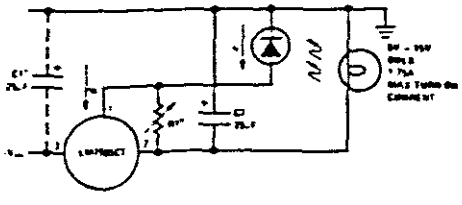
*R2 is optional. Ground pin current from the positive regulator flowing through R1 will increase $+V_{OUT}$ by 60 mV if R2 is omitted.

Current Source



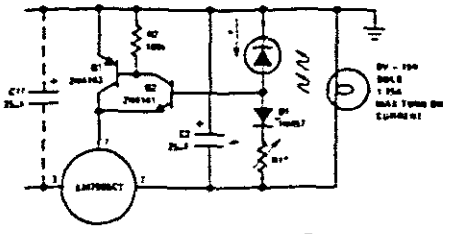
$$I_{OUT} = 1\ mA + \frac{5V}{R1}$$

Light Controllers Using Silicon Photo Cells



*Lamp brightness increases until $I_L = I_Q$ (≈ 1 mA) + 5V/R1.

†Necessary only if raw supply filter capacitor is more than 2" from LM7905CT



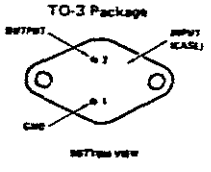
*Lamp brightness increases until I_L = 5V/R1 (I_L can be set as low as 1μA)

†Necessary only if raw supply filter capacitor is more than 2" from LM7905CT

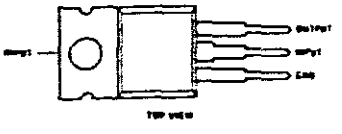
Connection Diagrams

TO-3 Package

Order Numbers:
LM7905CK
LM7912CK
LM7915CK
See NS Package KC02A



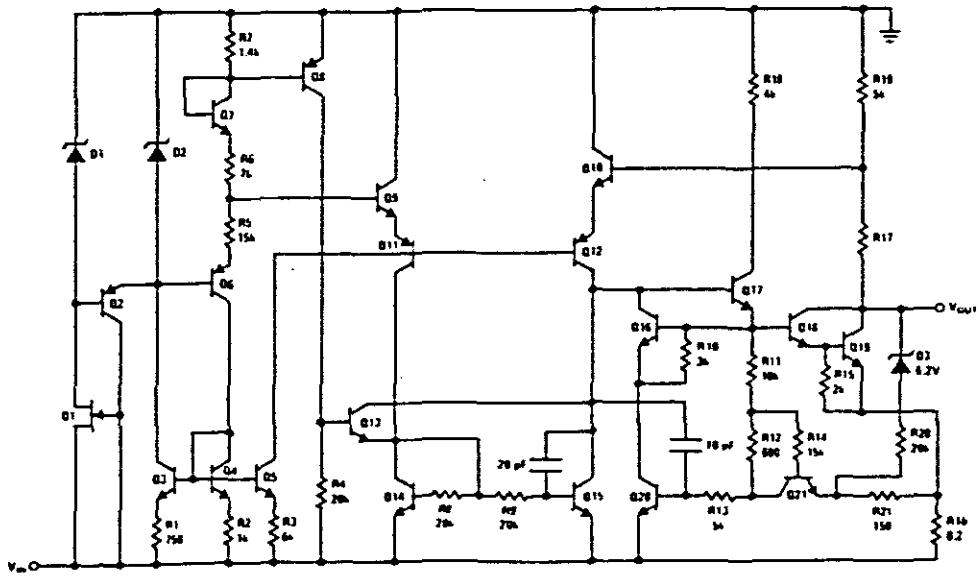
TO-220 Package



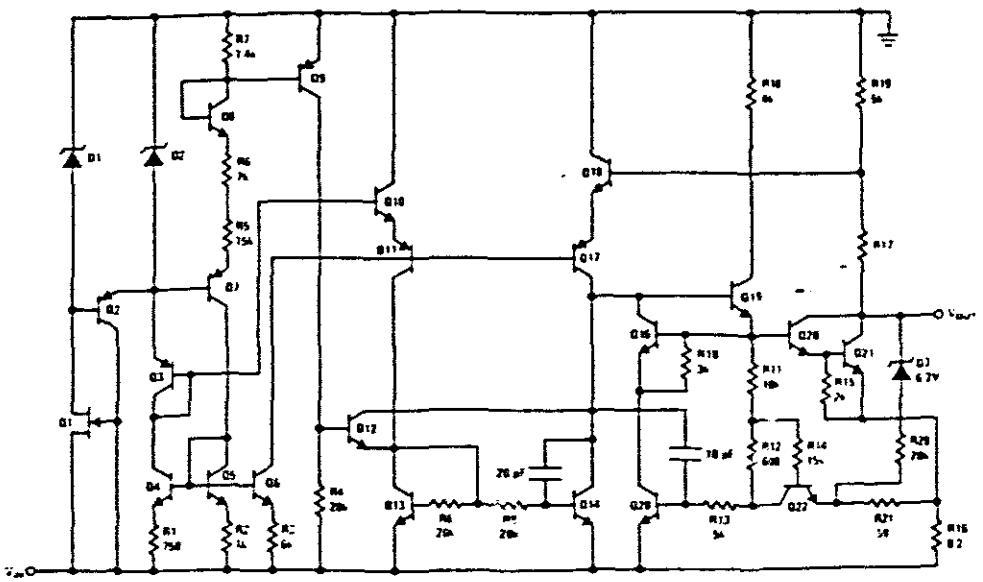
Order Numbers:
LM7905CT
LM7912CT
LM7915CT
See NS Package T03B

Schematic Diagrams

–5V



–12V and –15V



National Semiconductor

LM78XX Series Voltage Regulators

General Description

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expended to make the LM78XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

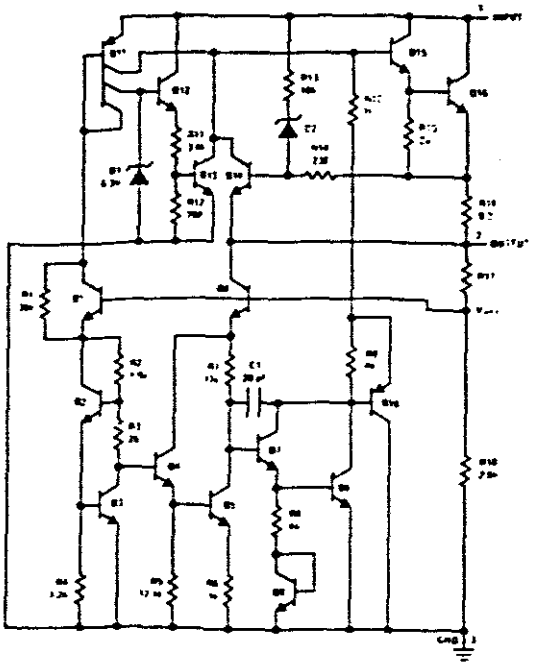
Features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

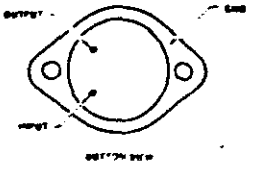
Voltage Range

LM7805C	5V
LM7812C	12V
LM7815C	15V

Schematic and Connection Diagrams

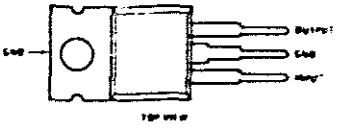


Metal Can Package
TO-3 (K)
Aluminum



Order Numbers
LM7805CK
LM7812CK
LM7815CK
See Package KC02A

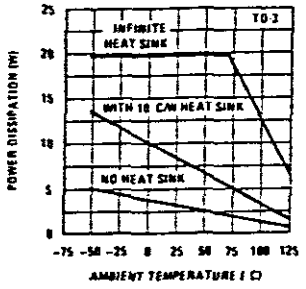
Plastic Package
TO-220 (T)



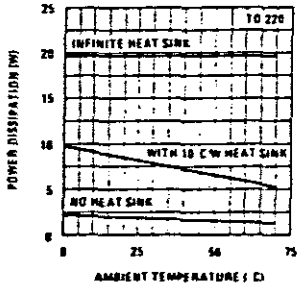
Order Numbers:
LM7805CT
LM7812CT
LM7815CT
See Package T03B

Typical Performance Characteristics

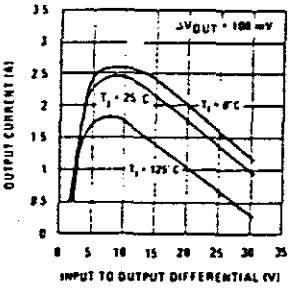
Maximum Average Power Dissipation



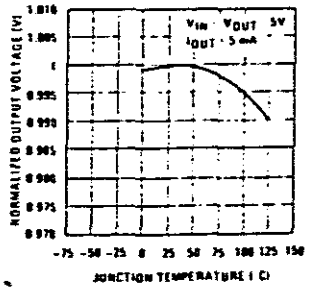
Maximum Average Power Dissipation



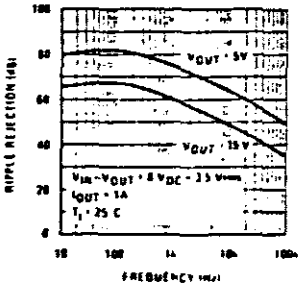
Peak Output Current



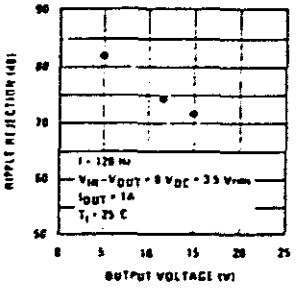
Output Voltage (Normalized to 1V at $T_j = 25°C$)



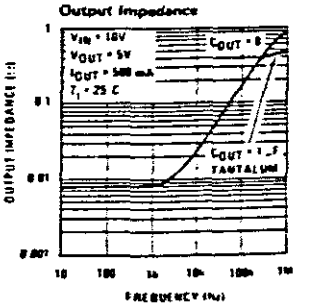
Ripple Rejection



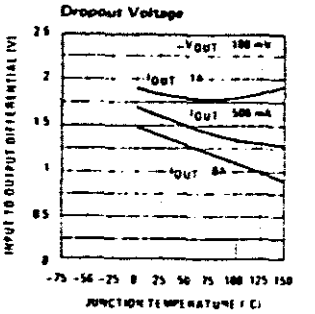
Ripple Rejection



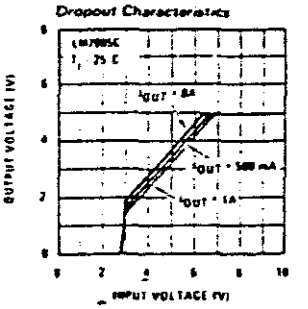
Output Impedance



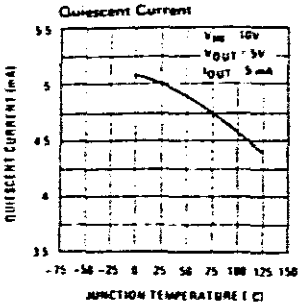
Dropout Voltage



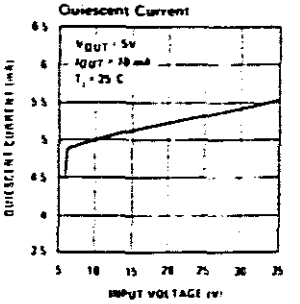
Dropout Characteristics



Quiescent Current



Quiescent Current



Absolute Maximum Ratings

Input Voltage (V_O = 5V, 12V and 15V)	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range (T_A)	0°C to +70°C
Maximum Junction Temperature	
(K Package)	150°C
(T Package)	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	
TO-3 Package K	300°C
TO-220 Package T	230°C

Electrical Characteristics LM78XXC *(Note 2)* $0°C \le T_J \le 125°C$ unless otherwise noted.

OUTPUT VOLTAGE				5V			12V			15V			UNITS
INPUT VOLTAGE (unless otherwise noted)				10V			19V			23V			
PARAMETER		CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	T_J = 25°C, 5 mA ≤ I_O ≤ 1A		4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		$P_D \le$ 15W, 5 mA ≤ I_O ≤ 1A, $V_{MIN} \le V_{IN} \le V_{MAX}$		4.75		5.25	11.4		12.6	14.25		15.75	V
				(7 ≤ V_{IN} ≤ 20)			(14.5 ≤ V_{IN} ≤ 27)			(17.5 ≤ V_{IN} ≤ 30)			V
ΔV_O	Line Regulation	I_O = 500 mA	T_J = 25°C		3	50		4	120		4	150	mV
			ΔV_{IN}	(7 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			V
			0°C ≤ T_J ≤ +125°C			50			120			150	mV
			ΔV_{IN}	(8 ≤ V_{IN} ≤ 20)			(15 ≤ V_{IN} ≤ 27)			(18.5 ≤ V_{IN} ≤ 30)			V
		$I_O \le$ 1A	T_J = 25°C			50			120			150	mV
			ΔV_{IN}	(7.3 ≤ V_{IN} ≤ 20)			(14.6 ≤ V_{IN} ≤ 27)			(17.7 ≤ V_{IN} ≤ 30)			V
			0° ≤ T_J ≤ +125°C			25			60			75	mV
			ΔV_{IN}	(8 ≤ I_N ≤ 12)			(16 ≤ V_{IN} ≤ 22)			(20 ≤ V_{IN} ≤ 26)			V
ΔV_O	Load Regulation	T_J = 25°C	5 mA ≤ I_O ≤ 1.5A		10	50		12	120		12	150	mV
			250 mA ≤ I_O ≤ 750 mA			25			60			75	mV
		5 mA ≤ I_O ≤ 1A, 0°C ≤ T_J ≤ +125°C				50			120			150	mV
I_Q	Quiescent Current	$I_O \le$ 1A	T_J = 25°C			8			8			8	mA
			0°C ≤ T_J ≤ +125°C			8.5			8.5			8.5	mA
ΔI_Q	Quiescent Current Change	5 mA ≤ I_O ≤ 1A				0.5			0.5			0.5	mA
		T_J = 25°C, $I_O \le$ 1A, $V_{MIN} \le V_{IN} \le V_{MAX}$				1.0			1.0			1.0	mA
				(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)			V
		$I_O \le$ 500 mA, 0°C ≤ T_J ≤ +125°C, $V_{MIN} \le V_{IN} \le V_{MAX}$				1.0			1.0			1.0	mA
				(7 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			V
V_N	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40			75			90		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz	$I_O \le$ 1A, T_J = 25°C or	62	80		55	72		54	70		dB
			$I_O \le$ 500 mA, 0°C ≤ T_J ≤ +125°C	62			55			54			dB
		$V_{MIN} \le V_{IN} \le V_{MAX}$		(8 ≤ V_{IN} ≤ 18)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)			V
R_O	Dropout Voltage	T_J = 25°C, I_{OUT} = 1A			2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz			8			18			19		mΩ
	Short-Circuit Current	T_J = 25°C			2.1			1.5			1.2		A
	Peak Output Current	T_J = 25°C			2.4			2.4			2.4		A
	Average TC of V_{OUT}	0°C ≤ T_J ≤ +125°C, I_O = 5 mA			0.6			1.5			1.8		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	T_J = 25°C, $I_O \le$ 1A		7.3			14.6			17.7			V

NOTE 1: Thermal resistance of the TO-3 package (K, KC) is typically 4°C/W junction to case and 35°C/W case to ambient. Thermal resistance of the TO-220 package (T) is typically 4°C/W junction to case and 50°C/W case to ambient.

NOTE 2: All characteristics are measured with capacitor across the input of 0.22 μF, and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \le$ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

8.5 Watt Triple Output

- Efficiencies to 78%
- Low Noise Operation
- Wide 4:1 Input Voltage Range
- Overvoltage Protection

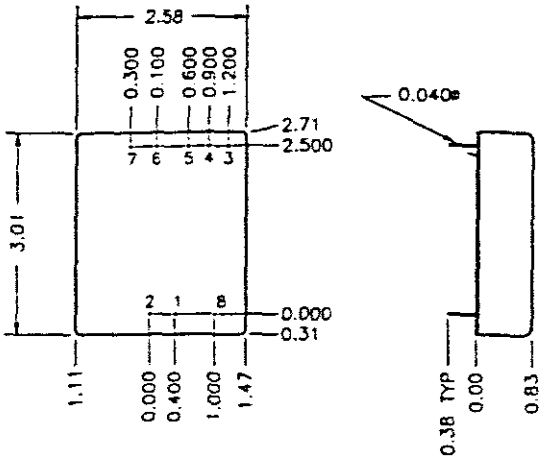
The wide input range of the 8.5 Watt triple series makes them ideal for solar powered RTU's and instruments.

These converters offer highly regulated triple outputs plus 500 VDC *input to output isolation. Each unit has both a logic* shutdown pin and thermal overload protection circuitry. All the outputs and the power switch are overvoltage protected.

8.5 Watt Triple Output			XC Case
INPUT VOLTAGE RANGE VDC MIN/MAX	OUTPUT VOLTAGE VDC	OUTPUT CURRENT mA	MODEL NUMBER
9.0/36.0	5, ±12	800, ±185	12T5.12UW
	5, ±15	800, ±150	12T5.15UW
18.0/72.0	5, ±12	800, ±185	48T5.12UW
	5, ±15	800, ±150	48T5.15UW
Mounting Kit		MS9	

LINE REGULATION TYPICAL	0.50%
LOAD REGULATION TYPICAL	2.00%
NOISE TYPICAL	20 mV P-P
ISOLATION	12T models: 700 VDC 48T models: 1544 VDC
CASE OPERATING TEMPERATURE	-25°C to +80°C
SIX-SIDED SHIELDED COPPER CASE	Do not immerse in liquid

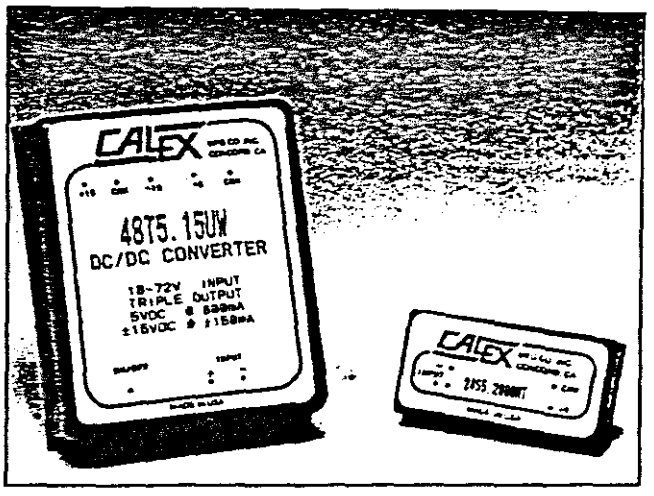
XC CASE: 8.5 Watt Triple UW



Pin	8.5 Watt Triple UW		
1	+INPUT	5	-12/-15V OUTPUT
2	-INPUT	6	+5V OUTPUT
3	+12/+15V OUTPUT	7	+5V CMN [1]
4	±CMN [1]	8	ON/OFF

[1] Note: Pins 4 and 7 are connected internally.

Pin	10 Watt Single NT
1	+INPUT
2	-INPUT
3	+OUTPUT
5	CMN



10 Watt Single Output

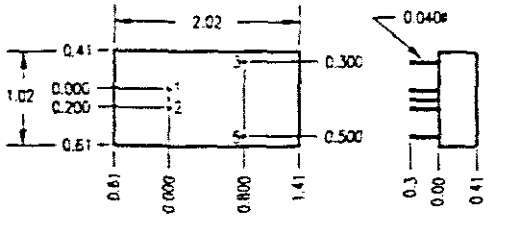
- High Power Density
- Water Washable Case
- Small 1.02" x 2.02" Cases
- Fully Self-Contained

These compact DC/DC converters are ideal for use in battery operated industrial, medical control and remote data collection systems. All inputs and outputs are fully filtered to minimize excess noise. Each converter is overload protected and offers a thermal shutdown system for maximum reliability.

10 Watt Single Output			E1 Case
INPUT VOLTAGE RANGE VDC MIN/MAX	OUTPUT VOLTAGE VDC	OUTPUT CURRENT mA	MODEL NUMBER
9.0/18.0	3.3	2000	12S3.2000NT
	5	2000	12S5.2000NT
	12	900	12S12.900NT
	15	700	12S15.700NT
18.0/36.0	3.3	2000	24S3.2000NT
	5	2000	24S5.2000NT
	12	900	24S12.900NT
	15	700	24S15.700NT
36.0/72.0	3.3	2000	48S3.2000NT
	5	2000	48S5.2000NT
	12	900	48S12.900NT
	15	700	48S15.700NT

LINE REGULATION TYPICAL	0.01%
LOAD REGULATION TYPICAL	0.2%
NOISE TYPICAL	60 mV P-P
ISOLATION	12S & 24S models: 700 VDC 48S models: 1544 VDC
CASE OPERATING TEMPERATURE	-25°C to +100°C
FIVE-SIDED SHIELDED COPPER CASE	Do not immerse in liquid

E1 CASE: 10 Watt Single NT



CALEX