DEVELOPMENT OF A "MAINS BORNE" REMOTE CONTROL SYSTEM

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Submitted in part fulfillment of the requirements laid down

for the

Master's Diploma in Technology

in the School of Electrical Engineering

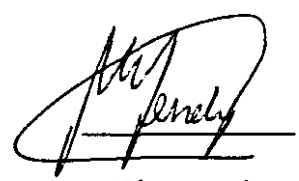
Cape Technikon

November 1991

Declaration

I declare that the contents of this thesis represents my own work and that the opinions contained herein are my own. This thesis has not been previously submitted for examination at this or any other institution.

N.B. van Ysendyk



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Synopsis

Many environments employ time switches to control the operation of electrical machinery and appliances. These devices are generally expensive and require extensive wiring and individualised treatment. The need therefore arises for a more efficient and economical control system that will not be subjected to the limitations found in conventional remote control systems.

This thesis describes a universal remote control system developed to suitably replace conventional systems prone to various limitations and restrictions. The system is "mains borne" and therefore makes use of the mains wiring for interconnectivity. The term "Mains borne" refers to the communicating medium interconnecting the various components.

Opsomming

Tydskakelaars word algemeen gebruik om elektriese masjinerie en toebehore te beheer. Hierdie skakelaars is gewoonlik duur en benodig ingewikkelde bedrading en individuele aandag. Daar bestaan dus 'n behoefte aan 'n meer effektiewe en ekonomiese beheerstelsel wat die beperkinge van die konvensionele afstandbeheerstelsels oorkom.

Hierdie tesis beskryf 'n veeldoelige afstandbeheerstelsel wat ontwikkel is om die beperkings van die konvensionele stelsels te oorkom en hierdie stelsels effektief te vervang. Hierdie stelsel gebruik die hoofkragtoevoerbedrading as kommunikasiemedium.

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1. Introduction.

A wide variety of techniques are employed in the industrial environment to control various manufacturing processes. These techniques may vary from manually controlled to microprocessor controlled processes and are subjected to one or more of the following limitations:

Interconnecting wiring and equipment required

Duplication of equipment

Inaccurate and unreliable operation

Synchronisation and coordination problems

Maintenance difficulties

Inadequate and obsolete status information

In the domestic environment, particularly in first world countries, the employment of time switches to control appliances such as central heating, security lighting, immersion heaters, irrigation systems and greenhouse heating, is rapidly increasing. As in the case of the industrial environment the domestic switches are also limited.

The objective of this project is to devise a system that will not be prone to the previously mentioned limitations and at the same time be suitable for use in both the industrial and domestic environments to automate the switching of machinery and appliances.

This is accomplished by a system comprised of a central controller/local transceiver and remote transceivers which use the mains wiring for interconnectivity. The transceivers have the capability of transmitting and receiving serial bit streams of virtually any coding which permits the transfer of information between two or more locations.

2. Modes of Operation.

Refer to Figures 1 and 2. The Remote Control System, comprising of a controller, a local transceiver and a remote transceiver, has two modes of operation viz. The Remote Control Mode and The Half-Duplex Mode. The first mode of operation enables the automated switching of remote electrical devices while the second mode makes intercommunication between the local and remote transceivers possible. Although the latter is not defined as being part of the thesis it has been included on account of the integral part it is envisaged to play in the future of remote control.

Figure 3 illustrates how the two modes of operation could be combined to produce a Half-Duplex Remote Control System that, in addition to automatically switching remote electrical devices on or off, will also support inter-transceiver communication which may be used for a large variety of applications including the management of energy consumption, remote site maintenance and the gathering of statistical data. Mode selection instructions and circuitry will be dealt with at a later stage.

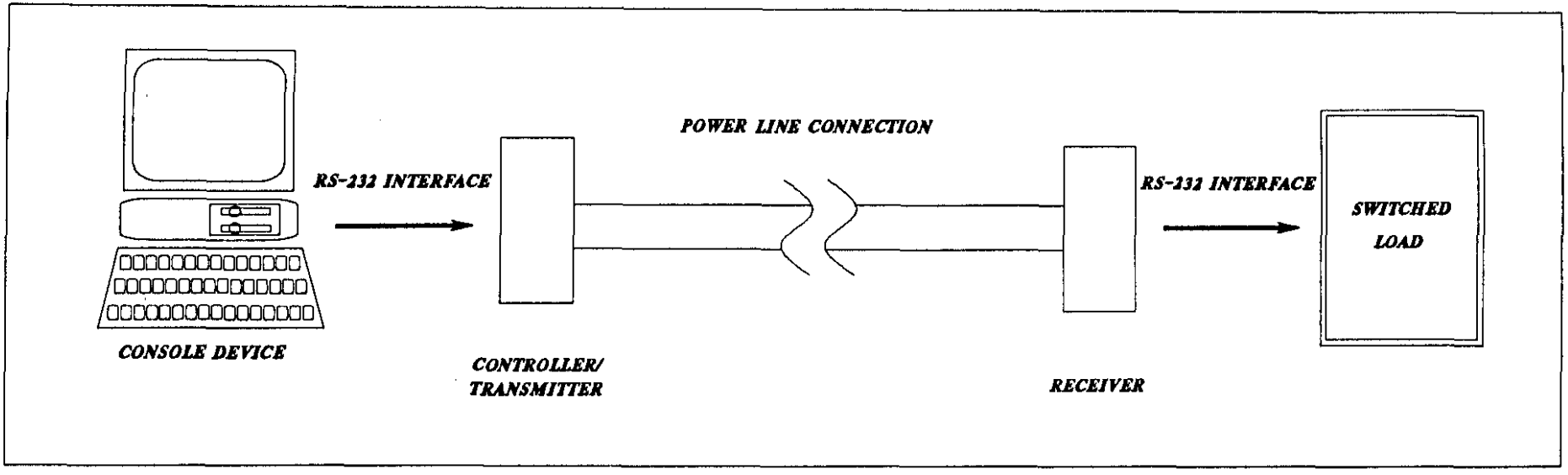


FIGURE 1 - REMOTE CONTROL MODE

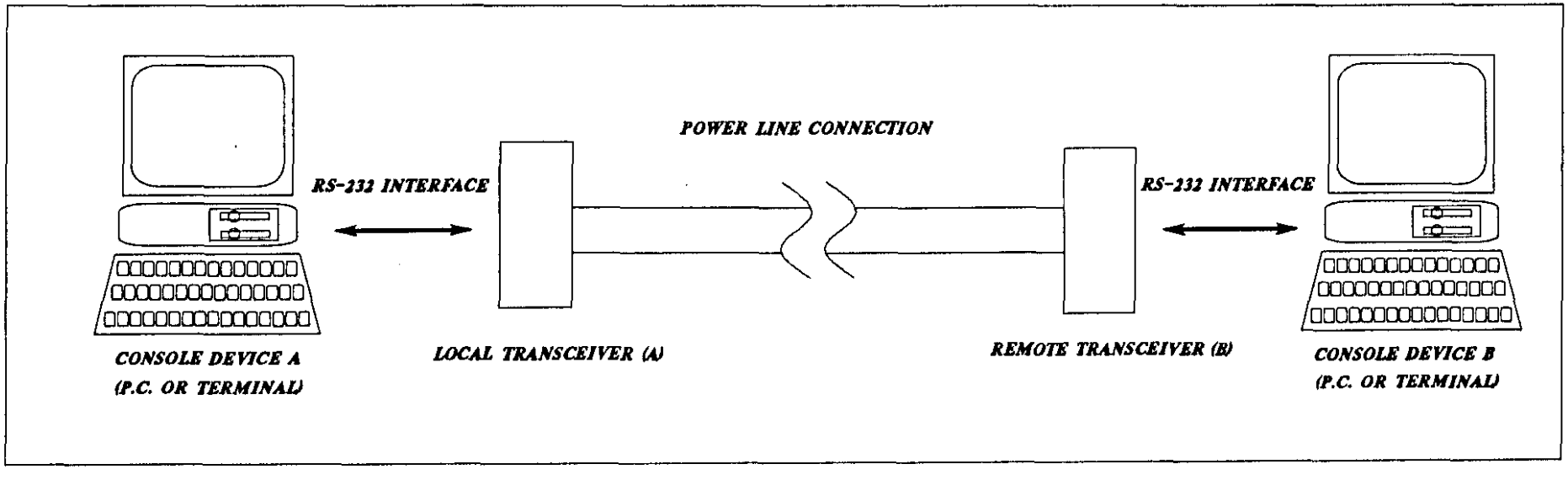


FIGURE 2 - HALF-DUPLEX MODE

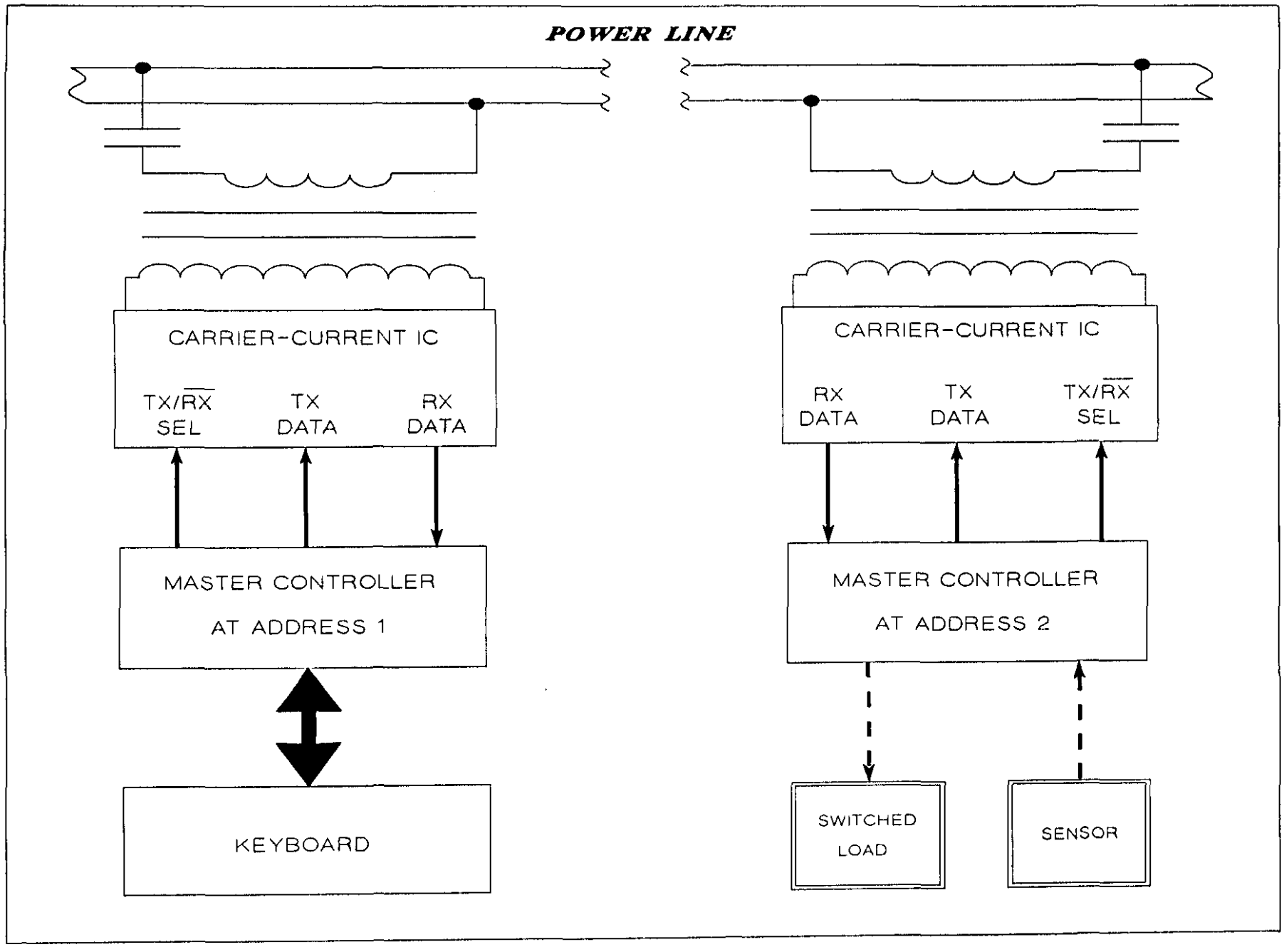


FIGURE 3 – HALF-DUPLEX REMOTE CONTROL SYSTEM

2.1 Remote Control.

Refer to Figure 4,5 and 6. The controller (Figure 4) is equipped with an RS-232 interface which serves to connect the 8052AH microcontroller to a console device. The RS-232 levels are generated and received by a line driver/receiver (U6) which is compatible with all RS-232 and V.28/V.24 communications interfaces. The console device, facilitates the manipulation of resident programs as well as the entering of the time of day and the remote switching times. If a Personal Computer is used, terminal emulation software will be required.

The controller according to pre-defined time intervals, generates an appropriate address to switch a particular remote device on or off. This address is sampled by the Digital Code Transmitter (U2) on the Local Transceiver (Fig. 5) and a TTL coded pattern, corresponding to the address issued by the controller, is generated. This output pattern is converted into a sinusoidal, FSK-modulated waveform by the Carrier-Current Transceiver (U1). This waveform is then impressed on the power line by the coupling transformer (T1).

The sinusoidal waveform is filtered from the mains line by the receive coupling transformer (T1) on the remote transceiver (Fig. 6). The Carrier-Current Transceiver (U1), 8 compensates for varying mains line conditions and converts the current sinusoid back into a TTL coded waveform. The Digital Code Receiver (U2) compares the incoming signal with the preset remote code (set on SW 1 and SW 2) in a sequential manner. Should all the bits of the preset code correlate with the received code, U2 will generate a valid signal which, after being inverted, drives a D-Type Positive Edge Triggered Flip-Flop (U3A). The non-inverting output

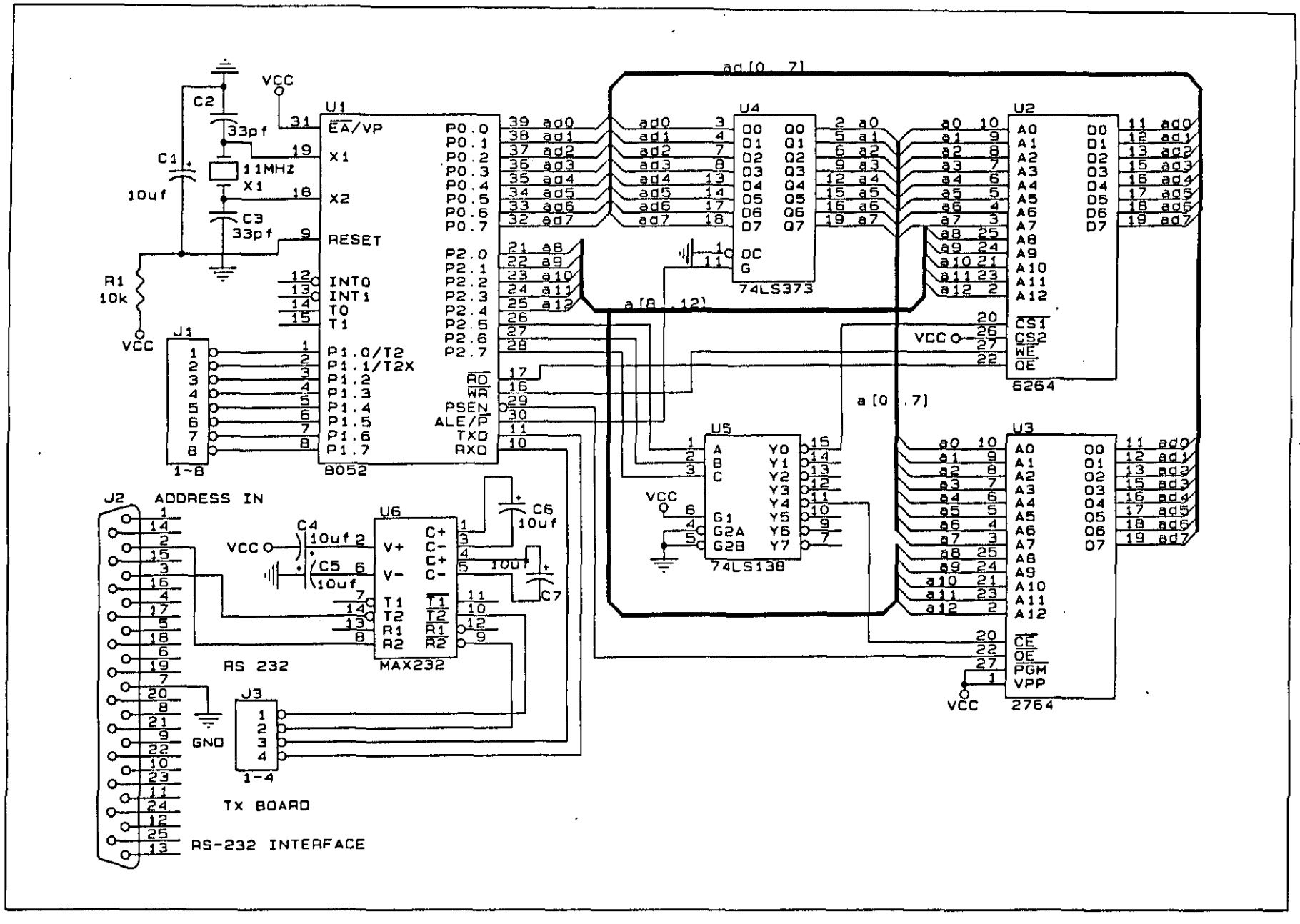


FIGURE 4 - CONTROLLER SCHEMATIC

of the Flip-Flop is coupled to transistor TR1 which serves as a driver circuit for the solid-state switching relay (Relay 1). The inverting input of U3A inverts the Digital Code Receiver inputs D1 and D8 so that the deactivation address is dissimilar to the activation address. This is a precautionary measure to prevent the defective operation of the relay which could otherwise result from power line noise.

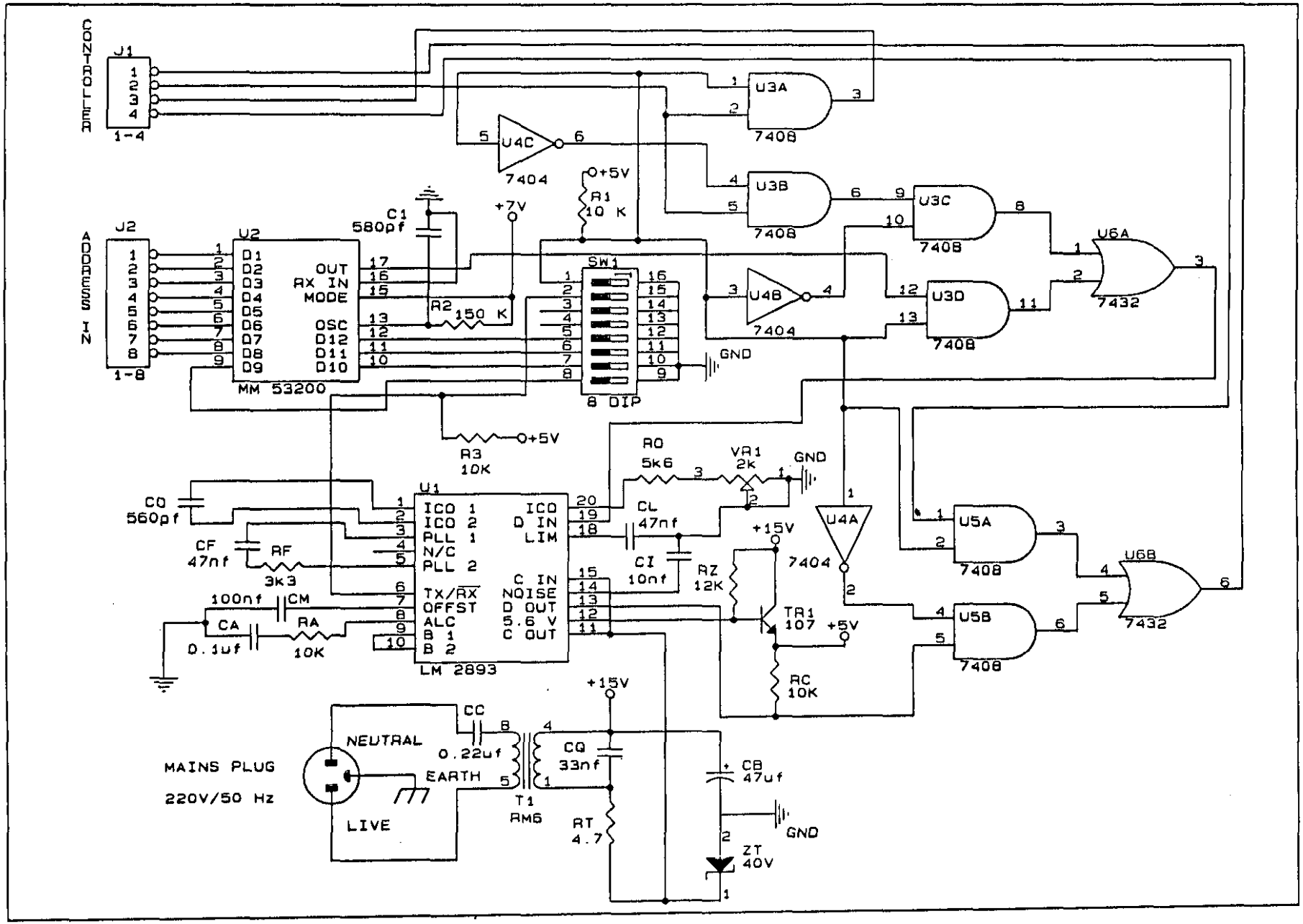


FIGURE 5 - LOCAL TRANSCEIVER SCHEMATIC

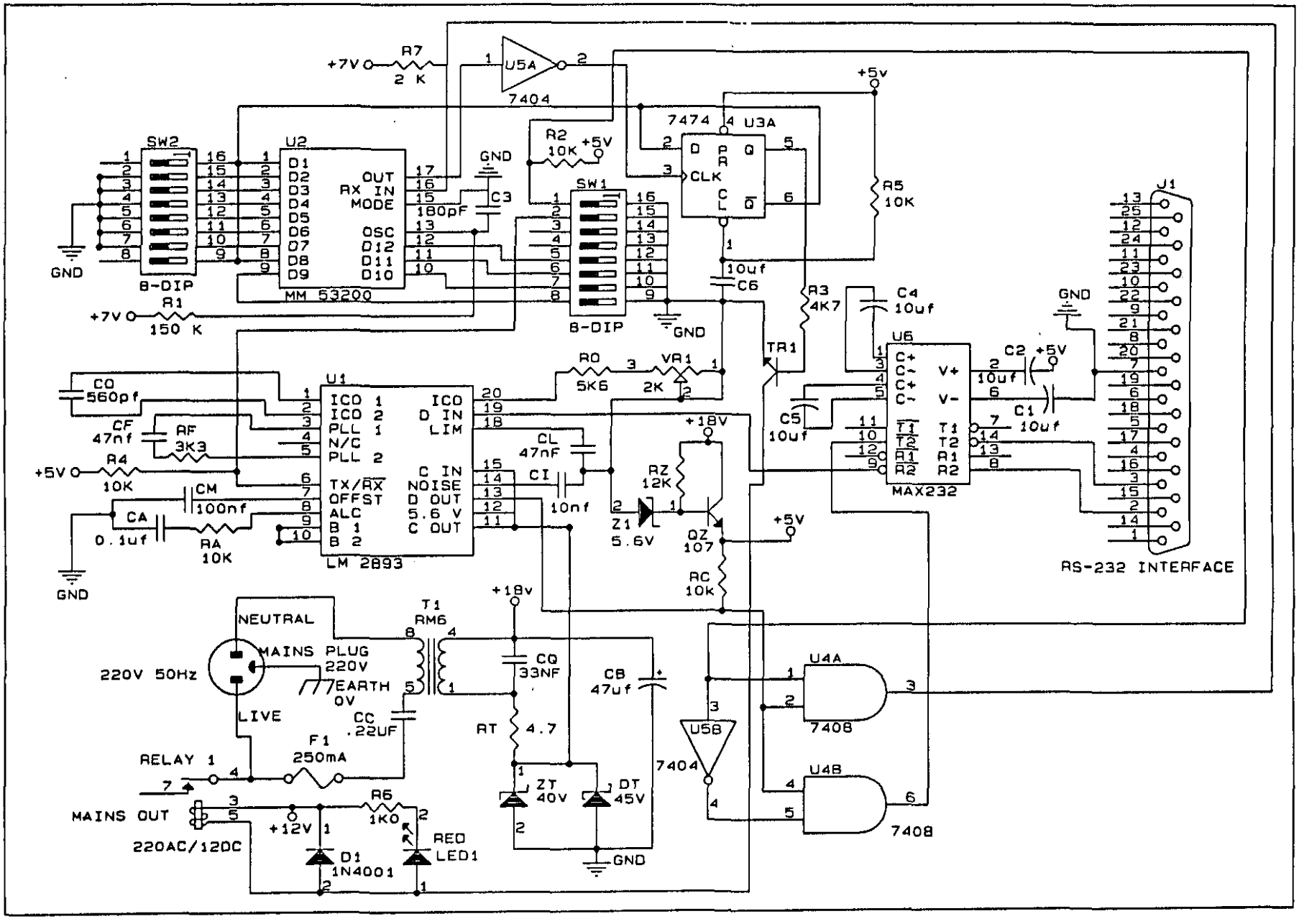


FIGURE 6 – REMOTE TRANSCEIVER SCHEMATIC

2.2 Half-Duplex Data Transmission.

Refer to Figures 4,5 and 6. In the Half-Duplex Mode of operation the control board (8052AH microcontroller and peripheral components) is not required and is disconnected from the local transceiver on selection of this mode. Figure 2 illustrates the configuration used to establish, mains borne, inter personal computer communication at speeds up to and including 4800 bits per second. In this example of Half-Duplex operation, the local transceiver's RS-232 interface, used to connect a terminal or P.C. to the controller in the remote control mode, is now used to interface the local P.C. to the local transceiver. Because the transmission paths between location A and location B are identical, it is necessary to explain one direction only.

Data emanating from the P.C. at point A is referred to transceiver A via the RS-232 interface. The data on entering the transceiver is routed by logic to the Current-Carrier Transceiver for conversion from a TTL waveform to a sinusoidal waveform. As the Digital Code Transmitter/Receiver (U2) is used for the addressing of remote devices in the Remote Control Mode only, it does not play any role in the half-duplex transmission of data and is therefore excluded from the circuit. As in the previous mode, the sinusoidal waveform is superimposed onto the mains line by the mains interface and recovered by the remote transceiver's line filter.

The recovered signal is reconverted into a TTL waveform and fed via logic to the RS-232 interface. The remote transceiver (transceiver B) is equipped with a Line

Driver/Receiver (U6) solely for this purpose. The RS-232 output levels are detected and processed by the remote P.C. at point B.

3. Hardware Design.

3.1 Power Supplies.

The local and remote units have similar power requirements. Tests revealed that the controller/transceiver combination (local unit), under full load conditions, required approximately 280 mA while the remote unit required approximately 150 mA.

Refer to figure 7. A 12/12 volt, 500 mA transformer is used to power the local supply. The two 12 volt coils are connected in series resulting in a 29 volt RMS AC unregulated supply voltage. A 24 volt DC supply voltage is attained after rectification. A smoothing capacitor (C1) provides the initial stage of ripple elimination. Two +5 volt regulators (REG1 and REG2), a 15 volt regulator (REG3) and associated smoothing capacitors (C2-C4) provide the regulated +5, +8 and +15 volt supplies. Resistors R1 and R2 connected to terminals 2 and 3 of REG2 produce the desired +8 volt regulated supply. REG1's function is to reduce the rectified 24 volt supply down to a 5 volts regulated supply i.e. a voltage reduction of 19 volts. This regulator, having to supply power to all of the 5 volt components, on both the controller and the local transceiver, is naturally subjected to a large load. This large load together with the large reduction in voltage necessitates that a heatsink be fitted to this regulator. The remote unit supply differs to the local unit supply in that it has a 250 mA transformer. The two power supplies are otherwise identical.

The requirement for a $\pm$ 12 volt supply was eliminated by using the MAX 232 line

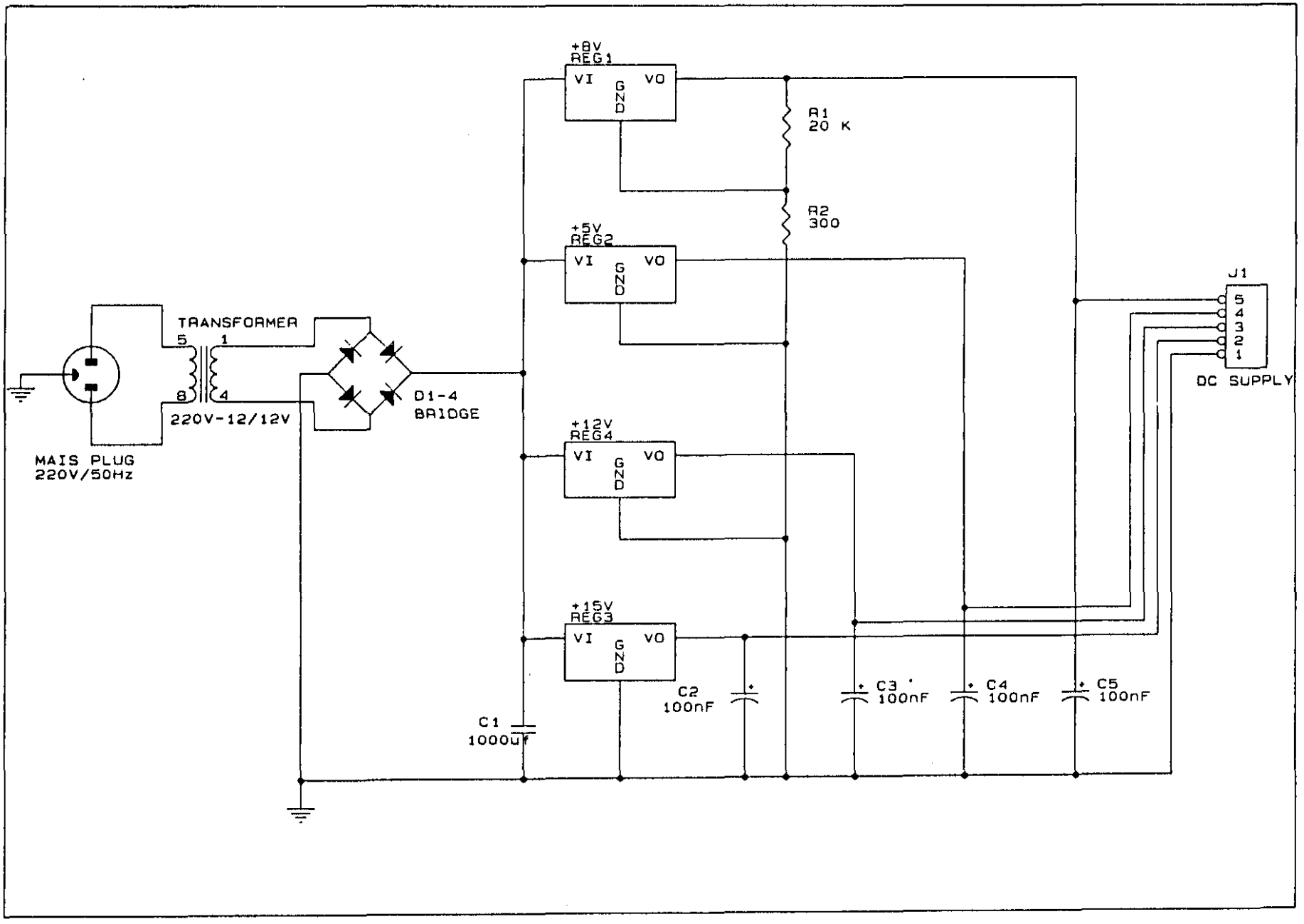


FIGURE 7 - POWER SUPPLY SCHEMATIC

driver/receiver for the RS-232 interface on the controller and remote transceiver. The MAX 232 has the advantage over conventional line driver/receivers in that it requires a supply voltage of +5 volts and not $\pm$ 12 volts.

3.2 *Controller.*

Figure 4 represents the controller board schematic diagram.

3.2.1 Microcontroller and Latch.

The 8052AH-BASIC 8-Bit microcontroller used has a full-featured basic interpreter, resident in the 8K of available ROM. Virtually all of the special function registers can be addressed allowing the user to set the timer or interrupt modes within the constructs of a BASIC program. An accurate interrupt driven REAL TIME CLOCK with a 5 millisecond resolution is also implemented. The clock can be enabled, disabled and used to generate interrupts. The 8052AH-BASIC is also capable of generating all of the timing necessary to program any standard EPROM with little external hardware being required.

Port 1 is a general purpose quasi-bidirectional 8-bit input/output port. The individual pins on this port have alternate functions which may be implemented if required. In this application Port 1 is used to output an 8 bit address for the switching of the remote electrical devices. The low-order address and data bus are multiplexed on port 0 with the low-order address being latched by the 74LS373 address latch. The latch is gated by the Address Latch Enable (ALE) on the microcontroller. Port 2 is used for the high order address during external memory access. The Program Store Enable pin ($\overline{\text{PSEN}}$) is used to enable EPROM memory that is addressed from 2000H to 7FFFH. For addresses between 8000H and 0FFFFH both the $\overline{\text{RD}}$ and $\overline{\text{PSEN}}$ pins are used to enable memory.

Other features of the microcontroller are :

128 Bytes Internal Data Memory

32 Programmable I/O lines

Two 16-Bit timer/counters

5 Interrupt Sources

64K Program Memory Space

3.5 to 12.0 MHz Oscillator Frequency

5 Volts Operating Voltage

3.2.2 Address Decoder.

The controller board is memory mapped and chip selection is accomplished using a SN74LS138 address decoder. Address lines A13-A15 on the microcontroller are used to select one of eight outputs on the decoder. Only two outputs are used in this application with the remaining outputs being available for future applications. Noteworthy specifications are:

4.75 to 5.25 V Supply Voltage

10 mA Maximum Supply Current

3.2.3 EPROM

The EPROM used is an Intel 2764, 5 volt, 65,536-bit, ultraviolet erasable and

electrically programmable read-only memory. It features a 200 nsec. access time and a standby mode which reduces power consumption from 60 mA to 20 mA without effecting the access time. The standby mode is initiated by pulling the Chip-Enable Input high. When in standby mode the outputs are in a high impedance state. Noteworthy specifications are:

± 5 % Variation of Supply Voltage

21 V Programming Voltage

3.2.4 RAM

The 8052AH-BASIC requires at least 1K of external memory (RAM) before it will issue the sign on banner to the console device. After reset the microcontroller sizes consecutive external memory locations from 0000H to 0DFFFH by writing 55H to each location and then verifying that the location contains this hex code. Once 1K of external memory is tested to be available the microcontroller will "sign on."

The HM6264LP-C-MOS Random Access Memory is used to provide the required 1K of external memory and to accommodate programs transferred from the EPROM for editing when the XFER command is used. The HM6264LP-C-MOS RAM has 65536 memory locations and can therefore store 8192 8-bit words. Noteworthy specifications are:

150 nsec. Maximum Access Time

5 V Supply Voltage

110 mA Supply Current

2 μA Typical Standby Supply Current

3.2.5 RS-232 Line Driver/Receiver

The RS-232 interface serves a dual purpose. Firstly, the console orientated features of the 8052AH-BASIC necessitates the requirement for an RS-232 interface. The second function of the interface is to accommodate the Half-Duplex Mode of operation. The MAX232 Line Driver/Receiver is used because it has the distinct advantage over conventional line drivers/receivers in that it only requires a single +5 volt supply voltage as opposed to a $\pm$ 12 volts supply.

The MAX232 is intended for all RS-232 and V28 communications interfaces. The low power shutdown reduces the power dissipation to less than 1 mA. The line driver/receiver has an on-board charge pump voltage converter which converts the +5 volts input power to the $\pm$ 10 volts needed to generate the RS-232 output levels.

3.3 Local and Remote Transceivers.

Figures 5 and 6 represent the Local and Remote Transceiver schematic diagrams. The transceiver's are similar in terms of hardware and are therefore categorised together.

3.3.1 Mains Interface.

In order to effectively superimpose and extract the sinusoidal waveform, generated by the Current-Carrier Transceivers, onto and from the mains line, a suitable interface is required that will match the impedances of the two circuits and allow the transfer of information between these circuits.

The coupling circuit may be described as a resonance tank and band-pass filter on the one hand and a high pass filter on the other. The resonance tank and band-pass filter is made up of capacitor CQ and T1's primary winding while the high pass filter is comprised of CC, T1's secondary winding and the tank band-pass filter. Capacitor CB acts as a supply bypass to reduce supply spikes.

During the transmission of the sinusoidal waveform, drive current from Current-Carrier Transceiver's Carrier I/O pin develops a voltage swing on T1's resonant tank proportional to the line impedance which passes through the high pass filter to the power line. Progressively small line impedances cause reduced signal swing, but never clipping thus avoiding potential radio frequency interference.

On receipt of the sinusoidal waveform, carrier signal, broad-band noise, transient spikes, and power line component impinge on the high pass filter. In band carrier signal, band limited noise, heavily attenuated line frequency component, and attenuated transient energy pass through to produce a voltage swing on the resonance tank, swinging about the positive supply to drive the Carrier I/O pin on the Current-Carrier Transceiver (refer to Fig.5 and 6 on pages 9 and 10).

3.3.1.1 Wide Band Transformer Analysis.

The term "wide band transformer" refers to a transformer that is specifically designed to pass a band of frequencies exceeding a few decades.

The principal function of a wide band transformer is to transfer information. This transfer of information, in the form of energy, should be efficient, but this requirement is viewed in a special sense in electronic circuits. Efficiency in the conventional sense (the ratio of power output to power input) is supplanted by the concept of the ratio of signal to noise.

Although the wide-band transformer is required to pass a broad band of frequencies, the distortion must be constrained. The various factors to be taken into account can be inferred from a complete set of specifications. The requirements parallel those for an ordinary power transformer, with additional constraints on the variation of amplitude and phase shift with frequency, the amount of harmonic distortion, the degree of unbalance and the vulnerability to stray fields. The effect of the external circuit must also be taken into account.

The Current-Carrier Transceiver is capable of generating an FSK modulated 50 to 300 kHz carrier and is therefore considered to operate in the mid-band frequency range. A mid-band frequency Wm may be defined by the expression:

$$Wm = \sqrt{(W1 \times W2)}$$

which is the geometric mean of the low-frequency cutoff W1 and the high frequency cutoff W2. Because Wm >> W1, the flux density is low in the mid-band frequency range and the shunt core-loss resistance is negligible. When the source resistance is fixed, the maximum overall gain occurs when the load resistance is matched to the source resistance.

The following transformer characteristics are important at the mid-band frequency: (1) related load power, (2) turns ratio, (3) transformer losses, (4) reflected impedance, and (5) degree of mismatch. The bandwidth of the transformer is inversely proportional to size, which is in turn proportional to the magnitude of the low frequency cutoff. The reduction in size of the wide-band transformer design proceeds until one of the following factors set a lower limit: (1) The allowable low frequency flux density (a function of harmonic distortion, shunt inductance and polarising bias), (2) The copper efficiency and regulation at the mid-band frequency, (3) the dielectric constraints.

3.3.1.2 Power Line Impedance.

Because power line impedance is known to vary enormously with changes in the power

line load, there are no guarantees on power line impedance irrespective of how wide the limits are placed. However, for this interface circuit design an estimation of the lowest expected line impedance ZLN to be encountered is acceptable for the determination of an efficient transmitter-to-line coupling. Once the line impedance is estimated to a given confidence level, reasonable values for the coupling transformers turns ratio, loaded Q factor and tank resonant frequency pull FQ may be found to enable the interface circuit design to function over the majority of power lines.

Figure 8 and 9 depict a limited sampling of line impedance on residential and commercial power lines. All measured impedances are contained within the shaded portions of Figure 8.

3.3.1.3 Power Line Attenuation.

All referenced line impedances refer to Live-to-Neutral impedances with a grounded center conductor. A typical power cable has a 100 Ω characteristic impedance, 125 kHz quarter-wavelength of 600m and a measured 7 dB attenuation for a 50 m run with a 10 Ω termination.

Tests conducted by National Semiconductor Corporation, on domestic and industrial power lines, show that the sinusoidal waveform superimposed on one phase of a distribution transformer was capable of covering distances up to 100's of meters, with link failure often occurring across transformer phases or through transformers unless coupling networks are

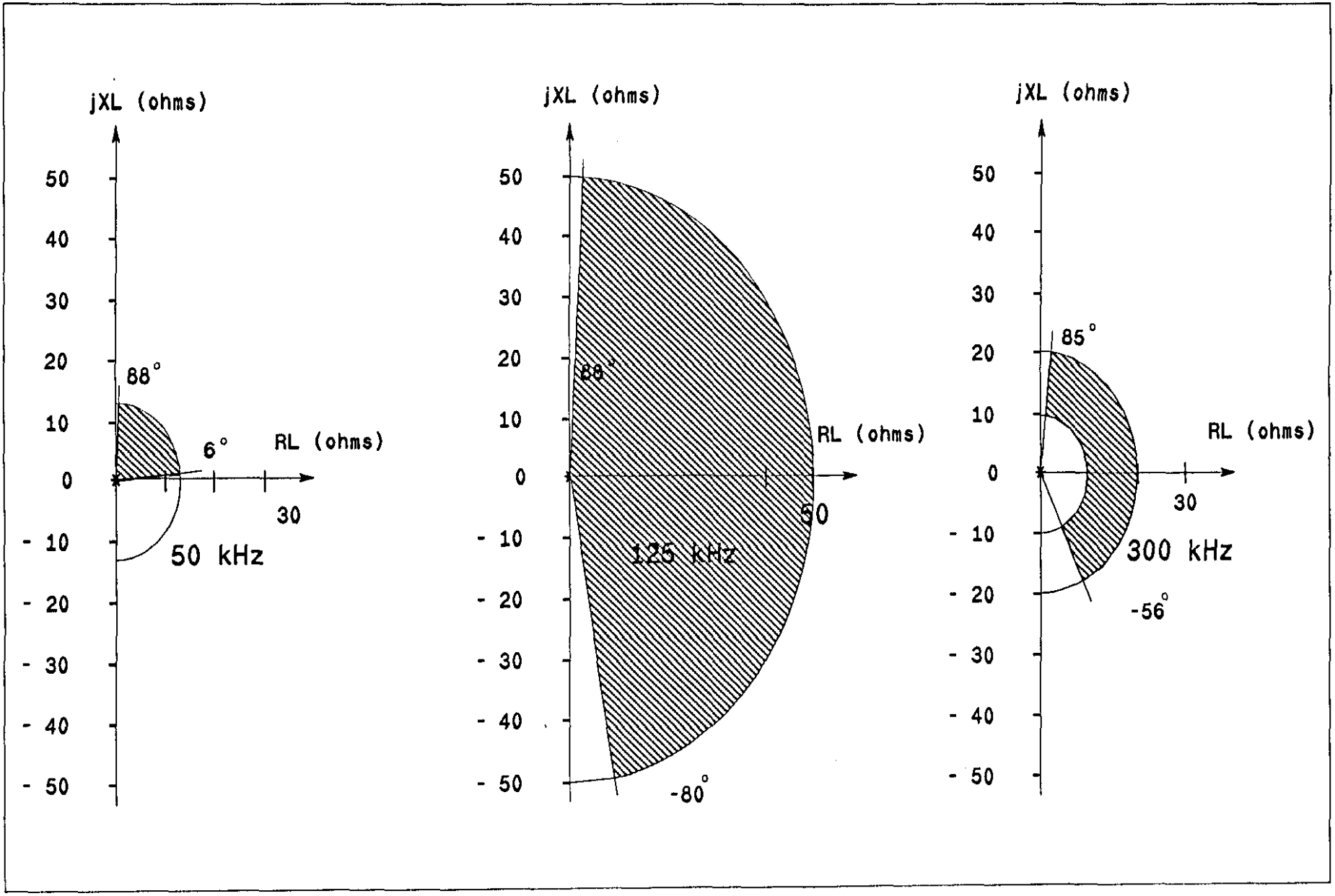


FIGURE 8 - COMPLEX-PLANE PLOTS OF MEASURED LINE IMPEDANCES

utilised. Total line attenuation allowed from full signal to limiting sensitivity is more than 70 dB. The signal may be coupled across the transformer phases by parasitic winding capacitance, giving 40 dB attenuation between phased 220 volt windings. Coupling capacitors may be installed for improved link operation across phases.

Power factor correction capacitor banks or filter capacitors across the power lines attenuate the carrier signal and should be isolated with inductors. An increased range may be accomplished by installing isolating inductors and coupling capacitors as well as using the boost option (see Figure 11) on the Current-Carrier Transceiver. Frequency translation or time division multiplexed repeaters will also increase range. In addition to preventing a low impedance device (measured at 125 kHz) from shorting the carrier signal, the isolation network also prevents devices from polluting the power line with noise.

3.3.1.4 Design Synthesis.

The goals of (1) building T1 with a stable resonant frequency, FQ, that is little effected by the de-tuning effect of the line impedance, ZL and of (2) building a tightly line-coupled transformer for transmitted carrier with loose coupling for transients are somewhat mutually exclusive. To accommodate these goals using a single transformer, a tradeoff between coupling, stability and selectivity must be made.

The design arrived at is a coupling network that functions as a band-pass filter, has loose coupling between the primary and secondary and has a single secondary. The turns ratio of 9

to 1 was selected from Figure 10, which is based on an estimated lowest line impedance, ZN, of 10 Ω that is likely to be encountered. This turns ratio produces a line signal voltage of approximately 3 volts peak-to-peak. The value of 10 Ω for ZLN is determined from Figure 9. The inductance of the tuned primary, L1, is determined as follows:

$$L1 = \frac{R}{2\pi\ Fo \times Q}$$

While standard transformer design gives a transformer self-inductance with an impedance at operating frequency well above load impedance, the tuned transformer requires a low L1 for adequate voltage magnification and minimum line pull resulting in relatively poor mutual coupling. If R in the previous expression is expanded, L1 becomes:

$$L1 = \frac{RQ\ //\ |ZLN|}{2\pi Fo \times QL}$$

where | ZLN | is the reflected line impedance, QL the loaded Q factor, and parallel resistance RQ models all transformer losses. The numerator is found knowing that the transformer is to function with an output current Io of up to 600 mApp.

$$Po = IoVo = \frac{Iopp}{2\sqrt{2}} \left[\frac{2(-\ VALC + V)}{2\sqrt{2}} \right] = \frac{(-\ 4.7 + V)\ Io}{4}$$

where Io is expressed in amps peak-to-peak.

$$Po = \frac{(18 - 4.7)\ 0.06}{4} = 0.200\ W$$

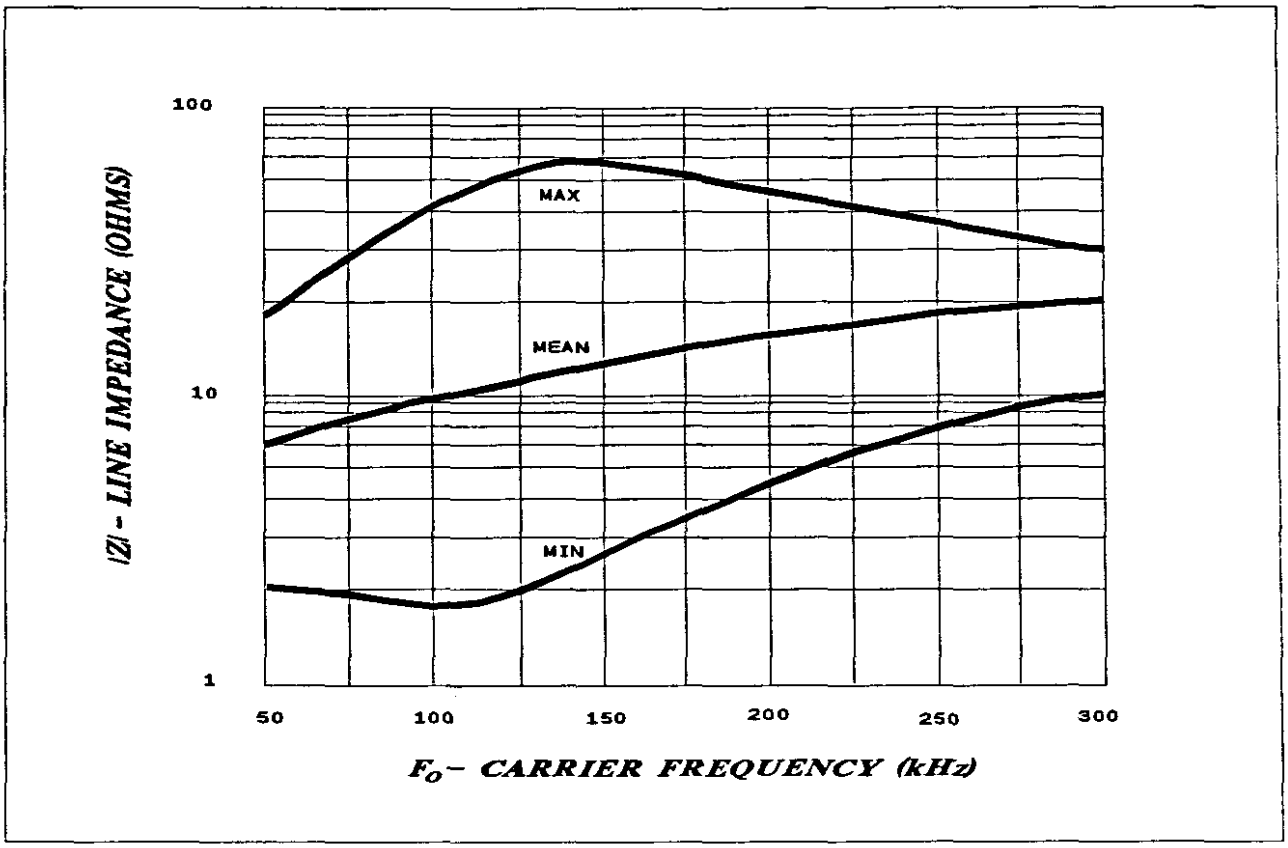


FIGURE 9

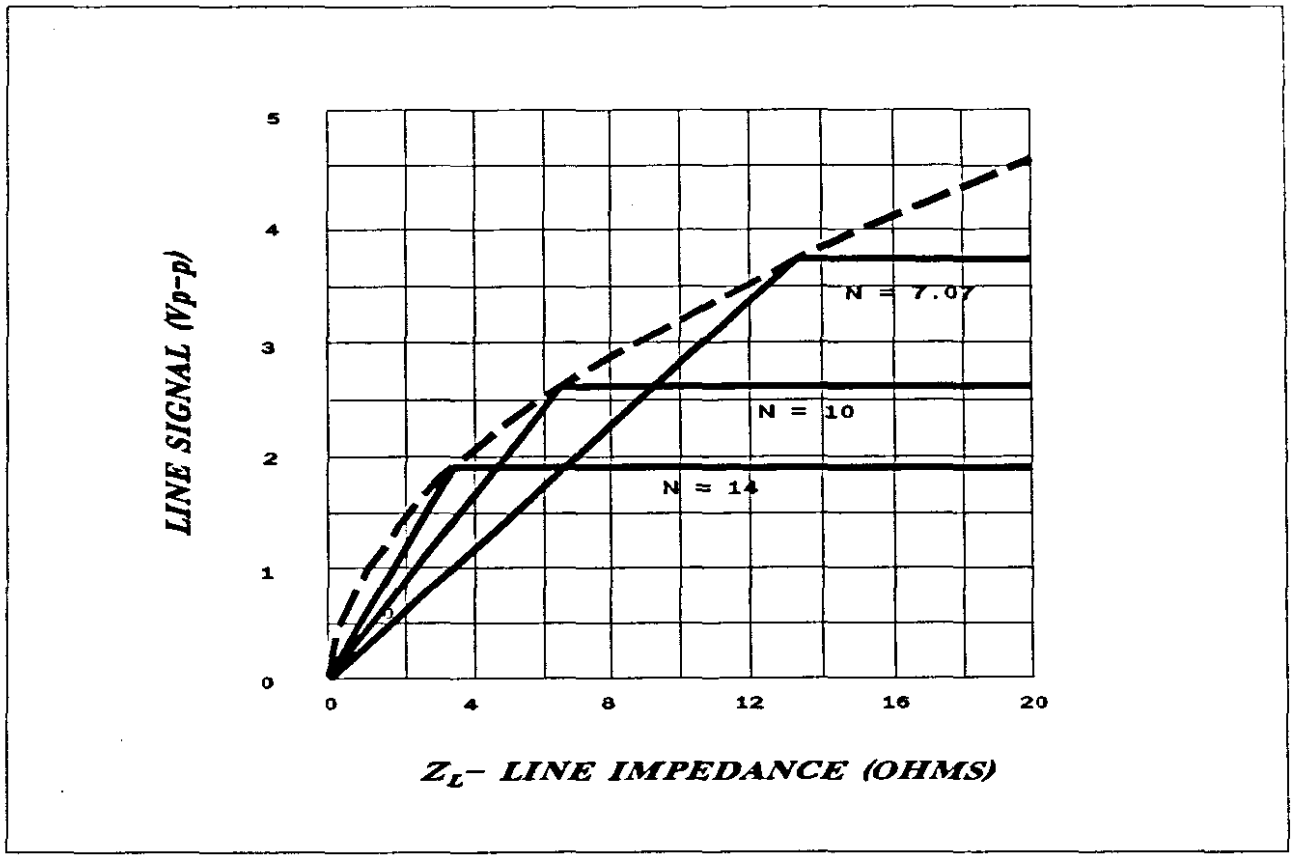


FIGURE 10

$$RQ \;//\; |ZLN| = \frac{(Vo)^2}{Po} = \frac{(9,42)^2}{0.200} = 442\ \Omega$$

QL is related to the -3 dB (half-power) bandwidth by:

$$QL = \frac{1}{BW(\%\ of\ Fo)}$$

The Current-Carrier Transceiver deviates from the carrier frequency by 4.4 % i.e. Fc $\pm$ 2.2 %. The effect of line pull is estimated to cause approximately 3.3 % deviation. The bandwidth required is approximated to be around Fc $\pm$ 8.7% which includes a 1 % temperature coefficient, giving QL a value of 11.5. Therefore L1 becomes:

$$L1 = \frac{442}{2\pi \times 125\ 000 \times 11.5} = 49.0\ \mu H$$

The number of turns is found knowing the core inductance per turn and L1.

$$T1 = \sqrt{\frac{L1}{L}} = \sqrt{\frac{49.0\ \mu H}{20\ nH/T}} = 49\frac{1}{2}\ turns$$

The secondary turns are calculated by taking the turns ratio into account:

$$T2 = \frac{T1}{N} = \frac{49.5}{9} = 5\frac{1}{2}\ turns$$

The resonance capacitor is calculated as follows:

$$CQ = \frac{1}{(2\pi FQ)^2 \times L1} = 33\ nF$$

Because the coupling transformer is used as a filter, the Current-Carrier Transceiver is susceptible to pulling off the center frequency under conditions of changing line impedances or when several Current-Carrier Transceivers are in close proximity on the mains line. Because the tuned transformer has a high Voltage Magnification Factor, Q, ringing will occur at the center frequency, in the presence of impulse noise. This has the effect of increasing the error rate of data transmissions, especially at relatively high data transmission rates (>2000 baud). Being the only tuned circuit in the system the selectivity is relatively limited.

The disadvantages discussed above may be eliminated by separating the transmit output and receive input. An untuned transmit coupling transformer with only core coupling (not air-coupled solenoid windings) would employ a high permeability, high magnetic field, low loss, square saturating, toroidal core. The resonant receive path would be isolated from line-pull problems by a unilateral amplifier that operates the line voltage with much more than 110 dB of dynamic range.

3.3.1.5 Transient Protection.

Potentially damaging transient energy passes through transformer T1 onto the Current-Carrier Transceiver I/O pin. For self protection the Current-Carrier Transceiver has an internal 44 V voltage clamp with a 20 Ω series resistance. A parallel low impedance 40 volt external transient suppression diode D1 (Figure 11) shunts the lions share of any current to

earth when transients force the Carrier I/O to a high voltage.

3.3.2 Carrier-Current Transceiver.

Figure 11 represents the block diagram of the Carrier-Current Transceiver. This bipolar Carrier-Current chip performs as a power line interface for half-duplex (bidirectional) communication of serial bit streams of virtually any coding. In transmission, a sinusoidal carrier is FSK modulated and impressed on the mains power line via a rugged on-chip driver. In reception, a phase-locked loop-based demodulator and impulse noise filter combine to give maximum range. Additional features offered by the Carrier-Current Transceiver are data transmission rates up to 4,8 kBaud, transmission of strings of 1's and 0's, sinusoidal line drive for low radio frequency interference, output power boost circuit, 50 to 300 kHz carrier frequency bandwidth, TTL and MOS compatible digital levels, and regulated voltage to power logic. Noteworthy specifications are:

13.5 - 30 V Supply Voltage

60 V Carrier I/O Peak Survivable Transient Voltage

41 V Carrier I/O Clamp Voltage

10 μs Rx-Tx Switch-Over Time

2 Bit Tx-Rx Switch Over Time

3.7 - 5.2 % FSK Deviation

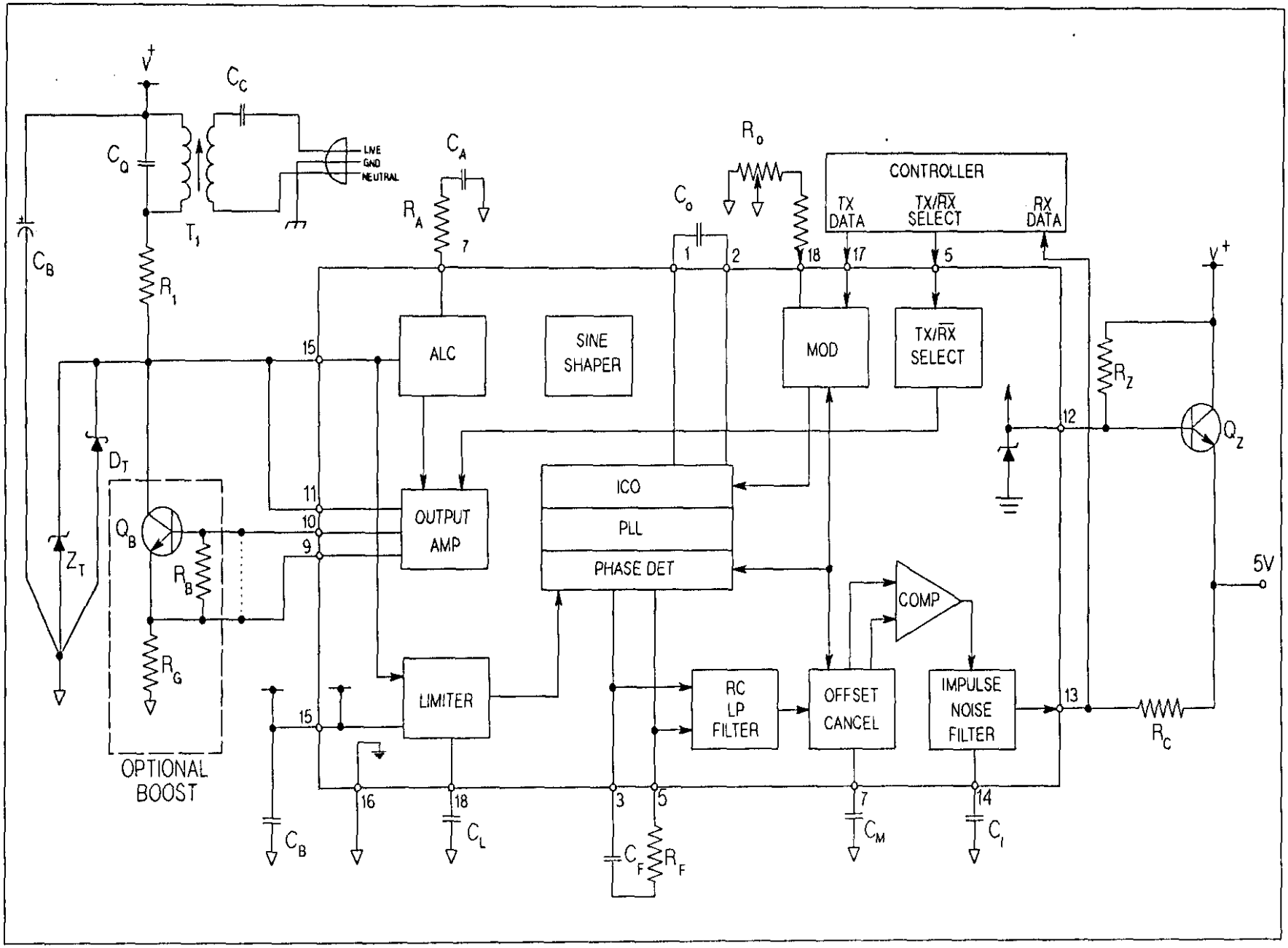


FIGURE 11 - BLOCK DIAGRAM OF THE CARRIER-CURRENT TRANSCEIVER

3.3.2.1 Operation.

Refer to Figure 11. The controller may select either the transmit (Tx) or the receive (Rx) mode of operation. Serial data is used to generate a FSK-modulated 50 - 300 kHz carrier on the line in the transmit mode. In the receive mode, line signal passes through the coupling transformer onto the phase-locked loop based receiver. The recreated bit stream drives the controller.

With the component in the transmit mode (pin 5 a logic high), baseband to 5 kHz drives the modulator's Data In pin to generate a switched 0.9781/1.0221 control current to drive the low temperature coefficient, triangle-wave, current-controlled oscillator to $\pm$ 2 % deviation. The tri-wave passes through a differential attenuator and sine shaper which deliver a current sinusoid through an automatic level control (ALC) circuit to the gain of 200. Drive current from the Carrier I/O develops a voltage swing on the coupling circuit which superimposes the signal on the power line. When large line impedances threaten to allow excessive output swing on pin 10, the automatic level control shunts current away from the output amplifier, holding the voltage swing constant and within the amplifiers compliance limit. The amplifier is therefore stable with a load of any magnitude or phase angle.

In the receive mode (pin 5 a logic low), the transmit sections on the Carrier-Current Transceiver are disabled. Carrier signal, broad-band noise, transient spikes, and power line component impinge on the receivers coupling circuit producing a voltage swing about the positive supply to drive the Carrier I/O receiver input. The balanced Norton-input limiter

amplifier removes DC offsets, attenuates line frequency, performs as a bandpass filter, and limits the signal to drive the phase-locked loop phase detector differentially. The differential demodulated output signal from the phase detector, containing AC and DC data signal, noise, system dc offsets, and a large twice-the-carrier-frequency component passes through a 3-stage RC lowpass filter to drive the offset cancel circuit differentially. The offset cancelling circuit works by insuring that the (fixed) ± 50 mV signal delivered to the data squaring ("slicing") comparator is centered around the comparator switch point. Whenever the comparator signal plus DC offset and noise moves outside the carefully matched ± 50 mV voltage "window" of the offset cancel circuit, it adjusts it's DC correction voltage in series with the differential signal to force the signal back to into the window. While the signal is within the ± 50 mV window, the DC offset is stored on capacitor CM. By grace of the highly non-linear offset hold capacitor charging during offset cancelling, the DC cancellation is done much more quickly than with an AC coupling capacitor normally used in place of the offset cancel circuit. Since impulse noise spikes normally ring the signal symmetrically around 0 V, the fully bilateral offset cancel topology affords excellent noise rejection. The switched current output of the comparator drives the impulse noise filter integrator capacitor that rejects all data pulses of less than the integrator charge time. Noise appears as duty-cycle jitter at the open collector serial data output.

3.3.2.2 Component Selection.

The external components in Figure 11 are determined in accordance with the selected design requirements. Table 1 illustrates how the component values effect the operation of the

COMPONENT	PURPOSE	EFFECT OF MAKING THE COMPONENT VALUE:	
		SMALLER	LARGER
C_O R_O	Together C_O and R_O set ICO F_O	Increases F_O Increases F_O < 5.6 k not recommended.	Decreases F_O Decreases F_O > 7.6 k not recommended
C_F R_F	PLL loop filter pole PLL loop filter zero	Less noise immune, higher F_{DATA}, more PLL stability PLL less stable, allows less C_F, less ringing.	More noise immune, lower F_{DATA}, less PLL stability PLL more stable, allows more C_F, more ringing.
C_C	Couples F_O to line, C_C and T_1 low-pass attenuates 50Hz.	Low Tx line amplitude, less 50 Hz T_1 current, less stored charge.	Drives lower line Z, more 50 Hz T_1 current, more stored charge.
C_Q T_1	Tank matches line Z, bandpass filters, isolates from line, and attenuates transients.	Tank F_O up or increase L of T_1 for constant F_O. smaller L: higher F_O or increase C_C, decreased F_O line pull.	Tank F_O down or decrease L of T_1 for constant F_O. larger L: lower F_O or decrease C_C, increased F_O Line pull.
C_A R_A	ALC Pole ALC Zero	Noise spikes turn ALC off. Less stable ALC.	Slower ALC response. More stable ALC.
C_L	Limiter 50 kHz pole, 50 Hz rejection.	Higher pole F, more 50 Hz reject. F_O attenuation.	Lower pole F, less 50 Hz reject, more noise BW.
C_M	Holds RX path V_{OS}.	Less noise immune, shorter V_{OS} hold, faster V_{OS} aquisition, longer preamble.	More noise immune, longer V_{OS} hold, slower V_{OS} aquisition, longer preamble.
C_I	Rejects short pulses like impulse noise.	Less impulse reject, delay, more pulse jitter.	More impulse reject, delay, less pulse jitter.
R_C	Open-collector pull-up.	Less available sink current.	Less available source current.
R_Z	5.6 V Zener bais.	Larger shunt current, more chip dissipation.	Smaller shunt current, less V+ current draw.
Z_T R_T	Transient clamp. Transient limit.	Higher R_Z - excess peak V, Zener and chip damage Z_T, pull up V+.	Lower R_Z gives enhanced transient clamp. Costly. Excessive TX attenuation.
R_B Q_B R_G	Base bleed Boost gain device Current setting R	Faster, lower THD I_O. Excessive T_J and V_{SAT}. More I_O, need higher h_{fe}.	Inadequate turn-off speed. More rugged but costly. Less I_O, lower min. h_{fe}.
C_B	Supply bypass	Transients destroy chip.	Less supply spike

TABLE 1 – EXTERNAL COMPONENT DESCRIPTION

Carrier-Current Transceiver. The maxims kept in mind, based on electrical performance considerations are (1) the higher the carrier frequency the better, (2) the lower the maximum data rate the better, and (3) the more time and frequency filtering the better. Before the component values were selected the following values were decided upon:

125 KHz Carrier Center Frequency

4,8 kBaud (Maximum data rate)

18 V Supply Voltage

220 V Power Line Voltage

50 Hz Power Line Frequency

Central to the chips operation is the low temperature coefficient of the carrier frequency emitter-coupled oscillator. With the correct value for CO, the carrier frequency of the triangular-wave oscillator may vary from near DC to above 300 kHz. CO should be made above 10 pF so that parasitic capacitance is not dominant. Excessive or unbalanced common-mode-to-ground should also be avoided. A low temperature coefficient of capacitance, such as a monolithic NPO ceramic multilayer type, preserves a low TC of the carrier frequency. A value for CO of 560 pF was selected using Figure 12 which is a graphical representation of the following expression:

$$CO = \frac{70.6 \times 10}{Fo}$$

Resistor RO is used by the chip to generate a VBE/R related current that is multiplied by

2 to produce the 200 μA ICO control current that sets the carrier frequency. The value of RO should be varied to trim the carrier frequency within limits. Raising Fo (carrier frequency) more than 20 % is not recommended. Low RO ,and the corresponding high control current, risks ICO saturation and a poor TC under worst conditions. Raising RO reduces the demodulated signal amplitude from the phase detector. Raising RO by more than a factor of 2 (1 octave) is not recommended. A maximum resistance of 7.6 K Ω was decided upon comprising of a 2 K Ω potentiometer and a fixed 5.6 K Ω resistor. This arrangement permits carrier frequencies between 105 kHz and 145 kHz.

Components CA and RA control the dynamic characteristics of the transmitter output envelope. Their values are not critical. CA and RA are functions of the loaded T1 tank Q, RO, fDATA, and line impulse noise. CA and RA values should be based on empirical measurements of the circuit on the line. Basically CA acts as an ALC pole while RA acts as an ALC zero. Values of 0.1 μF and 10 K Ω were selected for CA and RA respectively.

The boost gain transistor QB is required to operate at a high speed. Slow transistors do not preserve a sinusoidal waveform when the carrier frequency is high or will cause the output amplifier to oscillate. QB must have a certain minimum HFE for given boost levels.

The base bleed resistor RB turns the transistor QB off rapidly, which is necessary because the amplifier output swing is approximately 200V/μs. Values for RB below 24 Ω are not recommended as they will conduct excessive current and overload the chips amplifier.

Resistor RG in parallel with the internal 10 Ω resistor, fixes the current gain of the output amplifier thereby fixing the output current amplitude.

Although the boost circuit is not implemented in this particular application, it will be required if the system is expected to operate effectively over long distances and over a wide range of power lines. Likely values for RB and RG would be 180 Ω and 1.1 Ω respectively.

In this application the coupling transformer T1 should be optimised for use in the frequency range of 100 - 200 kHz with an unloaded Q factor of around 35, and a loaded Q factor of about 12. For versatility the secondary may have more than one secondary tap to drive industrial and residential power line impedances. The design of the transformer is described in detail in the Mains Interface Section 3.3.1.4.

The tank resonant frequency FQ must be correct to allow passage of the transmitter signal to the line. Trimming FQ to equal the carrier frequency Fo is done with T1's trimming slug. Since circulating current in the tank is 250 mA (RMS), CQ should have a low series resistance. Polypropylene capacitors are recommended while "orange drop" mylars and polystyrene capacitors will suffice. Many other mylars may prove to be inadequate. A 200 volt rating is recommended for transient protection. The value of CQ, 33μF, was calculated in section 3.3.1.4 using the resonant capacitor formula. A polystyrene capacitor was used due to the unavailability of the Polypropylene and "orange drop" capacitors. Figure 13 illustrates the relationship between the resonating capacitance and the carrier frequency Fo.

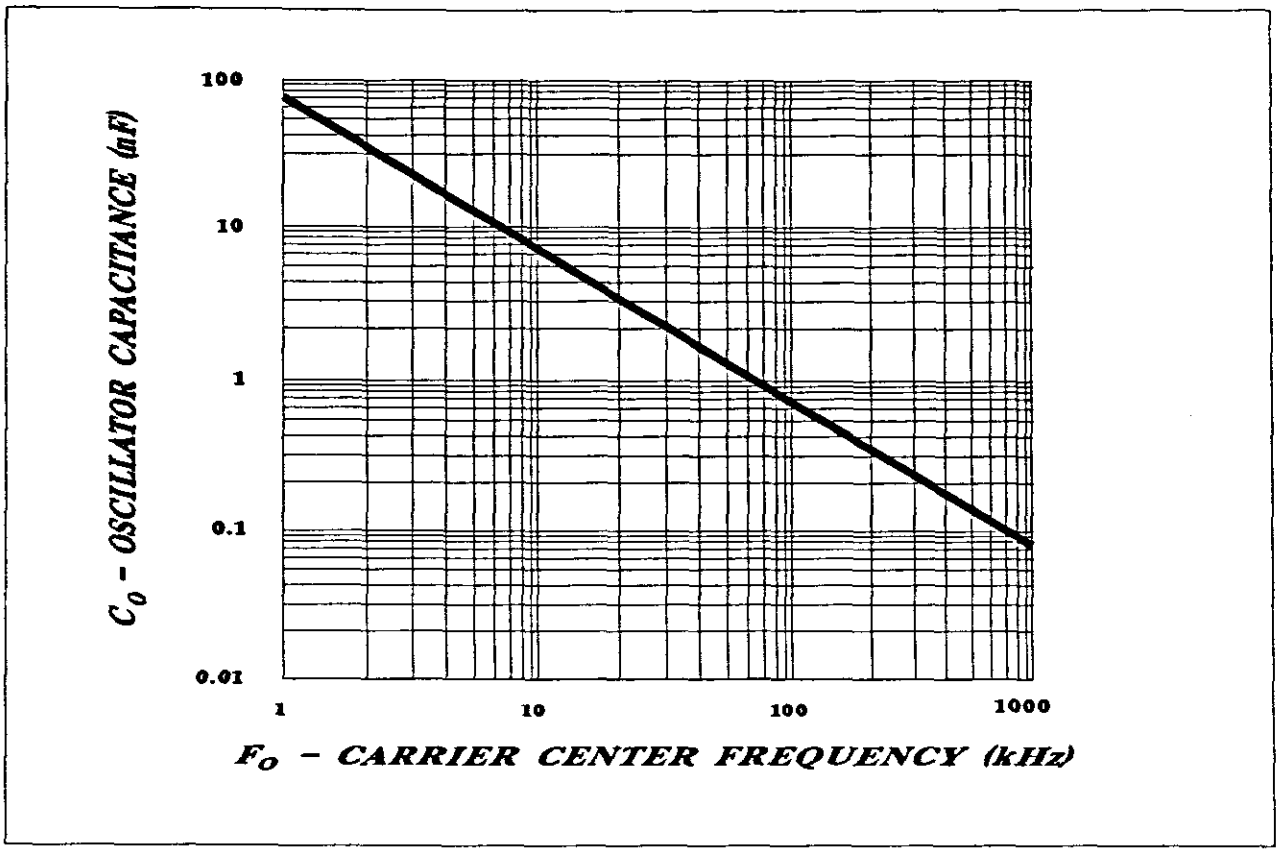


FIGURE 12

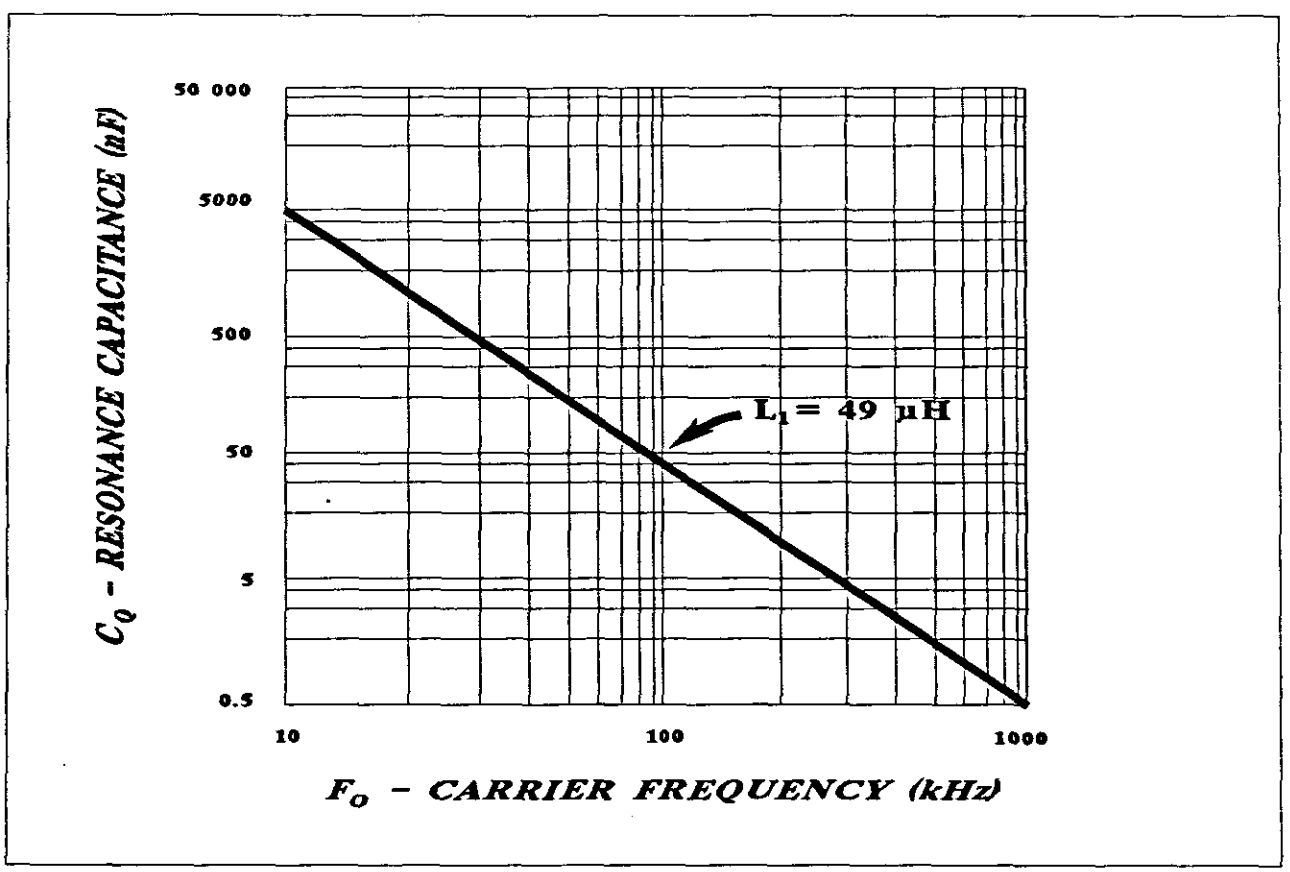


FIGURE 13

The coupling capacitor CC is included in the mains interface circuit to block the power line voltage from T1's line-side winding. In addition CC and the T1's line-side winding comprise a highpass filter. The self inductance of T1 is far to low to support a direct line connection. It is essential that CC has a low impedance at the carrier frequency to allow T1 to drive transmitted energy onto the line. To drive a 12 Ω power line the impedance of CC should be below 12 Ω. Figure 14 is used to select a capacitance that will yield the required inductance at the carrier frequency. Having selected an appropriate value for CC Figure 15, is used to check that the power line current is small enough to keep T1 well out of saturation.

To protect the Carrier-Current Transceiver from potentially damaging line transients or transients caused when stored line energy in CC is discharged by the random phase of power line connection and disconnection, a transient suppression diode, D1 is used. Refer to section 3.3.1.5 for a detailed description of the transient protection employed. The specifications for the recommended diode are as follows:

44 - 49 V Breakdown Voltage @ 1mA

1 μA Minimum Leakage @ 40 V

300 pF Capacitance @ BV

64.5 V Maximum Clamp Voltage @ 7.8 A

10 KW Peak Non-Repetitive Pulse Power for 1 μs

70 A Surge Current for 1/120 sec.

The resistor RT acts as a voltage divider with D1, absorbing transient energy that

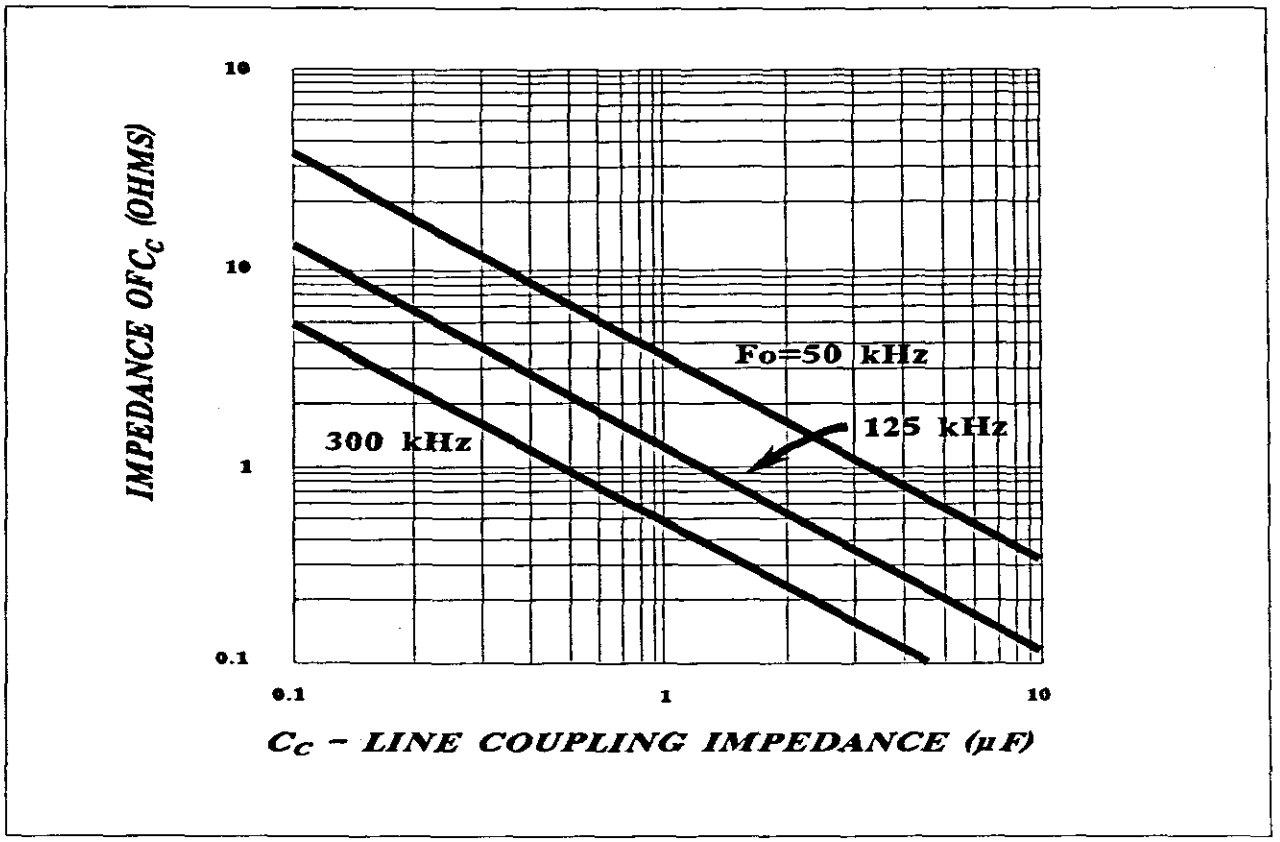


FIGURE 14

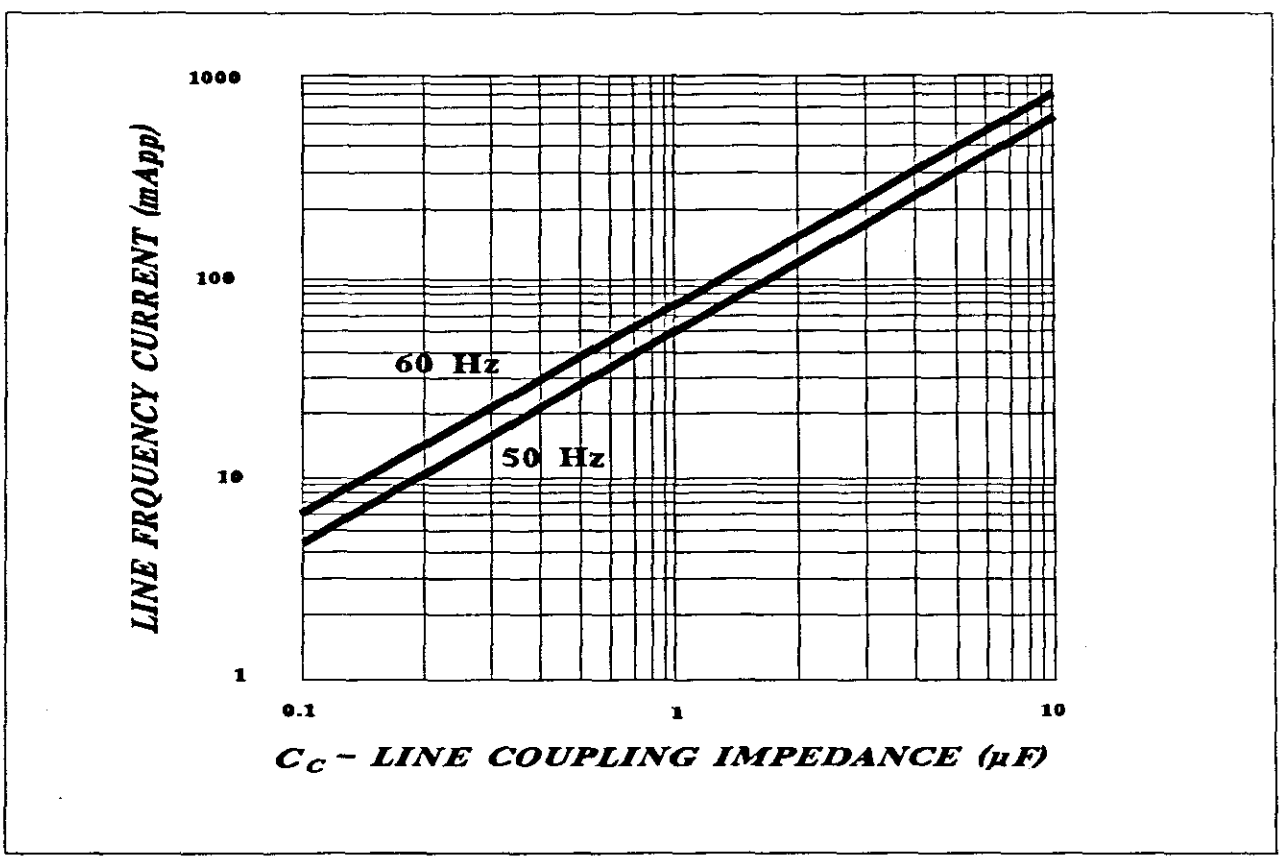


FIGURE 15

attempts to pull the carrier above 44 volts.The resistor used is a 4.7 Ω, 1/4 watt, carbon composition resistor.

The Norton input limiter amplifier has a bandpass filter for enhanced receiver selectivity, noise immunity, and line frequency rejection. The nominal response curve for Fo = 50 kHz is shown in Figure 16. The 300 kHz pole is fixed while the 50 kHz pole is set by capacitor CL. A suitable value for CL is determined from the graph in Figure 17. After a value for CL is found, the resulting line frequency attenuation for the bandpass filter is determined from Figure 18. A value of 0.047 μF was selected for CL which is 33 % larger than the nominal value.

The phase-locked loop (PLL) filter components, capacitor CF and resistor RF remove some of the noise and most of the 2Fo components present in the demodulated differential output voltage signal from the phase detector. They influence the PLL capture range, loop bandwidth, damping, and capture time. Because the PLL has an inherent loop pole due to the integrator action of the ICO (via Co), the loop pole set by CF and the zero set by RF gives the filter a classical 2nd-order response. PLL stability and response speed are traded off to find the most suitable combination for a particular application. Large values for CF combined with too small an RF value cause PLL loop instability which leads to poor capture range and poor step response or oscillation.

Calculation of CF and RF is relatively complex, involving not only the 2nd-order loop step response, but also the PLL non-dominant poles, the tuned transformer stepped-frequency response, and the RC lowpass step response (for data rates approaching 1 kHz). Therefore CF

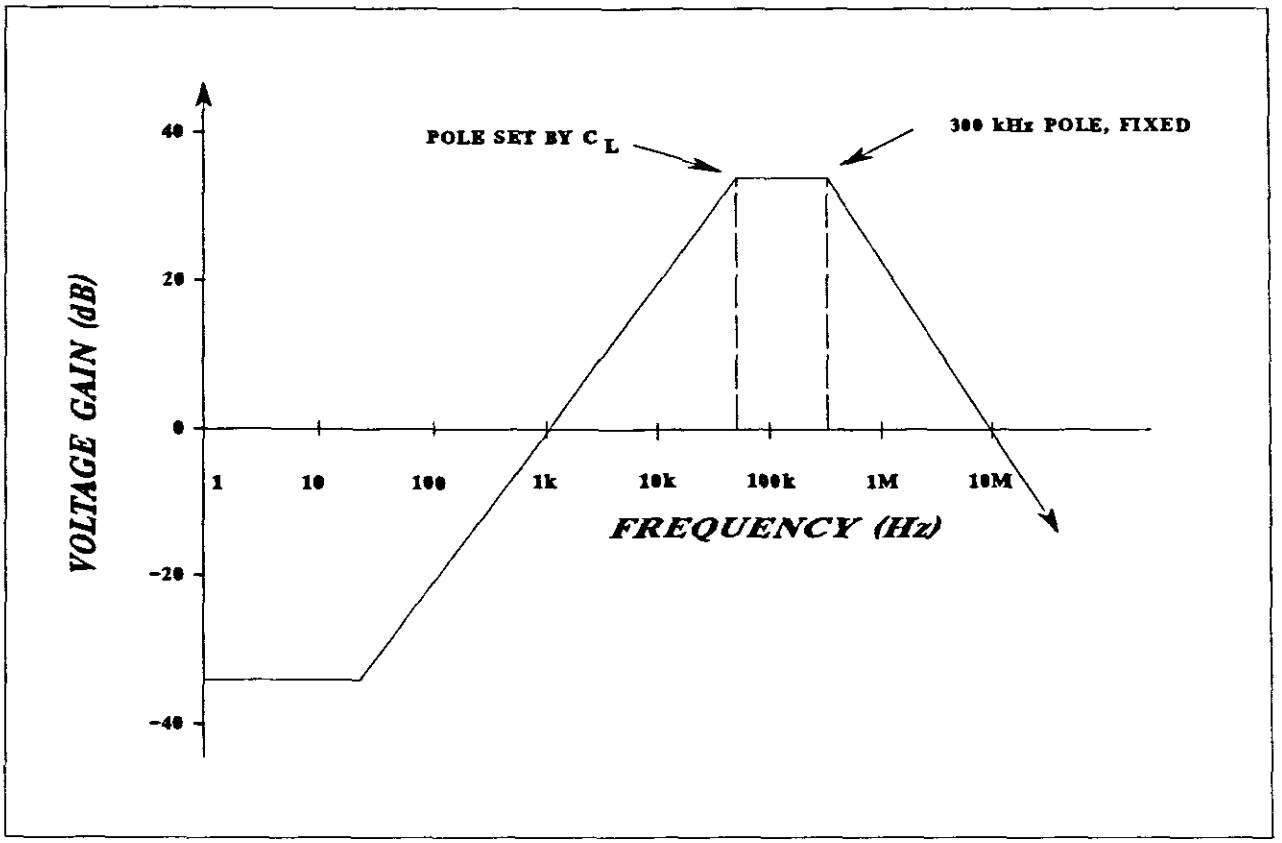


FIGURE 16

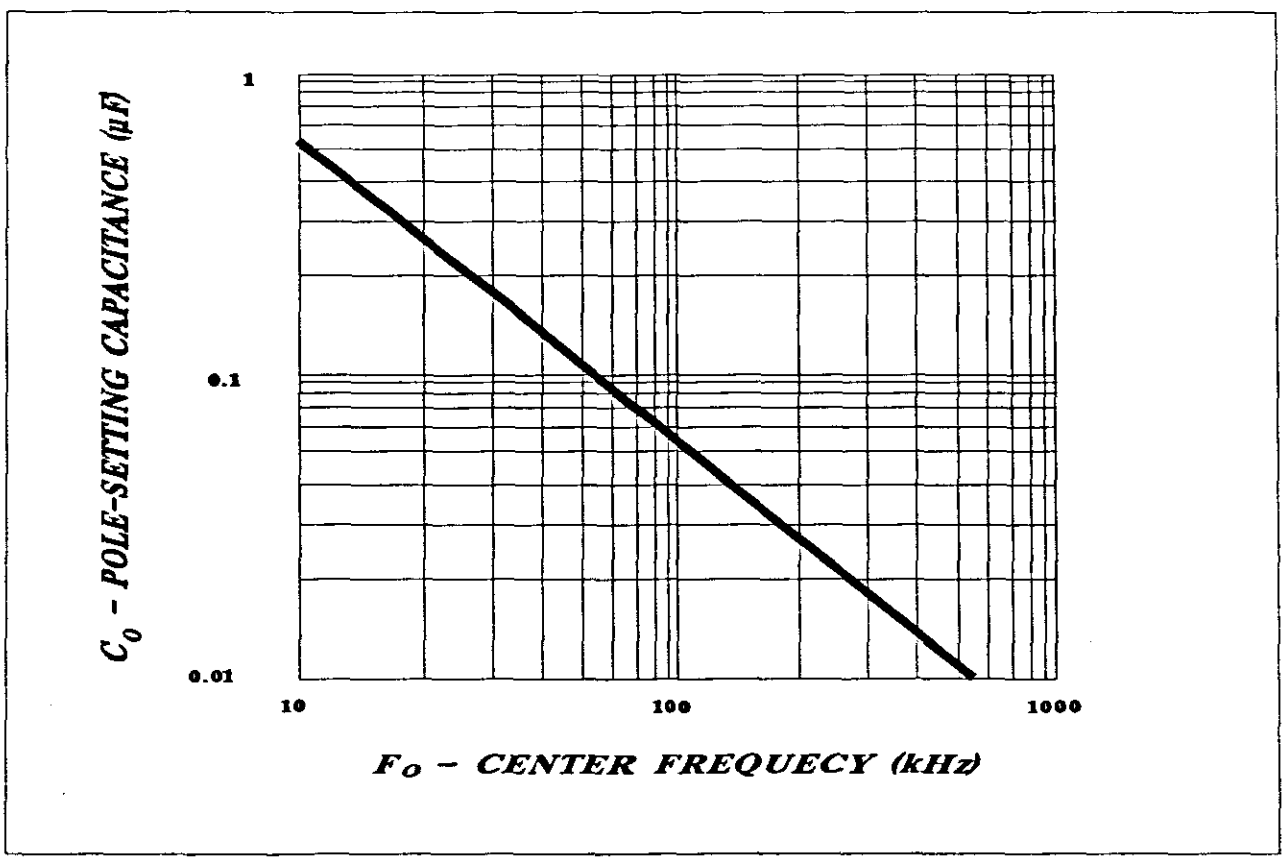


FIGURE 17

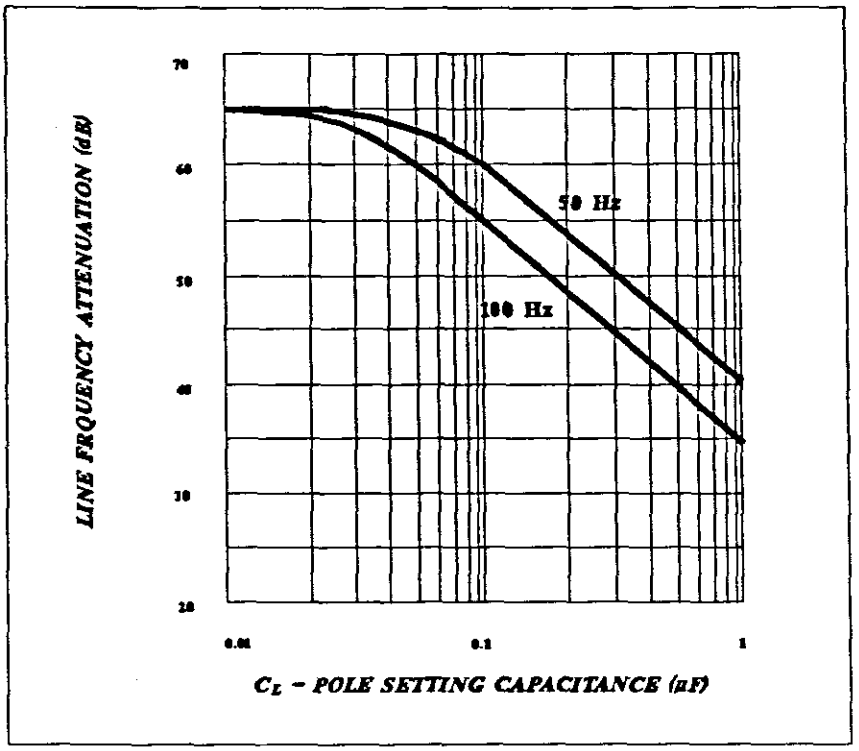


FIGURE 18

and RF are best found empirically. The component values are selected to give the best possible impulse noise rejection while preserving a 20 % capture range and a wide stability margin. Figures 19 and 20 give CF and RF values verses carrier frequency. Values of 0.047 μF and 3.3 K Ω were selected for CF and RF respectively.

Capacitor CM stores a voltage corresponding to a correction voltage required to cancel the phase detector differential output DC offsets. The stored value is 5/6 of the DC offset plus some bias level of about 2.2 volts. A large CM value increases the time required to bias-up the receive path at the beginning of transmission. A large CM filters well and stores the bias voltage for a longer period. Due to the initial random charge of CM, the receiver must be given a data transition to charge to the correct bias voltage. It is therefore not recommended

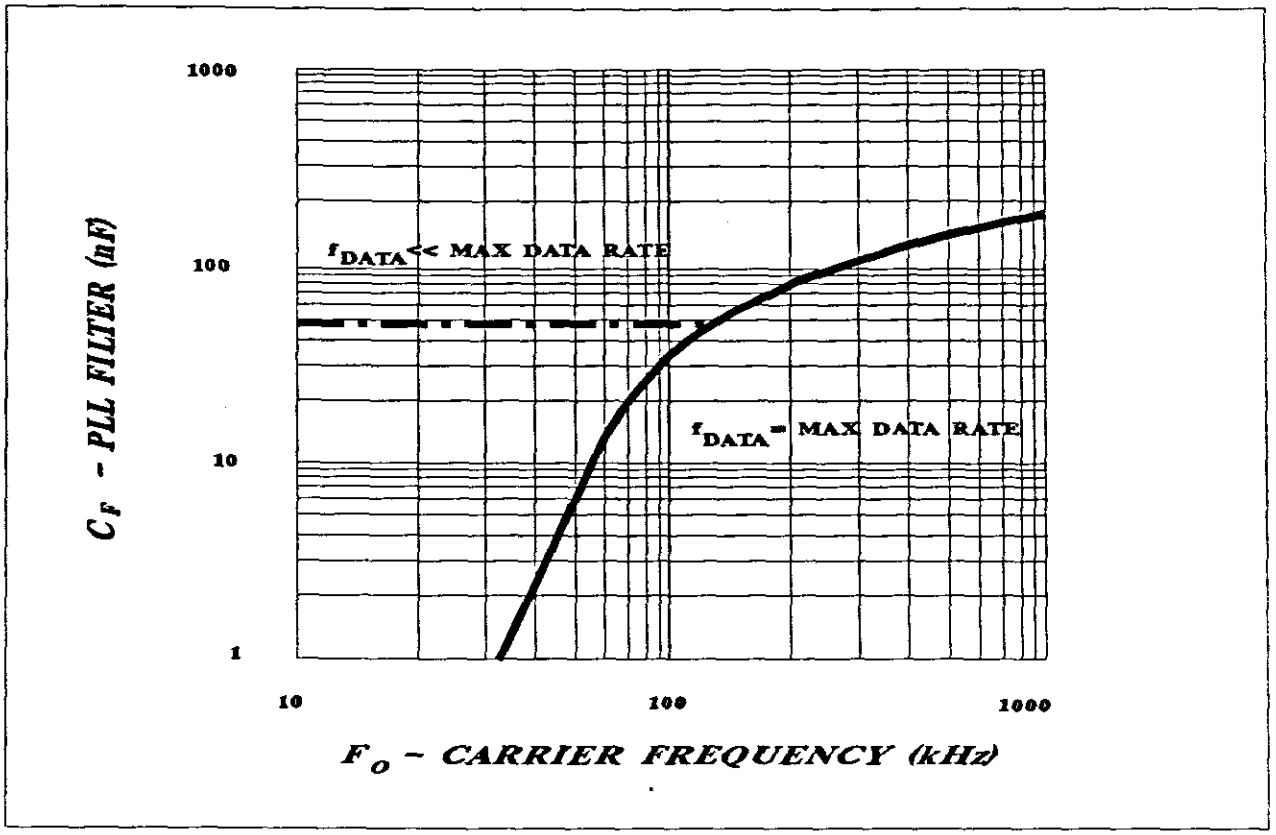


FIGURE 19

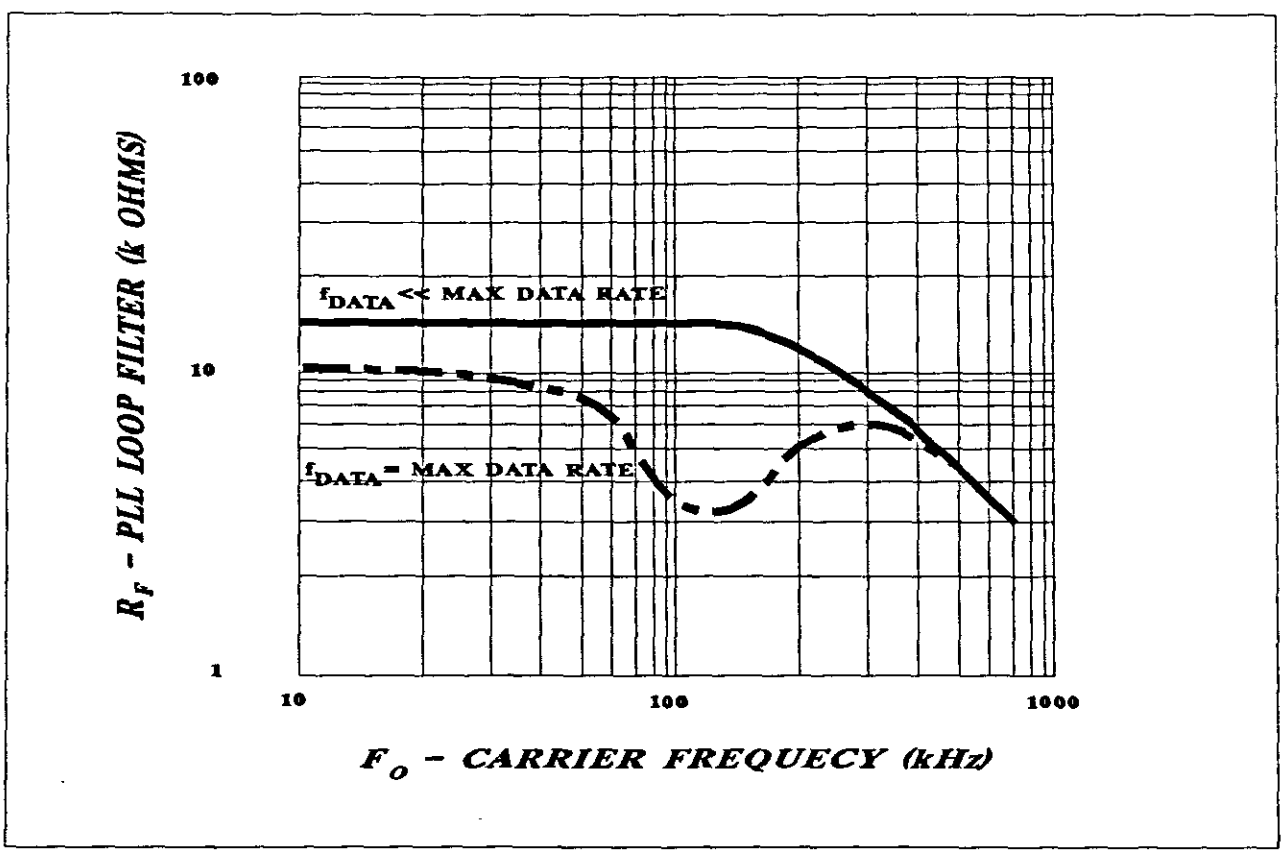


FIGURE 20

to reduce CM's value to the extent that the capacitor is charged in less than 2-bit times. Figure 21 illustrates how the value of CM may be determined observing the 2-bit charge time. A value of 0.47 μF was selected for CM.

The impulse noise filter integrator capacitor CI is used to prevent pulses, shorter than the integrator charge time, from passing through the impulse noise filter. A charge time, set to a nominal ½ bit time, is required for a $\pm$ 50 μA charge current to swing CI over a 2VBE range. The charge time in the worst case scenario, should never exceed one bit time as this would inhibit the passage of data. Figure 22 was used to find the value of 0.047 μF for CI at the specified carrier frequency.

The collector pull-up resistor RC is sized to supply sufficient pull-up current drive and speed while preserving adequate output low current drive.

The 5.1 volt silicon zener diode ZA is required when a short RX-to-TX switch-over time is desired while the chip is operating in the receive mode with a pin 10 input signal swing approaching or exceeding twice the supply voltage. Predominant causes of these large swings impinging on the receiver's supply are: (1) transmitter supply voltage higher than the receiver's supply voltage, (2) a TX and RX pair that are electrically close, or (3) a higher RX T1 step-up turns ratio than the TX T1 step-down ratio.

3.3.2.3 Tuning Procedure.

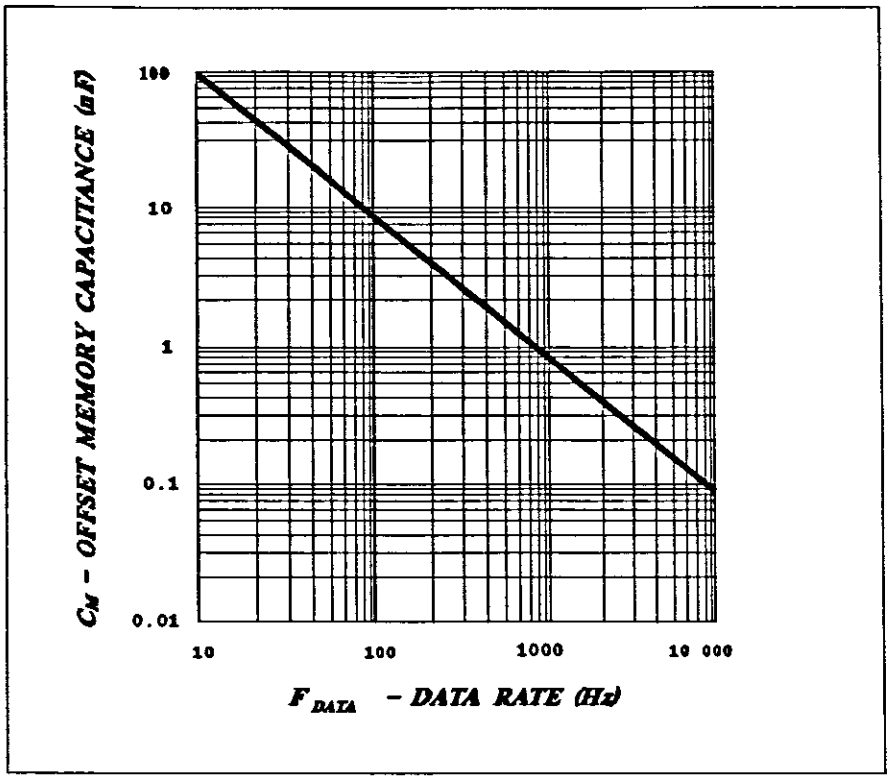


FIGURE 21

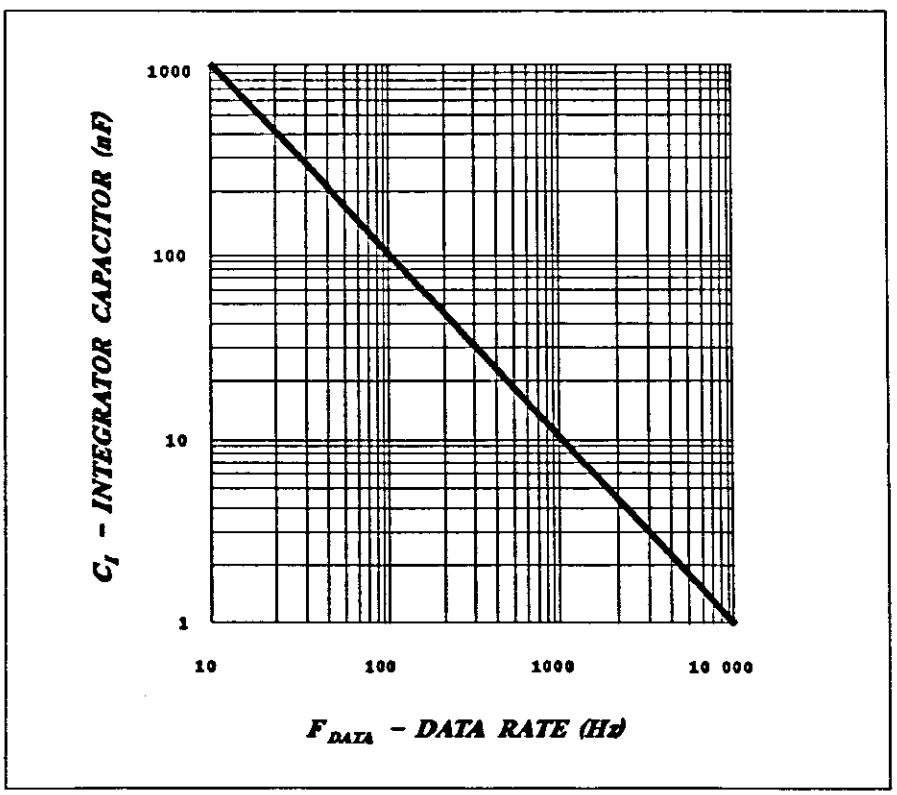


FIGURE 22

First, the carrier frequency is trimmed by placing the Carrier-Current Transceiver in the transmit mode, setting a logical high data input, and measuring the transmit high frequency on the Carrier I/O pin in accordance with the following steps: (1) place a logic low on pin 19, (2) place a logic high on pin 6, (3) place a frequency counter on pin 11, (4) adjust resistor Ro on pin 18 until the measured frequency is 1.022 Fo. This adjustment will result in a 2.2 % frequency deviation above and below the selected carrier frequency. The selected carrier frequency of 125 kHz therefore gave a measured frequency of 127,750 kHz. Conversely when a logic high was placed on the data input, pin 6, a measured frequency of 122.3 kHz (1/1.022 Fo) was observed.

Second, the line transformer is tuned. The Carrier-Current Transceiver is placed in the transmit mode and a resistive line load is connected to disable the Automatic Gain Control (AGC) by reducing the tank voltage swing below it's limit. FSK data is then passed through the tank allowing for adjustment of the tank envelope to ensure that the high and low data frequency amplitude is of equal magnitude. This procedure is detailed as follows: (1) place a logic low on pin 5, (2) place a logic level, square wave at or below the receivers maximum data rate on pin 17, (3) temporarily place a 330 Ω resistor across the tank, (4) place an oscilloscope on pin 10, (5) adjust the transformer slug until the envelope modulation is minimised. An alternative for the 330 Ω resistive load, is the use of a passive network which represents the average line impedance.

3.3.2.4 Thermal Considerations.

It is desirable to place the largest possible signal on the power line for maximum range, limited only by the Carrier-Current Transceiver's power dissipation and maximum junction temperature Tj. The declining output power at elevated Tj allows a more optimal power output i.e. high power at low Tj and lower power at high Tj for chip self-protection. However the maximum Tj may still be exceeded within the ambient temperature limit, TA, under worst conditions of 100 % transmit duty-cycle, high supply, shorted load, poor PC board layout, and an above nominal current part. Under these conditions, a part may dissipate 2140 mW, reaching a Tj of 170 degrees Centigrade.

A direct method of measuring the operating junction temperature is to measure the VBE voltage on pin 18, which is always available under all operation modes. The graph of Figure 23 is used to determine Tj, knowing VBE at the operating point in question and VBE at TA =

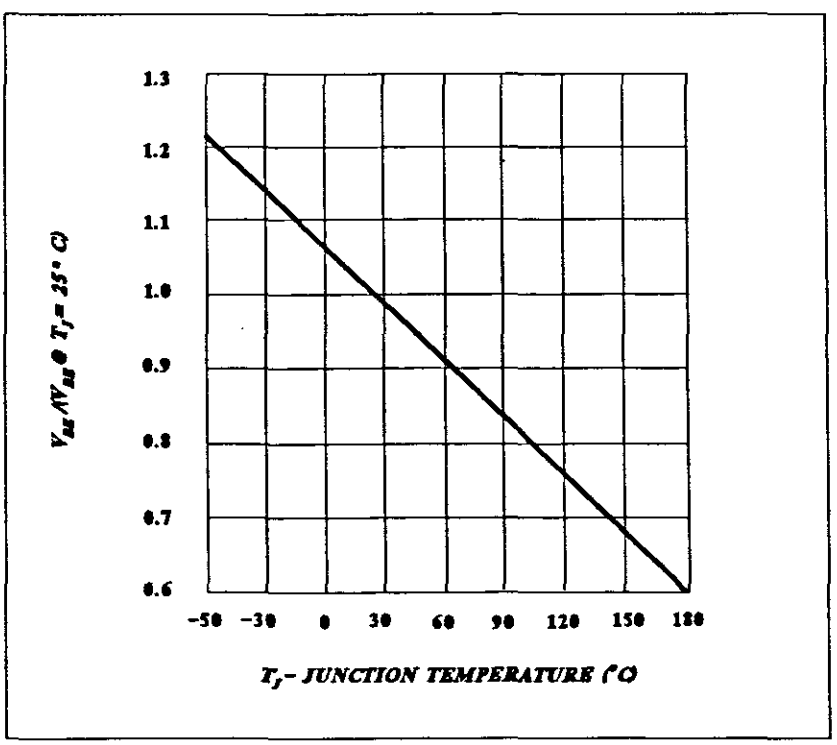


FIGURE 23

25° C. VBE is found by powering up the chip that has been dissipating zero power at some ambient temperature for some time and measuring VBE in less than 1 second. Alternatively, Tj may be calculated using the following expression:

$$Tj = TA + \Theta JA \times PD$$

where ΘJA is 75° C/W for the plastic (N) package using a socket.

3.3.2.5 Transmit/Receive Switch-Over Time.

An important figure-of-merit for a half-duplex CCT link, influencing effective data rate, is the transmit-to-receive switch over time TTR. Using the selected component values, a nominal 2 bit-time (1 bit-time = 1/[2fDATA]) is achieved over a wide range of operating conditions, where the receiver requires 1 data transition. TTR cannot be decreased significantly but does increase as noise filtering, especially via CM, is increased. Impulse noise on switching, signals near the limiting sensitivity, poor carrier frequency match between the receiver and transmitter caused by poor trim or worst case conditions, and the statistical nature of phase-locked loop signal acquisition may all contribute to the increase in transmit-to-receive switch-over time up to as much as 4 bit-times. In the receive mode the DC operating points are stored on CM and CF while in the transmit mode, under noisy worst case conditions , CM will discharge to the point of false operation after 35 bit-times.

The major components of the transmit-to-receive switch-over for Carrier-Current

Transceivers with a nominal 125 kHz carrier frequency, 360 Baud data rate and a coupling transformer Q factor of 20 are described in following example.

Assume that the remote circuit is operating in the transmit mode with a 26.6 Vpp tank swing and is selected as a receiver. First, the tank stored energy at the transmit frequency must decay to a level below 2.8 mVpp swing which is caused by the 0.14 mVpp incoming line signal containing the information to be received.

$$\text{decay time} = \frac{Q}{\pi Fo} \ln \left[\frac{V1}{Vo}\right]$$

$$= \frac{20}{\pi \times 125\ 000} \ln \left[\frac{26.6}{0.0028}\right] = 0.466 \text{ ms}$$

Second, the phase-locked loop must acquire the signal, lock and settle. The average acquisition time depends on the loop filter components CF and RF and the difference in center frequencies of the RX and TX pair. Using the selected CF and RF vales of 47nF and 6.2 K Ω with a 4.4 % deviation the lock time is less than 50 cycles of Fo i.e. 0.4 ms. Acquisition is incomplete until the second order PLL settles. For the selected CF and RF values, the loop natural frequency FN and the damping factor are 2.3 kHz and 1.0 respectively. Settling to within ± 25 mV of the 100 mV DC offset change requires 2.7 periods of FN or 1.2 ms.

Third, the RC lowpass filter introduces a 0.12 ms delay.

Fourth, CM must charge up to ± (5/6) 100mV = 83mV depending on the polarity of

Fo. Borderline data squaring with zero noise immunity is possible with only ± 50 mV of charging. CM charge current is an asymptotic function approximated by assuming a 50 μA charge current and the full 83 mV charge voltage. CM charge time is then 1.7 ms.

Finally, the impulse noise filter adds 1½ bit-time delay. The total transmit-to-receive time is 3.9 ms plus a ½ bit-time for a total of 1.9 bit-times at 360 Baud.

The receive-to-transmit switch-over time may be explained assuming that the transceiver is in the receive mode and the transmit mode is selected. In less than 10 μs, full output is exponentially building up a tank swing. 50 % of full swing is achieved in less than 10 cycles or 80 μs at 125 kHz. During the same 10 μs the output amplifier and the modulator input are activated while the phase detector and loop filter are disconnected. FSK modulation is produced within 10 μs after switching to the transmit mode.

3.3.2.6 Audio Transmission.

The Carrier-Current Transceiver is capable of analog data transmission and reception. Base-band audio-bandwidth signals FM modulate the carrier passing through the tuned transformer (placing a limit on the usable percent modulation) onto the power line to be linearly demodulated by the receiver PLL. Because the receiver data path beyond the phase detector permits the passage of digital signals only, external audio filtering and amplification is required. Filter bandwidth is held to a minimum to minimise noise, especially line-related noise.

3.3.2.7 Data Communication and System Protocols.

The protocols inherent in data transmission are communication and system protocols.

Communication protocol refers to the software method of encoding data that remains constant for every transmission in a system. It's first purpose is to convert data into a baseband digital form that is more easily recognised as a real message at the receive end. Secondly, it incorporates encoding techniques to ensure that noise induced errors do not easily occur. Lastly, the software algorithms used on the receive end for decoding of the incoming data, prevent the reception of noise induced "phantom" messages, and to insure that the real messages are recovered from an incoming bit steam that has been altered by noise.

System protocol refers to the manner in which messages are coordinated between nodes in a system. It's first purpose is to ensure message retransmission to correct errors (hand-shake). Secondly, it co-ordinates messages for maximum utilisation and efficiency on the network. Lastly, it ensures that message collision is avoided. Common system protocols include master-slave, carrier detect multiple access, and token passing. Token passing and master slave are generally preferred as they are inherently collision free.

Both protocols usually reside as software in the microcontroller connected to the transceiver. The difficulty in designing special protocols arises from the nature of the AC line, an environment laden with the worst imaginable noise conditions. The relatively low data rates possible over the power line (typically less than 9600 Baud) make it even more imperative that

the system utilise the most efficient means available to ensure network efficiency.

3.3.2.8 Data Encoding.

At the beginning of a received data transmission, the first 0 to 2 bits may be lost while the chip's receiver settles to the DC bias point required for the given transmitter/receiver pair carrier frequency offset. With the proper data encoding, dropped start bits can be tolerated and correct communication can take place. An example of an elementary coding scheme is discussed in the following paragraph.

Generally, a circuit system consists of many transceivers that monitor the line at all times (or during predetermined time windows), waiting for a transmission directed to them. If a receiver detects it's address in the transmitted data packet, further action such as handshaking with the transmitter is initiated. The receiver may indicate to the transmitter, via retransmission, that the data was received satisfactorily and is waiting for acknowledgement before acting on the received data. Error detecting and correcting codes may be employed throughout. The transmitter must have the capability to retransmit after a time if no response is received from the receiver-under the assumption that the receiver did not detect it's address because of noise, or that the response was lost due to noise or a line collision. A line collision occurs when more than one transmitter operates at once, causing one or more of the communications to fail. After many re-transmissions the transmitter might choose to abandon the attempt. Collision recovery is achieved by waiting some variable amount of time before attempting retransmission again, using a random number of bits delay or a delay based on each

transmitter's address.

An example of a simple data transmission packet is illustrated in Figure 24. The 8 bit 50 % duty- cycle preamble is long enough to allow receiver biasing with sufficient bits remaining to allow the receiver controller to detect the square-wave signalling the start of transmission. On detection of the alternating-polarity data square-wave the controller uses the synchronisation bit to signal that the address and the data is to follow immediately. The address data would then be loaded, assuming the fixed format, and tested against it's own address. If the two addresses correlate, the receiver would then load and store the data, if however the addresses are not identical, either, the data was not meant for the receiver or noise had corrupted the address. In the former case the controller should return immediately to monitoring the line for it's address. If the latter case were true, the controller would continue to detect edges, tying itself up by loading false data and being forced to handshake. The square-wave detection and address load and check routines should be fast to minimise the time spent in loops after being falsely triggered by noise. If the controller detects an error it should immediately resume the monitoring of the Data Out pin for transmissions with the next bit being shifted in and the process repeated.

A line synchronous circuit system passing 3 bits per half cycle may replace the long 8 bit preamble and synchronous pulse with a 2 bit start-of-transmission bias preamble. The receive controller might then assume that the preamble always starts after bit 1 i.e. any data transition at a zero crossing indicates the start of the address bits.

The examples discussed above assumed that the controller is always aware of the status of the Data Out pin. The controller must sample this pin at the correct time to monitor the Data Out state. Since noise is interpreted as pulse width jitter, symmetrically placed about the no-noise switch points, optimum Data Out sampling is done in the center of the received data pulse. The receive data path has a time delay that, at low data rates, is dominated by the impulse noise filter integrator and is normally ½ bit. At a 2 kHz data rate, an additional delay of approximately 1/10 bit is added due to cumulative delay of the remainder of the receiver. Figure 25 illustrates how the Data Out sampling occurs conveniently on the transmitted data edges for the line synchronous data transmission scheme discussed in the previous paragraph. With the asynchronous system discussed, the receive controller must sample the Data Out pin frequently to determine, with several bits of accuracy, where the square-wave data transitions take place, average their positions assuming a known data rate, and calculate where the center of the bits are and will continue to be as the address and data is read.

3.3.3 Address Encoder/Decoder.

The MM53200 Encoder/decoder is a MOS/LSI Digital Code Transmitter - Receiver system. This component contains both the Encoder and Decoder. Figure 26 illustrates how the MM53200 is connected in the transmit and receive modes of operation. Oscillator stability is not critical and therefore 5 % components may be used. Cross interference of the receivers in close proximity is virtually eliminated by circuitry requiring 4 valid words to be received, each within 64 ms of the other.

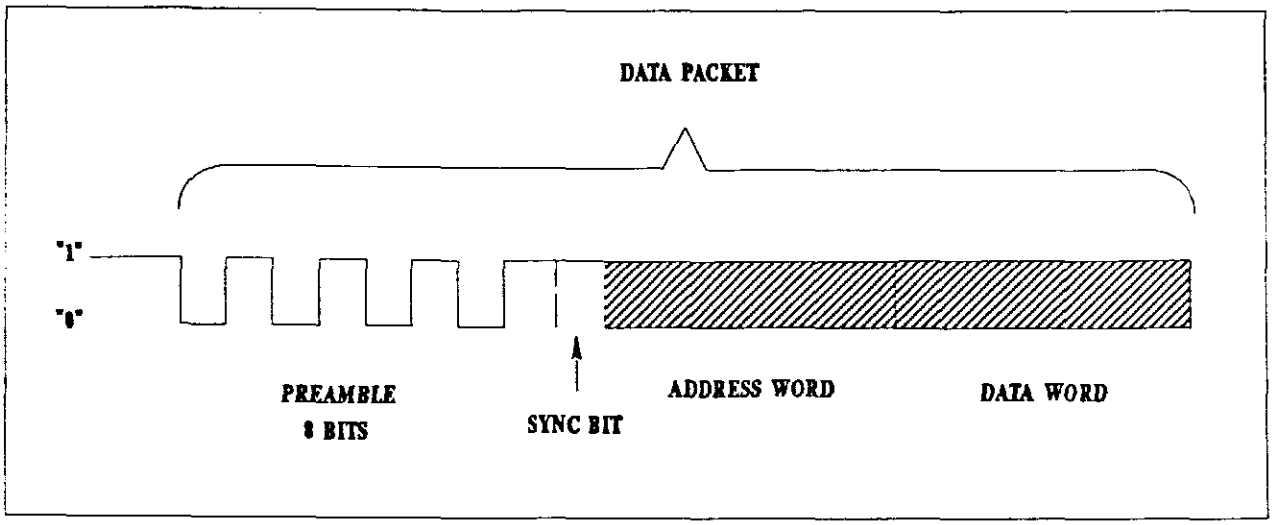
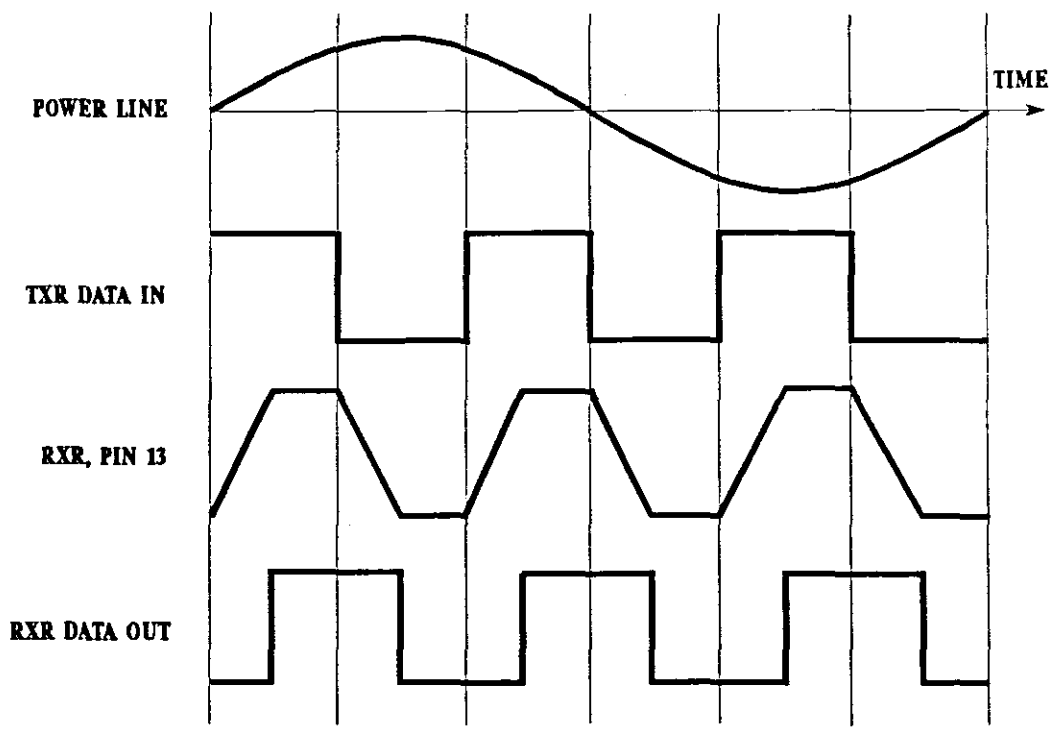


FIGURE 24



OPERATING WAVEFORMS OF A LINE-SYNCHRONISED TRANSCEIVER PAIR

FIGURE 25

In the transmit mode the twelve inputs are scanned sequentially producing the output pattern shown in Figure 27. This code is generated at the rate of 0.96 ms/bit, or 11.52 ms/word with a 11.52ms reset pulse between words.

In the receiver mode, the incoming signal is compared to the local code in a sequential manner. Should there be an error, the system is reset and begins it's comparison on the next pulse. If all twelve bits are received correctly, a "valid" signal is generated. This signal clears a 64 ms counter and clocks a 3 stage counter. The 3 stage counter counts the "valid" pulses and after 4 pulses have been received, the transmit/receive output is enabled. The next "valid" pulse must be received within 128 ms, giving a one in 6 valid requirement to keep the transmit/receive output low. Noteworthy characteristics are:

7 - 11 V Supply Voltage

12 mA Maximum Supply Current

3.3.4 RS-232 Interface.

As discussed in section 3.2.5, the controller is equipped with an RS-232 interface and it is therefore not necessary for the local transceiver to duplicate this facility. An additional RS-232 interface is however required on the remote transceiver to which an external device may be connected when operating in the Half-Duplex Mode. The interface used is identical to that used in the controller i.e. MAX232 driver/receiver. Refer to the above mentioned section for specifications and features pertaining to the MAX232.

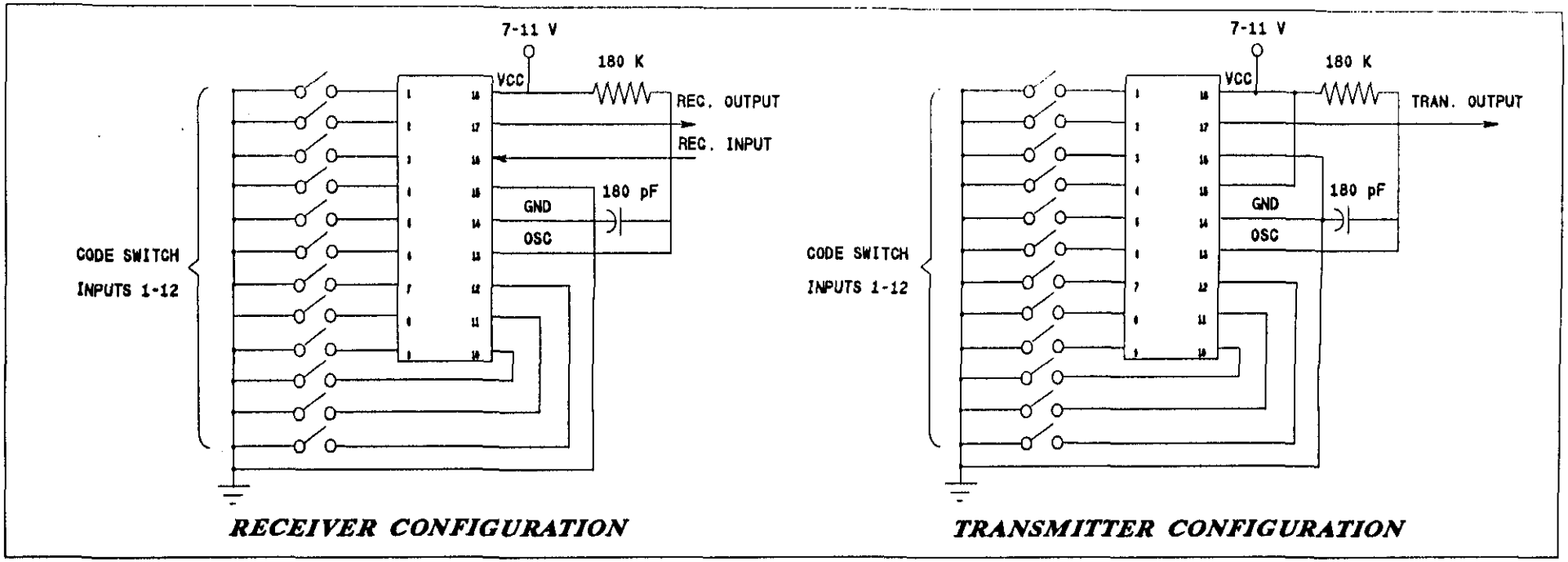


FIGURE 26

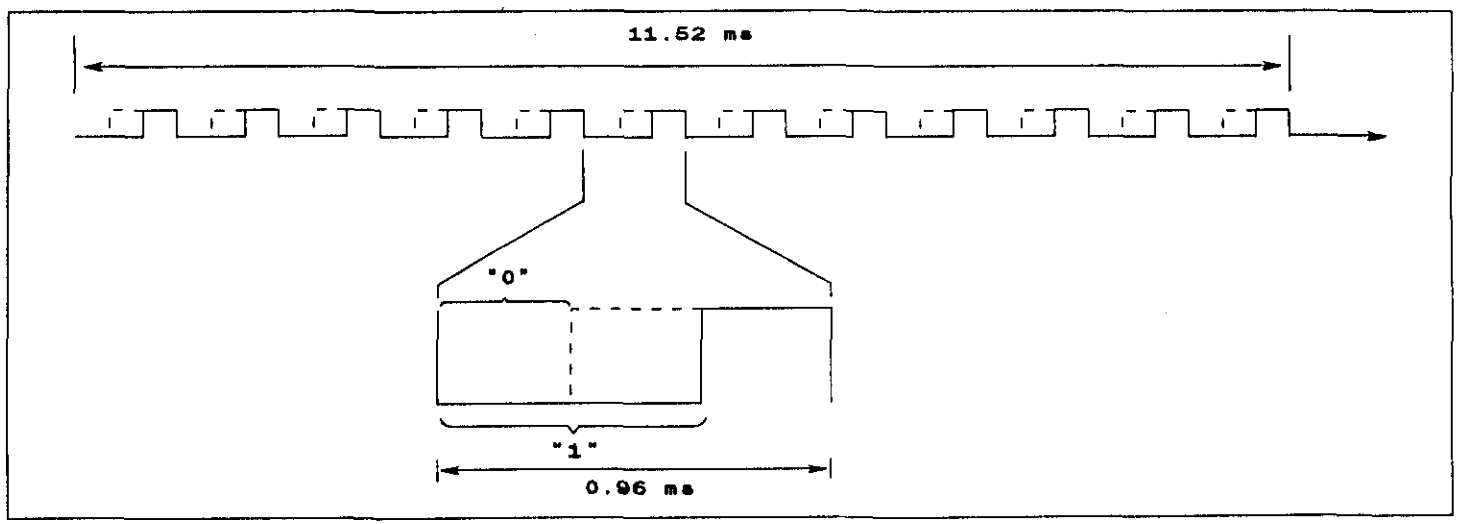


FIGURE 27

4. Software Development.

In the Remote Control Mode, the remote transceiver relies on commands emanating from the controller. Two programs were written to illustrate how the Remote Control System could be employed in both domestic and industrial applications. In the domestic application, remote electrical devices are switched on and off at predetermined times. In the industrial application, an immersion heater is switched at predetermined time intervals thereby controlling the temperature of the fluid. A disable facility is also included to enhance control. These programs are written in the extended BASIC language supported by the MCS BASIC-52 interpreter. Refer to section 4.4 and 4.5 for program listings and flowcharts.

4.1 MCS BASIC-52 Interpreter.

The 8052AH-BASIC has a complete full-featured basic interpreter, MCS BASIC-52, resident in the 8 K of available ROM. This product is specifically designed to address the needs of process control, measurement, and instrument applications. In addition to the standard BASIC commands and functions, the MCS BASIC-52 contains many unique features that enable the user to perform tasks that normally require assembler language. The MCS BASIC-52 is an interpreted language and enables the user to develop a program interactively without the cumbersome and repetitive process of editing, assembling, loading, and running which is required by other compilers.

The MCS BASIC-52 contains all standard BASIC commands, statements and operators.

Table 2 lists the software feature set of the MCS BASIC-52.

4.2 Stack Structure.

The MCS BASIC-52 reserves the first 512 bytes of external data memory to implement two "software" stacks. These are the control stack and the arithmetic or argument stack.

The control stack occupies locations 96 (60H) through 254 (0FEH) in external RAM memory. This memory is used to store all information associated with loop control (i.e. DO_WHILE, DO_UNTIL, and FOR_NEXT) and basic subroutines (GOSUB). The stack is initialised to 254 (0FEH) and "grows down".

The argument stack occupies locations 301 (12DH) through 510 (1FEH) in external RAM memory. This stack stores all constants that the MSC BASIC-52 has in use at a particular moment. Operations such as ADD, SUBTRACT, MULTIPLY, and DIVIDE always operate on the first two numbers on the argument stack and return the result to the same stack. The argument stack is initialised to 510 (1EFH) and "grows down" as more values are placed on the stack. Each floating point number placed on the argument stack requires 6 bytes of storage.

The stack pointer on the 8052AH (special function register, SP) is initialised to 77 (4DH). The 8052AH's internal stack pointer "grows up" as values are placed on the stack. The user has the option of placing the 8052AH's stack pointer anywhere (above location 77) in the

TABLE 2 - 8052AH SOFTWARE FEATURE SET

COMMANDS	STATEMENTS	OPERATORS
RUN	BAUD	ADD(+)
LIST	CALL	DIVIDE(/)
LIST#	CLEAR	EXPONENTIATION(**)
NEW	CLEARS	MULTIPLY(*)
NULL	CLEARI	SUBTRACT(-)
RAM	CLOCK0	LOGICAL AND(.AND.)
ROM	CLOCK1	LOGICAL OR(.OR.)
XFER	DATA	LOGICAL X-OR(.XOR.)
PROG	READ	LOGICAL NOT
PROG1	RESTORE	ABS ( )
FPROG	DIM	INT ( )
FPROG1	DO-WHILE	SGN ( )
FPROG2	DO-UNTIL	SQR ( )
	END	RND
	FOR-TO-NEXT	LOG ( )
	GOSUB	EXP ( )
	RETURN	SIN ( )
	GOTO	COS ( )
	ON-GOTO	TAN ( )
	ON-GOSUB	ATN ( )
	IF-THEN-ELSE	=, >, >/=,
	INPUT	<, </=, <>
	LET	ASC ( )
	ONERR	CHR ( )
	ONEXT1	CBY ( )
	ONTIME	GET
	PRINT	IE
	PRINT#	IP
	PH0.	PORT1
	PH0.#	PCON
	PH1.	RCAP2
	PH1.#	T2CON
	PUSH	TCON
	POP	TMOD
	PWM	TIME
	REM	TIMER0
	RET1	TIMER1
	STOP	TIMER2
	STRING	XTAL
	UI0	MTOP
	UI1	LEN
	UO0	FREE
	UO1	PI

internal memory.

4.3 Description of Statements.

Noteworthy program statements supported by the MCS BASIC-52 interpreter are the CLOCK1, DIM, ONTIME, and RETI statements.

The CLOCK1 statement enables the REAL TIME CLOCK feature resident on the MCS BASIC-52 device. The special function operator TIME is incremented once every 5 milliseconds after the CLOCK1 statement has been executed. The CLOCK1 statement uses TIMER/COUNTER 0 in the 13-bit mode to generate an interrupt once every 5 milliseconds i.e the special function operator TIME has a 5 millisecond resolution. The MCS BASIC-52 automatically calculates the proper reload value for TIMER/COUNTER 0 after the crystal value has been assigned. If no crystal value is assigned, the interpreter assumes a value of 11.0592 MHz. The special function operator TIME counts from 0 to 65535.995 seconds. After reaching the maximum count TIME overflows back to zero. The interrupts associated with the CLOCK1 statement cause the MSC BASIC-52 programs to run at 99.6 % of normal speed i.e. the interrupt handling for the REAL TIME CLOCK feature consumes only 0.4 % of the total CPU time.

The DIM statement reserves storage for matrices. The storage area is first assumed to be zero. Matrices in the MCS BASIC-52 may have only one dimension and the size of the dimensioned array may not exceed 254 elements. The number of bytes allocated for an array

is 6 times the array size plus 1 i.e. the array A(100) would require 606 bytes of storage.

Since the MCS BASIC-52 processes a line in the millisecond time frame and the timer/counters on the 8052AH operate in the micro-second time frame, there is an inherent incompatibility between the timer/counters. To eliminate this problem the ONTIME statement is used. The ONTIME statement generates an interrupt each time the special function operator, TIME, is equal to or greater than the expression following the ONTIME statement. The interrupt forces a GOSUB to the line number following the expression in the ONTIME statement. Because the ONTIME statement uses the special function operator, TIME, the CLOCK1 statement must be executed in order for ONTIME to operate. The ONTIME statement must be exited with a RETI statement.

The RETI statement is used to exit from interrupts that are handled by the MCS BASIC-52 program. The RETI statement performs the same function as the RETURN statement with the exception that it also clears a software interrupt flag to enable further interrupts.

PROGRAM 1 - INDUSTRIAL APPLICATION

LINE STATEMENT

```
1    PRINT " CARRIER CURRENT TRANSCEIVER DEMONSTRATION "
2    PRINT " ",CR
3    PRINT "ENTER INITIAL ACTIVATION TIME  :  ": INPUT "ON ",P,Q,R
4    PRINT " ",CR
5    PRINT "ENTER ON TIME INTERVAL  :  ": INPUT "ON INTERVAL ",M
6    PRINT "ENTER OFF TIME INTERVAL  :  ": INPUT OFF INTERVAL ",N
7    PRINT " ",CR
8    PRINT "ENTER DISABLE TIME  :  ": INPUT "DISABLE TIME ",S,T,U
9    PRINT "ENTER DISABLE INTERVAL  :  ": INPUT "INTERVAL ",V
10   PRINT " ",CR
11   PRINT "ENTER CURRENT TIME OF DAY  :  ": INPUT "TIME ",A,B,C
12   INPUT "AM=0,PM=1 ",D
20   Z=P*3600+Q*60+R
30   X=S*3600+T*60+U
40   Y=Z+M
50   E=A*3600+B*60+C
60   TIME=E : CLOCK 1 : ONTIME 1,100 : DO
70   WHILE TIME<43199 : GOTO 200
```

LINE STATEMENT

```
100     F=TIME
101     IF INT(TIME)=X THEN GOTO 500
102     IF INT(TIME)>X THEN GOTO 600
103     IF INT(TIME)=Z THEN GOTO 300 ELSE GOTO 104
104     IF INT(TIME)=Y THEN GOTO 400 ELSE GOTO 110
110     G=D*12*3600+F
120     H=INT(G/3600)
130     I=INT((G-H*3600)/60)
140     J=G-H*3600-I*60
150     PRINT USING (##),H,"HOURS",I,"MINUTES",J,"SECONDS",CR,
160     ONTIME F+1,100 : RETI
200     IF D=1 THEN D=0 ELSE D=1
210     E=0
300     PORT 1=0FFH
301     PRINT " ",CR : PRINT "ELEMENT SWITCHED ON !"
302     GOTO 104
400     PORT 1=07EH
401     PRINT " ",CR : PRINT "ELEMENT SWITCHED OFF !"
402     LET Z=Y+N
403     LET Y=Z+M
404     GOTO 110
```

LINE STATEMENT

```
500     LET Z=X+V+1
501     LET Y=Z+M
502     GOTO 102
600     IF INT(TIME)>X+V THEN 103
601     GOTO 110
```

PROGRAM 2 - DOMESTIC APPLICATION

LINE STATEMENT

```
1     PRINT " CARRIER CURRENT TRANSCEIVER DEMONSTRATION "
2     PRINT " ",CR
3     PRINT "DEVICE 1 :"
4     INPUT "ON TIME 1 ",P,Q,R : INPUT "OFF TIME 1 ",S,T,U
5     INPUT "ON TIME 2 ",P1,Q1,R1 : INPUT "OFF TIME 2 ",S1,T1,U1
6     INPUT "ON TIME 3 ",P2,Q2,R2 : INPUT "OFF TIME 3 ",S2,T2,U2
7     PRINT " ",CR
8     PRINT "DEVICE 2 :"
9     INPUT "ON TIME 1 ",J,K,L : INPUT "OFF TIME 1 ",M,N,O
10    INPUT "ON TIME 2 ",J1,K1,L1 : INPUT "OFF TIME 2 ",M1,N1,O1
11    INPUT "ON TIME 3 ",J2,K2,L2 : INPUT "OFF TIME 3 ",M2,N2,O2
12    PRINT " ",CR
13    PRINT "ENTER CURRENT TIME OF DAY : ": INPUT "TIME ",A,B,C
14    PRINT " ",CR
15    INPUT "AM=0,PM=1 ",D
16    DIM A(254)
17    LET V=1 : LET W=1
20    A(1)=P*3600+Q*60+R
```

LINE STATEMENT

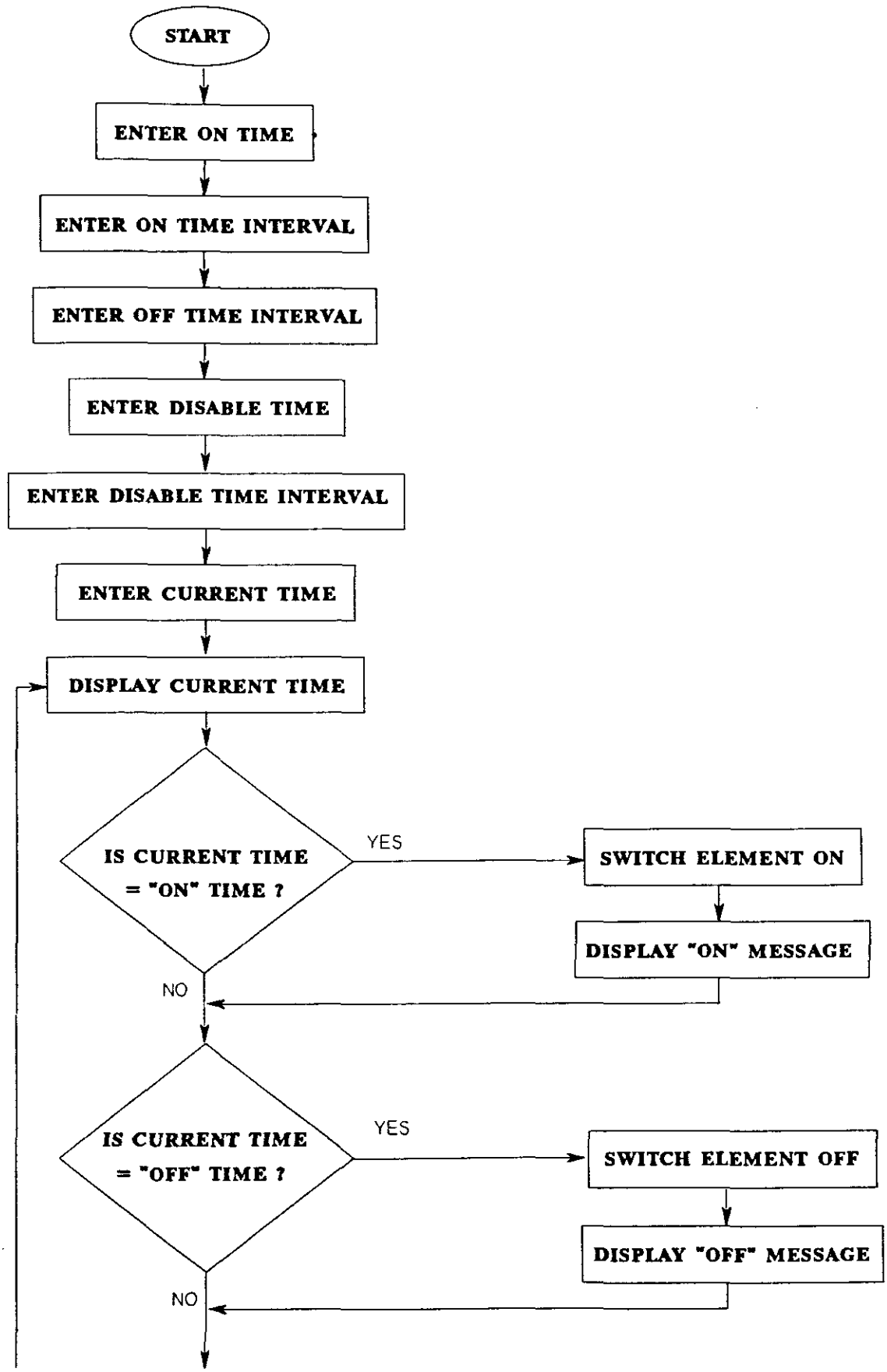
```
21    A(2)=P1*3600+Q1*60+R1
22    A(3)=P2*3600+Q2*60+R2
40    B(2)=S*3600+T*60+U
41    B(3)=S1*3600+T1*60+U1
42    B(4)=S2*3600+T2*60+U2
60    C(1)=J*3600+K*60+L
61    C(2)=J1*3600+K1*60+L1
62    C(3)=J2*3600+K2*60+L2
80    D(2)=M*3600+N*60+O
81    D(3)=M1*3600+N1*60+O1
82    D(4)=M2*3600+N2*60+O2
100   E=A*3600+B*60+C
105   TIME=E : CLOCK 1 : ONTIME 1,100 : DO
110   WHILE TIME<43199 : GOTO 200
115   F=TIME
120   IF INT(TIME)=A(V) THEN GOTO 300
121   IF INT(TIME)=B(V) THEN GOTO 400
122   IF INT(TIME)=C(V) THEN GOTO 500
123   IF INT(TIME)=D(V) THEN GOTO 600
130   G=D*12*3600+F
140   H=INT(G/3600)
```

LINE STATEMENT

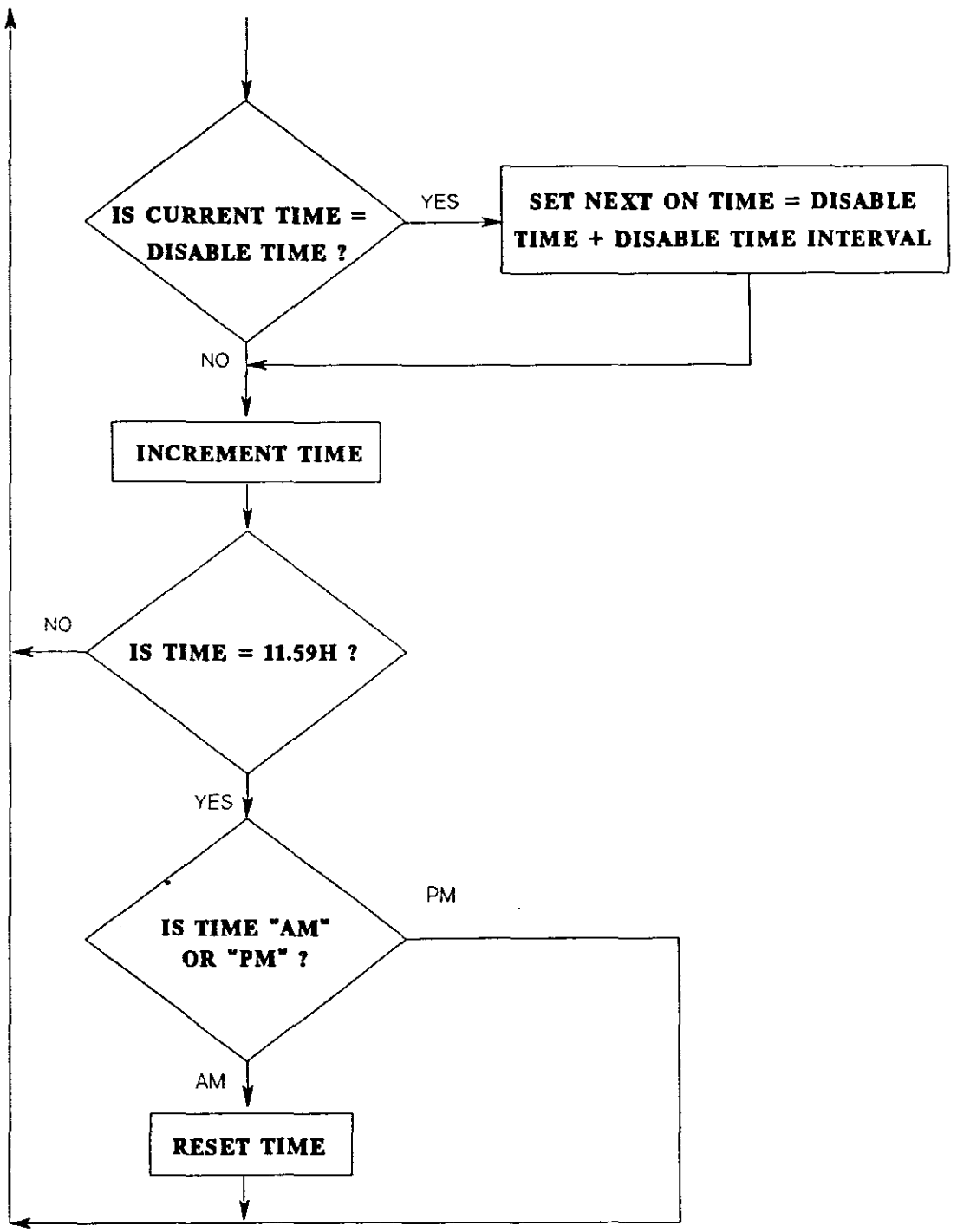
```
150     I=INT((G-H*3600)/60)
160     J=G-H*3600-I*60
170     PRINT USING (##),H,"HOURS",I,"MINUTES",J,"SECONDS",CR,
180     ONTIME F+1,100 : RETI
200     IF D=1 THEN D=0 ELSE D=1
210     E=0
220     GOTO 700
230     GOTO 105
300     PORT 1=0FFH
301     PRINT " ",CR : PRINT "DEVICE 1 SWITCHED ON !"
302     LET V=V+1
303     GOTO 121
400     PORT 1=07EH
401     PRINT " ",CR : PRINT "DEVICE 1 SWITCHED OFF !"
402     GOTO 122
500     PORT 1=06EH
501     PRINT " ",CR : PRINT "DEVICE 2 SWITCHED ON !"
502     LET W=W+1
503     GOTO 123
600     PORT 1=0EFH
601     PRINT " ",CR : PRINT "DEVICE 2 SWITCHED OFF !"
```

LINE	STATEMENT
602	GOTO 130
700	LET V=1
701	LET W=1
702	GOTO 230

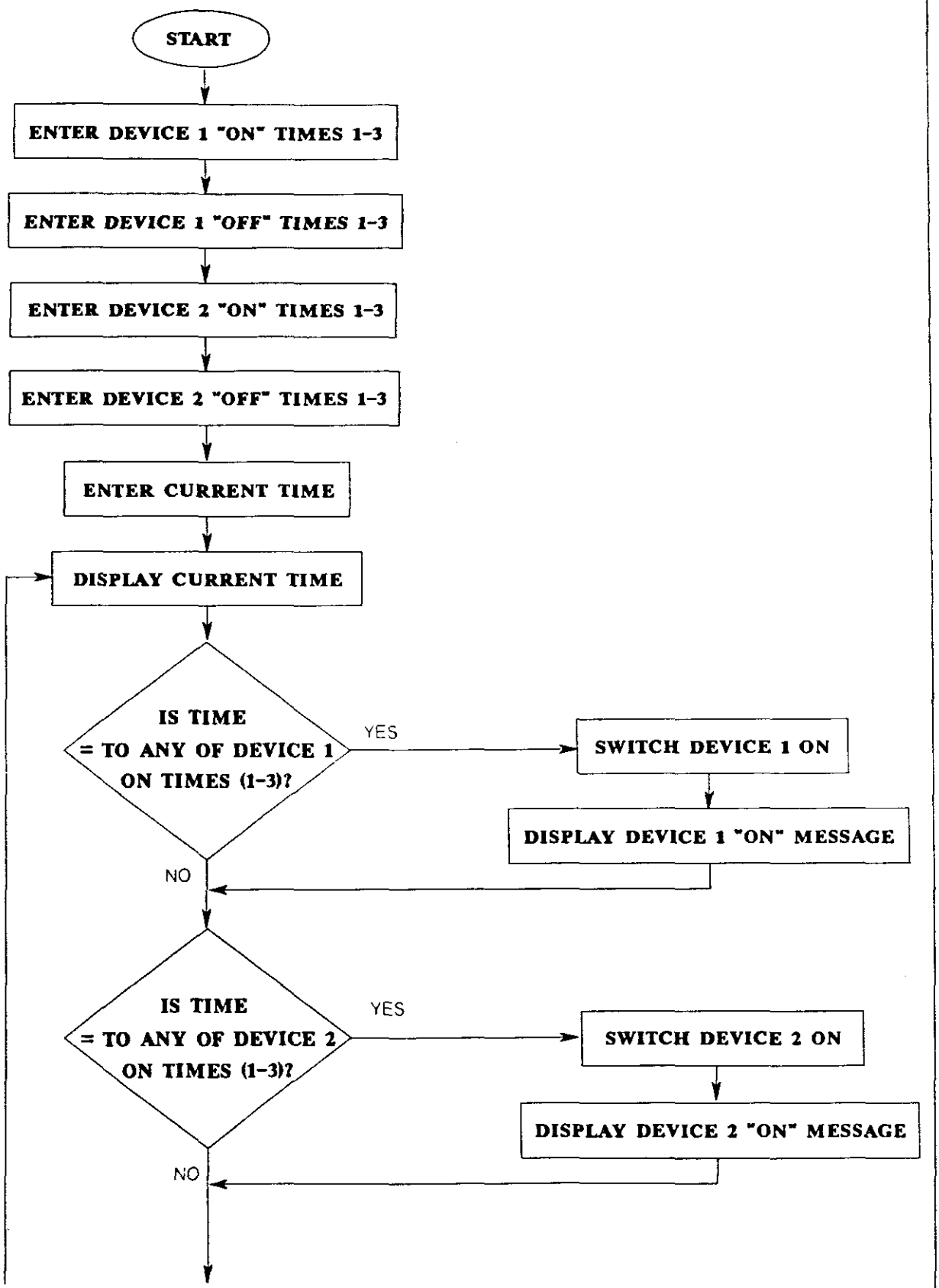
FLOW-CHART 1 – INDUSTRIAL APPLICATION



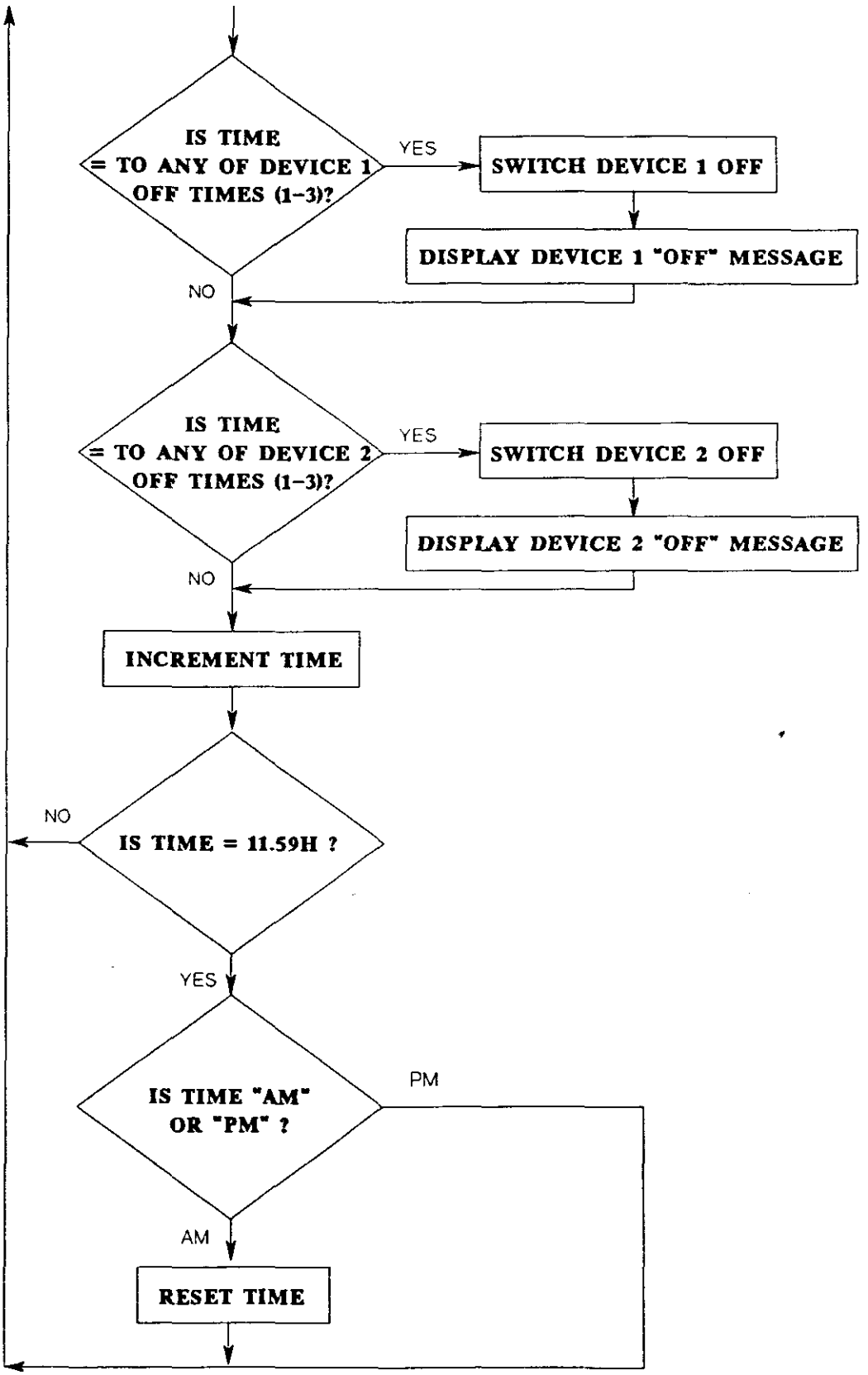
FLOW-CHART 1 - INDUSTRIAL APPLICATION



FLOW-CHART 2 - DOMESTIC APPLICATION



FLOW-CHART 2 - DOMESTIC APPLICATION



5. Operating Instructions.

As explained in Section 2 the Remote Control System may operate in either the Remote Control Mode or the Half-Duplex Mode. These modes are selected using dip-switches situated on the transceiver boards (refer to Figures 5 and 6 on pages 9 and 10).

5.1 Remote Control Mode.

To select the Remote Control Mode of operation, switches 1 and 2 of SW1 on the transmitter are set to the OFF position and switches 1 and 2 of SW1 on the receiver are set to the OFF and ON position respectively. Switch 1 selects the signal path by applying a logic high to the logic circuitry. Switch 2 applies a logic high and logic low to pin 6 of the Carrier-Current Transceiver on the transmitter and receiver respectively. This forces the Carrier-Current Transceivers into their respective transmit and receive modes.

The receiver address is comprised of an 8 bit address and a 4 bit PIN number. The 8 bit address is set using switches 2-7 on SW2 with the 4 bit PIN number being set by switches 5-8 on SW1. Both SW1 and SW2 are situated on the receiver board. Inputs 1 and 8 of the encoder, U2, are toggled each time the receiver is addressed thereby ensuring different on and off addresses. Using all of the available address settings, the Remote Control System is able to address up to 4096 remote switches.

Once the mode of operation has been set, the transmitter may be plugged into a mains

plug at any convenient location. The serial port of a terminal or P.C., used to initialise the program, is then connected to the transmitter's DB 25 connector. The electrical device to be switched is plugged into the receiver which is in turn plugged into the mains plug nearest the device.

Note: The receiver must be placed within the transmission range of the transmitter which is generally greater than one hundred meters. Refer to section 3.3.1.2 for a detailed description of power line attenuation and transmission range.

A terminal emulation package, VTERM, was used in conjunction with a P.C. in the development of this project and the operation thereof is therefore explained in the following paragraph.

Once VTERM is installed on the P.C. and the transmitter and receiver switched on, a space bar is typed on the keyboard. The following log-on banner will appear on the screen "MCS-51(tm)BASIC Vx.x". The required program is then retrieved from ROM by typing "ROM, the program number, CR". The 8052-AH will respond with the message "READY" if the program exists and is not corrupted. Program variables, such as on and off times, may be entered after the program has been retrieved from the EPROM memory and loaded into RAM. The program is transferred to RAM by typing "XFER, CR".

The entering of the variables will be prompted by the program. The 8052-AH will again respond with "READY" once this is successfully completed. Once the variables have been

entered the execution of the program is initiated by typing "RUN, CR". The remote electrical device will then be switched on and off according to the variables entered.

5.2 Half-Duplex Mode.

In this mode of operation both the local and remote sites have the capability of transmitting data and are therefore referred to as transceivers. To select the Half-Duplex Mode, dip-switch 1 on SW1 situated on the transceivers, is set to the ON position. Dip-switch 1 isolates the microcontroller, encoder and decoder from the data circuit and connects the RS-232 interfaces directly to the Carrier-Current Transceivers. As in the Remote Control Mode dip-switch 2 on SW1 selects the transmit and receive modes.

Once the dip-switches are set for half-duplex data transmission, the transceivers may be plugged into the mains (observing maximum range) and switched on. The external data source and destination are connected to the transceivers via the RS-232 interfaces. With a transparent data link established over the mains, RS-232 signals emanating from a data source will be transmitted to the remote destination at data speeds up to and including 4.8 kBaud. The example in section 2.2 (Page 8) illustrates how this mains link may be used to for inter-P.C. communication.

6. Project Synthesis and Recommendations.

The objective of this project was to develop a prototype remote control system that would use existing mains wiring systems for interconnectivity between local and remote sites. This concept of remote control has a distinct advantage over conventional remote control systems in that no interconnecting wiring needs to be installed. This feature makes remote control system extremely flexible and is simply and cost effectively installed.

In addition to remotely switching electrical devices, the transceivers may be used for a wide variety of applications i.e. energy management, inter-office communication, fire alarms, security systems, telemetry etc.

This project may be further developed to suit the above mentioned applications and may therefore be regarded as a foundation on which further work can be based.

7. Bibliography.

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