A Micro Processor Based A.C. Drive with a Mosfet Inverter

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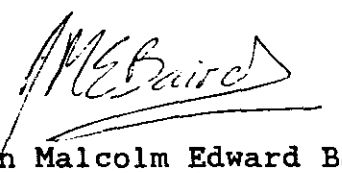
Declaration

I declare that the contents of this Thesis represent my own work and the opinions contained here are my own. It has not been submitted before for any examination at this or any other institute.



John Malcolm Edward Baird

Dedication

This humble effort is dedicated to the ALMIGHTY GOD who gave me life, health, wisdom, knowledge and guidance to complete this thesis.

Many thanks to my parents (Alex and Joan Baird) for their never ending source of encouragement and interest shown in my work. To my friends for there understanding. To Peter Cloete for all the help and assistance given during the developing and testing of the inverter. To the other Master students at the Cape Technikon for their help. To the Lecturers of the Electrical Engineering department at the Cape Technikon for their help and to the Cape Technikon for making available to me their facilities which made the completion of this thesis possible. Finally full thanks to Siemens (South Africa) for their sponsoring PART of this thesis for myself.

SUMMARY

A detailed study into the development of a three phase motor drive, inverter and microprocessor controller using a scalar control method. No mathematical modelling of the system was done as the drive was built around available technology.

The inverter circuit is of a Voltage source inverter configuration which uses MOSFETs switching at a base frequency of between 1.2 KHz and 2 KHz.

Provision has been made for speed control and dynamic braking for special applications, since the drive is not going to be put into a specific application as yet, it was felt that only a basic control should be implemented and space should be left for special requests from prospective customers.

The pulses for the inverter are generated from the HEF 4752 I.C. under the control of the micro processor thus giving the processor full control over the inverter and allowing it to change almost any parameter at any time.

Although the report might seem to cover a lot of unimportant ground it is imperative that the reader is supplied with the back-ground information in order to understand where A.C. drives failed in the past and where A.C. drives are heading in the future. As well as where this drive seeks to use available technology to the best advantage.

This Thesis covers only a small part of the research presently under way in Europe, the U.S.A, Japan and other countries. It seeks to apply some of this research in one of the best ways with components which are available locally, in a drive developed for the "small", low power, applications in South Africa.

OPSOMMING

'n Indiepte ondersoek van 'n drie-fasige motor aandrywer; omskakelaar en mikro-beheerder, wat gebruik maak van skaal-beheer-metode is gedoen. Geen wiskundige beheer-model is van hierdie stelsel gedoen nie, aangesien die aandrywer deur middel van bestaande tegnologie ontwerp is.

Die omskakelaar stroombaan is 'n spannings-bron in omskakel konfigurasie. Die omskakelaar maak gebruik van 'MOSFETs' wat tussen 'n frekwensie van 1,2kHz tot 2kHz skakel.

Voorsiening is gemaak vir spoed beheer en dinamiese remming, indien omstandighede dit sou verlang. Aangesien die aandrywer nie in spesifieke omstandighede gebruik gaan word nie, is daar gevoel dat slegs 'n basiese stelsel vir hierdie doel ontwerp gaan word. Voorsienning is egter gemaak vir verdere ontwikkiling van hierdie stroombaan in die toekoms, indien 'n klient dit sou verlang.

'n 'HEF4752' ge-intigreerde stroombaan verskaf die omskakelaar pulse. Hierdie vlokkie word deur die mikrobeheerder beheer, wat beteken dat enige parameter ter enige tyd verander kan word.

Dit is belangrik dat die leser van hierdie verslag oor 'n deeglike agtergrond-kennis van wisselstroom aandrywers beskik. Die leser sal moet verstaan wat die tekortkomings was in die verlede; die toekomstige doelwitte en hoe hierdie ontwerp bestaande tegnologie tot maksimum voordeel gebruik.

Hierdie verslag behandel slegs 'n klein gedeelte van die huidige ontwikkeling in Europa; die VSA; Japan en ander nywerheidslande. Dit streef daarna om van hierdie navorsing toe te pas deur plaaslik beskikbare komponente te gebruik in 'n lae-krag wisselstroom aandrywer, geskik vir dir Suid-Afrikaanse mark.

Contents

Figures

List of Principal Symbols

Lower case letters normally refer to instantaneous quantities and upper-case letters refer to constants, or average, rms, or peak values. Subscripts and superscript relate to particular circuits or systems concerned. Sometimes one symbol represents more than one quantity.

f Frequency (Hz)

I_f Machine field current

I_L Rms load current

I_m Rms magnetising current

I_P Rms active current

I_Q Rms reactive current

I_r Rms rotor current referred to the stator

I_s Rms stator current

T Moment of inertia

V_g Rms air gap

v Instantaneous supply voltage

X_c Commutating reactance

X_r Rotor reactance

X_s Synchronous reactance

X_{ls} Stator leakage reactance

X_{lr} Rotor leakage reactance

δ duty cycle ratio

θ Angle or torque angle

L_s Stator inductance

L_r Rotor inductance

L_{ls} Stator leakage inductance

L_{lr} Rotor leakage inductance

n Turns ratio

Ne Stator synchronous speed (rpm)

Nr Rotor electrical speed (rpm)

P Number of poles (also active power)

P_g Air gap power

P_m Mechanical output power

P_{sl} Slip power

Q Slip power

R_r Rotor resistance

R_s Stator resistance

S Slip per unit

T_e Developed torque

T_l Load torque

T_s Sampling time

V Rms supply voltage

V_f Induced emf

w_e Stator frequency (rad/s)

w_m Rotor mechanical speed (rad/s)

w_r Rotor electrical speed [(P/2) w_m](rad/s)

w_{sl} Slip frequency (rad/s)

Chapter 1

Introduction

The control of D.C. motors requires a variable D.C. voltage which can be obtained from D.C. choppers or controlled rectifiers. These voltage controllers are simple, cheap and easy to control. D.C. motors however are relatively expensive and require more maintenance, due to wear in the brushes and commutators. Although D.C. motors are expensive D.C. drives are used in many industrial applications because of their ability to deliver relatively large torque at low speeds.

The A.C. motor has a number of advantages over the D.C. motor.

To name but a few:

* They are lighter
* Less expensive
* Of lower maintenance because they have no commutators

The A.C. motor requires a complex control system. This system is an interdisciplinary technology which embraces many areas, including power semiconductor devices, A.C. machines, converter circuits, control theory and signal electronics. Because of the expertise required and due to the fact that component costs have been expensive in the past, A.C. drives had become expensive to develop. More recently with the advent of the microprocessor and VLSI circuits it is possible to develop cheap electronic controllers for A.C. drives.

This thesis will discuss in-depth some of the theory and how it was employed to produce an A.C. drive in the low power range. It should also be noted that although this inverter will not be able to drive large power motors of above 10 KW the control and interface circuitry can be standard throughout a whole range of inverters so that only the power circuit will need to change.

A block diagram of an A.C. drive is shown in figure 1.1 and consists of three main components:

* Motor

* Power Circuit (The Converter and Inverter)

* Controller

Each of these components contributes to the whole system and each will be dealt with separately.

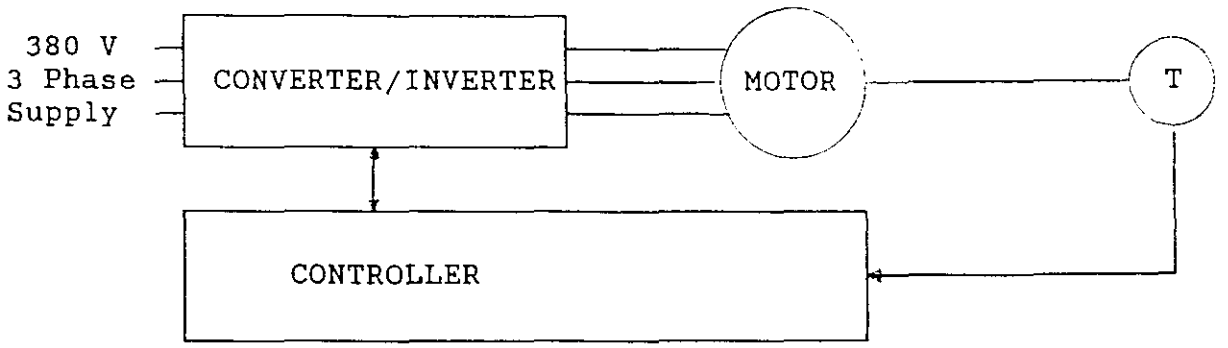


Figure 1.1: BASIC A.C. DRIVE SYSTEM

Chapter 2

A.C. Machines

2.1 Introduction

The A.C. motor is obviously the heart of any A.C. adjustable speed drive and understanding its characteristics is mandatory in designing any A.C. drive. The dynamic behaviour of the A.C. machine is considerably more complex than that of the D.C. machine.

In this chapter we will be looking at the basic static and dynamic characteristics of the induction motor; also an in-depth look at the performance characteristics with emphasis on variable speed applications. This is to note whether or not it is possible for an A.C. motor with the right control to emulate a D.C. motor.

2.2 Induction Machine

Figure 2.1 shows an idealised three phase two pole induction motor where each phase in the stator and rotor windings has a concentric coil. The stator windings are supplied with balanced three phase A.C. voltage, which induces current in the short circuit rotor winding by induction or transformer action.

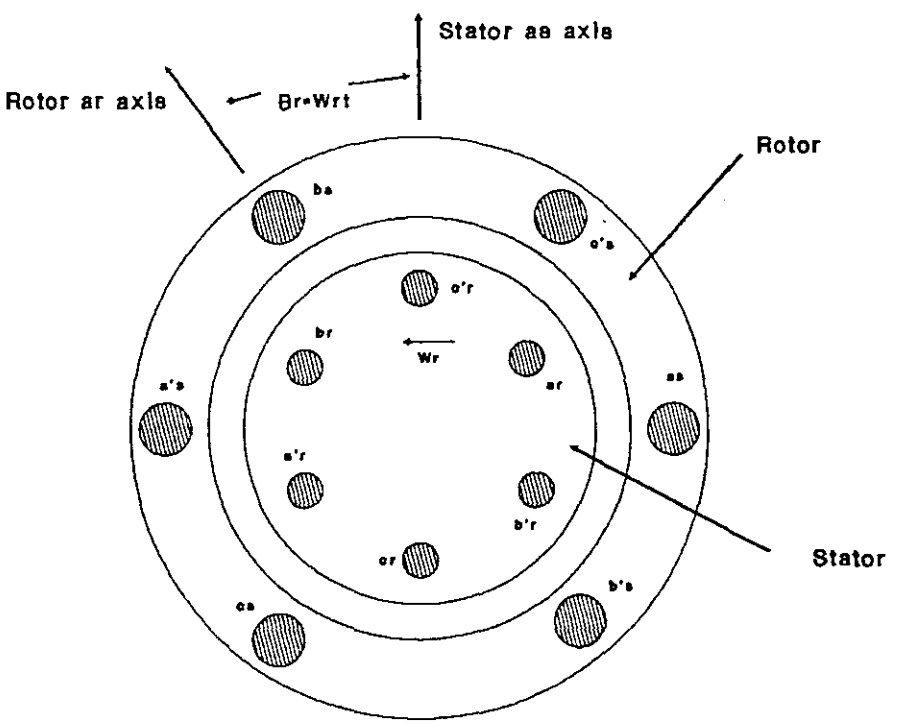


Figure 2.1: IDEALISED THREE-PHASE TWO POLE INDUCTION MOTOR

2.2.1 Torque Production

Assuming that there are no harmonics due to non-ideal distribution of windings and non-sinusoidal voltage and current waves , it has been shown that the stator establishes a spatially distributed sinusoidal flux density wave in the air gap at synchronous speed given by [Ref.1]:

$$N_e = \frac{120\ f_e}{P}$$

where N_e is the speed in rpm, f_e the stator frequency in hertz, and P is the number of poles. Since the rotor is initially stationary, its conductors are subjected to a sweeping magnetic field, thus inducing a rotor current at the same frequency. It is this interaction of the air gap flux with the rotor magnetomotive force (mmf) which produces torque in the induction machine. At synchronous speed there is no induction and thus no torque can be produced. At any other speed N_r, the speed differential N_e-N_r creates slip, and correspondingly the per unit slip S is defined as [Ref.1]:

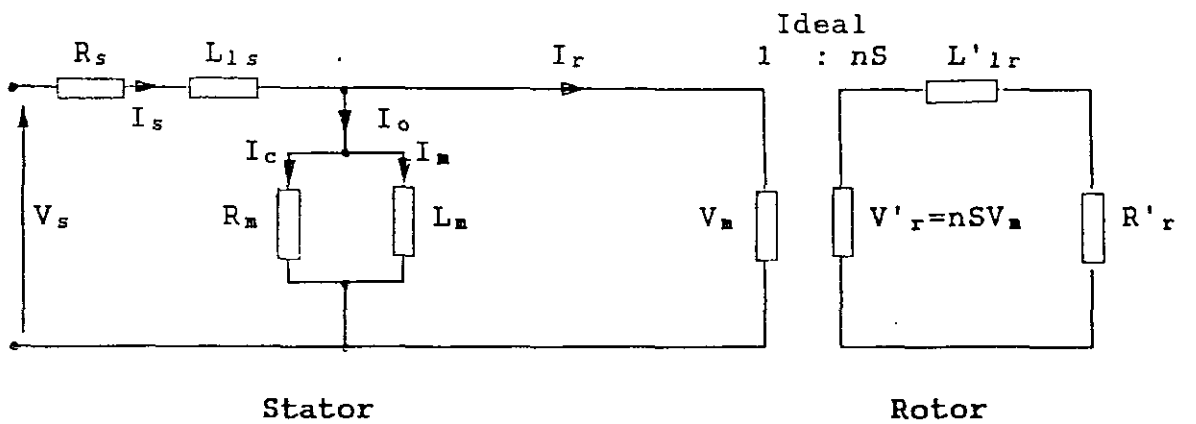
$$S = \frac{N_e - N_r}{N_e} = \frac{w_e - w_r}{w_e} = \frac{w_{sl}}{w_e}$$

The exact formula for torque produced can be shown to be [Ref.1]:

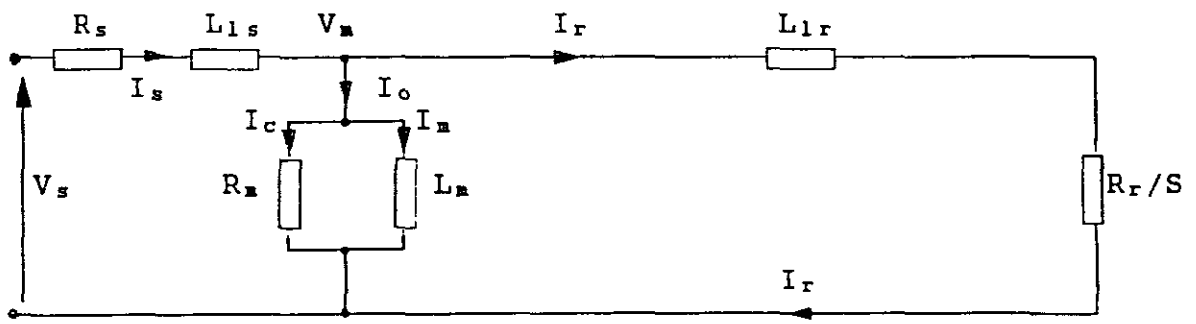
$$T_e = \pi(P/2)\, lr\, B_p\, F_p \sin\delta$$

2.3 Equivalent Circuit

So far the explanation given helps to develop a "transformer like" per phase equivalent circuit as shown in figure 2.2 which is extremely important for the steady state analysis [Ref.7].



(a)



(b)

Figure 2.2: PER PHASE EQUIVALENT CIRCUIT OF INDUCTION MOTOR

From this model it can be proved that the following formulas apply [Ref.1]:

$$\text{Input power } P_{in} = 3\, V_s I_s \cos\theta$$

$$\text{Stator copper loss } P_{ls} = 3I^2{}_s R_s$$

$$\text{Core loss } P_{lc} = 3\,\frac{V^2{}_m}{R_m}$$

$$\text{Power across air gap } P_g = 3I^2{}_r(R_r/S)$$

$$\text{Rotor copper loss } P_{lr} = 3I^2{}_r R_r$$

$$\text{Output power } P_0 = P_g - P_{lr} = 3I^2{}_r R_r\,\frac{1-S}{S}$$

$$\text{Shaft Power } P_{sh} = P_0 - P_{FW}$$

Where P_{FW} is friction and windage loss. Since the power is the product of developed torque T_e and speed, T_e can be expressed as [Ref.1]:

$$T_e = \frac{P_0}{w_m} = \frac{3}{w_m}\; I^2{}_r R_r\,\frac{1-S}{S} = 3\,\frac{P}{2}\, I^2{}_r\,\frac{R_r}{S w_e}$$

where $w_m = (2/P)w_r$ is the rotor mechanical speed (rad/s). By substitution [Ref.1]

$$T_e = \frac{P}{2}\;\frac{P_g}{w_e}$$

This indicates that torque can be calculated from the air gap power by knowing the stator frequency. The power P_g is often defined as torque in synchronous watts.

The equivalent circuit of Fig 2.2 can be simplified to that of fig 2.3 where the core loss resistor has been dropped out of the magnetising inductance L_m and it has been transferred to the input. The approximation is only valid for integral horse power machines [1] where $|(R_s + jw_e L_{ls})| << w_e L_m$. From figure 2.3 the current can be found as [Ref.1]:

$$I_r = \frac{V_s}{((R_s + R_r/S)^2 + w^2_e(L_{ls} + L_{lr})^2}$$

And again by substitution:

$$T_e = 3 \frac{P}{2} \frac{R_r}{S w_e} \frac{V_s}{(R_s + R_r/S)^2 + w^2_e(L_{ls} + L_{lr})^2}$$

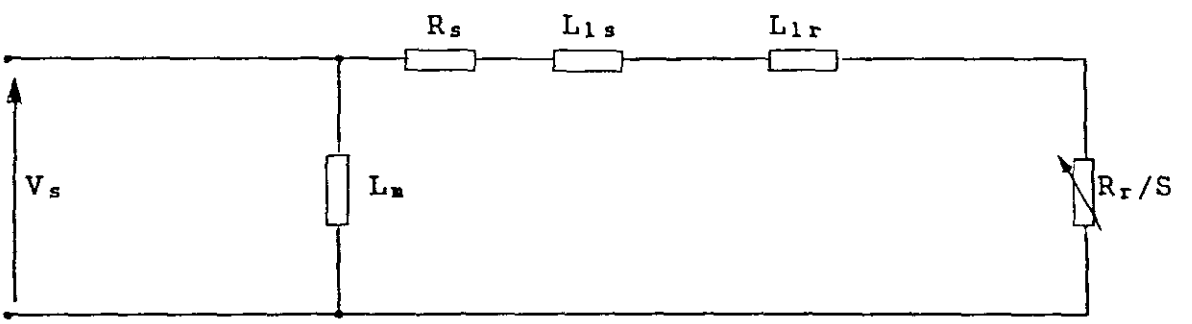


Figure 2.3: APPROXIMATE EQUIVALENT CIRCUIT

2.4 Torque speed curve

If the motor is supplied from a fixed voltage at a constant frequency, the developed torque is a function of the slip and the torque speed characteristic can be determined from the equation:

$$T_e = 3 \frac{P}{2} \frac{R_r}{S w_e} \frac{V_s}{(R_s + R_r/S)^2 + w^2_e(L_{1s} + L_{1r})^2}$$

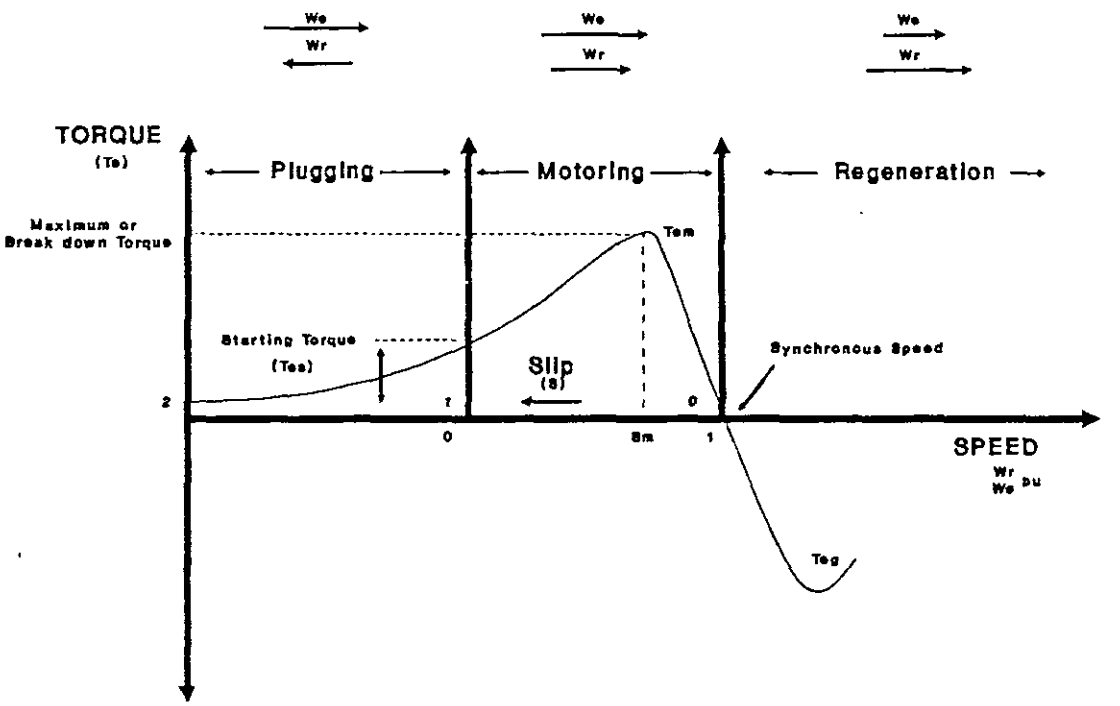


Figure 2.4: TORQUE SPEED CHARACTERISTIC AT CONSTANT VOLTAGE AND FREQUENCY

A typical plot of the developed torque as a function of the slip or speed is shown in figure 2.4. There are three regions of operation:

1. Motoring:

   In motoring, the motor rotates in the same direction as the field; and as the slip increases, torque also increases, the torque also increases while the air gap flux remains constant. Once the torque reaches its maximum value, T_m at $s = s_m$, the torque decreases, with the increase in slip due to reduction of the air gap flux.

2. Regeneration:

   In regeneration, the speed is greater than the synchronous speed, with w_s being in the same direction, and the slip is negative. Therefore R_r/s is negative. This means that power is being fedback from the shaft into the rotor circuit and the motor operates as a generator. The torque speed curve is similar to that of motoring, but having negative torque value.

3. Plugging:

   In plugging, the rotational speed is opposed to the direction of the field rotation therefore the slip is greater than unity. This may happen if the sequence of the supply is reversed, while motoring, so that the direction of the field is also reversed. The developed torque, which is in the same direction as the field,

opposes the motion and acts as a braking torque. Because $s>1$, the motor currents will be high, but torque low.

If $s<1$, $s^2<<s^2_m$ we can derive an equation which gives torque as a function of speed [Ref.4]:

$$w_r = w_s \ (1 - (S_m T_e / 2T_{em}))$$

It can be shown that if the motor operates with small slip, the developed torque is proportional to slip and the speed decreases with torque, therefore speed and torque can be varied by one of the following means:

1. Stator voltage control (Section 2.5)
2. Current control (Section 2.4)
3. Rotor voltage control (Section 2.7)
4. Frequency control (Section 2.8)

2.5 Stator Voltage control

The following equation derived from the torque equation where $S \leq 1$ [Ref.1]:

$$T_e = \frac{R_r(bV_s)^2}{Sw_e\,(R_s + R_r/S)^2 + w^2_e(L_{ls} + L_{lr})^2}$$

indicates that the torque is proportional to the square of the stator supply voltage and a reduction in stator voltage will produce a reduction in speed.

Figure 2.5 shows the typical torque speed characteristic for various values of b. The points of intersection define the stable operation points. This type of voltage control is NOT suitable for a CONSTANT torque load and is normally applied to situations requiring low starting torque and a NARROW range of speed at a relatively low slip.

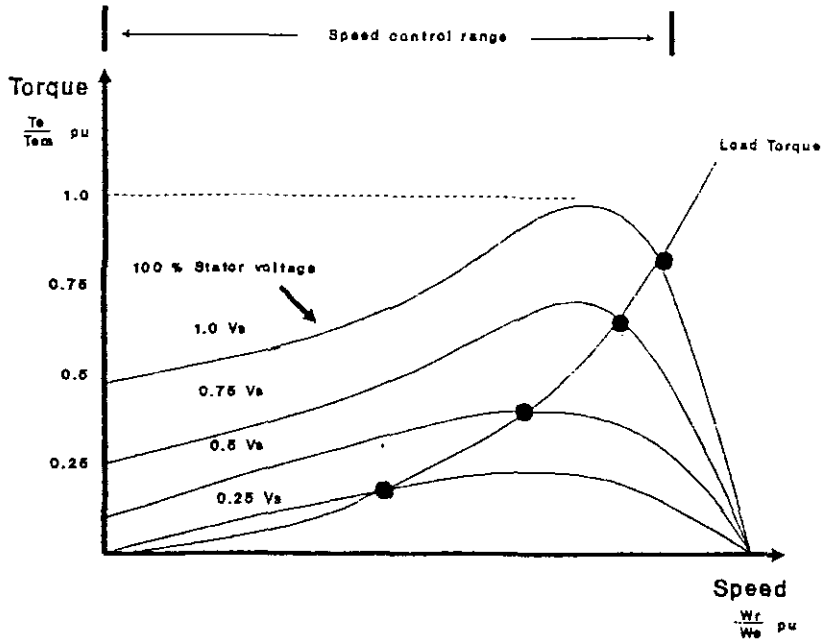


Figure 2.5: TORQUE SPEED CURVES WITH VARIABLE STATOR VOLTAGE

2.6 Current Control

Instead of controlling the stator voltage, the stator current can be controlled directly so as to control the developed torque. With current control, the torque characteristic depends on the relative distribution of magnetising current and rotor current for a fixed stator current magnitude but is independent of stator parameters R_s and L_{ls}. The distribution is affected by the inverse ratio of parallel impedances, which in turn are dependent on frequency and slip [Ref.1].

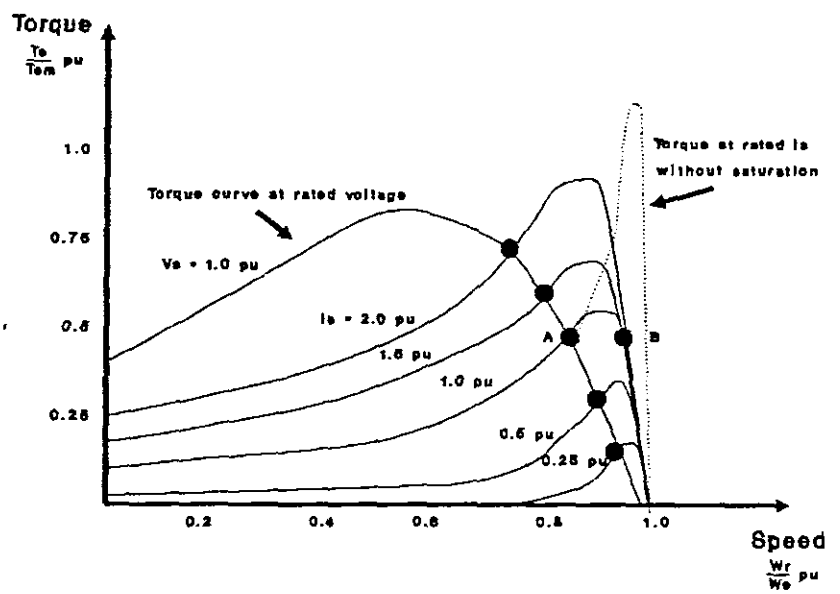


Figure 2.6: TORQUE SPEED CURVES WITH VARIABLE STATOR CURRENT

It can be shown that the maximum torque depends on the square of the current and is approximately independent of the frequency. The typical torque speed characteristics are shown in figure 2.6. As the speed increases the stator voltage rises and torque increases. The torque can be controlled by the stator current and slip. If saturation of the machine is neglected, the torque rises to a high value and then decreases to zero with a steep slope at synchronous speed. In a practical machine the saturation will limit the developed torque as shown. A torque curve with the rated voltage can be intersected at two different points (point A or B) for the same torque demand. Because of lower slip at point "B", the rotor currents will be lower and the air gap flux will be somewhat higher, causing partial saturation. This will result in higher core loss and harmonic torque pulsation (common in Current Source Inverters). Overall operation at "A" is more desirable, but point "A" is on the unstable region of the torque curve. Close loop control is therefore mandatory [Ref.1].

2.7 Rotor Voltage Control

In a wound rotor motor, an external three phase resistor may be connected to its slip rings as shown in figure 2.7. The developed torque may be varied by varying the resistance, R_x. If R_x is referred to the stator winding and added to R_r, the equation [Ref.4]:

$$T_e = \frac{R_r(bV_s)^2}{Sw_e\,(R_s + R_r/S)^2 + w^2_e(L_{ls} + L_{lr})^2}$$

may be applied to determine the developed torque. The typical torque speed characteristics for variations in rotor resistance are shown in Fig 2.8.

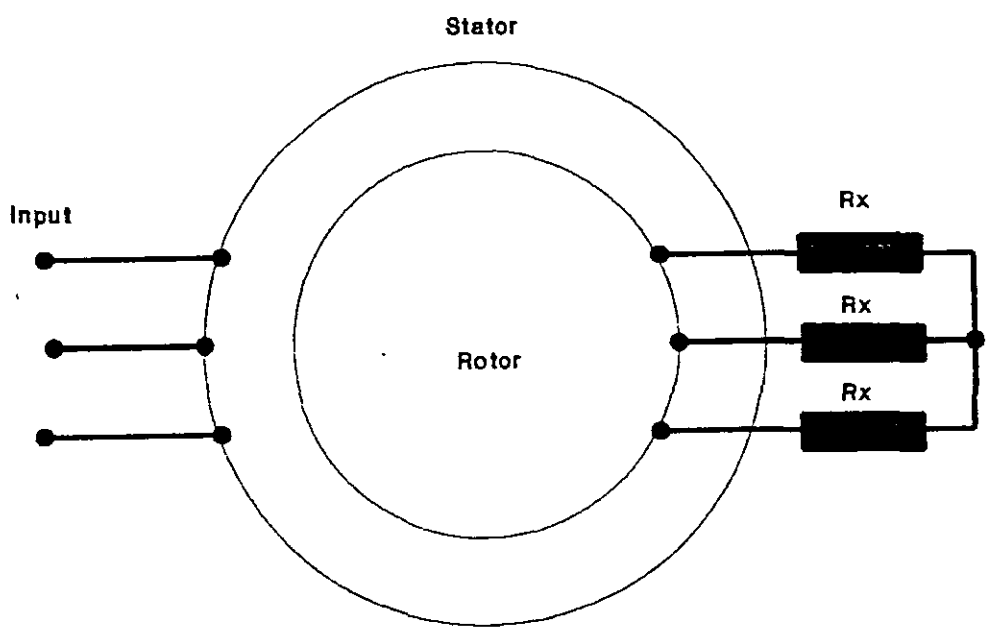


Figure 2.7: SPEED CONTROL BY ROTOR RESISTANCE

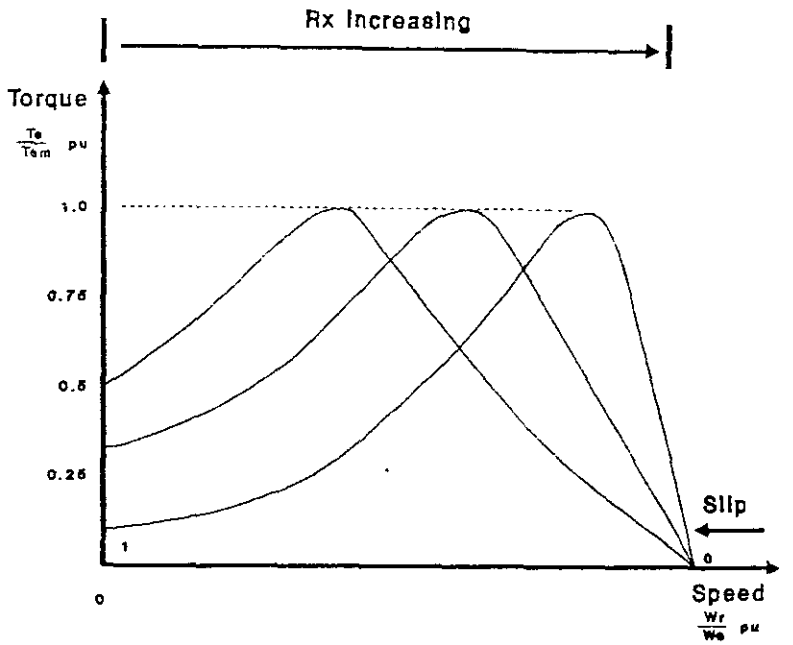


Figure 2.8: SPEED CONTROL BY ROTOR RESISTANCE

This method has been and still is in wide use, since it increases starting torque and decreases starting current; however the system is very inefficient. There would be an inbalance in the stator voltage and current if the resistors in the rotor circuit were not equal.

Two famous drive circuits use this principal namely the "Static Kramer" and "Static Scherbius" drives. These are normally used on large drive systems, due to their bulkiness.

2.8 Variable Frequency Operation

If the stator frequency is increased beyond the rated value, the torque-speed curves, derived from the equation [Ref.1]:

$$T_e = 3 \frac{P}{2} \frac{R_r}{S w_e} \frac{V_s}{(R_s + R_r/S)^2 + w^2_e (L_{ls} + L_{lr})^2}$$

can be plotted as shown in figure 2.9 [Ref.1].

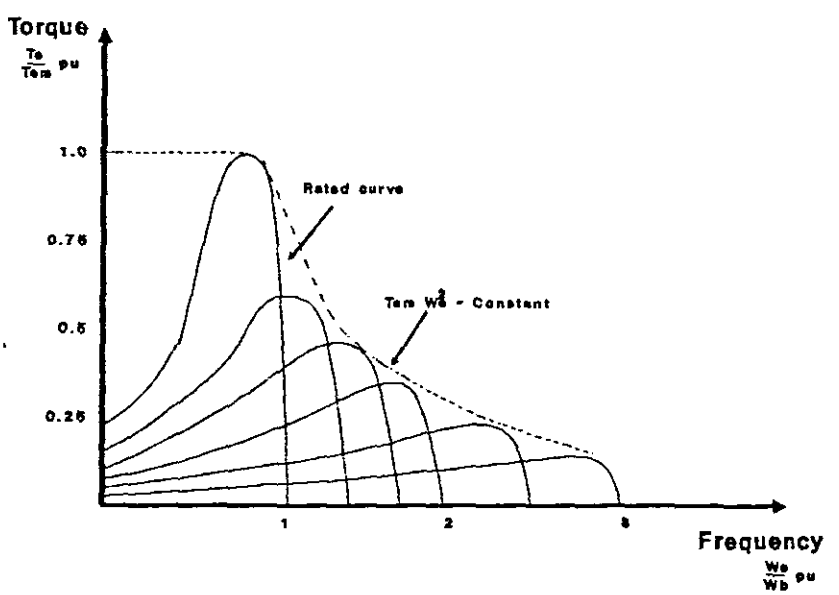


Figure 2.9: TORQUE SPEED CURVES AT VARIABLE FREQUENCY

The air gap flux and stator current decrease as frequency increases, and the maximum torque developed (T_{em}) decreases. The maximum torque as a function of slip can be derived from the torque (T_e) equation [Ref.1].

$$T_{em} = \frac{3}{4}\frac{P}{w_e}\frac{V^2_s}{\sqrt{(R_s^2 + w^2_e(L_{1s} + L_{1r})^2 + R_s)}}$$

Where $w_{slm} = R_r/L_{1r}$ is the slip frequency at maximum torque. The equation shows $T_{em}w^2_{1r}$ to be a constant, thus the machine behaves like a D.C. series motor in variable frequency operation.

If an attempt is made to decrease the supply frequency at rated voltage, the air gap flux will saturate, causing excessive stator current. Therefore, the region below the base frequency w_b should be accompanied by a corresponding reduction of stator voltage so as to maintain constant air gap flux. Figure 2.10 shows the plot of torque speed curves where the V_s/w_e (Volts/herts) ratio remains constant. The maximum torque remains approximately valid except in the low frequency region where the air gap flux is reduced by the stator impedance drop and therefore it has to be compensated for by an additional voltage boost so as to produce maximum torque.

Since the motor is operated at constant air gap flux in constant torque region, the torque sensitivity per ampere of stator current is high, permitting fast transient response of the drive system. In spite of low inherent starting torque for base frequency operation, the machine can always be started at maximum torque, as indicated in figure 2.10.

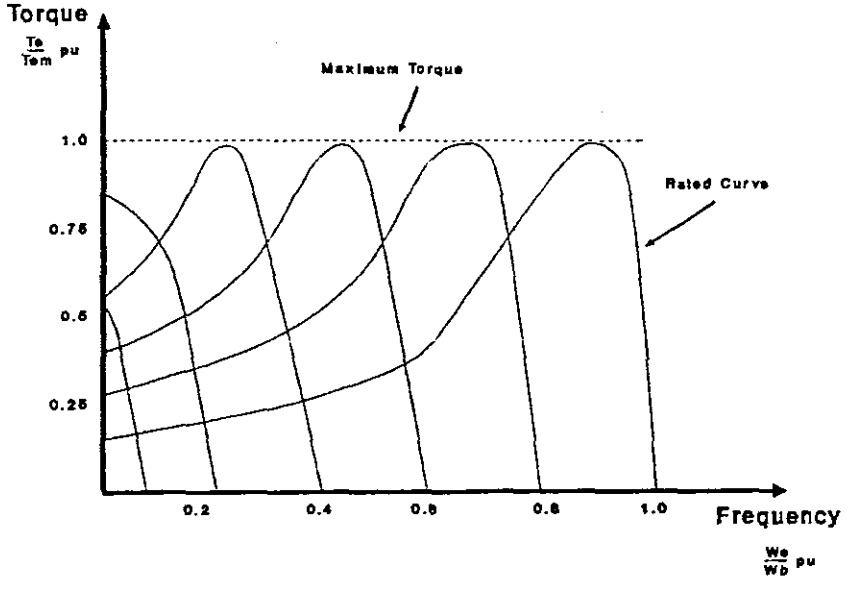


Figure 2.10: TORQUE SPEED CURVES AT CONSTANT VOLTS/HERTZ

The different regions of torque speed curves of a practical drive system with a variable voltage, variable frequency supply are shown in figure 2.11 and the corresponding voltage frequency relationship in figure 2.12.

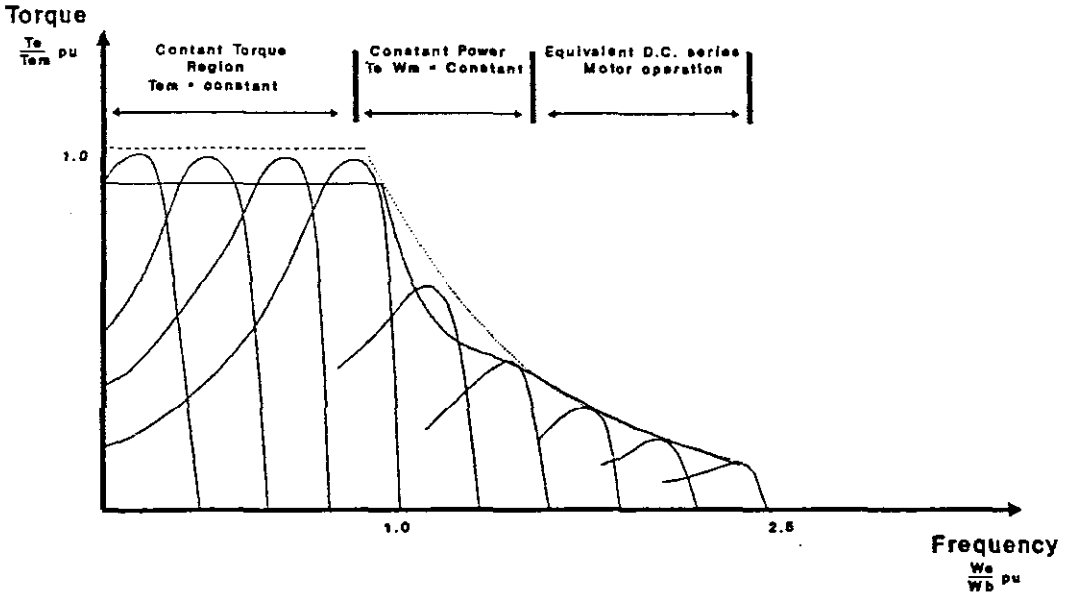


Figure 2.11: REGIONS OF TORQUE SPEED CURVES

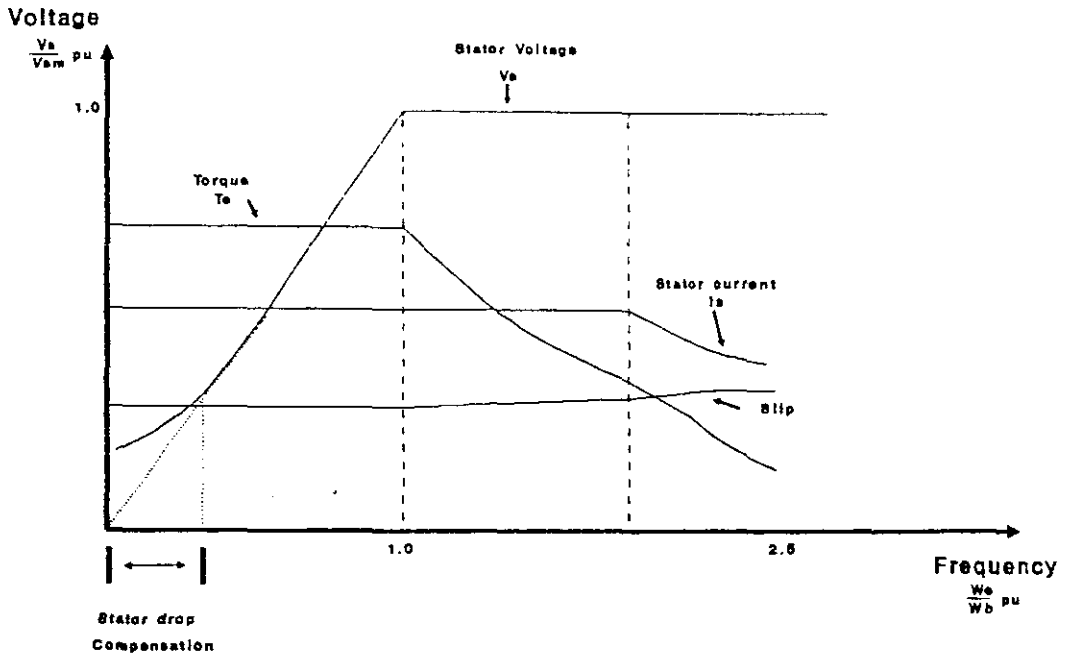


Figure 2.12: VOLTAGE FREQUENCY RELATIONSHIP OF INDUCTION MOTOR

At the right edge of the constant torque region, the stator will reach the rated voltage-value before the machine can enter the constant power region. In the constant power region, the air gap flux decreases, but the stator current is maintained constant by increasing slip. This is equivalent to the field weakening mode done in a separately excited D.C. motor. At the edge of the constant power region, the breakdown torque T_{em} is reached and then the machine speed can be increased by increasing the frequency as shown in figure 2.12 with a reduction of stator current.

2.9 Summary

From the information supplied thus far, one method stands out above the rest, that is the method of the constant volts/herts relationship. Not only does it operate similarly to a separately excited D.C. motor over its full operational range, but because the motor is operating at a constant air gap flux in the constant torque region it permits a fast transient response of the drive system.

Chapter 3

Inverters

With advances in Technology three types of Converter circuits have come to the fore:

* The Cycloconverter
* The voltage source inverter
* The current source inverter

The Cycloconverter is a well known method of controlling induction motors. With advancing technology it has become well established in the larger motor drive range where torque and not speed is the criterion. Normally used in low speed drives larger than 500 KW.

Between the latter two techniques a decision had to be made as to which should be implemented in this project.

A Current Fed Inverter (CFI) requires a stiff D.C. current source at the input, which is in contrast to the stiff voltage source desirable in a Voltage Fed Inverter (VFI). For a basic diagram of the Current Fed Inverter refer to figure 3.1 and for a Voltage Source Inverter refer to figure 3.2.

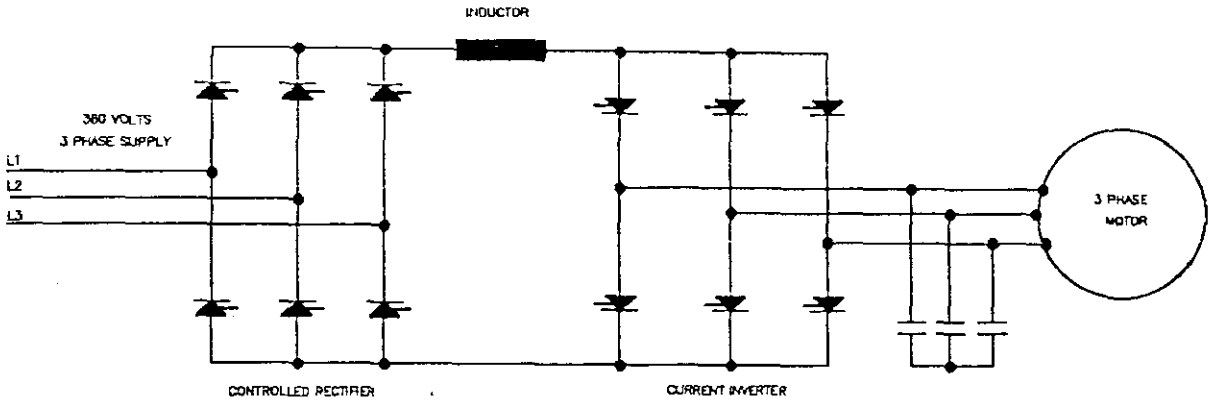


Figure 3.1: CURRENT SOURCE INVERTER

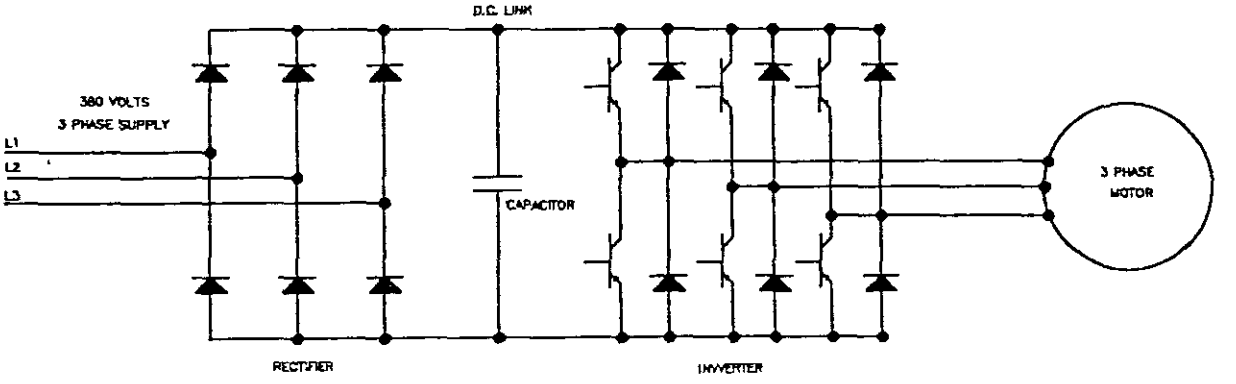


Figure 3.2: VOLTAGE SOURCE INVERTER

3.1 Current Fed Versus Voltage Fed Inverters

Note that a voltage fed inverter can operate in the current control mode by adding a current feedback loop. Similarly, a current fed inverter can operate in voltage control mode, if desired, by adding a voltage control loop. The definition of the voltage fed and current fed inverters is the basis of the question as to whether the D.C. supply is a voltage source or current source. The two classes of inverters have duality in many aspects. A summary comparison of the two classes of inverters can be given as follows (This comparison helped in the design of the inverter):

1. In a current fed inverter, the inverter is more interactive with the load, and therefore a close match between the inverter and machine is desirable. For example, the inverter requires a low leakage inductance, unlike that of the voltage fed inverter, because this parameter directly influences the inverter commutation process. A large leakage inductance of machine filters out harmonics in a voltage fed inverter, but in a current fed inverter it lengthens the current transfer interval and worsens the voltage spike problem. The thyristors and diodes of the inverter may require series connection to combat the spike voltage, which may be several times the peak counter emf.

2. In a current fed inverter because the motor forms part of the commutation circuit, commutation is load dependent thus it is time consuming. As a result, the commutation-angle of "force-commutated inverters" becomes large at light load and high frequency, thereby restricting the highest frequency of operation.

3. The current fed inverter has inherent four quadrant operation capability and does not require extra power components. On the other hand a voltage fed inverter requires a line commutated inverter connected in inverse parallel with the rectifier for regeneration or a pulsed resistor across the D.C. link for dynamic braking. In case of a mains power failure, the regenerated power in the current fed inverter cannot be absorbed in the line and therefore the machine speed can only be reduced mechanically. For a voltage fed inverter, however, dynamic braking is applicable in line power failure conditions.

4. A current fed inverter is more rugged and reliable and problems such as shoot-through fault do not exist. A momentary short circuit in the load and misfiring of the thyristors are acceptable, as the inverter is current limited by the controlled input rectifier (see figure 3.1). Fault interruption by gate circuit suppression is simple and straight forward.

5. In the current fed inverter thyristors have to withstand reverse voltage during part of the cycle and therefore such devices as GTOs, power MOSFETs, transistors and IGBTs cannot be used. Due to large turn off time, the thyristors can be of the inexpensive rectifier grade instead of expensive inverter grade thyristors required for voltage fed inverters.

6. The control of current fed inverters, especially for commonly used auto sequential commutated inverters and load commutated inverters, is simple and similar to the phase controlled line commutated converters.

7. Multi-machine load on a single inverter or multi-inverter load on a single rectifier is very difficult with current fed inverters. An industrial drive usually consists of one rectifier, one inverter and one machine system. In applications where multi-machine or multi-inverter capability is required, a voltage fed inverter may prove economical.

8. Current fed inverters have a sluggish dynamic performance compared to Pulse Width Modulator (PWM) voltage source inverters. The stability problem is more severe at light loads and high frequency conditions. On the other hand, stability problems are minimal in voltage fed inverters and the drive can operate in open loop.

9. The torque pulsations in the current inverter cause harmonic heating problems which are more severe at low frequency operation.

10. The successful operation of the current fed inverters requires that a minimum load should always remain connected. The inability to operate at no load invalidates their application in general purpose power supply application such as in a UPS system.

After considering the above conditions it was decided to develop a Voltage Source Inverter for the following reasons:

1. It has greater stability

2. It has a wider range of operating frequency

3. The ease with which the constant volts/herts control method can be implemented.

4. It is more efficient.

3.2 Voltage Source Inverter

A voltage source inverter is characterised by a stiff D.C. voltage supply at the input. The D.C. supply may be fixed or variable. The inverter application may include adjustable speed A.C. drives, regulated voltages and frequency power supplies, UPS and induction heating.

In a voltage fed inverter, the power semiconductor devices always show constant forward bias due to the D.C. supply voltage, therefore some type of forced commutation is mandatory when using thyristors. Alternatively self commutating with base or gate drive is possible when using GTOs, MOSFETs, transistors or IGBTs.

Voltage source inverters can be divided into two major types:

1. Square-wave type

2. Voltage and frequency controlled type

The latter was chosen as it is the better method of control when using the constant volts/herts relationship. It can be implemented by the following two methods:

1. A Pulse Width Modulation (PWM) method

2. A Pulse Amplitude Modulation (PAM) method

For the voltage control of a PAM method, only the former method is applicable. If the A.C. supply is rectified to D.C., there are two possible schemes, using

1. a phase controlled rectifier with filter

2. a diode rectifier chopper with filters.

With a phase controlled rectifier, the A.C. line side harmonics are high and power factor deteriorates at reduced voltage. In the latter case the power has to be converted twice but high line side power factor with near unity displacement factor is possible. The PWM method is used, since it does not convert the energy twice.

The variation of D.C. link voltage will not cause any problems in self commutated inverter operation using GTOs, MOSFETs or transistor devices.

3.3 Pulse Width Modulation

In the past, sinusoidal Pulse Width Modulation (PWM) speed control systems for three phase A.C. motors have been produced in a number of different forms and by as many methods. Figure 3.3 shows the general principle of PWM where an isosceles triangle carrier wave is compared with a fundamental frequency modulating sine wave, and the natural points of intersection determine the switching points of the power devices on the output bridge.

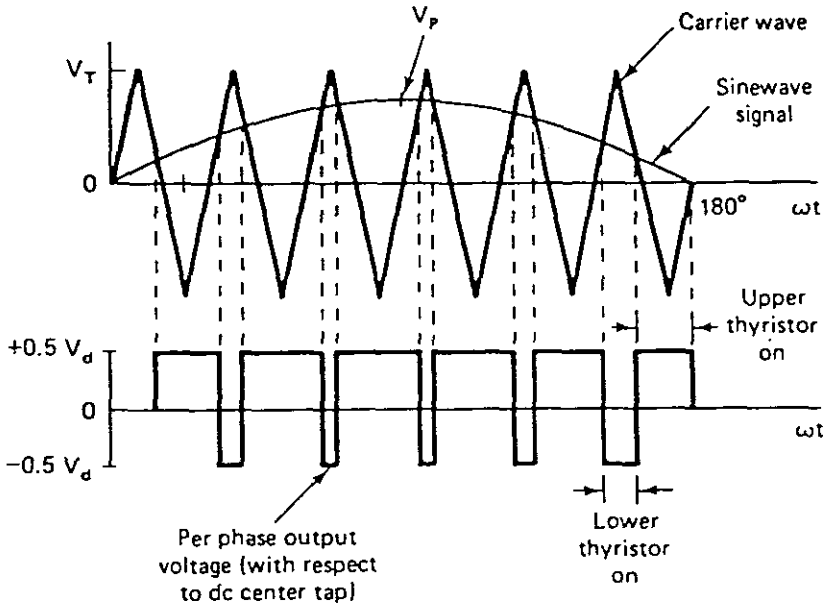


Figure 3.3: PRINCIPLE OF SINUSOIDAL PWM WITH NATURAL SAMPLING

Advanced Technology has allowed the generation of the PWM signal for inverters in using basically three methods:

1. A large scale integration device such as the HEF 4752

2. A peripheral component which has to be continually serviced by a micro processor to provide for the wave-form generation. Such is the SLE 4520.

3. A software intensive use of the port pins, timers and other peripheral devices of a micro processor to generate the wave-forms.

The generation of the PWM signal, although a small section of an inverter, has been the subject of extensive research in the recent past. It is quite understandable as it is here that the efficiency of the INVERTER is consummated and matched to its load.

Although very interesting, it is not necessary to enter into great studies in this section, in an inverter design, since there are Integrated Circuits (ICs) available on the market which incorporate this technology in an affordable package. One such device available in South Africa is the HEF 4752 manufactured by Philips.

The IC provides all three complementary pairs of output drive wave-forms for the six element inverter. All lock out times are also taken care of. By defining certain inputs into the IC the output parameters such as lock out time, output voltage

and frequency can be changed. The device is completely digital so that repetition frequency of the PWM signal is always an exact multiple of the inverter output frequency and therefore results in excellent phase and voltage balance, thus giving low motor losses.

For the harmonic content of the wave-forms produced and current wave-form obtained by the use of this IC refer to the section on results and to the appendix.

To save calculation time to establish the inputs, a simulation of the IC was performed on "Lotus" to obtain the necessary clock inputs and make sure that the range of performance was still in the range of the device's specifications. See appendix.

The HEF 4752 is a complex IC and is dealt with in-depth by references one, two and three of the periodicals (a part copy appears in the Appendix).

3.4 Dynamic Braking

In adjustable speed A.C. drives, the machine may be subject to electrical braking for reduction of speed. In electrical braking , the motor is operated in the generating mode. The energy stored in the system inertia is converted to electrical energy. The energy is then either dissipated in a resistor, used in parallel drive systems, or recovered in the power supply. The former is known as dynamic braking, see figure 3.4, and the latter is known as regenerative braking, see figure 3.5.

For small power drive applications dynamic braking is adequate.

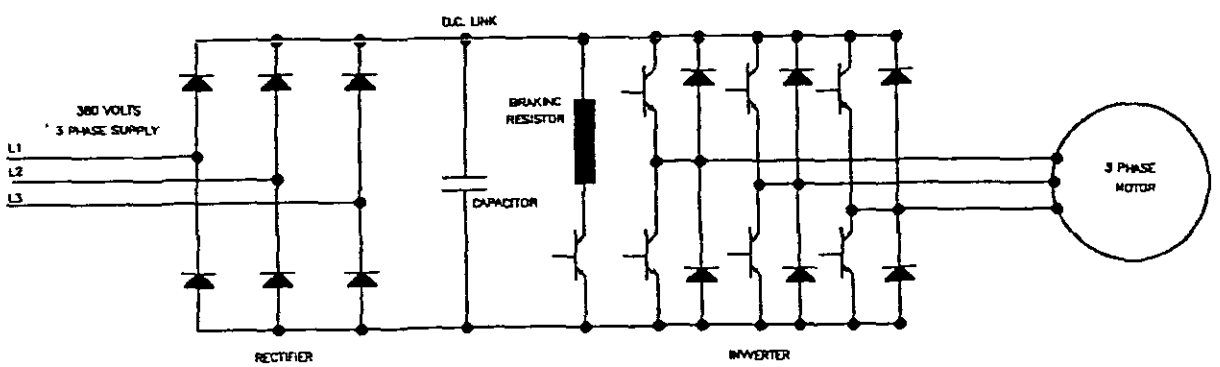


Figure 3.4: DYNAMIC BRACKING

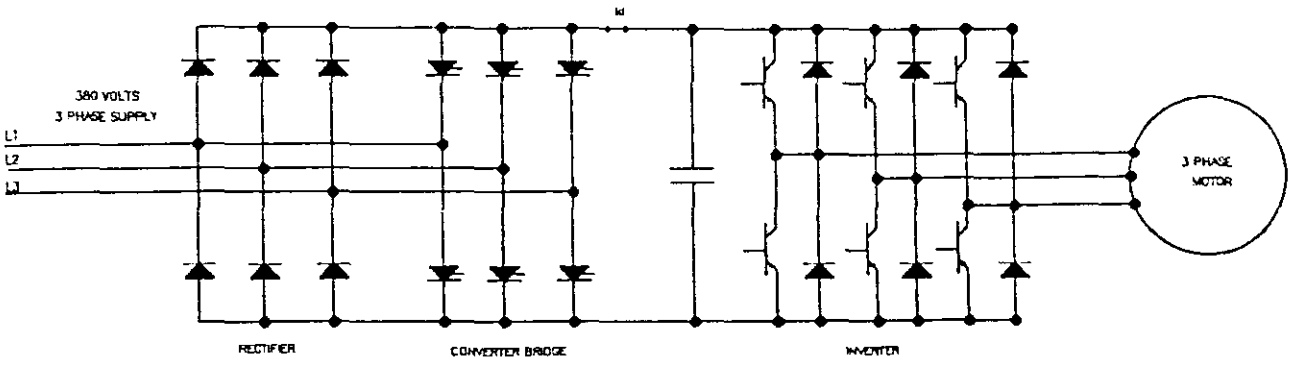


Figure 3.5: REGENERATIVE BRACKING

Chapter 4

Control of Induction Machines

There has arisen two basic methods of controlling the Induction machine

1. Scalar Method

2. Vector Method

Scalar control relates to the magnitude control of a variable only. The command and feedback signals are D.C. quantities which are proportional to the respective variables. This is in contrast to vector control or field orientation control (FOD), where both magnitude and phase of vector variables are controlled.

A break down of the methods of both scalar and Vector control methods is given in figure 4.1. Since the drive which was designed falls into the general purpose range it is quite adequate to use a scalar control method. Vector control needs expensive sensing and fast computation thus making it even more expensive.

An open loop scalar control is implemented on the system mainly because of cost and also because the drive is for limited applications only.

Control of an Induction Motor

1. Scalar Control Method
   - 1.1. Open Loop Constant Volts/herts Method
   - 1.2. Closed Loop Current Control Volts/herts Method
   - 1.3. Constant Volts/herts Speed Control with Slip Regulation
   - 1.4. Torque Flux Control
   - 1.5. Current Controlled PWM Inverter
   - 1.6. Constant Flux operation with Programmable Current Control
2. Vector Control Methods
   - 2.1. Direct Vector Control Method
   - 2.2. Indirect Vector Control Method
   - 2.3. Space Vector Modulation Method

Figure 4.1: METHODS OF CONTROL

Chapter 5

Power Semiconductors

There are three main groups of "Switching" Power Semiconductors

1. Thyristors
2. Transistors
3. MOSFETs

The Transistors and MOSFETs can be considered to be part of the same family. In recent years new components have been added to these families. For the thyristor the GTO, and for the most resent combination of the Transistor and the MOSFET there is the Insulated Gate Bipolar transistor (IGBT), which shows great promise for the medium power high frequency switch inverter range.

It is impossible to do a complete comparison of the devices and show the reason for choosing MOSFETs for the inverter. However, briefly it can be said that:

* Thyristors were not chosen. When used in a voltage source inverter they need to be force commutated, thus resulting in a bulky power circuit.

* Transistors require a high current drive on the base, leading to difficulty in switching.

* IGBT although very well suited are quite expensive and hard to obtain in South Africa at present.

* MOSFETs being quite easy to switch result in a compact power circuit design and are well suited to small power applications.

5.1 The Power Mosfet

The MOSFET is a voltage controlled majority - carrier device. With a positive voltage applied to the gate with respect to the source terminal, it induces an N-channel and permits electrons to flow from source terminal to the drain terminal. Because of SiO_2 layer isolation, the gate circuit impedance is extremely high typically in the range $10^9\Omega$. This feature permits power MOSFET to be driven directly from CMOS or TTL logic. The devices have an integrated reverse rectifier which permits free - wheeling current of the same magnitude as that of the main device.

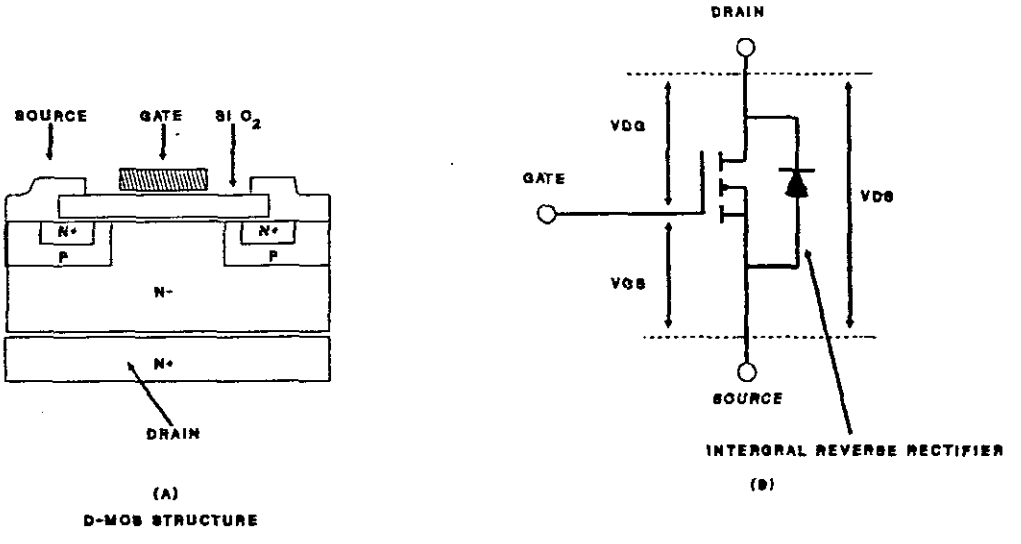


Figure 5.1: THE MOSFET

5.1.1 Characteristics

The fundamental drain source characteristics of a power MOSFET are shown in figure 5.1. The gate has a threshold voltage of between 2 and 4 volts below which the drain current is very small. The conduction loss of a High voltage MOSFET is very high. However its switching loss is almost negligible.

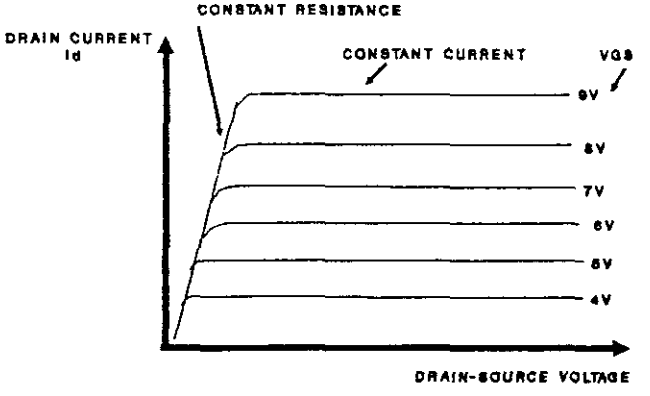


Figure 5.2: POWER MOSFET CHARATERISTICS

Although MOSFETs can be controlled statically by the voltage source, it is normal practice to drive it by a current source dynamically followed by a voltage source to minimise switching delays. Figure 5.2 shows a typical gate drive circuit of a MOSFET with R.C. snubber across the device.

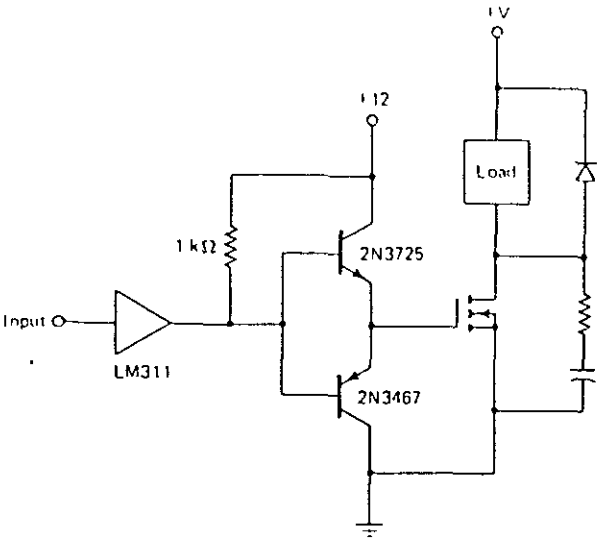


Figure 5.3: MOSFET GATE DRIVE CIRCUIT WITH SNUBBER (REF.1)

Chapter 6

Implementation

6.1 The Inverter

All calculations for this section appear in the appendix under their appropriate appendix-sections.

6.1.1 The Power Circuit

The configuration of the inverter is shown in figure 6.1. As stated before, the inverter circuit employs MOSFETs as its main switching component. The safe operation of these devices is solely determined by thermal considerations, the approximate calculations are shown in the appendix.

The devices are all N-channel type, thus the top side of each of the inverter legs have to be driven by isolated power supplies.

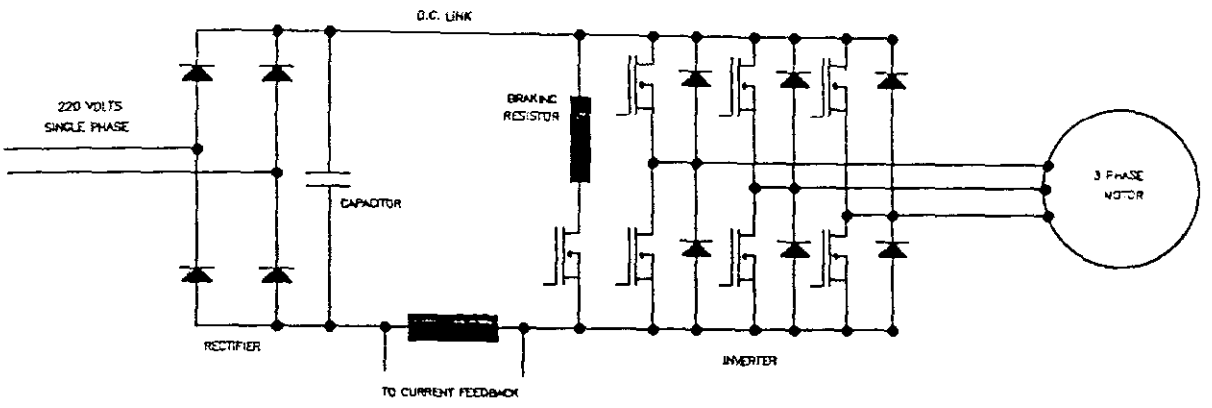


Figure 6.1: POWER CIRCUIT

The D.C. link contains two large capacitors so as to provide as smooth a D.C. supply as possible to the switching components. To the input is a mains filter which stops Radio Frequencies from the inverter radiating on to the mains supply and also limits the current during the charging of the capacitors and prevents spikes in either direction.

6.1.2 The Driver Circuit

In the section "The Power MOSFET" a driver circuit is shown in figure 5.2. It was used in the first prototype inverter and proved to be unsuccessful. A low, zeo volts, on the base of the two transistors causes the NPN to turn off and the PNP to turn on thus discharging the gate of the power MOSFET, but not completely. For as the gate voltage approached one volt the

transistor starts to turn off, because it requires a 0.7 volt drop across its base emitter to remain on, allowing a leakage current to flow.

The driver circuit, now used, is shown in the figure 6.2. The change being the use of the N and P channel signal FETs which provide a fast and clean switch from the positive rail to zero. Both devices have an extremely low "on" resistance and charge and discharge the gate of the power MOSFET easily.

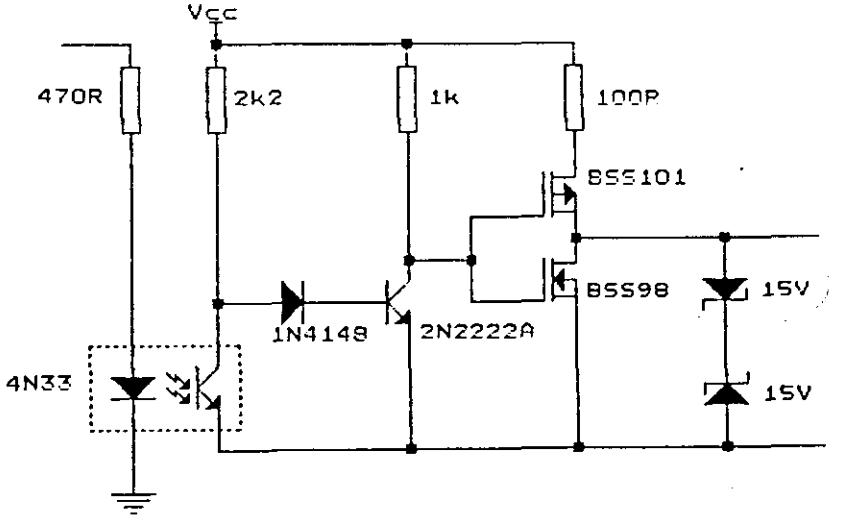


Figure 6.2: DRIVER CIRCUIT

With an inductive load, the drain source voltage transient is coupled to the gate via the drain-to-gate capacitance. To protect the gate from damaging overvoltage a Zener diode protection is necessary, since the drive circuit impedance is low.

The Opto couple circuit presented the largest problem as it is here that the turn on and turn off delay had to be compensated for. Although fast opto couple circuits are available their drive currents are quite high. While the ones used have a low drive current but slower switching speed. To compensate for the delay caused by the opto couple was no problem for the HEF4752 chip.

6.1.3 Protection

It is in this section where the greatest amount of experimentation took place as very little literature is available on this section. Most corporations that produce drives do not divulge information concerning protection and even place this section's components entirely in epoxy to prevent any investigation and copying.

Protection is divided into two sections. Firstly dv/dt protection then di/dt protection. Comprehensive derivation of the formulas will not be shown and it must be noted that during the derivation certain things were assumed thus rendering them applicable to this application only (See appendix for calculations).

6.1.3.1 dv/dt

dv/dt protection is normally in the form of a snubber network, which comes in many different forms see figure 6.2. In this application the unpolarised snubber was used, which provides protection during switching on and switching off of the device, as well as protection during the switching of the other half of the phase leg. The main reason for using a snubber is that when switching an inductive load a destructive voltage spike is produced, although this spike is bypassed by a fast recovery diode, the stray inductance, in the circuit which is not bypassed by the diode, may cause destructive

over-voltage. This over-voltage is attenuated by the R.C. snubber.

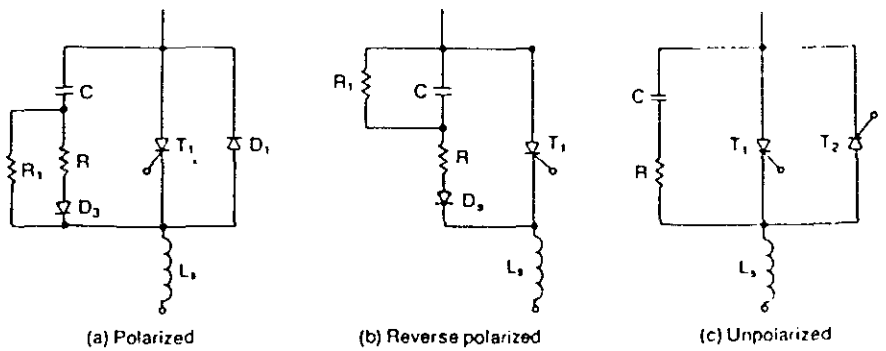


Figure 6.3: SNUBBER CIRCUITS (REF.4)

6.1.3.2 di/dt

Although not a serious problem, di/dt will destroy the power components in the inverter on occurrence. This problem arises when the output is shorted or the motor coils saturate. This problem is overcome by including three air gap coils on the output to prevent saturation. An overall current sensing circuit is included which when triggered shuts down the inverter thus protecting it against any damage. The response time for the shut down is approximately 3uS.

6.1.4 PWM

As already stated the HEF 4752 was used in the generation of the pulses and "Lotus" was used to derive the best input parameters.

The HEF 4752 has three clock frequency inputs (OCT and RCT were joined). Two clock frequency were generated using a counter chip, the reference clock (RCT) input and the voltage clock (VCT)input. The frequency clock (FCT) was generated using a phase lock loop as a multiplier so that a linear adjustment of the clock frequency was possible.

The HEF 4752 generates a PWM wave-form which corresponds to the constant volts/herts method of control. Voltage boosting is possible by adjusting the Voltage control clock (VCT). Since all signals are controlled by a counter chip which is controlled by the micro processor any parameter can be changed during operation with ease.

The reference clock sets the base switching speed in combination with the lock out time. "Lock out time" is a term which refers to the time between the switch off of the top half (top MOSFET) and the switching on of the bottom half of the same leg (and visa versa).

6.1.4 PWM

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6.2 Control

6.2.1 Hardware and interfacing

The control circuitry of the inverter is based around the 8051 micro controller chip. The micro controller provides for all monitoring and controlling routines. For specific details of the micro chip refer to reference [17].

One counter "chip" (8254), a "phase lock loop" (CD4046) and a parallel port interface "chip" (8255) are used in the interfacing. See block diagram figure 6.4. The drive which was developed is only a prototype. An 8051 microprocessor board from Kiberlab in Pretoria with a sub-rack card is being used, with the input commands coming from two push buttons and two switches. It is purposed to replace this system with a developed dedicated micro processor/interface board resulting in compact design.

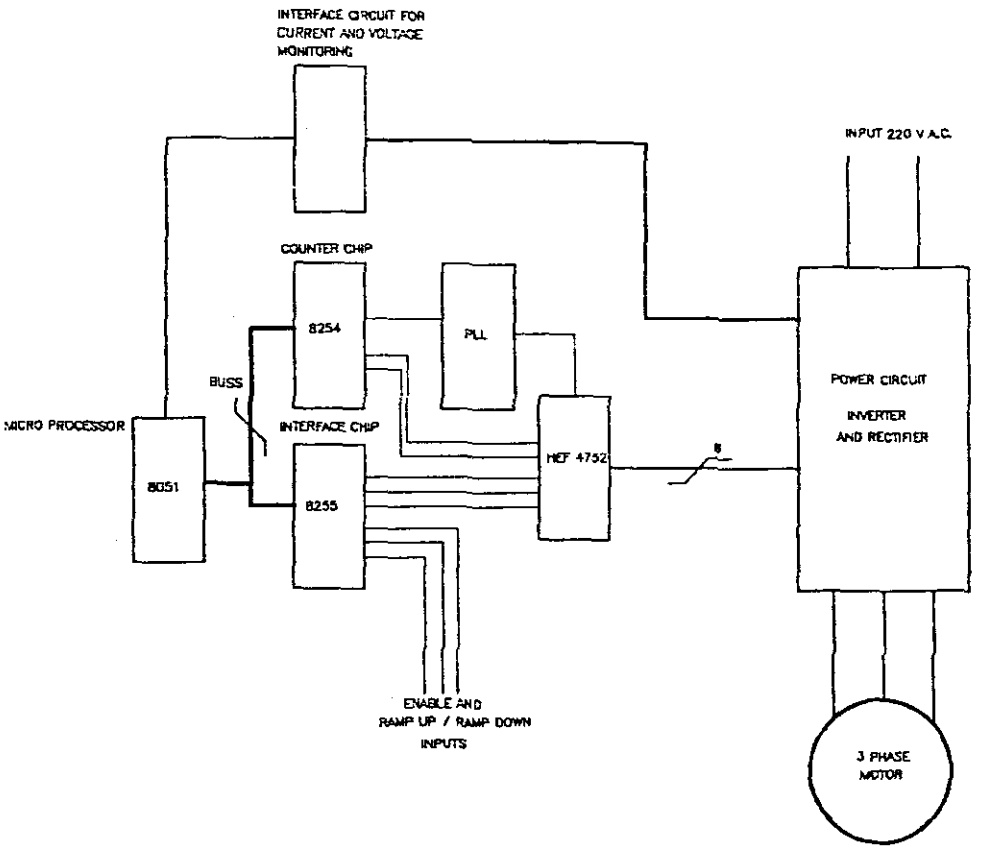


Figure 6.4: SYSTEM BLOCK DIAGRAM

6.2.2 Open loop Volts/Herts control

A block diagram of the control system is shown in figure 6.5. The frequency w_e is the command variable and it is close to the motor speed, neglecting the slip frequency. From the section on the induction motor it can be shown that the machine flux is approximately related to the ratio *vs/we*. Therefore maintaining the rated air gap flux will provide maximum torque sensitivity with current which is similar to that of the D.C. machine. As the frequency approaches zero near zero speed, the stator voltage will tend to be zero and will essentially be absorbed by the stator resistance. Thus it is necessary to boost the voltages at lower speeds.

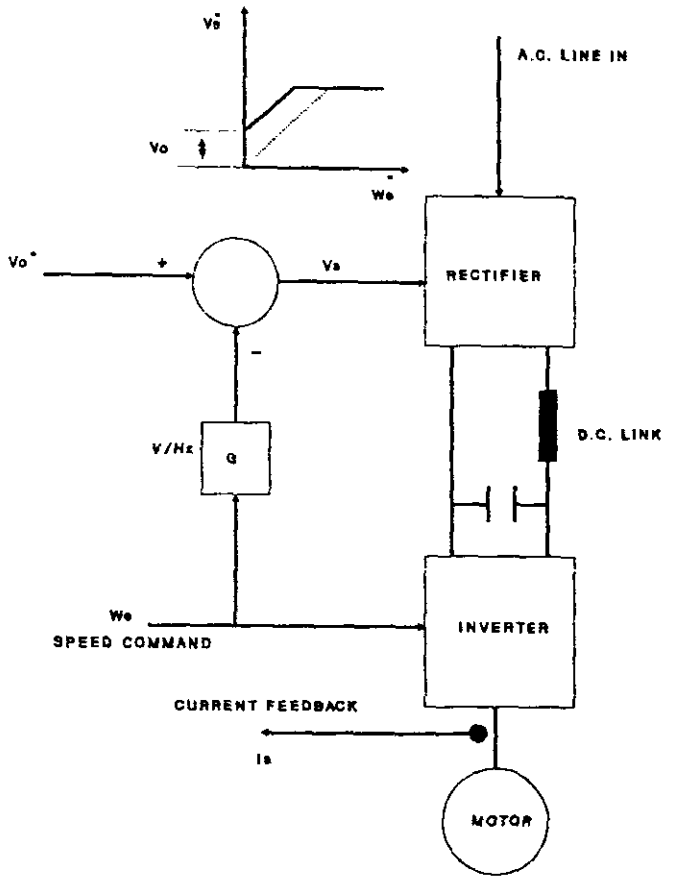
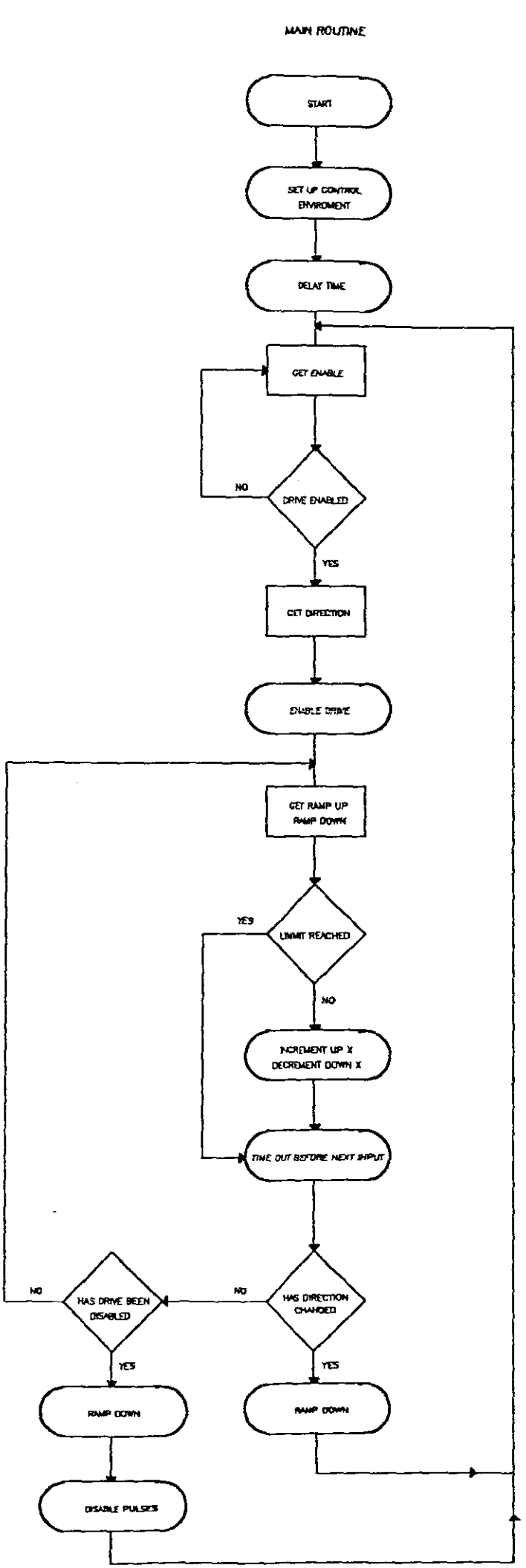


Figure 6.5: OPEN LOOP VOLTS/HERTS CONTROL

This configuration is adequate to drive a constant load. It is essential to ramp the speed up or down over a certain time seeing that the motor is bound by its mechanical time response and ramping too fast would cause the slip to become too large and trip on over current.

A flow chart of the software implemented is shown in figure 6.6. The actual software listing is presented in the appendix.



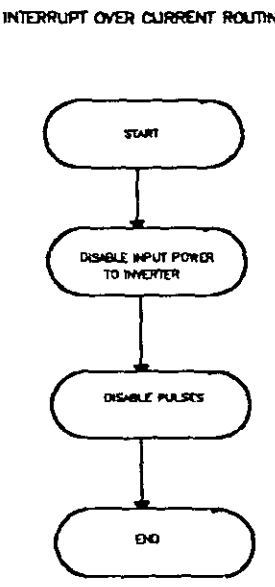


Figure 6.6: SOFTWARE FLOW CHART

Chapter 7

Equipment

The following equipment was used in the development of the drive and the testing thereof:

1. Digital Storage Adapter
   DSA 511
   Thrulby

2. 20 MHz Oscilloscope
   OS-7020
   Goldstar

3. 10 Mhz Frequency Counter

4. EV 80C51 FX Microcontroller Evaluation Board
   Intel

5. PC Based Eprom Programmer
   EW-901
   Sunshine

6. ASM 51
   Intel

7. 286 IBM PC

   With VGA Monitor

8. 3-Phase Motor

   380 Volts

   2 amps per phase

9. Digital Multimeter

   175

   Testmate

10. Analog Multimeter

    YF-303

    YUFUNG

Chapter 8

Results

8.1 Current Wave-form

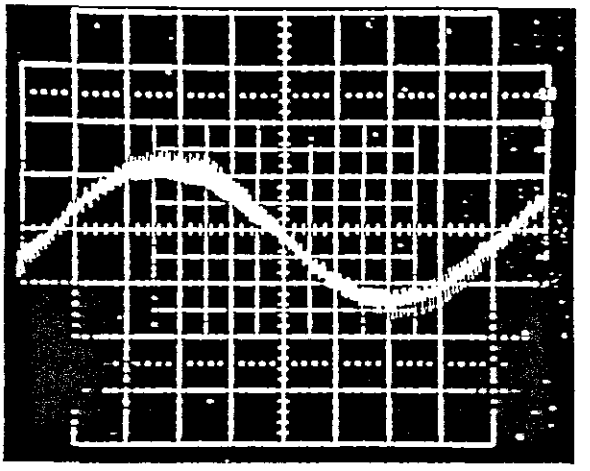


Figure 8.1: CURRENT WAVE-FORM AT 10 Hz

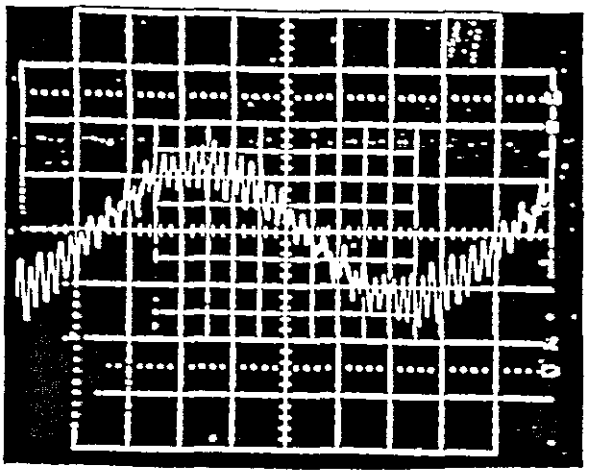


Figure 8.2: CURRENT WAVE-FORM AT 25 Hz

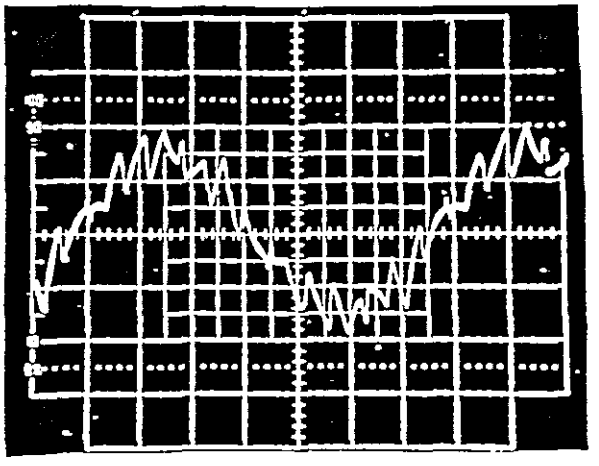


Figure 8.3: CURRENT WAVE-FORM AT 50 Hz

8.2 Torque Curve

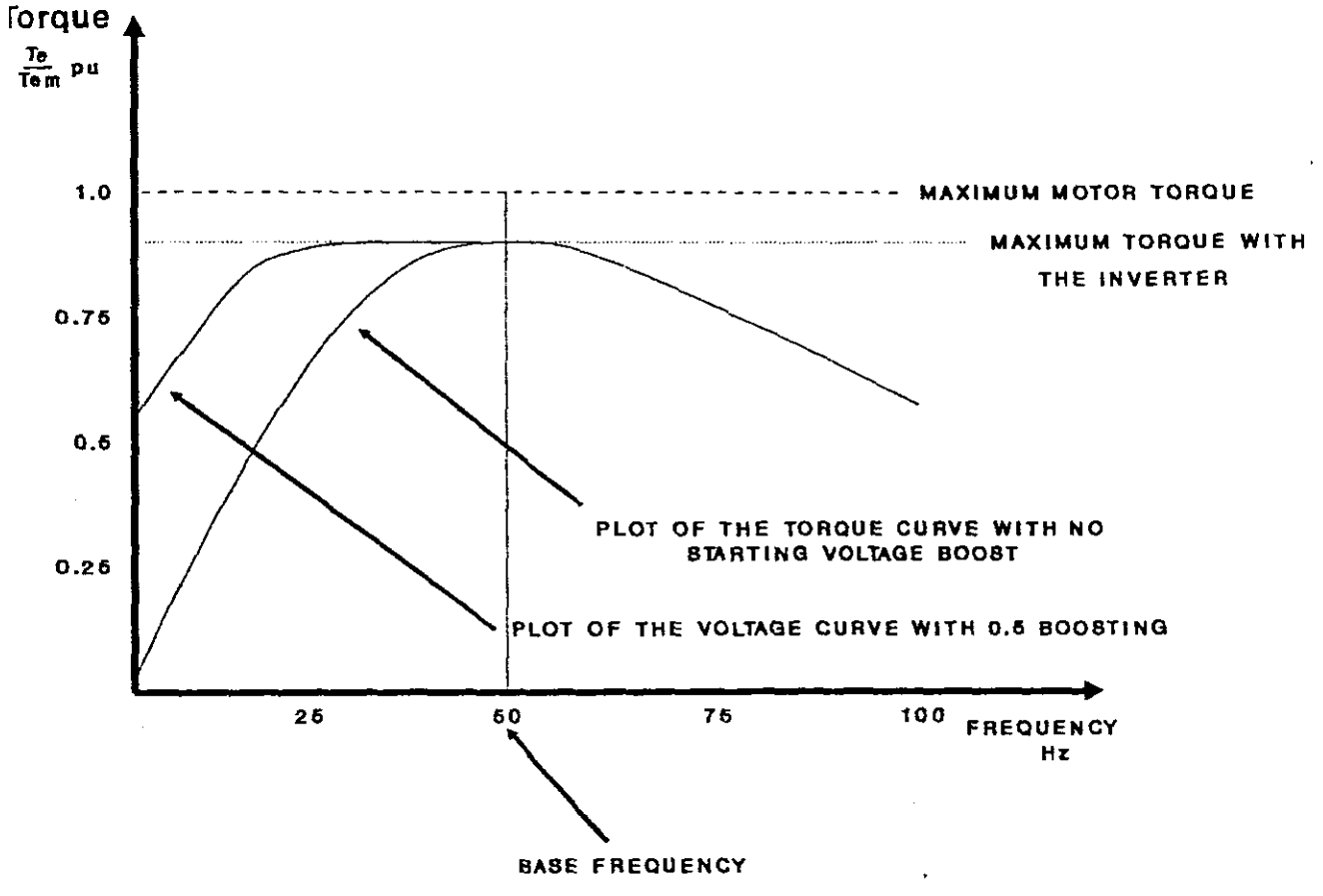


Figure 8.4: PLOT OF TORQUE CURVE

Chapter 9

Specifications

Supply Voltage	220 Volts A.C. Single Phase
Input Frequency	50/60 Hz
System Power Factor	≈1
Output Voltage	0 to 210 Volts Phase to Phase
Output Frequency	5 to 100 Hz
Output Current	Maximum Continuous Current 10 Amps
Power Factor	≤ 0.9
Efficency	90% Into a resistive Load

Chapter 10

Discussion of Results and Specifications

All results and specification were determined either experimentally or by computation of measurements taken.

The current wave-form output is of the same standard as any other drive equipment as it uses an integrated circuit to generate the Pulse Width Modulated signal (see page 68 and 69 for current wave-forms).

The current wave-form compared favourably with the current wave-forms given in the Data sheets of most manufactures of A.C. drives.

The Plot of the torque curve (figure 8.9) verses the input frequency, at first might seem strange as the inverter never allows the motor to reach its maximum torque. The input to the inverter is 220 Volts A.C. single phase allowing a maximum of 311 Volts D.C across the D.C. link. Consequently this in turn allows a maximum of 210 Volts A.C phase to phase out of the inverter. Therefore when using a standard three phase 380 Volt A.C. motor it is not possible to generate the maximum motor torque.

There are two graphical plots (figure 8.9) of the motor torque verses input frequency:

1. With no voltage boosting at the lower frequency levels. The resistance of the motor inhibits the reactive current (I_r) from flowing thus there is very little torque at low speeds.

2. With half voltage boosting. Boosting the voltage at low input frequency compensates for the "I R" loss in the motor (See Chapter Two).

Maximum torque can be achieved throughout the operating range by boosting the voltage at low speeds to maximum. This tends to cause heating in the motor and forced cooling may become necessary if the drive is to be used continually at low output frequencies from 0 Hz to 20 Hz .

The specification given for the drive are standard for most similar A.C. drives and needs no real explanation.

Chapter 11

Conclusion

The Development of the drive appears to be a success in both its development and operation. Pending the following points:

1. The Drive was demonstrated to Mr P.H. Kleinhans (Mentor) and other Lecturing Staff members of the School of Electrical Engineering at the Cape Technikon during October 1991.

2. A Dissertation pertaining to the development and performance of the drive was held at the Technikon during November 1991 for the Lecturing Staff and interested Parties.

3. The contents of this Thesis.

The prior stated objectives have been reached i.e.:

1. To build a "Low Power" Micro Processor based A.C. Drive for an Induction Motor with locally available components.

2. To obtain the necessary knowledge for designing and the construction of an A.C. drive.

11.1 Drive Conclusion

1. This drive enabled the A.C. Motor to operate in the constant torque region between 0 Hz to 50 Hz and from 50 Hz to 100 Hz in the constant Power region.

2. The drive construction and components are relatively inexpensive.

3. No negative performance results were recorded during tests as compared to other similar A.C. drives.

4. Cognisance must be taken that this drive will be further enhanced according to field application requirements.

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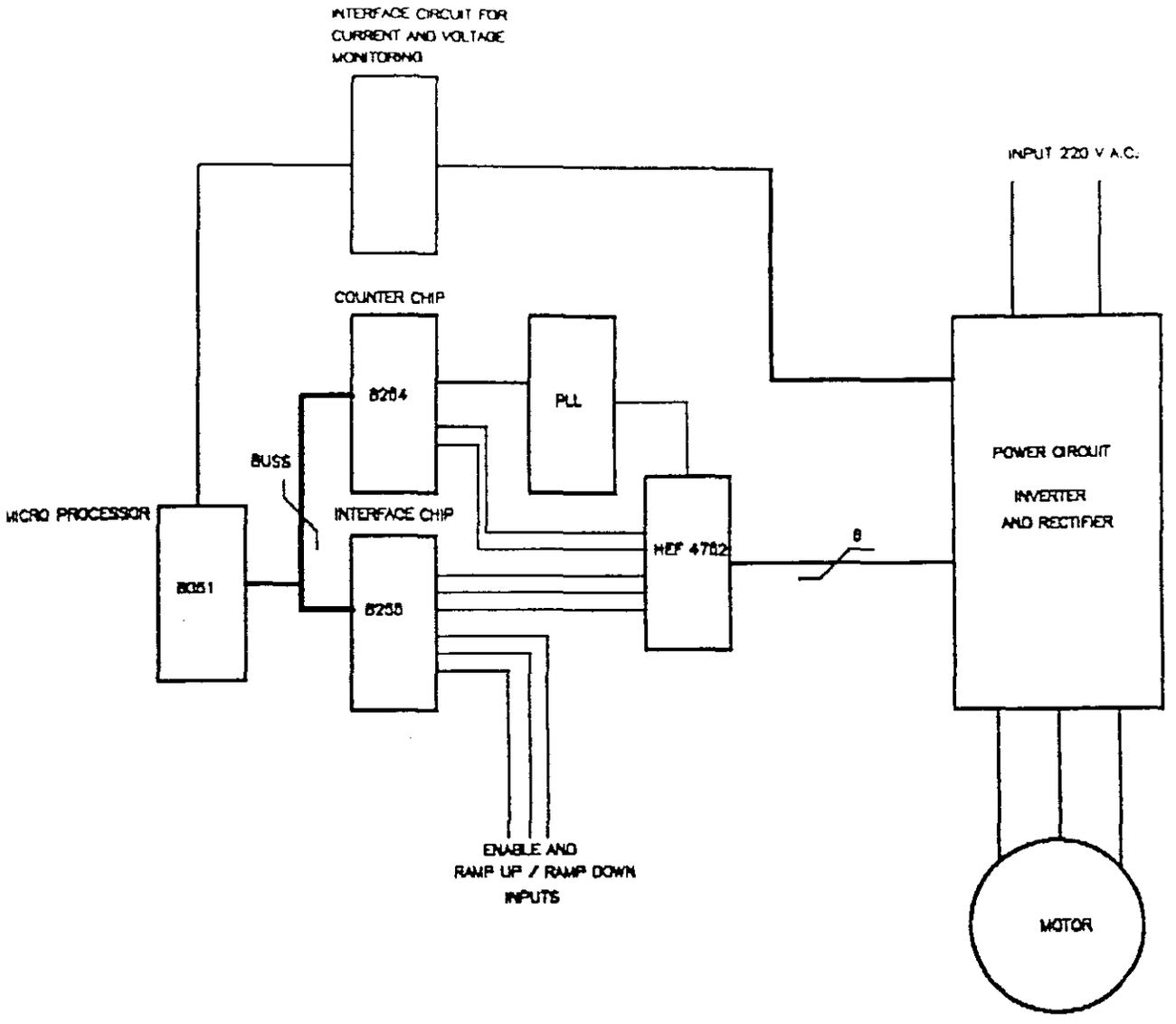
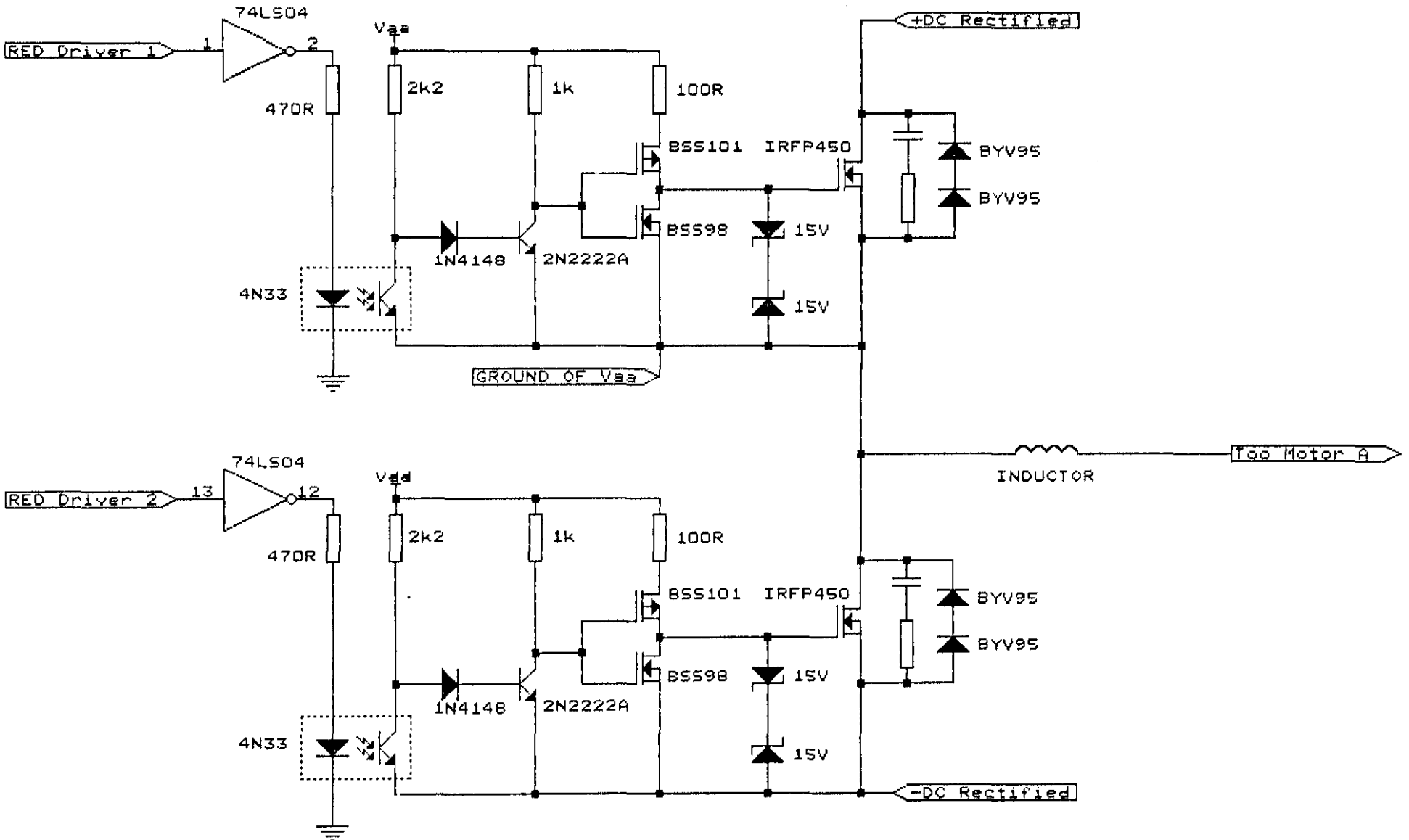
P.B. Prest, J.D. van Wyk, J.Schults and C.F. Landy

The Transaction of the S.A. Institute of Electrical Engineering March 1990

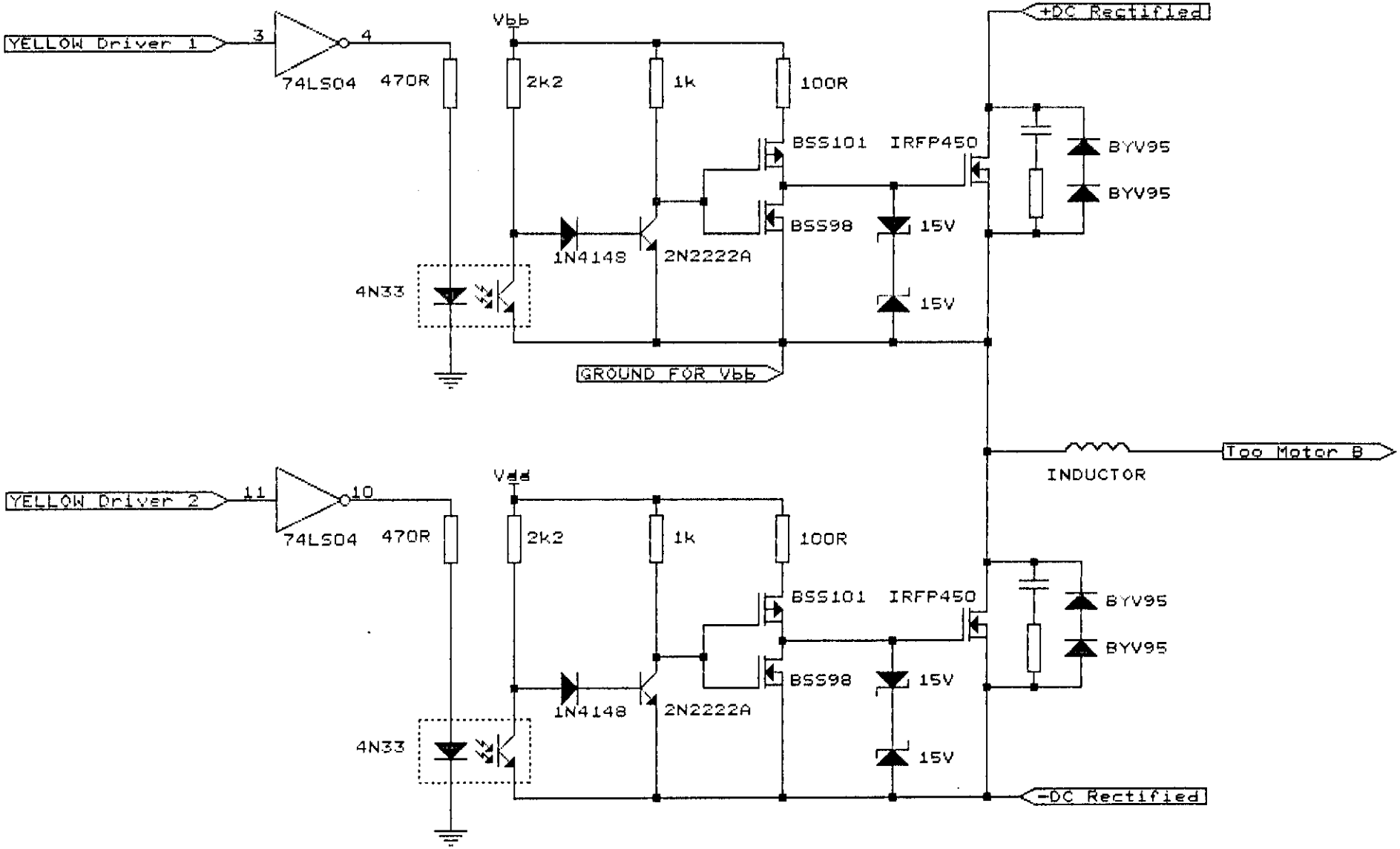
Appendix A

A.1 Circuit Diagrams

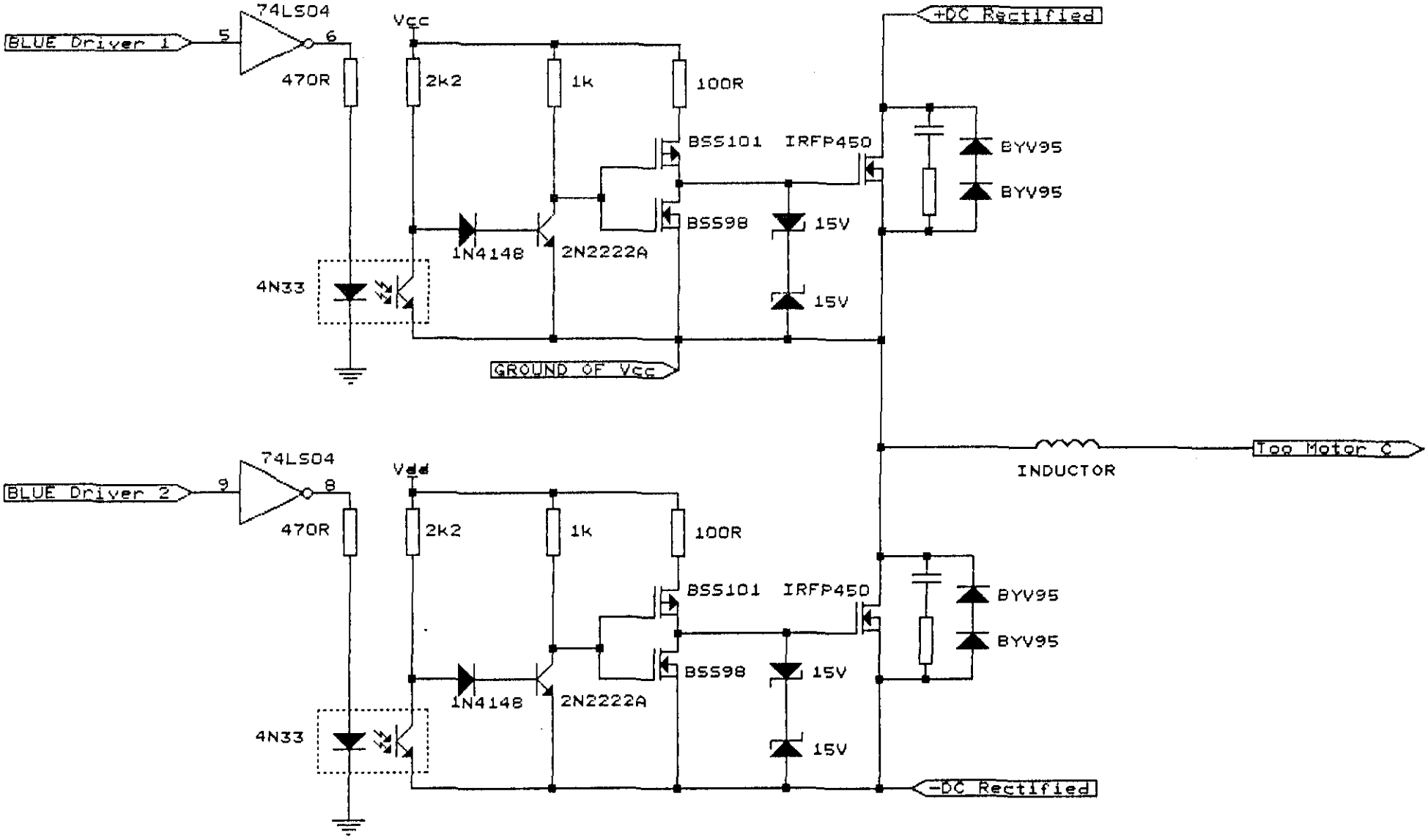

INTERFACE CIRCUIT FOR
CURRENT AND VOLTAGE
MONITORING
INPUT 220 V A.C.
COUNTER CHIP
8284
PLL
BUSS
MICRO PROCESSOR
INTERFACE CHIP
8051
8255
HEF 4752
8
POWER CIRCUIT
INVERTER
AND RECTIFIER
ENABLE AND
RAMP UP / RAMP DOWN
INPUTS
MOTOR



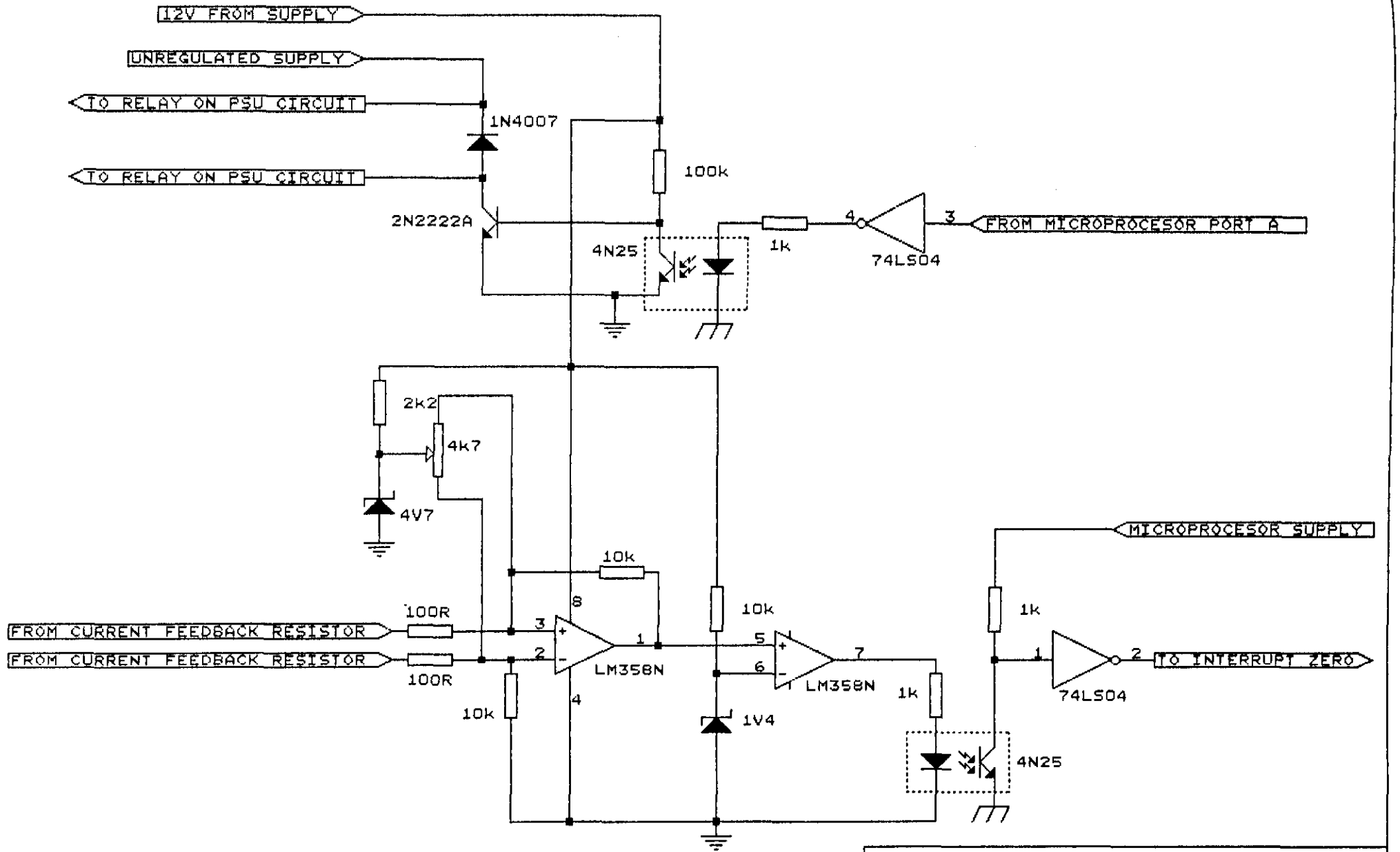
J.BAIRD		
Title: INVERTER LEG 1		
Size: A	Document Number	REV: 2
Date: February 22, 1992	Sheet 1 of 3	



J.BAIRD		
Size A	Document Number	REV 2
Date: February 22, 1992	Sheet 2 of 3	



J.BAIRD		
Title: INVERTER LEG 3		
Size: A	Document Number:	REV: 2
Date: February 22, 1992	Sheet 3 of 3	



J.BAIRD		
Title: INTERFACE CIRCUIT		
Size: A	Document Number	REV: 2
Date: February 22, 1992	Sheet 1 of 1	

SUB-RACK BUS

8255
D0 D1 D2 D3 D4 D5 D6 D7
RD WR A0 A1 RESET CS
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7
PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7

VCC

74193 ×3
A B C D QA QB QC QD UP DN LOAD CLR CO BO

8284
510R
10MHz
510R
X1 X2 RDY1 RDY2 AEN1 AEN2 EFI CSYNC ASYNC F/C RES
READY CLK RESET PCLK OSC

82C54
D0 D1 D2 D3 D4 D5 D6 D7 RD WR A0 A1 CS
CLK0 G0 OUT0 CLK1 G1 OUT1 CLK2 G2 OUT2
Vcc

VCC
4k7
82p
74LS123
CEXT REXT/CEXT A B CLR Q

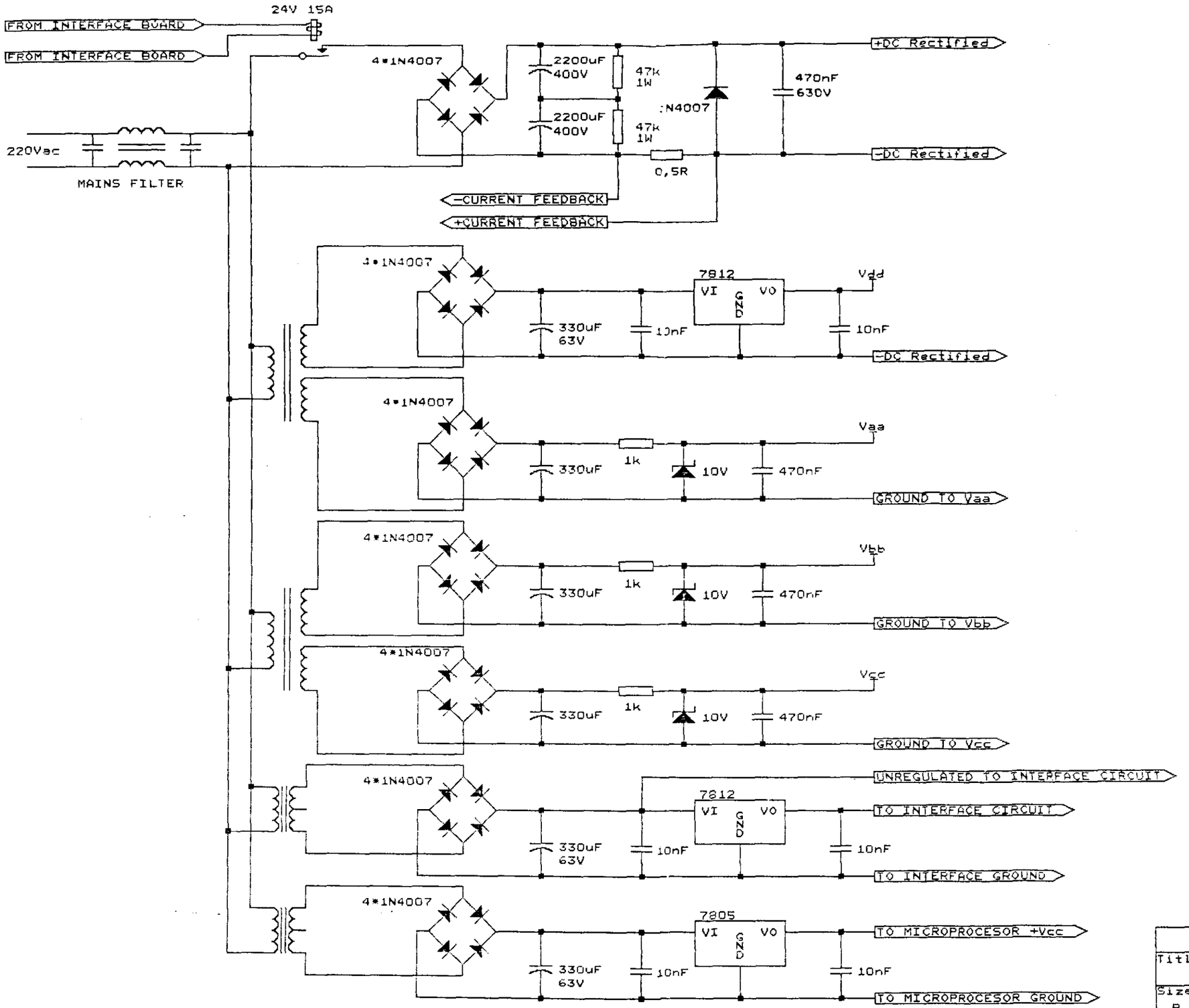
74LS74 ×2
D P R CLK C L Q

VCC
3k9
330p
4046
R2 R1 INH CX VCOIN ZEN DEMO CX SIN VCOUT CIN PD1 PD2
1M
1u
5k

VCC
HEF4752
FCT RCT VCT OCT LKIABC ORM1 ORM2 OYM1 OYM2 OBM1 OBM2 CW

TO INVERTER

J.BAIRD		
Title: INVERTER INTERFACE		
Size: B	Document Number	REV: 2
Date: February 22, 1992	Sheet 1 of 1	



J.BAIRD		
Title: POWER SUPPLY UNITS		
Size: B	Document Number	REV: 2
Date: February 22, 1992	Sheet: 1 of 1	

A.2 KIB Micro Controller Board Details

B2 CONNECTOR PINOUTS

B2.1 J1 - DIN 41612 EDGE CONNECTOR

	GND	A	1	C	GND
	+5V		2		+5V
	+12V/21,5V		3		−12V/21,5V
	$\overline{\text{CS-EF00H/LCD}}$		4		TTL SERIAL IN (CONSOLE) P3 0
	$\overline{\text{CS-EE00H}}$		5		$\overline{\text{PRGM ENABLE}}$ (P1.5)
	$\overline{\text{CS-ED00H}}$		6		$\overline{\text{PRGM\_PULSE}}$ (P1.4)
8255	$\overline{\text{CS-EC00H}}$		7		TIMER 1 IN (P3.5)
8254	$\overline{\text{CS-EB00H}}$		8		TIMER 0 IN (P3.4)
	$\overline{\text{CS-EA00H}}$		9		INT1 (P3.3)
IP/ 8255	$\overline{\text{CS-E900H}}$		10		$\overline{\text{PWM}}$ (P1.2)
	$\overline{\text{INT0/DMA-REQ}}$		11		$\overline{\text{DMA-ACK}}$ (P1.6)
	P1.1/TIMER 2 TRIG/WD-RST		12		RESET
	GND		13		GND
	ALE		14		$\overline{\text{PSEN}}$
	AD7		15		A0
	AD6		16		A1
	AD5		17		A2
	AD4		18		A3
	AD3		19		A4
	AD2		20		A5
	AD1		21		A6
	AD0		22		A7
P1.7	TTL PRINTER OUT		23		A8
P3 1	TTL-SERIAL-OUT (CONSOLE)		24		A9
	TIMER2-IN /P1.0		25		A10
	NO CONNECTION		26		A11
	$\overline{\text{OE}}$		27		A12
	$\overline{\text{RD}}$		28		A13
	$\overline{\text{WR}}$		29		A14
	DO NOT USE		30		A15
	+ 5V		31		+ 5V
	GND	A	32	C	GND

B2.2 J2 - 26 PIN DIL CONNECTOR (3 X 8 BIT PORTS)

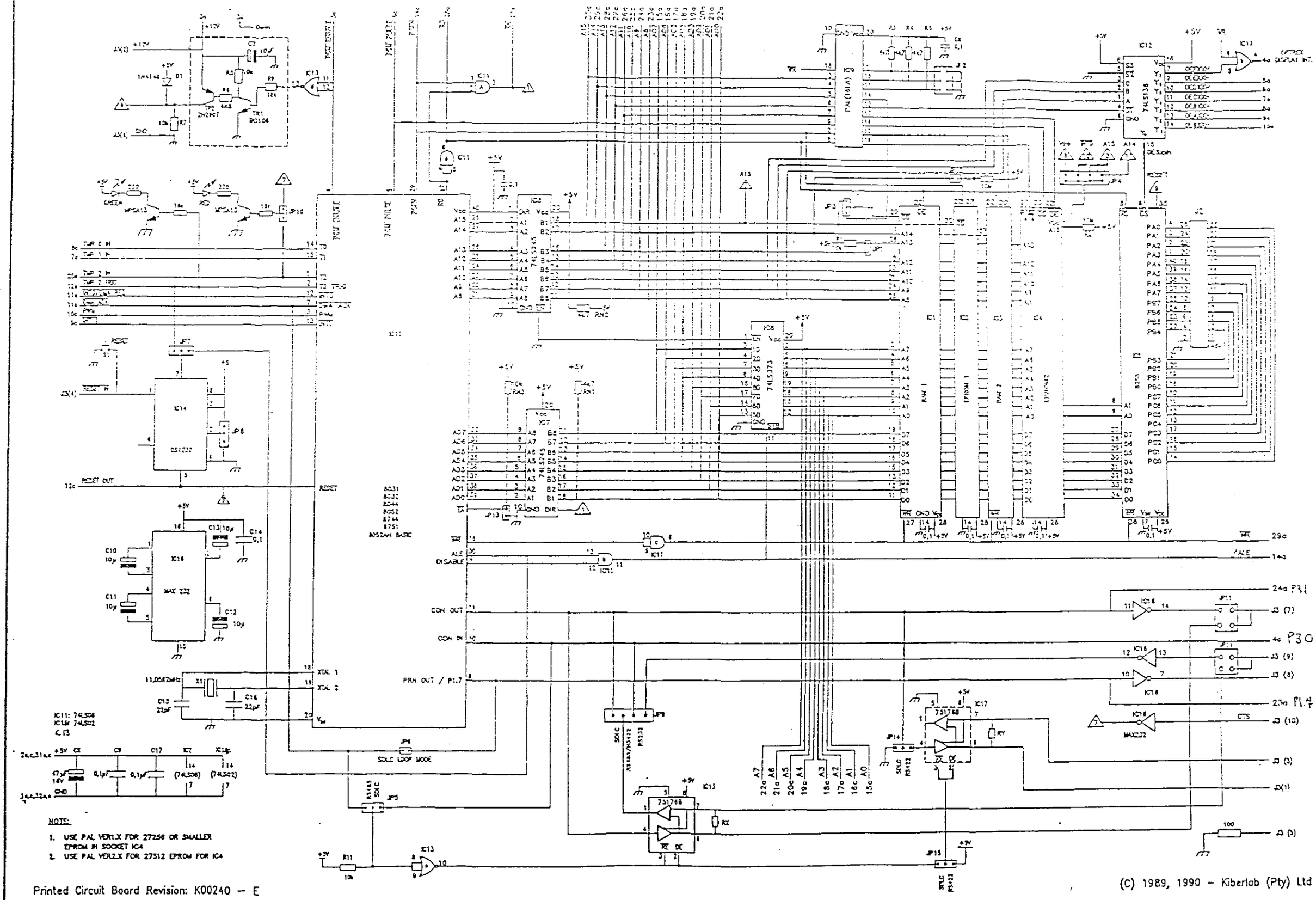
+5V	1	2	GND
PB3	3	4	PB4
PB2	5	6	PB5
PB1	7	8	PB6
PB0	9	10	PA7
PC7	11	12	PA7
PC6	13	14	PA6
PC5	15	16	PA5
PC4	17	18	PA4
PC3	19	20	PA3
PC2	21	22	PA2
PC1	23	24	PA1
PC0	25	26	PA0

PAX - PORT A
PBX - PORT B
PCX - PORT C

B2.3 J3 - 10 PIN DIL CONNECTOR

2	+12V	-	EXTERNAL INPUT: +12,5V 21,5V EPROM PROGRAMMING VOLTAGE
6	GND	-	GROUND (OV)
4	RST	-	EXTERNAL RESET SIGNAL (INPUT)
7	CTX	-	CONSOLE PORT OUTPUT (RS 232) - OR "B" LINE FOR RS485 (HDLC) - - OR RX "B" LINE FOR RS422
9	CRX	-	CONSOLE PORT - INPUT (RS 232) - OR "A" LINE FOR RS485 (HDLC) - - OR RX "A" LINE FOR RS422
8	PTX	-	PRINTER PORT (RS 232 - BASIC)
10	CTS	-	RS 232 STATUS INPUT LINE
3	A LINE	-	RS 422 TX
1	B LINE	-	RS 422 TX
5		-	HIGH IMPEDANCE GROUND FOR RS 485

64 WAY EDGE CONNECTOR
A 1 C
A 32 C
J1
KIB54 CONTROLLER
IC6
IC1 8/32k RAM
C1
JP1
JP12
C2
IC12
C8
C9
RN1
IC10 CPU
IC7
IC2 EPROM 8-32K
IC13
R11
RN3
RN2
IC8
IC3 8/32k RAM
R1
C3
JP6
C17
IC14
JP5
R2
IC4 PROM PROG.
D2
D3
C4
C16
R13
R14
JP8
JP7
A2
TR4
TR3
JP9
XTAL1
IC11
IC9 PAL
A3
JP3
JP2
R12
R3
L2
JP4
IC15
RX
R9
R4
R5
R6
R7
TR2
TR1
JP10
R16
C12
C3
C7
C6
R8
D1
R15
C10
C13
IC16
IC17
8255 PIA IC5
C14
C5
R17
RY
JP11
J3
SERIAL PORT
RESET SW
26p PIA CON.
J2



Printed Circuit Board Revision: K00240 – E

REV	DATE	SIGN	REV	DATE	SIGN	DATE	88-12-19
1.1	1989-08-21	EL	1.6	1990-05-01		DRAWN	EL
1.2	1989-10-18	EL				CHECKED	DvR
1.3	1989-10-31	DdR				APPR.	DvR
1.4	1990-02-07	DdR				SCALE	NTS
1.5	1990-03-02	DdR					

TITLE: KIB54 CONTROLLER

CUSTOMER: KIBERLAB

KIBERLAB (PTY) LTD

PROJ NO: 111

DWG NO: R01275

SHT 1 OF 1

A.3 Protection Calculations

di/dt

For full derivation of formulas see ref. [1] and [4].

Snubber current

$$L\ di/dt + Ri + 1/c\int idt + Vc = Vs$$

Input voltage $Vs = 311$ Volts

$L \approx 50\mu H$ (motor inductance)

Let $R = .47\ \Omega$

$C = 0{,}047\mu F$

From Ref [4] $$WO = \frac{10^6}{\sqrt{50 \times 0{,}047}} = 652 \text{ rad/s}$$

$$\delta = \frac{47}{2} \times \sqrt{\frac{0{,}047}{50}} = 0{,}288 \text{ rad/s}$$

$$W = 652\sqrt{1-0{,}288^2} = 597 \text{ rad/s}$$

Vpeak across the device

$$Vp = 311\ (1 + e^{-\alpha t_1}) \qquad \alpha t_1 = \frac{\delta}{\sqrt{1-\delta^2}} \tan^{-1} \frac{-2\delta\sqrt{1-\delta^2}}{1-2\delta^2}$$

$Vp = 335$ Volts

but power dissipated is given by ref [1]

$$Ps \simeq \tfrac{1}{2} C_x Vd^2 f$$

Maximum switching = 2KMz

$C = 0{,}047\mu F$

$Vd = 335$

$$Ps \approx \tfrac{1}{2}\ 0{,}047\mu F \cdot 335^2 \cdot 2KHz$$

$$\approx 5{,}25 \text{ Watts}$$

A.4 Thermal Considerations

Max current 10 Amps

Max on time 1mSec

Ref specifications

$$P = \frac{Tj\ max - 25}{\theta eff\ (tp\ D)} \qquad [1]$$

$$= \frac{150°C - 25}{0,8}$$

$$\therefore = 156\ Watts \qquad O.K.$$

Without heat sink device can handle 6 Amps pulsed at 1m-second pulses.

The heat sink used has a high efficiency rate and is more than adequate for the design.

A.5 Software

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs. Junction Temperature

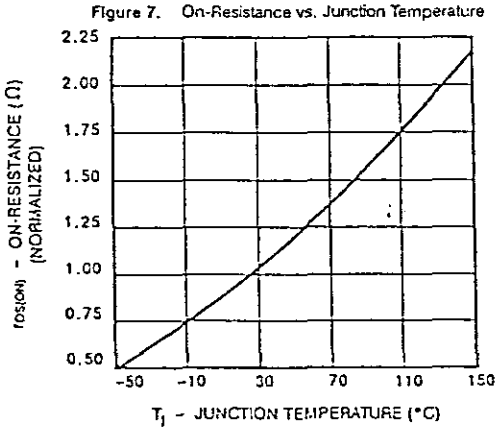
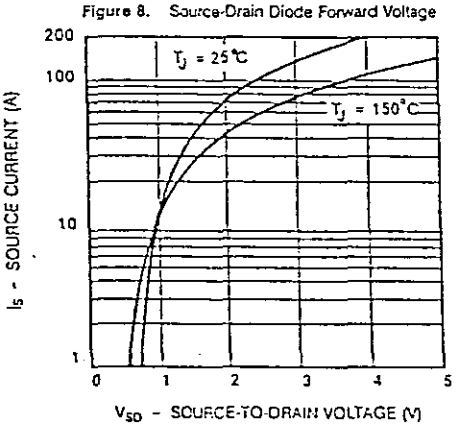


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

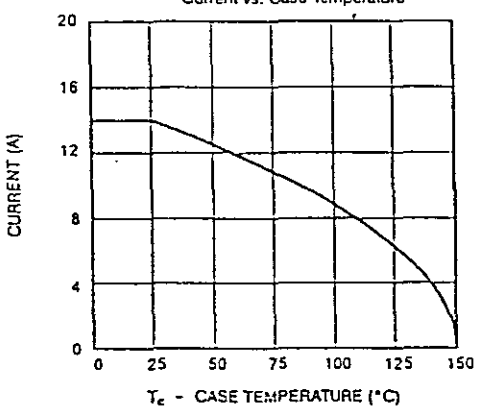
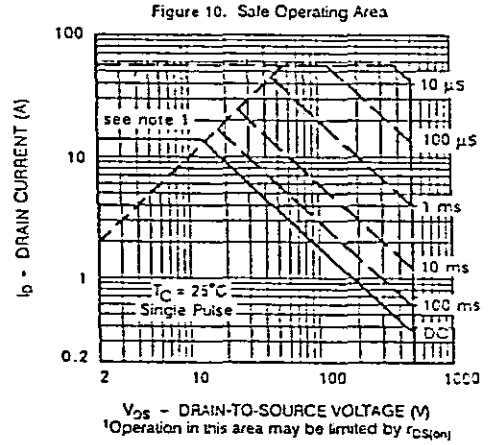
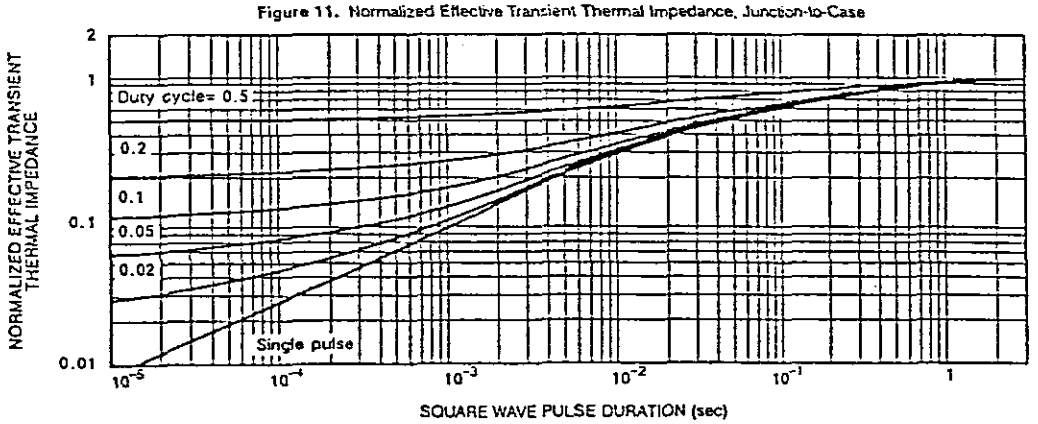


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



```
OOS 3.30 (038-N) MCS-51 MACRO ASSEMBLER, V2.2
OBJECT MODULE PLACED IN B:\PLL4752.08J
ASSEMBLER INVOKED BY:  C:\8051\51ASM\ASM51.EXE B:\PLL4752.A51


LOC  08J           LINE     SOURCE

                     1      $TITLE (8051 CONTROL OF THE HEF 4752 USING THE 8254 COUNTER CHIP AND A PLL NO FEEDBACK)
                     2      $NOMOD51
                     3      $NOLIST
                   152      ;
                   153      ;
                   154      OSEG
                   155      ;_____________________________________
                   156      ;       SPECIAL PORT FUNCTIONS        ;
                   157      ;-------------------------------------
                   158      ;RE_SET FOR 4752 ON 8255 PORT B-1  AT LOCATION OFFBXX
                   159      ;CW             :FOR 4752 ON 8255 PORT B-2  AT LOCATION OFFBXX
                   160      ;S_S             FOR 4752 ON 8255 PORT B-0  AT LOCATION OFFBXX
                   161      ;
                   162      ; _____________________________________
                   163      ;|      PORT OUTPUT BIT ALLOCATION    |
                   164      ; -------------------------------------
                   165      ;
                   166      ;       D_BRAKE BIT     P1.5    ;PWM USED TO PULSE RESTOR FOR DYNAMIC BRAKE NO IN USE UNTIL
                            L WE HAVE NEED FORCED BRAKING
                   167      ;
                   168      ;
                   169      ; ____________________________________________________
                   170      ;|     INPUT BIT ALLOCATION FOR PROGRAMING SCRATCH PATCH |
                   171      ; ----------------------------------------------------
                   172      ;
  0009             173              FW_SP   BIT     21H.1   ;FASTER FORWARD/REVERSE
  000A             174              RE_SP   BIT     21H.2   ;SLOWER FORWARD/REVERSE
  0008             175              FW_RE   BIT     21H.0   ;FORWARD / REVERSE
  000B             176              ST_GO   BIT     21H.3   ;STOP / GO
                   177      ; _____________________________
                   178      ;|      INPUT PORT ALLOCATION  |
                   179      ; -------------------------
  0096             180              SPEED   BIT     P1.6            ;SPEED INPUT FROM SHAFT ENCODER
  0097             181              OC_LINK BIT     P1.7            ;OC LINK FEEDBACK
                   182      ; ___________________________
                   183      ;|      OTHER BIT ALLOCATIONS   |
                   184      ; ---------------------------
                   185      ;
  0000             186              C_ONT   BIT     20H.0   ;CONTINUE IF SET FORM TIMER
  0001             187              R_LEASE BIT     20H.1   ;HAS DRIVE BEEN RELASED
                   188      ;
                   189      ;
----               190      CSEG
0000               191              ORG     0000H
0000 020040        192              JMP     MAIN
                   193      ;
0003               194              ORG     0003H
0003 02017E        195              JMP CURRENT     ;IF CURRENT EXCEEDS MAXIMUM THEN SHUT DOWN
                   196      ;
0008               197              ORG     0008H
```

```
LOC  OBJ            LINE     SOURCE

0008 020184           198            JMP     WAIT
                      199     ;
0033                  200            ORG     0033H
0033 020138           201            JMP     PAC_INT ;SERVICE THE PAC: 1) RAMP UP TIME
                      202     ;
0040                  203            ORG     0040H
                      204            MAIN:
                      205     ;
                      206     ; -------------
                      207     ;| MAIN PROGRAM |
                      208     ; -------------
                      209     ;
0040 C290             210            CLR     P1.0
0042 1200F7           211            CALL P_SET      ;SET UP AND CLEAR 8255 PORTS
0045 7820             212            MOV   . R0,#20H ;LOW BYTE OF PLL
0047 7900             213            MOV     R1,#00H ;HIGH BYTE OF PLL
0049 120120           214            CALL    L_OAD   ;LOADS THE 8255
004C    0E7           215            CALL COUNT_0    ;SET UP REF CLOCK
004F 1200C7           216            CALL    COUNT_2 ;SET UP VCT CLOCK - CHANGE LOAD VALUE IF BOAST IS REQUIRED
0052 1200D7           217            CALL COUNT_1    ;SET UP FCT
0055 120177           218            CALL I_SET      ;INPUT SETUP FROM SECOND 8255
0058 120104           219            CALL S_TIMER '          -
005B D288             220            SETB    IT0             ;EDGE TRIGGER INT0
005D D2A8             221            SETB    EX0             ;ENABLE INTERRUPT
005F D290             222            SETB    P1.0
0061 1201A0           223            CALL    TIMER
                      224     R:
0064 300906           225          . JNB     FW_SP,CO_NT2
0067 300A03           226            JNB     RE_SP,CO_NT2
006A 02018A           227            JMP     SHUT_DOWN
                      228     CO_NT2:
0060 90F800           229            MOV     DPTR,#0F800H
0070 E0               230            MOVX '  A,@DPTR
0071 F521             231            MOV     21H,A
0073 3008EE           232            JNB     ST_GO,R ;IF PORT PIN NOT SET THEN DO NOT RELASE
0076 300808           233            JNB     FW_RE,REVERSE
0079    1             234            MOV     A,#01H
0078 12012F           235           ,CALL    L_OAD2
007E 020086           236            JMP     RUN
                      237     REVERSE:
0081 7405             238            MOV     A,#05
0083 12012F           239            CALL    L_OAD2
                      240     RUN:
0086 D2AF             241            SETB    EA
0088 D2AE             242            SETB    EC      ;ENABLE PAC
008A C293             243            CLR     CEX0    ;ENABLE PAC
                      244     RUN2:
008C 120120           245            CALL    L_OAD
008F 300906           246            JNB     FW_SP,CO_NT
0092 300A03           247            JNB     RE_SP,CO_NT
0095 02018A           248            JMP     SHUT_DOWN
                      249     CO_NT:
0098 90F800           250            MOV     DPTR,#0F800H
0098 E0               251            MOVX    A,@DPTR
009C F522             252            MOV     22H,A
```

```
LOC  OBJ            LINE    SOURCE

009E 6521            253            XRL     A,21H
00A0 30E003          254            JNB     0E0H.0,CONTINUE
00A3 020081          255            JMP     D_EC
                     256    CONTINUE:
00A6 30E303          257            JNB     0E0H.3,CONT_NUE
00A9 020081          258            JMP     D_EC
                     259    CONT_NUE:
00AC 852221          260            MOV     21H,22H
00AF 8008            261            JMP     RUN2
                     262    D_EC:
0081 752104          263            MOV 21H,#04H
0084 120120          264            CALL L_OAD
0087 B900F7          265            CJNE    R1,#00H,D_EC
008A B820F4          266            CJNE    R0,#20H,D_EC
008D 752100          267            MOV     21H,#00H
00C0 7400            268            MOV     A,#00H
00C2 12012F          269            CALL    L_OAD2
00C5 80              270            JMP     R
                     271    ;
                     272    ;_____________________
                     273     COUNT_2:       ;SET REF CLOCK !
                     274    ;-----------------------
                     275
00C7 90F803          276            MOV     DPTR,#0F803H    ;CONTROL WORD
00CA 7487            277            MOV     A,#087H
00CC F0              278            MOVX    @DPTR,A
00CD 90F802          279            MOV     DPTR,#0F802H    ;COUNT VALUE
0000 7419            280            MOV     A,#19H
0002 F0              281            MOVX    @DPTR,A
0003 7400            282            MOV     A,#00H
0005 F0              283            MOVX    @DPTR,A
0006 22              284    RET
                     285    ;
                     286    ;_________________
                     287    COUNT_1:        ;SET VCT !
                     288    ;-----------------
                     289    ;
0007 90F803          290            MOV     DPTR,#0F803H    ;CONTROL WORD
000A 7477            291            MOV     A,#77H
000C F0              292            MOVX    @DPTR,A
000D 90F801          293            MOV     DPTR,#0F801H    ;COUNT VALUE
00E0 7424            294            MOV     A,#24H          ;CHANGE THIS VALUE TO BOOST VOLTAGE AT LOW SPEEDS
00E2 F0              295            MOVX    @DPTR,A
00E3 7400            296            MOV     A,#00H
00E5 F0              297            MOVX    @DPTR,A
00E6 22              298    RET
                     299    ;
                     300    ;_____________________________________
                     301    COUNT_0:        ;SET MIN STEP FOR PLL FOR VCT !
                     302    ;-------------------------------------
                     303    ;
00E7 90F803          304            MOV     DPTR,#0F803H    ;CONTROL WORD
00EA 7437            305            MOV     A,#037H
00EC F0              306            MOVX    @DPTR,A
00ED 90F800          307            MOV     DPTR,#0F800H    ;COUNT VALUE
```

```
LOC  OBJ            LINE     SOURCE

00F0 74FF            308            MOV     A,#0ffH
00F2 F0              309            MOVX    @DPTR,A
00F3 74F0            310            MOV     A,#0f0H
00F5 F0              311            MOVX    @DPTR,A
00F6 22              312     RET
                     313     ;
                     314     ;_____________________________
                     315     P_SET:  ;SET UP CONTROLLING 8255 ;
                     316     ;-----------------------------
                     317     ;
00F7 90FC03          318            MOV     DPTR,#0FC03H    ;CONTROL WORD
00FA 7480            319            MOV     A,#80H
00FC F0              320            MOVX    @DPTR,A
00FD 90FC01          321            MOV     DPTR,#0FC01H    ;4752 CONTROLL
0100 7400            322            MOV     A,#00H
0102 F0              323            MOVX    @DPTR,A
0103 22              324     RET
                     325     ;
                     326     ;_____________________________________________
                     327     S_TIMER:        ;SET TIMER 0 AND TIMER 1 TO 16 BIT TIMER  ;
                     328     ;-----------------------------------------------
                     329     ;
0104 758922          330            MOV     TMOD,#22H       ;SET TIMER 0 TO AUTO LOAD AND TIMER 1 TO 16 BIT TIMER
0107 758C01          331            MOV     TH0,#01H        ;LOAD HIGH BYTE TIMER
010A 75DA49          332            MOV     CCAPM0,#049H
010D 75EAE8          333            MOV     CCAP0L,#232
0110 75FAE8          334            MOV     CCAP0H,#232
0113 75D840          335            MOV     CCON,#040H
0116 75D900          336            MOV     CMOD,#00H
0119 75F900          337            MOV     CH,#00H
011C 75E900          338            MOV     CL,#00H
011F 22              339     RET
                     340     ;
                     341     ;_______
                     342     L_OAD: ;|
                     343     ;-------
0120    .E           344            CLR     EC
0122 90FC02          345            MOV     DPTR,#0FC02H    ;HIGH BYTE PLL
0125 E9              346            MOV     A,R1
0126 F0              347            MOVX    @DPTR,A
0127 90FC00          348            MOV     DPTR,#0FC00H    ;LOW BYTE PLL
012A E8              349            MOV     A,R0
0128 F0              350            MOVX    @DPTR,A
012C D2AE            351            SETB    EC
012E 22              352     RET
                     353     ;_______
                     354     L_OAD2:;|
                     355     ;-------
012F C2AF            356            CLR     EA
0131 90FC01          357            MOV     DPTR,#0FC01H    ;HIGH BYTE PLL
0134 F0              358            MOVX    @DPTR,A
0135 D2AF            359            SETB    EA
0137 22              360     RET
                     361     ;
                     362     ;_________________________
```

```
LOC  OBJ            LINE     SOURCE

                     363     PAC_INT:        ;PAC INT ROUTINE  ;
                     364     ;-------------------------
                     365     ;
0138 100801          366             JBC     CCF0,JUMP_PAC0  ;MODULE ZERO RAMP UP TIMER
0138 32              367             RETI
                     368     ;
                     369     JUMP_PAC0:
013C C2AF            370             CLR     EA
013E C0E0            371             PUSH    ACC
0140 7460            372             MOV     A,#LOW(60000)
0142 25EA            373             ADD     A,CCAP0L
0144 74EA            374             MOV     A,#HIGH(60000)
0146 35FA            375             ADDC    A,CCAP0H
                     376     ;
0148 300912          377             JNB     FW_SP,F_NNISH
014B B90106          378             CJNE    R1,#01H,CON_I
014E B80003          379             CJNE    R0,#00H,CON_I
015#   015D          380             JMP     F_NNISH
                     381     CON_I:
0154 B8FF05          382             CJNE    R0,#0FFH,N_CARRY
0157 08              383             INC     R0
0158 09              384             INC  R1
0159 02015D          385             JMP     F_NNISH
                     386     N_CARRY:
015C 08              387             INC     R0
                     388     F_NNISH:
015D 300A12          389             JNB     RE_SP,F_NNISHED
0160 B90006          390             CJNE    R1,#00H,CONT
0163 B82003          391             CJNE    R0,#20H,CONT
0166 020172          392             JMP     F_NNISHED
                     393     CONT:
0169 B80005          394             CJNE    R0,#00H,N_BORROW
016C 18              395             DEC     R0
016D 19              396             DEC  R1
016E 020172          397             JMP     F_NNISHED
                     398     N_BORROW:
0171                 399             DEC     R0
                     400     F_NNISHED:
0172 D2AF            401             SETB    EA
0174 D0E0            402             POP     ACC
0176 32              403     RETI
                     404     ;
                     405     ;_____________________________________
                     406     I_SET:  ;8255 RESPONSIBLE FOR INPUTS;
                     407     ;-------------------------------------
                     408     ;
0177 90F803          409             MOV     DPTR,#0F803H    ;CONTROL WORD
017A 7498            410             MOV     A,#10011000B
017C F0              411             MOVX    @DPTR,A
017D 22              412     RET
                     413     ;
                     414     ;_________________
                     415     CURRENT:        ;SHUT DOWN;
                     416     ;-----------------
                     417     ;
```

```
LOC  OBJ            LINE    SOURCE

017E C2AF            418            CLR     EA
0180 C290            419            CLR     P1.0            ;DISABLE POWER
0182 7400            420            MOV     A,#00H  ;DISABLE PULSES
0184 90FC01          421            MOV     DPTR,#0FC01H    ;HIGH BYTE PLL
0187 F0              422            MOVX    @DPTR,A
                     423    LOOP:
0188 80FE            424            JMP LOOP        ;WAIT FOR RESET
                     425    ;
                     426    ;_____________________________________
                     427    SHUT_DOWN:      ;DISABLE POWER TO INVERTER¦
                     428    ;-------------------------------------
018A C290            429            CLR P1.0        ;DISABLE POWER
                     430    D_EC2:
018C 752104          431            MOV 21H,#04H
018F 3120            432            CALL L_OAD
0191 8900F8          433            CJNE    R1,#00H,D_EC2
0194 8820F5          434            CJNE    R0,#20H,D_EC2
0197  100            435            MOV     21H,#00H
019A 7400            436            MOV     A,#00H
019C 312F            437            CALL    L_OAD2
                     438    LOOP2:
019E 80FE            439            JMP LOOP2
                     440    ;
                     441    ;_____________________________
                     442    TIMER:  ;SETTLING TIME OUT  ¦
                     443    ;-----------------------------
                     444    ;
01A0 D28C            445            SETB    TR0             ;RUN TIMER
01A2 D2AF            446            SETB    EA
01A4 D2A9            447            SETB    ET0
01A6 70F0            448            MOV     R5,#0F0H
                     449    START:
01A8 7CFF            450            MOV     R4,#0FFH
                     451    DELAY:
01AA BC00FD          452            CJNE    R4,#00H,DELAY
01AD D0F9            453            DJNZ    R5,START
01AF    .F           454            CLR     EA
01B1 C2A9            455            CLR     ET0
01B3 22              456    RET
                     457    ;
                     458    WAIT:
01B4 1C              459            DEC     R4
01B5 32              460    RETI
                     461    ;
                     462    END
```

SYMBOL TABLE LISTING
------ ----- -------

NAME	TYPE	VALUE	ATTRIBUTES
AC	B ADDR	00D0H.6	A
ACC	D ADDR	00E0H	A
B	D ADDR	00F0H	A
C_ONT	B ADDR	0020H.0	A
C_T2	B ADDR	00C8H.1	A
CCAP0H	D ADDR	00FAH	A
CCAP0L	D ADDR	00EAH	A
CCAP1H	D ADDR	00F8H	A
CCAP1L	D ADDR	00E8H	A
CCAP2H	D ADDR	00FCH	A
CCAP2L	D ADDR	00ECH	A
CCAP3H	D ADDR	00FDH	A
CCAP3L	D ADDR	00EDH	A
CCAF	D ADDR	00FEH	A
CCAP4L	D ADDR	00EEH	A
CCAPM0	D ADDR	00DAH	A
CCAPM1	D ADDR	00D8H	A
CCAPM2	D ADDR	00DCH	A
CCAPM3	D ADDR	00DDH	A
CCAPM4	D ADDR	00DEH	A
CCF0	B ADDR	00D8H.0	A
CCF1	B ADDR	00D8H.1	A
CCF2	B ADDR	00D8H.2	A
CCF3	B ADDR	00D8H.3	A
CCF4	B ADDR	00D8H.4	A
CCON	D ADDR	00D8H	A
CEX0	B ADDR	0090H.3	A
CEX1	B ADDR	0090H.4	A
CEX2	B ADDR	0090H.5	A
CEX3	B ADDR	0090H.6	A
CEX4	B ADDR	0090H.7	A
CF	B ADDR	00D8H.7	A
CH	D ADDR	00F9H	A
CL	D ADDR	00E9H	A
CMOD	D ADDR	00D9H	A
CO_NT	C ADDR	0098H	A
CO_NT2	C ADDR	0060H	A
CON_T	C ADDR	0154H	A
CONT_NUE	C ADDR	00ACH	A
CONT	C ADDR	0169H	A
CONTINUE	C ADDR	00A6H	A
COUNT_0	C ADDR	00E7H	A
COUNT_1	C ADDR	0007H	A
COUNT_2	C ADDR	00C7H	A
CP_RL2	B ADDR	00C8H.0	A
CR	B ADDR	00D8H.6	A
CURRENT	C ADDR	017EH	A
CY	B ADDR	00D0H.7	A
D_EC	C ADDR	0081H	A
D_EC2	C ADDR	018CH	A
DC_LINK	B ADDR	0090H.7	A

NAME	TYPE	VALUE	ATTRIBUTES
DELAY. . .	C ADDR	01AAH	A
DPH. . . .	D ADDR	0083H	A
DPL. . . .	D ADDR	0082H	A
EA	B ADDR	00A8H.7	A
EC	B ADDR	00A8H.6	A
ECI. . . .	B ADDR	0090H.2	A
ES	B ADDR	00A8H.4	A
ET0. . . .	B ADDR	00A8H.1	A
ET1. . . .	B ADDR	00A8H.3	A
ET2. . . .	B ADDR	00A8H.5	A
EX0. . . .	B ADDR	00A8H.0	A
EX1. . . .	B ADDR	00A8H.2	A
EXEN2. . .	B ADDR	00C8H.3	A
EXF2 . . .	B ADDR	00C8H.6	A
F_NNISH. .	C ADDR	015DH	A
F_NNISHED.	C ADDR	0172H	A
F0	B ADDR	00D0H.5	A
FW_R .	B ADDR	0021H.0	A
FW_SP. . .	B ADDR	0021H.1	A
I_SET. . .	C ADDR	0177H	A
IE	D ADDR	00A8H	A
IE0. . . .	B ADDR	0088H.1	A
IE1. . . .	B ADDR	0088H.3	A
INT0 . . .	B ADDR	00B0H.2	A
INT1 . . .	B ADDR	00B0H.3	A
IP	D ADDR	00B8H	A
IT0. . . .	B ADDR	0088H.0	A
IT1. . . .	B ADDR	0088H.2	A
JUMP_PAC0.	C ADDR	013CH	A
L_OAD. . .	C ADDR	0120H	A
L_OAD2 . .	C ADDR	012FH	A
LOOP . . .	C ADDR	0188H	A
LOOP2. . .	C ADDR	019EH	A
MAIN . . .	C ADDR	0040H	A
N_BORROW .	C ADDR	0171H	A
N_CARRY. .	C ADDR	015CH	A
OV	B ADDR	00D0H.2	A
P_SET. . .	C ADDR	00F7H	A
P.	B ADDR	00D0H.0	A
P0	D ADDR	0080H	A
P1	D ADDR	0090H	A
P2	D ADDR	00A0H	A
P3	D ADDR	0080H	A
PAC_INT. .	C ADDR	0138H	A
PCON . . .	D ADDR	0087H	A
PPC. . . .	B ADDR	00B8H.6	A
PS	B ADDR	00B8H.4	A
PSW. . . .	D ADDR	00D0H	A
PT0. . . .	B ADDR	0088H.1	A
PT1. . . .	B ADDR	0088H.3	A
PT2. . . .	B ADDR	00B8H.5	A
PX0. . . .	B ADDR	0088H.0	A
PX1. . . .	B ADDR	00B8H.2	A
R_LEASE. .	B ADDR	0020H.1	A
R.	C ADDR	0064H	A

NAME	TYPE	VALUE	ATTRIBUTES
RB8. . . .	B	ADDR	0098H.2 A
RCAP2H . .	D	ADDR	00CBH A
RCAP2L . .	D	ADDR	00CAH A
RCLK . . .	B	ADDR	00C8H.5 A
RD	B	ADDR	0080H.7 A
RE_SP. . .	B	ADDR	0021H.2 A
REN. . . .	B	ADDR	0098H.4 A
REVERSE. .	C	ADDR	0081H A
RI	B	ADDR	0098H.0 A
RS0. . . .	B	ADDR	00D0H.3 A
RS1. . . .	B	ADDR	00D0H.4 A
RUN. . . .	C	ADDR	0086H A
RUN2 . . .	C	ADDR	008CH A
RXD. . . .	B	ADDR	0080H.0 A
S_TIMER. .	C	ADDR	0104H A
SADDR. . .	D	ADDR	00A9H A
SADEN. . .	D	ADDR	00B9H A
SBUF . . .	D	ADDR	0099H A
SCON . . .	D	ADDR	0098H A
SHUT_DOWN.	C	ADDR	018AH A
SM0. . . .	B	ADDR	0098H.7 A
SM1. . . .	B	ADDR	0098H.6 A
SM2. . . .	B	ADDR	0098H.5 A
SP	D	ADDR	0081H A
SPEED. . .	B	ADDR	0090H.6 A
ST_GO. . .	B	ADDR	0021H.3 A
START. . .	C	ADDR	01A8H A
T0	B	ADDR	0080H.4 A
T1	B	ADDR	0080H.5 A
T2	B	ADDR	0090H.0 A
T2CON. . .	D	ADDR	00C8H A
T2EX . . .	B	ADDR	0090H.1 A
T2MOD. . .	D	ADDR	00C9H A
TB8. . . .	B	ADDR	0098H.3 A
TCLK . . .	B	ADDR	00C8H.4 A
TCON . . .	D	ADDR	0088H A
TF0. . . .	B	ADDR	0088H.5 A
TF1. . . .	B	ADDR	0088H.7 A
TF2. . . .	B	ADDR	00C8H.7 A
TH0. . . .	D	ADDR	008CH A
TH1. . . .	D	ADDR	008DH A
TH2. . . .	D	ADDR	00CDH A
TI	B	ADDR	0098H.1 A
TIMER. . .	C	ADDR	01A0H A
TL0. . . .	D	ADDR	008AH A
TL1. . . .	D	ADDR	008BH A
TL2. . . .	D	ADDR	00CCH A
TMOD . . .	D	ADDR	0089H A
TR0. . . .	B	ADDR	0088H.4 A
TR1. . . .	B	ADDR	0088H.6 A
TR2. . . .	B	ADDR	00C8H.2 A
TXD. . . .	B	ADDR	0080H.1 A
WAIT . . .	C	ADDR	0184H A
WR	B	ADDR	0080H.6 A

```
NAME    TYPE  VALUE    ATTRIBUTES

REGISTER BANK(S) USED: 0

ASSEMBLY COMPLETE, NO ERRORS FOUND
```

A.6 HEF 4752

LSI circuit for AC motor speed control

B.G. STARR and J.C.F. van LOON

In the past, sinusoidal Pulse-Width Modulation (PWM) speed control systems for three-phase a.c. motors have been produced in a number of different forms. However, no single system has been completely satisfactory. High costs, circuit complexity, output variation with temperature, etc. have all prevented the widespread application of this potentially attractive method of a.c. motor speed control. This article describes a purpose-designed LSI circuit, type HEF4752V, which has been developed specifically for signal generation in such systems, and overcomes all the previous disadvantages. The IC is manufactured using locally-oxidised complementary MOS technology (LOCMOS) and is mounted in a standard 28-pin dual-in-line package.

This is the third in a series of articles all devoted to our a.c. motor speed control system. A general introduction to this subject is given in Refs.1 and 2, and a description of an inverter circuit developed specifically for the system is given in Ref.3.

PWM CONTROL OF A.C. MOTORS

A block diagram of our PWM speed control system is shown in Fig.1. In this system, the output waveforms from the three phases Red (R), Yellow (Y), and Blue (B) of a six-element inverter consist of sinusoidally modulated trains of carrier pulses, both edges of each pulse being modulated to give an average voltage difference between any two of the output phases which varies sinusoidally. This is illustrated in Fig.2 for a carrier wave having 15 pulses for each cycle of the inverter output.

Figure 2a shows the 15-fold carrier, Fig.2b the double-edge modulated R-phase, and Figs.2c and 2d show the double-edge modulated Y and B phases. The line-to-line voltage obtained by subtracting the Y-phase from the R-phase is shown in Fig.2e.

A detail of the double-edge modulation of a carrier wave is shown in Fig.3. Each edge of the carrier wave is modulated by a variable time δ, where δ is proportional to $\sin\alpha$, and α is the angular displacement of the unmodulated edge. The modulation of a 15-fold carrier requires a total of 30 δ values.

The modulation of the output waveforms is achieved by opening and closing the upper and lower switching elements (transistors or thyristors) in each phase of the inverter. Closing the upper element gives a high output voltage, and closing the lower element gives a low output voltage. The basic function of the PWM IC is to provide three complementary pairs of output drive waveforms which, when applied to the six-element inverter, open and close the switching elements in the appropriate sequence to produce a symmetrical three-phase output. The drive waveforms are supplied to the inverter via buffer amplifiers with isolation where necessary. The integrated circuit is completely digital, so that the repetition frequency of the PWM signal (switching frequency) is always an exact multiple of the inverter output frequency. This results in excellent phase and voltage balance and consequent low motor losses.

A 15-fold carrier multiple is used only for the highest motor speed range. To improve the pulse distribution at lower motor speeds the switching frequency is derived from higher multiples of the inverter output frequency. A hysteresis between the switching points is included to avoid jitter when operating in these regions. Typical

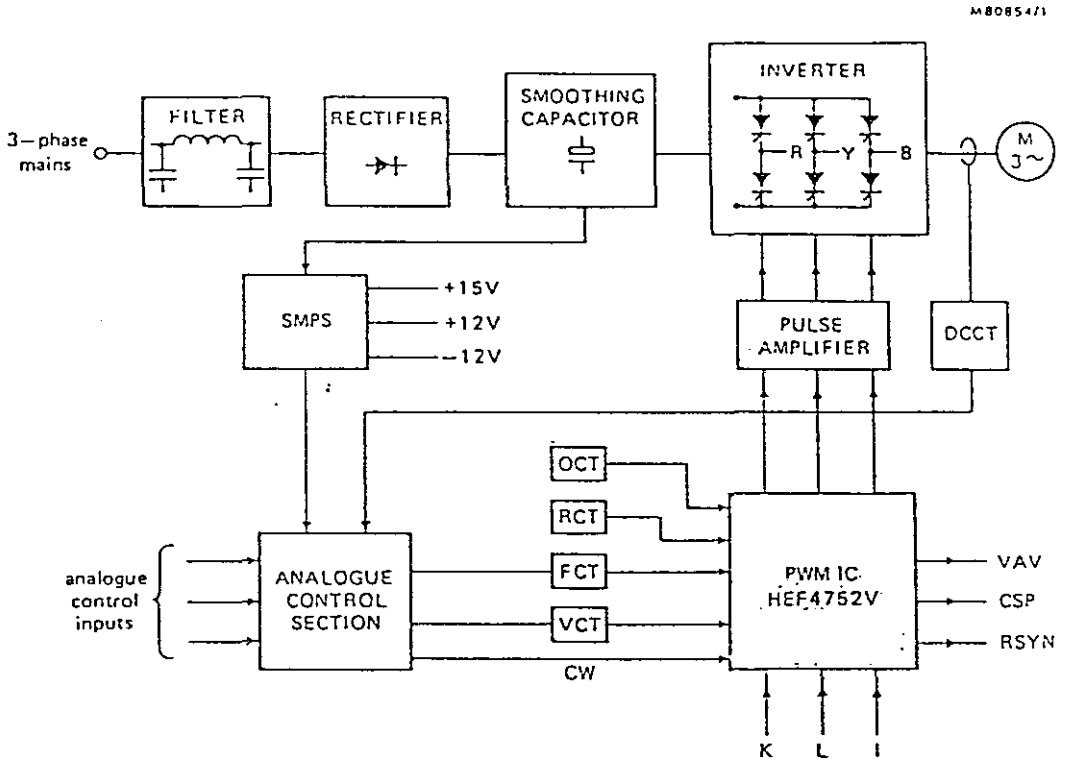


Fig.1 PWM motor control system using HEF4752V

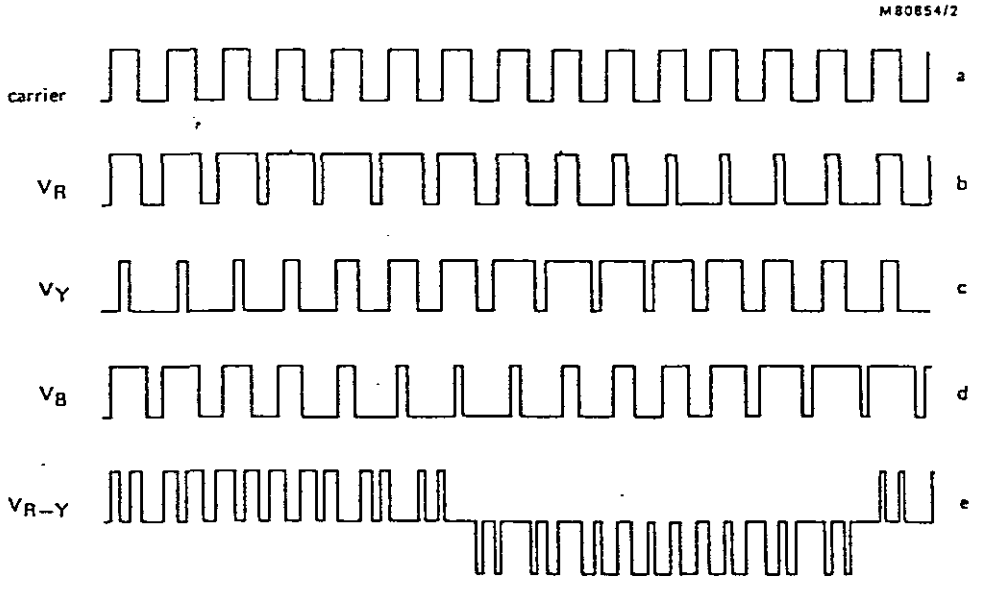


Fig.2 15-pulse sinusoidal PWM waveforms

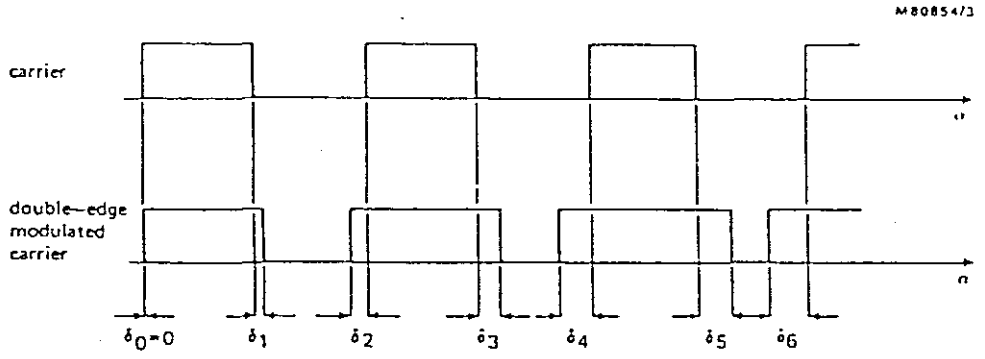


Fig.3 Detail of double-edge modulation

values of the carrier multiple and the output frequency are given in Table 1. It should be noted that this table applies only for a particular set of input conditions. The selection of input conditions is discussed later in this article.

For the values shown in Table 1, the IC has full control of the inverter switching frequency for output frequencies in the range 4.0 to 71.3 Hz. For output frequencies greater than 71.3 Hz, the switching frequency will increase beyond 1070 Hz until over-modulation is reached. Over-modulation implies a merging of adjacent pulses, with a corresponding reduction in switching frequency, until eventually a quasi-square output waveform is obtained. The point at which over-modulation occurs is determined by two of the clock inputs of the IC: VCT and FCT. This is covered in detail under the discussion of the VCT clock input. The practical upper limit on the output frequency is determined by the rating of the motor under control, the design of the inverter, and the performance of the IC. Detailed advice on the recommended maximum output frequency is also given under the discussion of the VCT clock input.

TABLE 1

Variation of carrier multiple with output frequency

Output frequency range Hz	Carrier multiple	Switching frequency Hz
0 to 4.0	168	0 to 675
4.0 to 6.4	168	675 to 1070
5.7 to 8.9	120	675 to 1070
8.1 to 12.8	84	675 to 1070
11.2 to 17.9	60	675 to 1070
16.3 to 25.5	42	675 to 1070
22.3 to 35.7	30	675 to 1070
32.5 to 51	21	675 to 1070
44.6 to 71.3	15	675 to 1070
71.3 +	15	See text

HEF4752V INTERNAL ORGANISATION

A block diagram indicating the internal organisation of the IC is shown in Fig.4. The circuit comprises three counters, one decoder, three output stages, and a test circuit. The test circuit is used primarily for testing the IC during manufacture, and is not discussed in this article. The operation of the IC is now considered in outline, and this is followed by a detailed discussion of the various input/output functions.

The three output stages (Fig.4) correspond to the R, Y, and B phases of the inverter. Each output stage has four outputs: two main outputs which control the upper and lower switching elements in each phase of the inverter, and two auxiliary outputs used to trigger commutation thyristors in 12-thyristor inverter systems. As explained above, the essential function of the IC is to provide the output waveforms which open and close the upper and lower inverter switching elements in the appropriate sequence. This is achieved by alternately switching between the upper and lower main outputs in each output stage. To ensure that the main outputs cannot be on simultaneously, an interlock delay period is used to separate the on condition of the upper and lower outputs. The interlock delay period is determined by inputs OCT and K, while the switch between the main outputs is controlled by an internally-generated control signal. A change in the level of this control signal causes the HIGH main drive output to switch off, and then after the interlock delay period, causes the LOW main drive output to switch on. With the interlock delay period fixed, variations in motor speed are produced by changes in the control signal, and a description of the production of this signal provides a basic understanding of the operation of the IC.

The control signal is derived from the carrier wave modulated by the appropriate δ values. Production of the control signal therefore requires the determination of the correct carrier frequency, and the corresponding δ modulations. The carrier frequency, which is equal to the product of the output frequency and the carrier multiple, is set by the FCT counter and the RCT counter. Dividing the clock input of the FCT counter by 3360 gives the output frequency, while the correct carrier multiple is determined by gating RCT clock pulses into the RCT counter, with a gating time equal to a fixed number of FCT clock pulses. For a given frequency of the RCT clock, the number of pulses counted in the gating time will fall as the frequency of the FCT clock increases, and this is used to derive a correspondingly lower value of the carrier multiple.

For each value of the carrier multiple, the decoder holds a corresponding set of δ values. Each δ value is

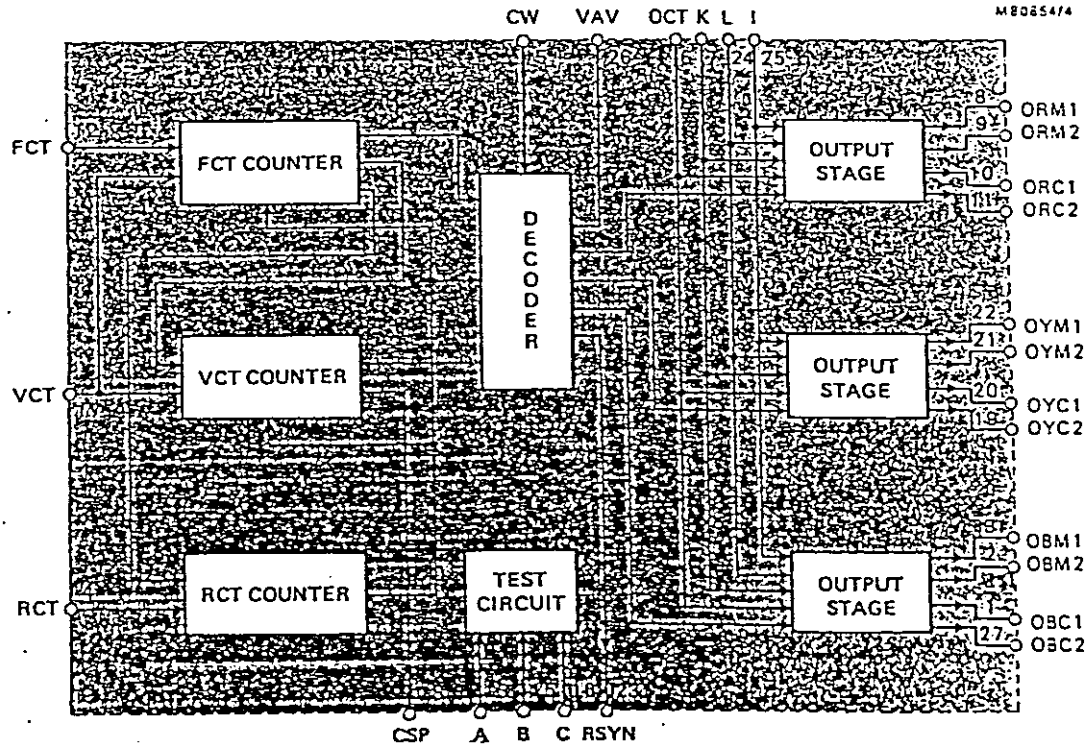


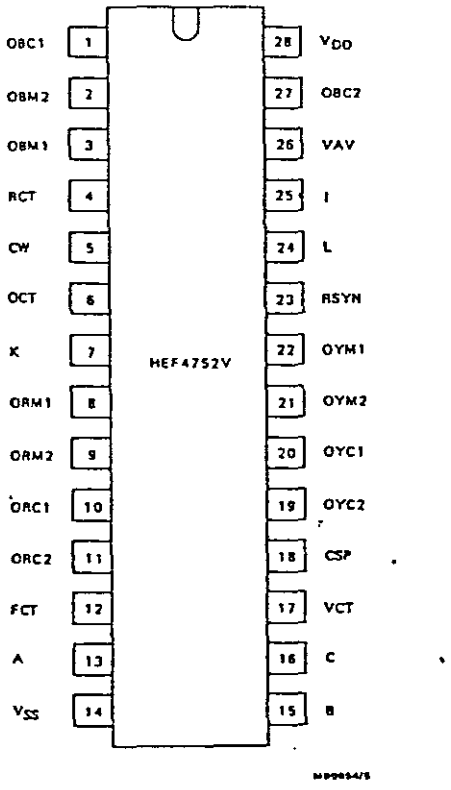
Fig.4 Block diagram of HEF4752V

stored as a number, and the width of the corresponding modulation is determined by the rate at which this number is counted. The counting frequency used is the VCT clock input, and the modulation depth is therefore inversely proportional to the frequency of the VCT clock input.

From the carrier frequency, and the δ modulations, the decoder finally assembles the control signal. A total of three control signals is produced by the decoder, one for each output stage, with a phase difference of 120° between each signal.

INPUT/OUTPUT FUNCTIONS OF THE HEF4752V

A pinning diagram of the HEF4752V IC is shown in Fig.5. The IC has 12 inverter drive outputs, three control outputs, four clock inputs, and seven data inputs.



Inverter drive signals

There are six main drive outputs which are arranged in complementary pairs. The pins are coded as follows.

First letter	O (output)
Second letter	R, Y, or B (phase indication)
Third letter	M (main)
Number	1 for output of upper switching element, or 2 for lower switching element

For example, ORM2 is the main drive waveform for the Red phase lower switching element.

Associated with each main output is the auxiliary output used to trigger the commutation thyristor in 12-thyristor inverter systems. These outputs are identified by a C as the third letter of the pin code, so that ORC2 is the commutation trigger pulse output associated with ORM2.

The inverter drive signals can be obtained in two

PINNING

Inverter drive signals		
8	ORM1	R-phase main
9	ORM2	R-phase main
10	ORC1	R-phase commutation
11	ORC2	R-phase commutation
22	OYM1	Y-phase main
21	OYM2	Y-phase main
20	OYC1	Y-phase commutation
19	OYC2	Y-phase commutation
3	OBM1	B-phase main
2	OBM2	B-phase main
1	OBC1	B-phase commutation
27	OBC2	B-phase commutation
Data inputs		
24	L	data
25	I	data
7	K	data
5	CW	data
13	A	data
15	B	data
16	C	data
Clock inputs		
12	FCT	frequency clock
17	VCT	voltage clock
4	RCT	reference clock
6	OCT	output delay clock
Control outputs		
23	RSYN	R-phase synchronisation
26	VAV	average voltage
18	CSP	current sampling pulses

Fig.5 Pinning diagram

forms, one mode for driving transistor inverters, the other for thyristor inverters. The form produced by the IC is determined by the logic level applied to the data input I.

Data inputs

Data inputs I, K, and L

As explained above, input I determines whether the inverter drive signals are in the thyristor or transistor mode. Input I LOW corresponds to the transistor mode; input I HIGH corresponds to the thyristor mode. In the transistor mode the main upper and lower switching elements in the inverter are switched HIGH alternately, with an interlock delay period (both switches LOW) at each changeover. During the delay period the commutation output associated with the off-going main output is set HIGH. The data input K, in association with the clock input OCT, is used to adjust the length of the interlock delay period. The details of this adjustment are described under the discussion of clock input OCT.

Input L provides a stop/start facility. In the transistor mode, with L LOW, all main and commutation signals are inhibited, and with L HIGH, the normal modulated block pulses continue. The action of L inhibits the actual output circuits only, so that while L is LOW the internal circuits generating the output signals continue to operate. Typical output waveforms for the transistor mode are shown in Fig.6. Figures 6a to 6d show the normal inverter drive outputs, and Fig.6e shows the internally-generated control signal which effects the transition between the upper and lower main drive outputs. Figures 6g to 6j illustrate the influence of changes in the level of input L (Fig.6f) on the inverter drive outputs.

With input I HIGH, thyristor mode, the main outputs become pulse trains with a mark-space ratio of 1:3, and the commutation outputs become a single pulse lasting for the first quarter of the interlock delay period. This is used to facilitiate the use of trigger transformers for isolation purposes. The interlock delay period is set in the same way as that used in the transistor mode, but in this case the logic level at input K and the frequency of OCT also control the frequency of the main output pulse trains, which in turn will affect the choice of trigger transformer. The delay period is selected to allow time for the commutation circuit to operate and reset in the 12-thyristor circuit, or to set the minimum pulse width for the six-thyristor self-commutated circuit. In this mode, with L LOW, the three lower switching elements in the inverter are triggered continuously, the upper elements being inhibited. Typical output waveforms for the thyristor mode are shown in Fig.7.

Data input CW

The phase sequence input CW is used to control the direction of rotation of the motor by altering the phase sequence. This is illustrated in Table 2. The phase sequences shown in Table 2 represent the order in which the phases pass through zero voltage in a positive direction.

TABLE 2

Phase sequence input CW

Input CW	Phase sequence
LOW	R, B, Y
HIGH	R, Y, B

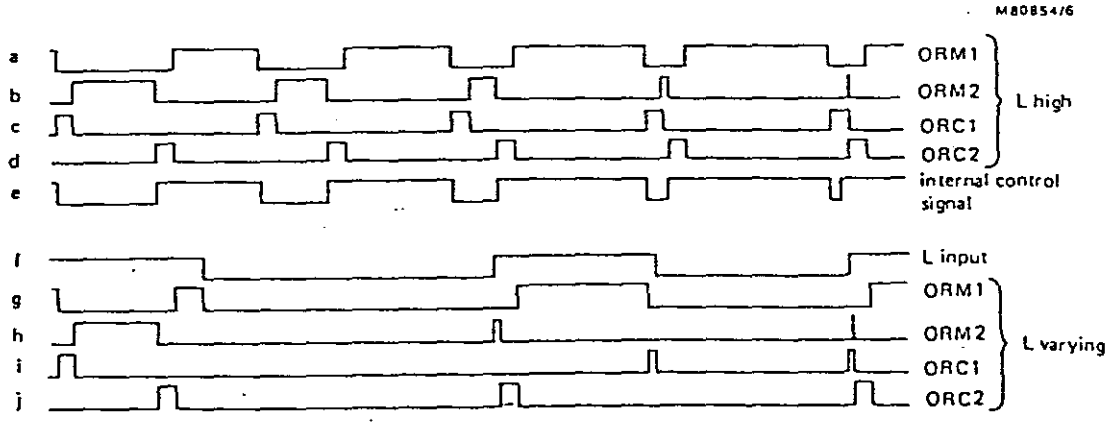


Fig.6 Typical output waveforms for transistor mode

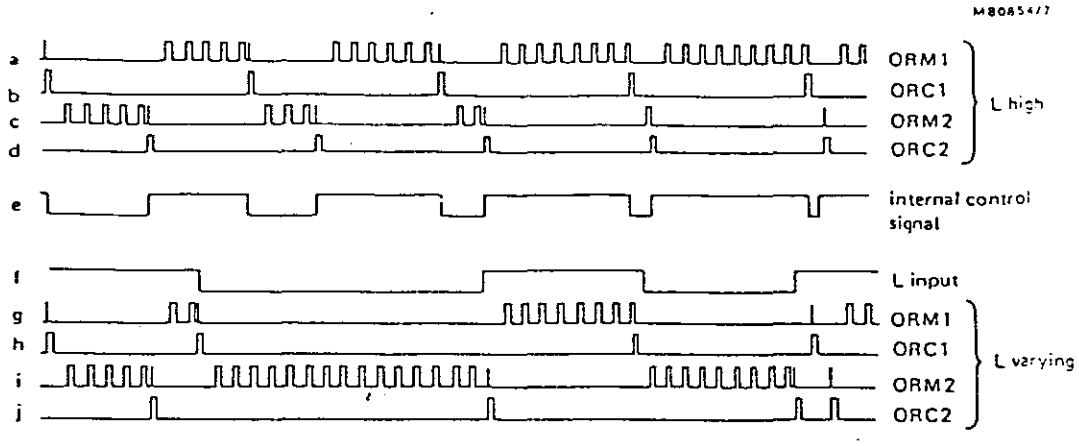


Fig.7 Typical output waveforms for thyristor mode

Data inputs A, B, and C

The three inputs A, B, and C are provided for use during production testing. They are not used during normal operation, when they must be connected to V_{SS} (0 V). Input A HIGH initiallises all the IC circuits, and can be used for reset. The use of input A is considered in detail below under the discussion of switch-on conditions.

Clock inputs

There are four clock inputs which are used to control the output waveforms. The following sections give a guide to selecting the frequency, or range of frequencies, for each clock.

Frequency control clock FCT

The clock input FCT controls the inverter output frequency f_{out}, and therefore the motor speed. The clock frequency f_{FCT} is related to f_{out} by the following equation:

$$f_{FCT} = 3360 \times f_{out}.$$

It is permissible to stop the FCT clock during system operation, the effect being to switch the outputs to either all M1 or all M2 outputs, and this occurs irrespective of the state of input I.

Voltage control clock VCT

An induction motor is governed by the general expression:

$$V = N\frac{d\Phi}{dt},$$

so that to maintain constant motor flux, the voltage-time product Vt must be kept constant. The IC automatically satisfies this requirement by making the output voltage directly proportional to the output frequency. The level of the average inverter output voltage, at a given output frequency, is controlled by the VCT clock input, changes in output voltage being achieved by varying the modulation depth of the carrier. Increasing f_{VCT} reduces the modulation depth, and hence the output voltage, while decreasing f_{VCT} has the opposite effect.

The maximum undistorted sinusoidal output voltage, which is obtainable in a given system, is determined by the voltage of the d.c. link, V_{link}; the maximum r.m.s. value of the fundamental component is given by $0.624 \times V_{link}$. This voltage occurs at 100% modulation of the carrier; that is, when some adjacent pulses are just about to merge. The output frequency at which this condition can apply in a given system is determined by the Vt product of the motor. The frequency at 100% modulation, $f_{out(m)}$, can be determined by relating the maximum r.m.s. inverter output voltage to the motor ratings as follows:

$$f_{out(m)} = f_N \times \frac{0.624\,V_{link}}{V_N},$$

where f_N is the motor rated frequency and V_N the motor rated r.m.s. voltage.

Once $f_{out(m)}$ has been established, a value of f_{VCT} can be determined which will set the Vt product correctly throughout the frequency range of the motor to be controlled. This nominal value of f_{VCT} is denoted by $f_{VCT(nom)}$, and is related to $f_{out(m)}$ by:

$$f_{VCT(nom)} = 6720 \times f_{out(m)}.$$

With f_{VCT} fixed at $f_{VCT(nom)}$, the output voltage will be a linear function of the output frequency up to $f_{out(m)}$. Any required variation in this linear relation-

ship is obtained by changing f_{VCT}. For example, to double the output voltage at low frequencies, as a possible compensation for 'IR' losses, f_{VCT} is made equal to 0.5 $f_{VCT(nom)}$.

The frequency ratio f_{FCT}/f_{VCT} is important in system design. At 100% modulation it will have a value given by:

$$\frac{f_{FCT}}{f_{VCT(nom)}} = \frac{3360 \times f_{out(m)}}{6720 \times f_{out(m)}},$$

$$= 0.5.$$

Below 0.5 the modulation is sinusoidal, while above 0.5 the phase waveform approaches a squarewave, giving a quasi-squarewave line-to-line voltage. At approximately 2.5, the full squarewave is obtained. Above 3.0, the waveform becomes unstable as the internal synchronising circuits cannot function correctly, and 3.0 is therefore the recommended limit.

Reference clock RCT

RCT is a fixed clock which is used to set the maximum inverter switching frequency $f_{s(max)}$. The clock frequency, f_{RCT}, is related to $f_{s(max)}$ by the following equation:

$$f_{RCT} = 280 \times f_{s(max)}.$$

The absolute minimum value of the inverter switching frequency, $f_{s(min)}$, is set by the IC at 0.6 $f_{s(max)}$. These figures apply provided f_{FCT} is within the range 0.043 f_{RCT} to 0.8 f_{RCT}, and f_{FCT}/f_{VCT} is less than 0.5.

Figures 8 and 9 show the variation of inverter switching frequency plotted against output frequency with f_{RCT} = 280 kHz, and $f_{s(max)}$ = 1 kHz. To obtain the equivalent figures for different values of $f_{s(max)}$, both scales and f_{RCT} should be multiplied by the required value of $f_{s(max)}$ in kHz. For example, with $f_{s(max)}$ = 2 kHz, f_{RCT} = 2 X 280 = 560 kHz, and referring to Fig.9, the value of f_s for f_{out} = 50 Hz (2 X 25) will be 1.5 kHz (2 X 0.75) at a pulse rate of 30 pulses per output cycle. Referring to Figs.8 and 9, it can be seen that the range of f_{out} that will keep f_s in the band 2 to 1.2 kHz will be 7.1 Hz (2 X 3.55) to 133 Hz (2 X 66.5), provided the ratio f_{FCT}/f_{VCT} is less than 0.5.

Output delay clock OCT

The OCT clock input, operating in conjunction with the data input K, is used to set the interlock delay period which is required at the changeover between the complementary outputs of each phase. For a thyristor inverter, where the output thyristors are triggered by a train of pulses (mark-space ratio 1:3), OCT and K have the additional function of determining the frequency of the pulse train.

The operation of OCT and K is shown in Table 3. Whenever possible input K should be HIGH as this keeps the jitter caused by lack of synchronisation between FCT and OCT to a minimum. In many cases a design economy can be obtained by using the same clock for both RCT and OCT.

Control outputs

Oscilloscope synchronisation RSYN

This is a pulse output of frequency f_{out} and pulse width identical to the VCT clock pulse. It is timed to occur just before the positive-going zero transition of the R-phase voltage. It therefore provides a stable reference for triggering an oscilloscope.

Output voltage simulation VAV

VAV is a digital waveform which simulates the average value of the expected line-to-line voltage of the inverter output; however, it excludes the effect of the interlock

TABLE 3

Operation of clock input OCT* and data input K

K	Interlock delay period ms	Trigger pulse frequency kHz	Trigger pulse width ms
LOW	$8/f_{OCT}$	$f_{OCT}/8$	$2/f_{OCT}$
HIGH	$16/f_{OCT}$	$f_{OCT}/16$	$4/f_{OCT}$

*f_{OCT} in kHz

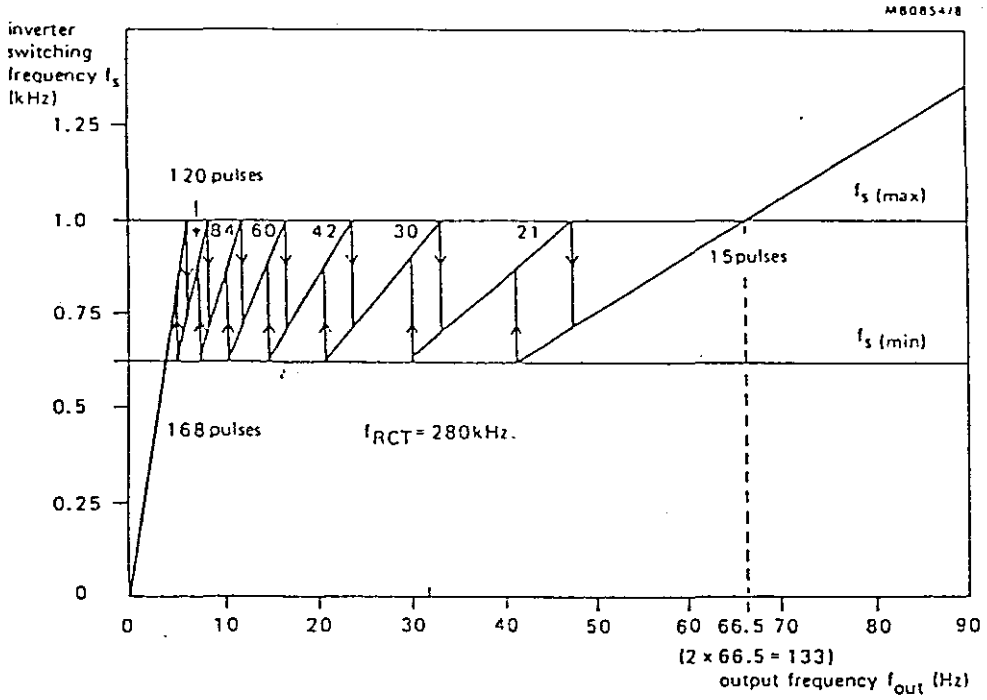


Fig.8 Inverter switching frequency against output frequency (full range)

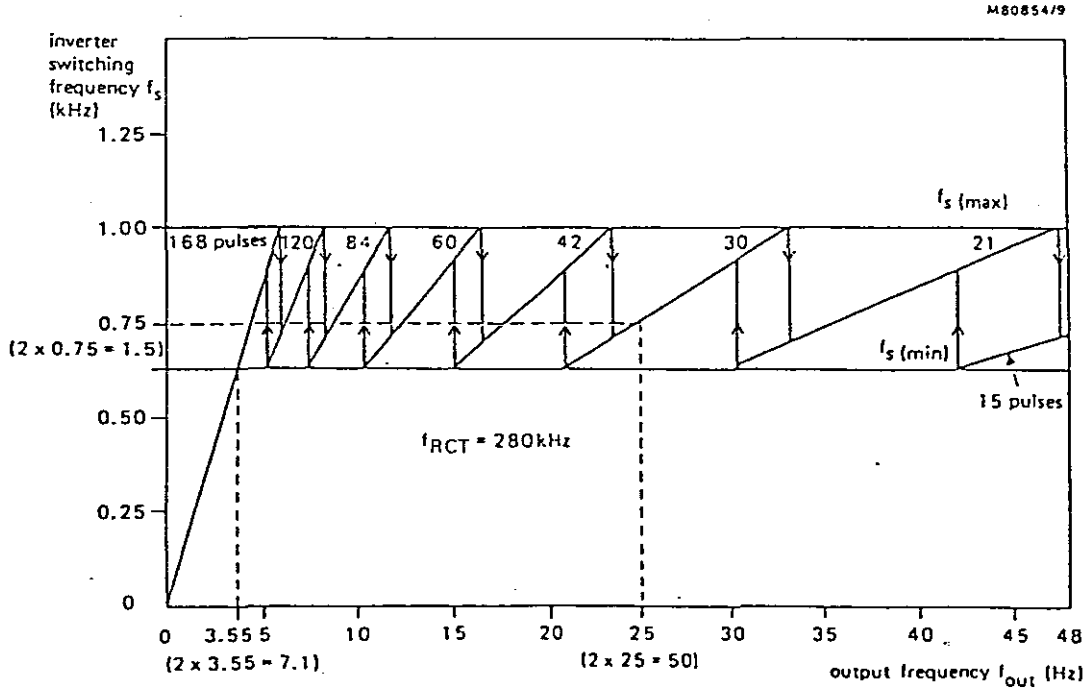


Fig.9 Inverter switching frequency against output frequency (expanded scale for low frequencies)

delay set by the K and OCT inputs, and is present irrespective of the L input state. The VAV signal has a frequency equal to the inverter switching frequency f_{out}, and a modulation given by $6f_{out}$.

VAV is useful for closed-loop control of f_{VCT} to obtain some improvement in the linearity of voltage with frequency when the frequency ratio f_{FCT}/f_{VCT} is greater than 0.5. The variation of VAV with frequency ratio is shown in Fig.10.

Inverter switching output CSP

The output CSP is a pulse train at twice the inverter switching frequency. The falling edge of each pulse occurs at the point of zero modulation of the main outputs. When f_{FCT}/f_{VCT} exceeds 0.5, CSP represents the theoretical inverter frequency; however, because of the merging of pulses from over-modulation, the actual switching frequency will be less. As with the VAV output, CSP is unaffected by the state of input L.

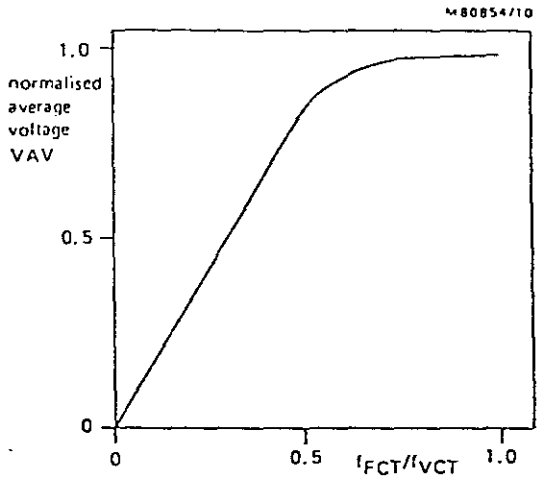


Fig.10 VAV against f_{FCT}/f_{VCT}

APPLICATION ADVICE

Proper operation of the IC requires limitations on the frequency ratio f_{FCT}/f_{VCT}, and on the range of f_{FCT}. These limitations have already been described under the discussion of the clock inputs VCT and RCT. Three additional conditions for ensuring satisfactory performance are now considered.

Start/stop input L

If input L is used in the thyristor mode, care must be taken to ensure that the switching edges are clean. For example, if some switch bounce occurs when switching to the LOW condition, then this can result in one or more of the M1 outputs being on instead of all the M2 outputs. A simple circuit to overcome this problem, together with the corresponding output waveform, is shown in Fig.11.

Switch-on conditions

For safe operation an initial switch-on period is required, during which the thyristor trigger circuits or transistor drive circuits are inhibited, and the correct clock and input conditions are established. During the first half of the switch-on period, the internal IC circuit should be reset. This can be done by either applying a HIGH signal to input A, or running the FCT clock for at least 3360 FCT pulses.

The required input states on all inputs must be established during the second half of this period. If FCT is to

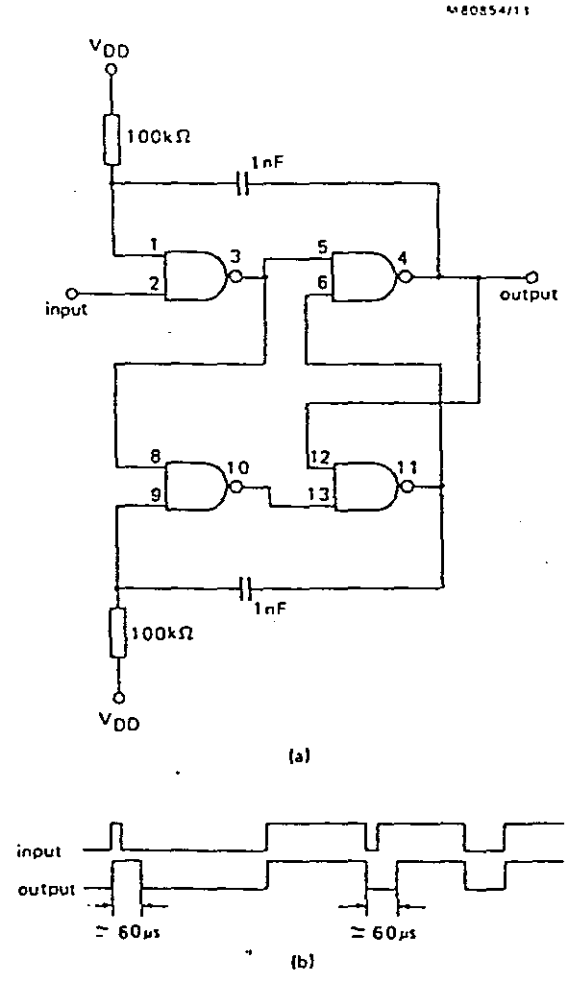


Fig.11 Circuit for use with L input to ensure a minimum pulse width: (a) Circuit with pinning corresponding to IC type HEF4093. (b) Input/output pulse trains

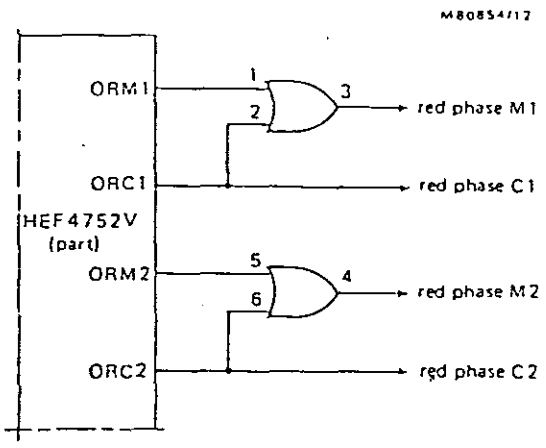


Fig.12 Circuit for producing a full length trigger pulse under minimum pulse width conditions. Pinning corresponds to IC type HEF4071

be started from zero during normal operation, it is advisable to run the FCT clock at about 0.04 f_{RCT} during the second half of the switch-on period for at least 3360 pulses, otherwise the output circuits will be set at 15 pulses per cycle for the first few pulses, instead of 168, which could result in damage to the inverter.

Minimum pulse width

From Figs.6 and 7 it can be seen that once the control signal (waveforms 6e and 7e) produces a pulse width equal to, or less than, the interlock delay, the appropriate main output is reduced to a narrow pulse. The width of this pulse is $1/f_{OCT}$ and it is always followed by a full-width commutation pulse. In the transistor mode, this narrow pulse will normally have little or no effect on the inverter. However, in the thyristor mode the correct triggering of the main thyristor may require the connection of the commutation pulse to the main pulse via an OR-function. A circuit to achieve this result is shown in Fig.12.

The next article in this series will describe the analogue control section.

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ERRATA

E.C. and A., Vol. 2 No. 3, May 1980. The article 'Electret microphone for telephony' should have included the following acknowledgement:

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Required output frequency Input	Frequency Control Clock Input	For normal operation Below 0.5 sine wave above 0.5 a Quasi - Square wave. 3 is the Limit	For Boosting output Voltage
2 Hz	6720 Hz		
3 Hz	10080 Hz		
4 Hz	13440 Hz		
5 Hz	16800 Hz	0.051270	0.102541
6 Hz	20160 Hz	0.061524	0.123049
7 Hz	23520 Hz		
8 Hz	26880 Hz		
9 Hz	30240 Hz		
10 Hz	33600 Hz		
11 Hz	36960 Hz		
12 Hz	40320 Hz	0.123049	0.246099
13 Hz	43680 Hz	0.133304	0.266608
14 Hz	47040 Hz	0.143558	0.287116
15 Hz	50400 Hz	0.153812	0.307624
Hz	53760 Hz	0.164066	0.328133
Hz	57120 Hz	0.174320	0.348641
18 Hz	60480 Hz	0.184574	0.369149
19 Hz	63840 Hz	0.194829	0.389658
20 Hz	67200 Hz	0.205083	0.410166
25 Hz	84000 Hz	0.256354	0.512708
26 Hz	87360 Hz	0.266608	
27 Hz	90720 Hz	0.276862	
28 Hz	94080 Hz	0.287116	
29 Hz	97440 Hz	0.297370	
30 Hz	100800 Hz	0.307624	
31 Hz	104160 Hz	0.317879	0.635758
32 Hz	107520 Hz		
33 Hz	110880 Hz		
34 Hz	114240 Hz		
35 Hz	117600 Hz		
36 Hz	120960 Hz		
37 Hz	124320 Hz		
38 Hz	127680 Hz		
Hz	131040 Hz		
40 Hz	134400 Hz	0.410166	0.820333
50 Hz	168000 Hz	0.512708	1.025416
51 Hz	171360 Hz		
52 Hz	174720 Hz		
53 Hz	178080 Hz		
54 Hz	181440 Hz		
55 Hz	184800 Hz		
56 Hz	188160 Hz		
57 Hz	191520 Hz		
58 Hz	194880 Hz		
59 Hz	198240 Hz		
60 Hz	201600 Hz		
61 Hz	204960 Hz	0.625504	1.251008
62 Hz	208320 Hz		
63 Hz	211680 Hz		
64 Hz	215040 Hz		
65 Hz	218400 Hz		

66 Hz	221760 Hz		
67 Hz	225120 Hz		
68 Hz	228480 Hz		
69 Hz	231840 Hz		
70 Hz	235200 Hz	0.717791	1.435583
71 Hz	238560 Hz		
72 Hz	241920 Hz		
73 Hz	245280 Hz		
74 Hz	248640 Hz		
75 Hz	252000 Hz		
76 Hz	255360 Hz		
77 Hz	258720 Hz		
78 Hz	262080 Hz		
79 Hz	265440 Hz		
80 Hz	268800 Hz	0.820333	1.640666
81 Hz	272160 Hz		
82 Hz	275520 Hz		
83 Hz	278880 Hz		
84 Hz	282240 Hz		
85 Hz	285600 Hz		
86 Hz	288960 Hz		
87 Hz	292320 Hz		
88 Hz	295680 Hz		
89 Hz	299040 Hz		
90 Hz	302400 Hz	0.922874	1.845749
91 Hz	305760 Hz		
92 Hz	309120 Hz		
93 Hz	312480 Hz		
94 Hz	315840 Hz		
95 Hz	319200 Hz		
96 Hz	322560 Hz		
97 Hz	325920 Hz		
98 Hz	329280 Hz		
99 Hz	332640 Hz		
100 Hz	336000 Hz	1.025416	2.050833

Mains input = 210 Volts A.C.
D.C Link Voltage = 296.94 Volts D.C.
Motor rated frequency = 100 Hz
Motor Rated r.m.s. voltage = 380 Volts A.C.

The Frequency at 100% Modulation = 48.76067 Hz

Voltage control clock VCT = 327671.7 Hz

To double the voltage at lower Frequencies
multiply F (VCT norm) by 0.5 = 163835.8 Hz

Reference clock (RCT) = 567000 Hz

Maximun switching frequency = 2025 Hz
Minimun switching frequency = 1215 HZ

Is FCT in range
For minimum 24381 Hz FCT
For Maximum 453600 Hz FCT