DEVELOPMENT OF THE MINITEL PERIPHERAL PORT ADAPTOR (MPPA)

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(i)

DECLARATION

I declare that the contents of this thesis represents my own work and the opinions contained here are my own. It has not been submitted before for any examination at this or any other institute.

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(Signature)

Abstract

This thesis describes how an adaptor board was developed to enable serial devices, such as modems and serial printers operating on RS-232 signals, to be used in conjunction with the MINITEL terminal. Furthermore it enables parallel Centronix interfaces to be used in conjunction with the MINITEL terminal.

The revolutionary 87C751 microprocessor was fully researched, and implemented in the project.

Two marketable products emerged during the course of the project: 1. The 8031-processor solution

2. The 87C751-processor solution

Opsomming

Hierdie verhandeling beskryf hoe 'n apparaat ontwikkel is wat series-werkende toestelle, soos modems en series-drukkers wat RS-232 seining gebruik, in staat stel om aan die Minitel terminaal gekoppel te word. Verder stel dit ook parallel Centronix koppelvlakke in staat om aan die Minitel terminaal gekoppel te word. Die revolusionere 87C751 mikroverwerker is ten volle nagevors en in hierdie projek geimplementeer.

Twee bemarkbare produkte het voortgespruit uit hierdie projek:

1. Die 8031 oplossing

2. Die 87C751 oplossing

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1. Objective.

The objective of this project was to design and build a marketable product that would promote the MINITEL terminal by overcoming the following limitations:

a) The single serial port that the MINITEL is manufactured with.b) The TTL orientated design of the MINITEL.

The above-mentioned limitations restricted the choice of peripheral devices that the Minitel could communicate with.

The improved MINITEL was to comply to the following specifications:

Enable the usage of serial RS-232 printers or modems.
Enable the usage of parallel CENTRONIX printers.

3. Have the capability of buffering at least 8K of data during parallel operation.

4. Have as small as practically possible physical dimensions. 5. Be as reasonably priced as possible to make it affordable for all potential MINITEL users.

2. Introduction

The "MINITEL" terminal as it is known in South Africa is manufactured by ALCATEL in France.

The main objective of MINITEL is to provide a cheap service to the South African public, which will make it possible for anyone to afford BELTEL and other services offered by TELKOM SA, such as EASY-ACCESS.

Services such as BELTEL, were amongst other things implemented to promote the X25 Packet Switched Network of TELKOM SA. This service is a major source of income for Telkom. It is therefore of extreme importance to Telkom that the MINITEL terminal be made as attractive as possible to the South African public.

A major disadvantage of the Minitel terminal is that its peripheral port supports only serial communication at TTL levels (+5V and OV). Very few printers and modems operate at these levels and a large number of potential Minitel users are already in possession of a parallel printer which unfortunately cannot interface to the Minitel terminal.

The need therefore arose to develop a cheap adaptor, that could fit onto the peripheral port of the MINITEL terminal and would make it possible to connect to serial devices such as modems via a RS-232 interface or to communicate with a PC via the COMMS port.

In effect the MINITEL would operate as a cheap, RS-232 compatible, asyncronous terminal. This would also make the MINITEL terminal compatible to most serial printers on the market.

The most important feature of such an adaptor would be to make it possible for the MINITEL terminal to print to any parallel printer.

Two solutions are described in this thesis:

1. The first is the hardware solution, utilising an 8031 microprocessor with a relatively small assembler program in EPROM. Data buffering is done by including 8K of RAM into the design. Configuration is done by means of DIP switches. The PC-board is mounted on the peripheral backplane of the MINITEL terminal and once installed, only the serial and parallel port connectors are accessable to the user.

2. The second is the software solution, utilising only an 87C751 microprocessor with an assembler program. All data buffering is done by utilising internal RAM of the processor. XON/XOFF flow-control is implemented.

Configuration is done by means of software routines, which transmit messages to the MINITEL screen prompting the user for setup information. The adaptor then processes the instructions entered by the user on the MINITEL keyboard.

Throughout the remainder of this document there will be distinguished between the two versions by referring to either the 8031 or the 87C751 model.

In cases where no distinction is made between the two versions it should be assumed that that part of the operation is identical for both versions. 3. Operation of the MPPA.

3.1 The 8031 Model.

3.1.1 Configuration.

Configuration is done by setting the dipswitches according to the table in the operating instructions. This must be done while the adaptor is powered down. After powering up the MPPA, it tests the settings of the dip switches and sets up the speed and other selectable parameters accordingly.

3.1.2 Serial Operation.

During serial operation, data received from the serial interface is converted from RS-232 to TTL levels to be compatible with the main Minitel logic levels.

Data transmitted from the main Minitel circuitry is converted from TTL levels to RS-232 levels and then transmitted via the serial interface.

Asynchronous operation for speeds up to 9600 Bps is supported.

3.1.3 Parallel Operation.

The built-in UART of the 8031 processor is used to capture serial data from the Minitel and convert it to parallel format. Each byte from the SBUF register is then temporarily sent to the external RAM buffer. During idle periods, bytes are fetched from RAM and placed on the parallel databus via Port 1 of the 8031.

Bytes are then latched into the parallel device by pulsing the STROBE line.

During parallel operation the BUSY line from the parallel device is continually monitored. When the BUSY line goes active, no data is sent to the parallel device, whilst additional data from the Minitel is buffered in the 8k buffer. If the 8k buffer fills up then additional data from the Minitel will overwrite the buffered data, beginning at the lowest RAM location. No direct flowcontrol exists between the Minitel and the MPPA and therefore a maximum of 8k data can be stored.

3.2 The 87C751 Model.3.2.1 Configuration.

After power-up, the Minitel speed defaults to 1200Bps. To simplify use of the adaptor, configuration therefore takes place at 1200Bps.

After power up the MPPA waits for 5 seconds to enable the Minitel to warm up before configuration commences. It then transmits preprogrammed messages to the Minitel screen, prompting the user for input from the Minitel keyboard. Since the Minitel currently only supports even parity, the parity bit of each byte needs to be adjusted before it is transmitted to the Minitel. The byte is then clocked out to the Minitel in serial format. After transmis-

sion of the complete message, the MPPA waits for a response from the user. This response is shifted into a register (bit by bit), interpreted by the MPPA and according to the response received the correct flags are set internally. In the case of an invalid response from the user, the previous message is retransmitted. After the user has completed configuration of the adaptor he is prompted to set up the speed of the Minitel the same as the MPPA and the operational routine starts.

3.2.2 Serial Operation.

During serial operation, data received from the serial interface is converted from RS-232 to TTL levels and sent to P0.0 on the processor. The parallel port is disabled and data is copied from P0.0 to P0.1 which in turn is connected to RXD on the Minitel. Data transmitted from the Minitel terminal is converted from TTL levels to RS-232 levels and then sent to TXD on the serial interface.

3.2.3 Parallel Operation.

Serial data received from the Minitel terminal is shifted into a register (bit by bit) by the processor and once a full byte has been received, it is transmitted to the parallel data bus via Port 3 on the processor. The strobe line is then pulsed to latch the data into the parallel device's receive buffer.

During parallel operation the BUSY line from the parallel device

continuously monitored. If the BUSY line goes active, is data from the Minitel is stored in the internal RAM of the processor. When the busy line goes inactive, the data stored in internal RAM transmitted to the parallel device. While the internal is RAM contains buffered data all subsequent data bytes from the Minitel internal RAM from where it is transmitted to the is sent to parallel port. This is done to ensure that "first in" data from the Minitel is "first out" to the parallel port. Since parallel transmission from the processor to the parallel device is considerably faster than serial reception from the Minitel, the internal RAM buffer is rapidly depleted and transmission can commence normally to the parallel device.

In the case of printers, a carriage return would cause the busy line to go active for a short period during which the internal RAM will fill up partially and the process described in the previous paragraph takes effect.

Most printers have a data buffer of their own. If, however, this buffer becomes full the printer will activate the BUSY line until certain percentage of its buffer has been emptied before it a accepts additional data. In the event of this happening the internal RAM buffer, being very small (approximately 25 bytes), will also fill up. When the MPPA detects that its internal buffer almost full it waits for the startbit of the next byte from is the Minitel and while clocking that byte into internal RAM it clocks out an XOFF to the Minitel's RXD pin, sharing the timing used to clock in the byte from the Minitel. (This is full-duplex operation.) Once the BUSY line goes inactive, the MPPA empties

its internal buffer and then transmits an XON to the Minitel. The Minitel will then continue with its transmission.

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FIGURE 1: 8031 MODEL PARALLEL OPERATION



FIGURE 2: 8031 MODEL SERIAL OPERATION



FIGURE 3: 87C751 MODEL CONFIGURATION AND OPERATION

4. The Hardware Design.

4.1 The Power Supply.

The adaptor requires +5V for correct operation. Since the MINITEL provides a +8.5V supply voltage, a voltage regulator was required to provide the required voltage. For this purpose the 7805 voltage regulator was used. The 7805 is a 5V (1A) voltage regulator.

4.2 The Parallel Printer Interface.

printer will not accept any input unless the SELECT input The line is in the proper state. The INITIALISE printer line is used initialise the printer when the system is powered up. to The correct signal must be on the line for at least 50 micro seconds. The data to the printer is placed on the eight DATA_BIT lines and line is pulsed. The printer processes the STROBE data the and sends a pulse back to the ACKNOWLEDGE line. When the acknowledge pulse is received by the processor, another character may be sent to the printer. Instead of waiting for the ACKNOWLEDGE pulse processor may check the busy line. The processor may send the characters to the printer as long as the printer is not busy. The OUT-OF-PAPER input indicates to the processor that the printer is out of paper. The SELECT input indicates to the computer that the printer is on line. The ERROR input indicates to the computer that the printer is off line, out of paper, or in another error state.

THE BUSY SIGNAL ALSO REFLECTS ALL THESE ERROR CONDITIONS.

Certain printers are sensitive to the AUTO FEED line. This line can be used to force the printer to generate an automatic line feed each time it prints a carriage return.

4.3 The Serial Port.4.3.1 The Minitel Serial Port.

The Minitel serial port consists of the following pins: Transmit Data (TTL voltage levels) Receive Data '(TTL voltage levels) Signal ground

4.3.2 The RS-232 Serial Port.

The RS-232 serial port (typically a serial printer or ASCII terminal) has the following relevant pins :

Transmit Data (RS-232 voltage levels) Receive Data (RS-232 voltage levels) Signal Ground

4.3.3 Conversion Of Serial Port Voltage Levels.

In both the 8031 and 87C751 models, the MAX232 line driver/receiver chip was used to convert voltage levels from TTL to RS-232 and vice versa. It is relatively cheap and very convenient to use in this application since it is dirven from a single 5V supply.

4.4 The 8031 Model.

4.4.1 The 8031 Microprocessor.

An 8031 8-bit microprocessor was used which provides extensive on-chip support for one-bit variables as a separate data type, allowing direct bit manipulation and testing in control and logic systems that require Boolean processing. The Address/Data is shared on Port 0 and the lower address-byte is latched by the 74LS573. The processor specifications are:

128 Bytes Internal Data memory 32 I/O Lines (Four 8-bit ports) Providing 5 interrupts 2x16-bit Timers/Event Counters 64K Program Memory (Only 8K was used in this application) 5V operating voltage 3.5 to 12.0 MHz Oscillator Freq.(External clock source)

3.5 to 12.0 MHZ USCITTATOR Tred. (Excernal clock source)

To minimise the use of external chips, the processor was fully utilised and not one pin was left unused.

A15 was used to chip-select either the 8K external RAM or 8K EPROM.

RXD was used for reception of data from the Minitel (Using serial interrupt)

The INTO pin was used to pulse the STROBE line and INT1 pin was used to monitor the status of the BUSY signal.

TO, T1, A14, A13 and TXD was used to setup the speed, 8 or 7 bit data and formfeed suppression by means of dipswitches that are connected to GND when ON and connected to +5V via 10K pull-up

resistors when OFF.

A0-A12 was used to address external 8K RAM and 8K EPROM.

Port 1 connects to the parallel port databus.

An 11.0592 MHz Crystal was used as external clock source. The use of this value made the programming of timers to provide correct Baudrates considerably easier.

4.4.2 The 8K External RAM.

A 6264 8K static RAM chip was used for data buffering on the MPPA.

4.4.3 The 8K EPROM

An assembler program was written in a 2764 8K EPROM.

4.5 The 87C751 Model.

The Philips 87C751 offers the advantages of the 8051 architecture in a small package and at low cost.

The 87C751 microcontroller contains a 2Kx8 EPROM, a 64x8 RAM, 19 I/O lines, a 16-bit auto-reload counter/timer, a five-source, fixed priority level interrupt structure, an on-chip oscillator and an inter-integrated circuit serial bus interface.

The on-board inter-integrated circuit bus interface facilitates I/O and RAM expansion, access to EEPROM and processor-to-processor communication. This feature was not used in the design of the MPPA.

Other features of the 87C751 are: Small package size (24-pin 300mm "skinny DIP") Low power consumption Fixed-rate timer Boolean processor

Since the 87C751 has 2k EPROM on board it eliminated the need for external program memory. Furthermore the external RAM used in the 8031 model was eliminated by using internal RAM buffering and XON/XOFF flow control.

The P1.7 pin was used to STROBE data into the parallel device. Port 3 was used as parallel data-bus. The BUSY line status was monitored on the P0.2 pin.

In the 87C751 model the speed, number of databits and formfeed suppression is configured from the Minitel keyboard and therefore the dipswitches and resistor pack used on the 8031 model was eliminated.





5. The Software Design.

5.1 The 8031 Model.

The CYS8051 package was used to write and assemble the program.

5.1.1 The External Memory Map

EPROM 0000h - 7FFFh External RAM 8000h - A000h

5.1.2 The Internal RAM Memory Map.

R0 - R7 00h - 07h STACK 08h - 7fh

5.1.3 The Initialization Routine.

During the initialisation routine, all registers are initialised:

5.1.3.1 The PCON register.

The double Baudrate bit SMOD is set.

5.1.3.2 The IE Register.

The global interrupt enable bit EA is set . The serial port interrupt enable bit ES is set. This enables the processor to react on serial interrupts.

5.1.3.3 The TCON Register.

Timer 1 Run control bit TR1 is set. Interrupt 0 Type control bit is set. (falling edge)

5.1.3.4 The TMOD Register.

Timer 1 is set up as an 8-bit auto-reload timer. The reload value is held by register TH1.

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5.1.3.5 The SCON Register.

SMO and SM1 are both set in order to set up the serial port as an 8-bit UART.

SM2 is set in order to not activate the RI flag unless a valid stopbit was received.

REN is set to enable reception on the RXD pin.

5.1.3.6 The PSW Register.

Bits RSO and RS1 are both 0, which allocates internal RAM location 00h - 07h to R0 - R7 and lets the SP point to 08h.

5.1.2 The Speed Configuration Routine.

During this routine, the setting of the speed-dipswitches are

checked and the TH1 register is loaded with the correct value.

The following formula is used to calculate the value for TH1: Baudrate = $2xSMOD/32 \times (oscillator frequency) / 12x[256-(TH1)]$

5.1.3 The Serial Interrupt Vector Routine.

When a startbit is received from the Minitel on the TXD pin of the 8031, a serial interrupt occurs.

The byte is loaded into the ACC, the dipswitches are checked to determine whether 7-bit Or 8-bit data is to be transferred to the parallel device and whether formfeed suppression takes place. The data is then stored in the next available RAM location. A check is done to see whether the external RAM is full. If it is full the next byte to be stored will overwrite the first RAM location and an overflow flag is set.

5.1.4 The Load Byte Routine.

This routine fetches the next outstanding byte from the external RAM and sends it to the parallel device if the BUSY line is inactive. The byte is latched into the parallel device after placing it on the databus. A check is done to determine whether the last RAM location has been transmitted. If true then the byte stored in the first location will be the next byte transmitted and an overflow flag is set.

5.2 The 87C751 Model.

The CYS8051 assembler package was used to write the assembler program.

Since the CYS8051 package does not support the 87C751, precautions had to be taken in order to correctly assemble the program for usage in the 87C751 microprocessor:

1. Because the 87C751 has only one external, 16-bit timer with auto-reload, the different counter registers are referred to as addresses in memory.

TLTIMER LOW BYTE8AHTHTIMER HIGH BYTE8CHRTLTIMER LOW RELOAD VALUE8BHRTHTIMER HIGH RELOAD VALUE8DH

 The timer must be started with the following command: SETB 8CH

3. The timer is stopped with the following command: CLR 8CH

Other differences between the 8031 and 87C751 are:

1. The internal RAM of the 87C751 is only 64 bytes.

2. The available EPROM memory of the 87C751 is 2k bytes.

5.2.1 The Internal RAM Memory Map

The RSO and RS1 bits in the PSW register are both set to 0 and therefore 00h - 07h are allocated to registers R0 - R7.

03h - 2Bh Internal data buffering

2Ch - 2Fh Bit variables

30h - 34h Byte variables

35h - 3Fh Stack

02h

00h

-

Note that no external memory map is used in the 87C751 model. (The MOVX command is not supported)

R0 - R2

5.2.2 The 5-Second Delay Routine.

One of the problems encountered, was the fact that the MPPA started sending the first configuration screen to the Minitel screen before the Minitel has properly warmed up. This resulted in a loss of characters. To enable the Minitel to warm up sufficiently before starting configuration, a 5-second delay was incorporated into the script.

5.2.3 The Configuration Routine.

Since the Minitel speed defaults to 1200Bps, configuration is done at 1200Bps.

5.2.3.1 Transmission to Minitel.

All the messages to be sent to the Minitel are stored in EPROM. At the start of the program the datapointer (DPTR) is directed to the first byte of the message to be transmitted. That byte is

fetched and placed in the accumulator.

The parity bit is then adjusted to EVEN parity since the Minitel defaults to this setting. Reception from the Minitel is disabled during transmission.

The start bit is then transmitted to the Minitel after which the rest of the bits are shifted out of a data-register at regular intervals, controlled by the timer interrupts.

The following routine is used :

MOV A, XMTDAT

RRC A

MOV XMTDAT, A

MOV TXX,C

A register is used to count the number of bits transmitted, in order to determine when a full byte has been sent. Once the complete byte has been transmitted, the DPTR points to the next byte and the procedure is repeated. The end of a message is indicated by OH. Once a OH is loaded into the accumulator transmission stops and reception is enabled.

5.2.3.2 Setting Up The Timer for Transmission.

The transmission of a byte starts by clearing the TXD pin to the Minitel, directly after which the timer is started. The timer start value is the same as the timer reload value (ie. BAUDVAL). This value is calculated as follows:

The '-' sign is necessary since the timer interval counter is an up-counter. This implies that this counter counts from FD00h to FFFFh before a timer interrupt occurs. (See figure 6)

5.2.2.3 Reception from the Minitel.

Once a full message has been transmitted to the Minitel screen, the program waits for a response from the Minitel keyboard. An external interrupt indicates the arrival of a startbit from the Minitel. At this point further external interrupts are disabled and the internal timer is started. Each bit received is



FIGURE6

STOP TIM





clocked and shifted into a register as follows: MOV A,RCVDAT MOV C,P1.5 RRC A MOV RCVDAT,A

5.2.2.4 Setting Up The Timer For Reception.

Reception of a byte starts with an external interrupt caused by the startbit. The startvalue of the timer (STRTVAL) causes the timer to wait until the middle of the startbit before it issues the first interrupt. It then uses the reload value (BAUDVAL) to provide interrupts at regular intervals (1 bit time).

STRTVAL is calculated as follows :

BAUDVAL/2 - DELAY

where DELAY is the number of timer intervals that would equal the time it takes the program to start the timer, after it receives an external interrupt.

This procedure ensures that bits are sampled at the point when half the bit has been received. (See figure 7)

Once again a count register is used to determine when the full byte has been received. On reception of a complete byte, the byte is decoded to determine whether it was a valid response or not. (Once again parity has to be taken into account.)

The program then reacts to the response by setting the necessary flags and then starts the transmission of the next message to the Minitel. Once the configuration is complete a flag is set which will pass control over to the second half of the program ie. "The Operational Routine". This flag is also used in the interrupt vector routines to indicate which routine to execute in the case of an interrupt. (The interrupt routines are different for the Configuration and Operational routines.)

5.2.4 The Operational Routine.

5.2.4.1 Serial Operation.

During serial operation the status of the Minitel's transmit is continually monitored and copied to the MAX232 line driver. This is done by means of a JNB command in conjunction with a SETB/CLR command.

5.2.4.2 Parallel Operation.

All the bit-variables that are set up during the configuration routine is checked and the MPPA is set up accordingly. During the operational routine serial data is received from the Minitel. The process of reception is the same as in the Configuration Routine except that the timer "start" and "reload" values are calculated according to the speed selected for operation. Once a full byte has been received and the BUSY signal from the Centronix interface is inactive, the byte is transmitted to the

parallel port by placing the byte on the parallel databus and then pulsing the STROBE line with a CLR bit/SETB routine.

In the event of a byte being ready to be sent to the parallel interface and the BUSY line is active, the data has to be buff-ered.

incremented, the value stored in R1 then points R1 is to the internal RAM address where the byte has to be stored. If this value exceeds 20H, the program detects that the internal RAM is full. The byte currently being handled is then stored in internal RAM location 20H and the XOF flag is set. When the next external interrupt occurs the program detects that XOF is set and starts to write an XOFF to the Minitel, using the same timing as byte being received. (The byte received will be half of the the bit time out of phase with the XOFF being transmitted).

Once the XOFF has been transmitted, the XOF flag is cleared and the XF flag is set which indicates to the program that an XOFF has been transmitted to the Minitel. The program will now be idle until the BUSY signal goes inactive. When this occurs, the internal RAM buffer is flushed to the parallel device, the XF flag is the XON flag is set. This flag indicates to cleared and the an XON must be sent to the Minitel. The timer is program that then started and the XON is clocked out to the Minitel. Once the XON has been transmitted, the XON flag is cleared and the XN flag is set. The XN flag indicates to the program that an XON has been to the Minitel and all registers and bits are set for sent qu reception from the Minitel. The XN bit is then cleared.
The Program Listings. .1 The 8031 Model Program Listing. the Cybernetic Micro Systems 8051 Family Assembler, Version 3.04 25-11-92 0000 ORG OH ;8S . 0000 020062 LJMP BEGIN 0023 ORG 23H 0023 020026 LJMP NEW NEW: 0026 COEO PUSH ACC 0028 CODO PUSH PSW 002A C082 PUSH DPL 002C C083 PUSH DPH 002E 8882 MOV DPL, RO ;LOAD DPTR WITH NEXT RAM ADDRESS 0030 8983 MOV DPH,R1 0032 E599 MOV A, SBUF ;LOAD RECEIVED BYTE INTO ACCUMULATOR ' LJMP 6200H 0034 026200 ;LOAD A13 AND A14 WITH 1'S CNT1: 0037 D29C SETB REN ;ENABLE RECEPTION 0039 C298 CLR RI 003B D083 POP DPH ;RESTORE REGISTERS FROM STACK 003D D082 POP DPL DOJF DODO POP PSW POP ACC 0041 DOEO 0043 32 ;RETURN INTERRUPT RETI NEXT: 0044 FO MOVX @DPTR,A ;LOAD BYTE INTO NEXT RAM LOCATION 045 A3 INC DPTR ; INCREMENT DATAPOINTER P046 A882 MOV RO, DPL ;STORE CONTENTS OF DATAPOINTER MOV R0, D12 MOV R1, DPH CJNE R0, #00H, CONT ;IS RAM FULL? CJNE R1, #0A0H, CONT MOV R1, #80H ;POINT TO FIR ;INDICATE OVE 048 A983 04A B80008 04D B9A005 **P0**50 7980 ; POINT TO FIRST RAM LOCATION 052 EE ; INDICATE OVERFLOW MOV A,R6 053 F4 CPL A 0054 FE MOV R6,A CONT: 055 D29C SETB REN ;ENABLE RECEPTION 057 D083 ;RESTORE REGISTERS FROM STACK POP DPH 059 D082 POP DPL 105B DODO POP PSW 05D DOEO POP ACC 05F C298 CLR RI 061 32 RETI RETURN INTERRUPT BEGIN: 062 758780 MOV PCON, #80H 0₆₅ 75A890 MOV IE,#90H 0₆₈ 75B800 MOV IP, #00H 06B 758841 MOV TCON, #41H 06E 758920 MOV TMOD, #20H 071 759870 MOV SCON, #70H

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0074 0077 0079 0078	1200D2 7800 7980 908000		LCALL S MOV RO, MOV R1, MOV DPT	PEED #00H #80H R,#8000H	;C) ;D]	ALL SPE PTR=800	ED SUBRON OH	UTINE	
007E 0081 0083 0085	75D000 AA82 AB83 7E00 7E00		MOV PSW MOV R2,1 MOV R3,1 MOV R6,1	,≇00H DPL DPH ≇00H	; M2	ARK LOC	ATION OF	NEXT PRI	INT BYTE
0089 008C	7590FF 7580FF		MOV P1, MOV P1, MOV P3,	#OGH #OFFH #OFFH	;11	ITIALI:	SE PORTS	1 AND 3	•
008F 1 0090 (0091 9 0092 (0094 (0095 1	EA C3 98 400C C3 EB	WAIT:	MOV A,R CLR C SUBB A,I JC BACK CLR C MOV A,R	2 RO 2	;15	5 THERE	A BYTE 1	FOR PRINT	ER?
0096 0097 0099 1 009A 9 009B 1 009D (99 4007 EE 9F 7010 02008F		SUBB A,I JC BACK MOV A,R(SUBB A,I JNZ BACI LJMP WA	R1 . 2 5 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7					
00A0 0 00A1 1 00A2 9 00A3 0 00A5 0 00A5 0 00A6 1 00A7 9 00A8 0 00A8 0	C3 EA 98 4008 C3 EB 99 4003 D2008F	BACK2	CLR C MOV A,R SUBB A,H JC BACK CLR C MOV A,R SUBB A,H JC BACK LJMP WAD	2 20 3 3 8 1 3 1 5 1 7					
00AD (00AE : 00B1 (23 30B303 02008F	BACK3	CLR C JNB P3.1 LJMP WAI	3,LOAD1 IT	;19	5 PRINT	ER BUSY?		
00B4 8	3A82	LOAD1	MOV DPL,	R2	;LC ;PF	AD DPTI RINT BY:	R WITH LO Fe	CATION C	F NEXT
0086 8 0088 1 0089 1 0088 0 0080 4 0080 1 0080 1 0000 1 00000 1 00000 1 00000000	3B83 50 5590 22B2 43 4A82 4B83 3A0008 3BA005		MOV DPH, MOVX A, MOV P1, CLR P3.2 INC DPTF MOV R2, MOV R3, CJNE R2, CJNE R3,	R3 DPTR 2 DPL DPL #00H,COM	; SF ; LF ; ST ; ST NT1 NT1	END BYT	E TO PARA TE INTO I CATION OI IS THE LA	ALLEL BUS PRINTER F NEXT PF AST RAM I	S RINTER BYTE COCATION?
OCA H	7880 Ef		MOV R3, MOV A,R7	80H 7		;WRAP ;INDIC	ATE OVER	FLOW	

rhe (Cybernetic	Micro Sys	tems 80	51 Family	Assembler,	Version	3.04 25-11-92
00CE 00CC	8 F4 2 FF		CPL A MOV R7	, A			
		CONT1:					
00CI 00CI	D2B2 02008F		SETB P: LJMP WA	3.2 AIT			
		SPEED:					
00D2 00D5 00D8	30B504 758DFA 22		JNB P3 MOV TH RET	.5,SPEED1 1, # 0FAH	;96001	BPS ?	
		SPEED1:					
00D9 00DC 00DF 00E2	30B107 30B40B 758DF4 22		JNB P3. JNB P3. MOV TH1 RET	1,SPEED2 4,SPEED3 1,#0F4H	;48005	3PS ?	
a migure manageme		SPEED2:					
00E3 00E6 00E9	30B408 758DE8 22		JNB P3. MOV THI RET	.4,SPEED4 L,#0E8H	;24005	BPS ?	
		SPEED3:					
00EA 00ED	758DD0 22		MOV THI RET	L, ∦ 0D0H	;12008	BPS	
		SPEED4:					
00EE 00F1	758D40 22		MOV THI RET	L,#40H	;300BF	s?	
6200		ORG 6200	H				
6200 6203	30A502 547F		JNB P2. ANL A,	5,FORM 7FH	;8-BII ;Mask	DATA ? BIT 7 WI	TH O
	_	FORM:					
205 5208	30A606 B40C03		JNB P2.	6,NEXT1 #OCH NEXT	SUPPR	LESS FORM	IFEEDS?
52 0B	020037		LJMP CN	T1	_ ,10 11		··· ••••
		NEXT1:					
52 0E	020044	- 9.77	LJMP NE	EXT			
000		; & E END					

The Cybernetic Micro Systems 8051 Family Assembler, Version 3.04

25-11-92

;9	T		S	ym.	bo	1	Na	me						•	Ту	pe	Value
BA	CK2	2	•	•	-	•		-	•		•	•		•		L	00A0
BA	CK3	3	•	•			•	•			•			•		L	00AD
BE	GIN	Ŧ	•			•	•		•	•	•	•		•	•	\mathbf{L}	0062
CN	Τ1.	,	•	•		•	•	•	•	•	•			•	•	\mathbf{L}	0037
CC	NT.		٠	•	٠	•		•	•			•				L	0055
CC	NT1	L	•	•	•	•	•	•	•	•	•	•		•		L	00CD
FC	RM.		•	•	•	•		•	•	•		-	-	•		L	6205
LC	AD1	•	•	•	•	•		•	•	•				٠	•	\mathbf{L}	00B4
NE	W		•	•	•	•	•	•	•				•	•		L	0026
NE	XT.		•	-	•	•	•	•	•	•	•	•	•	•	•	\mathbf{L}	0044
NE	XT1	•	•	•		•	•	•	•		•	•		•	•	\mathbf{L}	620E
SP	EED)	•	•	•		-	•	•	•	•	•	•	•	•	\mathbf{L}	00D2
SP	EED)1	•	•	•		•		•		•		•	•		\mathbf{L}	00D9
SP	EEC)2	•	•	•	•		•		•	-			•		L	00E3
SP	EED)3	•	•	•		•	•	•	.'	•	•	•	•	•	L	00EA
SP	EED	4	•		•	•		•	•	•		•		•	•	L	OOEE
WA	IT.		•	٠	•	٠	•		•	٠	•	٠	•	•	٠	L	008F
	Z																
00	Er	r	or	s	1	(00	00))									

6.2 The 87C751 Program Listing

The Cybernetic Micro Systems 8051 Family Assembler, Version 3.04

	-		-	25-11-92
	; * * * * * * * * * * * *	******	******	******
	;*			*
	;*	THE MINIT	EL PERI	PHERAL PORT INTERFACE MODULE *
	*			*
	********	*******	*****	* * * * * * * * * * * * * * * * * * * *
	:			
	:			
	:			
	;			
	, 	*******	******	******
	, • * * * * * * * * * * * * *	*****0801	ARATTON	OF VARIABLES***************
	, • * * * * * * * * * * * *	********	*******	****
	/			
FD00 =	BAUDVAL	FOIL	-768	BTT TIME AT 1200Bpg
FE93 =	STRTVAL	FOU	-365	HALF OF BIT TIME AT 1200Bps
0030 =	XMTDAT.	<u>-2</u> -	30H	DATA TO BE TRANSMITTED
0034 =	RCVDAT	DATA	34H	DATA RECEIVED
0033 =	BITCNT	ወለፓብ	33H	COINTS THE BITS DECEIVED
0032 =	LOODCAL	DATA ከእሞል	- 30H	COULD THE BITS RECEIVED
0031 =	CNT	עשעם	3211 3111	COINT PEC FOR 5 SEC DELAV
0077 -	UNI MVELAC	DAIA	310 770	TNDTCATE TDANENTESTON
0076 -	TAL DAG		774	TNDICATES TRANSMISSION
0070 - 0075 -	KAT LAG		700	INDICATES RECEPTION
	RAERR		750	, INDICATES ERROR CONDITION
0074 = 0073 -	RCVRDY	BIT	748	I TNDTCAMPO MUNM MDANCHICCION OP
	GO	BTT	/31	CURCENTER CORFERE CONTENCES
1091 -	m .777	क र ली		JODSEQUENT SCREENS COMMENCES.
0001 = 0072 = 00072	TXX	BIT	20.1	TRANSMIT DATA PIN
4072 =	L'T M	BIT	/28	A TIME OF THE INITIAL
007.			~	;/FINAL SETUP SCREEN.
	TSET	BIT	71H	INDICATES THAT THE SPEED
0070				SCREEN IS DISPLAYED
00/8 =	TWO	BIT	78H	;INDICATES 2400 BPS
00/F =	THR	BIT	7Fh	;INDICATES 300 BPS
00/E =	ONE	BIT	7 EH	;INDICATES 1200 BPS
007D =	FOU	BIT	7DH	;INDICATES 4800 BPS
107C =	NIN	BIT	7CH	;INDICATES 9600 BPS
0070 =	PPS	BIT	70H	;INDICATES THAT THE PORT SELECT
				;SCREEN IS DISPLAYED
007A =	RAM1	\mathtt{BIT}	7AH	; IF SET INDICATES THAT CONFIGURA-
				;TION IS COMPLETE AND THAT THE
				;MODULE IS NOW READY FOR OPERATION.
0079 =	PAR	BIT	79H	;INDICATES PARALLEL OPERATION
006F =	FORM	BIT	6FH	;INDICATES THAT THE FORMFEED SCREEN
				IS DISPLAYED
007B =	FFON	BTT	7BH	IF SET THEN SUPPRESS FF'S. TF
	T T A14	~ - +		CLEARED THEN PRINT FF'S
006E =	סרס	RTT	6EH	INDICATE THAT CURRENT SCREEN MUST
	REF	D17	<u> </u>	BE REPEATED.
006D =	Μκα	BIT	6DH	INDICATES THAT SETTID IS CONDITIONE
006C -	RAM	914 111	60H	TNDTCATES THAT THE ENDIFER COMPLETE
	rukur	710	001	(1.01 JUNI THE FORMELED STATU:

The (Cybernet	ic Micro	Systems 8051	Family	Assembler, Version 3.04 25-	11-92
006E	3 =	PORTI	BIT	6BH	; IS TO BE DISPLAYED ; INDICATES THAT THE T	YPE OF TRANS-
0067	<i>l</i> =	FIN1	BIT	бАН	; MISSION IS TO BE DIS ; INDICATES THAT FINAL ; BE DISPLAYED	MESSAGE IS TO
0069) =	DEL	BIT	69H	;IF SET INDICATES THA ;WARMUP DELAY IS STIL	T THE 5-SECOND L IN PROGRESS
unimmedia en sécura de seconomica		; * * * * * * * * ; * * * * * * * * ; * * * *	* * * * * * * * * * * * * * * * * * *	******* THE INTE ******	**************************************	************* *****************
0000		ORG OH ;%S				
0000	0115		• AJMP RES	SET .	;GOTO INITIA ;ROUTINE	LISATION
0003 0003	307A02	ORG 0	3H JNB RAM1	.,SET1	CHECK W	HETHER CONFIG-
0006	C170		AJMP EEX	XINTO	; URATION ; GOTO OF • INTERRU	PERATIONAL PT ROUTINE
8000	2183		SET1: AJ	MP EXIN	ro ;GOTO CO ;INTERRU	NFIGURATION PT ROUTINE
000B	20696A	ORG 0	BH JB DEL,D	ELAY1	;CHECK W ;DELAY I •PROCEES	HETHER WARMUP S STILL IN
000E	307A02		JNB RAM1	, SET2	; CHECK W ; URATION ; PROCEES	HETHER CONFIG- IS STILL IN
0011	CICD		AJMP TTI	MRO	;GOTO ;TIMER I ;TINE.	OPERATIONAL NTERRUPT ROU-
0013	2159	SET2:	AJMP TIM	IR0	;GOTO ;TIMER I ;TINE.	CONFIGURATION

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	The Cyberne	tic Micro Sys	tems 8051 Famil	y Assembler,	Version 3.04
. :					25-11-92
	a un un de la compañía de la compañí	; * * * * * * * * * * * * * * * * * * *	**************************************	**************************************	**************************************
t south and the second s	0015 758139 0018 75D000	5 RESET:	MOV SP, # 35H MOV PSW, # 00H		;STACK STARTS AT 35H ;CLEAR THE PROGRAM
	001B 758800	D	MOV TCON, #00H		; STATUS WORD ; LOAD TIMER CONTROL
	001E 75A883	3	MOV IE, # 83Н		; LOAD INTERRUPT ENABLE ; REGISTER WITH 83H
	transformed at the state of the	;NOTE :	ALL DEFINED BIT:	S ARE INITIAL	ISED AS ZEROS
- - - - - - - - - - - - - - - - - - -	0021 C276 0023 C277 0025 C275 0027 C274 0029 C273 002B C272		CLR RXFLAG CLR TXFLAG CLR RXERR CLR RCVRDY CLR GO CLR FIN		
	002D C271 002F C278 0031 C27F 0033 D27E	· · · ·	CLR TSET · CLR TWO CLR THR SETB ONE		;SET SPEED UP FOR 1200 ;BAUD
	0035 C27D 0037 C27C 0039 C270 003B C27A 003D D279		CLR FOU CLR NIN CLR PPS CLR RAM1 SETB PAR		;SET PORT UP FOR PARAL-
	003F C26F		CLR FORM		;LEL OPERATION
و المحمد الم	0041 D27B 0043 C269 0045 C26E 0047 C26D 0049 C26C 004B C26B 004D C26A		SETB FFON CLR DEL CLR REP CLR RAM CLR FORMF CLR PORT1 CLR FIN1		;SUPPRESS FORMFEEDS
	004F 753147	,	MOV CNT, #47H		;SETUP CNT REGISTER FOR ;47 TIMER INTERRUPTS
	contraction and the second	;*SETUP TIM	ER START VALUE	AND TIMER RELO	DAD VALUE FOR 5-SEC DELAY=
	0052 7A00 0054 8A8C 0056 7A01 0058 8A8A 005A 7A00 005C 8A8D 005E 7A01 0060 8A8B		MOV R2, # 00H MOV 8CH, R2 MOV R2, # 01H MOV 8AH, R2 MOV R2, # 00H MOV 8DH, R2 MOV R2, # 01H MOV 8BH R2		

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	The C	ybernet:	ic Micro Systems	8051 Family Assem	bler, Version 3.04 25-11-92
	a to an and a local sector and the s		; * * * * * * * * * * * * * * * * * * *	**************************************	**************************************
	and the state		DELAY:		
	0062	D269		SETB DEL	;5-SEC DELAY IN PROGRESS
	0064	D28C		SETB 8CH	;START TIMER
	0066	E531		MOV A, CNT	;LOAD ACCUMULATOR WITH
			,		THE NUMBER OF REMAINING
	0068	B400F7		CINE & #0 DELAY	FXTT DELAY ROUTINE WHEN
	-	D40017		COME A, FO, DELAT	CNT REGISTER REACHES
	ang kanan				ZERO.
	006B	C28C		CLR 8CH	STOP TIMER
	006D	C269		CLR DEL	;INDICATE THAT CONFIGU-
	OOCE	a a			;RATION CAN COMMENCE.
	0051	C2A8		SETB FIN	INDICATES THAT INTTIAL SETUP
	0071	0272	·	Ship iim	;MESSAGE IS DISPLAYED TO
10					REACT CORRECTLY WHEN RESPONSE
				•	;IS RECEIVED AFTER MESSAGE HAS
	0070				; BEEN SENT.
	0073	900335		MOV DPTR, #MSG1	POINT TO MESSAGE 1
	0076	2111		AJMP PRI	STARTS OUTPUT TO MINT-
-			,		TEL SCREEN
	and the second				
	0070	1501	DELAY1:		DELAV WINED INVERDION
	0078	1231		DEC CNT	ROUTINE
	007A	32		RETI	
		-			
	0078	207202	LOOP1:	TB CO CC01	• IS BIT GO SET?
	007E	207302		ATMP LOOP2	,15 bil do bel.
1		22211			
1		,	GG01:		· · · · · · · · · · · · · · · · · · ·
	0800	C2A8		CLR EXO	;DISABLE RECEPTION
	0082	C273		CLR GO	ידכ בזת עדא כבת 7
	0087	30/208		JND FIN,MESZ	TS BIT REP SET ?
	008A	900335		MOV DPTR. #MSG1	POINT DPTR TO MSG1
	008D	2111		AJMP PRT	•
			N722 -		
	008F	307100	ML52:	JNB TSET MESS	IS BIT TSET SET ?
	0092	9002B4		MOV DPTR. #MSG2	POINT DPTR TO MESG2
	0095	2111		AJMP PRT	
and the second se			1004		
	0097	026F	MES4:	CLR RFP	
		C20E			
	,				

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	1		-		
1	he	Cybernetic	Micro Systems	8051 Family Assem	bler, Version 3.04 25-11-92
	0 09 0 09	9 900335 C 2111		MOV DPTR, # MSG1 AJMP PR	;POINT DPTR TO MESG1
	009 00A 00A	E 306F05 1 900319 4 2111	MES5:	JNB FORM,MES6 MOV DPTR,#MSG3 AJMP PRT	;IS BIT FORM SET ? ;POINT DPTR TO MESG3
	00A 00A 00A	6 306D05 9 9004FD Ç 2111	MES6:	JNB RAM,MES7 MOV DPTR,#MSG6 AJMP PRT	;IS BIT RAM SET ? ;POINT DPTR TO MESG6
	00A 00B	E 9004A7 1 805E	MES7:	MOV DPTR,#MSG5 SJMP PRT	; POINT DPTR TO MESG5
1 * * * * * * * * * * * * * * * * * * *	00B 00B 00B 00B 00C 00C	3 206C33 6 206B45 9 207E0C C 207810 F 207F14 2 207D18 5 207C1C	LOGO:	JB FORMF, LOGO1 JB PORT1, LOGO2 JB ONE, LOGO01 JB TWO, LOGO02 JB THR, LOGO03 JB FOU, LOGO04 JB NIN, LOGO05	; FORMFEED MESSAGE ?
A STATE AND A STATE AN	00C 00C	8 900384 B D26C D 8042	LOGO01:	MOV DPTR, # MSG101 SETB FORMF SJMP PRT	
	00C 00D 00D	F 90038D 2 D26C 4 803B	LOGO02:	MOV DPTR,#MSG102 SETB FORMF SJMP PRT	
r 7 men is die mit die Swande als Spin Applikation werden. Als Lieben Advectionen	00D 00D 00D	6 900396 9 D26C B 8034	LOGO03:	MOV DPTR,#MSG103 SETB FORMF SJMP PRT	
<mark>nan min fagi</mark> rik kunan senara k aranji Mita a siya ki sama ta m	00D 00E 00E	D 90039E 0 D26C 2 802D	LOGO04:	MOV DPTR, ∦ MSG104 SETB FORMF SJMP PRT	

LOGO05:

		•		25-11-92
00E4 00E7	9003A7 8028		MOV DPTR, ≸ MSG10 SJMP PRT	
00E9 00EC 00EF 00F1 00F3	207B09 9003D9 C26C D26B 801C	LOG01:	JB FFON,LOGO101 MOV DPTR,≇MSG107 CLR FORMF SETB PORT1 SJMP PRT	
00F5 00F8 00FA 00FC	9003B0 C26C D26B 8013	LOGO101:	MOV DPTR,#MSG106 CLR FORMF SETB PORT1 SJMP PRT	
00FE 0101 0103 0105 0108	207909 D26A C26B 900456 8007	LOGO2:	JB PAR,LOGO201 SETB FIN1 CLR PORT1 MOV DPTR,#MSG109 SJMP PRT	
010A 010C 010E	D26A C26B 900403	LOG0201:	SETB FIN1 CLR PORT1 MOV DPTR,#MSG108	
0111 0113 0115 0117 0119 011C 011E	C2A8 516A 3136 D2A8 306A04 C26A 8003	PRT:	CLR EX0 ACALL MESS ACALL XMTBYTE SETB EX0 JNB FIN1, PRT1 CLR FIN1 SJMP PRT2	;DISABLE RECEPTION ;ENABLE RCEPTION ;IS BIT FIN SET?
0120	207211	PRT1:	JB FIN,LOOGOO	
0123	306D04 D27A	PRT2:	JNB RAM, LOOP2 SETB RAM1	;IS BIT RAM SET

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The	су	bernetic	: Micro Syst	tems 8051 Family Ass	embler, Version 3.04 25-11-92
01 01	2A 2D	208C02 D2A8	LOOP2:	JB TRO,IEN SETB EXO	
01	2F 32	3073F8 017B	IEN:	JNB GO,LOOP2 AJMP LOOP1	
01	34	01B3	LOOGOO:	AJMP LOGO	
n on a normania			;*******	**************************************	RANSMIT ROUTINE************************************
01:	36	2076FD	XMTBYTE:	JB RXFLAG,\$;CHECK WHETHER RECEPTION
01: 01:	39 3B	313F 2077FD		ACALL RSXMT JB TXFLAG,\$;IS IN PROGRESS ;GOTO THE BIT ROUTINE ;IS TRANSMISSION IN ;PROGRESS
A			; PROGRAM	WAITS FOR TIMER INT	ERRUPT WHILE TXFLAG IS SET.
01:	3E	22		RET	
يەرىپ تەرىپەر يەرىپەر يەرىپەر يەرىپەر مەرىپەر يەرىپەر يەرىپەر يەرىپەر يەرىپەر		;	******	*********THE BIT TRA	NSMISSION ROUTINE***************
01:	3F 41	F530 75330A	RSXMT:	MOV XMTDAT,A MOV BITCNT,#10	;FETCH BYTE TO BE XMITTED ;LOAD BITCOUNTER
sa dindan sa difina dan shanada na analisi		;	******	****LOAD THE TIMER W	ITH THE VALUE FOR 1200 BAUD**
014 014 014 014 014	14 16 18 1A	7AFD 8A8C 7A00 8A8A 7AFD		MOV R2, # 0FDH MOV 8CH, R2 MOV R2, # 00H MOV 8AH, R2 MOV R2, # 0FDH	·
015	* # 50 52	5A8D 7A00 8A8B		MOV 8DH, K2 MOV R2, #00H MOV 8BH, R2	;TIMER SETUP COMPLETED
015	54	C281		CLR TXX	;TRANSMIT STARTBIT

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The Cybernetic Micro Systems 8051 Family Assembler, Version 3.04 25-11-92 EXINTO: MOV BITCNT, #10 ;COUNT TEN BITS MOV R2, #LOW STRTVAL ;LOAD TIMER WITH VALUE FOR 0183 75330A 0186 7A93 :1200 BPS 0188 8A8A MOV 8AH, R2 018A 7AFE MOV R2, #HIGH STRTVAL 018C 8A8C MOV 8CH, R2 018E 7AFD MOV R2, #HIGH BAUDVAL 0190 8A8D MOV 8DH, R2 0192 7A00 MOV R2, #LOW BAUDVAL MOV 8BH, R2 MOV RCVDAT, #0 ;INITIATE THE RXD REGISTER 0194 8A8B 0196 753400 0199 C2A8 CLR EXO ;DISABLE EXTERNAL INTERRUPTS CLR RXERR 019B C275 019D D28C SETB 8CH ;START TIMER SETB RXFLAG RECEPTION IN PROGRESS 019F D276 01A1 32 RETI . RXBIT: DJNZ BITCNT, RXBUSY ; WAS THE STOP BIT RECEIVED ? 01A2 D53302 SJMP RXBITEX 01A5 8010 RXBUSY: MOV A, BITCNT 01A7 E533 CJNE A, #9, RXNEXT ; IS THIS THE STOPBIT 01A9 B40902 SJMP TOEX2 01AC 80B7 RXNEXT: **Q1AE E534** MOV A, RCVDAT MOV C, P1.5 ;LOAD THE NEXT BIT INTO RCVDAT 01B0 A295 RRC A 01B2 13 MOV RCVDAT, A 01B3 F534 01B5 80AE SJMP TOEX2 RXBITEX: 01B7 C276 CLR RXFLAG ;RECEPTION COMPLETE MOV A, RCVDAT 01B9 E534 01BB 207209 JB FIN, FINISH ; WAS THIS THE INITIAL/FINAL ;MESSAGE 01BE 20711E JB TSET, SPEED ;WAS THIS THE SPEED MESSAGE JB FORM, FF 01C1 206F78 ;WAS THIS THE FORMFEED MESSAGE 01C4 207009 JB PPS, PORT1 ;; WAS THIS THE PORT MESSAGE FINISH: 01C7 B45908 CJNE A, #59H, OUT1 ;'Y' RECEIVED ?

The Cybernetic Micro Systems 8051 Family Assembler, Version 3.04 25-11-92 01CA C272 CLR FIN 01CC D26D SETB RAM ; INDICATE TRANSMISSION OF LAST ;MESSAGE 01CE 4166 AJMP OUT PORT1: 01D0 4152 AJMP PORT OUT1: 01D2 B44E06 CJNE A, #4EH, OUT5 ;'N' RECEIVED ? 01D5 C272 CLR FIN 01D7 D271 SETB TSET ;SPEED MUST BE SET UP 01D9 4166 AJMP OUT OUT5: ;MESSAGE HAS TO BE 01DB D26E SETB REP ;REPEATED 01DD 4166 AJMP OUT . ٠ SPEED: 01DF B43910 CJNE A, #39h, FOUR ;9600 ? 01E2 D27C SETB NIN D1E4 C27D CLR FOU D1E6 C278 CLR TWO CLR ONE D1E8 C27E DIEA C27F CLR THR CLR TSET D1EC C271 SETB FORM DIEE D26F ;FORMFEED MESSAGE IS NEXT 01F0 4166 AJMP OUT FOUR: 01F2 B4B410 CJNE A, #OB4H, TWEE ;4800 ? 01F5 D27D SETB FOU 01F7 C27C CLR NIN 01F9 C278 CLR TWO CLR ONE 01FB C27E CLR THR 01FD C27F CLR TSET 01FF C271 SETB FORM ;FORMFEED MESSAGE IS NEXT 0201 D26F AJMP OUT 0203 A166 TWEE: 0205 B4B20E CJNE A, #0B2H, EEN ;2400 ? 0208 D278 SETB TWO 020A C27C CLR NIN D20C C27D CLR FO CLR THR 020E C27F CLR TSET ;FORMFEED MESSAGE IS NEXT 0210 C271 0212 D26F SETB FORM 0214 4166 AJMP OUT

The	Cybernetic	Micro	Systems	8051	Family	Assem	bler,	Version	3.04 25-11-92	
02 02 02 02 02 02 02 02 02 02 02	16 B4B110 19 D27E 1B C27C 1D C278 1F C27D 21 C27F 23 C27I 25 D26F 27 4166	EEN:		CJNE SETB CLR 1 CLR 1 CLR 1 CLR 1 SETB AJMP	A, #0B1H ONE NIN TWO FOU THR TSET FORM OUT	,DRIE ;IN	;1200) ? E FORMFEI	ED MESSAGE	IS NEXT
02 02 02 02 02 02 02 02 02 02	29 B4333A 2C D27F 2E C27C 30 C278 32 C27E 34 C27D 36 D26F 38 C271 3A 4166	DRIE:	•	CJNE SETB CLR 1 CLR 2 CLR 2 CLR 3 SETB CLR 2 AJMP	A, # 33H, THR NIN TWO DNE FOU FOU FOU ISET OUT	OUT ; ; IN	300 ? DICATH	E FORMFEI	ED MESSAGE	IS NEXT
02:02:02:02:02:02:02:02:02:02:02:02:02:0	3C B45908 3F D27B 41 C26F 43 D270 45 4166	FF:		CJNE SETB CLR I SETB AJMP	A, # 59H, FFON FORM PPS OUT	OUT3	;'Y' H ;SUPPH ;INDIC	RECEIVED RESS FORM CATE PORT	? MFEEDS I MESSAGE :	IS NEXT
024 024 024	47 B44E1C 4A C27B 4C C26F 4E D270 50 4166	OUT3 :		CJNE CLR I CLR I SETB AJMP	A, #4 EH, FFON FORM PPS OUT	OUT	;'N' I ; DO I ;INDIC	RECEIVED NOT SUPPI CATE PORT	? RESS FORMF I MESSAGE	EEDS IS NEXT
02: 02: 02: 02: 02:	52 B45008 55 D279 57 C270 59 D272 5B 4166	PORT:		CJNE SETB CLR I SETB AJMP	A, # 50H, PAR PPS FIN OUT	OUT4	; 'P' ; PARI ;INIT ;NEXT	RECEIVEI ALLEL OPI IAL/FINAJ	D ? ERATION L MESSAGE	IS
D2:	5D B45306	OUT4:		CJNE	A, ≸ 53H,	OUT	;'s']	RECEIVED	?	

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Fhe	Cybernet	ic Micro	Systems	8051	Family	Assem	bler,	Versio	on 3	.04 25-:	11-	-92	
026	50 C279			CLR I	PAR		; SERI	IAL OP	ERAT	ION			
026 026	52 C270 54 D272			CLR I SETB	PPS FIN		;INITI ;NEXT	AL/FI	NAL	MES	SAC	GE IS	
026 026	6 D273 8 2163	OUT:		SETB AJMP	GO TOEX1		;SET 1	TRANSM	ISSI	ON :	STI	ART FLAG	
and a state of the		;******	*******	****1	THE FETC	CH BYT	'E ROUI	TINE***	****	***	**1	*****	
026	A COEO C 7800	MESS:	•	PUSH MOV H	ACC R0,#0		;SAVE ;R0 VA ;BYTE ;CURRE	CONTEN ALUE IN IN THI ENTLY 1	NTS NDIC E ME FRAN	OF ATE SSA SMI	ACC S V GE TTI	CUMULATOR WHICH IS ED.	
026 026	E E8 F 93	MES1:	-	MOV A MOVC	A,RO A,@A+DI	PTR	;LOAD ;TEL	BYTE (ro x	MIT	т	D MINI-	
مرد می از این از ای مرد با این از		;******	******	**THF	E PARITY	ROUT	INE***	*****	* * * *	***	***	******	* *
a de la compañía de l		;COUNT E	ITS IN E	BYTE I	THAT ARE	SET.	IF IT	T IS A	N OD	DN	UME	BER THEN	
an a		;BIT7 MU	IST BE SE	ET. IN	TIT IS	AN EV	'EN NUN	ABER TI	HEN	BIT	71	IUST BE	
and a second	-	;RESET.											
027 027 027	0 7F00 2 30E001 5 0F			MOV F JNB A INC F	87, ≇ 00H ACC.0,B] 87	T 0		;IS B	IT O	-	0 1	?	
027 027	6 30E101 9 OF	BITO:		JNB F INC F	ACC.1,B] 87	.T1		;IS B	IT 1	. =	o <i>'</i>	?	
027	A OF	BIT1:		INC F	27								
027 027	B 30E301 E OF	BIT2:		JNB A INC H	ACC.3,B] 87	[T3		;IS B	IT 3	; =	0	?	

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The Cybernetic Micro Systems 8051 Family Assembler, Version 3.04 25-11-92 BIT3: 027F 30E401 JNB ACC. 4, BIT4 ; IS BIT 4 = 0? 0282 OF INC R7 BIT4: 0283 30E501 JNB ACC. 5, BIT5 ; IS BIT 5 = 0? 0286 OF INC R7 BIT5: 0287 30E601 JNB ACC. 6, BIT6 ; IS BIT 6 = 0 ? 028A OF INC R7 ; CHECK IF THERE IS AN EVEN OR ODD NUMBER OF ONES IN THE BYTE BIT6: 028B BF0104 CJNE R7, #01, BIT7 028E D2E7 SETB ACC.7 ;SET THE PARITY BIT 0290 41A9 AJMP PARITY BIT7: 0292 BF0304 CJNE R7, #03, BIT8 ;SET THE PARITY BIT 0295 D2E7 SETB ACC.7 AJMP PARITY 0297 41A9 BIT8: 0299 BF0504 CJNE R7, #05, BIT9 029C D2E7 SETB ACC.7 ;SET THE PARITY BIT 029E 41A9 AJMP PARITY BIT9: CJNE R7, #07, BIT10 Q2A0 BF0704 ;SET THE PARITY BIT 02A3 D2E7 SETB ACC.7 AJMP PARITY Q2A5 41A9 BIT10: 02A7 C2E7 CLEAR THE PARITY BIT CLR ACC.7 ;CHECK IF THIS IS THE END OF Q2A9 B40003 CJNE A, #0, SEND PARITY: ;THE MESSAGE Q2AC DOEO POP ACC 02AE 22 RET SEND: Q2AF 3136 ACALL XMTBYTE ;START TO CLOCK OUT THE BYTE ;SERIALLY 02B1 08 INC RO ; MOVE POINTER TO NEXT BYTE OF rhe Cybernetic Micro Systems 8051 Family Assembler, Version 3.04 25-11-92 :MESSAGE 02B2 80BA SJMP MES1 ; ī ;############# OA = LF ;############ 8D = CR ;############ OC = FF MSG2: DB 08DH, OCH 02B4 8D 0C 02B6 45 4E 54 DB 'ENTER SPEED' 02B9 45 52 20 53 50 45 45 44 02C1 8D 0A 0A DB 8DH, OAH, OAH 02C4 20 39 20 DB ' 9 = 9600Bps' 02C7 3D 20 39 36 30 30 42 70 73 02D0 8D 0A DB 8DH, OAH DB ' 4 = 4800Bps' 02D2 20 34 20 02D5 3D 20 34 38 30 30 42 70 73 OZDE 8D OA DB 8DH, OAH 02E0 20 32 20 DB / 2 = 2400Bps'02E3 3D 20 32 34 30 30 42 70 73 02EC 8D OA DB 8DH, 0AH 02EE 20 31 20 DB / 1 = 1200Bps' 02F1 3D 20 31 32 30 30 42 70 73 02FA 8D OA DB 8DH, OAH 02FC 20 33 20 DB ' 3 = 300Bps' 02FF 3D 20 33 30 30 42 70 73 0307 8D 0A DB 8DH, OAH DB 'ENTER CHOICE : ', OH 0309 45 4E 54 030C 45 52 20 43 48 4F 49 43 45 20 0316 3A 20 00 MSG3: 0319 8D 0C · DB 8DH, OCH DB 'SUPPRESS FORMFEEDS? (Y/N)', OH 031B 53 55 50 031E 50 52 45 53 53 20 46 4F 52 4D 0328 46 45 45 44 53 3F 20 28 59 2F 0332 4E 29 00 MSG1: 0335 8D 0C DB 8DH, OCH DB 'CONFIGURATION OF THE INTERFACE MODULE' 0337 43 4F 4E 033A 46 49 47 55 52 41 54 49 4F 4E ⁰³44 20 4F 46 20 54 48 45 20 49 4E ⁰³4E 54 45 52 46 41 43 45 20 4D 4F 0358 44 55 4C 45 035C 8D 0A 0A 035F OA OA OA OA OA OA 0365 43 55 52 DB 'CURRENT CONFIGURATION : SPEED=', OH

The Cybernetic Micro Systems 8051 Family Assembler, Version 3.04 041C 20 50 41 52 41 4C 4C 45 4C 20 0426 50 4F 52 54 042A 8D 0A 0A 042D OA OA OA OA OA DB 'IS THE CONFIGURATION CORRECT? (Y/N)',0 0432 49 53 20 0435 54 48 45 20 43 4F 4E 46 49 47 043F 55 52 41 54 49 4F 4E 20 43 4F 0449 52 52 45 43 54 3F 20 28 59 2F 0453 4E 29 00 MSG109: 0456 8D 0A DB 8DH, OAH 0458 20 20 20 DB ' SERIAL PORT' 045B 20 20 20 20 20 20 20 20 20 20 20 20 0465 20 20 20 20 20 20 20 20 20 20 20 046F 20 53 45 52 49 41 4C 20 50 4F 0479 52 54 MSG4: DB 8DH, OAH, OAH, OAH, OAH, OAH, OAH, OAH 047B 8D 0A 0A 047E OA OA OA OA OA DB 'IS THE CONFIGURATION CORRECT? (Y/N)',0 0483 49 53 20 0486 54 48 45 20 43 4F 4E 46 49 47 0490 55 52 41 54 49 4F 4E 20 43 4F 049A 52 52 45 43 54 3F 20 28 59 2F 04A4 4E 29 00 MSG5: 04A7 8D 0C DB 8DH, OCH DB 'SELECT PARALLEL OR SERIAL OPERATION' 04A9 53 45 4C 04AC 45 43 54 20 50 41 52 41 4C 4C 04B6 45 4C 20 4F 52 20 53 45 52 49 04C0 41 4C 20 4F 50 45 52 41 54 49 04CA 4F 4E 04CC 8D OA DB 8DH, OAH 04CE 50 20 3D DB 'P = PARALLEL'04D1 20 50 41 52 41 4C 4C 45 4C 04DA 8D OA DB 8DH, OAH DB 'S = SERIAL' 04DC 53 20 3D 04DF 20 53 45 52 49 41 4C 04E6 8D 0A DB 8DH, OAH DB 'MAKE SELECTION (P/S)', OH 04E8 4D 41 4B 04EB 45 20 53 45 4C 45 43 54 49 4F 04F5 4E 20 28 50 2F 53 29 00 MSG6: DB 8DH, OCH 04FD 8D OC DB 'CONFIGURATION OF THE INTERFACE MODULE' 04FF 43 4F 4E 0502 46 49 47 55 52 41 54 49 4F 4E **10**50C 20 4F 46 20 54 48 45 20 49 4E

The Cybernetic Micro Systems 8051 Family Assembler, Version 3.04 25-11-92 0516 54 45 52 46 41 43 45 20 4D 4F 0520 44 55 4C 45 0524 8D OA DB 8DH, OAH 0526 49 53 20 DB 'IS NOW COMPLETE.' 0529 4E 4F 57 20 43 4F 4D 50 4C 45 0533 54 45 2E 0536 8D OA OA DB 8DH, OAH, OAH 0539 52 45 46 DB 'REFER TO THE "MINITEL USERS GUIDE", IF' 053C 45 52 20 54 4F 20 54 48 45 20 0546 22 4D 49 4E 49 54 45 4C 20 55 0550 53 45 52 53 20 47 55 49 44 45 055A 22 2C 20 49 46 055F 8D 0A DB 8DH, OAH 0561 4E 45 43 DB 'NECESSARY, AND CONFIGURE THE PERIPHERAL 0564 45 53 53 41 52 59 2C 20 41 4E Q56E 44 20 43 4F 4E 46 49 47 55 52 0578 45 20 54 48 45 20 50 45 52 49 0582 50 48 45 52 41 4C 0588 50 4F 52 DB 'PORT OF THE MINITEL TERMINAL. (SEE P.28)', OH 058B 54 20 4F 46 20 54 48 45 20 4D 0595 49 4E 49 54 45 4C 20 54 45 52 Q59F 4D 49 4E 41 4C 2E 20 28 53 45 Q5A9 45 20 50 2E 32 38 29 00 RRESET: JB PAR,BEGIN MOV IE,**≸**00H ; PARALLEL OR SERIAL OPERATION 95B1 20790E 95B4 75A800 ;DISABLE INTERRUPTS SERIAL: ;COPY PO.0 TO PO.1 95B7 308004 JNB PO.O, SEREAL 05BA D281 SETB P0.1 95BC 80F9 SJMP SERIAL SEREAL: 05BE C281 C 05C0 80F5 C CLR P0.1 SJMP SERIAL ;DEFINE BITS AND REGISTERS BEGIN: RRXFLAG BIT 77H RRXERR BIT 76H RRCVRDY BIT 75H XOF BIT 74H XON BIT 73H XF BIT 72H XN BIT 71H 0077 = RRXFLAG BIT 77H 0076 =0075 = 0074 =0073 =072 = 0071 =

The	Cybernetic	Micro	Systems 8051 Family	y Assembler, Version 3.04 25-11-92
	70 —		VNO DIE 20U	
	10 - 11 750125		MOU GD #25U	
	2 750135		MOV SP, #35R	
	,3 /3A003		MOV TE,#USSA	
050	0000C1 8.		CIP PRYETAC	
	$\frac{1}{2} \frac{1}{2} \frac{1}$		CLR REAFLAG	
	D C276		CLA KRALKK	
050	r (275)			FLOW CONTROL FLAGS
05L	$\frac{1}{2} \frac{1}{2} \frac{1}$		CLR XOR	THOW CONTROL THREE
LOST LOST	15 C274		CLP YF	
051	17 (272		CLR XN	
050	9 0271		CLR XNO	· · · · · · · · · · · · · · · · · · ·
050	B 750000		MOV PSW #00H	
050)F 7590FF		MOV P1 #OFFH	INTTIALISE PORTS 1 AND 3
05 5	1 7580FF		MOV P3 #OFFH	<i>finitimita</i> fonto = 00.0 0
05 F	4 D281		SETB PO. 1	MINITEL RXD
05	6 7803		MOV R0. #03H	INTERNAL RAM POINTERS
05 F	8 7903		MOV R1, #03H	,
055	A 307C10		TNB NIN WATT	
05 F	'D 73FF		MOV R2. #OFFH	SETUP TIMER REGS. FOR 9600BPS
05F	F SASA		MOV SAH R2	,
05F	1 7AFF		MOV R2. #0FFH	
05F	3 8A8C		MOV 8CH.R2	
05F	5 7AFF		MOV R2. #0FFH	
05F	7 888D		MOV 8DH.R2	
05F	9 7883		MOV R2. #0A3H	
05F	B 8A8B		MOV 8BH, R2	
4		WAIT:		
05F	D 208CFD		JB 8CH,WAIT	; IS TIMER RUNNING ?
060	0 208BFA		JB 8BH,WAIT	; IS EXTERNAL INTERRUPT SERVICED ?
060	3 D113		ACALL LOAD	
060	5 307309		JNB XON, BITE	
060	8 D271		SETB XN	; INDICATE THAT XON IS XMITTE
060	A D28C		SETB 8CH	; START TIMER
060	C 75310A		MOV CNT,#OAH	
060	F A1FD		AJMP WAIT	
		BITE:		
061	1 A1FD		AJMP WAIT	
	_	LOAD:		EVIN TE DETNMED TE DUCY
001	.3 20962A		JE PI.6, EXLOAD	JEAN IF PRIMIER IS DUST
1001	.6 08		INC RU	
1001	./ E9		MOV A,RI	
1001	.8 98		SUBB A, RU	,15 THERE BUTTERED DATA
Loo T	9 5012		JNC LOAD2	
061	.в СЗ		CLR C	
0001	C C2A8		CLR EXU	
062	L /803		MOV RU, FUSA	
Ine-	0 7903		MUV KI, FUJN CEMP EVA	
1060	4 UZA8		SEID EAU	HAS MINIGEL DECEIVED YORE
0602	4 307219		UND AF, EALUAU	TNDTCATE THAT SHEFED IS CLEAD
1062	1 D273		SEID AUN	JUDICALE HIML BUFFER 15 CHEAR
_∰.ЩU∠	- C272		ULK AF	

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The C	ybernetic	Micro Sys	stems 8051 Famil	y Assembler, Version 3.04 25-11-92
06A7 06A9 06AB 06AD 06AF 06B1	8A8C 7AFD 8A8D 7A00 8A8B C1C3		MOV 8CH,R2 MOV R2,#0FDH MOV 8DH,R2 MOV R2,#00H MOV 8BH,R2 AJMP SSPEED	
06B3 06B5 06B7 06B9 06BB 06BD 06BF 06C1	7A23 8A8A 7AFA 8A8C 7AF4 8A8D 7A00 8A8B	TTHREE:	MOV R2, #23H MOV 8AH, R2 MOV R2, #0FAH MOV 8CH, R2 MOV R2, #0F4H MOV 8DH, R2 MOV R2, #00H MOV 8BH, R2	;IS SPEED 300BPS ?
06C3 06C6 06C8 06CA 06CC	753000 C2A8 D28C D277 32	SSPEED;	MOV XMTDAT, #0H CLR EX0 SETB 8CH SETB RRXFLAG RETI	;DISABLE EXTERNAL INTERRUPTS ;START TIMER ;INDICATE RECEPTION IS IN PROGRESS
06CD 06CF 06D1	F532 927F A295	TTIMR0:	MOV LOOPCNT, A MOV THR, C MOV C, P1.5	;STORE CONTENTS OF A IN LOOPCNT ;STORE CONTENTS OF CARRY IN THR ;STORE NEXT BIT FROM MINITEL IN PAR ;VIA CARRY FLAG.
06D3 06D5	9279 207709		MOV PAR,C JB RRXFLAG,RRXE	Ĩ
06D8	C28C	TTOEX1:	CLR 8CH	;STOP TIMER
06DA 06DC 06DE 06E0	C270 A27F E532 32	TTOEX2:	CLR XNO MOV C,THR MOV A,LOOPCNT RETI	;INDICATE THAT XON HAS BEEN TRANSMITTED ;RESTORE CARRY FLAG ;RESTORE ACCUMULATOR
06E1 06E4 06E7 06E9 06E9	D5311E 208106 D281 C271 D270	RRXBIT:	DJNZ CNT, RRXBUS JB P0.1, EXIT9 SETB P0.1 CLR XN SETB XNO	ςΥ
06ED 06F0 06F2 06F4 06F5 06F5	2070E8 C277 C275 09 E530 F7	EXIT9:	JB XNO,TTOEX1 CLR RRXFLAG CLR RRCVRDY INC R1 MOV A,XMTDAT MOV @R1,A	

e Cybernetic	Micro Sy	stems 8051 Family As	sembler, Ver:	sion 3.04 25-11-92
6F8 E9 6F9 B42002 6FC D274		MOV A,R1 CJNE A,#20H,XLOAD SETB XOF	;IS INTERNA ;INDICATE TH	L RAM FULL ? IAT XOFF MUST BE SENT
6FE D2A8 700 80D6	XLOAD:	SETB EXO SJMP TTOEX1		
702 E531 704 B4090A 707 207403 70A 307102	RRXBUSY	: MOV A, CNT CJNE A, #9, RRXNEXT JB XOF, OK5 JNB XN, EXIT8		
70D C281	OK5:	CLR P0.1		
70F 80C9	EXIT8:	SJMP TTOEX2		
711 E530 713 A279 715 13 716 F530 718 307102 718 F146	RRXNEXT	: MOV A,XMTDAT MOV C,PAR RRC A MOV XMTDAT,A JNB XN,OK6 ACALL TIMR2		
71D 307400	OK6:	JNB XOF, EXIT		
720 80B8	EXIT7:	SJMP TTOEX2		-
722 E531 724 B40803 727 D281 729 22	TIMR1: M C S R	OV A,CNT JNE A,#8,LLL ETB P0.1 ET		
72A B40603 72D C281 72F 22	LLL: C C R	JNE A, # 6,QQQ Lr P0.1 ET		
730 B40403 733 D281 735 22	QQQ: C S R	JNE A,#4,RRR ETB P0.1 ET		
⁷ 36 B40303 ⁷ 39 C281 ⁷ 3B 22	RRR: C C R	JNE A,#3,SSS LR P0.1 ET		

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ie Cy	ybernetic	Micro Systems 8051 Family Assembler, Version 3.04 25-11-9
1		SSS:
073C	B40106	CJNE A, #1, EXIT
73F	D281	SETB P0.1
741	D272	SETB XF
743	C274	CLR XOF
		EXIT:
745	22	RET
		TIMR2:
746	E531	MOV A, CNT
1748	B40804	CJNE A, #8, LLLL
174B	D281	SETB P0.1
174D	E169	AJMP EX176
in a l'internet		LLLL:
74F	B40704	CJNE A, #7, PPPP
752	C281	CLR P0.1
754	E169	AJMP EXIT6
al de altre de		PPPP:
756	B40604	CJNE A,#6,QQQQ
759	C281	CLR P0.1
75B	E169	AJMP EXIT6
		QQQQ:
75D	B40404	CJNE A, #4, RRRR
760	D281	SETB P0.1
762	E169	AJMP EXIT
L'anna airte		RRRR:
764	B40302	CJNE A,#3,EXIT6
767	C281	CLR P0.1
		EXIT6:
769	22	RET
		;8E
000		END

ne Cybernetic Micro Systems 8051 Family Assembler, Version 3.04 25-11-92

e															
;%T	Sy	mb	01	N	Ian	ie							тур	e	Value
BAUDVA	L				•	•		•	•				•	I	FD00
BEGIN														L	05C2
BITO.	-													T.	0276
BIT1.		-	-	-										T.	027A
ATT10														Ť.	0247
втт 2 .	•	•				•	•				•			T.	0278
87ጥ3	•	•	•			•	•	•	•	•	•		•	<u>т</u> .	0275
ятт4.	•	•	•	•	•	•	•	•	•	•	•		•	T.	02271
ATTS	•	•	•	•	•	•	•	•	•	•	•	•	•	T.	0205
ATTE	•	•	•	•	•	•	•	•	•	•	•	•	•	Т.	0207
110. 1707	•	•	•	•	•	•	•	•	•	•	•	•	•	ц т	0200
RTTTO	•	•	•	•	•	•	•	•	•	•	•	•	•	ц т	0292
110. 1700	•	•	•	•	•	•	•	•	٠	•	٠	•	•	ц т	0233
113. TTCNT	•	•	٠	•	•	•	•	•	•	•	•	•	•	л Ц	02A0
TUCNT TUDE	•	•	•	•	•	•	•	•	•	•	•	٠	•	U T	0033
HITE.	•	٠	•	•	•	•	•	٠	•.	•	٠	٠	•	ц Б	0611
	•	•	•	•	•	•	•	•	•	•	•	٠	•	D	0031
	•	•	•	•	•	•	•	٠	•	•	•	٠	٠	В -	0069
ELAY	•	•	•	•	•	٠	•	•	•	•	٠	•	٠	Ē.	0,062
ELAY1	•	•	•	•	•	•	•	•	•	•	•	•	-	F.	0078
RIE.	•	•	•	•	•	•	•	•	•	•	•	٠	•	L	0229
AEN .	٠	•	•	•	٠	•	•	•	•	•	•	٠	•	L	0216
EXINT	0	•	•	•	•	•	٠	٠	•	•	٠	٠	•	L	0670
XINTO	•	•	•	•	•	•	•	•	•	•	•	٠	•	L	0183
XIT.	•	•	•	•	•	•	•	•	•	•	•	٠	٠	L	0745
XIT6	•	•	•	•	•	•	•	•	•	•	•		•	L	0769
XIT7	•		•	•	•	•	•	•	•	•	•	•	•	L	0720
XIT8	•		•	•	•	•	•	•	•	•	•			\mathbf{L}	070F
XIT9	•	•		•	•	•	٠	•	•	•	•	•	•	L	06ED
XLOAD	•		•	•	•		•	•		•			•	L	0640
XLOAD	1		•	•		•		•			•		•	L	0636
F	-	•									•	•	•	L	023C
FON.			-	_										в	007B
FOUR	-										-			Ŀ	0676
IN		•		-						-				B	0072
IN1	•	•	•	•	•	•	•					-		R	006A
INTSH	•	•	•	•	•	•	•	•	•	•	•		•	T.	0107
ORM	•	•	•	•	•	•	•	•	•	•	•		•	R	006F
URME	•	•	•	•	•	•	•	•	•	•	•	•	•	B	0060
icii Cii	•	•	•	•	•	•	*	•	•	•	•	•	•	D R	0000
atio	•	•	•	•	•	•	•	•	•	•	•	•	•	D T	0070
601	•	•	•	•	•	•	•	•	•	•	•	•	•	TT T	0112
	•	•	•	•	•	•	•	•	•	•	•	•	•	<u>ь</u>	0000
Ext	•	•	٠	•	•	•	•	•	•	•	•	٠	٠	В -	0073
5-11 1 T	•	•	•	•	•	•	•	•	٠	٠	•	•	•	<u>т</u>	0125
lili Tra	•	•	•	•	•	•	•	•	•	٠	٠	٠	٠	Ц.	072A
	•	•	•	•	•	•	٠	•	•	•	•	•	•	Ŀ	074F
NAD.	•	•	•	•	•	•	•	•	•	•	•	٠	•	L	0613
1D2	•	•	•	•	•	•	•	•	٠	•	•	٠	•	L	062D
0.	•	•	•	•	•	•	•	•	•	•	•	•	•	L	00B3
3001	•	•	•	•	•	•	•	•	•	•	•		•	L	00C8
3002	•	•	•	•	•	•	•	•	•	•	•	•	•	L	OOCF
3003	•	•	•	•	•	•	•	•	•	•	•	•	•	L	00D6
3004	•		•			•		•	•		•		•	L	00DD

.0G O	05	•	•	•	•	•		•	•	•	•	•	•	•	L	00E4
,0G O	1		•	•	•			•	•	•	•		•	•	\mathbf{L}	00E9
,0G O	10	1	•		•		•			•	•	•	•	•	L	00F5
,0 60	2	•	•	•	•				•	•	•		•	•	L	OOFE
JOGO	20	1						•							\mathbf{L}	010A
00G	00	-		-	-			-	-						T.	0134
.00P	1									•		•			T.	007B
	2	•	•	•	•	•	•	•	•	•	•	•	•	•	Ť.	0122
	CN	• ጥ	•	•	•	•	•	•	•	•	•	•	•	•	n	0120
1005	CN	Ŧ	•	٠	•	•	•	•	•	•	• .	•	•	•	D T	0032
LEST LECT	•	•	•	•	•	•	•	•	•	•	•	•	•	•	ц т	0205
ILSZ	•	•	•	•	•	•	•	•	•	•	٠	•	•	•	Ц т	0081
IES4	•	•	•	•	•	•	•	•	•	•	•	•	•	٠	Ц Т	0097
ILSO Marca	•	•	•	•	•	•	•	•	•	•	•	•	•	•	÷.	0095
HrS6	•	•	•	•	•	•	٠	٠	•	•	•	•	•	•	Ц т	00A6
HES7	•	•	•	•	٠	•	•	•	•	•	•	•	•	•	L	OOAE
MESS	•	•	•	•	•	•	•	•	٠	•	•	٠	•	٠	L	026A
MSG1	•	•	•	•	•	•	٠	•	•	•	•	•	•	٠	L	0335
ISG1	01	•	•	•	•	•	٠	•	•	•	•	•	•	٠	L	0384
U SG1	02	•	•	•	•	•	•	•	•	•	•	•	•	•	\mathbf{L}	038D
ISG1	03						•		•	•	•		•	•	L	0396
ISG1	04		•	•	•	•	•	•	•	•	•			•	L	Q39E
ISG1	05		•		•	•		•	•	•		•	•	•	\mathbf{L}	03A7
ISG1	06					_			•				•	•	L	03B0
MSG1	07						-								\mathbf{L}	03D9
MSG1	08		-	-			-	-				-			L	0403
ISCI	60	•	•	•	•	•				•	-			-	T.	0456
HSC2	00	•	•	•	•	•	•	•		•	•	•			T.	0284
1002	•	•	•	•	•	•	•	•	•	•	•	•	•	•	<u>т</u> .	0219
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1366	•	•	•	•	٠	•	•	•	•	•	•	•	•	٠	ц Г	04PD
ATN -	•	•	•	•	•	•	•	•	•	٠	•	•	•	•	В	0070
VK5	•	•	•	•	•	•	٠	•	•	•	•	٠	•	•	ц Т	0700
UK6	•	•	• .	•	٠	•	•	•	•	•	•	•	•	٠	Γ.	0710
ONE	•	•	•	•	•	•	•	٠	•	•	•	•	•	٠	В	007E
CONE	•	•	•	•	•	•	•	•	•	•	•	٠	٠	•	L	069E
OUT	•	•	•	•	•		•	•	•	•	•	•	•	•	\mathbf{L}	0266
QUT1	•	•	•	•	•		•	•	-	•	•	•	•	•	L	01D2
OUT3	•		•	÷	•	•	•	•	•	•	•		•	•	L	0247
OUT4									•		•		•	•	L	025D
0UT5													•	•	L	01DB
PAR				-					_						В	0079
PART	тv т	•			•	•			-		-				L	02A9
FORT	* *	•		•	•	•									Ē	0252
POPT	1	•	•	•	•	•	•	•	•	•	•	•			B	0068
POPm	+ v	•	•	•	•	•	•	•	•	•	•	•	•	•	τ.	0100
Pppp	I	•	•	•	•	•	•	•	•	•	•	•	•	•	T.	0756
PDC PDC	•	•	•	•	•	•	•	•	•	•	•	•	•	•	2	0130
e co Dom	•	•	•	•	*	•	•	•	•	•	•	•	•	•	D T	0070
AT.	•	•	•	•	•	•	٠	•	•	•	•	•	•	•	14 7	UIII
RT1	•	•	•	•	•	•	•	•	•	•	•	•	•	•	ь -	0120
KT2	•	•	•	•	•	•	٠	•	•	٠	•	•	•	•	Ŀ	0123
ΨŲQ	•	•	•	•	•	•	٠	•	•	•	•	٠	•	•	$\mathbf{\Gamma}$	0730
KQQQ	•	•	•	•	•	•	•	•	•	•	•	•	•	•	Г	075D
XAM	•	•	•		•	•	•	•	•	٠	•	•	•	•	В	006D
RAM 1		_			_		_								В	007A

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RCVDAT	.	•		•	•	•	•	•	•	•	٠	٠	•	D	0034
RCVRDY												•		В	0074
סייס	•	-	-	-	•	-	+	•	-	•	-	-	•	- -	0068
KEF .	<u>.</u>	•	•	•	•	•	•	•	•	•	•	•	•	0	1000
RRCVRD	Y.	•	•	•	•	•	٠		•	•		•		B	0075
RRESET	•		•	•	•	•		•	•		•	•		L	05B1
RRR							_							Τ.	0736
	•	•	•	•	•	•	•	•	•	•	•	•	•	÷	0730
RRRR.	•	٠	•	•	•	•	٠	•	٠	•	•	•	•	ч	0764
RRXBIT	•	•	•	•	•	•	٠	•	•	•		٠	•	L	06E1
RRXBUS	Y							•		•	•			L	0702
DDYFDD	-	-	-	-	-	-		-	-		-	-	Ť		0076
NALAR		•	•	٠	•	٠	•	•	•	•	•	•	•	5	0070
REXELA	G	•	•	•	•	•	٠	•	•	-	•	•	٠	В	0077
RRXNEX	T	•			•	•		•	•			•		\mathbf{L}	0711
RSXMT	_	_	_	_	-	_						_		T.	0138
DVDTM	•	•	•	•	•	•	•	•	•	•	•	•	• .	÷	0130
KADIT.	•	•	•	•	•	•	*	•	•	•	•	•	٠	<u>ц</u>	UIA2
RXBITE	X	•	•	•	•	•	٠	•	•	•		٠	•	L	01B7
RXBUSY	•		•	•	•	•		•	•	•	•			L	01A7
RXFRR														в	0075
DVDING	•	•	•	•	•	•	•	•	•	•	•	•	•	5	0075
RAFLAG	•	٠	٠	•	•	*	• 1	•	٠	•	٠	٠	٠	В	0076
RXNEXT	•		•	•	•	•	•	•	•	•	•	-	•	L	OIAE
SEND.			_		_			_		_				τ.	02AF
SEDENT	•	•	•	•	•	-	•	-	•	•	•	•		Ŧ	OFPE
SEREAL	•	•	•	•	•	•	٠	•	•	•	•	•	٠	1	adc
SERIAL	•	•	•	•	•	•	•	•	•	•	•	•	•	L	05B7
SET1.						•						•	-	L	0008
SET 2	•		-	•			-		•	-	•		•	T.	0013
CDDDD	•	•	•	•	•	•	*	•	•	•	•	•	•	-	0015
SPEED	٠	٠	•	٠	•	٠	٠	٠	٠	•	•	•	٠	Ч	OIDF
SSPEED		•	•					•	•	•				\mathbf{L}	06C3
SSS .		_			_				_	-		-		T.	0730
STEDTER	÷	•	•	•	•	•	•	•	•	•	•	•	•	Ŧ	EE03
SIRIVA	بل.	•	•	•	•	•	•	•	•	•	•	•	•	<u> </u>	FE93
TOEX1	•	•	•		•	•	•	٠	•	•	•	•	٠	L	0163
TOEX2	•				•	•		•		•	•	•		\mathbf{L}	0165
THR		-	-	-										R	0075
TIMO	•	•	٠	•	•	•	•	•	•	•	•	•	•	Ŧ	0150
IIMRU	•	•	٠	•	•	•	٠	•	•	•	•	•	٠	Ŀ	0123
TIMR1	•	•	٠	•	•	•	•	•	•	•	•	•	•	\mathbf{L}	0722
TIMR2		-	_							_	-		_	L	0746
TCET	-	-	•	•	•	•	•	•	•	•	-	•	-	b	0071
TOTIT.	•	•	•	•	•	•	¢	•	•	•	٠	•	•	5	0071
TTOEX1	•	•	•	•	•	•	•	•	•	•	•	•	•	$\mathbf{\Gamma}$	06D8
TTOEX2										-				L	06DA
TTUDEE	•	•	•	-	•	•	•	-	•	-	-	-	-	T	0693
MULTINE E	•	•	•	•	•	•	•	•	•	•	•	•	•	-	0000
TTIMRO	•	•	•	•	•	٠	•	•	٠	•	•	٠	•	L	06CD
TTWO.					•			•	•	•		•		\mathbf{L}	0689
TWEE		•	•											Τ.	0205
TWO	•	•	•	•	•	•	•	•	٠	•	•	•	•	5	0205
INO .	•	•	٠	٠	٠	•	•	•	•	٠	٠	•	٠	в	0078
TXBIT	•	•	•		•	•			•	•	•	•		L	016A
TXBUSY	_	_	_		_	<u>.</u>	_	_		_			-	T.	0171
TYPINC	•	•	•	•	•	•	•	•	•	•	•	•	•		0077
THAG	•	•	•	*	•	•	•	•	•	•	•	•	•	<u>р</u>	0077
TXNEXT	•		•	•	•	•	•	•	•	•	•	•	•	\mathbf{L}	017A
TXX .										•			-	В	0081
WATT	-	-	•	•	•	•	•	•	-	•	-	-	-	Ŧ	0520
Yes	•	•	•	٠	•	•	•	•	•	٠	•	•	•	5	OSFD
AF	•	•	•	*	٠	٠	•	•	•	•	٠	*	•	В	0072
^X LOAD	•				•	•			•			•		L	06FE
XMTRVm	F		-						_					Τ.	0136
XMmr-	نل.	•	•	•	•	•	•	•	•	•	•	•	٠		0000
-441 UAT	•	•	٠	٠	•	٠	٠	•	•	•	٠	٠	٠	U	0030
AN .	•	•	•		•		•	•	•	•	•	•	•	В	0071
XNO _			-	•		-	-					•	•	В	0070
XOF	-	-	-	-	-	~	-	~	-	-	-	•	-	R	0074
	٠	•	٠		•	•	٠	•				•	٠	-	







7.2 The 87C751 Model.

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7.2.1 The Configuration Routine.





A = SUBROUTINE 'MESS'

B = SUBROUTINE 'XMTBYTE'





































8. The Operating Instructions.

8.1 The 8031 Model.

Set up the the dipswitches according to the following table:

Suppress formfeeds: switch 1 = off
8-Bit data: switch 2 = on
Speed (Bps):

	switch 3	switch 4	switch 5
9600	off	off	off
4800	on	off .	off
2400	on	off	on
1200	on	on	off
300	on	on	on

Insert the 5-pin DIN plug of the adaptor into the 5-pin socket of the MINITEL peripheral port. Engage the bottom of the adaptor board into the peripheral slot and push it forward until the top clicks home.

The MINITEL terminal should now be switched on and the peripheral port should be set up according to the instructions in the Minitel Users Guide.

8.2 The 87C751 Model.

Insert the 5-pin DIN plug into the 5-pin DIN socket of the MINI-TEL terminal.

Switch the terminal on and press "FNCT MEM" to enter LOCAL MODE. The program in the 87C751 waits for 5 seconds and then transmits the following message to the MINITEL screen: " CONFIGURATION OF THE INTERFACE MODULE CURRENT CONFIGURATION : SPEED=1200Bps FF SUPPRESS ON

PARALLEL PORT

IS THE CONFIGURATION CORRECT ? (Y/N)"

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Enter either "Y" to indicate that the configuration is correct or "N" to indicate that the configuration is not correct. Any other character entered will cause the prompt to be re-transmitted to the MINITEL.

If "N" is entered the program will transmit the following message to the MINITEL screen:

- " ENTER SPEED
- 9 = 9600 Bps
- 4 = 4800Bps
- 2 = 2400 Bps
- 1 = 1200 Bps
- 3 = 300Bps "

Press '9' for operation at 9600Bps, '4' for operation at 4800Bps, '2' for operation at 2400Bps, '1' for operation at 1200Bps or '3' for operation at 300Bps.

Any other key will cause the program to retransmit the message to the MINITEL screen.

After pressing a valid key, the program will transmit the following message to the MINITEL screen:

" SUPPRESS FORMFEEDS? (Y/N)"

Press 'Y' to suppress formfeeds or 'N' to print them. Any other key will cause the program to retransmit the message.

After pressing a valid key, the following message will be transmitted to the MINITEL screen:

" SELECT PARALLEL OR SERIAL OPERATION

P = PARALLEL

S = SERIAL

MAKE SELECTION (P/S) "

Press 'P' for parallel operation or 'S' for serial operation. Any other key will cause the program to retransmit the message. After pressing a valid key, the operator is prompted to indicate whether the configuration is correct. If 'Y' is pressed the following message is displayed :

" CONFIGURATION OF THE INTERFACE MODULE IS NOW COMPLETE.

REFER TO THE 'MINITEL USERS GUIDE', IF NECESSARY AND CONFIGURE THE PERIPHERAL PORT OF THE MINITEL TERMINAL. (SEE P.28) "

Hereafter the adaptor enters operational mode.

It should be noted that the SOFTWARE SOLUTION assumes 7-BIT data with even parity since the MINITEL terminal does not support any other data format at present.

The PARALLEL or SERIAL selection activates either the parallel port or the serial port.

To change the configuration the MINITEL terminal should be reset, which will force the adaptor module to enter the configuration mode of operation.

9. <u>Problems Encountered</u>

9.1 Hardware Problems

False triggering of the timing signals was encountered.
 This problem was solved by using decoupling capacitors. (Both models)

2. Even though 5V was placed on A14 and A13, the program would not read a '1' on those pins until '1s' was eventually written into the pin latches. (8031 model)

9.2 Software Problems

1. Parallel operation at 9600BPS (87C751 model) initially produced errors on the output to the printer.

A 'race' problem was then diagnosed. When the internal RAM buffer is full and an XOFF has to be transmitted, the time available to sample one bit of the XOFF to the Minitel, is only 104 microseconds. The length of one clock cycle is 180 nanoseconds. One machine cycle is available between bits. (72 2-byte instructions or 48 3-byte instructions)

Solution: All routines involved in this process were optimised. Two of the measures taken to solve this problem illustrates clearly how critical the timing is:

 PUSH PSW was replaced with MOV THR,C. (Since only the Carry flag was used in the PSW Register, it was not necessary to store the whole PSW, but only the Carry flag). Valuable time was recovered by this measure.

2. PUSH ACC was substituted with a MOV instruction. Once again saving valuable time.

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10. Results.

In order to test the serial ports of the two models the TXD and RXD pins on the external RS-232 connector were connected by means of a loop plug. In the case of both models it was found that all characters transmitted from the MINITEL keyboard was successfully echoed back to the screen.

The parallel port was tested by connecting a printer with a Centronix interface to it. The screen of the MINITEL was then filled with characters. In ASCII mode the MINITEL screen displays a maximum of 2000 characters. 'CTRL P', which is the command to print the screen to a printer, was then repeatedly typed from the keyboard.

In the case of the 8031 Model, the first four print operations completed successfully. Subsequent printing resulted in errors.

In the case of the 87C751 Model, no errors were encountered during repetitive printing.

11. Conclusion.

The operation of the serial port is identical for both the 8031 and the 87C751 models and tested satisfactory in both cases.

The results of the tests performed on the parallel ports of the two models differed. This difference can be attributed to the fact that the 8031 does not implement any flowcontrol and relies on the data buffering only. The buffer fills after printing four pages and subsequent printing results in errors.

In the case of the 87C751 model, XON/XOFF flow control is implemented and therefore no errors occur during printing.

12. <u>Recommendations</u>

The 8031 solution is a very elegant solution, since the board fits neatly into the back of the Minitel terminal. It is also more cost effective than the 87C751 model for small quantities.

The 87C751 model however has the feature of a menudriven configuration routine. It is also guaranteed to not run errors during repetitive printing. If large quantities are to be manufactured, mask programming can be used and in this case the cheaper 83751 can be used.

It is therefore recommended that the 8031 model be used if at all possible, but it should be kept in mind that the 87C751 model becomes feasible in a production environment.

13. Bibliography.

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