THE DEVELOPMENT OF A 100 KHZ SWITCHED-MODE POWER SUPPLY

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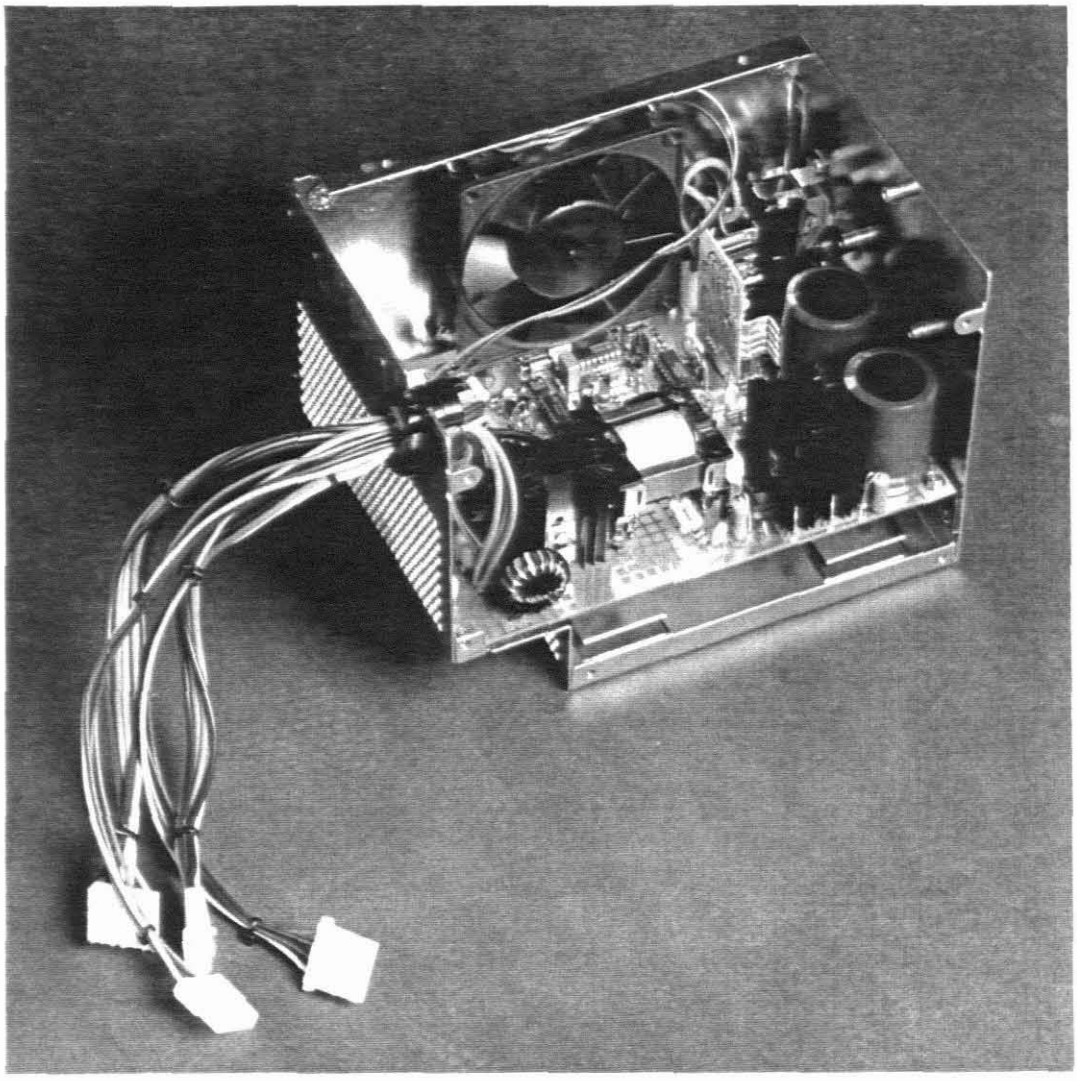

The complete 210 watt 100 kHz direct-off-line switched-mode power supply.

DECLARATION

I declare that the contents of this thesis represents my own work and that the opinions expressed are my own. It has not been submitted before any examination at this or any other institute.

Date : 27:11:91.

A.M. Gärtner

ABSTRACT

At the time of the design the maximum allowable operating frequency for an output power of between 200 and 250 watts was 100 kHz. Although a 600 kHz operating frequency could have been achieved, it would only be at a very low output power level.

To maximise the current components available, a 210 watt 100 kHz direct-off-line switched-mode power supply was developed. The design presented can be used to power any compatible IBM XT/AT personal computer.

The prototype was tested. An overall efficiency of 61% was achieved. The final prototype required 1 521 cm^3 and weighed approximately 980 g, representing a power to volume ratio of 0.14 W/cm^3 (2.26 $W/inch^3$).

Detailed procedures are also presented to help with the design and selection of the reactive components.

Special design features include the half-bridge push-pull topology, MOSFETS as power switches, digital current limiting, primary power limiting, multiple outputs and fault counting to name but a few.

SAMEVATTING

Ten tye van die ontwerp was die maksimum toelaatbare werkfrekwensie vir 'n kraglewering van tussen 200 en 250 watt 100 kHz. Alhoewel 'n werkfrekwensie van 600 kHz moontlik was, sou dit net geld vir baie lae kraglewerings.

Om huidige komponente dus maksimaal te benut, is 'n 210 watt 100 kHz skakelkragbron ontwikkel. Die gegewe ontwerp kan ook gebruik word om enige bestaanbare IBM XT/AT persoonlike rekenaar aan te dryf.

Die prototipe is ook getoets. 'n Algehele doeltreffendheid van 61% is behaal. Die finale prototipe beslaan 1 521 cm^3 en weeg om en by 980 g, wat 'n kraglewering tot volume verhouding van 0.14 W/cm^3 (2.26 $W/duim^3$) beteken.

Gedetailleerde prosedures is ook bepaal om te help met die ontwerp en seleksie van die reaktiewe komponente.

Spesiale kenmerke sluit die volgende in, die halfbrug-trek-stoot-topologie, MOSFETS as kragskakelaars, digitale beheer van die stroom, beheer van primêre kraglewering, verskeie uitsette en fouttelling om maar net 'n paar te noem.

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I would also like to thank the many suppliers who were involved, especially for their patience and help in supplying the necessary samples and technical information. To name a few: Spectratech (Joe Sanzul), Electrocomp (Tobie Steenkamp) and Microsource. Thanks to Bennie for taking time off to take the photographs presented in this thesis. Many thanks to all the other persons not mentioned above who were either directly or indirectly involved with the project and their view points.

Finally I would like to thank my family for their support and encouragement throughout the project.

Andy Michael Gärtner

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SYMBOLS

a	attenuation factor or correction factor	--
A_c	minimum core cross-sectional area	cm^2
A_e	effective core cross-sectional area	cm^2
A_L	inductance factor	nH
A_p	area product	cm^4
A_t	surface area	cm^2
A_v	gain	dB
A_w	wire area	cm^2
$A_{w(B)}$	bare wire area	cm^2
B	flux density	T
ΔB	maximum flux density swing (-B to +B)	T
b	breadth of strip	mm
B_{ac}	alternating current flux density	T
B_{CF}	maximum winding breadth of coil former	mm
B_m	operating flux density	T
B_{max}	maximum flux density	T
B_{sat}	saturation flux density	T
b_w	actual winding breadth of coil former	mm
C	capacitance	F
C_e	effective capacitance	F
C_j	junction capacitance	F
C_o	output capacitance	F
d	diameter (power transformer)	cm
d	wire diameter including isolation (pulse transformer)	cm

d_c	wire diameter, copper only (power transformer)	mm
dI/dt	rate of change of current with respect to time	A/s
dt	charging interval	s
dV_c	charging voltage	V
d_w	wire diameter, including insulation (power transformer)	mm
E	energy handling capability	Ws
f	frequency	Hz
F_R	the effective ac resistance of the wire to its DC resistance	--
f_s	switching frequency or operating frequency	Hz
f_{xo}	zero cross-over frequency	Hz
G_m	gain margin	dB
H	magnetizing force	Oe
H	height of winding (portion)	mm
h	height of strip or wire	mm
H_{CF}	maximum winding height of coil former	mm
H_p	height of primary winding portion	mm
H_s	height of secondary winding portion	mm
$H_{s(n)}$	height of secondary winding portion (n)	mm
I_B	transistor base current	A
I_{Bmax}	maximum transistor base current	A
I_{Bmin}	minimum transistor base current	A
I_C	transistor collector current	A
I_{Cmax}	maximum transistor collector current	A
I_{c-}	allowable capacitor rms ripple current	A

I_{Crms}	alternating current loading of capacitor	A
I_D	drain current	A
I_{DAV}	mean drain current	A
I_{Dmax}	maximum drain current	A
$\acute{I}_{Dmax}$	maximum drain current, adjusted	A
I_{FAV}	diode average forward current	A
I_{FDM}	diode flywheel current	A
I_{FM}	diode peak forward current	A
$I_{FM(ave)}$	diode average forward current	A
$I_{FM(rep)}$	maximum permissible repetitive current	A
$I_{FM(tot)}$	total average forward current	A
I_{iAV}	mean converter input current	A
$I_{iAV(110)}$	mean converter input current with line 110 V	A
$I_{iAV(220)}$	mean converter input current with line 220 V	A
I_{irms}	input rms current	A
ΔI_L	choke ripple current or ripple current	A
I_{Lmax}	maximum choke current	A
I_M	magnetising current	A
I_{mag}	magnetising current (current transformer)	A
I_o	output current	A
I_{omax}	maximum allowable output current	A
ΔI_{omax}	maximum step change in load current	A
$I_{o(n)}$	output current for (n) winding (power transformer)	A
$I_{o(nmax)}$	maximum output current for (n) winding	A
$I_{o(step)}$	maximum possible step change in load current	A

I_p	primary current	A
$I_{p(max)}$	maximum primary current	A
$I_{p(rms)}$	primary rms current	A
I_{RM}	maximum diode reverse current	A
I_{Rmax}	maximum capacitor residual current	mA
I_s	secondary current	A
I_{sn}	secondary current in winding (n) (power transformer)	A
$I_{sn(max)}$	maximum current in secondary winding (n) (power transformer)	A
$I_{sn(rms)}$	rms current in secondary winding (n) (power transformer)	A
I_z	zener diode current	A
I_{Zmax}	maximum zener diode current	A
I_{Zmin}	minimum zener diode current	A
J	current density	A/cm^2
K_f	waveform coefficient	--
k_{fD}	diode current form factor	--
k_{fi}	converter input current form factor	--
K_j	current density coefficient	--
K_s	surface area coefficient	--
K_u	window utilisation factor	--
K_v	volume coefficient	--
K_w	weight coefficient	--
l_e	effective magnetic path length	mm
l_g	length of the air gap	mm
L_i	RFI/EMI filter inductance	H
L_o	output choke inductance	H

L_p	primary inductance	H
L_s	secondary inductance or leakage inductance	H
MLT	mean length turn	cm
M_{lt}	actual turn length	cm
MPL	magnetic path length	cm
N	number of turns	--
n	primary-to-secondary turns ratio	--
N_p	number of primary turns	--
N_s	number of secondary turns	--
N_{sec}	number of secondary turns (pulse transformer)	--
$N_{s(n)}$	number of secondary turns for output winding (n) (power transformer)	--
P	power	W
P_{ave}	average power dissipation	W
P_c	core losses	W
P_{cu}	copper losses	W
$P_{cu(p)}$	primary copper losses	W
$P_{cu(sn)}$	copper losses in secondary winding (n) (power transformer)	W
$P_{cu(tot)}$	total copper losses	W
P_D	peak power dissipated in diode	W
$P_{D(tot)}$	total loss in diode	W
P_{DC}	diode conduction loss or forward loss	W
P_{DR}	diode reverse loss	W
P_i	input power	W
P_o	output power	W
$P_{o(max)}$	maximum output power	W

$P_{o(n)}$	output power for (n) winding (power transformer)	W
P_t	apparent power	W
P_{Tr}	power dissipated in transistor or MOSFET	W
P_{Trc}	conduction loss, transistor or MOSFET	W
$P_{Tr(tot)}$	total transistor or MOSFET losses	W
$P_{Trs(off)}$	transistor or MOSFET, turn-off losses	W
$P_{Trs(on)}$	transistor or MOSFET, turn-on losses	W
P_{Σ}	total loss	W
Q_{rr}	reverse recovery charge	As
R	resistance	Ω
R_{ac}	wire working or ac resistance	Ω
$R_{ac(p)}$	ac resistance of primary winding (power transformer)	Ω
$R_{ac(sn)}$	ac resistance of secondary winding (n) (power transformer)	Ω
R_{DC}	wire DC resistance	Ω
$R_{DC(tot)}$	total DC resistance	Ω
$R_{DS(on)}$	on resistance, drain to source	Ω
$R_{DS(on)max}$	maximum on resistance, drain to source	Ω
R_{ESR}	equivalent series resistor	Ω
R_i	mains impedance	mΩ
R_L	load resistor	Ω
R_{RL}	relay coil resistance	Ω
R_{th}	thermal resistance	°C/W
R_{thca}	thermal resistance, case to ambient	°C/W
R_{thjc}	thermal resistance, junction to case	°C/W
S_3	ratio of usable window area to window area	--

T	period ($T = 1/f$)	s
T	temperature	°C
ΔT	rise in temperature	°C
ΔT_j	rise in junction temperature	°C
$\tan\delta$	dissipation factor	--
t_d	required time delay period (saturable reactor)	s
t_d	discharge time, capacitor	ms
t_f	fall time	ns
T_j	junction temperature	°C
T_{jmax}	maximum allowable junction temperature	°C
t_{on}	conducting "on" time period	s
t_r	rise time	ns
t_{tr}	transient recovery time	s
ΔV	permissible overvoltage or overshoot allowed	V
ΔV_o	maximum permissible output ripple voltage	V
V_{CE}	voltage, collector to emitter	V
V_{DS}	voltage, drain to source	V
$V_{DS(on)}$	"on" time period voltage, drain to source	V
V_F	forward voltage drop	V
V_i	direct input voltage	V
$V_{i(110)}$	110 V line input	V_{rms}
$V_{i(220)}$	220 V line input	V_{rms}
V^*_{imax}	effective maximum input voltage	V
V_{imax}	maximum possible direct input voltage	V
$V_{imax(110)}$	maximum possible direct input voltage with 110 V line	V

$V_{imax(220)}$	maximum possible direct input voltage with 220 V line	V
V_{imin}	minimum possible direct input voltage	V
V'_{imin}	minimum voltage across input capacitor	V
$V_{imin(110)}$	minimum possible direct input voltage with 110 V line	V
$V_{imin(220)}$	minimum possible direct input voltage with 220 V line	V
V_{in}	input voltage (feedback)	V_{rms}
V_{inom}	nominal direct input voltage	V
$V_{inom(220)}$	nominal direct input voltage with 220 V line	V
V_L	voltage drop across choke	V
V_{Lp}	voltage drop, primary winding	V
V_{Ls}	voltage drop, secondary winding and choke	V
V_m	mean secondary voltage (current transformer)	V
V_o	output voltage	V
ΔV_o	change in output voltage	V
ΔV_o	maximum permissible output ripple voltage	V
$V_{o(actual)}$	actual output voltage	V
V_{omax}	maximum output voltage allowed	V
ΔV_{omax}	maximum permissible deviation in output voltage during step change in load	V
$V_{o(n)}$	output voltage for (n) winding	V
$V_{o(nmin)}$	minimum output voltage for (n) winding	V
$V_{o(req)}$	required output voltage	V
V_p	peak voltage or primary voltage	V
V_{p-p}	ripple voltage, peak-to-peak value	V

$V_{p(max)}$	maximum primary voltage (power transformer)	V
$V_{p(min)}$	minimum primary voltage (power transformer)	V
$V_{p(nom)}$	nominal primary voltage (power transformer)	V
V_R	diode reverse voltage	V
V_{ramp}	PWM sawtooth ramp voltage	V
V_{ref}	reference voltage	V
$V_{RL(max)}$	maximum relay operating voltage	V
$V_{RL(min)}$	minimum relay operating voltage	V
V_{rm}	peak repetitive reverse voltage	V
V_{Rmax}	maximum diode reverse voltage	V
V_{rms}	root mean square voltage	V_{rms}
V_s	secondary voltage	V
$V_{s(n)}$	secondary voltage for (n) output winding (power transformer)	V
V_Z	zener diode voltage	V
V_{Zmax}	maximum zener diode voltage	V
V_{Zmin}	minimum zener diode voltage	V
W_a	window area	cm^2
W_{ae}	effective window area	cm^2
W_{tfe}	core piece weight	g
X	ratio (V_{p-p} versus $V_{imin(220)}$)	--
x	exponential exponent (power transformer)	--
y	exponential exponent (power transformer)	--
α	transient factor	--
Δ	a small increment	--
δ_T	duty cycle	--

δ_{T1}	duty cycle where possible step in load current could occur	--
δ_{Tmin}	minimum duty cycle	--
δ_{Tmax}	maximum duty cycle	--
ϵ	unbalance factor	--
ζ	resistance correction factor	--
η	efficiency	%
η^*	efficiency (power transformer)	%
θ_a	ambient temperature	°C
θ_{amax}	maximum ambient temperature	°C
θ_{jmax}	maximum junction temperature	°C
θ_{on}	conduction interval	°
θ_s	phase angle where diode conduction starts	°
μ	permeability	--
μ_e	effective permeability	--
μ_i	initial permeability	--
μ_r	required core permeability	--
τ	time constant	s
ϕ_m	phase margin	°
ψ	heat flux density	W/cm^2
$'$	a new or practical adjusted value	--

ABBREVIATIONS

ac	alternating current
AWG	American wire gauge
B/H	hysteresis loop of magnetic material
CT	current transformer
dB	decibels
DC	direct current or voltage
EMI	electromagnetic interference
ESL	effective series inductance
ESR	effective series resistance
ETD	economic transformer design
FCC	Federal Communications Commission
IC	integrated circuit
IR	International Rectifier
LC	a low pass filter consisting of a series inductor and shunt capacitor
MLT	mean length per turn
MOSFET	metal-oxide semiconductor field-effect transistor
"on"	conducting state of a device
"off"	nonconducting state of a device
OVP	overvoltage protection
pcb	printed circuit board
p-p	peak-to-peak value
PTC	positive temperature coefficient
P.U.	polyurethane
PWM	pulse-width modulation
RFI	radio-frequency interference

rms	root mean square
SMPS	switched-mode power supply
SR	saturable reactor
TTL	transistor-transistor logic
UL	Underwriter's Laboratories
UVP	undervoltage protection
Vcc	supply voltage
VDE	Verband Deutscher Elektrotechniker

GENERAL CONVERSION FACTORS

TO CONVERT	MULTIPLY BY
Centimeter^4 to inches^4	2.4×10^{-2}
Inches to centimeters	2.54
Mils to inches	1×10^{-3}
Oersted to amp-turns per centimeter	0.796

CONSTANTS

μ_o - magnetic field constant	$4\pi \times 10^{-7}$ H/m
π - physical constant	3.1416

1. INTRODUCTION

Today the switching regulator or switched-mode power supply (SMPS) with its high efficiency (70 - 80%), small size and light weight is a proven design concept, already replacing the linear regulator in many applications where high efficiency and small size are of importance.

The development of the switching regulator was not always easy, especially in the early days when the control circuitry was made up of discrete transistor stages, controlling the duty cycle of the switching transistors. The physical layout of the control circuitry formed the inevitable weak link causing instability and noise, which made the switching regulator unreliable, difficult to design and a second choice to the linear regulator.

With the demands of the space programme in the 1960's came the development of more highly reliable, efficient and light weight switching regulators.

Until now only low voltage secondary switchers were employed. Then in the late 1960's with the commercial availability of high voltage and fast switching transistors the era of the direct-off-line switching regulator began.

For some years now the basic building blocks for the control circuitry have been available in integrated circuit (IC)

form, which has resulted in the design of more reliable switching regulators with reduced size and increased performance.

For further reduction in size and increased performance the basic elements of the control circuitry were included into one package, which led to the development of the first practical switching regulator control IC, the SG1524 by Silicon General in 1976. Besides the normal functions it also included some protective functions (analog current limiting and digital shutdown). Since its introduction many others followed e.g. the ZN1066, the TL494A and the MC3420, of which the TL494 is still used today in the majority of switched-mode power supplies for personal computers.

As the popularity of the switched-mode power supply grew, more and more demands were made for a better integrated control circuit, resulting in the development of a second (SG1525A) and third (SG1526) generation of pulse width modulator control circuits.

With the ever-increasing use of the personal computer the Cape Technikon saw the need to develop a SMPS locally. With the current SMPS's for personal computers running at 20 - 50 kHz it was decided to develop a high frequency (100 kHz) SMPS to power any IBM compatible XT/AT personal computer, thus keeping in step with the ever increasing switching speeds of power supply manufacturers.

The objective will therefore be to develop a 210 watt 100 kHz half-bridge push-pull converter with the following as primary features:

1) Dual line operation
2) Minimum efficiency 70%
3) Multiple outputs (±5 V and ±12 V)
4) MOSFETS as switching devices
5) Third generation SMPS control circuit (SG3526N)
6) Power limiting and
7) Fault counting.

1.1. DEVELOPMENT

This chapter concludes with a brief description of the half-bridge push-pull converter topology, followed by the complete circuit diagram for the SMPS. To obtain an overall view of the SMPS a simplified block diagram is provided in Chapter 2 in which the functions of the non-critical components are discussed. The more critical components in the design are dealt with in detail in the relevant chapters.

The preliminary design specifications are laid down in Chapter 3 while Chapter 4 deals with the detailed development of the complete input stage for the SMPS.

The power stage is dealt with in Chapter 5. This includes the design of the driver stage, overcurrent transformer and the development of a detailed design procedure for the power

transformer.

The output stage, which includes the design and selection of the output rectifiers, chokes and filter capacitors, is dealt with in Chapter 6. The feedback loop is closed in Chapter 7, followed by the results and conclusion in Chapter 8.

1.2. THE HALF-BRIDGE PUSH-PULL CONVERTER

1.2.1. TOPOLOGY SELECTION

The half-bridge push-pull topology shown in Figure 1.1 was used in the 210 watt switched-mode power supply for the following reasons:

1) Dual line operation (220 or 110 volts) can be easily implemented for domestic or foreign operation.
2) The voltage stress imposed on the primary switching devices does not exceed V_{in}.
3) Flux symmetry problems can be corrected by simple means, in this case by the addition of a single capacitor C_x as illustrated in Figure 1.1.
4) Better transformer utilisation when compared to the conventional push-pull topology where only one half of the winding is used during each half cycle.

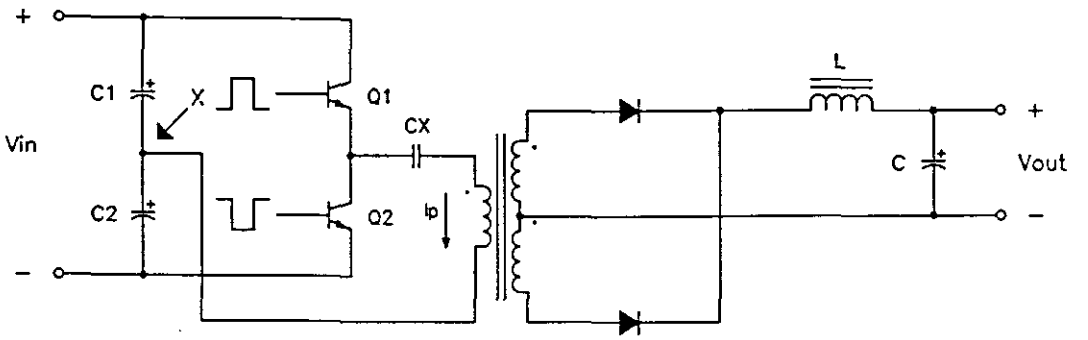

Figure 1.1 The half-bridge push-pull converter topology (bipolar transistors are used for the sake of simplicity).

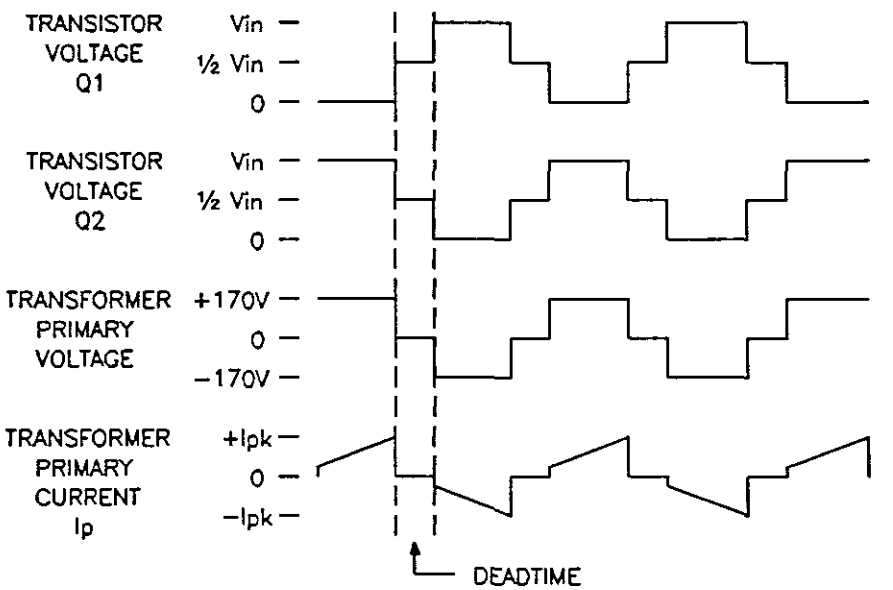

Figure 1.2 Half-bridge push-pull converter waveforms.

1.2.2. OPERATING PRINCIPLE

To simplify the discussion, a transistor duty cycle of 45% is assumed and all waveforms are idealized. The switching sequence for the half-bridge push-pull converter is shown in

Figure 1.2.

A steady-state condition is assumed, with capacitors C_1 and C_2 fully charged. The node marked X in Figure 1.1 will therefore float at one half of V_{in} or 170 volts DC at nominal input voltage.

When transistor Q_1 turns on the junction of the Q_1 emitter and Q_2 collector is pulled towards $+V_{in}$ and a positive pulse of +170 volts is generated across the primary winding. The "on" time for Q_1 is determined by the control circuit after which Q_1 is turned off. A mandatory "deadtime" (see Figure 1.2) is then followed set by the control circuit. During this period both transistors are turned off, which prevents cross conduction from occurring and the possible destruction of the switching devices.

When transistor Q_2 turns on, the junction of the Q_1 emitter and Q_2 collector is pulled towards $-V_{in}$ and a negative pulse of -170 volts is generated across the primary winding. After a certain "on" time has elapsed, transistor Q_2 turns off and the cycle is completed.

An alternating voltage of 340 volts peak-to-peak (due to the turn-on-turn-off action of Q_1 and Q_2) will therefore appear across the primary winding, which is then stepped down, rectified and filtered to produce the required output DC voltage. By varying the "on" time or duty cycle, the output

can be compensated for any variations in line or load.

1.3. THE COMPLETE CIRCUIT DIAGRAM

The complete 210 watt 100 kHz switched-mode power supply is given schematically in Appendix A.

2. THE BLOCK DIAGRAM

The block diagram of the 210 watt 100 kHz SMPS is shown in Figure 2.1. A brief discussion of the individual components is presented elaborating on the non-critical components (e.g. the control circuit, the fault counting circuit etc.). The more critical components (e.g. the input rectifier and filter circuit, the power transformer etc.) are left to be discussed in detail in the relevant chapters (Chapters 4 to 7).

2.1. EMI FILTER

The electromagnetic interference (EMI) filter is a low-pass filter, which reduces the conducted switching noise back into the ac line to an acceptable level.

2.2. INPUT RECTIFIER AND FILTER

The input rectifier and filter section converts the ac line voltage into an unregulated DC voltage V_i. Dual input voltage operation (220/110 volt) is provided by a link option. For 220 volt line operation the input section is configured as a full-wave bridge, and for 110 volt line operation the input section is configured as a voltage doubler. Both configurations will provide a V_i range of 260 - 340 volts to the converter.

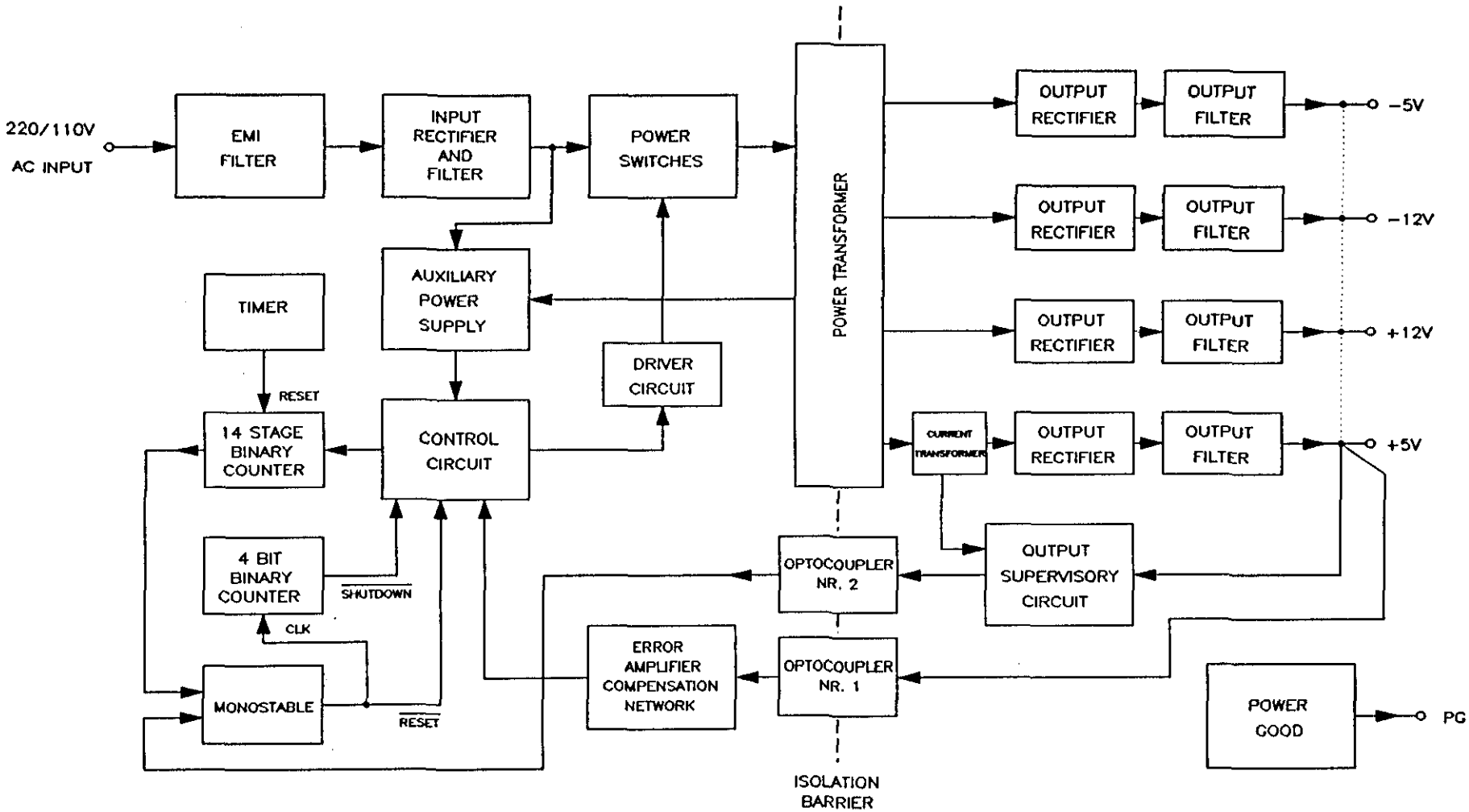

Figure 2.1 The block diagram of the 210 watt 100 kHz multiple output SMPS.

The input filter capacitors also supply the required high-and low-frequency energy to the converter.

2.3. THE POWER SWITCHES

The power switches or MOSFETS as used in the design, switch very fast between saturation and cut-off. The MOSFETS act as "gates", which control the amount of energy to be transferred from the input to the load.

The amount of energy to be transferred is determined by the control circuit, which determines the "on" time for the MOSFETS, depending on the demand of the load.

2.4. POWER TRANSFORMER

The power transformer provides the required DC isolation between the input line and the output. In this configuration the transformer stores no energy, but is simply used to step down the input voltage and generate the multiple output voltages as required for this design.

2.5. OUTPUT RECTIFIERS

The output rectifier diodes for this converter configuration conduct at the same time as the power switches. The bipolar square waves at the secondary side of the power transformer are converted to unipolar square waves at twice the operating

frequency.

2.6. OUTPUT FILTERS

The output filters are made up of a single stage second order (LC) filter, the function of which is twofold, viz. (1) to store energy for the load during the "off" time or non-conducting state of the power switches and (2) to reduce the high-frequency conducted series and common-mode output noise to an acceptable level.

2.7. AUXILIARY POWER SUPPLY

The auxiliary power supply provides power to the control and drive circuits of the converter from the initial start-up stage to the continuous operating mode of the converter.

2.8. THE CONTROL CIRCUIT

Figure 2.2 shows the control circuit as it is configured for this design. The integrated circuit used is the SG3526N, which is a pulse width modulated (PWM) control circuit.

The double totem-pole output drive circuit of the SG3526N can sink and source up to 200 mA. A drive circuit can therefore be implemented, using a minimum of additional external components, which makes the SG3526N an ideal choice for driving the power MOSFETS (see also Chapter 5).

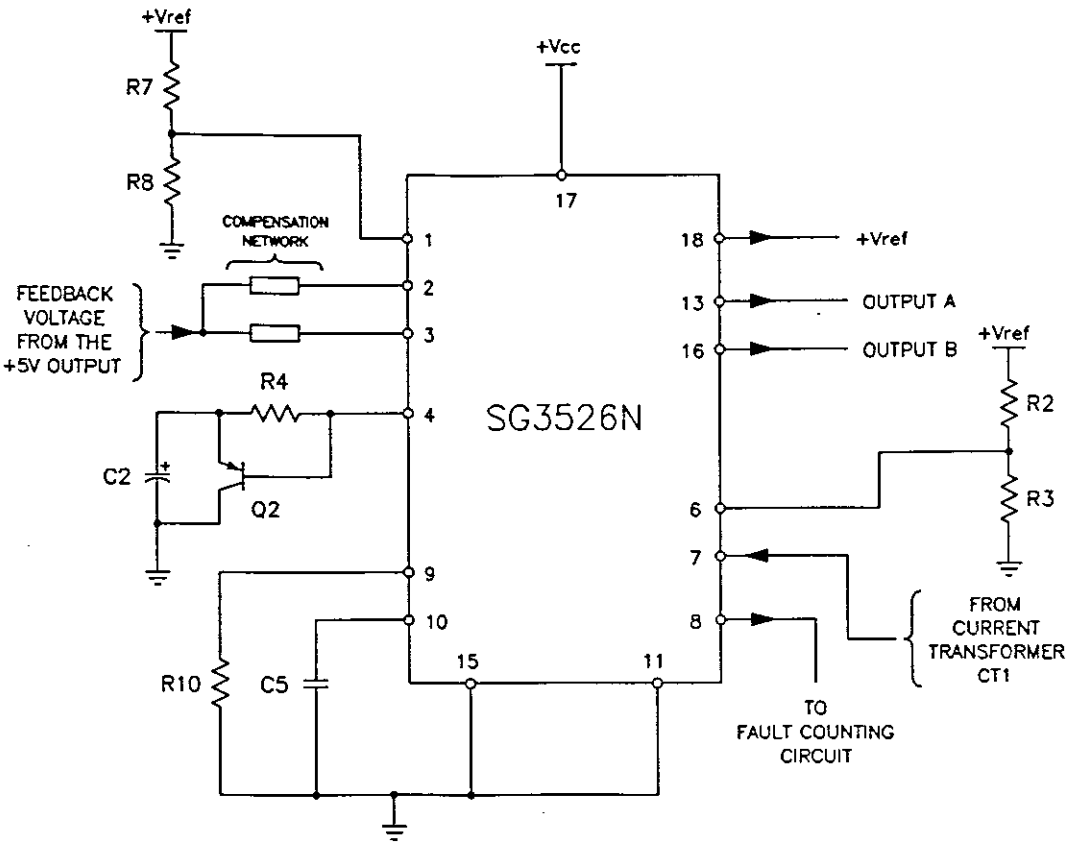

Figure 2.2 The SG3526N pulse width modulated control circuit.

The output A and B (pin 13 and 16) provides an out-of-phase square wave at one half the oscillator frequency, which is determined by two external components R_{10} and C_5. In this application the oscillator frequency is set to 200 kHz, providing a 100 kHz switching frequency.

The error amplifier (pin 1, 2 and 3) including the external compensation network forms the "error amplifier and compensation network" (see Chapter 7 for design detail). This generates an error voltage, which in turn determines the pulse width or "on" time of the switching devices.

The deadtime control circuit of the SG3526N provides a deadtime of 1.5 μs (pin 11 grounded). This prevents cross-conduction and the possible destruction of the power switching devices.

The soft-start circuit of the SG3526N (pin 4) provides a low-stress start-up action. The converter start-up is first delayed for several line cycles, allowing the input filter capacitors to fully charge, after which the pulse width is progressively increased until the output is established. This protects the power switching devices and the input rectifier diodes from large surge currents during power supply turn-on.

A turn-on delay time of 280 ms is selected, providing sufficient time for the input filter capacitors to charge. To accommodate the larger delay capacitor C_2 selected, a surge limiting circuit is included (see Figure 2.2, pin 4).

A voltage equivalent of the current flowing through the current transformer CT1 is applied to the inverting input (pin 7) of the current sense comparator, which is compared to a reference voltage of 2.5 volt.

With the current transformer CT1 placed in series with the primary winding of the power transformer T2, the current through the power switching devices and the primary winding will therefore be monitored on a pulse-by-pulse basis.

If an overcurrent situation should arise, the output of the current sense comparator will immediately terminate the drive pulse to the relevant power switching device. The maximum throughput power of the converter will therefore be limited (power limiting), contributing to a more reliable power supply.

The terminating pulses which are available at pin 8 ($\overline{SHUTDOWN}$) are also monitored by a fault counting circuit, providing further power supply protection.

The control circuit also provides a stable reference voltage of +5 volt, which is used in many places throughout the design as a reference.

2.9. THE FAULT COUNTING TECHNIQUE

The basic schematic diagram for illustrating the fault counting technique is shown in Figure 2.3.

The technique is used to reduce the power dissipation in the switching devices during sustained current limiting conditions as would occur if an output is being short-circuited or overloaded.

A 14 stage binary counter is used to accumulate pulse terminating commands from the SG3526N (pin 8). Once 2^{13} or 8 192 counts have been accumulated, the output of the 14th

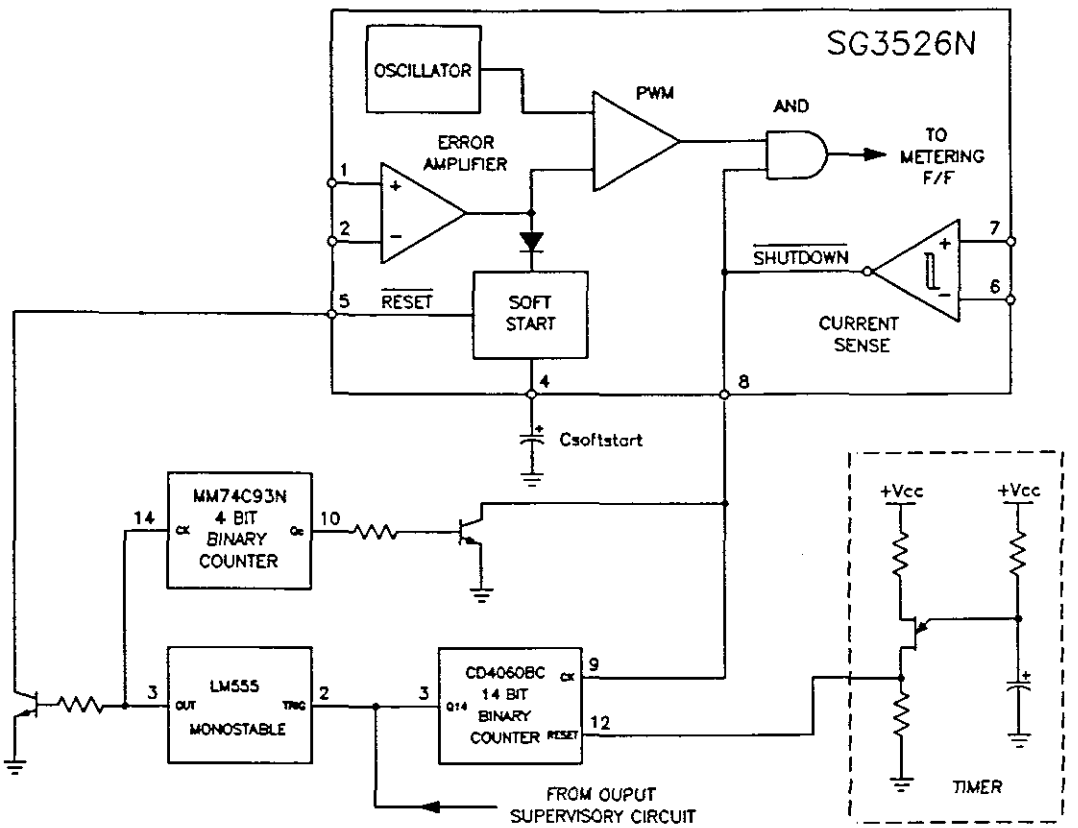

Figure 2.3 The simplified schematic diagram, illustrating the fault counting technique.

stage of the CD4060BC goes high. At 200 kHz this represents a delay of 41 ms. The relaxation oscillator is used to periodically reset the accumulated count in the CD4060BC, which is done every 50 ms.

With the 14th stage of the CD4060BC high, the monostable is triggered, keeping the reset (pin 5) of the SG3526N low for 200 ms. This allows the soft-start timing capacitor C_2 to fully discharge after which a soft-start cycle begins.

At the same time a second counter is advanced by one count.

The MM74C93N is a 4-bit binary counter and accumulates the "hiccup" cycles. The counter will be referred to as the "hiccup" counter.

A total of four "hiccup" cycles are allowed after which the supply will be shut off. To restore normal operation of the power supply the user must switch the main power switch (SW1) off and back on again.

The implementation of the fault counting technique is only possible due to the fact that the $\overline{SHUTDOWN}$ and $\overline{RESET}$ terminals of the SG3526N are compatible with both TTL and CMOS logic.

2.10. THE OUTPUT SUPERVISORY CIRCUIT

A simplified schematic diagram of the output supervisory circuit is shown in Figure 2.4.

The SG3543 forms the basis for the output supervisory circuit. It provides both over- and under-voltage protection for the main output (20 A, 5 V).

The threshold for both the over- and under-voltage is set by the addition of a single resistor divider string R_{49}, R_{50} and R_{53} at pins 6 and 7 of the SG3543. A tolerance of ±10% (4.5 V to 5.5 V) of the output voltage V_o is allowed.

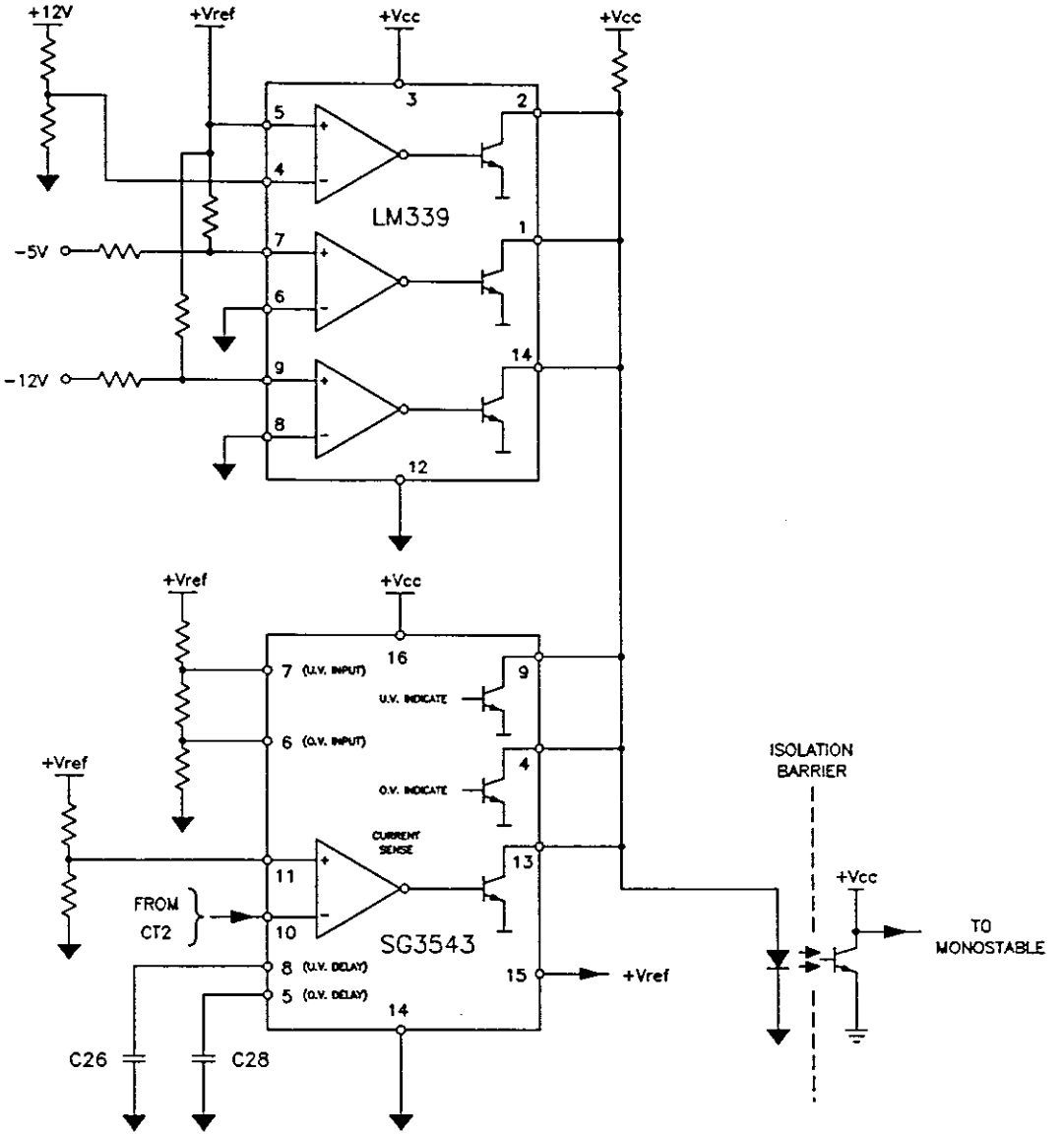

Figure 2.4. The simplified schematic diagram for the output supervisory control circuit.

The externally connected capacitors C_{28} (pin 5) and C_{26} (pin 8) provide a delay before activating the output circuitry. The over- and under-voltage delay times are set to 1.5 ms and 10 ms respectively. This provides sufficient time for the output voltages to settle down.

To protect the main output against excessive overload conditions a second current transformer CT2 is placed in the output winding. A voltage equivalent of the current through the current transformer CT2 is compared to a preset reference voltage (pin 11). The current amplifier in the SG3543 is configured as a comparator. The comparator is only activated when the output current exceeds 22 amps or 20% above I_o.

The addition of the LM339 quad comparator facilitates the over-voltage monitoring of the -5 V, -12 V and +12 V auxiliary outputs. Again a tolerance of +10% is allowed for each individual output.

The comparators used in the SG3543 and LM339 all have open collector outputs, which are all tied together so that the operation of any single comparator will transfer a "hiccup" cycle via the optocoupler OK2 to the monostable, which in turn will initiate a soft-start cycle. At the same time the "hiccup" counter is advanced by one count.

2.11. POWER GOOD

A power good signal is a requirement for all IBM compatible XT/AT personal computers. The circuit commonly used is shown in Figure 2.5 and provides a high state signal or "1" after a delay of 100 ms.

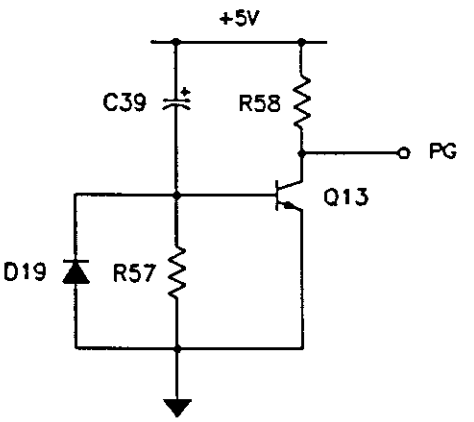

Figure 2.5 The power good circuit.

3. DESIGN SPECIFICATIONS

TOPOLOGY :

Half-bridge push-pull converter

LINE INPUT :

220 volts -15%, +10% (187 - 242 volts), 50 Hz

110 volts -15%, +10% (93 - 121 volts), 60 Hz

MAIN OUTPUT :

Voltage	:	+5 volts
Current	:	2 to 20 amperes
Current limit	:	22 amperes
Over-voltage limit	:	+10% of output voltage
Under-voltage limit	:	-10% of output voltage
Ripple voltage	:	less than 50 mV_{p-p} maximum
Line regulation	:	± 1%
Load regulation	:	± 1%

AUXILIARY (SEMIREGULATED) OUTPUTS :

Voltage	:	-5 volts
Current	:	0.1 to 1 ampere
Over-voltage limit	:	+10% of output voltage
Ripple voltage	:	less than 50 mV_{p-p} maximum

Voltage	:	-12 volts
Current	:	0.1 to 1 ampere
Over-voltage limit	:	+10% of output voltage
Ripple voltage	:	less than 100 mV_{p-p} maximum
Voltage	:	+12 volts
Current	:	0.8 to 8 amperes
Over-voltage limit	:	+10% of output voltage
Ripple voltage	:	less than 100 mV_{p-p} maximum
Cross regulation	:	±5% for auxiliary outputs

OTHER FEATURES :

Efficiency	:	75%
Switching frequency	:	100 kHz
Primary power limiting	:	210 watt maximum
Fault counting		

4. THE INPUT STAGE FOR THE HALF-BRIDGE PUSH-PULL CONVERTER

The schematic diagram for the complete input stage is shown in Figure 4.1. This chapter presents the design and selection of the components for the input stage, starting with the selection of the input filter capacitors.

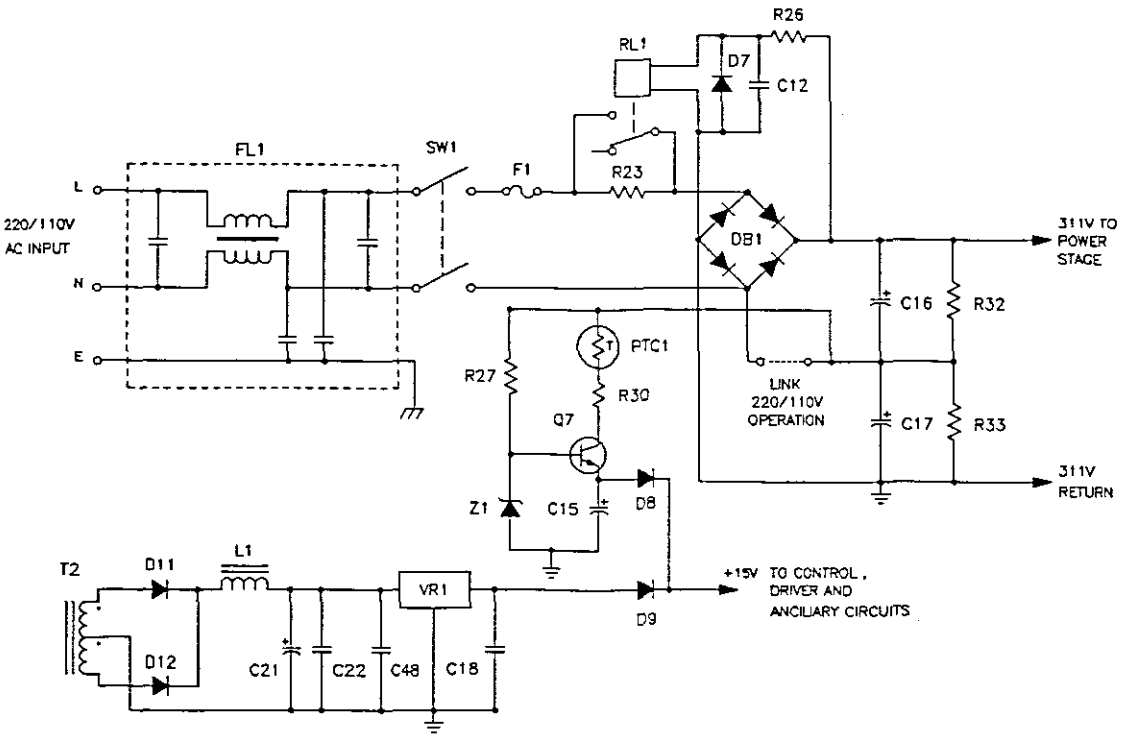

Figure 4.1 The complete schematic diagram of the input stage for the half-bridge push-pull converter.

4.1. INPUT FILTER CAPACITORS

To simplify the design procedure use is made of Figure 4.2, which represents a simplified version of the input stage showing only the relevant components.

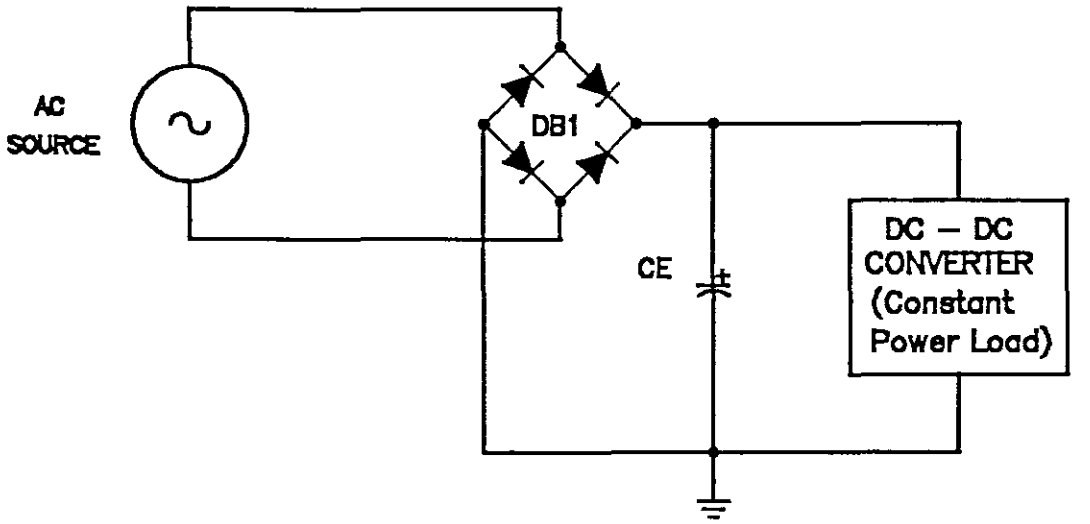

Figure 4.2 The simplified version of the input stage showing the ac source, bridge rectifier and DC-DC converter.

To start of with, the input filter capacitors C_{16} and C_{17} are replaced by their equivalent capacitance C_e. The selection of C_e is controlled by several practical factors (e.g. rms ripple current rating, ripple voltage, voltage rating etc.). In this application the selection of C_e is based on the following three factors:

1) Ripple voltage
2) RMS ripple current rating and
3) Size and cost

The value for C_e is calculated as follows: The DC-DC converter worst case DC output power is 291 W. Assuming an initial efficiency of 75%, the input power is given by

$$P_i = \frac{P_o}{\eta} \quad (W) \tag{4-1}$$

$$P_i = 388\ W$$

The maximum mean converter input current I_{iAV} is obtained at low line. Therefore

$$V_{imin(220)} = (V_{i(220)} \times 0.85 \times \sqrt{2}) - 2V_F \quad (V) \tag{4-2}$$

$$V_{imin(220)} = 263\ V$$

where $V_F = 1$ V

$$I_{iAV(220)} = \frac{P_i}{V_{imin(220)}} \quad (A) \tag{4-3}$$

$$I_{iAV(220)} = 1.48\ A$$

According to [1] the peak-to-peak ripple voltage V_{p-p} is selected not larger than 10% of the nominal input voltage V_{inom} with

$$V_{inom(220)} = \sqrt{2} \times V_{i(220)} \quad (V) \tag{4-4}$$

$$V_{inom(220)} = 311\ V$$

Therefore

$$V_{p-p} = 0.1 \times V_{inom(220)} \quad (V) \tag{4-5}$$

$$V_{p-p} = 31\ V$$

To obtain a sufficient margin for capacitor tolerances and variation with temperature, it is assumed that the capacitor

C_e must carry current for the entire half cycle, i.e. 10 ms for 50 Hz.

With a peak-to-peak ripple voltage V_{p-p} of only 10% of $V_{inom(220)}$, a linear discharge period can be assumed, making it possible to apply the linear equation (4-6), which will provide an approximate value for C_e.

$$C_e = \frac{I_{iAV(220)}}{V_{p-p}} \times \frac{T}{2} \quad (F) \qquad (4\text{-}6)$$

$$C_e = 477\ \mu F$$

Since C_{16} and C_{17} are in series, each capacitor will have a value of

$$C_{16} = C_{17} = 954\ \mu F$$

A 680 μF/250 V capacitor is selected, although the capacitor value is smaller than calculated. Taking into consideration the conservative estimates made in equation (4-6) and a capacitor tolerance of ± 20%, the choice made is quite acceptable.

Using equation (4-6) the hold-up time at nominal input voltage and full load will be approximately 20 ms.

4.1.1. RMS RIPPLE CURRENT RATING

To prevent an excessive temperature rise in the input filter

capacitors and premature failure it is of great importance to ensure that the selected filter capacitor's allowable rms ripple current rating $I_{c\sim}$ is more than adequate. The method described in [2] is used. Being a theoretical based method the obtained result will only be an approximation, giving a value of 20 - 50% larger than would be obtained using a practical method.

Therefore the maximum alternating current I_{Crms} flowing in the capacitor C_e is given by

$$I_{Crms} = I_{iAV(220)} \sqrt{0.5k_{fD}^2 + k_{fi}^2 - 2} \quad (A) \tag{4-7}$$

This leaves two unknown variables:

k_{fD} - Diode current form factor and
k_{fi} - Converter input current form factor

With the help of Figure 4.3, adapted from [2] and equation (4-8), the diode form factor k_{fD} is determined.

$$X = \frac{V_{p-p}}{V_{imin(220)}} \tag{4-8}$$

With the ratio X calculated the diode current form factor k_{fD} is read off from Figure 4.3 on page 27.

From Figure 4.3, $k_{fD} = 4.1$

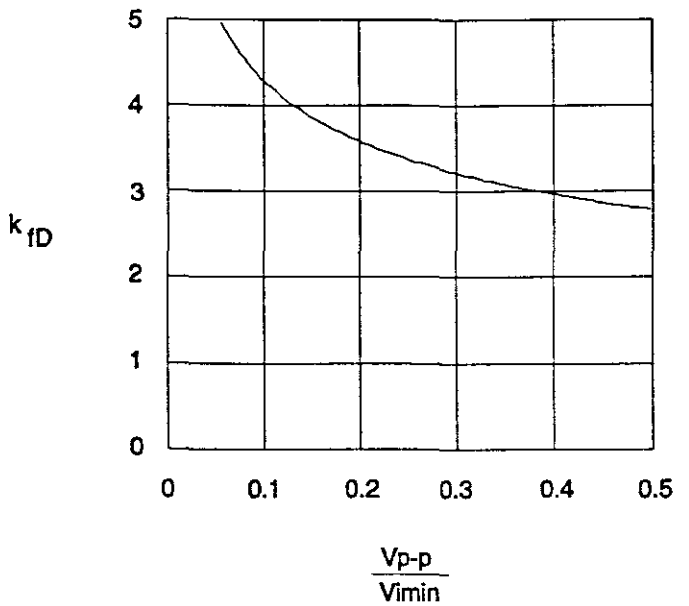

Figure 4.3 The diode current form factor k_{fD} versus the peak-to-peak ripple voltage V_{p-p}, relative to the minimum direct input voltage V_{imin}.

The converter input current form factor k_{fi} lies between the limits, from [2]

$$1.3 < k_{fi} > 1.7 \qquad (4\text{-}9)$$

A mean value of 1.5 for k_{fi} is selected. Substituting obtained variables in equation (4-7), results in an I_{Crms} of 4.35 A.

However, I_{Crms} (4.35 A) is larger than $I_{c\sim}$ (3.8 A). Taking into consideration size, cost and that I_{Crms} calculated is 20 - 50% larger than the practical value ($I_{Crms} \approx 3$ A), the choice of the input filter capacitors would therefore meet the alternating current loading requirement.

4.2. DIVIDER RESISTORS

Since the series connected capacitors are not capable of dividing the direct voltage equally, a method must be applied to force the voltage division. This is shown in Figure 4.4.

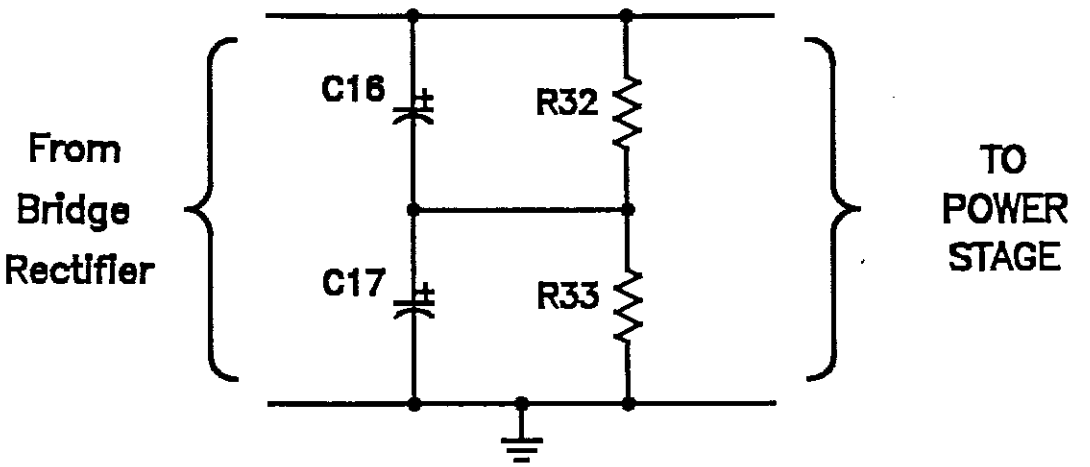

Figure 4.4 The input filter capacitors C_{16} and C_{17} with the voltage divider resistors R_{32} and R_{33}.

The method used to calculate R_{32} and R_{33} is adapted from [2]. The capacitor's maximum residual current I_{Rmax} at θ_a = 45 °C is given by

$$I_{Rmax} = (2.1 \times 10^{-3}) \times 3.5 \times 1 \quad (A) \qquad (4\text{-}10)$$

$$I_{Rmax} = 7.35 \quad mA$$

Taking into consideration such factors as resistor power rating and its capability to handle the maximum capacitor residual current I_{Rmax}, a compromise is therefore made by multiplying I_{Rmax} with a factor of 0.3.

The current through R_{32}/R_{33} will be 0.3 × 7.35 mA = 2.21 mA.

Therefore

$$R_{32} = R_{33} = \frac{0.5\ V_{imax(220)}}{I_{R32/33}} \quad (\Omega) \tag{4-11}$$

with

$$V_{imax(220)} = (V_{i(220)} \times 1.1 \times \sqrt{2}) - 2V_F \quad (V) \tag{4-12}$$

$$V_{imax(220)} = 340\ V$$

where V_F = 1 V.

Therefore

$$R_{32} = R_{33} = \frac{170\ V}{2.21 \times 10^{-3}\ A} \quad (\Omega) \tag{4-13}$$

$$R_{32} = R_{33} = 76.92\ k\Omega$$

selected, $R_{32} = R_{33}$ = 100 kΩ.

Loss in R_{32}/R_{33}:

$$P = \frac{(0.5\ V_{imax(220)})^2}{R_{32/33}} \quad (W) \tag{4-14}$$

$$P = 0.29\ W$$

selected, $R_{32} = R_{33}$ = 100 kΩ/1 W.

4.3. INPUT RECTIFIERS

The selection of the input rectifier diodes will be based on the following three factors:

1) Diode average forward current I_{FAV}
2) Peak repetitive reverse voltage V_{rm} and
3) Diode junction temperature T_j.

Maximum mean converter input current I_{iAV} will flow at a line voltage of 110 V_{rms}. With the line voltage halved I_{iAV} will be doubled, giving

$$I_{iAV(110)} = 2 \times I_{iAV(220)} \quad (A) \tag{4-15}$$

$$I_{iAV(110)} = 2.96\ A$$

Therefore the diode average forward current will be

$$I_{FAV} = \frac{I_{iAV(110)}}{2} \quad (A) \tag{4-16}$$

$$I_{FAV} = 1.48\ A$$

The peak repetitive reverse voltage V_{rm} is selected such that

$$V_{rm} \geq 2.83\ V_{i(220)} \quad (V) \tag{4-17}$$

$$V_{rm} \geq 623\ V$$

Taking obtained I_{FAV} and V_{rm} into consideration, the PBL407 bridge rectifier from Silitek was chosen with I_{FAV} = 4 A and

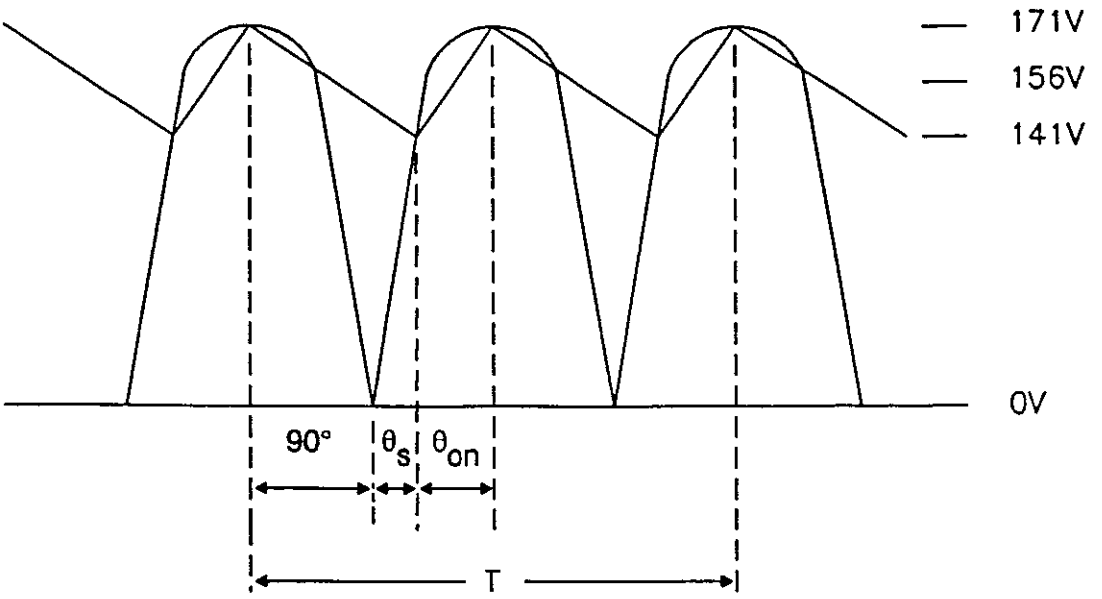

Figure 4.5 The output waveform from the input rectifier and filter circuit.

V_{rm} = 1000 V.

All that remains now is to verify that the bridge rectifier's maximum junction temperature θ_{jmax} is not exceeded. The method as described in [1] is followed. Figure 4.5 represents the output waveform from the input rectifier and filter circuit.

At an input voltage of 110 V the input rectifier and filter circuit will operate in the voltage doubler mode. Therefore C_{16} and C_{17} will in turn charge to a peak voltage of

$$V_p = \sqrt{2}(110\ V_{rms}) + 0.5V_{p\text{-}p} \quad (V) \qquad (4\text{-}18)$$

$$V_p = 171\ V$$

At a peak voltage of +171 V the phase angle will be 90°. With a peak-to-peak ripple voltage V_{p-p} of 31 V centering about +156 V the diode will start conducting at +140 V, corresponding to a phase angle of

$$\theta_s = \sin^{-1} \frac{140\ V}{171\ V} \tag{4-19}$$

$$\theta_s = 54.96°$$

giving a diode conduction interval of

$$\theta_{on} = 90° - \theta_s \tag{4-20}$$

$$\theta_{on} = 35.04°$$

which corresponds to a diode conduction time t_{on} (at 50 Hz) of

$$t_{on} = (\frac{35.04}{180}) 10 \times 10^{-3} \quad (s) \tag{4-21}$$

$$t_{on} = 1.95\ ms$$

During t_{on} the diode will conduct a peak forward current I_{FM} of

$$I_{FM} = \frac{V_{p-p} \times C_{16/17}}{t_{on}} + I_{iAV(110)} \quad (A) \tag{4-22}$$

$$I_{FM} = 13.77\ A$$

assuming a diode forward voltage drop V_F of 1.1 V.

The peak power dissipation during t_{on} will be

$$P_D = I_{FM} \times V_F \quad (W) \tag{4-23}$$

$$P_D = 15.15\ W$$

resulting in an average power dissipation per diode of

$$P_{ave} = P_D \times \frac{1.95\ ms}{20\ ms} \quad (W) \tag{4-24}$$

$$P_{ave} = 1.48\ W$$

with a thermal resistance of junction to case R_{thjc} = 15 °C/W. The junction temperature will rise

$$\Delta T_j = P_{ave}(15°C/W) \quad (°C) \tag{4-25}$$

$$\Delta T_j = 22.2\ °C$$

Although the junction temperature rises ± 22 °C above the case, it is still well below the allowable junction temperature. The choice made is therefore acceptable.

4.4. THE INRUSH CURRENT LIMITING RESISTOR

Since the converter operates directly from mains into the capacitive input filter, a large inrush current will flow in the supply lines, RFI/EMI filter, switch (SW1), fuse and rectifier diodes at switch on. Initially the inrush current is only limited by two components:

1) The low impedance of the mains R_i (of only a few milliohms) and
2) The filter inductance L_i.

This only adds up to a few milliohms, which is not enough to limit the inrush current sufficiently to prevent the operation of the fuse or the destruction of the input rectifier diodes.

Thus some method of inrush current limiting control should be implemented. The method used is illustrated in Figure 4.6, whereby a series inrush-limiting resistor is placed in one of the supply lines.

From [2] the series inrush-limiting resistor R_{23} is calculated as follows. Taking the average that fuses can handle between 50 to 100 A of surge current for a very short period of time (a few milliseconds), the value for R_{23} is calculated.

$$R_{23} \geq \frac{V_{imax(220)}}{100 - 50A} \quad (\Omega) \qquad (4\text{-}26)$$

$$R_{23} \geq 3.4 - 6.8\ \Omega$$

Selected R_{23} = 6.8 Ω/ 5 W.

With the addition of R_{23} the inrush current is limited to approximately 50 A. The power loss in R_{23} is calculated as follows.

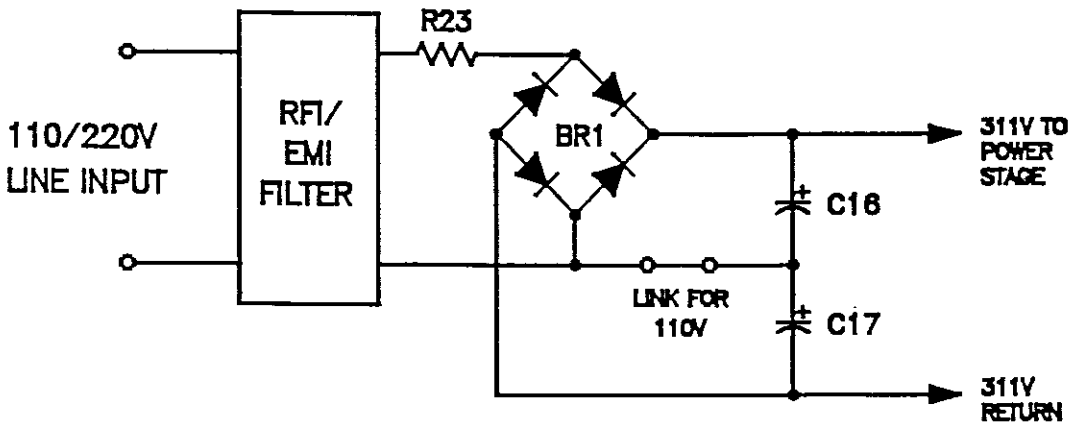

Figure 4.6 The simplified input rectifier and filter circuit, illustrating the addition of the series inrush-limiting resistor R_{23}.

From [2] the input rms current I_{irms} is

$$I_{irms} = I_{iAV(220)} \frac{k_{fD}}{\sqrt{2}} \quad (A) \tag{4-27}$$

$$I_{irms} = 4.29\ A$$

This results in a power loss of

$$P_{R23} = I_{irms}^2 \times R_{23} \quad (W) \tag{4-28}$$

$$P_{R23} = 125\ W$$

taking into consideration that this result alone would reduce the overall efficiency by 43%, which makes it unacceptable.

A method must therefore be applied that would short circuit R_{23} after a few milliseconds (or when the filter capacitors are fully charged). A time-delay relay is selected for this

function. The design of the active limiting circuit (time-delay relay) is discussed in Section 4.5.

4.5. THE TIME-DELAY RELAY

Due to the fact that R_{23} will be very dissipative under normal operating conditions, resulting in a considerable decrease in efficiency as shown in Section 4.4, it was decided to bypass the limiting device by a relay (once the input filter capacitor C_e has been fully charged). The circuit is shown in Figure 4.7.

The values for the different components are calculated in the following paragraphs.

A suitable relay from Takamisawa (VS 48TBU-5) was selected with the following specifications:

Contact ratings	:	Maximum switching voltage, 240 V
		Maximum switching current, 10 A
Coil ratings	:	Operating range, 34 - 100 V
		Nominal voltage, 48 V
		Coil resistance, 3k3 ± 10%

Applying the voltage divider principle, R_{26} is calculated using equation (4-29). R_{26} should be selected such that the minimum relay operating voltage of 34 V is attained at $V_{imin(220)}$ and that the maximum operating voltage of 100 V is

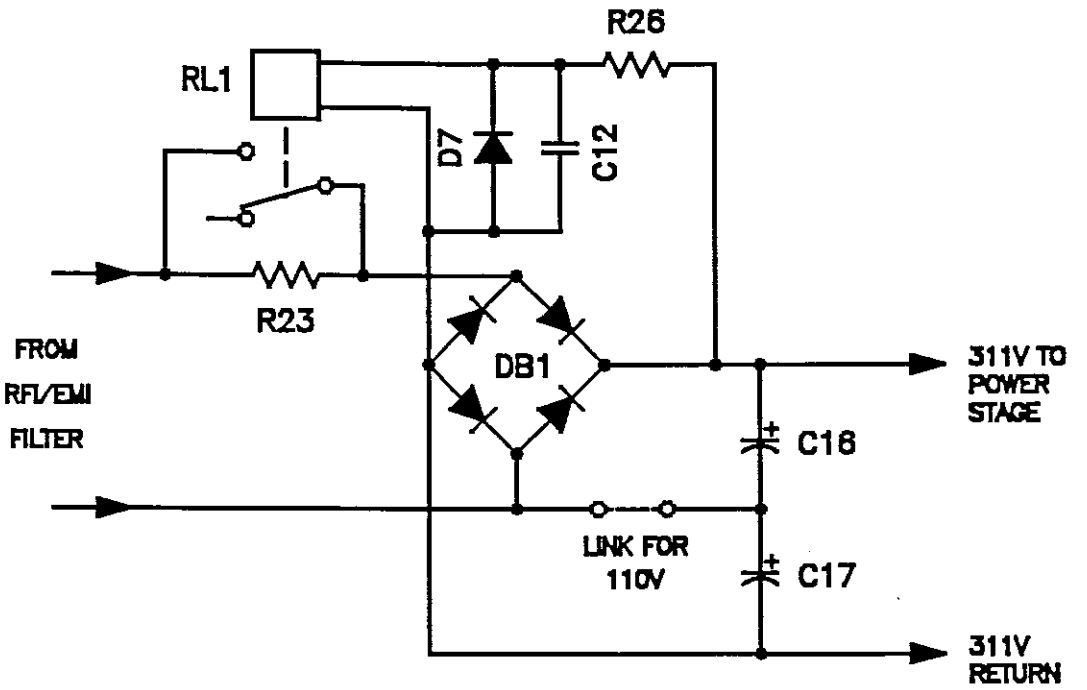

Figure 4.7 Resistive inrush-limiting circuit with a relay bypass to improve efficiency.

not exceeded at $V_{imax(220)}$.

Hence

$$R_{26} \leq \frac{V_{imin(220)} - V_{RL1(min)}}{V_{RL1(min)}} \times (R_{RL1}+10\%) \quad (\Omega) \qquad (4\text{-}29)$$

$$R_{26} \leq 24.45\ k\Omega$$

Selected R_{26} = 22 kΩ.

$$I_{R26} = \frac{V_{imax(220)}}{R_{26}+(R_{RL1}-10\%)} \quad (A) \qquad (4\text{-}30)$$

$$I_{R26} = 13.62\ mA$$

Power dissipation for R_{26}

$$P_{R26} = I_{R26}^2 \times R_{26} \quad (W) \tag{4-31}$$

$$P_{R26} = 4.1\ W$$

Selected R_{26} = 22 kΩ/5 W.

At $V_{imax(220)}$, the maximum relay operating voltage will be

$$V_{RL1(max)} = I_{R26} \times (R_{RL1}+10\%) \quad (V) \tag{4-32}$$

$$V_{RL1(max)} = 49.44\ V$$

thus $V_{RL1(max)}$ < 100 V, which is still within the safe operating margin of the relay coil.

The value for C_{12} is calculated using the following method.

With R_{26} and C_e forming a simple RC circuit, the time taken for C_{26} to reach 63% of full charge or one time constant (τ) is given by equation (4-33).

$$\tau = R_{26} \times (C_e + 20\%) \quad (ms) \tag{4-33}$$

$$\tau = 2.77\ ms$$

Assuming that the input filter capacitor C_e would be fully charged within 5 time constants, an operation delay of at least 10 to 20 ms should be selected.

Therefore

$$C_{12} = \frac{\tau}{R_{26}} \quad (F) \tag{4-34}$$

$$C_{12} = 681.8\ nF$$

It should be noted that equation (4-34) only results in an approximate value for C_{12}. The final value for C_{12} should be practically adjusted to compensate for the mechanical characteristics of the relay and the inductance of the coil windings.

Selected C_{26} = 1 μF/400 V.

4.6. MAINS EMI/RFI FILTER

There are many regulatory authorities world wide which limit the permitted interference levels by laws. Therefore the selection of such a filter will vary according to the country of origin, regulatory authority applicable and intended application.

The FCC EMI/RFI regulations follow that of the VDE closely, with VDE regulations the more stringent of the two (VDE regulations specify conducted EMI/RFI emissions over a wider spectrum, from 10 kHz to 30 MHz). The selected EMI/RFI filter should at least contain the VDE-Mark.

The input current rating rms of the filter should at least

exceed that calculated in equation (4-27) or I_{irms} = 4.29 A.

Selected the EMI/RFI filter from the Shurter company rated at 6 A/250 V.

4.7. INPUT FUSE

The maximum input current I_{irms} will flow when the SMPS is operated from a line voltage of 110 V, adapting equation (4-27) for a line voltage of 110 V.

$$I_{irms} = I_{iAV(110)} \frac{k_{fD}}{\sqrt{2}} \quad (A) \qquad (4\text{-}35)$$

where $I_{iAV(110)}$ = 2.96 A from equation (4-15).

The new value for k_{fD} is given by equation (4-8), adapting for a line voltage of 110 V

$$X = \frac{V_{p\text{-}p}}{V_{imin(110)}}$$

where

$$V_{imin(110)} = (V_{i(110)} \times 0.85 \times \sqrt{2}) - 2V_F \quad (V) \qquad (4\text{-}36)$$

$$V_{imin(110)} = 130\ V$$

With the ratio X = 0.24, the value for k_{fD} is read off from Figure 4.3, page 27 (k_{fD} = 3.4), substituting into (4-29)

$$I_{irms} = 2.96 \times \frac{3.4}{\sqrt{2}}$$

$$I_{irms} = 7.12\ A$$

From [3] the fuse's current rating should be selected approximately 150% of I_{irms}, resulting in a maximum fuse current of 1.5 × 7.12 A = 10.68 A, which insures a longer fuse life.

To prevent excessive arcing during a fault condition the fuse should be rated for 250 V.

Compromising between a line operating voltage of 110 volt or 220 volt a (5.1 A/250 V) slow-blow fuse was selected.

4.8. AUXILIARY POWER SUPPLY

Figure 4.8 shows the auxiliary power supply for the converter, which basically consists of two circuits: a linear regulator formed by R_{27}, R_{30}, Z_1 and Q_7, also called the start-up regulator, and an auxiliary winding ($N_{s(1a)}$ and $N_{s(1b)}$) in the power transformer T2 followed by a LC filter and a post-regulator VR1. The post-regulator is a LM340T15 and provides additional output regulation.

At turn-on the start-up regulator supplies approximately +10 volts to the control and driver circuits. Converter operation is initiated and the auxiliary winding in the power

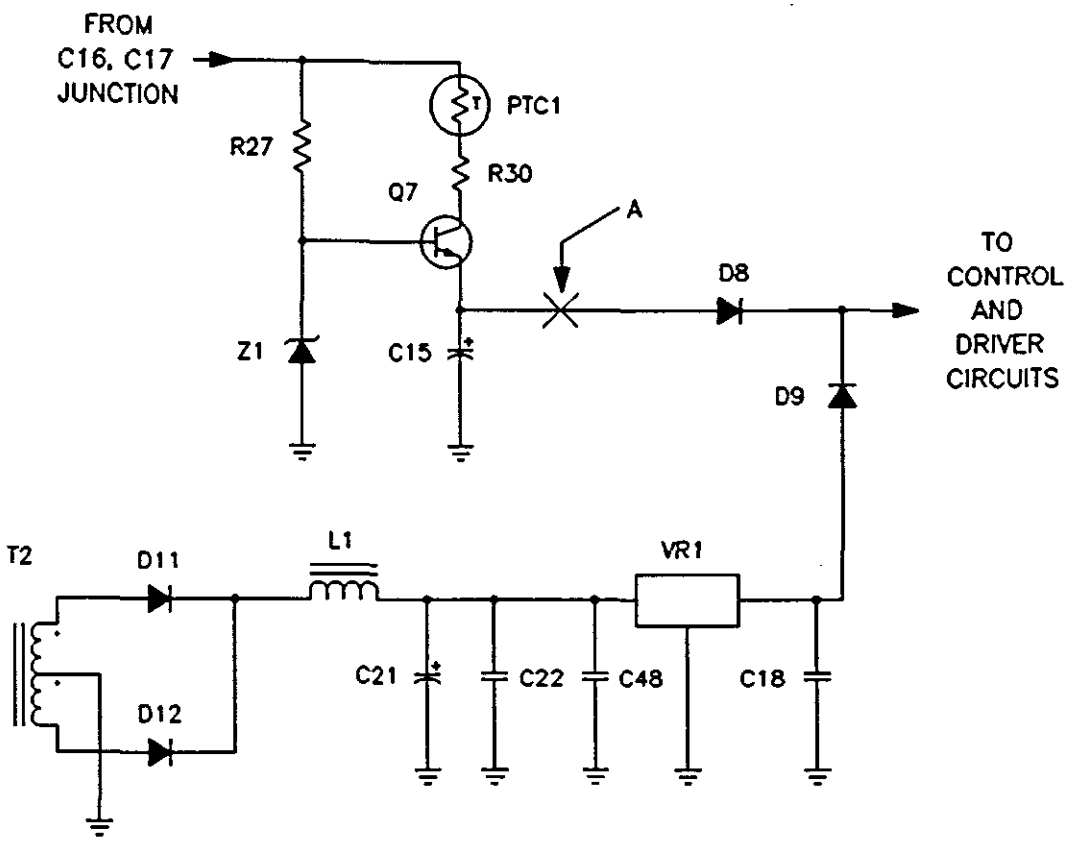

Figure 4.8 The auxiliary power supply.

transformer provides an output voltage of +15 volt, back-biasing diode D_8 and turning off the start-up regulator.

The converter therefore generates its own supply voltage of +15 volts in order to maintain its operation, while the more dissipative start-up regulator is turned off.

Since the design of the post-regulator VR1 is fairly straightforward only the design of the start-up regulator will be presented in this section.

Selecting the zener diode Z_1:

When selecting the zener diode voltage, allowance should be made for a voltage drop of 0.7 V in the base-emitter path of transistor Q_7.

A zener diode (BZX83C12V) was selected, giving a voltage at point A of 11.3 volt.

Determining the value for R_{27}:

From [2] the value for R_{27} is calculated using the following two equations.

$$R_{27} \leq \frac{V_{imin(110)} - V_{Zmax}}{I_{Bmax} + I_{Zmin}} \quad (\Omega) \qquad (4\text{-}37)$$

$$R_{27} \geq \frac{V_{imax(110)} - V_{Zmin}}{I_{Bmin} + I_{Zmax}} \quad (\Omega) \qquad (4\text{-}38)$$

Where

$V_{imin(110)}$ = 130 V

$V_{imax(110)}$ = 169 V

V_{Zmin} = 11.4 V (from data sheet)

V_{Zmax} = 12.6 V (from data sheet)

I_{Zmin} = 2 mA

I_{Zmax} = 45 mA

I_{Bmin} = 0 A

I_{Bmax} = 1 mA

Therefore

$$R_{27} \leq 39.13\ k\Omega$$

and

$$R_{27} \geq 3.5\ k\Omega$$

The value for R_{27} should be selected so that at $V_{imin(110)}$;

1) a sufficient current would still flow in the zener diode (I_{Zmin} = 2 mA) and
2) the base current would be more than adequate to sustain maximum collector current I_{Cmax}.

Selected R_{27} = 33 kΩ/1.6 W.

Maximum power dissipated in R_{27}

$$P_{R27} = \frac{(169 - 12)^2}{33 \times 10^3} \quad (W)$$

$$P_{R27} = 0.75\ W$$

Selecting Transistor Q_7:

To keep the losses to a minimum the maximum transistor collector current I_{Cmax} selected should not exceed 50 mA. With the maximum value set, a I_{Cmax} of 45 mA is selected.

Therefore a transistor with a minimum V_{CE} rating of 200 V and a maximum collector current rating of at least 30 - 70 mA should be selected. The 2N3439 was selected.

Determining the value for R_{30}:

The value for R_{30} is calculated using equation (4-39).

$$R_{30} \leq \frac{V_{imin(110)} - V_Z}{I_{Cmax}} \quad (\Omega) \qquad (4\text{-}39)$$

$$R_{30} \leq 2.62\ k\Omega$$

Selected R_{30} = 2.7 kΩ/5 W.

The start-up regulator, as previously mentioned, is a very dissipative circuit, being used for a brief period only to initialise converter operation during start-up after which it is "turned off". But what will happen if the start-up regulator is forced to operate continuously as would occur during a converter failure or shutdown? This will be investigated in the following paragraphs.

During a converter failure or shutdown excessive power will be dissipated in R_{30} and Q_7 as will be shown in the following analyses.

Power dissipated in R_{30} during a fault condition:

Maximum power dissipated in R_{30} will be

$$P_{R30} = \frac{V_{R30}^2}{R_{30}} \quad (W) \tag{4-40}$$

$$P_{R30} = 10.7\ W$$

From equation (4-40) it is noted that the selected resistor of 5 W is by far underrated. It would therefore be more suitable to substitute or add a PTC thermistor in series with R_{30}, reducing the excessive power dissipation in the resistor during a fault condition. A PTC thermistor from Siemens, type Q63100-P2350-C870 was placed in series with R_{30}, creating a "fail safe" condition.

Power dissipated in Q_7 during a fault condition:

The only time when maximum power will be dissipated in the transistor is when maximum current and maximum voltage $V_{imax(110)}$ are applied. Therefore maximum power dissipated in the transistor will be

$$P_{Q_7(max)} = (V_{imax(110)} - I_{Cmax}R_{30} - V_Z)\, I_{Cmax} \quad (W) \tag{4-41}$$

$$P_{Q_7(max)} = 1.6\ W$$

The thermal resistance for the transistor's heatsink is calculated using equation (4-42).

With

$\theta_{jmax} = 150\ °C$

$\theta_{amax} = 45\ °C$

$R_{thjc} = 35\ °C/W$

$$R_{thca} \leq \frac{\theta_{jmax} - \theta_{amax}}{P_{Q_7\,(max)}} - R_{thjc} \quad (°C/W) \qquad (4\text{-}42)$$

$$R_{thca} \leq 31\ °C/W$$

A heatsink from Assmann, type V623C with 31 °C/W was selected.

5. THE DESIGN OF THE POWER STAGE

The schematic diagram for the power stage is shown in Figure 5.1.

The following sections will be presented in this chapter:

1) Selection of the power MOSFET transistors
2) The driver circuit
3) Series coupling capacitor C_{24}
4) Design of the power transformer T2 and
5) Overcurrent limiting.

5.1 SELECTION OF THE POWER MOSFET TRANSISTORS

With the half-bridge push-pull topology the voltage across each MOSFET will never exceed the input voltage V_i. Therefore the selected MOSFET must at least have an off-state voltage of 400 V.

Before a suitable MOSFET is selected the necessary reduction in permissible drain current and the increase in $R_{DS(on)}$ with increasing temperature must be accounted for in any further calculations.

Taking this into consideration the maximum permissible drain current I_{Dmax} is calculated.

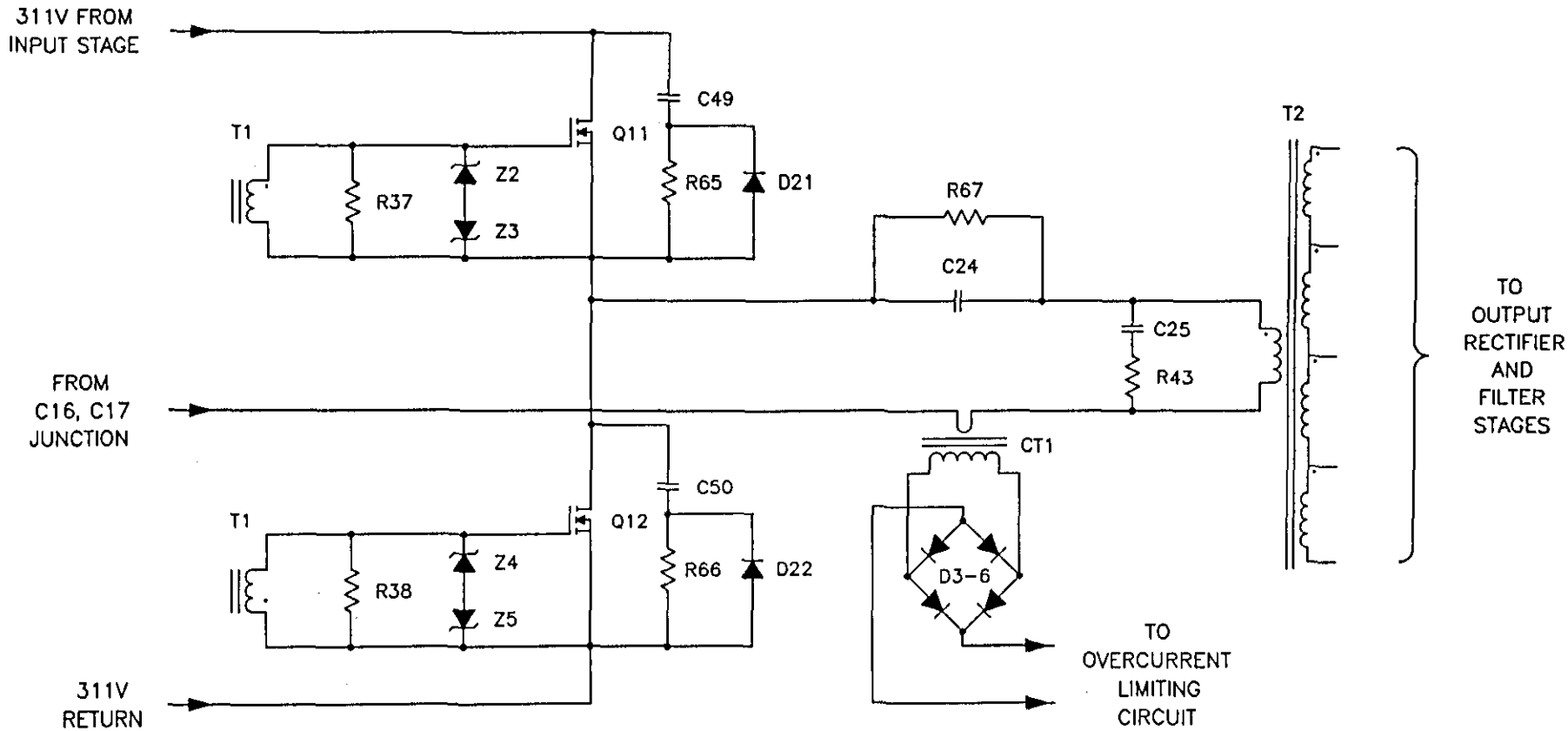

Figure 5.1 The power stage for the half-bridge push-pull converter.

From Section 4.1 an input power of 388 W is obtained, which means that each MOSFET must alternatively switch a total of 388 watts. Maximum drain current will be obtained at a minimum input voltage V_{imin} of 263 V. With 263 V/2 or 132 V appearing across each MOSFET the maximum drain current I_{Dmax} will be

$$I_{Dmax} = \frac{388\ W}{132\ V} \quad (A) \tag{5-1}$$

$$I_{Dmax} = 2.94\ A$$

This represents only a theoretical value. To obtain a more practical value the result in equation (5-1) is multiplied by a correction factor of 1.4, which includes the sum of $\frac{\Delta I_L}{2}$

reflected from the secondary (+20%) and a portion of the magnetising current (+20%). The new maximum drain current $\acute{I}_{Dmax}$ will therefore be equal to

$$\acute{I}_{Dmax} = I_{Dmax} \times 1.4 \quad (A) \tag{5-2}$$

$$\acute{I}_{Dmax} = 4.12\ A$$

The mean drain current I_{DAV} is calculated using equation (5-3) from [2]

$$I_{DAV} = \acute{I}_{Dmax} \times \delta_{Tmax} \quad (A) \tag{5-3}$$

With a maximum duty cycle δ_{Tmax} of 0.4 and $\acute{I}_{Dmax}$ of 4.12 A the mean drain current will be

$$I_{DAV} = 1.65\ A$$

The selected MOSFET must therefore be capable of sustaining a mean drain current of at least 1.65 A.

To summarise:

The selected MOSFET must therefore at least satisfy the following two requirements:

$$V_{DS} \geq 400\ V$$

$$I_D \geq 4.5\ A$$

Selected the IRF 740 from International Rectifier.

To ensure that the selected MOSFET transistor is suitable for the application, the losses within the device should be analyzed.

Conduction loss:

From [2] the conduction loss P_{Trc} is calculated using equation (5-4). With the on-state resistance $R_{DS(on)}$ not given in the data sheets it will be assumed as 1.7 Ω at a reasonable junction temperature of 100 °C.

Therefore

$$P_{Trc} = R_{DS(on)max}\, I^2_{Dmax}\, \delta_{Tmax} \quad (W) \qquad (5\text{-}4)$$

$$P_{Trc} = 11.54\ W$$

Turn-on loss:

From [2]

$$P_{Trs(on)} = V_{imax}\, I_{Dmax}\, (\frac{t_r}{2})\, f_s \quad (W) \tag{5-5}$$

$$P_{Trs(on)} = 3.5\ W$$

The switching times t_r and t_f are dependent on the driver circuit used. For this application it was found that a t_r and t_f time of 100 ns would be a good estimate.

Turn-off loss:

$$P_{Trs(off)} = V_{imax}\, I_{Dmax}\, (\frac{t_f}{2})\, f_s \quad (W) \tag{5-6}$$

$$P_{Trs(off)} = 3.5\ W$$

which is the same as the turn-on loss.

The total transistor loss is thus

$$P_{Tr(tot)} = P_{Trc} + P_{Trs(on)} + P_{Trs(off)} \quad (W) \tag{5-7}$$

$$P_{Tr(tot)} = 18.54\ W$$

The transistor loss of 18.54 W represents a 5% (per transistor) reduction in overall converter efficiency, which

is quite acceptable.

Recommended heatsink:

$$R_{thca} \leq \frac{\theta_{jmax} - \theta_{amax}}{P_{Tr(tot)}} - R_{thjc} \quad (°C/W) \tag{5-8}$$

$$R_{thca} \leq \frac{125\ °C - 45\ °C}{18.54\ W} - 1\ °C/W$$

$$R_{thca} \leq 3.32\ °C/W$$

Selected a SK104 from Fisher with a R_{thca} of 9 °C/W. With forced air cooling used, the thermal resistance of the selected heatsink is further increased to approximately 0.5 °C/W, which is more than sufficient.

5.2. DRIVER CIRCUIT

One of the main disadvantages of the half-bridge push-pull topology is that a floating drive is required for the MOSFET transistor Q_{11}. To solve this problem a balanced push-pull transformer coupling or pulse transformer will be used. The circuit is shown in Figure 5.2.

The pulse transformer therefore not only solves the floating drive requirement, but also provides the necessary isolation and phasing for the secondary windings.

Another requirement for driving MOSFET transistors is that

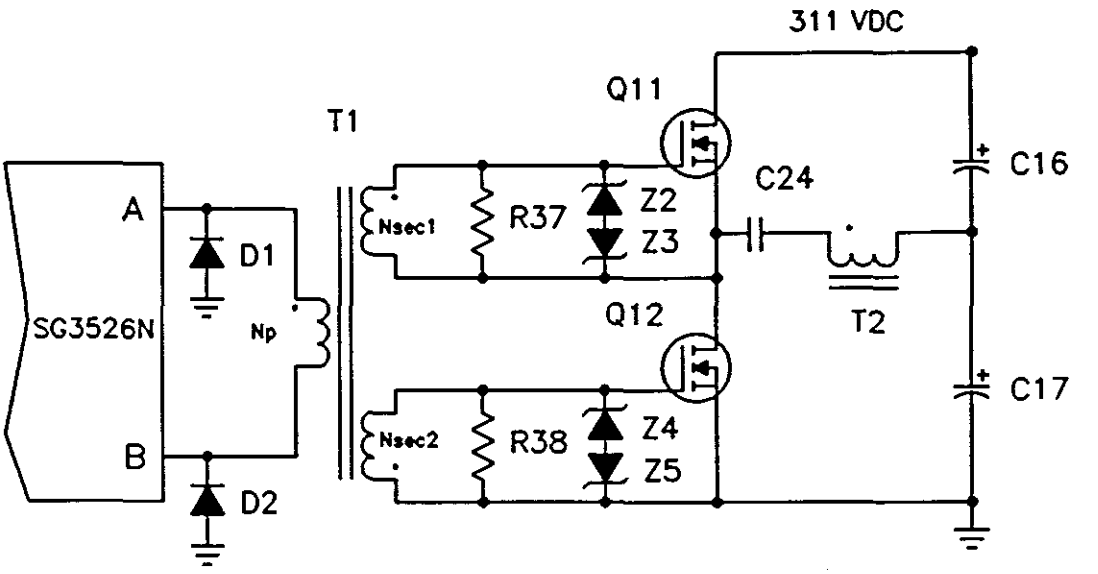

Figure 5.2 The driver circuit for the half-bridge push-pull topology using transformer coupling.

the driver should be a low-impedance push-pull type, for example a totem-pole driver. The reason for this is to keep the MOSFET transistor from oscillating during turn-on as would happen in a high-impedance drive circuit.

To obtain a low-impedance drive requirement, minimum components and simplicity the SG3526N regulating pulse width modulator was selected. Figure 5.3 shows the internal totem-pole driver of the SG3526N, providing the necessary low-impedance drive requirement. The increased drive current of 200 mA also adds to circuit simplicity, making it possible to implement the driver circuit as shown in Figure 5.2.

Care should be taken in the selection of the voltage to be supplied to the MOSFET's gate. First the voltage should be

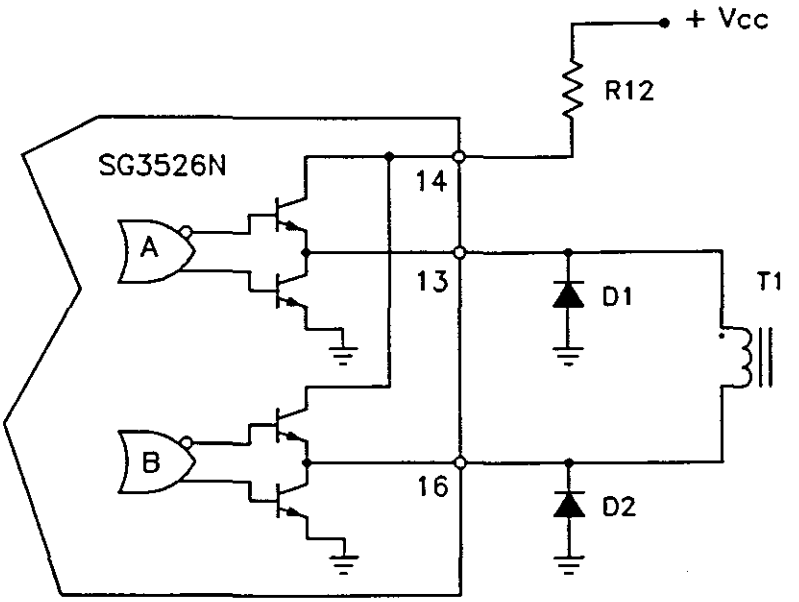

Figure 5.3 The simplified internal circuit for the SG3526N, indicating the totem-pole output driver and the externally mounted current limiting resistor R_{12}.

adequate to switch the MOSFET hard-on and secondly the voltage should not exceed the maximum permissible gate voltage of ± 20 V.

The auxiliary power supply (Section 4.8) was designed for 15 V. From the transfer characteristics of the IRF 740 Figure 5.4 a gate voltage of 5 V would be necessary to switch on the MOSFET. Although a gate voltage of 8 V would ensure a low residual voltage, it was decided to use the same voltage (15 V) as supplied by the auxiliary power supply to drive the MOSFETs, leaving a 5 V safety margin.

The design of the pulse transformer:

With a gate voltage of 15 V, the pulse transformer will be

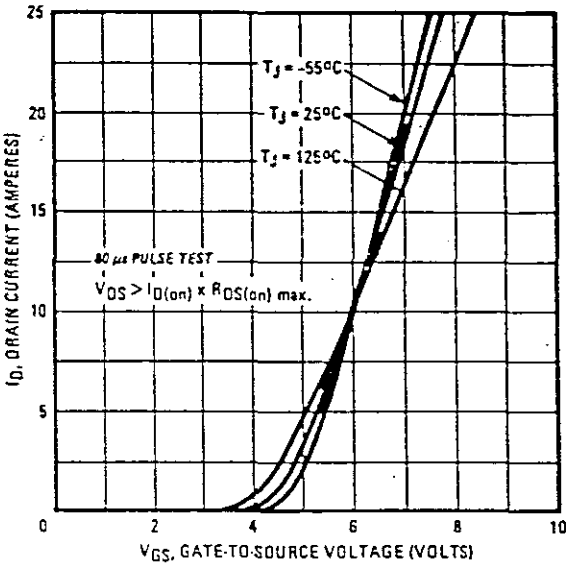

Figure 5.4 The typical transfer characteristic for the IRF 740 (abstract from [4]).

designed for a turns ratio of 1:1. The main design objective of the pulse transformer T1 was to keep the magnetising current below 70 mA, thus keeping the steady state power consumption low.

From [2] the primary inductance L_p is calculated using equation (5-9). Rearranging the variables

$$L_p = \frac{V_p \, \delta_{Tmax}}{I_M \, f_s} \quad (H) \qquad (5\text{-}9)$$

where

L_p - primary input voltage, V

δ_{Tmax} - maximum duty cycle

I_M - magnetising current, A

f_s - switching frequency, Hz

A maximum duty cycle δ_{Tmax} of 0.4 is selected.

Substituting into equation (5-9)

$$L_p = \frac{15 \times 0.4}{(66 \times 10^{-3})(100 \times 10^3)}$$

$$L_p = 909.1\ \mu H$$

Once the primary inductance has been calculated a suitable core material can be selected.

Taking the size and availability of core materials into consideration, an EE ferrite core (E20/10/5) of the 3E1 material from Philips was selected (Appendix I).

With an inductance factor of A_L = 1 920 nH (worst case) the number of primary turns N_p can be calculated with equation (5-10).

$$N_p = \sqrt{\frac{L_p}{A_L}} \qquad (5\text{-}10)$$

$$N_p = 21.76\ T$$

Selected N_p = 22 T.

To ensure that the applied pulse does not saturate the selected core material it should be verified before

finalising the design because core saturation would reduce the primary inductance to a very low value, resulting in the distortion of the pulse.

Using the method described in [5], core saturation can be verified. Therefore from [5] follows that

$$B_{max} = \frac{a\ V_p\ t_{on} \times 10^4}{N_p\ A_e} \quad (T) \qquad (5\text{-}11)$$

where

B_{max} - maximum flux density, T

a - attenuation factor

t_{on} - conducting "on" time period, s

N_p - number of primary turns

A_e - effective core cross-sectional area, cm^2

The attenuation factor is selected so that a = 1, thus obtaining a maximum possible flux density. The pulse duration is selected for that obtained during $\delta_{Tmax} = 0.4$.

Substituting the variables

$$B_{max} = \frac{1 \times 15 \times (4 \times 10^{-6}) \times 10^4}{22 \times 0.312}$$

$$B_{max} = 87.41\ mT$$

From the data sheet in Appendix I it is clearly seen that $B_{max} << B_{sat}$, thus the core does not saturate under these

conditions. Also note that $B_{max} < 0.1$ T, ensuring a good pulse characteristic.

Having selected a turns ratio of 1:1 the two secondary windings will have the same amount of turns as the primary winding.

Therefore

$$N_p = N_{sec1} = N_{sec2} = 22 \text{ T}$$

Note: The secondary windings of the pulse transformer T1 should be **out of phase** as shown in Figure 5.2 ensuring alternate conduction of the two MOSFET transistors.

The winding design for the pulse transformer:

Since the MOSFETs are only supplied with short charging and discharging pulses from the pulse transformer thinner wire diameters can be selected for the windings. Wire sizes will also be chosen so as to fill the coil former.

As previously stated each winding consists of 22 turns. Therefore each winding will fill approximately ⅓ of the total window area W_a, taking into consideration the necessary insulation requirements.

From equation (5-12) an approximate wire diameter can be calculated. Since all windings have the same number of

turns, the number of turns N can be taken as the sum of all three windings, namely N = 3 × 22 = 66 turns.

From [2] follows that

$$d \leq \sqrt{\frac{4\ W_a\ K_u}{N\ \pi}} \quad (cm) \qquad (5\text{-}12)$$

where

W_a - window area, cm^2

K_u - window utilisation factor

N - number of turns

d - wire diameter including isolation, cm

Hence

$$d \leq \sqrt{\frac{4 \times 0.4 \times 0.27}{66 \times \pi}}$$

$$d \leq 0.0457\ cm$$

From the AWG winding data table Appendix C, it follows that a single wire of d = 0.046 cm (AWG # 26) can be used.

Figure 5.5, page 61 shows the coil former's maximum winding length and winding depth.

With a wire diameter of d = 0.046 cm chosen, the primary winding can be wound in one layer, thus occupying 22 × 0.46 mm = 10.12 mm, leaving 0.34 mm on each side. In terms of the insulation requirements this is not adequate. At least 1.8 mm

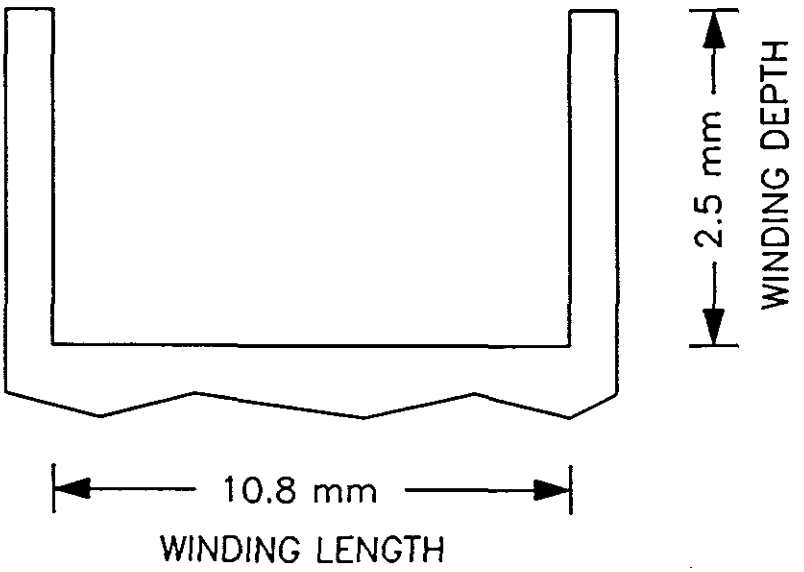

Figure 5.5 The E20/10/5 coil former, indicating the winding length and depth.

will be required on each side to provide the necessary creepage distance of approximately 4 mm (see Figure 5.6) between windings (for example the primary and secondary winding).

It was then decided to use the multiple wire technique, where each wire is made up of 2 or 3 strands (see Figure 5.6 for clarity). Using 2 strands of wire with a diameter of d = 0.033 cm per strand, with 11 turns per layer, the primary winding would occupy 11 × 2 × 0.33 mm = 7.26 mm, leaving 1.77 mm on each side. The primary winding will now consist of 2 layers with a winding depth of 0.66 mm. The same applies for the two secondary windings.

The total winding depth will thus be equal to 6 × 0.33 mm = 1.98 mm, leaving 0.52 mm for the protective layer and

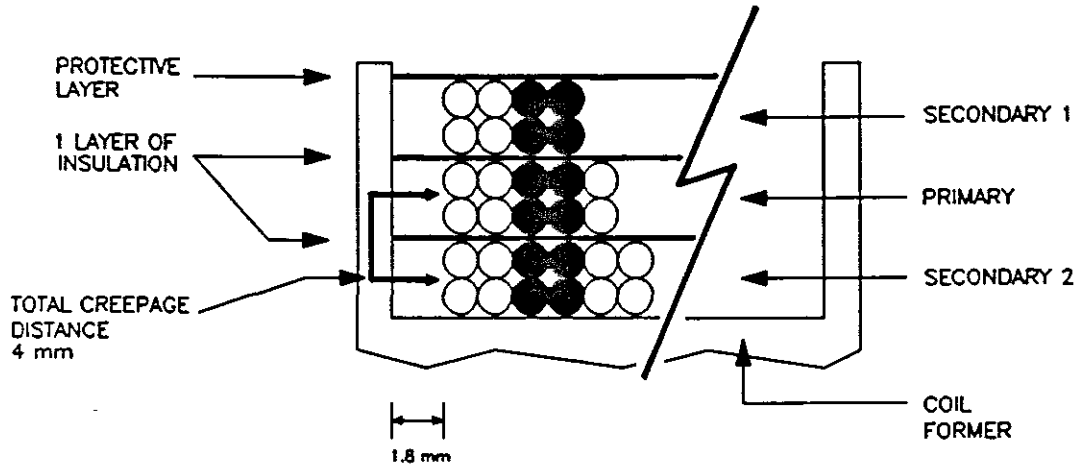

Figure 5.6 Cross-sectional view of the coil former showing the build, creepage distance and multiple wire winding technique used. (The strands indicated by the black dots, refer to one turn).

insulation film between the primary, secondary 1 and secondary 2 windings. In Figure 5.6 it can be seen that if the primary winding is wound exactly in the middle, it would leave a space of ± 1.8 mm on each side. Thus the total separation between the primary and the secondary will be approximately 2 × 1.8 mm = 3.6 mm. Adding the thickness of the insulation film to this, should provide the necessary creepage distance of 4 mm. This concludes the pulse transformer design.

The selection of the ancillary components:

Additional protection for the MOSFET transistors are provided by placing two 15 V zener diodes back to back between the gate and source. Low power zener diodes can be selected. The resistor R_{37} and R_{38} of 1 kΩ each assist the MOSFET in

turning off.

To prevent the pulse transformer's leakage inductance from forcing the output of the SG3526N negative when it turns off, external diodes D_1 and D_2 are added to provide the necessary clamping action. D_1 and D_2 should be fast switching diodes. Selected 1N5819 from Silitek.

5.3. SERIES COUPLING CAPACITOR

The series coupling capacitor C_{24} is placed in series with the power transformer's primary winding where it is used to maintain the balance of the volts-second integral between the switching devices or MOSFET transistors.

The unbalance in the volts-second integral is caused by the inevitable asymmetry found in the switching devices e.g. unequal storage times and saturation voltages. The capacitor senses the volts-second unbalance and converts it to a proportional shift in DC level, resetting the volts-second unbalance, thus preventing flux walking, which will eventually result into core saturation and the possible destruction of the switching devices.

An approximate value for C_{24} is obtained by using the method described in [6].

From [6], taking worst case conditions, it follows that

$$C_{24} = I_{pmax}\frac{dt}{dV_c} \quad (F) \tag{5-13}$$

where

I_{pmax} - maximum primary current, A

dt - charging interval, s

dV_c - charging voltage, V

This leaves two unknown variables dt and dV_c. The charging interval is calculated by using equations (5-14) and (5-15).

$$T = \frac{1}{f_s} \quad (s) \tag{5-14}$$

$$T = 10 \times 10^{-6}\ s$$

$$dt = T\delta_{Tmax} \tag{5-15}$$

$$dt = 4 \times 10^{-6}\ s$$

The charging voltage dV_c, according to [6] is selected such that it falls within the 10 - 20% margin of $\frac{V_{imax}}{2}$ or 170 V.

Therefore

$$17\ V \leq dV_c \leq 34\ V$$

Selected dV_c = 30 V. $I_{pmax} = \acute{I}_{Dmax}$ = 4.12 A as calculated in equation (5-2).

Substituting into equation (5-13)

$$C_{24} = 4.12 \times \frac{4 \times 10^{-6}}{30}$$

$$C_{24} = 549.3\ nF$$

Selected a standard value of 0.47 μF. Although the capacitor voltage can be selected to equal the theoretical value of 30 V, a more practical value of at least 200 V is selected for safety purposes.

To prevent C_{24} from resonating with stray inductances a practically determined damping resistor of 1.8 kΩ/1 W is placed in parallel with it (see Figure 5.1, page 49).

The maximum charging voltage should be verified for the chosen capacitance since an excessive high voltage could interfere with the converter's regulation at low line.

Using equation (5-16) from [6] the charging voltage dV_c is calculated at a nominal mains voltage of 220 V_{rms} and the corresponding mean duty cycle. This is then compared to the practical measured value.

$$dV_c \approx \frac{f_{Dmax}}{C_{24}} dt \quad (V) \qquad (5\text{-}16)$$

$$dV_c \approx 8\ V$$

The obtained charging voltage dV_c of approximately 8 V is

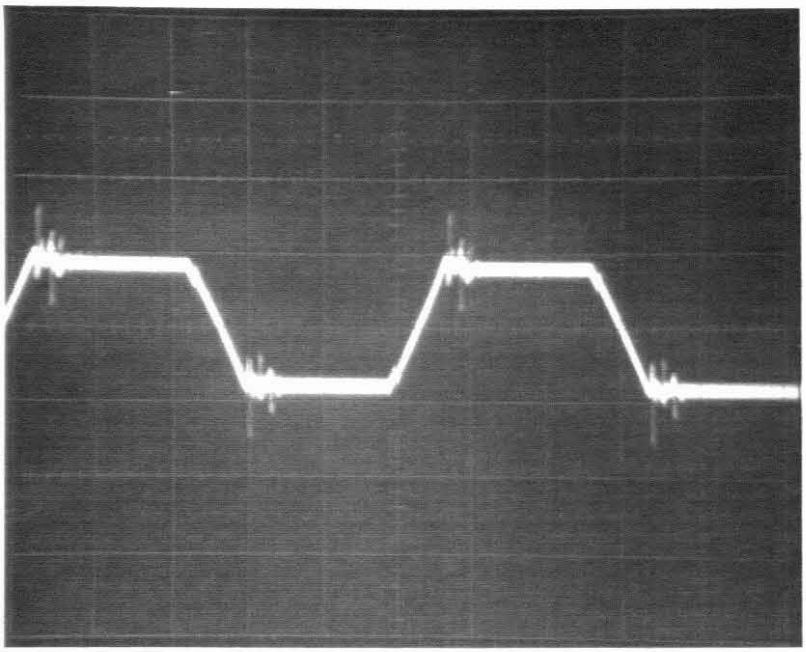

Figure 5.7 The voltage across the series coupling capacitor C_{24}. (Measured at 83% of the rated load $P_{o(max)}$ and nominal input voltage $V_{i(220)}$).

Horizontal scale : 2 μs/division
Vertical scale : 10 V/division

acceptable and also confirmed by Figure 5.7 ($\frac{16V}{2} \approx 8\ V$).

The following guide lines should be taken into account when selecting the series coupling capacitor:

1) it should be a film type
2) nonpolar
3) sustain maximum primary current and
4) have a low ESR value (reduce heating).

Selected a MKT 0.47 μF/400 V metallised film capacitor from Philips.

5.4. THE POWER TRANSFORMER T2

5.4.1. THE APPARENT POWER-HANDLING CAPABILITY

A very good estimate of the transformer's core and winding size can be obtained by considering only the first order effects. This means that the second order effects i.e. core losses, copper losses etc. are not considered.

The apparent power-handling capability P_t, which represents a good estimate of the first-order effects, will be considered in this section.

The apparent power-handling capability P_t may be as much as three times the input power rating, depending on the application of the power transformer.

Figure 5.8 displays some of the symbols that will be used during the design of the multi-output power transformer.

The individual output powers are first calculated and then summed together to obtain the total output power P_Σ from which then follows the input power P_i and the apparent power P_t.

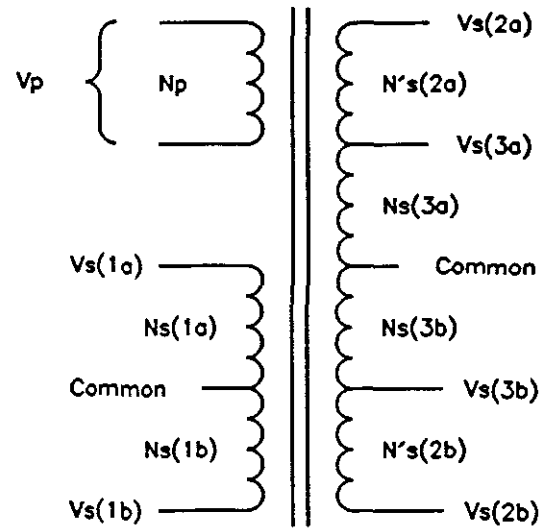

Figure 5.8 The power transformer T2.

Note: $V_F = 1\ V$

$$P_{o(+5)} = (V_{o(+5)} + V_F)\, I_{o(+5)} \quad (W) \tag{5-17}$$

$$P_{o(+5)} = 130\ W$$

$$P_{o(-5)} = (V_{o(-5)} + V_F)\, I_{o(-5)} \quad (W) \tag{5-18}$$

$$P_{o(-5)} = 6.5\ W$$

$$P_{o(+12)} = (V_{o(+12)} + V_F)\, I_{o(+12)} \quad (W) \tag{5-19}$$

$$P_{o(+12)} = 113.6\ W$$

$$P_{o(-12)} = (V_{o(-12)} + V_F)\, I_{o(-12)} \quad (W) \tag{5-20}$$

$$P_{o(-12)} = 14.2\ W$$

$$P_{o(+15)} = (V_{o(+15)} + V_F)\, I_{o(+15)} \quad (W) \tag{5-21}$$

$$P_{o(+15)} = 26.25\ W$$

Summing up the output powers:

$$P_\Sigma = 291\ W$$

With an estimated converter efficiency of 75% ($\eta^* = 0.75$) the input power will be

$$P_i = \frac{P_\Sigma}{\eta} \quad (W) \tag{5-22}$$

$$P_i = 388\ W$$

From [7] the resulting apparent power P_t is calculated using equation (5-23).

$$P_t = P_\Sigma\left(\frac{1}{\eta^*} + \sqrt{2}\right) \quad (W) \tag{5-23}$$

Where

η^* - transformer efficiency (not to be confused with the converter efficiency).

Selected $\eta^* = 0.95$.

Therefore

$$P_t \approx 718\ W$$

The calculated apparent power P_t is related to the area product as described in Section 5.4.4.

Before proceeding with Section 5.4.4 the intended core material and operating flux density should first be selected as described in Section 5.4.2 and 5.4.3.

5.4.2. SELECTING THE CORE MATERIAL

The ETD (Economic Transformer Design) core range from Siemens was selected, using the N27 ferrite material from the same company. The ferrite material has extremely low core losses especially at frequencies above 50 kHz. Therefore the material will be suitable for this application.

5.4.3. DETERMINING THE OPERATING FLUX DENSITY

In the selection of the operating flux density B_m allowance should be made for a working margin. The reason for this is to prevent core saturation during start-up and transient operating conditions (e.g. sudden load changes).

From Figure 5.9 the maximum permissible flux density will be 320 mT at 100°C. Therefore a peak flux density of 320 mT should not be exceeded.

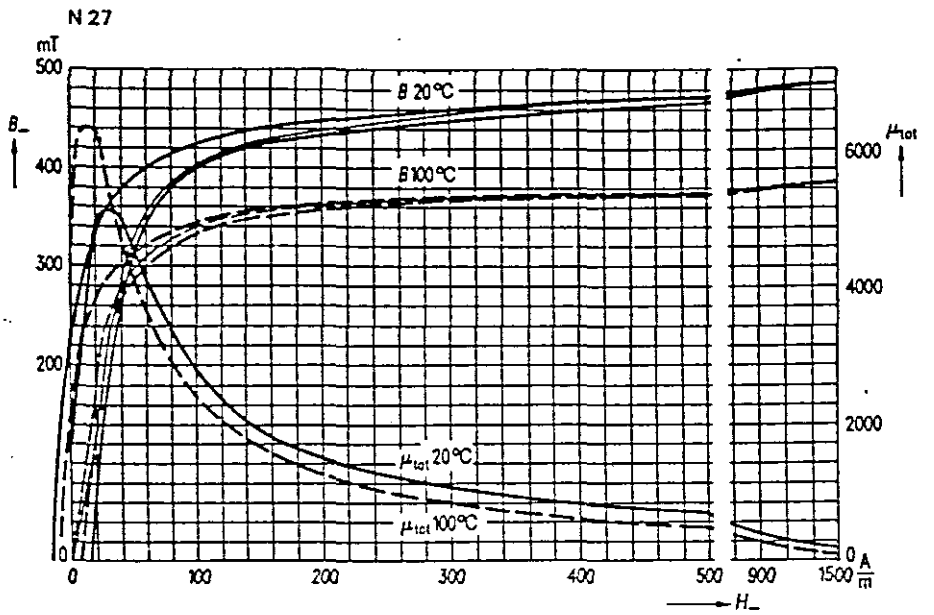

Figure 5.9 The B/H curve for the N27 ferrite material (Siemens).

To obtain a realistic operating flux density two factors will be introduced [8].

The <u>first</u> factor to be introduced is the transient factor α, which is related to the range of input voltages for which the converter is designed. Equation (5-24) describes the transient factor.

$$\alpha = \frac{V_{imax}}{\hat{V}_{imin}} \qquad (5\text{-}24)$$

Note: $\hat{V}_{imin}$ is the minimum voltage across the input capacitor C_e (Section 4.1), corresponding to a discharge time t_d of 8 ms.

From [11] $\acute{V}_{imin}$ will be

$$\acute{V}_{imin} = \sqrt{V_{imin}^2 - \frac{2\ P_i\ t_d}{C_e}} \quad (V) \tag{5-25}$$

$$\acute{V}_{imin} \approx 226\ V$$

Substituting into (5-24)

$$\alpha = \frac{340\ V}{226\ V}$$

$$\alpha = 1.5$$

The second factor to be introduced is the unbalance factor ϵ. Since the series coupling capacitor provides balancing and therefore protection against asymmetry or core saturation the unbalance factor ϵ can be selected as $\epsilon = 1.15$.

The two factors are then represented in equation (5-26) from [8], resulting in the following operating flux density.

$$B_m = \frac{0.32}{\alpha\ \epsilon} \quad (T) \tag{5-26}$$

$$B_m \approx 0.18\ T$$

Although the calculated flux density level is on the high side for an operating frequency of 100 kHz, no reduction in this level will be considered at this stage.

This allows for a smaller core size to be selected as long as

the transformer $\eta^* \geq 95\%$.

The relative increase in the core losses will also have to be accepted as long as the total rise in temperature is not excessive.

5.4.4. SELECTING THE CORE SIZE

From [7] it can be seen that the apparent power-handling capability P_t for the core can be related to its area product A_p as follows.

$$A_p = \left(\frac{P_t \times 10^4}{K_f B_m f_s K_u K_j}\right)^x \quad (cm^4) \qquad (5\text{-}27)$$

where

P_t - apparent power, W

K_f - waveform coefficient

B_m - operating flux density, T

f_s - switching frequency, Hz

K_u - window utilization factor

K_j - current density coefficient

Selected

$x = 1.12$ (Appendix D)

$K_u = 0.4$ (assumed)

$K_j = 665$ (Appendix D)

$K_f = 4$ (for a square wave)

Substituting into (5-27)

$$A_p = \left(\frac{718 \times 10^4}{4 \times 0.18 \times 100 \times 10^3 \times 0.4 \times 665}\right)^{1.12}$$

$$A_p = 0.33\ cm^4$$

Referring to Appendix D the ETD 34/17/11 with an A_p of 1.2 cm^4 could be selected, but the need to meet the UL and VDE safety requirements and the extra space required for the secondary windings (centre-tapped), forced the selection of the next larger core size, namely the ETD 39/20/13.

Note: VDE specifies a minimum of 4- to 8- mm of creepage distance between the primary and secondary windings for off-line applications.

The data for the ETD 39/20/13 (Appendix D and Appendix J):

Area product	:	A_p	= 2.22 cm^4
Mean length turn	:	MLT	= 6.9 cm
Effective core cross-sectional area	:	A_e	= 1.25 cm^2
Window area	:	W_a	= 1.78 cm^2
Surface area of transformer	:	A_t	= 91.79 cm^2
Magnetic path length	:	MPL	= 9.22 cm
Core piece weight	:	W_{tfe}	= 30 g
Maximum winding height	:	H_{CF}	= 6.9 mm
Maximum winding breadth	:	B_{CF}	= 25.7 mm

5.4.5. THE PRIMARY WINDING

5.4.5.1. CALCULATING THE PRIMARY TURNS

Once the core material has been selected and the core size calculated the number of primary turns can be calculated using equation (5-28), adapted from [3]. In equation (5-28) the primary turns are related to the applied volt-seconds as follows.

$$N_p = \frac{V_{p(min)}\ t_{on} \times 10^4}{\Delta B\ A_c} \qquad (5\text{-}28)$$

where

N_p - primary turns

$V_{p(min)}$ - minimum primary voltage, V

t_{on} - pulse duration, s

ΔB - maximum flux density swing, T

A_c - minimum core cross-sectional area, cm^2

Note: If A_c is not quoted in the data sheets, A_e can be used.

Substituting into equation (5-28)

$$N_p = \frac{132 \times 4 \times 10^{-6} \times 10^4}{0.36 \times 1.25}$$

$$N_p = 11.73\ T$$

Selected N_p = 12 T.

Although the magnetising current can be neglected it should be verified, because at a higher operating frequency the primary inductance will be reduced, increasing the magnetising current.

With an inductance factor of A_L = 2 700 nH (Appendix J) the primary inductance L_p is determined using equation (5-29).

$$L_p = N^2 A_L \quad (H) \tag{5-29}$$

$$L_p = 388.8\ \mu H$$

The magnetising current for a steady state operation can therefore be obtained using equation (5-30), adapted from [2].

$$I_M = \frac{V_{p(max)}\ \delta_{Tmin}}{f_s\ L_p} \quad (A) \tag{5-30}$$

From [2] the minimum duty cycle δ_{Tmin} is calculated using equation (5-31).

$$\delta_{Tmin} = \frac{V_{o(+5min)} + V_F + V_{Ls}}{n_3\ V^*_{imax}} \tag{5-31}$$

Where

n_3 - turns ratio (main output versus primary)

$V_{o(+5min)}$ - minimum output voltage for +5 V winding, V

V_F - forward voltage drop of rectifier diode, V

V_{Ls} - voltage drop across secondary winding and choke, V

V^*_{imax} - effective maximum input voltage, V

The effective maximum input voltage V^*_{imax} is

$$V^*_{imax} = V_{imax} - V_{DS(on)} - V_{Lp} \quad (V) \tag{5-32}$$

Where

$V_{DS(on)}$ - "on" time period voltage, drain to source, V

V_{Lp} - voltage drop due to the primary winding, V

With

$V_{DS(on)}$ = 2 V (estimated) and

V_{Lp} = 2 V (estimated)

Substituting into (5-32)

$$V^*_{imax} = 336\ V$$

Referring to equation (5-31) with V_F = 0.8 V (estimated),

V_{Ls} = 0.5 V (estimated) and $n_3 = \frac{N_{s(3a)}}{N_p} = \frac{1}{6}$ or 0.167.

The minimum duty cycle δ_{Tmin} will therefore be

$$\delta_{Tmin} = \frac{4.5 + 0.8 + 0.5}{0.167 \times 336}$$

$$\delta_{Tmin} = 0.104$$

Therefore

$$I_M = \frac{170 \times 0.104}{100 \times 10^3 \times 388.8 \times 10^{-6}}$$

$$I_M = 0.45\ A\ (1.75\ A)$$

Note the increase in the magnetising current with a step change in load current (shown in brackets). The magnetising current is acceptable.

Taking the magnetising current into consideration, the maximum primary current will be from [2].

$$\begin{aligned} I_{p(max)} = {} & (I_{o(+5max)} + \frac{\Delta I_L}{2})\ n_{(3)} + \\ & (I_{o(+12max)} + \frac{\Delta I_L}{2})\ n_{(2)} + \\ & (I_{o(-5max)} + \frac{\Delta I_L}{2})\ n_{(3)} + \\ & (I_{o(-12max)} + \frac{\Delta I_L}{2})\ n_{(2)} + \\ & (I_{o(+15max)} + \frac{\Delta I_L}{2})\ n_{(1)} + I_M \quad (A) \end{aligned} \tag{5-33}$$

$$I_{p(max)} = 4.1\ A$$

The result compares well to the estimated figure in Section 5.1.

5.4.5.2. CURRENT DENSITY

From [7] the maximum current density for the core size will be

$$J = K_j \ (A_p)^y \quad (A/cm^2) \tag{5-34}$$

where

K_j = 665 (Appendix D) and

y = -0.11 (Appendix D)

$$J \approx 610 \ A/cm^2$$

5.4.5.3. PRIMARY WIRE SIZE

The bare wire area $A_{w(B)}$ for the primary is

$$A_{w(B)} = \frac{I_{p(max)}}{J} \quad (cm^2) \tag{5-35}$$

$$A_{w(B)} = 0.00672 \ cm^2$$

This corresponds to the AWG # 18 (Appendix C) with a wire diameter including insulation of d_w = 1.11 mm.

The maximum winding breadth for the ETD 39/20/13 bobbin is 25.7 mm. Since a grounded safety screen will be used (see Figure 5.10, page 100), the total creepage distance can be reduced to 6 mm. This leaves an actual winding breadth of

b_w = 25.7 mm - 6 mm or 19.7 mm. Using the AWG # 18, 17 turns will be required to fill one layer. Only 12 turns are necessary, resulting in an easy fit.

For the wire gauge selected the primary winding height H_p will be 1.11 mm, occupying approximately 16% of the total winding height H_{CF} (see Appendix E for definitions). Considering the amount of windings still to be included a further reduction in the primary winding height H_p will be considered.

Taking the skin and proximity effects into consideration, a multiple-wire technique is used, providing a higher resistance to the induction of eddy currents, because of the smaller diameter of each wire used.

Selecting 3 strands, the ideal wire diameter (per strand), including the insulation d_w, will be $\frac{19.7\ mm}{(3 \times 12)}$ or 0.55 mm.

From the wire table (Appendix C) the closest wire gauge will be the AWG # 25 with

$A_{w(B)}$ = 0.001624 cm^2

d_w = 0.51 mm

d_c = 0.45 mm

$\mu\Omega$/cm = 1 062

The 12 turns of 3 strands in parallel will now occupy

(12 × 3) × 0.51 mm or 18.36 mm (1 layer). This reduces the previously calculated primary winding height H_p by 9%, which is a considerable improvement.

Although the total bare wire area of the 3 strands only add up to 0.00487 cm^2 (3 × 0.001624 cm^2), which is less than the calculated value in equation (5-35), it will be acceptable, because the increase in wire resistance will be made up for by the reduction in the F_R ratio.

5.4.5.4. PRIMARY SKIN EFFECT

From [9] the optimum wire diameter will be found when the F_R ratio (the effective ac resistance of the wire to its DC resistance) is approximately equal to 1.5 ($F_R \approx 1.5$).

The optimum primary wire thickness for a single-layer at 100 kHz can be obtained from Figure G.1 (Appendix G) as 0.45 mm (d_c = 0.45 mm). Since the wire diameter calculated in Section 5.4.5.3 exactly matches this "optimum" no further recalculations will be necessary (F_R = 1.5).

5.4.5.5. PRIMARY COPPER LOSSES

Since the primary winding is wound directly around the centre post Figure 5.10 the actual turn length M_{lt} can be used instead of the MLT.

$$M_{lt} = \pi \times d \quad (cm) \tag{5-36}$$

$$M_{lt} = 5.34\ cm$$

Using equation (5-37) from [7] the DC resistance per strand can be calculated. The formula also includes the resistance correction factor ζ (zeta) to compensate for the increase in resistance at the higher operating temperature of 75 °C, which includes a temperature rise of 30 °C.

$$R_{DC} = M_{lt} \times N \times (\mu\Omega/cm) \times 10^{-6} \times \zeta \quad (\Omega) \tag{5-37}$$

$$R_{DC} = 0.08336\ \Omega$$

With 3 strands in parallel the total DC resistance will be $R_{DC(tot)} = 0.02779\ \Omega$.

At the operating frequency the working resistance R_{ac} will be greater than the DC resistance R_{DC} (due to the skin and proximity effects), by the F_R ratio.

Therefore

$$R_{ac(p)} = F_R \times R_{DC(tot)} \quad (\Omega) \tag{5-38}$$

$$R_{ac(p)} = 0.04168\ \Omega$$

The primary rms current $I_{p(rms)}$, which is responsible for the temperature rise is calculated using equation (5-39) from [2].

$$I_{p(rms)} = \acute{I}_{p(max)} \sqrt{2\ \delta_{Tmax}} \quad (A) \tag{5-39}$$

Where $\acute{I}_{p(max)}$ is calculated using equation (5-40), neglecting the ripple currents ΔI_L.

$$\begin{aligned} \acute{I}_{p(max)} = {} & I_{o(+5max)} \cdot n_{(3)} + I_{o(+12max)} \cdot n_{(2)} + \\ & I_{o(-5max)} \cdot n_{(3)} + I_{o(-12max)} \cdot n_{(2)} + \\ & I_{o(+15max)} \cdot n_{(1)} + I_M \quad (A) \end{aligned} \tag{5-40}$$

$$\acute{I}_{p(max)} = 3.69\ A$$

Substituting into (5-39)

$$I_{p(rms)} = 3.69 \sqrt{0.8}$$

$$I_{p(rms)} = 3.3\ A$$

The copper loss in the primary is

$$P_{cu(p)} = (I_{p(rms)})^2\ R_{ac(p)} \quad (W) \tag{5-41}$$

$$P_{cu(p)} = 0.454\ W$$

5.4.6. THE +5V MAIN OUTPUT WINDING

5.4.6.1. +5V MAIN OUTPUT TURNS

The required secondary output voltage $V_{s(3a)}$ (Figure 5.8, page 68) should be large enough to obtain the final desired

output voltage of 5 V. Equation (5-42) describes the required secondary output voltage from [9], based on an average duty cycle of 25%.

Selected V_F = 1 V.

$$V_{s(3a)} = 4\,(V_{o(+5)} + V_F) \quad (V) \tag{5-42}$$

$$V_{s(3a)} = 24\ V$$

The number of secondary turns $N_{s(3a)}$ required is simply calculated by using the transformer turns ratio.

$$N_{s(3a)} = \frac{N_p \times V_{s(3a)}}{V_{p(nom)}} \tag{5-43}$$

$$N_{s(3a)} = 1.86\ T$$

Selected $N_{s(3a)} = N_{s(3b)}$ = 2 T (centre-tapped).

5.4.6.2. +5V MAIN OUTPUT WIRE SIZE

The bare wire area $A_{w(B)}$ is

$$A_{w(B)} = \frac{I_{s3a(max)} \times 0.707}{J} \quad (cm^2) \tag{5-44}$$

where $I_{s3a(max)}$ is equal to the total current flowing through the winding.

Therefore

$$A_{w(B)} = \frac{30\ A \times 0.707}{610\ A/cm^2}$$

$$A_{w(B)} = 0.03477\ cm^2$$

This corresponds to the AWG # 11 with d_c = 2.31 mm (Appendix C).

The selected wire gauge will be impractical and it was decided to use a copper strip instead with approximately the same bare wire area. A copper strip with height h = 0.2 mm and breadth b = 19.7 mm (limited by the 6 mm creepage allowance) was selected.

The bare wire area is

$$A_{w(B)} = h \times b \quad (cm^2) \tag{5-45}$$

$$A_{w(B)} = 0.03940\ cm^2$$

which is more than adequate.

The copper strip specifications are therefore:

$A_{w(B)}$ = 0.03940 cm^2

h = 0.2 mm

$\mu\Omega$/cm = 43.76

To achieve minimum leakage inductance and a near-perfect

balance about the centre-tap the winding is wound bifilarly and is then seriesly connected. Care should be taken in the connection of the take-off windings to prevent any windings from cancelling each other.

With each turn representing 1 layer (4 layers in total), adding to this the required insulation layers between the copper strips, the total winding height $H_{s(2a \& 2b)}$ will amount to 2.28 mm or about 33% of the total winding height H_{CF}.

At this stage a total of 40% (7% + 33%) of the total winding height H_{CF} is used, leaving 60% for the auxiliary windings, protective screens and extra insulation layers, including the protective cover.

5.4.6.3. SKIN EFFECT

The optimum strip thickness h for an F_R ratio of 1.5 can be found using Figure G.2 in Appendix G. For 2 layers at an operating frequency of 100 kHz a strip of maximum height h = 0.25 mm can be used.

Since the selected height is less than "optimum" the F_R ratio will be smaller than 1.5. From Appendix G using Figure G.3 the new F_R ratio will be equal to 1.2 (F_R = 1.2).

5.4.6.4. +5V MAIN OUTPUT COPPER LOSSES

The DC resistance is calculated using the same equation as in Section 5.4.5.5, but only this time an empirically determined correction factor of a = 1.5 is included, thus providing the necessary compensation for the increasing MLT (see Figure 5.10, page 100).

Rewriting equation (5-37)

$$R_{DC} = a \times MLT \times N \times (\mu\Omega/cm) \times 10^{-6} \times \zeta \quad (\Omega) \qquad (5\text{-}46)$$

$$R_{DC} = 0.00111\ \Omega$$

The working resistance R_{ac} at the operating frequency is

$$R_{ac(s3a)} = F_R \times R_{DC} \qquad (5\text{-}47)$$

$$R_{ac(s3a)} = 0.00133\ \Omega$$

From [2] the secondary rms current $I_{s3a(rms)}$ is

$$I_{s3a(rms)} = I_{s3a(max)}\sqrt{0.25 + 0.75\ \delta_{Tmax}} \quad (A) \qquad (5\text{-}48)$$

$$I_{s3a(rms)} = 22.25\ A$$

The copper loss is

$$P_{cu(s3a)} = (I_{s3a(rms)})^2 \times R_{ac(s3a)} \quad (W) \qquad (5\text{-}49)$$

$$P_{cu(s3a)} = 0.658\ W$$

5.4.7. THE ±12V AUXILIARY OUTPUT WINDING

5.4.7.1. ±12V AUXILIARY OUTPUT TURNS

The required secondary output voltage $V_{s(2a)}$ is given by

Note: $V_F = 1$ V

$$V_{s(2a)} = 4\,(V_{o(+12)} + V_F) \quad (V) \tag{5-50}$$

$$V_{s(2a)} = 52\ V$$

This averages out to about 13 V at an average duty cycle of 25%. Subtracting the voltage drop due to the rectifier diode and choke leaves $V_o = 12$ V.

The number of turns for $N_{s(2a)}$ are

$$N_{s(2a)} = \frac{N_p \times V_{s(2a)}}{V_{p(nom)}} \tag{5-51}$$

$$N_{s(2a)} = 4.03\ T$$

Selected $N_{s(2a)} = N_{s(2b)} = 4$ T.

Referring to Figure 5.8, page 68

$$\acute{N}_{s(2a)} = \acute{N}_{s(2b)} = N_{s(2a)} - N_{s(3a)} = 4 - 2 = 2\ T.$$

5.4.7.2. ±12V AUXILIARY OUTPUT WIRE SIZE

The bare wire area $A_{w(B)}$ is

$$A_{w(B)} = \frac{I_{s2a(max)} \times 0.707}{J} \quad (cm^2) \qquad (5\text{-}52)$$

$$A_{w(B)} = \frac{9\ A \times 0.707}{610\ A/cm^2}$$

$$A_{w(B)} = 0.01043\ cm^2$$

To obtain the necessary wire area it was decided to use 4 strands. With the objective of limiting the winding height $\acute{H}_{s(2a\ \&\ 2b)}$ the windings $\acute{N}_{s(2a)}$ and $\acute{N}_{s(2b)}$ will be placed side by side to make up one complete layer. The ideal wire diameter including insulation d_w can be obtained as follows.

Knowing that each winding ($\acute{N}_{s(2a)}$ and $\acute{N}_{s(2b)}$) consists of 2 turns, or 4 turns in total, and each turn is made up of 4 strands, gives an equivalent of (4 × 4) or 16 turns. Adding to this another 16 turns for practical purposes (pick-up and take-off windings) the total number of turns to be considered are (2 × 16) 32 turns, resulting in a maximum wire diameter d_w of $\frac{19.7\ mm}{32}$ or 0.62 mm.

From Appendix C the AWG # 24 is selected with the following specifications:

$A_{w(B)}$ = 0.002047 cm^2

d_w = 0.57 mm

d_c = 0.51 mm

$\mu\Omega/cm$ = 842

With a winding height of $\acute{H}_{s(2a\ \&\ 2b)}$ = 0.57 mm the winding would occupy another 8% of the total available winding height H_{CF}.

5.4.7.3. SKIN EFFECT

From Figure H.1 (Appendix H) the optimum wire diameter d_w for a single layer will be 0.45 mm (d_w = 0.45 mm). The selected wire gauge is clearly above the "optimum", resulting in an F_R ratio above 1.5.

Using the method in [11] the new F_R ratio will be F_R = 1.88.

5.4.7.4. ±12V AUXILIARY OUTPUT COPPER LOSSES

From [7] the DC resistance per strand is

$$R_{DC} = MLT \times N \times (\mu\Omega/cm) \times 10^{-6} \times \zeta \quad (\Omega) \qquad (5\text{-}53)$$

$$R_{DC} = 0.01423\ \Omega$$

For the 4 strands in parallel $R_{DC(tot)}$ will be

$$R_{DC(tot)} = 0.00356\ \Omega$$

The working resistance R_{ac} at the operating frequency is

$$R_{ac(s2a)} = F_R \times R_{DC(tot)} \quad (\Omega) \tag{5-54}$$

$$R_{ac(s2a)} = 0.00669\ \Omega$$

The secondary rms current for the winding is

$$I_{s2a(rms)} = I_{s2a(max)}\sqrt{0.25 + 0.75\ \delta_{Tmax}} \quad (A) \tag{5-55}$$

$$I_{s2a(rms)} = 6.67\ A$$

The copper loss is

$$P_{cu(s2a)} = (I_{s2a(rms)})^2 \times R_{ac(s2a)} \quad (W) \tag{5-56}$$

$$P_{cu(s2a)} = 0.298\ W$$

5.4.8. THE +15V AUXILIARY OUTPUT WINDING

5.4.8.1. +15V AUXILIARY OUTPUT TURNS

The required secondary voltage $V_{s(1a)}$ is

Note: $V_F = 1$ V

$$V_{s(1a)} = 4\,(V_{o(+15)} + V_F) \quad (V) \tag{5-57}$$

$$V_{s(1a)} = 64\ V$$

The number of turns required are

$$N_{s(1a)} = \frac{N_p \times V_{s(1a)}}{V_{p(nom)}} \qquad (5\text{-}58)$$

$$N_{s(1a)} = 4.95\ T$$

Selected $N_{s(1a)} = N_{s(1b)} = 5$ T (centre-tapped).

5.4.8.2. +15V AUXILIARY OUTPUT WIRE SIZE

The bare wire area $A_{w(B)}$ is

$$A_{w(B)} = \frac{I_{s1a(max)} \times 0.707}{J} \quad (cm^2) \qquad (5\text{-}59)$$

$$A_{w(B)} = 0.00174\ cm^2$$

Selected 4 strands. The winding bifilarly wound and then seriesly connected, amounts to the following number of turns. Each winding-half is made up of 5 turns, 10 in total, with each turn made up out of 4 strands, 40 turns in total. Adding to this another (2 × 4) 8 turns (for the pick-up and take-off windings), amounts to 48 turns. Therefore the maximum possible wire diameter d_w (including the insulation thickness), to fill one layer will be $\frac{19.7\ mm}{48}$ or 0.41 mm.

The AWG # 27 from Appendix C was selected with the following specifications:

$A_{w(B)}$ = 0.001021 cm^2

d_w = 0.41 mm

d_c = 0.36 mm

$\mu\Omega$/cm = 1 689

The total wire area should be verified. With 4 strands the total bare wire area will be (4 × 0.001021 cm^2) or 0.004084 cm^2, which is more than adequate.

With a winding height $H_{s(1a\ \&\ 1b)}$ of 0.41 mm, another 6% of the total winding height H_{CF} will be occupied by the winding. Therefore 54% (48% + 6%) of the total winding height H_{CF} will be occupied by the different windings. The remaining 46% will be used up by the protective screens and extra insulation layers thus obtaining an easy fit (see Figure 5.10, page 100).

5.4.8.3. ***SKIN EFFECT***

From Figure G.1 (Appendix G) the optimum wire diameter for a single layer at the operating frequency will be 0.45 mm for an F_R ratio of 1.5. Since the selected wire diameter is smaller than the "optimum" the F_R ratio will have to be adjusted to reflect this change.

From Figure G.3 (Appendix G) the new F_R ratio will be

$$F_R = 1.2$$

5.4.8.4. +15V AUXILIARY OUTPUT COPPER LOSSES

For this winding the actual turn length M_{lt} can be used.

$$M_{lt} = \pi \times d \quad (cm) \tag{5-60}$$

$$M_{lt} = 5.65\ cm$$

From equation (5-37) the DC resistance per strand is

$$R_{DC} = M_{lt} \times N \times (\mu\Omega/cm) \times 10^{-6} \times \zeta \quad (\Omega) \tag{5-61}$$

$$R_{DC} = 0.05752\ \Omega$$

For 4 strands in parallel $R_{DC(tot)}$ is

$$R_{DC(tot)} = 0.01438\ \Omega$$

The working resistance R_{ac} at the operating frequency is

$$R_{ac(s1a)} = F_R \times R_{DC(tot)} \quad (\Omega) \tag{5-62}$$

$$R_{ac(s1a)} = 0.01726\ \Omega$$

From equation (5-48) the secondary rms current is

$$I_{s1a(rms)} = I_{s1a(max)}\sqrt{0.25 + 0.75\ \delta_{Tmax}} \quad (A) \tag{5-63}$$

$$I_{s1a(rms)} = 1.11\ A$$

The copper loss is

$$P_{cu(s1a)} = (I_{s1a(rms)})^2 \times R_{ac(s1a)} \quad (W) \qquad (5\text{-}64)$$

$$P_{cu(s1a)} = 21.27 \times 10^{-3}\ W$$

or

$$P_{cu(s1a)} = 21.27\ mW$$

5.4.9. CORE LOSSES

From Figure F.1 (Appendix F) the core losses for the N27 ferrite material, expressed in mW/g at an operating flux density B_m of 0.18 T, will be

$$mW/g = 249.23$$

With a total core weight of (2 × 30 g) or 60 g the total core loss P_c will be

$$P_c = mW/g \times W_{tfe} \quad (W) \qquad (5\text{-}65)$$

$$P_c = 14.95\ W$$

From the above result it is apparent that the core losses have risen more than proportionally with respect to the frequency, resulting in an unacceptable temperature rise.

To reduce the core losses to an acceptable level and hence the temperature rise a small air gap will be introduced.

The air gap will reduce the core losses to a more acceptable level, but it also entails some disadvantages, one of which is increasing the magnetising current and hence the primary current, due to the reduction in primary inductance.

It also has the advantage of magnetising the core quicker, reducing the switching time and consequently the switching losses. In this instance the advantages will outweigh the disadvantages as long as the increase in magnetising current is kept within reasonable limits.

The effect of the inclusion of an air gap will be analyzed in the following paragraphs.

From [12] the effective permeability μ_e, can be approximated for an air gap of 0.05 mm by using equation (5-66).

$$\mu_e = \frac{l_e \times \mu_i}{l_e + l_g \mu_i} \qquad (5\text{-}66)$$

$$\mu_e \approx 960$$

The resulting change in inductance factor follows from [12].

$$A_L' = \frac{0.4\ \pi\ \mu_e}{\sum \frac{l}{A}} \quad (nH) \qquad (5\text{-}67)$$

$$\acute{A}_L = 1630\ nH$$

Hence

$$\acute{L}_p = N^2\ \acute{A}_L \quad (H) \tag{5-68}$$

$$\acute{L}_p = 234{,}7\ \mu H$$

The new magnetisation current $\acute{I}_M$ is calculated using equation (5-30).

$$\acute{I}_M = \frac{V_{p(max)}\ \delta_{Tmin}}{f_s\ L_p} \quad (A)$$

$$\acute{I}_M = 0.75\ A$$

The increase in $I_{p(max)}$ and $I_{p(rms)}$ will only amount to about 8%, due to the increase in magnetisation current, which is negligible.

Using the equation from [2] the core loss including the air gap will be

$$\acute{P}_c = P_c\ \frac{\mu_e}{\mu_i} \quad (W) \tag{5-69}$$

$$\acute{P}_c = 7.18\ W$$

All that remains now is to determine the resulting temperature rise.

5.4.10. SUMMARISING THE DIFFERENT LOSSES

$$
\begin{aligned}
& P_{cu(p)} = 0.454\ W \\
& P_{cu(s3a)} = 0.658\ W \\
& P_{cu(s2a)} = 0.298\ W \\
+\ & P_{cu(s1a)} = 0.021\ W \\
\hline
& P_{cu(tot)} = 1.431\ W \\
+\ & \acute{P}_c = 7.176\ W \\
\hline
& P_{\Sigma} = 8.611\ W
\end{aligned}
$$

5.4.11. TEMPERATURE RISE

From [7] the average power dissipated per unit area ψ is

$$\psi = \frac{P_{\Sigma}}{A_t} \quad (W/cm^2) \tag{5-70}$$

where

$$P_{\Sigma} = P_{cu(tot)} + \acute{P}_c \quad (W) \tag{5-71}$$

$$P_{\Sigma} = 8.611\ W$$

Substituting into (5-70)

$$\psi = \frac{8.611\ W}{91.79\ cm^2}$$

$$\psi = 0.0938\ W/cm^2$$

From [7] the calculated ψ of 0.0938 W/cm^2 will result in an estimated temperature rise ΔT of 53 °C at an ambient temperature of 45 °C. This would result in an estimated hot spot temperature of 98 °C under worst case conditions.

5.4.12. POWER TRANSFORMER EFFICIENCY

The power transformer efficiency is

$$\eta = \frac{P_o}{P_o + P_\Sigma} \times 100 \quad (\%) \qquad (5\text{-}72)$$

$$\eta = 97\%$$

5.4.13. TRANSFORMER WINDING LAYOUT

The construction of the power transformer windings is shown in Figure 5.10 on page 100.

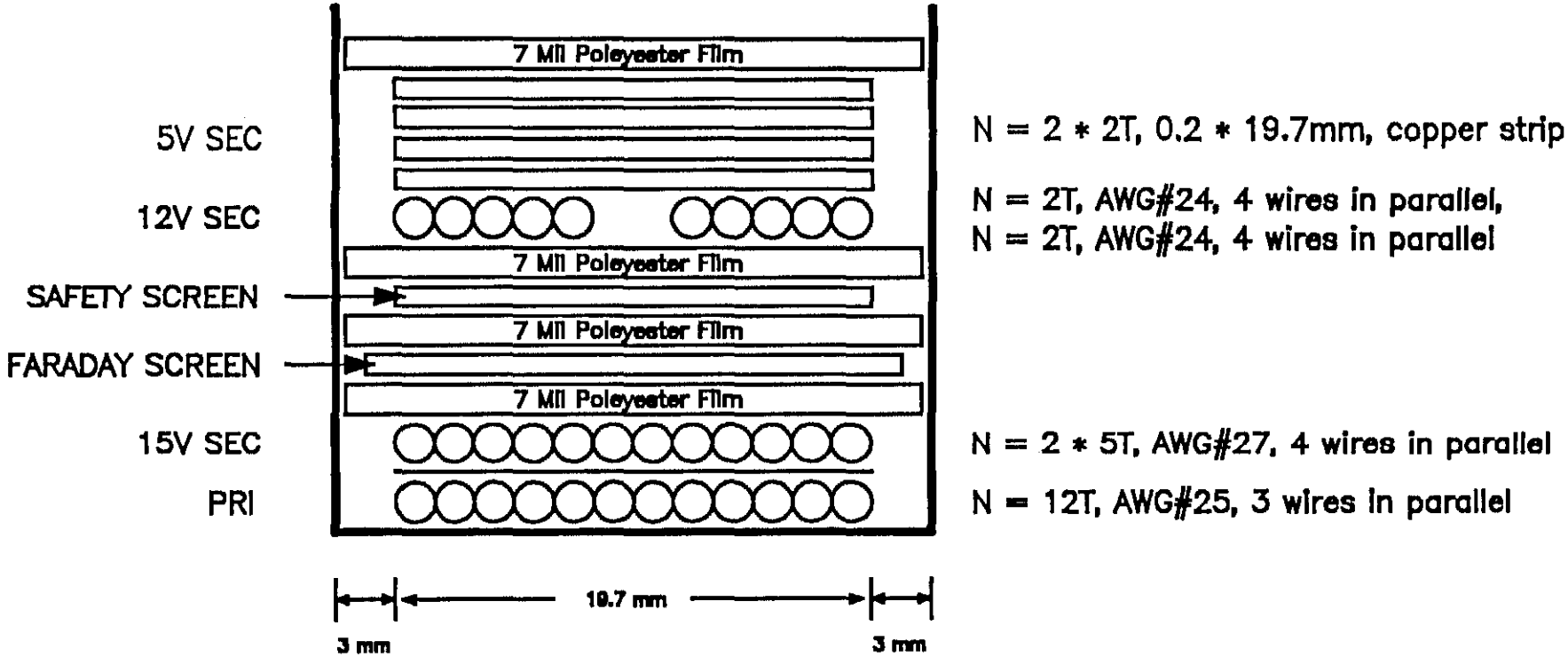

Figure 5.10 The construction of the power transformer windings.

For VDE requirements a polyester film laminate Code A03, rated at 155 °C, was used. All magnet wires used are P.U. (also rated at 155 °C).

5.4.14. RC SNUBBER

To limit the spikes caused by the power transformer's leakage inductance to a safe value a RC snubber is placed across the primary winding.

From [2] the value for the series capacitor C_{25} is calculated using equation (5-73).

$$C_{25} \geq L_s \frac{(I_{p(max)})^2}{(\Delta V)^2} \quad (F) \qquad (5\text{-}73)$$

Where

L_s - secondary leakage inductance, H

ΔV - permissible overvoltage, V

With the secondary leakage inductance measured at 0.9 μH and the permissible overvoltage ΔV not to exceed 150 V (assumed), substituting into equation (5-73) the series capacitor will be

$$C_{25} \geq 0.9 \times 10^{-6} \frac{(4.1\ A)^2}{(150\ V)^2}$$

$$C_{25} \geq 672.40\ pF$$

From [2] the series resistor R_{43} is calculated using equation (5-74)

$$R_{43} \leq \frac{t_f}{C_{25}} \quad (\Omega) \qquad (5\text{-}74)$$

with the fall time t_f estimated at 0.2 μs

$$R_{43} \leq \frac{0.2 \times 10^{-6}}{672.40 \times 10^{-12}}$$

$$R_{43} \leq 297.44\ \Omega$$

From [2] the power dissipated in R_{43} will be

$$P_{R43} = \frac{1}{2} C_{25} V_{imax}^2 f_s \quad (W) \qquad (5\text{-}75)$$

$$P_{R43} = 0.97\ W$$

It should be noted that the above values obtained are only good estimates and that the final values should be experimentally adjusted, once construction is completed.

The final values are:

C_{25} = 561 pF/500 V

R_{43} = 260 Ω/5 W.

5.5. OVERCURRENT LIMITING

To protect the SMPS against overloads and possible short circuits a pulse-by-pulse overcurrent limiting technique is used. The circuit is shown in Figure 5.11.

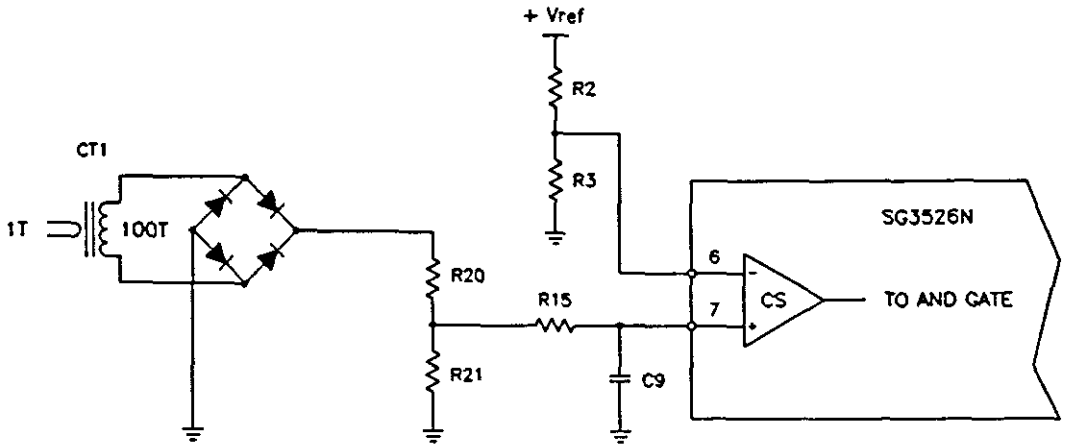

Figure 5.11 The pulse-by-pulse overcurrent limiting circuit.

With the current transformer CT1 in series with the primary switching devices the drain current (from here on referred to as forward current) in the switching devices will be monitored in real time. A voltage proportional to the forward current will be developed across the load.

The load consists of the voltage divider (R_{20} and R_{21}), followed by a RC circuit. The RC circuit (R_{15} and C_9) introduces a time delay of approximately 1μs, preventing operation of the circuit by unavoidable spikes of very short duration.

The current sensing operational amplifier of the controller acts as a comparator and is triggered once the forward current has reached 30% above $I_{p(max)}$, terminating any further increase in forward current.

The main advantage of the pulse-by-pulse overcurrent limiting technique is the protection of the primary switching devices (MOSFETS).

The technique also provides constant power limiting.

5.5.1. THE DESIGN OF THE CURRENT TRANSFORMER

The design of the current transformer CT1 is based on the method as described in [3].

5.5.1.1. PRIMARY AMPERE-TURNS

The maximum allowable forward current in the switching device is preset to be no more than 30% above $I_{p(max)}$. This results in a maximum forward current of 5.33 A, which is within the switching device's capability.

The primary winding is set to 1 turn (for practical reasons), obtaining a magnetising force of 5.33 ampere-turns.

5.5.1.2. SECONDARY AMPERE-TURNS

The secondary winding with 100 turns of AWG # 36 will need to conduct 53.3 mA to reset the core.

5.5.1.3. REQUIRED SECONDARY VOLTAGE

The secondary voltage is predetermined at 3.3 V, consisting of 0.4 V for each diode drop and 2.5 V for the current analog signal across the load.

With 3.3 V at the secondary, transforming V_s to the primary would result in a voltage drop of 33 mV across the primary winding. Hence primary insertion loss will be minimal.

5.5.1.4. VERIFYING THE MAGNETIZING CURRENT

To keep the magnetizing current low a core material with a high permeability was chosen. A ferrite ring core of the 3E2 material, size (9 × 6 × 5), from Philips, was selected.

The 100 turns of AWG # 36 will fill 1 layer providing a good high-frequency performance. Since the magnetizing current is subtracted from the current to be measured, it should be verified.

With an A_L value of 1 673 nH practically determined the inductance for the secondary winding is calculated.

$$L_s = N^2 A_L \quad (H) \tag{5-76}$$

$$L_s = 16.73\ mH$$

From [3] the slope of the magnetizing current $\frac{dI}{dt}$ will be

$$\left|\frac{dI}{dt}\right| = \frac{V_s}{L_s} \quad (A/s) \tag{5-77}$$

$$\left|\frac{dI}{dt}\right| = 197.3\ A/s$$

This will result in a magnetizing current I_{mag} of 0.789 mA at the end of the 4 μs pulse. Transforming I_{mag} to the primary, results in 78.9 mA, which is minimal compared to the measured current of 5.33 A.

The magnetizing current of 0.789 mA or 1.5% of the total secondary current is well within the 10% design restriction. Therefore the effect of the magnetizing current will be considered to be negligible and the selected core is suitable for the application.

The load resistor will be

$$R_L = \frac{V_o}{I_s} \quad (\Omega) \tag{5-78}$$

$$R_L = 46.9\ \Omega$$

To compensate for the loss in amplitude due to the voltage drop in the windings and diodes the load resistor R_L has been practically adjusted to 110 Ω.

5.5.1.5. FLUX DENSITY

Although the current transformer will not saturate due to the series coupling capacitor C_{24} that will prevent any DC component from developing the maximum flux density excursion should be verified.

From [3] the mean flux density excursion during each pulse will be

$$B = \frac{V_m \, t_{on} \times 10^4}{N_s \, A_e} \quad (T) \qquad (5\text{-}79)$$

where

B - flux density, T

V_m - mean secondary voltage, V

A_e - effective core cross-sectional area, cm^2

$$B = 13.1 \; mT$$

With a maximum flux density excursion of 13.1 mT the core losses will be negligible.

This completes the design for the current transformer.

The values for the associated components can be found in the component list (Appendix B).

6. THE DESIGN OF THE OUTPUT STAGE

This Chapter presents the design and selection of the output rectifier diodes, filter chokes and filter capacitors.

6.1. THE DESIGN OF THE OUTPUT RECTIFIER DIODES

6.1.1. THE DESIGN OF THE MAIN OR +5V OUTPUT RECTIFIER DIODE

The simplified main or +5 volt output section is shown in Figure 6.1.

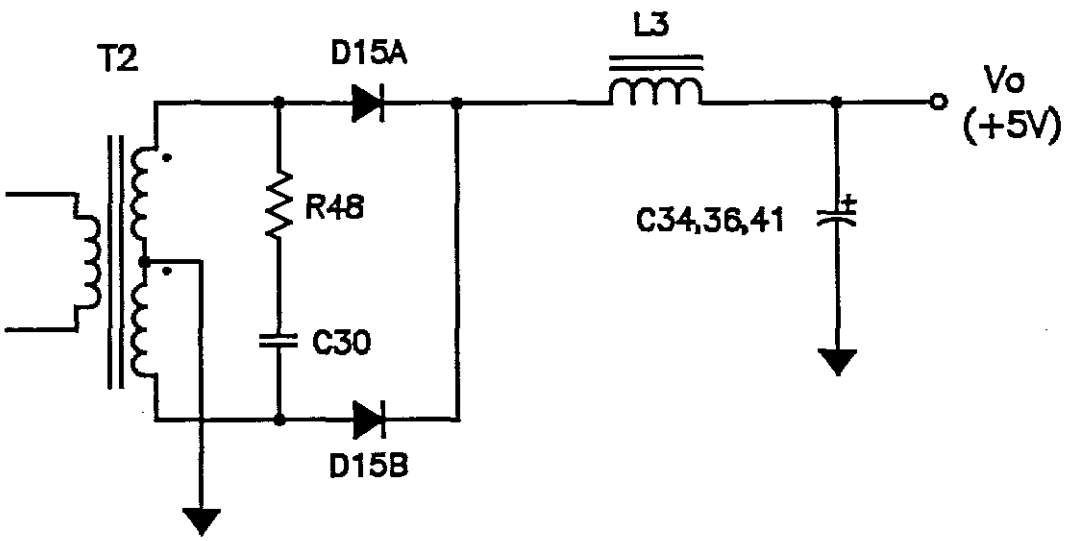

Figure 6.1 The simplified main or +5 volt output section for the half-bridge push-pull converter, *including the RC snubber network.*

It is of great importance to select a high efficiency diode for $D_{15a\&b}$, the main reason being to keep the diode losses to a minimum.

The selected diode should therefore have the following minimum requirements:

1) a low forward voltage drop and
2) a fast recovery time.

6.1.1.1. MAXIMUM REVERSE VOLTAGE

From [2] the maximum reverse voltage will be

$$V_{Rmax} = \frac{V_o^*}{\delta_{Tmin}} + V_F \frac{(1 - \delta_{Tmin})}{\delta_{Tmin}} \quad (V) \qquad (6\text{-}1)$$

where

$$V_o^* = V_{omin} + V_F + V_{Ls} \quad (V) \qquad (6\text{-}2)$$

with V_F = 0.9 V and V_{Ls} = 0.5 V estimated.

$$V_o^* = 4.5\ V + 0.9\ V + 0.5\ V$$

$$V_o^* = 5.9\ V$$

Substituting into equation (6-1)

$$V_{Rmax} \approx 65\ V$$

6.1.1.2. MAXIMUM PERMISSIBLE REPETITIVE CURRENT

From [2] the maximum repetitive current will be

$$I_{FM(rep)} = 2\ I_o \quad (A) \tag{6-3}$$

$$I_{FM(rep)} = 40\ A$$

6.1.1.3. AVERAGE FORWARD CURRENT

With one diode always acting as a flywheel when the other one turns off as illustrated in Figure 6.2 the average forward current $I_{FM(ave)}$ can be calculated as follows:

From [6] the average forward current rating for each output diode will be

$$I_{FM(ave)} = I_o \frac{T_2}{T_1} \quad (A) \tag{6-4}$$

$$I_{FM(ave)} = 8\ A$$

The current during flywheel or dead time will be

$$I_{FDM} = I_o \frac{T_3}{T_1} \quad (A) \tag{6-5}$$

$$I_{FDM} = 2\ A$$

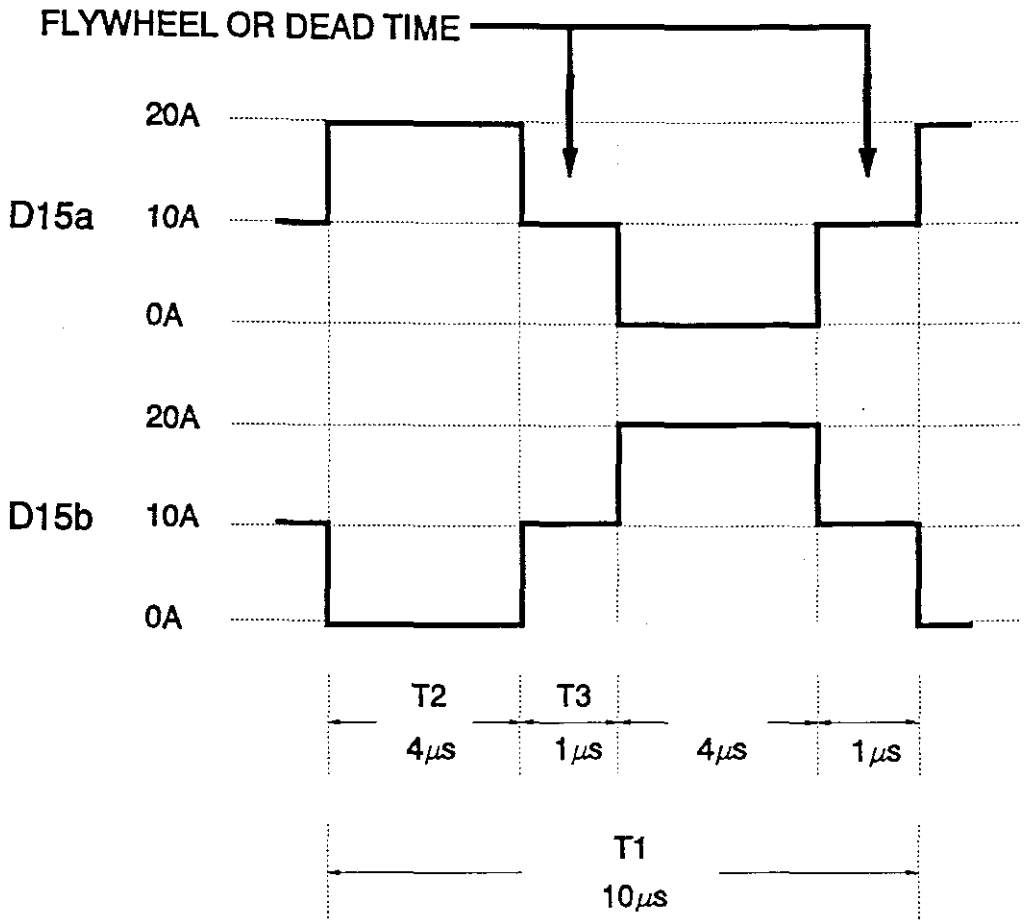

Figure 6.2 The current waveform in the output diodes.

Total average forward current

$$I_{FM(tot)} = I_{FM(ave)} + I_{FDM} \quad (A) \qquad (6\text{-}6)$$

$$I_{FM(tot)} = 10\ A$$

6.1.1.4. DIODE CHOICE

The diode most suitable for this application will be a schottky barrier diode, with its low forward voltage drop and very fast recovery time.

Selected the double diode ESAC87-009 from Fuji Electric.

6.1.1.5. DIODE LOSSES

Because of the relatively high leakage current present, the schottky diode will be more susceptible to thermal runaway. Therefore sufficient heatsinking should be provided.

The total diode loss for the double diode will consist of the maximum conduction loss P_{DC} and the reverse loss P_{DR} due to the leakage current.

Therefore the conduction loss P_{DC} will be

$$P_{DC} = I_o \, V_F \quad (W) \tag{6-7}$$

where V_F = 0.9 V (estimated)

$$P_{DC} = 18 \; W$$

and

$$P_{DR} = V_R \, I_{RM} \, \delta_{Tmax} \quad (W) \tag{6-8}$$

$$P_{DR} = 0.26 \; W$$

Total diode loss

$$P_{D(tot)} = P_{DC} + P_{DR} \quad (W) \tag{6-9}$$

$$P_{D(tot)} = 18.26\ W$$

Recommended heatsink

$$R_{thca} \leq \frac{\theta_{jmax} - \theta_{amax}}{P_D} - R_{thjc} \quad (°C/W) \tag{6-10}$$

$$R_{thca} \leq 3.18\ °C/W$$

Since R_{thjc} was not given in the data sheet, it was assumed.

The SK104 ST3 (50.8 mm) heatsink with 9 °C/W from the Fisher Company was selected. Assuming that forced air cooling is used, the heatsink will reduce to 9 °C/W × 0.14 or 1.26 °C/W, which is more than adequate.

6.1.1.6. RC SNUBBER NETWORK

The components for the RC snubber network are calculated according to [2]. Since various parameters are not known and are assumed, the answers obtained are very good estimates only and therefore experimentally adjusted once the prototype has been completed.

The reverse recovery charge

$$Q_{rr} = C_j\ V_{Rmax} \quad (As) \tag{6-11}$$

$$Q_{rr} = 150 \times 10^{-12}\ F \times 65\ V$$

$$Q_{rr} = 9.75 \times 10^{-9}\ As$$

The maximum reverse current

$$I_{RM} = \frac{2\ Q_{rr}}{t_{rr}} \quad (A) \tag{6-12}$$

$$I_{RM} = \frac{2 \times 9.75 \times 10^{-9}\ As}{30 \times 10^{-9}\ s}$$

$$I_{RM} = 0.65\ A$$

The series capacitor C_{30}

$$C_{30} \geq \frac{L_s\ I_{RM}^2}{V_{Rmax}^2} \quad (F) \tag{6-13}$$

$$C_{30} \geq \frac{15 \times 10^{-6}\ H \times (0.65\ A)^2}{(65\ V)^2}$$

$$C_{30} \geq 1.5\ nF$$

The series resistor R_{48}

$$R_{48} \leq \frac{V_{Rmax}}{I_{RM}} \quad (\Omega) \tag{6-14}$$

$$R_{48} \leq \frac{65\ V}{0.65\ A}$$

$$R_{48} \leq 100\ \Omega$$

The above calculated values were experimentally adjusted to R_{48} = 10 Ω/0.5 W and C_{30} = 1 nF/50 V.

The power dissipated in R_{48} will be

$$P_{R48} = f_s \, C_{30} \, V_{Rmax}^2 \quad (W) \qquad (6\text{-}15)$$

$$P_{R48} = 0.423 \; W$$

$$P_{R48} \approx 0.5 \; W$$

6.1.2. THE DESIGN OF THE AUXILIARY OUTPUT RECTIFIER DIODES

Although only the main or +5 volt output diode was calculated in detail in this section, the output diodes for the +12V, -12V, -5V and +15V auxiliary outputs are calculated, using exactly the same formulae. The different output diodes selected are briefly summarized below.

The +12V auxiliary output:

ESAC92-02, double diode, fast recovery.

The -12V auxiliary output:

1N4936, single diode, fast recovery.

The -5V auxiliary output:

1N5819, single diode, schottky.

The +15V auxiliary output:

UF3007, single diode, superfast recovery.

6.2. THE DESIGN OF THE OUTPUT FILTER CHOKES

6.2.1. THE DESIGN OF THE +5V OUTPUT FILTER CHOKE

6.2.1.1. REQUIRED INDUCTANCE

From [2] the minimum choke inductance is calculated using equation (6-16)

$$L_3 \geq \frac{V_o^*(1 - 2\delta_{Tmin})}{\Delta I_L \, 2 \, f_s} \quad (H) \tag{6-16}$$

where

$$V_o^* = V_{omax} + V_F + V_L \quad (V) \tag{6-17}$$

To obtain a more practical result V_o^* is used instead of the output voltage V_o, with V_{omax} = 5.5 V, V_F and V_L estimated at 0.9 V and 0.2 V respectively.

V_o^* will be

$$V_o^* = 5.5 \; V + 0.9 \; V + 0.2 \; V$$

$$V_o^* = 6.6 \; V$$

To limit the peak choke current and the output ripple current, the ripple current ΔI_L is selected not larger than 25% of the maximum output current I_{omax}.

Therefore ΔI_L will be

$$\Delta I_L = 0.25\ I_{omax} \quad (A) \tag{6-18}$$

$$\Delta I_L = 5\ A$$

Substituting into equation (6-16)

$$L_3 \geq \frac{6.6(1 - 2 \times 0.104)}{5 \times 2 \times 100 \times 10^3}$$

$$L_3 \geq 5.23\ \mu H$$

To keep the transient recovery time t_{tr} reasonable the final selection of the inductance value L_3 should not be too large.

From [2] the maximum value of the inductance is calculated using equation (6-20).

A reasonable t_{tr} will be

$$t_{tr} \approx (5 - 20)\frac{T}{2} \quad (s) \tag{6-19}$$

The divide by two is due to the doubling in frequency of the output section.

Therefore

$$t_{tr} \approx 25 - 100\ \mu s$$

Selected t_{tr} = 50 μs (a good average).

$$L_3 \leq \frac{V_o^*}{I_{o(step)}} t_{tr} \left(\frac{\delta_{Tmax}}{\delta_{T1}} - 1\right) \quad (H) \tag{6-20}$$

where $I_{o(step)}$ is the maximum possible step change in load current, selected as 50% of I_{omax} or 10 A.

δ_{T1} is estimated as 0.12 and represents the assumed duty cycle where the possible step in load current would occur. V_o^* is calculated using equation (6-21) and should not be confused with the previous V_o^* calculated in equation (6-17).

$$V_o^* = V_o + V_F + V_L \quad (V) \tag{6-21}$$

$$V_o^* = 5\ V + 0.9\ V + 0.2\ V$$

$$V_o^* = 6.1\ V$$

Substituting into equation (6-20)

$$L_3 \leq \frac{6.1}{10} 50 \times 10^{-6} \left(\frac{0.4}{0.12} - 1\right)$$

$$L_3 \leq 71.17\ \mu H$$

The required inductance range will therefore be

$$5.23\ \mu H \leq L_3 \leq 71.17\ \mu H$$

6.2.1.2. SELECTING THE APPROPRIATE INDUCTANCE VALUE

Taking into consideration the availability of core materials and sizes an inductance value of $L_3 = 5\ \mu H$ was chosen.

6.2.1.3. DETERMINING THE CORE SIZE AND MATERIAL

Having selected the inductance value, all that remains now is to select the core material and size. The procedure is based on the method as described in [7].

6.2.1.3.1. CHOKE MEAN CURRENT

To obtain the maximum choke current the $\frac{\Delta I_L}{2}$ is added to the mean choke current I_{omax}.

$$I_{Lmax} = I_{omax} + \frac{\Delta I_L}{2} \quad (A) \tag{6-22}$$

$$I_{Lmax} = 22.5\ A$$

6.2.1.3.2. CHOKE ENERGY-HANDLING CAPABILITY

From [7] the energy-handling capability will be

$$E = \frac{L_3\ I_{Lmax}^2}{2} \quad (W\ s) \tag{6-23}$$

$$E = 1.27 \times 10^{-3}\ W\,s$$

6.2.1.3.3. REQUIRED AREA PRODUCT

The area product A_p from [7] will be

$$A_p = \left(\frac{2\ E \times 10^4}{B_m\ K_u\ K_j}\right)^{1.14} \quad (cm^4) \qquad (6\text{-}24)$$

To keep the core losses to a minimum the maximum flux density B_m is selected as 0.15 T

with

$$K_u = 0.4$$

$$K_j = 654$$

Substituting into equation (6-24)

$$A_p = \left(\frac{2 \times 1.27 \times 10^{-3} \times 10^4}{0.15 \times 0.4 \times 654}\right)^{1.14}$$

$$A_p = 0.609\ cm^4$$

6.2.1.3.4. SELECTING THE APPROPRIATE CORE

An iron powder toroidal core T90 mix #6 from Micrometals was selected.

The following specifications apply:

A_p = 0.65 cm^4

MLT = 3.36 cm

A_c = 0.422 cm^2

W_a = 1.539 cm^2

A_t = 23.7 cm^2

MPL = 5.8 cm

W_{tfe} = 19 g

6.2.1.3.5. CURRENT DENSITY

From [7] the current density J for the selected core will be

$$J = K_j A_p^{-0.12} \quad (A/cm^2) \tag{6-25}$$

$$J = (654)(0.65)^{-0.12}$$

$$J \approx 689\ A/cm^2$$

6.2.1.3.6. BARE WIRE AREA

With a current density of J = 689 A/cm^2 the bare wire area will be

$$A_{w(B)} = \frac{I_{Lmax}}{J} \quad (cm^2) \tag{6-26}$$

$$A_{w(B)} = 0.03266\ cm^2$$

6.2.1.3.7. SELECTING THE APPROPRIATE WIRE SIZE

Although the AWG # 12 (Appendix C) could be used for this application, it would result in winding problems and a poor packing factor (especially with the small core size selected).

To reduce the skin effect two strands of AWG # 15 will be used with the following specifications:

$A_{w(B)}$ = 0.016504 cm^2

d_w = 1.56 mm

d_c = 1.45 mm

$\mu\Omega/cm^2$ = 104

6.2.1.3.8. EFFECTIVE WINDOW AREA

From [7] the effective window area will be

$$W_{ae} = W_a S_3 \quad (cm^2) \tag{6-27}$$

where S_3 is the ratio of usable window area to window area, selected as 0.75.

$$W_{ae} = 1.539\ cm^2 \times 0.75$$

$$W_{ae} = 1.15\ cm^2$$

6.2.1.3.9. NUMBER OF TURNS REQUIRED

The number of turns required will be

$$N = \sqrt{\frac{L_3}{A_L}} \qquad (6\text{-}28)$$

with an inductance factor of A_L = 69 nH (from data sheet)

$$N = 8.5\ T$$

Selected N = 9 T, obtaining an easy fit.

6.2.1.3.10. REQUIRED CORE PERMEABILITY

From [7] the required core permeability will be

$$\mu_r = \frac{L_3 \times MPL \times 10^8}{0.4 \times \pi \times N^2 \times A_c} \qquad (6\text{-}29)$$

$$\mu_r = 67.5$$

$$\mu_r \approx 68$$

With the selected core permeability (μ = 75) larger than calculated, the selected core should be more than adequate for the application.

6.2.1.3.11. WINDING RESISTANCE

Using the equation from [7] the winding resistance per strand will be

$$R_{DC} = MLT \times N \times (\mu\Omega/cm) \times \zeta \quad (\Omega) \tag{6-30}$$

$$R_{DC} = 0.00359\ \Omega$$

The total resistance for the 2 strands in parallel are

$$R_{DC(tot)} = \frac{0.00359\ \Omega}{2}$$

$$R_{DC(tot)} = 0.00179\ \Omega$$

6.2.1.3.12. COPPER LOSSES

$$P_{cu} = I_{Lmax}^2 \times R_{DC(tot)} \quad (W) \tag{6-31}$$

$$P_{cu} = 0.908\ W$$

6.2.1.3.13. AC FLUX DENSITY

From [7] the ac flux density will be

$$B_{ac} = \frac{0.4\ \pi\ N\ (\frac{\Delta I_L}{2})\ \mu \times 10^{-4}}{MPL} \quad (T) \tag{6-32}$$

$$B_{ac} = \frac{0.4 \times \pi \times 9 \times (\frac{5}{2}) \times 75 \times 10^{-4}}{5.8}$$

$$B_{ac} = 36.56\ mT$$

6.2.1.3.14. CORE LOSSES

From [14] the core loss will be

$$mW/g = 0.144\ (2\ f_s)^{(1.12)}\ B_m^{(2.01)} \qquad (6\text{-}33)$$

$$mW/g = 161.1$$

With a total core weight of 19 g the total core loss will be

$$P_c = mW/g \times W_{tfe}\ (W) \qquad (6\text{-}34)$$

$$P_c = 3.06\ W$$

6.2.1.3.15. TOTAL LOSSES

$$P_\Sigma = P_c + P_{cu} \quad (W) \qquad (6\text{-}35)$$

$$P_\Sigma = 3.97\ W$$

6.2.1.3.16. TEMPERATURE RISE

From [7] the rise in temperature will be

$$\psi = \frac{P_\Sigma}{A_t} \quad (W/cm^2) \tag{6-36}$$

$$\psi = 0.17 \ W/cm^2$$

At an ambient temperature of 45 °C the rise in temperature will be approximately 85 °C from Figure H.1 Appendix H. The core operating temperature will therefore be 130 °C forcing the core to operate at its upper temperature limit.

With forced air cooling the operating temperature will be reduced somewhat, making the design feasible.

6.2.1.3.17. DC MAGNETISING FORCE

Since the applied DC magnetising force reduces the permeability it should be verified.

From [7] the DC magnetising force will be

$$H = \frac{0.4 \ \pi \ N \ I_{Lmax}}{MPL} \quad (Oe) \tag{6-37}$$

$$H = 43.87 \ Oe$$

The DC magnetizing force of approximately 44 Oersted will reduce the initial permeability by 44%, leaving 56% of useful

permeability. This will reduce the inductance of 5 μH selected by 12% leaving 4.4 μH at full load current. To correct for the drop in permeability the number of turns will be increased by 12% or one turn.

6.2.1.3.18. SUMMARY

L_3	: 5 μH
Core	: Micrometals mix #26, T90 - 26 Iron powder toroidal core
Winding	: 2 × 10 turns, AWG # 15
Losses	: 4.01 W
Temperature rise	: 85°C

This then completes the design for the +5 volt output filter choke.

6.2.2. THE DESIGN OF THE AUXILIARY FILTER CHOKES

The filter chokes for the auxiliary outputs +12V, -12V, -5V and +15V are designed using exactly the same formulae and procedures.

Summarising the different output filter chokes:

The +12V auxiliary output filter choke:

L_2	: 30 μH
Core	: Micrometals mix #26, T90 - 26

Iron powder toroidal core

Winding : 2 × 20 turns, AWG # 19

Losses : 1.86 W

Temperature rise : 40°C

The -12V auxiliary output filter choke:

L_5 : 231 μH

Core : Micrometals mix #8, T68 - 8/90

Iron powder toroidal core

Winding : 1 × 108 turns, AWG # 26

Losses : 0.42 W

Temperature rise : 28°C

The -5V auxiliary output filter choke:

L_4 : 100 μH

Core : Micrometals mix #8, T68 - 8/90

Iron powder toroidal core

Winding : 1 × 71 turns, AWG # 26

Losses : 0.27 W

Temperature rise : 18°C

The +15V auxiliary output filter choke:

L_1 : 185 μH

Core : Micrometals mix #8, T68 - 8/90

Iron powder toroidal core

Winding : 1 × 96 turns, AWG # 24

Losses : 0.55 W

Temperature rise : 38°C

6.3. THE DESIGN OF THE OUTPUT FILTER CAPACITORS

6.3.1. THE DESIGN OF THE +5V OUTPUT FILTER CAPACITOR

6.3.1.1. REQUIRED CAPACITANCE

The design of the output filter capacitor C_o (where $C_o = C_{34}$, C_{36} and C_{41}) is based on the method described in [2].

From [2] the minimum capacitance will be

$$C_o \geq \frac{\Delta I_L}{16\ \Delta V_o\ f_s} \quad (F) \tag{6-38}$$

where

ΔI_L - choke ripple current

ΔV_o - maximum permissible output ripple voltage

$$C_o \geq 62.5\ \mu F$$

The maximum permissible ESR will be

$$ESR \leq \frac{\Delta V_o}{2\ \Delta I_L} \quad (\Omega) \tag{6-39}$$

$$ESR \leq 5\ m\Omega$$

Since the above results are only applicable to capacitors

with negligible effective series resistances and inductances (i.e. ideal capacitors), the final capacitor value is selected larger than calculated to allow for the parasitic series resistances and inductances in the non-ideal capacitors.

Selected three 100 μF/20 V tantalum capacitors with the capacitors placed in parallel, the total capacitance will add up to 300 μF.

To ensure a minimum ripple voltage of 50 mV_{p-p} at the output the total ESR of the selected capacitors should be verified.

In this case the data sheet does not indicate the magnitude of the ESR at the required frequency. It will therefore be calculated.

$$ESR = \frac{\tan\delta}{4\ \pi\ f_s\ C_o} \quad (\Omega) \qquad (6\text{-}40)$$

$$ESR = 0.265\ m\Omega$$

With a practical achievable ESR of only 0.16 Ω per capacitor the theoretical calculated value of 0.265 mΩ will therefore not reflect the true ESR and cannot be used in this application. Therefore the total ESR will be 0.053 Ω, which is larger than the required ESR as calculated in equation (6-39).

Due to space restrictions and availability of low ESR

capacitors the choice made was retained, having to settle for a considerable increase (up to 250 mV_{p-p}) in output ripple voltage.

To limit the overshoot voltage ΔV_{omax} to 1 V during a maximum possible step change in load ΔI_{omax} the capacitor selected should have the following minimum value

$$C_o \geq \frac{t_{tr}}{2} \times \frac{\Delta I_{omax}}{\Delta V_{omax}} \quad (F) \qquad (6\text{-}41)$$

The transient recovery time t_{tr} of 50 μs has already been calculated in Section 6.2.1.1.

Therefore

$$C_o \geq 250\ \mu F$$

Maximum capacitor value allowed:

With the time constant equal to the t_{tr} the maximum possible capacitor value is calculated using equation (6-42).

Note that any further increase in C_o will show no improvement in the reduction of ΔV_{omax}.

Therefore

$$C_o \leq \frac{t_{tr}}{ESR} \quad (F) \tag{6-42}$$

$$C_o \leq 943\ \mu F$$

To keep the ESR requirement and output ripple voltage ΔV_o to a minimum the choice made is accepted.

Capacitor alternating-current loading:

Since the alternating-current loading is responsible for the heating of the capacitor it will be verified.

$$I_{Crms} = \frac{\Delta I_L}{2\sqrt{3}} \quad (A) \tag{6-43}$$

$$I_{Crms} = 1.44\ A$$

With the total permissible alternating current loading estimated at 4.2 Amps or approximately 3 times that of the actual current loading the effect of the alternating current flowing in the output capacitor C_o will be negligible.

6.3.2. THE DESIGN OF THE AUXILIARY OUTPUT FILTER CAPACITORS

Again exactly the same procedure and formulae will be used to calculate the +12V, -12V, -5V and +15V output filter capacitors.

Summarizing the different output filter capacitors selected:

The +12V auxiliary output filter capacitor:

$C_o \geq 83\ \mu F$

ESR $\leq$ 30 mΩ

Selected 3 $\times$ 100 μF/20 V

The -12V auxiliary output filter capacitor:

$C_o \geq 10\ \mu F$

ESR $\leq$ 240 mΩ

Selected 1 $\times$ 47 μF/25 V

The -5V auxiliary output filter capacitor:

$C_o \geq 25\ \mu F$

ESR $\leq$ 100 mΩ

Selected 1 $\times$ 68 μF/16 V

The +15V auxiliary output filter capacitor:

$C_o \geq 12\ \mu F$

ESR $\leq$ 66.67 mΩ

Selected 1 $\times$ 470 μF/25 V

This concludes the design for the output section.

7. CLOSING THE FEEDBACK LOOP

7.1. THE PHYSICAL CIRCUIT ELEMENTS

Figure 7.1 shows a simplified illustration of the physical circuit elements that make up the closed feedback loop.

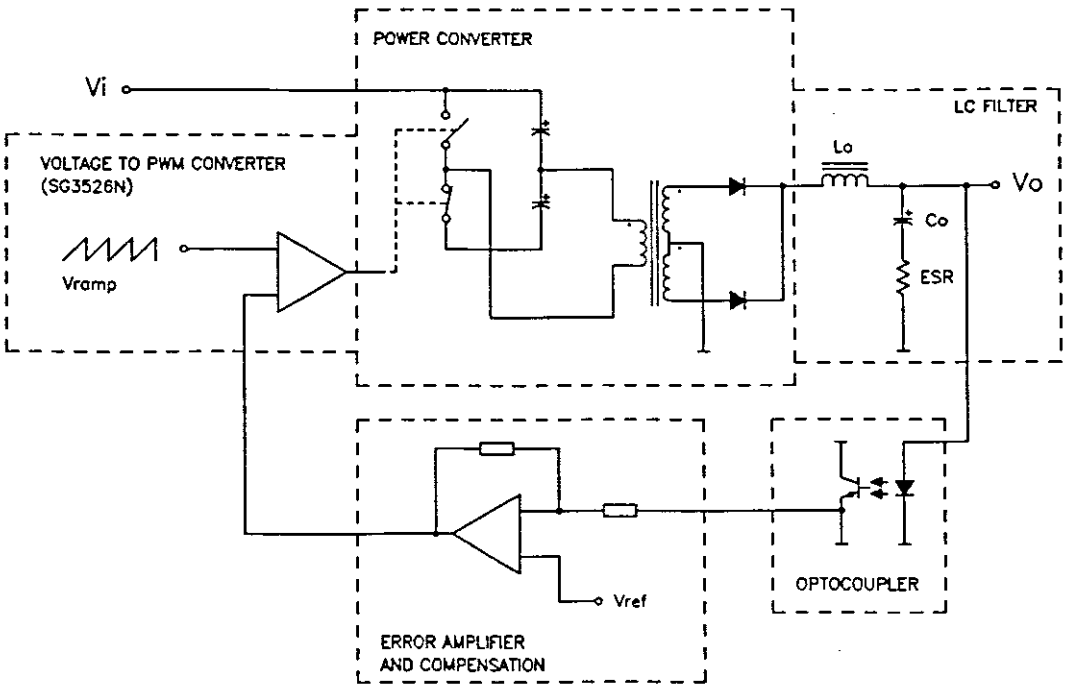

Figure 7.1 A simplified illustration of the closed feedback loop.

7.2. OUTPUT LC FILTER

The transfer function for the circuit shown in Figure 7.2 is given in equation (7-1).

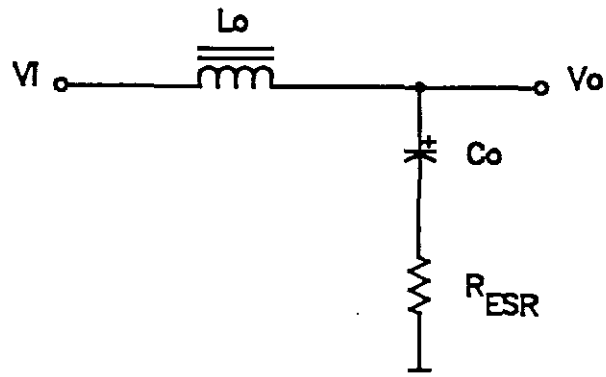

Figure 7.2 Output LC filter.

$$\frac{V_o}{V_i} = \frac{R_{ESR} + \frac{1}{sC_o}}{R_{ESR} + \frac{1}{sC_o} + sL_o} \qquad (7\text{-}1)$$

Simplifying

$$T(s) = \frac{V_o}{V_i} = \frac{sR_{ESR}C_o + 1}{s^2L_oC_o + sR_{ESR}C_o + 1} \qquad (7\text{-}2)$$

The filter will therefore introduce (1) a double-pole at its resonance frequency $f_{p(LC)}$ and (2) a zero caused by the capacitor ESR at $f_{z(ESR)}$. Figure 7.3 shows the frequency characteristics of the output LC filter.

With the output choke L_o (Section 6.2.1.1.), C_o and ESR

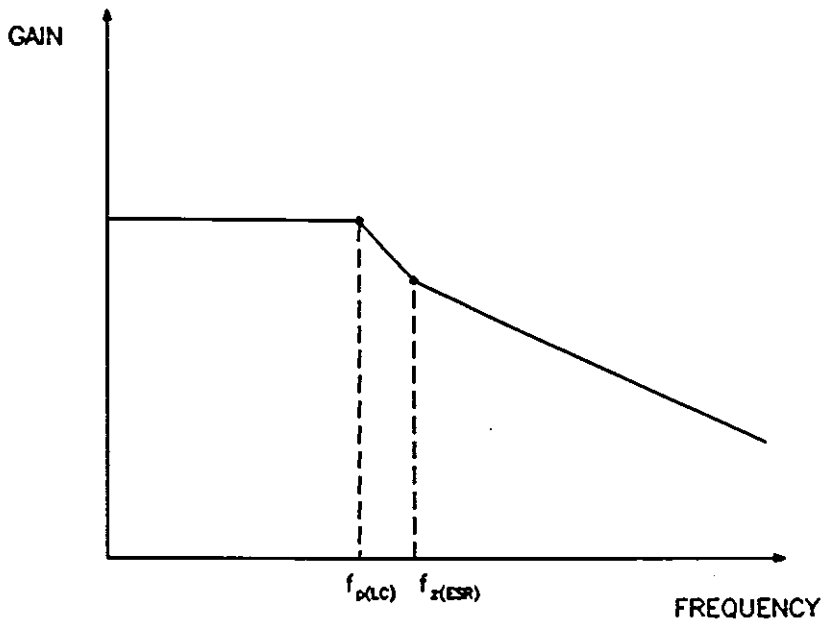

Figure 7.3 The frequency characteristics of the output LC filter.

(Section 6.3.1.) already calculated, $f_{p(LC)}$ and $f_{z(ESR)}$ is calculated.

The filter double-pole $f_{p(LC)}$ will be at

$$f_{p(LC)} = \frac{1}{2\ \pi\ \sqrt{L_o C_o}} \quad (Hz) \tag{7-3}$$

$$f_{p(LC)} = 3.75\ kHz$$

and the filter single-zero $f_{z(ESR)}$ will be at

$$f_{z(ESR)} = \frac{1}{2\ \pi\ R_{ESR}\ C_o} \quad (Hz) \tag{7-4}$$

$$f_{z(ESR)} = 8\ kHz$$

7.3. THE CONTROL-TO-OUTPUT DC GAIN

The control-to-output dc gain according to [6] will be

$$(dc\ gain)_{dB} = 20 \log \frac{V_{p(max)}}{V_{ramp}} \frac{N_{s(3a)}}{N_p} \qquad (7\text{-}5)$$

where

$V_{p(max)}$ - maximum applied primary voltage, V

V_{ramp} - PWM sawtooth ramp voltage, V

$N_{s(3a)}$ - number of turns for secondary winding 3a

N_p - primary turns

Substituting

$$(dc\ gain)_{dB} = 20 \log \frac{171}{2.5} \frac{2}{6}$$

$$(dc\ gain)_{dB} = 21.14\ dB$$

7.4. CONTROL-TO-OUTPUT TRANSFER FUNCTION

The control-to-output transfer function, which includes the gain of the voltage to PWM converter (SG3526N), the power converter and the characteristics of the output filter are shown in Figure 7.4.

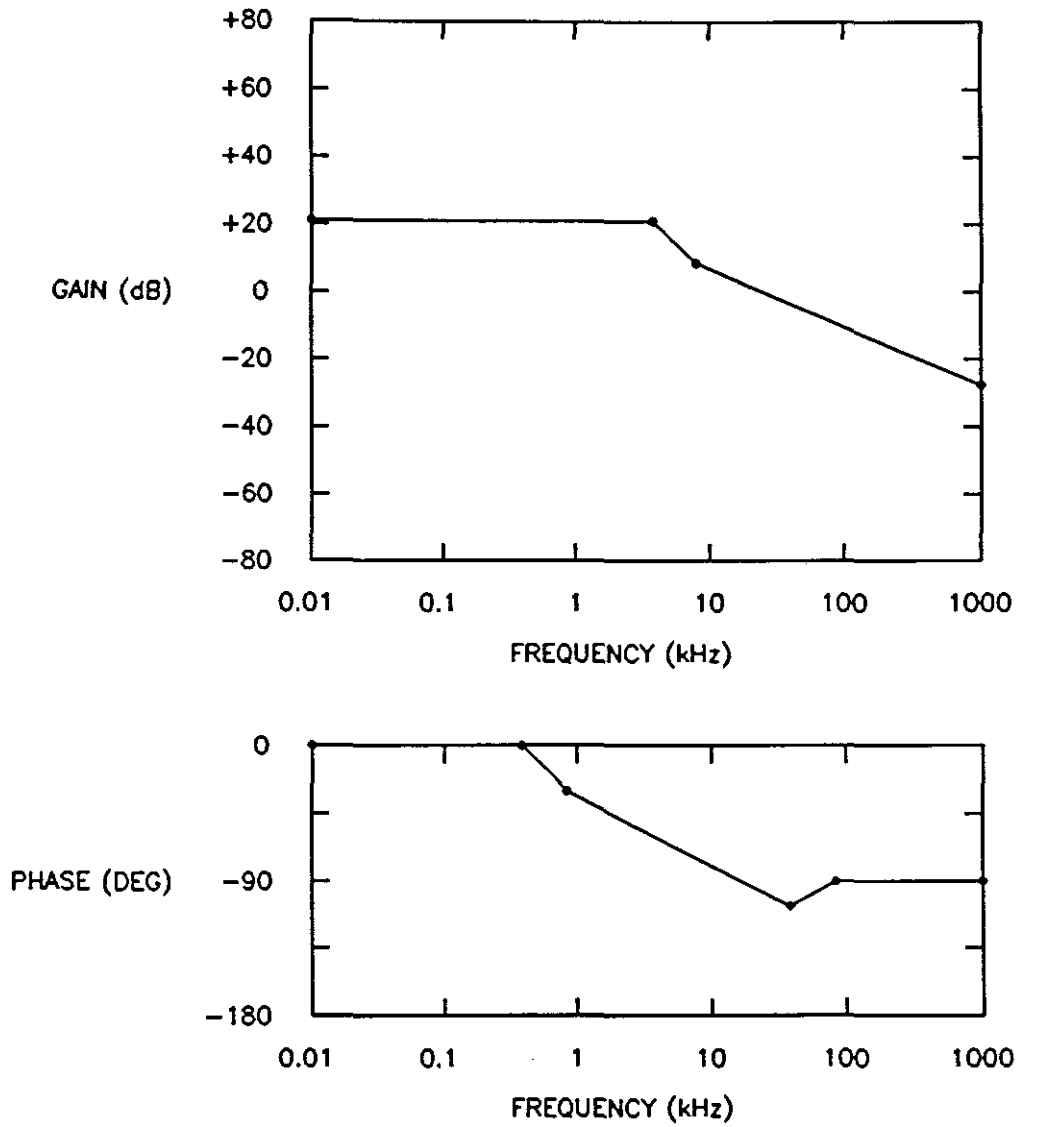

Figure 7.4 The gain and phase plot for the control-to-output transfer function.

7.5. OPTOCOUPLER

The optocoupler has no defined transfer function and is therefore the only unknown element in the feedback path. To be able to ignore the optocoupler and simplify the analyses the optocoupler is configured for (1) unity gain and (2) minimal phase shift.

7.6. ERROR AMPLIFIER COMPENSATION

The design of the error amplifier compensation network is based on the methods as described in [6], [15] and [16].

To prevent the control-to-output transfer function from jeopardising the power supply stability a compensation network is added to the error amplifier counteracting the gain and phases developed by the control-to-output transfer function.

To ensure power supply stability, the design objective will be to obtain an overall loop gain that crosses the 0 dB line at a -20 dB/decade slope with an adequate phase margin.

The error amplifier configuration as shown in Figure 7.5 is used, producing a good transient response.

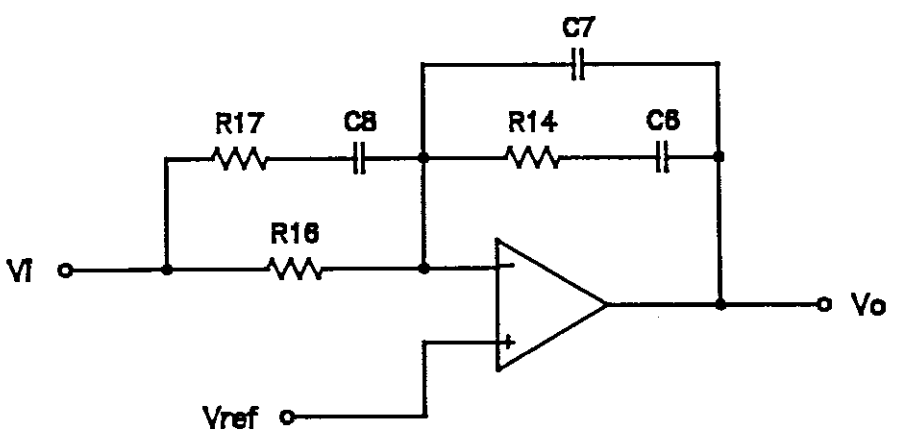

Figure 7.5 Error amplifier compensation network.

The transfer function for the circuit in Figure 7.5 is given in equation (7-6).

$$T(s) = \frac{V_o}{V_i} = \frac{[1 + sC_8(R_{17} + R_{16})]\ [1 + sC_6R_{14}]}{[sR_{16}(C_6 + C_7)]\ [1 + sC_8R_{17}]\ [1 + sR_{14}\frac{C_6}{C_7}]} \qquad (7\text{-}6)$$

The transfer function will introduce two zero-pole pairs, the placement of which will be done according to the following criteria:

1) Due to the stability criteria the zero cross-over frequency f_{xo} must be equal or below $\frac{1}{5}$ of the switching frequency.

$$f_{xo} = \frac{f_s}{5} \quad (Hz) \qquad (7\text{-}7)$$

$$f_{xo} = 20\ kHz$$

2) The gain required to bring the control-to-output transfer function (Figure 7.4) back to zero at the zero crossover frequency f_{xo} will be +1 dB.

3) The two zeros will be placed at

$$f_{z1} = f_{z2} = \frac{f_{p(LC)}}{2} \quad (Hz) \qquad (7\text{-}8)$$

$$f_{z1} = f_{z2} = 1.88\ kHz$$

4) To counteract the zero caused by the ESR of the capacitor, the lower frequency pole is placed at

$$f_{z1} = f_{z(ESR)} = 8\ kHz$$

5) The second higher frequency pole is placed above the zero crossover frequency to limit the effect of the higher frequency components.

$$f_{z2} \geq 1.5\ f_{xo} \quad (Hz) \tag{7-9}$$

$$f_{z2} \geq 30\ kHz$$

6) The gain at f_{z1} and f_{z2}

$$A_{v1} = A_{v2} + 20 \log \frac{f_{z2}}{f_{z1}} \quad (dB) \tag{7-10}$$

$$A_{v1} = -11.58\ dB$$

The resulting gain and phase plot for the error amplifier compensation network is shown in Figure 7.6.

Determining the different component values:

Selected R_{16} = 10 kΩ/¼ W

$$R_{14} = R_{16}\ A_{v1} \quad (\Omega) \tag{7-11}$$

$$R_{14} = 2.7\ k\Omega$$

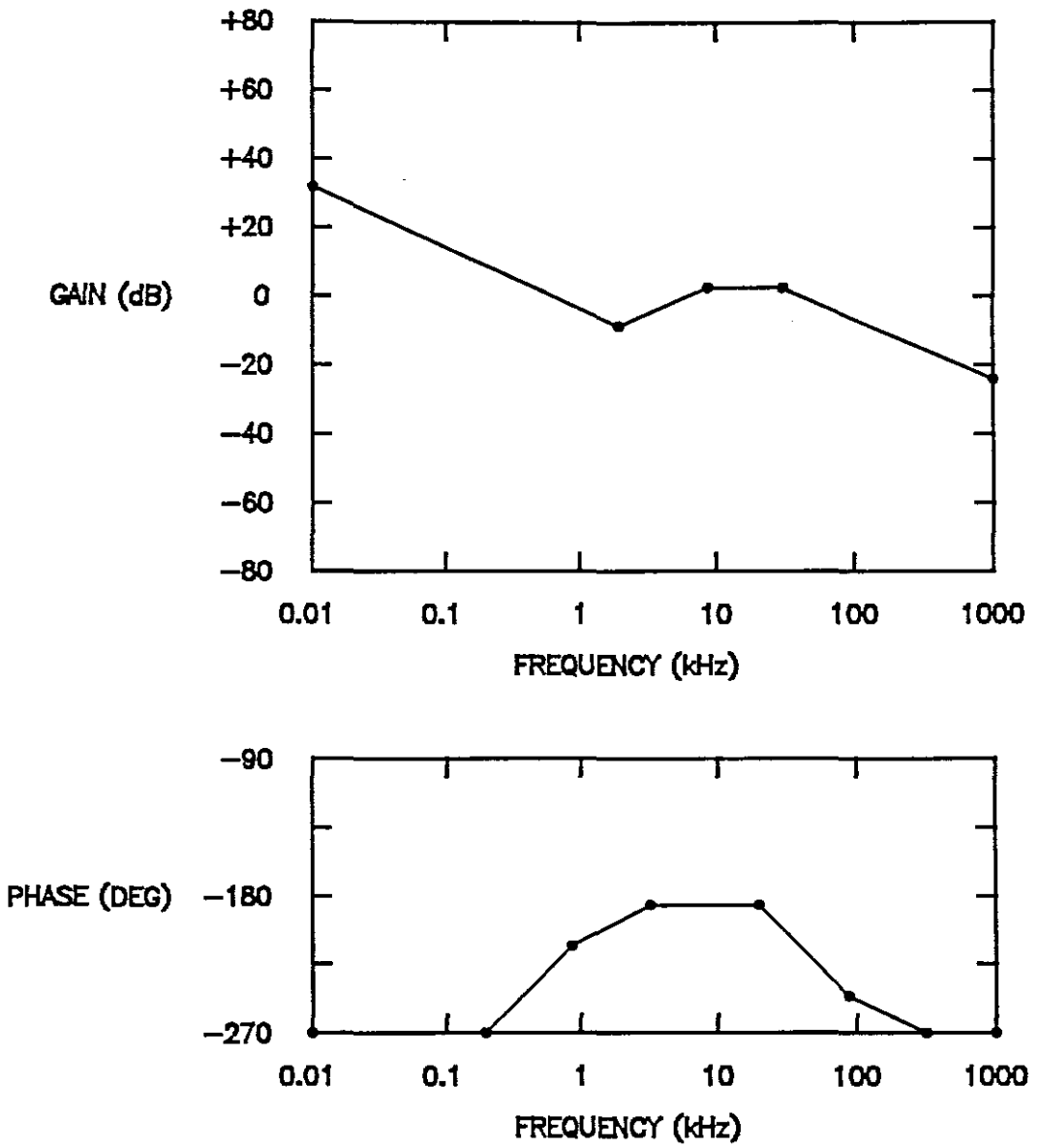

Figure 7.6 The gain and phase plot for the error amplifier compensation network.

Selected R_{14} = 2.7 kΩ/¼ W

$$R_{17} = \frac{R_{14}}{A_{v2}} \quad (\Omega) \tag{7-12}$$

$$R_{17} = 2.4\ k\Omega$$

Selected R_{17} = 2.4 kΩ/¼ W

$$C_6 = \frac{1}{2\ \pi\ R_{14}\ f_{z1}} \quad (F) \tag{7-13}$$

$$C_6 = 31.35\ nF$$

Selected C_6 = 33 nF/50 V

$$C_8 = \frac{1}{2\ \pi\ R_{17}\ f_{p1}} \quad (F) \tag{7-14}$$

$$C_8 = 8.29\ nF$$

Selected C_8 = 8.2 nF/50 V

$$C_7 = \frac{1}{2\ \pi\ R_{14}\ f_{p2}} \quad (F) \tag{7-15}$$

$$C_7 = 1.97\ nF$$

Selected C_7 = 2.2 nF/50 V.

The overall gain and phase plot is shown in Figure 7.7. The graph clearly displays where the overall gain crosses the 0 dB line at 20 kHz with a slope of -20 dB/decade as desired. This concludes the design for the feedback loop.

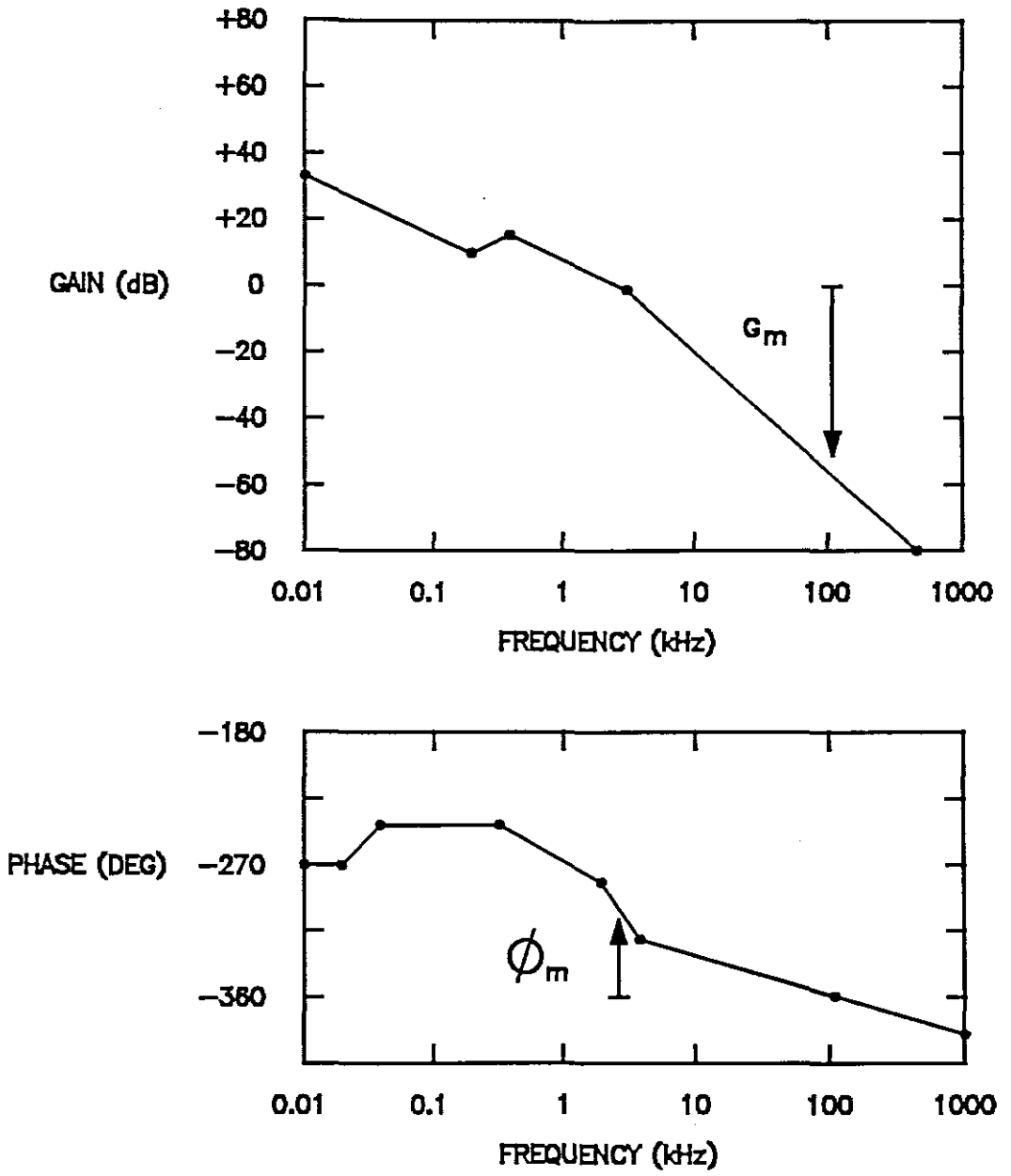

Figure 7.7 The overall gain and phase plot of the feedback network.

8. RESULTS AND CONCLUSION

A detailed discussion of the circuitry used to implement a half-bridge push-pull converter as shown in Appendix A, was presented. The design met the objectives as stated in the introduction and highlighted the following components:

1) Two IRF 740 HEXFETS. These devices switch approximately 4 amperes at 200 volts. Their maximum switching frequency of 500 kHz and higher, makes them an ideal choice for this application.

2) The SG3526N, a third generation PWM control circuit, provides the normal housekeeping functions e.g. digital current limiting and is CMOS and TTL compatible.

3) A CNX36 optocoupler. This device provides an electrically isolated feedback signal from the load to the control circuit.

4) The SG3543 output supervisory circuit complemented by a LM339 quad comparator provide the all important power supply and load protection.

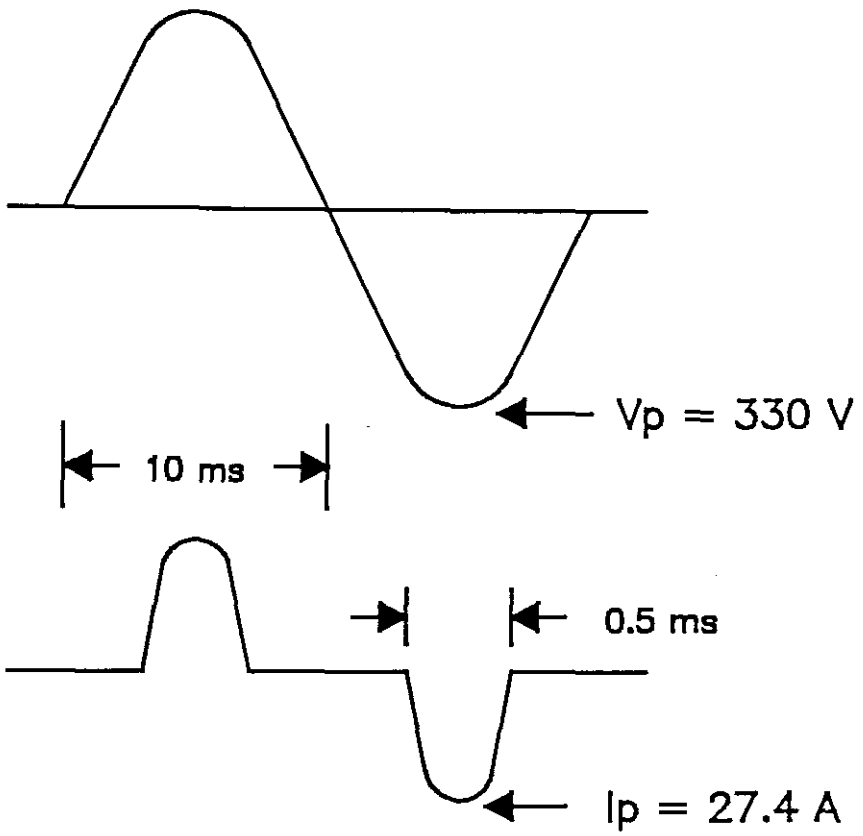

Figure 8.1 Input voltage and current pulses as measured by voltage and current probe.

The efficiency is measured at 85% (176 watts) of the rated load. To simplify measurements and subsequent calculations the input voltage (V_{in} = 233 V_{rms}) is assumed to be constant during current conduction.

A representation of the input voltage and current pulses as seen on the oscilloscope display is shown in Figure 8.1.

Since both waveforms are sinusoidal the average input power can be calculated using equation (8-1).

$$P_i = \frac{2}{\pi} V_p \times I_p \left(\frac{t_{on}}{T}\right) \quad (W) \tag{8-1}$$

$$P_i = (330 \times \frac{2}{\pi})(27.4 \times \frac{0.5\ ms}{10\ ms})$$

$$P_i = 288\ W$$

The overall efficiency will therefore be

$$\eta = \frac{P_o}{P_i} \times 100 \quad (\%) \tag{8-2}$$

$$\eta = \frac{176}{288} \times 100$$

$$\eta = 61\ \%$$

With an overall efficiency of 61% the total power lost in the design is about 112 watts. Of this approximately 73% is lost to the two power MOSFETS, the output rectifiers and the power transformer T2.

The overall efficiency can be further increased by selecting power MOSFETS with even lower $R_{DS(on)}$ specifications and rectifier diodes with lower forward voltage drops.

The results for the line, load and cross regulation are presented in Tables 1, 2 and 3.

Table 8.1: Line Regulation

Output	Condition	ΔV_o	Percent Regulation
+5V	V_{in} = 187 V to 242 V I_o = 17.6 A	0.01 V	0.2%
+12V	V_{in} = 187 V to 242 V I_o = 7.6 A	0.16 V	1.3%

Table 8.2: Load Regulation

Output	Condition	ΔV_o	Percent Regulation
+5V	I_o = 9.4 A to 18.3 A V_{in} = 230 V	0.04 V	0.8%
+12V	I_o = 3.3 A to 7.8 A V_{in} = 230 V	0.16 V	1.3%

Table 8.3: Cross Regulation

Output	Condition	ΔV_o	Percent Regulation
+12V	$I_{o(+5)}$ = 9.4 A to 18.3 A V_{in} = 230 V	0.96 V	8%
-12V		0.47 V	3.92%
-5V		0.05 V	1%

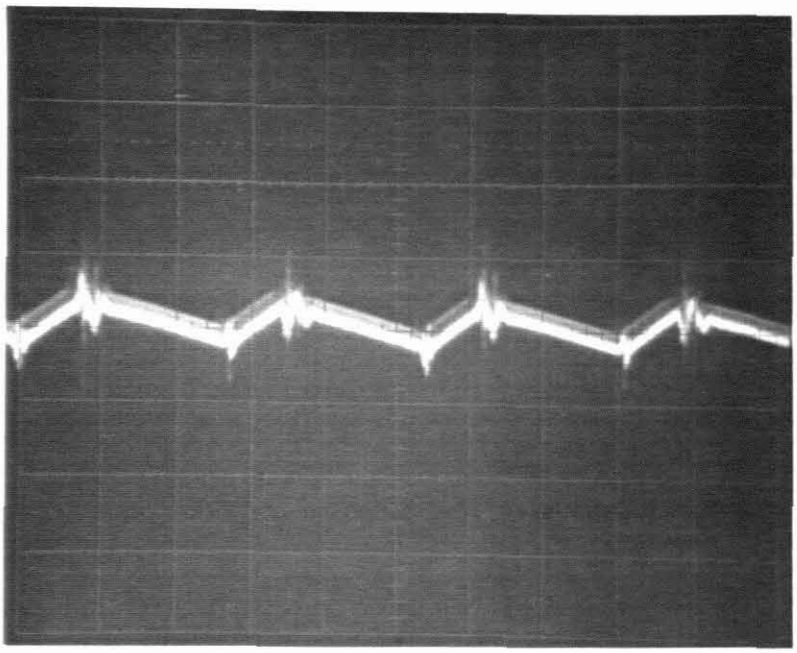

Figure 8.2 Output ripple ΔV_o, measured across C_{34}, C_{36} and C_{41}.

Horizontal scale: 2 μs/division
Vertical scale : 0.5 V/division

The ripple content for the +5V main output at 80% of the rated load (20 A) is shown in Figure 8.2. From Figure 8.2 a ripple voltage of about 200 mV_{p-p} can be recognised. The increase in output ripple was unavoidable, due to the lower grade tantalum capacitors selected. These capacitors presented a much larger ESR and ESL value than desired, providing a poor attenuation in noise and ripple as seen in Figure 8.2.

The ripple content can be further reduced by selecting higher quality capacitors or by the addition of a high frequency LC filter circuit. The thickening of the trace noticed in

Figure 8.2 is due to a proportion of the 100 Hz input ripple appearing at the output, which is inevitable.

In all a 61% efficient, 210 watt 100 kHz half-bridge push-pull converter was successfully developed. The prototype required about 1 521 cm^3 and weighed approximately 2.56 kg including the metal enclosure.

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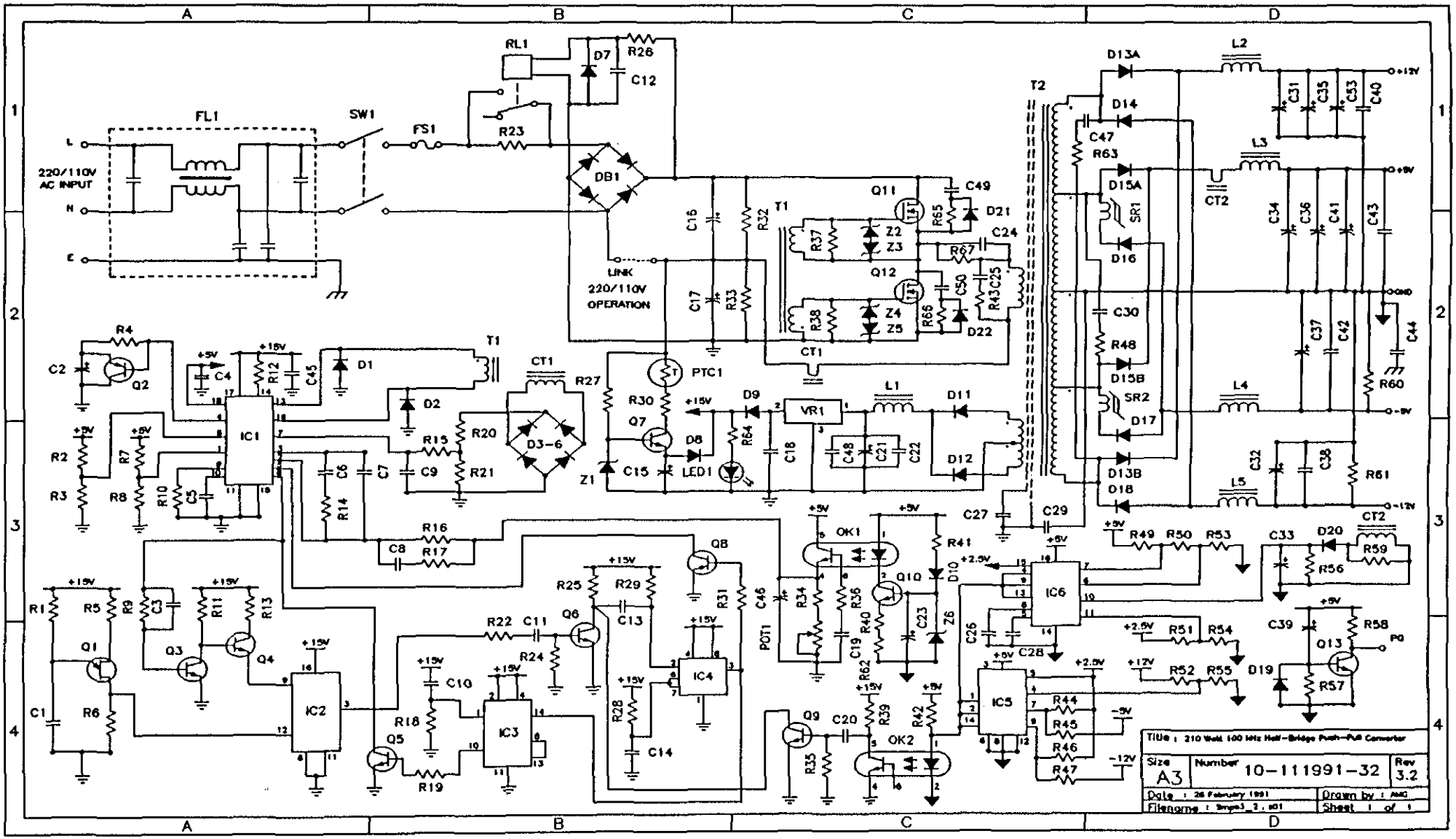
APPENDIX A

THE CIRCUIT DIAGRAM FOR THE 210 WATT 100 kHz HALF-BRIDGE PUSH-PULL CONVERTER


A
B
C
D
1
2
3
4
FL1
SW1
FS1
RL1
D7
R26
C12
R23
DB1
220/110V
AC INPUT
L
N
E
LINK
220/110V
OPERATION
T1
T2
CT1
CT2
PTC1
VR1
IC1
IC2
IC3
IC4
IC5
IC6
OK1
OK2
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
D1
D2
D3-6
D8
D9
D10
D11
D12
D13A
D13B
D14
D15A
D15B
D16
D17
D18
D19
D20
D21
D22
LED1
Z1
Z2
Z3
Z4
Z5
Z6
SR1
SR2
L1
L2
L3
L4
L5
PO1
+5V
+15V
+12V
-5V
-12V
+2.5V
GND
Title : 210 Watt 100 kHz Half-Bridge Push-Pull Converter
Size
A3
Number
10-111991-32
Rev
3.2
Date : 26 February 1991
Drawn by :
Filename :
Sheet 1 of 1

APPENDIX B

COMPONENT LIST

COMPONENT LIST

RESISTORS

Reference Designator	Type	Value	Rating
R1	Carbon	470 kΩ	¼ W
R2	Carbon	27 kΩ	¼ W
R3	Carbon	27 kΩ	¼ W
R4	Carbon	100 Ω	¼ W
R5	Carbon	39 Ω	¼ W
R6	Carbon	390 Ω	¼ W
R7	Carbon	18 kΩ	¼ W
R8	Carbon	18 kΩ	¼ W
R9	Carbon	68 kΩ	¼ W
R10	Carbon	3.3 kΩ	¼ W
R11	Carbon	5.6 kΩ	¼ W
R12	Carbon	10 Ω	½ W
R13	Carbon	47 Ω	¼ W
R14	Carbon	2.7 kΩ	¼ W
R15	Carbon	15 Ω	¼ W
R16	Carbon	10 kΩ	¼ W
R17	Carbon	2.4 kΩ	¼ W
R18	Carbon	220 Ω	¼ W
R19	Carbon	560 kΩ	¼ W
R20	Carbon	162 Ω	¼ W
R21	Carbon	33 Ω	¼ W

RESISTORS (continued)

Reference Designator	Type	Value	Rating
R22	Carbon	10 kΩ	¼ W
R23	Wire wound	6.8 Ω	5 W
R24	Carbon	10 kΩ	¼ W
R25	Carbon	4.7 kΩ	¼ W
R26	Carbon	22 kΩ	5 W
R27	Wire wound	33 kΩ	1.6 W
R28	Carbon	1 MΩ	¼ W
R29	Carbon	2.2 kΩ	¼ W
R30	Wire wound	2.7 kΩ	5 W
R31	Carbon	27 kΩ	¼ W
R32	Carbon	100 kΩ	1 W
R33	Carbon	100 kΩ	1 W
R34	Carbon	390 Ω	¼ W
R35	Carbon	1.2 kΩ	¼ W
R36	Carbon	10 kΩ	¼ W
R37	Carbon	1 kΩ	¼ W
R38	Carbon	1 kΩ	¼ W
R39	Carbon	3.3 kΩ	¼ W
R40	Carbon	33 Ω	¼ W
R41	Carbon	390 Ω	¼ W
R42	Carbon	820 Ω	¼ W
R43	Wire wound	330 Ω	5 W
R44	Carbon	5.1 kΩ	¼ W

RESISTORS (continued)

Reference Designator	Type	Value	Rating
R45	Carbon	12 kΩ	¼ W
R46	Carbon	5.1 kΩ	¼ W
R47	Carbon	27 kΩ	¼ W
R48	Carbon	10 Ω	1 W
R49	Carbon	15 kΩ	¼ W
R50	Carbon	3.3 kΩ	¼ W
R51	Carbon	22 kΩ	¼ W
R52	Carbon	22 kΩ	¼ W
R53	Carbon	15 kΩ	¼ W
R54	Carbon	27 kΩ	¼ W
R55	Carbon	5.1 kΩ	¼ W
R56	Carbon	100 Ω	¼ W
R57	Carbon	10 kΩ	¼ W
R58	Carbon	470 Ω	¼ W
R59	Carbon	330 Ω	1 W
R60	Wire wound	47 Ω	1 W
R61	Wire wound	100 Ω	5 W
R62	Carbon	510 Ω	¼ W
R63	Wire wound	82 Ω	5 W
R64	Carbon	1.5 kΩ	¼ W
R65	Wire wound	220 Ω	5 W
R66	Wire wound	220 Ω	5 W
R67	Carbon	1.8 kΩ	1 W

CAPACITORS

Reference Designator	Type	Value	Rating
C1	Metallized polyester	0.1μF	63 V
C2	Electrolytic	10 μF	63 V
C3	Ceramic	470 pF	500 V
C4	Metallized polyester	10 nF	63 V
C5	Polyester film	2200 pF	400 V
C6	Polyester film	33 nF	250 V
C7	Ceramic	2.2 nF	500 V
C8	Ceramic	8.2 nF	500 V
C9	Mylar	1 nF	50 V
C10	Electrolytic	4.7 μF	63 V
C11	Ceramic	100 nF	50 V
C12	Film	1 μF	100 V
C13	Ceramic	10 nF	50 V
C14	Metallized polyester	1 μF	63 V
C15	Electrolytic	47 μF	63V
C16	Electrolytic	680 μF	250 V
C17	Electrolytic	680 μF	250 V
C18	Ceramic	0.01 μF	50 V
C19	Ceramic	0.1 μF	63 V
C20	Ceramic	100 nF	50 V
C21	Electrolytic	470 μF	25 V
C22	Multilayer ceramic	0.1 μF	63 V
C23	Electrolytic	4.7 μF	25 V

CAPACITORS (continued)

Reference Designator	Type	Value	Rating
C24	Metallized polyester	0.47 μF	400 V
C25	Ceramic	561 pF	2 kV
C26	Metallized polyester	1 μF	63 V
C27	Ceramic	0.01 μF	3 kV
C28	Metallized polyester	10 nF	63 V
C29	Ceramic	0.01 μF	3 kV
C30	Ceramic	1.5 nF	500 V
C31	Tantalum	100 μF	20 V
C32	Tantalum	47 μF	25 V
C33	Electrolytic	100 μF	25 V
C34	Tantalum	100 μF	20 V
C35	Tantalum	100 μF	20 V
C36	Tantalum	100 μF	20 V
C37	Tantalum	68 μF	16 V
C38	Multilayer ceramic	0.1 μF	63 V
C39	Electrolytic	10 μF	63 V
C40	Multilayer ceramic	0.1 μF	63 V
C41	Tantalum	100 μF	20 V
C42	Multilayer ceramic	0.1 μF	63 V
C43	Multilayer ceramic	0.1 μF	63 V
C44	Ceramic	0.01 μF	3 kV
C45	Tantalum	10 μF	63 V
C46	Not used	--	--

CAPACITORS (continued)

Reference Designator	Type	Value	Rating
C47	Ceramic	2.2 nF	500 V
C48	Not used	--	--
C49	Ceramic	1 nF	500 V
C50	Ceramic	1 nF	500 V
C51	Not used	--	--
C52	Not used	--	--
C53	Tantalum	100 μF	20 V

DIODES

Reference Designator	Type	Description
D1	1N5819	Schottky rectifier
D2	1N5819	Schottky rectifier
D3	1N5819	Schottky rectifier
D4	1N5819	Schottky rectifier
D5	1N5819	Schottky rectifier
D6	1N5819	Schottky rectifier
D7	1N4007	Silicon rectifier
D8	1N4004	Silicon rectifier
D9	1N4004	Silicon rectifier

DIODES (continued)

Reference Designator	Type	Description
D10	1N4004	Silicon rectifier
D11	UF3007	Superfast switching
D12	UF3007	Superfast switching
D13	ESAC92-02	Fast Recovery diodes
D14	1N4936	Fast Recovery diode
D15	ESAC87-009	Schottky rectifiers
D16	1N5819	Schottky rectifier
D17	1N5819	Schottky rectifier
D18	1N4936	Fast Recovery diode
D19	1N4007	Silicon rectifier
D20	1N5819	Schottky rectifier
D21	UF3007	Superfast switching
D22	UF3007	Superfast switching
DB1	PBL405	Bridge rectifier

ZENER DIODES

Reference Designator	Type
Z1	BZX79C12
Z2	BZX79C15
Z3	BZX79C15
Z4	BZX79C15
Z5	BZX79C15
Z6	BZX79C2V7

TRANSISTORS

Reference Designator	Type	Description
Q1	2N2646	UJT
Q2	2N2907A	Bipolar
Q3	2N3903	Bipolar
Q4	2N2222A	Bipolar
Q5	BC237BC	Bipolar
Q6	BC184C	Bipolar
Q7	2N3439	Bipolar
Q8	BC239C	Bipolar
Q9	BC184C	Bipolar

TRANSISTORS (continued)

Reference Designator	Type	Description
Q10	BC238C	Bipolar
Q11	IRF740	POWERMOS
Q12	IRF740	POWERMOS
Q13	BC237	Bipolar

TRANSFORMERS

Reference Designator	Type	Description	Material
T1	E20/10/5	Core half (×2) Coil former	3E2
T2	ETD39	Core half (×2) Coil former Clip (×2)	N27

CURRENT TRANSFORMERS

Reference Designator	Type	Description	Material
CT1	RCC 9/6/3	Toroid	3E2
CT2	T50 - 8/90	Toroid	Iron powder

INDUCTORS

Reference Designator	Type	Description	Material
L1	T68 - 8/90	Toroid	Iron powder
L2	T90 - 26	Toroid	Iron powder
L3	T90 - 26	Toroid	Iron powder
L4	T68 - 8/90	Toroid	Iron powder
L5	T68 - 8/90	Toroid	Iron powder

SATURABLE REACTORS

Reference Designator	Type	Description	Material
SR1	RCC 14/9/5	Toroid	3R1
SR2	RCC 14/9/5	Toroid	3R1

INTEGRATED CIRCUITS

Reference Designator	Description
IC1	SG2526J
IC2	CD4060BC
IC3	MM74C93N
IC4	LM555
IC5	LM339
IC6	SG3543
OK1	CNX36
OK2	CNX36
VR1	LM340T15

HEATSINKS

Reference Designator	Type	Description	Manufacturer
HS1	VC5259C	44 K/W	Assmann
HS2	SK104	9 K/W	Fischer Elektronik
HS3	SK104	9 K/W	Fischer Elektronik
HS4	SK104	9 K/W	Fischer Elektronik
HS5	SK104	9 K/W	Fischer Elektronik

CONNECTORS

Reference Designator	Description
CON1	Molex plug and socket with lock ramp, 2 pins
CON2	Molex plug and socket with lock ramp, 3 pins
CON3	Card connector vertical 2.54 mm, 7 pins
CON4	Molex plug and socket with lock ramp, 2 pins

MISCELLANEOUS

Reference Designator	Description	Manufacturer
FS1	5A/250V, time-lag, 5 × 20 mm	ESKA
	Fuse-holder, OGB, 5 × 20 mm	Schurter
PTC1	Q63100 - P2350 - C870	Siemens
RL1	VS48TBU - 5	Takamisawa
POT1	Trimpot, 200 Ω	Bourns
FAN	12V axial fan, 49.4 CFM	Papst
	92 × 92 × 25 mm and	
	finger guard (×1)	

APPENDIX C

AWG WINDING DATA TABLE (COPPER WIRE, HEAVY INSULATION)

TABLE C.1 AWG WINDING DATA

AWG	Diameter, copper, cm^2	Area, copper, cm^2	Diameter, insulation, cm^2	Ω/cm 20 °C
10	0.259	0.052620	0.273	0.000033
11	0.231	0.041729	0.244	0.000041
12	0.205	0.033092	0.218	0.000052
13	0.183	0.026243	0.195	0.000062
14	0.163	0.020811	0.174	0.000083
15	0.145	0.016504	0.156	0.000104
16	0.129	0.013088	0.139	0.000132
17	0.115	0.010379	0.124	0.000166
18	0.102	0.008231	0.111	0.000209
19	0.091	0.006527	0.100	0.000264
20	0.081	0.005176	0.089	0.000333
21	0.072	0.004105	0.080	0.000420
22	0.064	0.003255	0.071	0.000530
23	0.057	0.002582	0.064	0.000668
24	0.051	0.002047	0.057	0.000842
25	0.045	0.001624	0.051	0.001062
26	0.040	0.001287	0.046	0.001339
27	0.036	0.001021	0.041	0.001689
28	0.032	0.000810	0.037	0.002129
29	0.029	0.000642	0.033	0.002685
30	0.025	0.000509	0.030	0.003386
31	0.023	0.000404	0.027	0.004269
32	0.020	0.000320	0.024	0.005384
33	0.018	0.000254	0.022	0.006789
34	0.016	0.000201	0.020	0.008560
35	0.014	0.000160	0.018	0.010795
36	0.013	0.000127	0.016	0.013612
37	0.011	0.000100	0.014	0.017165
38	0.010	0.000080	0.013	0.021644
39	0.009	0.000063	0.012	0.027293
40	0.008	0.000050	0.010	0.034417
41	0.007	0.000040	0.009	0.057982

APPENDIX D

CORE CONFIGURATION CONSTANTS FOR THE ETD CORE RANGE

TABLE D.1 ETD CORE CHARACTERISTICS

Core	A_t (cm^2)	A_p (cm^4)	MLT (cm)	N / AWG	Ω(55°C)	P_Σ	$I = \sqrt{\frac{W}{\Omega}}$	Δ T (30°C) $J = \frac{I}{cm^2}$	Weight fe (g)	Weight Cu (g)	Vol (cm^3)	A_e (cm^2)
ETD 34/17/11	72.11	1.197	6	81/20	0.184	2.88	3.96	763	40	22.97	7.64	0.971
ETD 39/20/13	91.79	2.217	6.9	117/20	0.306	3.67	3.46	667	60	38.15	11.5	1.25
ETD 44/22/15	112.41	3.7	7.7	141/20	0.411	4.50	3.31	638	94	51.31	17.8	1.73
ETD 49/25/16	136.44	5.761	8.5	180/20	0.580	5.46	3.07	592	124	72.31	24	2.11

TABLE D.2 ETD CORE CONFIGURATION CONSTANTS

Core	K_j (Δ 30°C)	(x)	(y)	K_s	K_w	K_v
ETD Core	665	1.12	-0.11	103.19	62.85	15.24

(Adapted from [7] and [13])

APPENDIX E

DEFINITIONS OF COIL FORMER AND WINDING DIMENSIONS

DEFINITIONS OF COIL FORMER AND WINDING DIMENSIONS

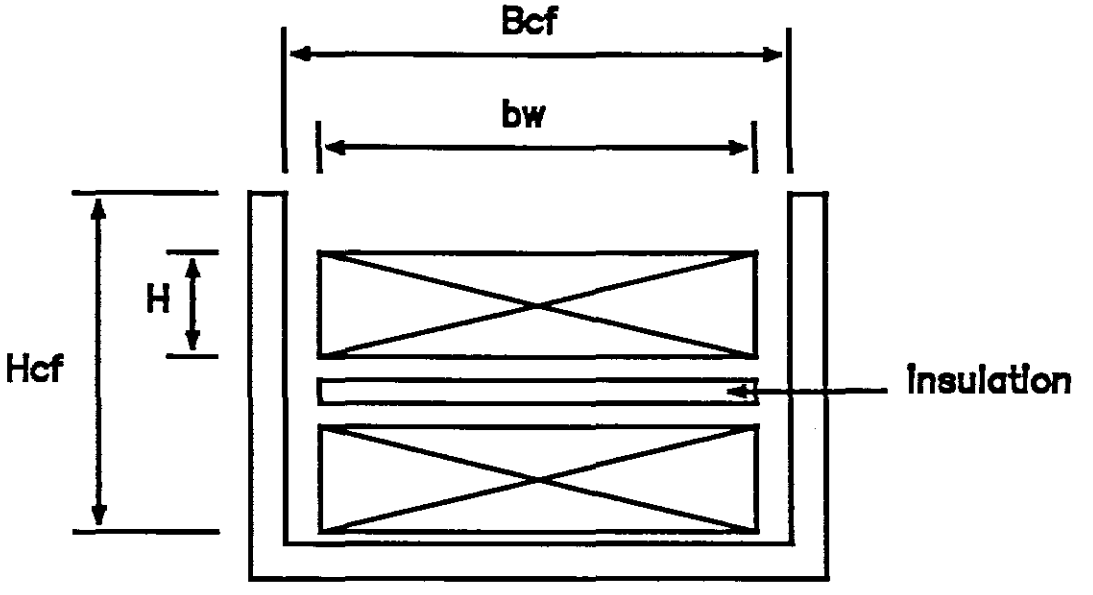


Figure E.1 Symbols of coil former and winding dimensions as used in power transformer design (adapted from [11]).

Where

H_{CF} - height of the coil former or winding window

B_{CF} - coil former breadth

b_w - actual winding breadth (influenced by the required safety standard)

H - height of a winding (portion)

Note : All dimensions are given in millimeters, except where stated in text to simplify calculations.

APPENDIX F

CORE LOSS CURVE FOR THE N27 FERRITE MATERIAL

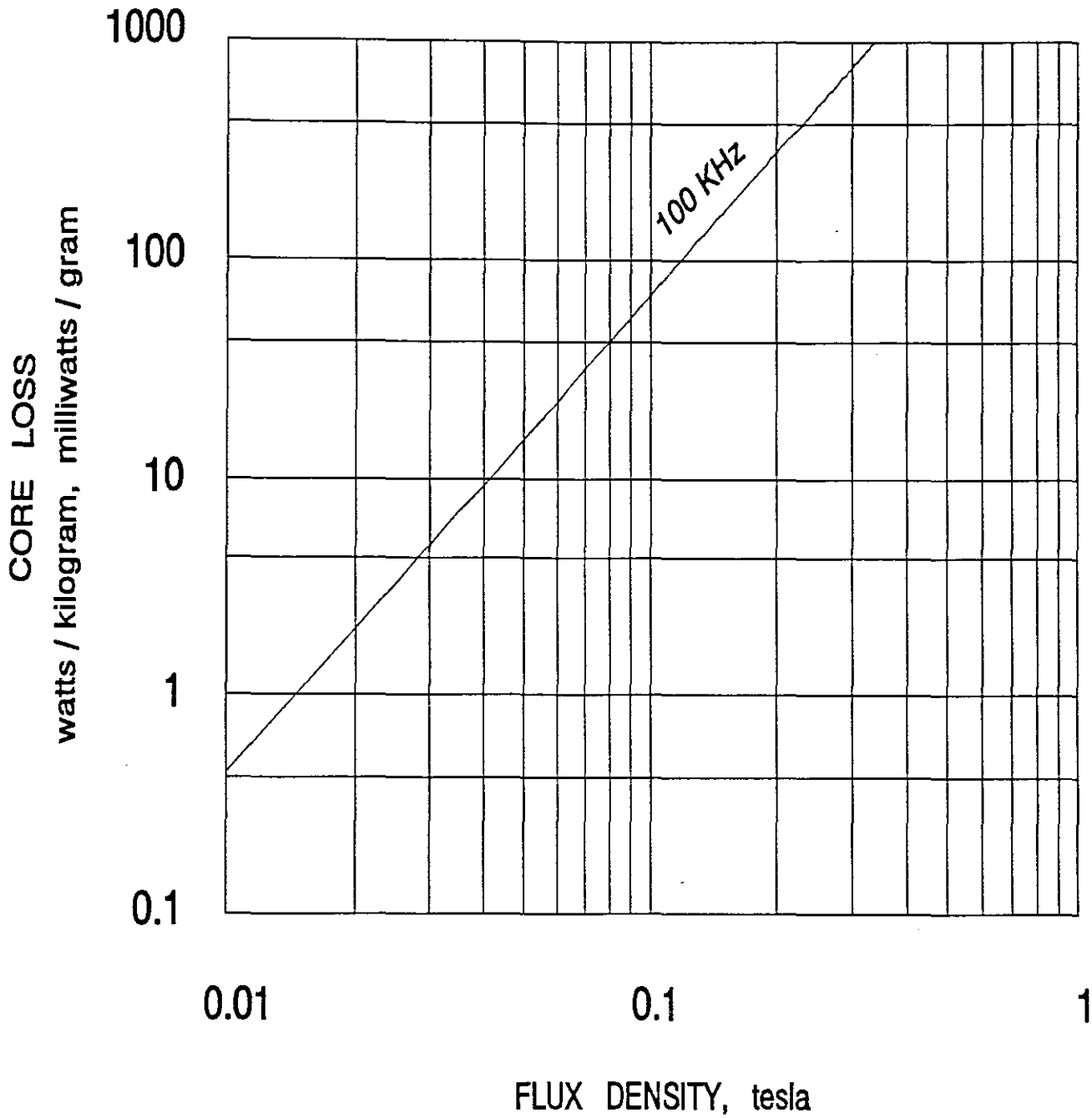


Figure F.1 Core loss curve for the N27 ferrite material as a function of flux density B_m and frequency (adapted from [14]).

APPENDIX G

CONDUCTOR SELECTION

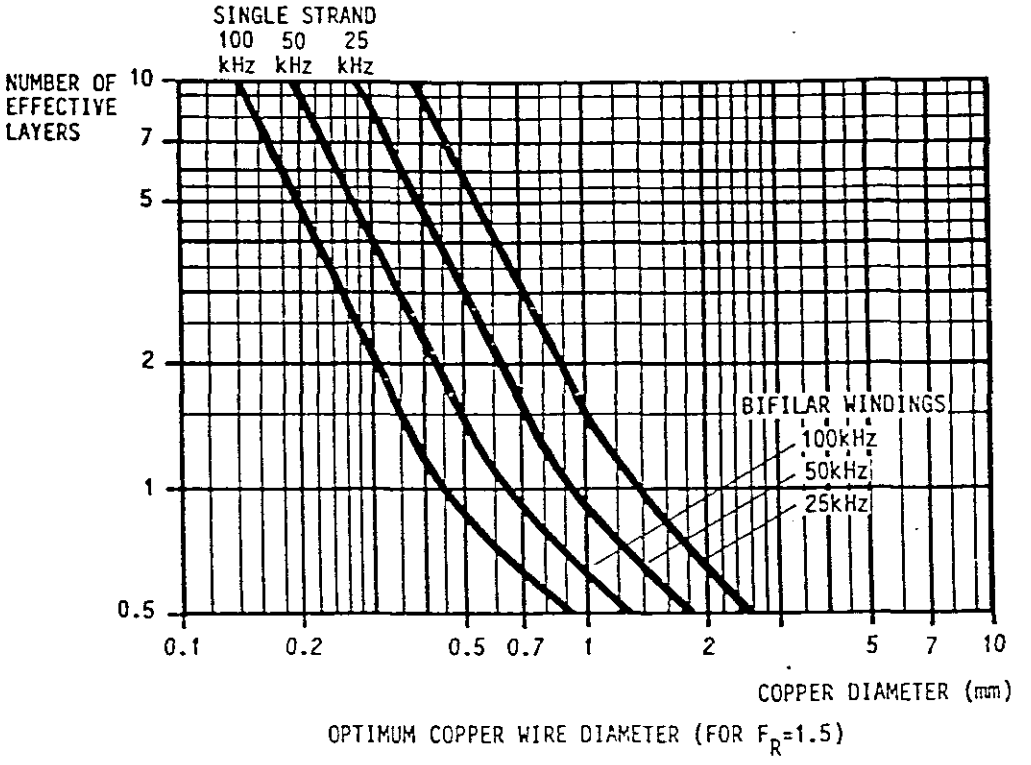


Figure G.1 The optimum copper wire diameter d_c for an F_R ratio of 1.5 (Mullard Ltd.).

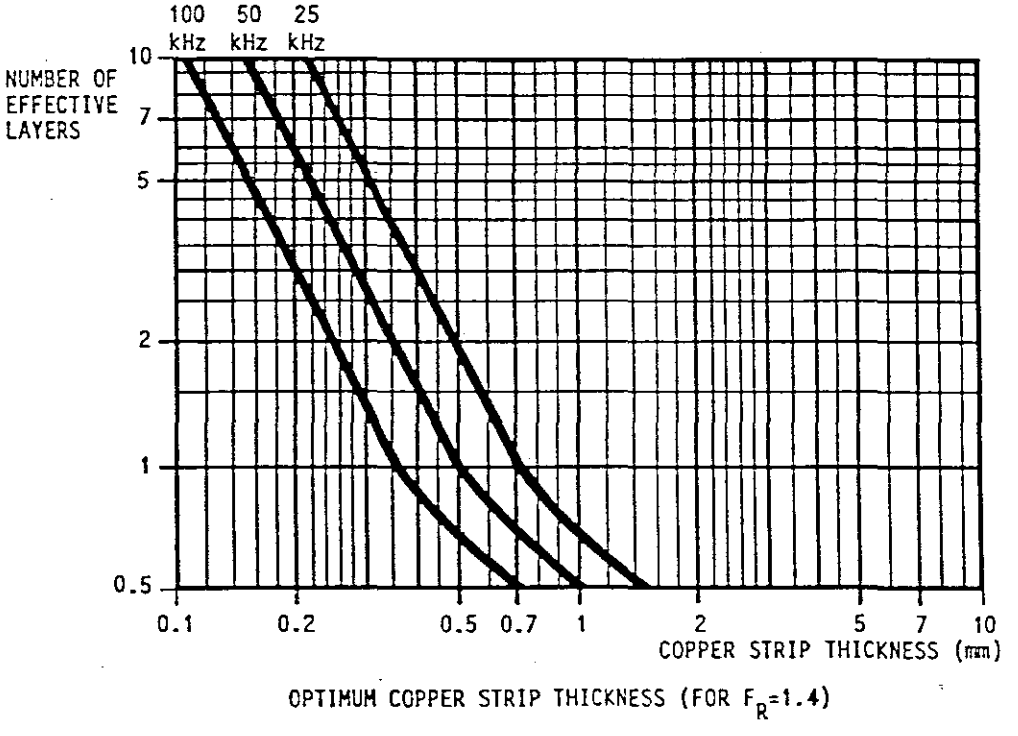


Figure G.2 The optimum copper strip thickness h for an F_R ratio of 1.5 (Mullard Ltd.).

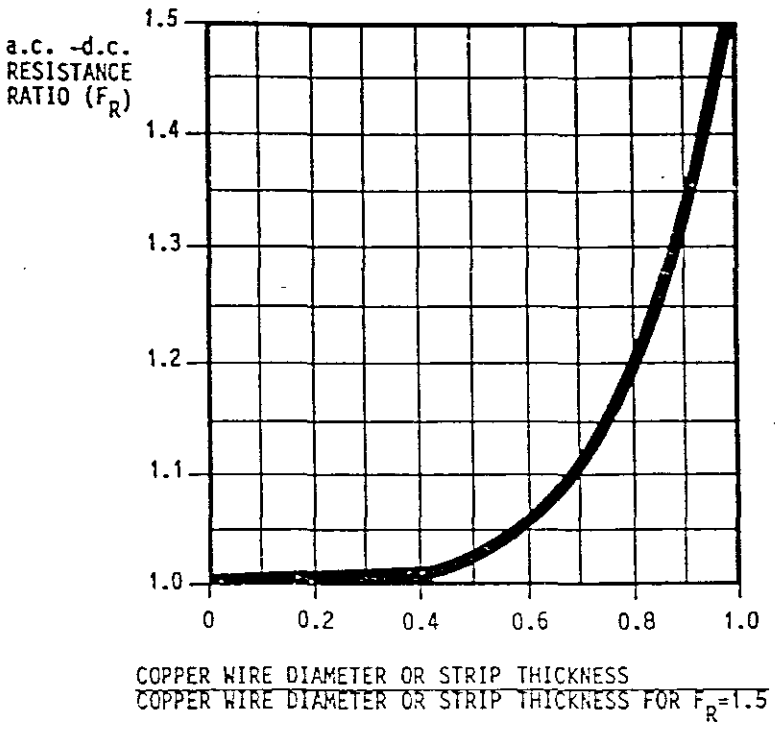


Figure G.3 The corrected F_R ratio for wires below the optimum thickness (Mullard Ltd.).

APPENDIX H

TEMPERATURE RISE VERSUS SURFACE DISSIPATION

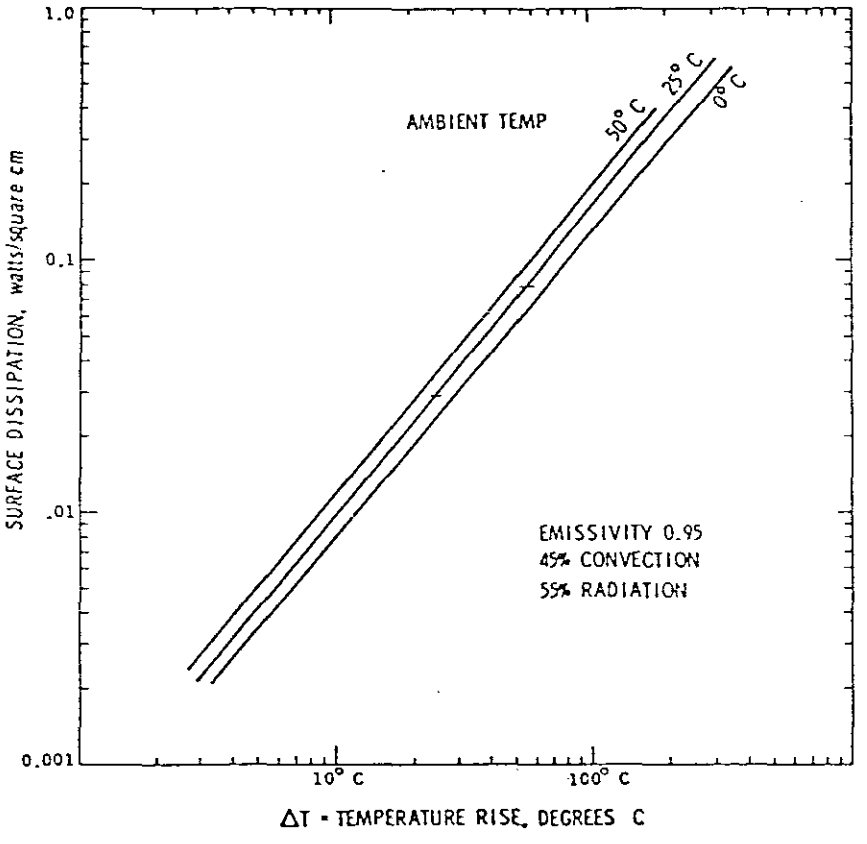


Figure H.1 Temperature rise versus surface dissipation (abstract from [7]).

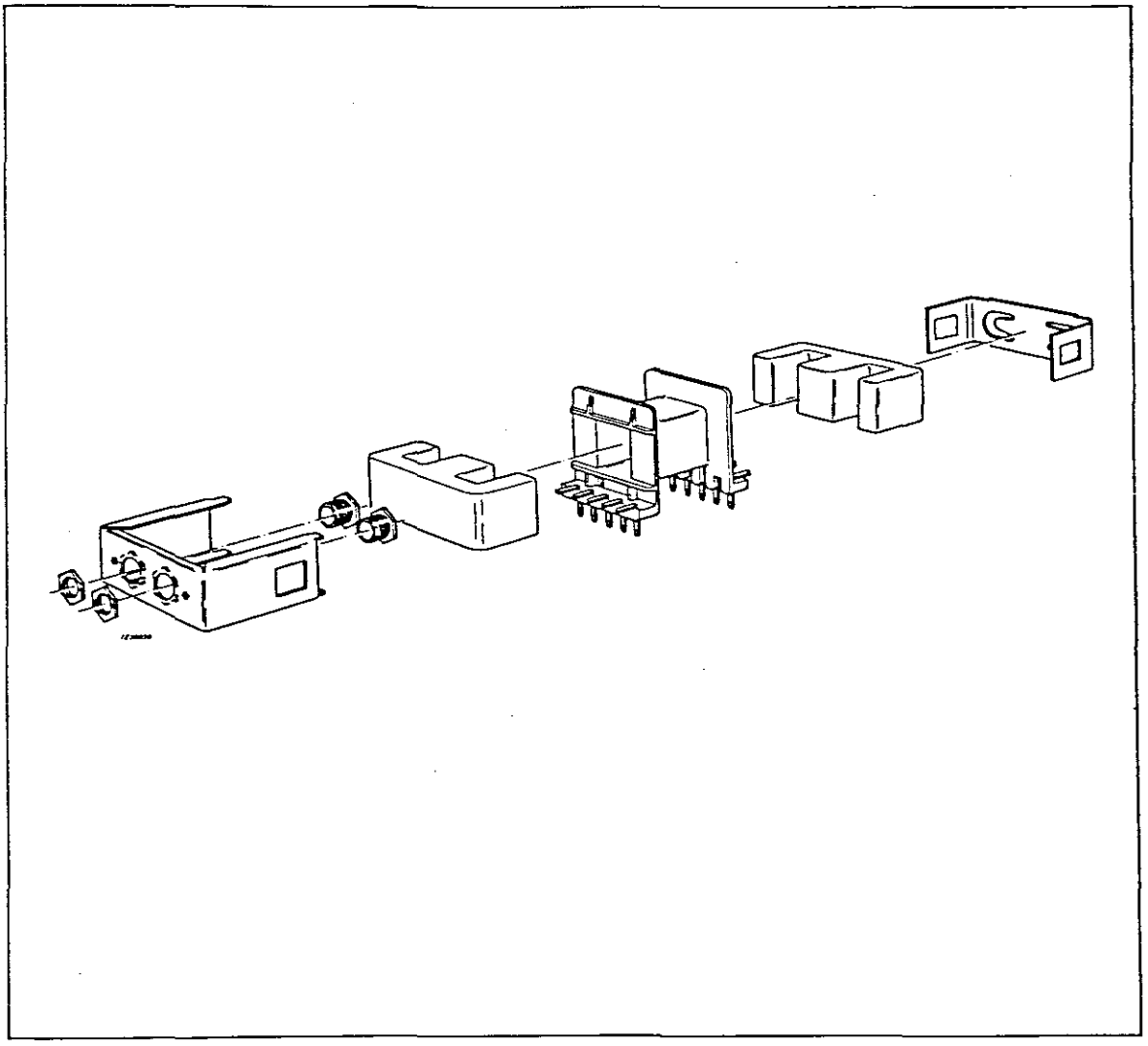
APPENDIX I

THE DATA SHEET FOR THE E20/10/5 FERRITE CORE

Philips Components

Data sheet	
status	Product specification
date of issue	August 1990

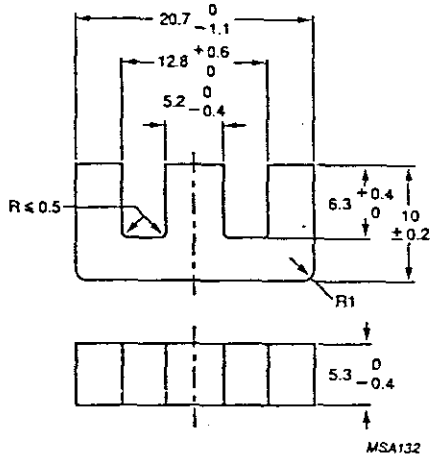
E20/10/5 to E65/32/27
E cores and accessories
EF12.6/7/4 to EF32/16/9
EF cores and accessories



(Abstract from [13])

E cores and accessories

E20/10/5



Dimensions in mm

Fig.1 E20/10/5 core half.

EFFECTIVE CORE PARAMETERS

SYMBOL	PARAMETER	VALUE	UNIT
$\Sigma(l/A)$	core factor (C1)	1.37	mm^{-1}
V_e	effective volume	1340	mm^3
l_e	effective length	42.8	mm
A_e	effective area	31.2	mm^2
A_{min}	minimum area	25.5	mm^2
	mass of core half	≈ 4	g

CORE HALVES

GRADE	AIRGAP (μm)	A_L* (nH)	μ_e	ORDERING CODE
3C80	= 0	1300 ± 25%	≈ 1430	4312 020 3407
	50	≈ 460	≈ 510	4312 020 3536
	150	≈ 210	≈ 230	4312 020 3537
	500	≈ 85	≈ 100	4312 020 4538
3C85	≈ 0	1300 ± 25%	≈ 1430	4312 020 4539
	50	≈ 460	≈ 510	4312 020 4540
	150	≈ 210	≈ 230	4312 020 4541
	500	≈ 85	≈ 100	4312 020 4542
3F3	= 0	1150 ± 25%	≈ 1270	4312 020 4552
	50	≈ 450	≈ 510	4312 020 4578
	150	≈ 210	≈ 230	4312 020 4579
	500	≈ 85	≈ 100	4312 020 4580
3C11	= 0	2600 ± 25%	≈ 2850	4312 020 3597

* measured in combination with an ungapped core half, clamping force 20 ± 10 N

PROPERTIES OF CORE SETS UNDER POWER CONDITIONS

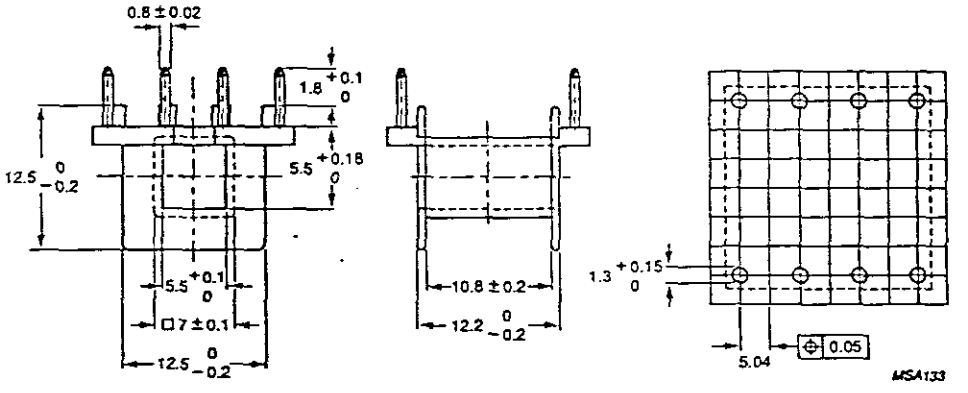
GRADE	B (mT) at H = 250 A/m; f = 25 kHz; T = 100 °C	P_V (W) at f = 25 kHz; $\hat{B}$ = 200 mT; T = 100 °C	P_V (W) at f = 100 kHz; $\hat{B}$ = 100 mT; T = 100 °C	P_V (W) at f = 400 kHz; $\hat{B}$ = 50 mT; T = 100 °C
3C80	≥ 320	≤ 0.50	-	-
3C85	≥ 320	≤ 0.25	≤ 0.27	-
3F3	≥ 320	-	≤ 0.15	≤ 0.25

August 1990

E cores and accessories — E20/10/5

COIL FORMER DATA

Coil former material:	phenolformaldehyde (PF), glass reinforced, flame retardent in accordance with UL 94V-0
Pin material:	CuSn, SnPb plated
Maximum operating temperature:	180 °C
Resistance to soldering heat:	430 °C, 2 s
Solderability:	IEC 68-2-20, Part 2, Test TA, method 1



Dimensions in mm

Fig.2 E20/10/5 coil former.

WINDING DATA

NUMBER OF SECTIONS	NUMBER OF PINS	WINDING AREA (mm^2)	WINDING WIDTH (mm)	WINDING LENGTH (mm)	ORDERING CODE
1	8	27	10.6	38	4322 021 2024

Material grade specification — 3E1

SYMBOL	CONDITIONS	VALUE	UNIT
μ_i	≤ 10 kHz, 0.1 mT, 25 °C	3800 ± 20%	
B	10 kHz, 250 A/m, 25 °C	≈ 350	mT
	10 kHz, 250 A/m, 100 °C	≈ 200	mT
$\tan\delta/\mu_i$	100 kHz, 0.1 mT, 25 °C	$\leq 20.10^{-6}$	
	300 kHz, 0.1 mT, 25 °C	$\leq 150.10^{-6}$	
η_B	10 kHz, 1.5 - 3 mT, 25 °C	$\leq 1.2.10^{-3}$	T^{-1}
D_F	10 kHz, 0.1 mT, 25 °C	$\leq 5.10^{-6}$	
ρ	DC, 25 °C	≈ 1	Ωm
T_c		≥ 125	°C
density		≈ 4800	kg/m^3

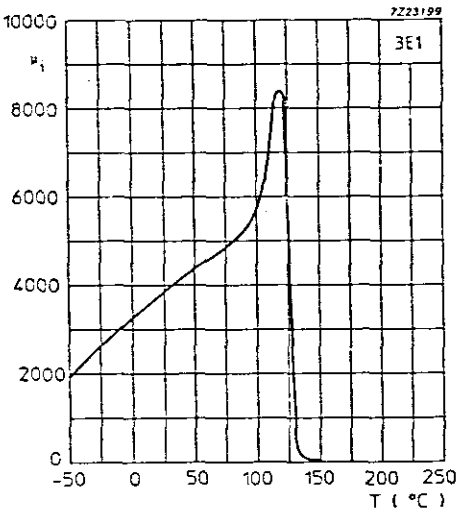


Fig.2 Initial permeability as a function of temperature.

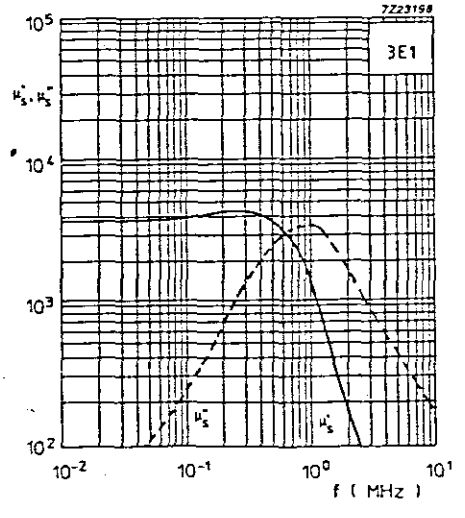


Fig.1 Complex permeability as a function of frequency.

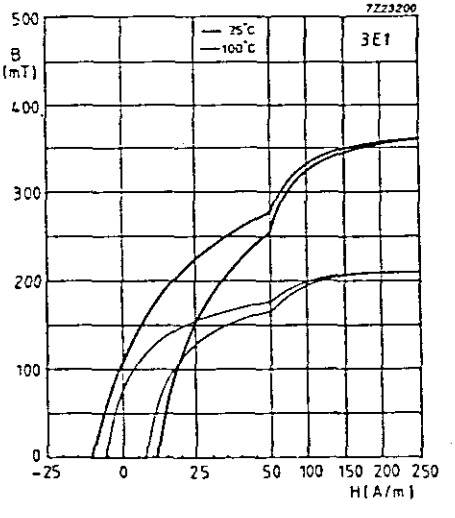


Fig.3 Typical B-H loops.

Material grade specification 3E1

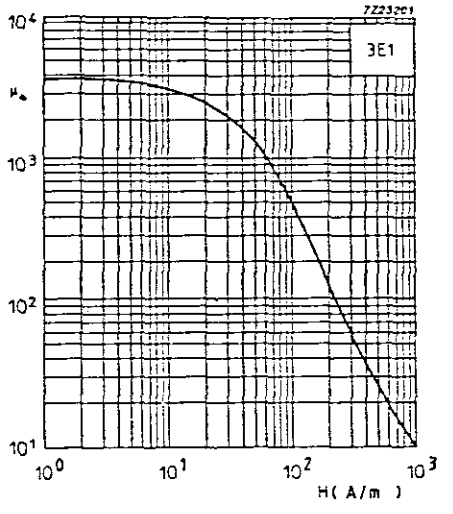
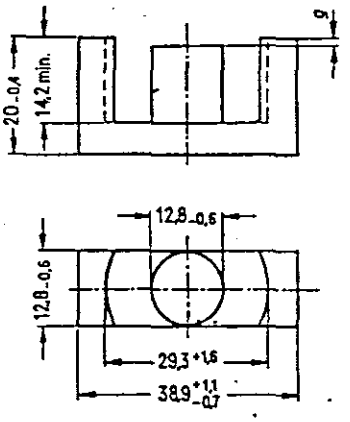


Fig.4 Incremental permeability as a function of magnetic field strength.

APPENDIX J

THE DATA SHEET FOR THE ETD 39/20/13 FERRITE CORE

ETD cores are intended for SMPS transformer design with optimum weight-referred power at small volume.



Dimensions in mm

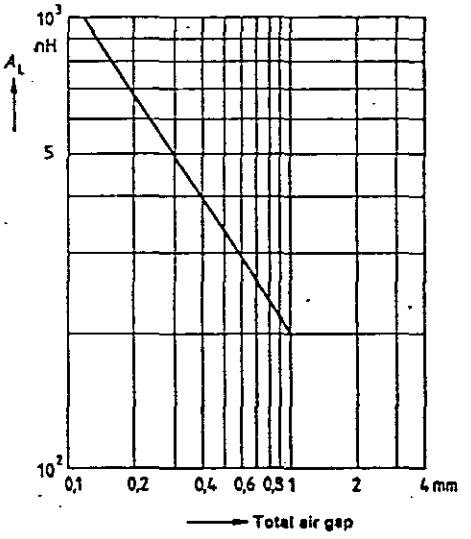
Magnetic characteristics (per set)

Core factor	$\Sigma l/A$ =	0.74	mm^{-1}
Effective area	A_e =	125	mm^2
Min. core cross-section[1]	A_{min} =	123	mm^2
Effective length	l_e =	92.2	mm
Effective volume	V_e =	11500	mm^3

Approx. weight 30 g/item

A_L value versus total air gap
for a set consisting of

1 core B66363-G-X1*7 (*g* appr. 0) and
1 core B66363-G... (*g* > 0)
or
2 cores B66363-G... (*g* > 0)



ETD cores are delivered individually and according to dimension "g" (shortened center leg). Dimension "g" applies to a core set comprising one core with "g" approximately 0 and one core with shortened center leg.

Ferrite *material*	Dimension "g" mm	tolerance mm	A_L value[2] (approx.) nH	Effective *permeability* (approx.) μ_e	Ordering code *(PU: 200 items)*	
N27	appr.0	–	2700	1590	B66363-G-X127	S
N67	appr.0	–	2800	1650	B66363-G-X167	
N27	0,1	±0,02	1050	618	B66363-G100-X127	
	0,2	±0,03	660	389	B66363-G200-X127	
	0,5	±0,05	340	200	B66363-G500-X127	S
	1,0	±0,1	200	118	B66363-G1000-X127	S
N67	0,5	±0,05	340	200	B66363-G500-X167	
	1,0	±0,1	200	118	B66363-G1000-X167	

For power loss P_v and amplitude permeability μ_a refer to page 461.

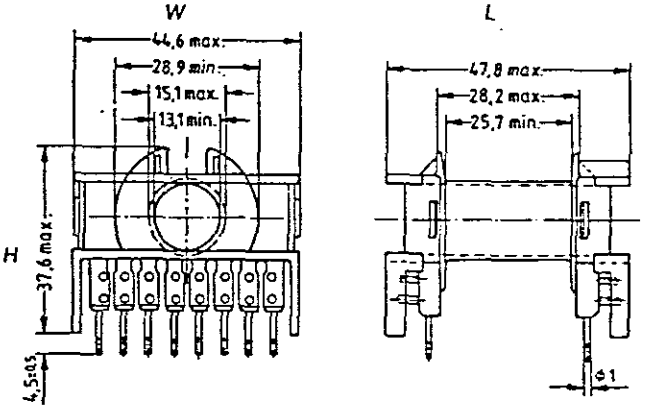
[1] Required to calculate the max. flux density [2] Measuring temperature 25 °C, measuring flux density $\hat{B} \leq 1$ mT
S Preferred products (refer to page 4)

(Abstract from [17])

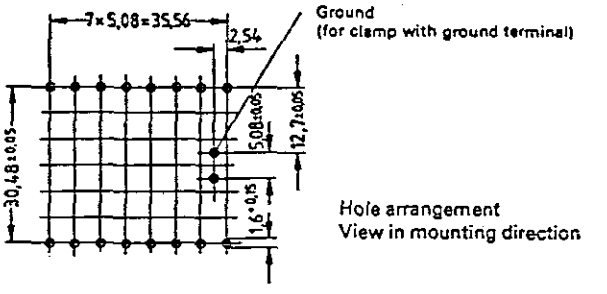
Coil former B 66364

Glass-fiber reinforced polyterephthalate coil former, flame-retardant in accordance with UL 94 V-0. Available with 16 solder terminals, also suitable for automatic winding.

For solderability of terminal pins refer to page 89. For winding details refer to page 77.



Built-in dimensions for the transformer (approx.)
L = 48 mm
W = 45 mm
H = 38 mm



Hole arrangement
View in mounting direction

Dimensions in mm

Number of sections	Useful winding cross section A_N mm²	Average length of turn l_N mm	A_R value[1] µΩ	Approx. weight g	Ordering code (PU: 100)
1	178	69	13,3	18	B66364-A1016-T1 S

[1] $R_{Cu} = A_R \cdot N^2$ (dc resistance = A_R · number of turns²)

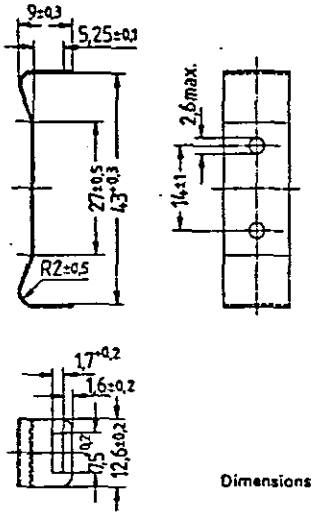
S Preferred products (refer to page 4)

Mounting assembly and clamp with ground terminal B 66364

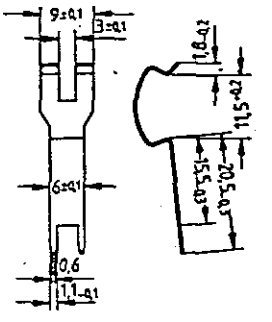
The mounting assembly comprises two stainless steel yokes.

Clamp with ground terminal *made of 0.4 mm thick nickel silver incl. tinned ground pins;* necessary if the core must be grounded. It can be plugged upon the core, thus comprising both core halves.

Yoke



Clamp with ground terminal



Dimensions in mm

	Ordering code	PU: items
Yoke (ordering code for individual yoke; 2 are required)	B66364–A2000 ◙	200
Clamp with ground terminal	B66364–A2001	100
Sealing can	upon request	

◙ Preferred products (refer to page 4)

APPENDIX K

CENTERING THE -5V AUXILIARY OUTPUT

CENTERING THE -5V AUXILIARY OUTPUT

With the completion of the prototype, it was found that the -5 volt auxiliary output voltage was too high (-12.5 V) at a duty cycle of approximately 30%. This is unacceptable.

Since the duty cycle (pulse width) is determined by the closed-loop regulated +5 volt output, the pulse width cannot be reduced to correct for the error in voltage, without reducing the regulated output voltage itself.

To solve the problem saturable reactors were included into the -5 volt output (Figure K.1), providing enough delay to reduce the pulse width to the -5 volt output, so that the error in voltage was cancelled.

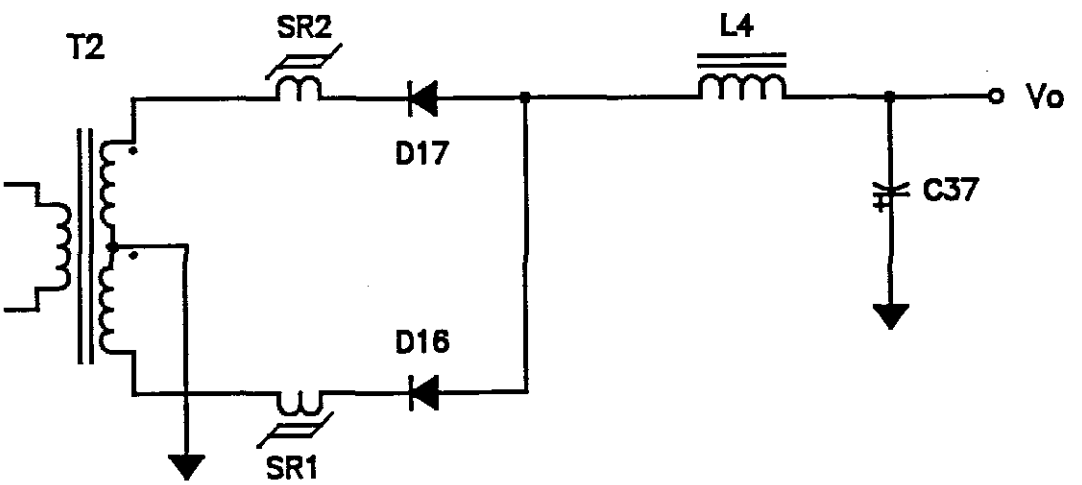


Figure K.1 Saturable reactors applied to the -5 volt output.

The design of the saturable reactor:

From [3] follows that the required time delay period t_d will be

$$t_d = t_{on} - \frac{V_{o(req)}\ t_{on}}{V_{o(actual)}} \quad (\mu s) \qquad \text{(K-1)}$$

where

t_d - required time delay period, μs

t_{on} - conducting "on" time period, μs

$V_{o(req)}$ - required output voltage, V

$V_{o(actual)}$ - actual output voltage, V

Substituting

$$t_d = 1.5 - \frac{5 \times 1.5}{12.5}$$

$$t_d = 0.9\ \mu s$$

One of the requirements for a saturable reactor is for the core material to have a near-square magnetisation characteristic (square loop material). To satisfy the requirement a 3R1 ferrite material from Philips is used.

The number of turns which will provide the calculated time delay t_d is calculated from [3] using equation (K-2).

$$N = \frac{V_s \, t_d \, 10^4}{\Delta B \, A_e} \qquad \text{(K-2)}$$

Where

N - number of turns

V_s - secondary voltage, V

t_d - required time delay period, s

ΔB - flux density swing, T

A_e - effective core cross-sectional area, cm^2

The selected saturable reactor toroid has the following specifications from [13]:

Size : 14 × 9 × 5

Material : 3R1

A_e : 0.123 cm^2

with

V_s = 40 V (measured) and

ΔB = 0.1 T (selected)

Substituting into equation (K-2)

$$N = \frac{40 \times 0.9 \times 10^{-6} \times 10^4}{0.1 \times 0.123}$$

$$N = 29.27 \; T$$

Selected N = 30 T of AWG # 24.

The core and copper losses may be neglected.

The error in voltage has been successfully cancelled bringing the -5 volt output back to normal.

This concludes the design for the saturable reactor.