Cape Peninsula
University of Technology

# DESIGN OF A HIGH EFFICIENCY *S*-BAND POWER AMPLIFIER FOR A CUBESAT

**by**

**MOISE SAFARI MUGISHO**

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**at the**

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**Supervisor: Mr. Clive Whaits**
**Co-supervisor: Dr. Gérard Orjubin**

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# Declaration

I, MOISE SAFARI MUGISHO, declare that the contents of this thesis represent my own unaided work and that the thesis has not previously been submitted for academic examination towards any qualification. Furthermore, it represents my own opinions and not necessarily those of the Cape Peninsula University of Technology.

**Signed** **Date**

# Abstract

In all radio frequency (RF) electronic communication systems, power amplifiers (PAs) are used to generate the final transmitted signal. Specifically, these PAs are used to increase the output power of the transmitted signal. The PA accomplishes this by converting the applied direct current (DC) power to the PA into RF power, while being driven by a RF input signal. The portion of DC power that is not converted into RF power is dissipated as heat. The power conversion mechanism that takes place in a PA is described by the power conversion efficiency (*PE*) and the power added efficiency (*PAE*).

A CubeSat is a small satellite in the shape of a 10 × 10 × 10 cm cube, weighing less than 1 kg and contains a RF electronic communication system which allows communication with the satellite. A CubeSat requires a PA with high *PE* in order to increase the lifetime of the on-board battery, facilitate thermal management on-board the satellite, increase system reliability, and reduce the size and manufacturing cost of the satellite.

To maximize the theoretical *PE* of a RF PA, several design techniques and classes of operation were investigated, the basis of which lies in the fulfilment of the necessary and sufficient conditions for a maximum *PE*. A PA, which uses the Class-$F^{-1}$ (inverse Class-F) mode of operation, fulfils the necessary and sufficient conditions for a maximum theoretical *PE*, and therefore presents itself as a good option for a high efficiency PA.

This thesis presents the design of a Class-$F^{-1}$ PA, using the Cree CGH40010F GaN power active device. An optimum output matching network is used to terminate the drain of the GaN power active device with the required load impedances at the fundamental, $2^{nd}$ and $3^{rd}$ harmonic frequencies of operation. The designed PA delivers a maximum *PE* of 95 % at an operating frequency of 2.2 GHz, a maximum *PAE* of 82 % at an operating frequency of 2.2 GHz and a maximum output power of 40.6 dBm at an operating frequency of 2.2 GHz.

# Acknowledgements

First and foremost, I would like to thank my Lord and saviour, Jesus Christ, for all that he is for me and has been for me during the completion of this research. He is all I have, all I have ever wanted and all that I need.

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Opinions expressed in this thesis and the conclusions arrived at, are those of the author, and are not necessarily to be attributed to the National Research Foundation.

Last but not least, my sincere gratitude goes to the Zanga family, the Mputu family and the Panzu family for welcoming me into their homes as a friend, a brother, an uncle and a son.

# Dedication

I dedicate this thesis to my beloved dad, Mr. SAFARI CÔME CHAMBA KASENGO. May you find in the work presented in this thesis one of the fruits of your career and may you have a peaceful and healthy retirement.

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# Abbreviations and Acronyms

| | |
|---|---|
| ADS: | Advanced Design System |
| ACLR: | Adjacent Channel Leakage Ratio |
| ACPR: | Adjacent Channel Power Ratio |
| BJT: | Bipolar Junction Transistor |
| C/I: | Carrier-to-Intermodulation |
| CMCD: | Current-Mode Class-D |
| CPUT: | Cape Peninsula University of Technology |
| DC: | Direct Current |
| DQPSK: | Differential Quadrature Phase-Shift Keying |
| EVM: | Error Vector Magnitude |
| F'SATI: | French South African Institute of Technology |
| FSK: | Frequency Shift Keying |
| GaAsMESFET: | Gallium Arsenide Metal Semiconductor Field Effect Transistor |
| GaN: | Gallium Nitride |
| GMSK: | Gaussian minimum shift keying |
| HBT: | Heterojunction Bipolar Transistor |
| HEMT: | High Electron Mobility Transistor |
| HFET: | Heterojunction Field Effect Transistor |
| InP: | Indium Phosphide |
| $IP_{1dB}$: | Input Power at 1 dB compression point |
| $IP3_{in}$: | Third order Input Power level |
| $IP3_{out}$: | Third order Output Power level |
| JFET: | Junction Field Effect Transistor |
| LDMOS: | Laterally Diffused Metal Oxide Semiconductor |
| LEO: | Low Earth Orbit. |
| MOSFET: | Metal Oxide Semiconductor Field Effect Transistor |
| NPR: | Noise Power Ratio |
| $OP_{1dB}$: | Output Power at 1 dB compression point |

| | |
|---|---|
| PA: | Power Amplifier |
| *PAE*: | Power Added Efficiency |
| PCB: | Printed Circuit Board |
| *PE*: | Power Conversion Efficiency |
| pHEMT: | pseudomorphic High Electron Mobility Transistor |
| QPSK: | Quadrature Phase Shift Keying |
| RHP: | Right Hand Plane |
| RCA: | Radio Corporation of America |
| RF: | Radio Frequency |
| SiC: | Silicon Carbide |
| STX: | *S*-band Transmitter |
| VMCD: | Voltage-Mode Class-D |

# Chapter 1

# Introduction

This introductory Chapter presents the reasons for which the author, in accordance with the French South African Institute of Technology (F'SATI) program, has decided to carry out the research presented in this thesis. The objectives of the research are presented as well as the methodology to achieve these objectives. RF power amplification is a wide field of research and, to delimit the scope of this research, the focus area for this specific topic is presented in this Chapter. The organisation of this document is also presented to facilitate the reading thereof.

## 1.1. Motivation

A CubeSat is a small satellite in the shape of a 10 × 10 × 10 centimetre cube, weighing less than 1 kilogram. A CubeSat has a mission lifetime of less than 2 years in a low earth orbit (LEO). A CubeSat consists of different subsystems, each performing a specific task (Andrew & Christopher, 2012: 1).

CubeSats use solar panels and Li-Ion batteries for their direct current (DC) power requirements. However, the restricted surface area of a CubeSat limits the amount of solar power that may be generated. The restricted space and the designated weight of the CubeSat impose the use of small batteries. These facts lead to stringent DC power constraints in CubeSats, which are critical to the design and operation of the communication subsystem of the CubeSat.

The communication subsystem of the CubeSat is one of the most power-consuming of all subsystems. This is due to the necessity of having a power amplifier (PA) in the final stage of the transmitter of the communication subsystem.

PAs are used to amplify the transmitted signal. This amplification is achieved at the cost of significant DC power dissipation, resulting in the waste of useful energy.

PAs are used in a wide range of applications, such as jamming, imaging, RF heating, plasma generation, laser drivers, magnetic-resonance, miniature DC to DC converters as well as CubeSats (Raab *et al*., 2002: 814-816).

This research proposes a method of minimizing DC power dissipation in CubeSats while maximizing the amplification of the transmitted signal.

The first ever African CubeSat, ZACUBE-1 (TshepisoSat), which was developed at the Cape Peninsula University of Technology (CPUT) under the F'SATI program, was launched in 2013. The second CubeSat, ZACUBE-2 is under development at F'SATI and will use a 2 W *S*-band transmitter (STX) built by the F'SATI development team as part of its communication subsystem. However, the STX uses an off the shelf PA with a power conversion efficiency (*PE*) of 25 %. This means that for a power consumption of 8 W DC, ZACUBE-2 will be transmitting a 2 W RF signal. Thus, only 25 % of the DC power is converted into useful RF power and 75 % of the DC power is dissipated as heat. Knowing that CubeSats have limited DC power, losing 75 % of this power constitutes a major problem and negatively impacts on the battery life on the CubeSat. Also, the 75 % of DC power dissipated as heat means that a complex thermal management system is required to ensure that the heat generated due to the dissipation of power does not damage other subsystems within the CubeSat. Moreover, CubeSats have limited space due to their small size, hence the difficulty to accommodate such a PA system.

## 1.2. Objectives

The objectives of the research presented in this dissertation are as follows:

Main objective:

- To design, develop, build and test a high efficiency *S*-band PA for ZACUBE-2.

Subsidiary objectives:

- To study and review the PAs in general.
- Select the optimum topology for a PA suitable for use in a CubeSat.
- To evaluate the performance of the built PA relative to existing PAs.

## 1.3. Research Methodology

- Determine the efficiency of the existing PA used in the STX on-board ZACUBE-1.
- Conduct a literature study on the maximum obtainable efficiency in existing PAs.
- Investigate existing solutions, that is, existing PAs used in CubeSats
- Investigate available PA design techniques, and select the most suitable topology for use in the design of the PA.
- Investigate available RF power transistors and their suitability for applications in space.
- Define the specifications of the PA to be designed.
- Select the appropriate RF power transistor.
- Design and simulate the PA in ADS.
- Construct and test the designed PA
- Measure the efficiency and output power of the constructed PA.
- Compare the measured results and the simulated results.
- Compare the performance of the constructed PA to the defined specifications.

## 1.4. Delineation

In modern RF transmitters, the input drive signal to a PA is a modulated signal, which is generated by shifting or keying the amplitude, frequency or phase of an analogue carrier signal in accordance with the message signal.

It is important that the PA, which is the last stage in a transmitter, does not distort the modulated signal, thus the need for linear amplification. However, a higher *PE* is obtained by driving the active device of the PA into its non-linear region of operation. In the design of a PA, the techniques implemented to achieve good linearity and high *PE* are mutually exclusive. The modulation scheme used and the particular application of the PA determine the required trade-off that must be implemented to achieve reasonable linearity and good *PE*.

According to Cripps (2006:133), applications using modulation schemes such as FSK, GMSK, QPSK and DQPSK can tolerate significant amplitude distortion and thus the linearity of the PA can be traded for a higher *PE*.

Since a QPSK modulation scheme will be used in the transmitter of ZACUBE-2, the linearity of the PA will not be a major design goal in the design and performance of the PA.

## 1.5. Synopsis

In Chapter 2, an overview of RF PAs is presented, the performance parameters, classes of PAs, design techniques, and RF power device technology are briefly described. A mathematical condition for achieving 100 % theoretical *PE* is presented.

In Chapter 3, the Class-F and inverse Class-F (Class-$F^{-1}$) PAs are discussed in more detail, the operational conditions for the Class-F and Class-$F^{-1}$ are mathematically described, a comparison between the Class-F and Class-$F^{-1}$ PA is made and an alternative topology of wave-shaping network that meets the defined operational conditions is proposed.

Chapter 4 presents the different steps involved in the design of a Class-$F^{-1}$ PA using the proposed topology of wave-shaping network. The simulated performance parameters of the designed Class-$F^{-1}$, the layout of the printed circuit board (PCB), the electromagnetic simulations and optimization are presented in Chapter 4.

Chapter 5 presents the construction of the PA, the procedure involved, and the measured performance parameters are discussed in detail, with an emphasis on efficiency. Comparisons between simulated, measured and specified performance parameters are made.

In Chapter 6, conclusions and recommendations are made and future work proposals are presented.

## 1.6. Conclusions

CubeSats require a PA with high *PE* in order to increase battery lifetime, to facilitate optimal thermal management, to increase reliability, and to reduce the physical size and manufacturing cost thereof. Such PAs can be designed by carefully selecting a suitable design technique and active device. Based on the available active devices and using the appropriate design techniques, it is possible to design such a PA.

# Chapter 2

# Overview of RF Power Amplifiers

## 2.1. History of RF Power Amplification

Since the 19th century, RF power was generated by a spark, an arc and commutator action. The invention of the Deforest audion in 1907 enabled power amplification of electrical signals. This made wireless radio communication practicable as it offered a means of generating and controlling RF signals (Raab *et al*., 2002: 814).

In the late 1960s, discrete solid state RF power devices such as the 2N6093 silicon power transistor (active device) were introduced by the Radio Corporation of America (RCA) (Raab *et al*., 2002: 814).

The development of new materials such as, indium phosphide (InP), silicon carbide (SiC) and gallium nitride (GaN), enabled the development of new solid state RF power devices. Examples are the high electron mobility transistor (HEMT), the pseudomorphic high electron mobility transistor (pHEMT), the heterojunction field effect transistor (HFET) and the heterojunction bipolar transistor (HBT), with the ability of amplifying signals at 100 GHz or more in the late 1990s (Raab *et al*., 2002: 8).

## 2.2. Theory of Operation

A PA is an electronic circuit that is used in the final stage of a transmitter to increase the power of the transmitted signal. The PA accomplishes this by converting DC power into RF power while being driven by a RF input signal. The portion of DC power that is not converted into RF power is dissipated as heat and constitutes a loss of power. The power conversion mechanism that takes place in a PA is described by the power conversion efficiency (*PE*) and the power added efficiency (*PAE*) (Pozar, 2012: 596; Colantonio *et al.*, 2009: 179; Prodanov & Banu, 2007: 350).

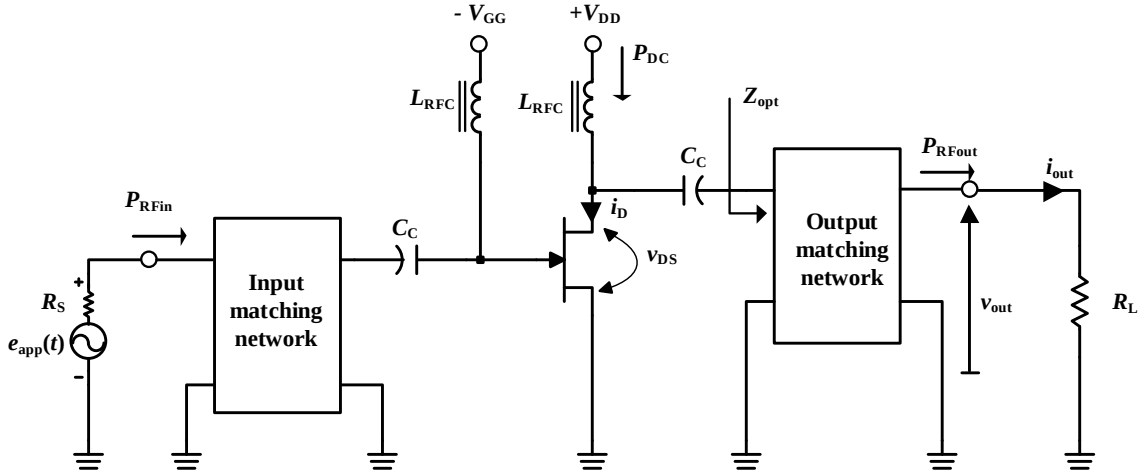



**Figure 1: Basic circuit diagram of a power amplifier (Adapted from Colantonio *et al.*, 2009: 179)**

The basic circuit diagram of an ideal PA is shown in Figure 1, where an RF choke $L_{RFC}$ presents a low impedance path (short circuit) to the DC signal and a high impedance path (open circuit) to the RF signal. A coupling capacitor $C_C$ presents a high impedance path (open circuit) to the DC signal and a low impedance path (short circuit) to the RF signal. The active device is driven by an RF source delivering an input power ($P_{RFin}$) through the input matching network and the DC power ($P_{DC}$) from the DC biasing circuit is converted into RF output power ($P_{RFout}$) at the fundamental frequency.

## 2.3. Performance Parameters of a RF Power Amplifier

The operation of a RF PA is characterised by the following performance parameters:

### 2.3.1. Power Conversion Efficiency

The power conversion efficiency is the percentage of the DC power that is converted into useful RF output signal power. It is additionally referred to as the drain efficiency or the collector efficiency (Prodanov & Banu, 2007: 351-352), and is given by:

$$PE = \frac{P_{RFout}}{P_{DC}} \tag{1}$$

In a CubeSat, the PA is the primary consumer of DC power, thus, the *PE* is one of the most important performance parameters of the PA. A higher *PE* leads to longer battery lifetime, simple thermal management requirements, and a small size of PA for CubeSats (Hasani & Mahmoud, 2008: 1759; Moon *et al*. 2012: 1937; Pozar, 2012: 597).

### 2.3.2. Power Added Efficiency

The power added efficiency is the percentage of DC power that is converted into useful RF output signal power, taking into account the effect of the RF input signal or drive signal. For larger gain PAs, the *PAE* approaches the *PE* (Prodanov & Banu, 2007: 351-352; Pozar, 2012: 597). The *PAE* is given by:

$$PAE = \frac{P_{RFout} - P_{RFin}}{P_{DC}} \tag{2}$$

### 2.3.3. Output Power

Colantonio *et al*., *(*2009:2-3), states that the output power of a PA is the power delivered to the load at a specific frequency or in a frequency band and expressed as:

$$P_{RFout}(f) = \frac{1}{2}\mathrm{Re}\{V_{out}I_{out}^{*}\} \quad \text{W} \tag{3}$$

The power level of a PA is expressed in logarithmic units, assuming 1 mW as the reference level, the actual power level is expressed in decibels relative to 1 mW that is, in dBm.

$$P_{dBm} = 10\ \log_{10}\left(\frac{P}{1\ \text{mW}}\right) = 10\ \log_{10}(P_{mW}) = 10\ \log_{10}(P_{W}) + 30 \tag{4}$$

As the PA is driven into saturation, the output voltage and output current swing allowed by the active device is limited by the non-linear behaviour of that active device and the output power reduces to its saturated value (Colantonio *et al*., 2009:2-3), given by:

$$P_{\text{sat}}(f) = \lim_{P_{\text{RFin}} \to \infty} [P_{\text{RFout}}(f)] \tag{5}$$

### 2.3.4. Power Gain

The power gain of a PA is the amount by which the power level of the input signal has been amplified (Pozar, 2012: 597; Colantonio *et al*., 2009:2-3) and is given by:

$$G(f) = \frac{P_{\text{RFout}}(f)}{P_{\text{RFin}}(f)} \tag{6}$$

Due to the nonlinear behaviour of the active device used in a PA, the power gain depends on the power level of the input signal. For a low power level input signal, the active device of the PA operates in its linear region and the corresponding gain is referred to as small signal or linear gain (Colantonio *et al*., 2009:2-3) and is given by:

$$G_{\text{L}}(f) = \lim_{P_{\text{RFin}} \to 0} [G(f)] \tag{7}$$

As the PA is driven into compression, the output power tends to saturate and the corresponding gain approaches zero (Colantonio *et al*., 2009:2-3). This is mathematically described by:

$$\lim_{P_{\text{RFin}} \to \infty} [G(f)] = 0 \tag{8}$$

The power gain expressed in dB is given by:

$$G_{\text{dB}} = 10 \log_{10}(G) = P_{\text{RFout, dBm}} - P_{\text{RFin, dBm}} \tag{9}$$

### 2.3.5. Linearity

The Linearity of a PA specifies the degree of similarity between the input signal and the output signal of the PA, hence it constitutes one of the main design goals in a modern PA. In CubeSats the linearity requirements depend on the modulation technique that is used in the transmitter (Cripps, 2006:17-37).

According to Raab *et al*., (2002: 814-815), for a given application, the linearity of a PA is characterised, designated and quantified by the adjacent channel power ratio (ACPR), the gain compression, the third order intercept point ($IP_3$), the carrier-to-intermodulation ratio (C/I Ratio) and the error vector magnitude (EVM):

### 2.3.5.1. Adjacent Channel Power Ratio

The ACPR is a measure of how much of the spectral power of the transmitted signal has leaked into the adjacent channel due to the nonlinear behaviour of the PA. It is also referred to as adjacent channel leakage ratio (ACLR) (Colantonio *et al*., 2009:15-16-17) and is given by:

$$ACPR \triangleq \frac{P_{\text{in band}}}{P_{\text{in adjacent channels}}} \tag{10}$$

### 2.3.5.2. Gain Compression

Gain compression refers to the decrease of the power gain of a PA from its linear value as the PA is driven into compression by an increase in the power level of the input signal. A commonly used Figure of merit to quantify gain compression is the 1 dB compression point ($P_{1dB}$) which is the level at which the output power has decreased by 1 dB from the ideal linear characteristic. This $P_{1dB}$ point can be stated with reference to the input power ($IP_{1dB}$) or the output power ($OP_{1dB}$) (Pozar, 2012: 511-513; Colantonio *et al*., 2009:3-4; MacPherson & Whaits, 2007: 2-6).

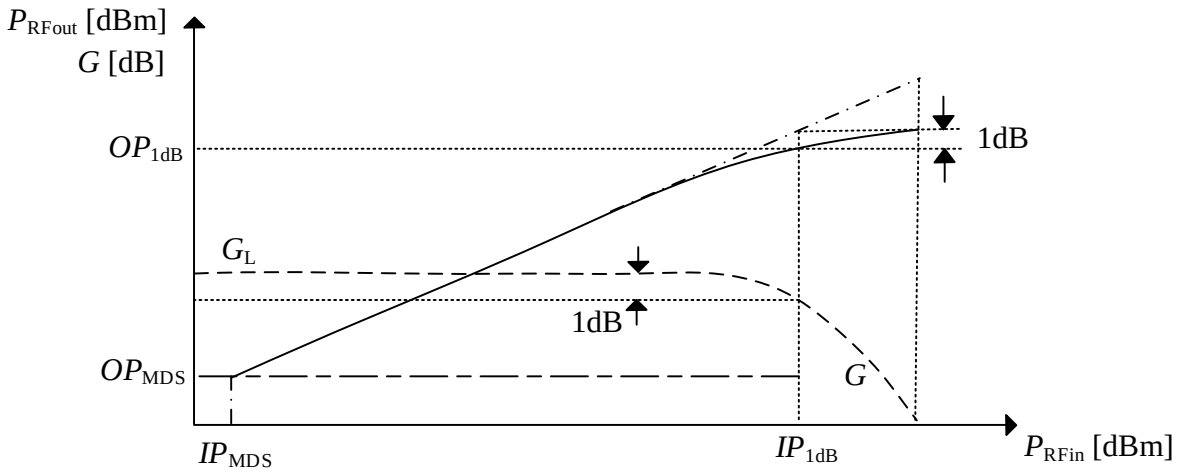



**Figure 2: 1 dB compression point (Adapted from Colantonio *et al*., 2009: 3)**

The $OP_{1dB}$ is given by:

$$OP_{1dB} = (G - 1\text{dB}) + IP_{1dB} \qquad \text{dBm} \tag{11}$$

### 2.3.5.3. Third-Order Intercept Point

The third order intercept point is a hypothetical intersection point where the third order output ($IP3_{out}$) or the input ($IP3_{in}$) power level is equal to the ideal linear output power level or the first order power level of a PA (Pozar, 2012: 513-515; Colantonio *et al*., 2009:13; MacPherson & Whaits, 2007: 2-6).

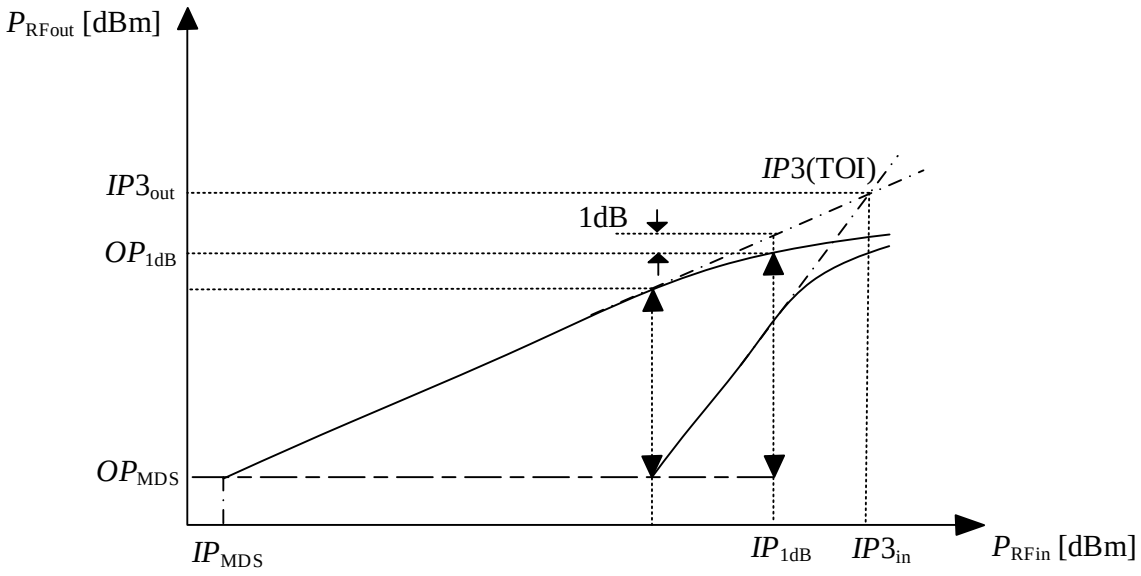



**Figure 3: Third order intercept point (Adapted from Colantonio *et al*., 2009: 13)**

### 2.3.5.4. Carrier-to-Intermodulation Ratio

The C/I ratio is a measure of the useful output power level relative to the power level of the intermodulation products, measured in decibel below the carrier dBc (Colantonio *et al*., 2009:14-15) and is given by:

$$C/I \triangleq 2\,(IP3_{out} - P_{RFout,\,dBm}) \qquad \text{dBc} \tag{12}$$

### 2.3.5.5. Error Vector Magnitude (EVM)

The EVM is a measure of the distortion caused by a PA to a digital signal and it is defined as the difference between an ideal reference waveform and a measured one (Colantonio *et al*., 2009:20).

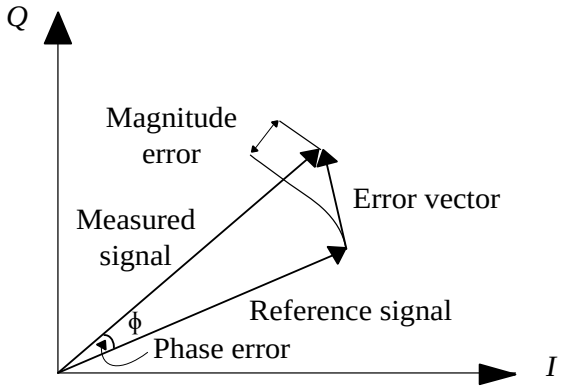



**Figure 4: Error vector magnitude and related quantities (Adapted from Colantonio *et al*., 2009: 3)**

## 2.4. Power Balance in a RF Power Amplifier

The diagram of the power flow and power balance shown in Figure 5, constitute a starting point in the analysis of the maximum achievable *PE* as it allows the identification of all circuit elements sharing the supplied DC power.

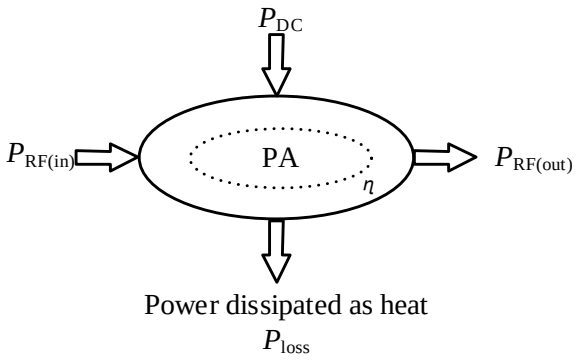



**Figure 5: Power flow and balance diagram in a typical PA (Adapted from Prodanov & Banu, 2007: 351)**

For a PA to achieve 100 % *PE*, all of the DC power supplied must be converted into RF output power.

One of the major limiting factors in achieving 100 % *PE* is the power loss due to the power dissipated in the active device. The main cause of power dissipation in the active device is the power reflected back to the drain of the active device by the output matching network. In the case of a switching PA, the switching loss caused by the non-ideal switching behaviour of the active device contributes to the power dissipated in the active device as well. The power dissipated in the active device is a function of the drain current and voltage as per Equation 13 (Colantonio *et al*., 2009:178-181).

$$P_{\text{diss}} = \frac{1}{T}\int_0^T v_{\text{DS}}(t)\, i_{\text{DS}}(t)\, dt \qquad \text{W} \tag{13}$$

The RF output power consists of two components, namely the power delivered to the load at the fundamental frequency, $P_{\text{RFout}}(f)$, and the power delivered to the load at the multiples of the fundamental frequency, called the harmonic frequencies, denoted $P_{\text{RFout}}(nf)$, with $n$ a positive integer greater than one (Colantonio *et al*., 2009:179).

The power delivered to the load impedance at the fundamental and harmonic frequencies is a function of the amplitudes of the $n^{\text{th}}$ harmonic voltage and current, $V_{\text{n}}$ and $I_{\text{n}}$ respectively, but also a function of the phase shift $\phi_{\text{n}}$ between $V_{\text{n}}$ and $I_{\text{n}}$ . From first principles, $V_{\text{n}}$ and $I_{\text{n}}$ are related by the load impedance $Z_{\text{L}}(nf)$ at the output port of the active. Thus, $P_{\text{RFout}}(nf)$ is given by Equation 14.

$$P_{\text{RFout}}(nf) = \frac{1}{2} V_{\text{n}} I_{\text{n}} \cos(\phi_{\text{n}}) = \frac{1}{2} Z_{\text{L}}(nf) I_{\text{n}}^2 \cos(\phi_{\text{n}}) \qquad \text{W} \tag{14}$$

The consequence of the above observations are that, the power balance condition of a PA states that the supplied DC power must be equal to the sum of the power delivered to the load at the fundamental frequency, the power delivered to the load at the harmonic frequencies and the power dissipated in the active device. That is,

$$P_{\mathrm{DC}} = P_{\mathrm{diss}} + P_{\mathrm{RFout}}(f) + \sum_{\mathrm{n=2}}^{\infty} P_{\mathrm{RFout}}(nf) \qquad \mathrm{W} \tag{15}$$

It can be noted that for a PA to achieve a theoretical *PE* of 100 %, the power delivered to the load at the fundamental frequency must be equal to the DC power. This condition occurs when the sum of the power dissipated in the active device and the power delivered to the load at harmonic frequencies is zero. That is,

$$P_{\mathrm{diss}} + \sum_{\mathrm{n=2}}^{\infty} P_{\mathrm{RFout}}(nf) = 0 \qquad \mathrm{W} \tag{16}$$

Thus, two conditions must be simultaneously fulfilled for a PA to achieve a theoretical *PE* of 100 %. That is,

$$P_{\mathrm{diss}} = \frac{1}{T}\int_0^T v_{\mathrm{DS}}(t)\, i_{\mathrm{DS}}(t)\, dt = 0 \qquad \mathrm{W} \tag{17}$$

and

$$\sum_{\mathrm{n=2}}^{\infty} P_{\mathrm{RFout}}(nf) = \frac{1}{2}\sum_{\mathrm{n=2}}^{\infty} V_{\mathrm{n}} I_{\mathrm{n}} \cos\left(\phi_{\mathrm{n}}\right) = \frac{1}{2}\sum_{\mathrm{n=2}}^{\infty} Z_{\mathrm{L}}(nf) I_{\mathrm{n}}^2 \cos\left(\phi_{\mathrm{n}}\right) = 0 \qquad \mathrm{W} \tag{18}$$

Equation 17 is the mathematical counterpart of the well-known no overlapping between the drain voltage and the drain current, the fulfilment of which alone is erroneously considered sufficient to achieve a 100 % *PE*, neglecting the condition in Equation 18. However, Colantonio *et al*., (2009:179), have shown that a PA can achieve a maximum theoretical *PE* of 81.06 % by fulfilling the condition in Equation 17 only, thus highlighting the importance of the condition in Equation 18.

## 2.5. Classification of RF Power Amplifiers

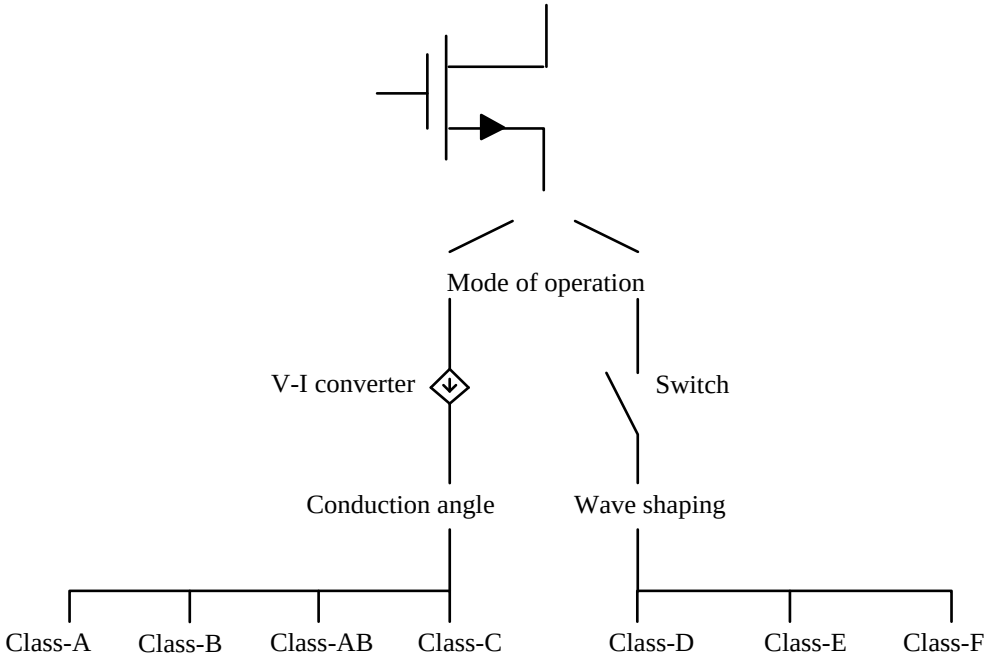



**Figure 6: PA family tree (Adapted from Prodanov & Banu, 2007: 354)**

### 2.5.1. Linear Power Amplifiers

Linear PAs are biased in such a way that the transistor always operates in its linear region. Based on the conduction angle of the transistor, linear PAs are further divided into Class-A, Class-B, Class-AB and Class-C PAs (Nadir & Touati, 2009: 318).

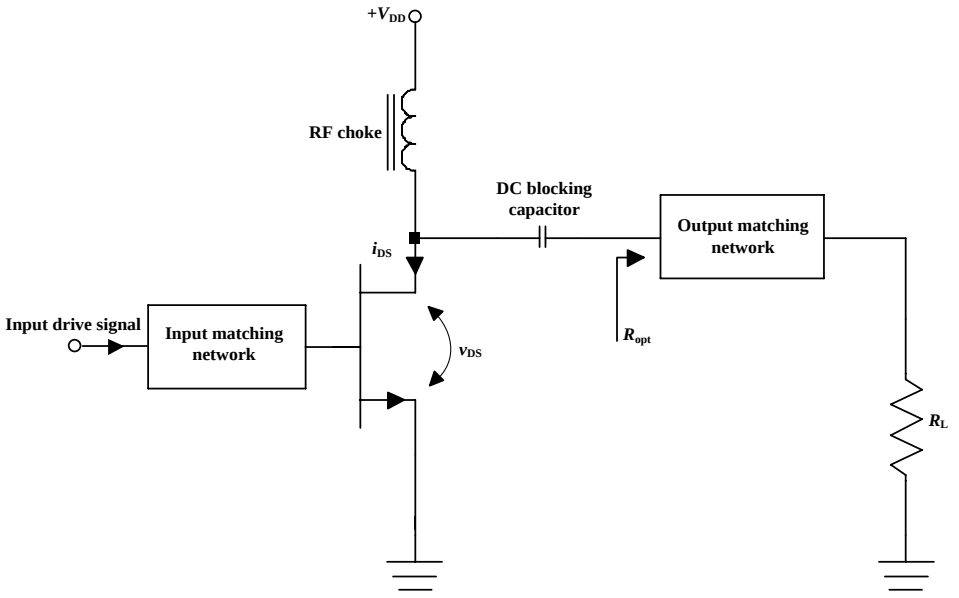



**Figure 7: Basic topology of a linear power amplifier (Adapted from Berglund *et al*., 2006: 93)**

### 2.5.1.1. Class-A Power Amplifiers

Class-A PAs are inherently linear circuits where the transistor is biased to conduct over the entire period of the input signal cycle. The maximum theoretical *PE* of Class-A PAs is 50 %, thus half of the supplied DC power is dissipated in the active device due to a non-negligible overlap between the drain voltage and the drain current as illustrated in Figure 8 (Cripps, 2006:17; Pozar, 2012: 597; MacPherson & Whaits, 2007: 12-16).

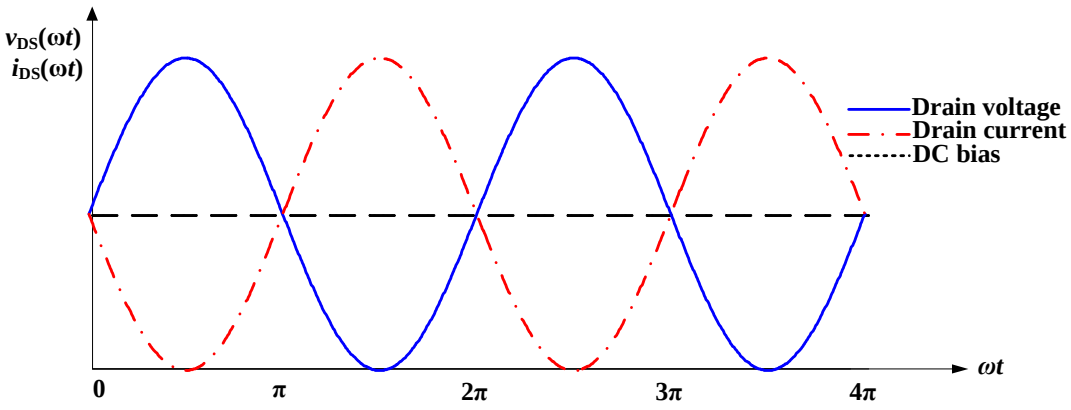



**Figure 8: Drain voltage and current waveforms for a Class-A PA (Adapted from Prodanov & Banu, 2007: 355)**

According to Paul (2004: 176), Class-A PAs are used in applications requiring low output power levels and where power dissipation and efficiency are not critical.

### 2.5.1.2. Class-B Power Amplifiers

The transistor in Class-B PAs conducts for one half of the cycle period of the input signal, resulting in a half sine wave output current. As a result of the reduced conduction angle, the linearity of Class-B PAs is less than that of a Class-A PA. However, the area of overlap between the drain voltage and current waveforms of a Class-B PA, as shown in Figure 9, is less than that of a Class-A PA, thus a Class-B PA is more efficient than a Class-A PA. A theoretical *PE* of 78.5 % can be obtained from a Class-B PA (Cripps, 2006:51; Raab *et al*., 2002: 817).

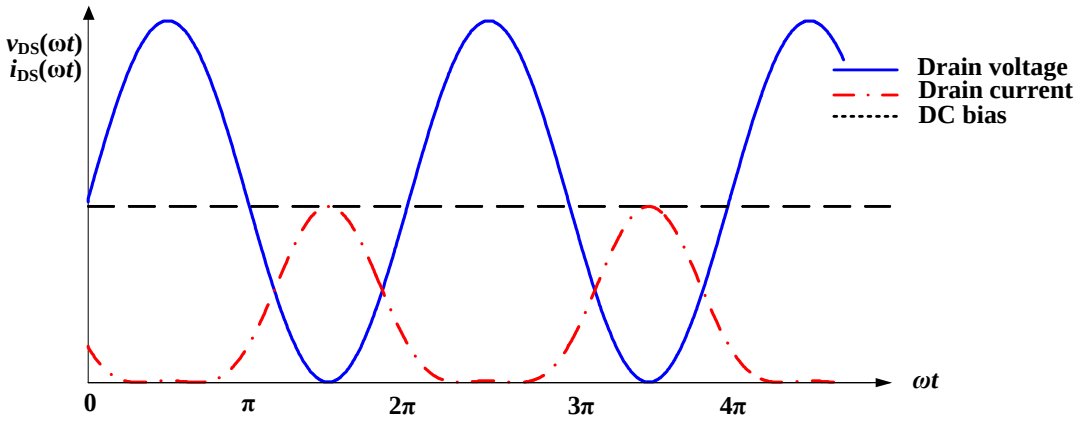



**Figure 9: Drain voltage and current waveforms for a Class-B PA (Adapted from Prodanov & Banu, 2007: 355)**

Class-B PAs are widely used in applications requiring a high output power level and a high *PE* (Raab *et al*., 2002: 817; Paul, 2004: 176).

### 2.5.1.3. Class-AB Power Amplifiers

The Class-AB PA offers a compromise between linearity and efficiency. The drain voltage and current waveforms for a Class-AB amplifier are shown in Figure 10. The Class-AB amplifier is widely used in wireless communication systems, which use modern modulation schemes which require a certain degree of linearity with an acceptable *PE* (Kophon *et al*., 2011: 380). Hayat *et al*., (2013:389), state that a Class-AB PA can achieve a *PE* of up to 60 %.

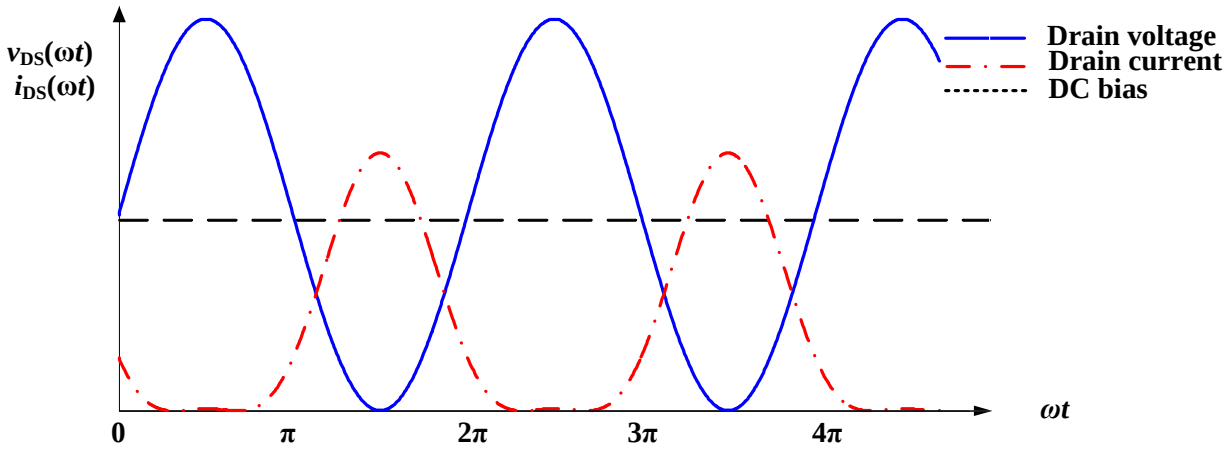



**Figure 10: Drain voltage and current waveforms for a Class-AB PA (Adapted from Prodanov & Banu, 2007: 355)**

### 2.5.1.4. Class-C Power Amplifiers

The transistor in a Class-C PA conducts for less than one half of the cycle period of the input signal, as shown in Figure 11, resulting in a much greater *PE* relative to those of a Class-A and a Class-B PA. Ideally, a Class-C PA can achieve a *PE* of 90 % (Cripps, 2006:51; Raab *et al*., 2002: 817).

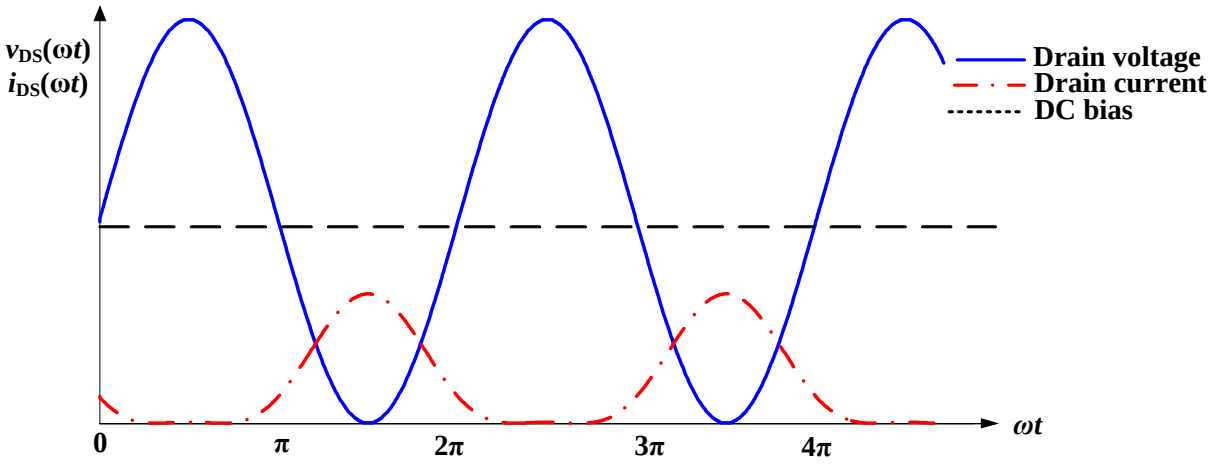



**Figure 11: Drain voltage and current waveforms for a Class-C PA (Adapted from Prodanov & Banu, 2007: 355)**

According to Raab *et al*., (2002: 817) Class-C PAs are widely utilized in power vacuum-tube transmitters, but are generally impractical for solid state PAs. The output power of a Class-C PA is limited due to the reduced conduction angle of the active device.

### 2.5.1.5. Summary of Linear Power Amplifiers

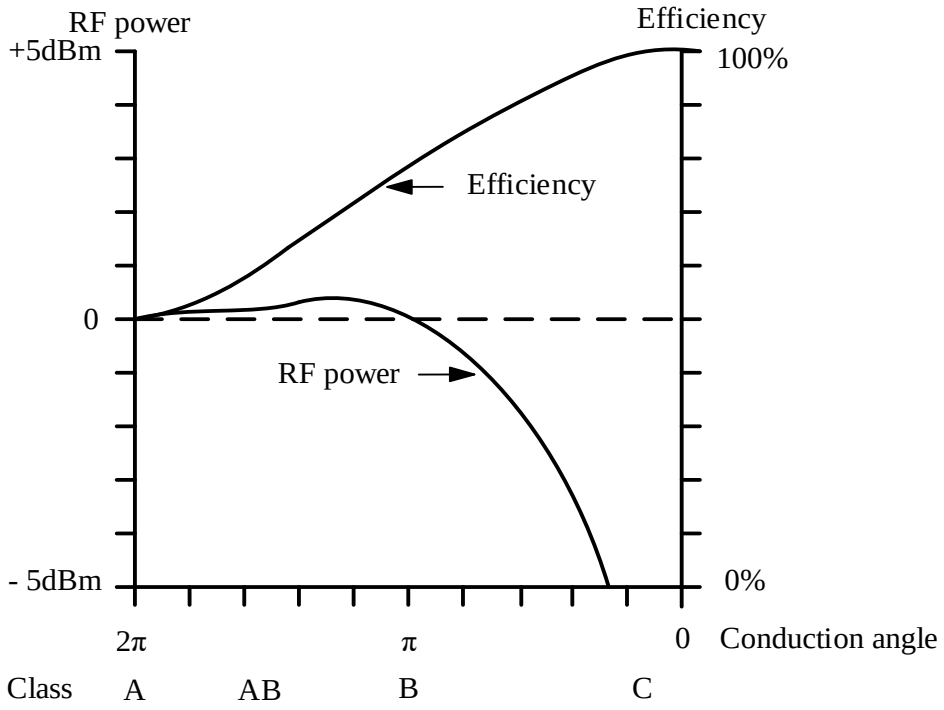



**Figure 12: Output power and efficiency as a function of conduction angle of linear PAs (Adapted from Cripps, 2006:46)**

As shown in Figure 12, a Class-A PA can deliver the same output power level as a Class-B PA. However, the conduction angle of a Class-B amplifier is half of that of a Class-A amplifier, resulting in better efficiency for the Class-B amplifier. A Class-C PA has a much higher *PE* relative to that of Class-A, AB and B amplifiers, but this is associated with a significant reduction in output power (Cripps, 2006:46; Prodanov & Banu, 2007: 356-357).

**Table 1: Comparison of PAs classes of operation**

| Classes of operation | Theoretical *PE* | Linearity |
|---|---|---|
| A | 50 % | good |
| B | 78.5 % | poor |
| AB | 60 % | good |
| C | 90 % | Very poor |

### 2.5.2. Switching Power Amplifiers

The transistor in switching a PA is operated as a switch. Based on the method of pulse shaping, switching PAs are further divided into Class-D, Class-E and Class-F PAs (Nadir & Touati, 2009: 318).

#### 2.5.2.1. Class-D Power Amplifiers

A Class-D PA consists of two transistors and either a series or a parallel resonant circuit at the output port of the PA for the purpose of pulse shaping. A Class-D PA which utilises a series resonant circuit is referred to as Voltage-Mode Class-D (VMCD) PA (Berglund *et al*., 2006: 94-95; Raab *et al*., 2002: 817). An example of such a PA is illustrated in Figure 13.

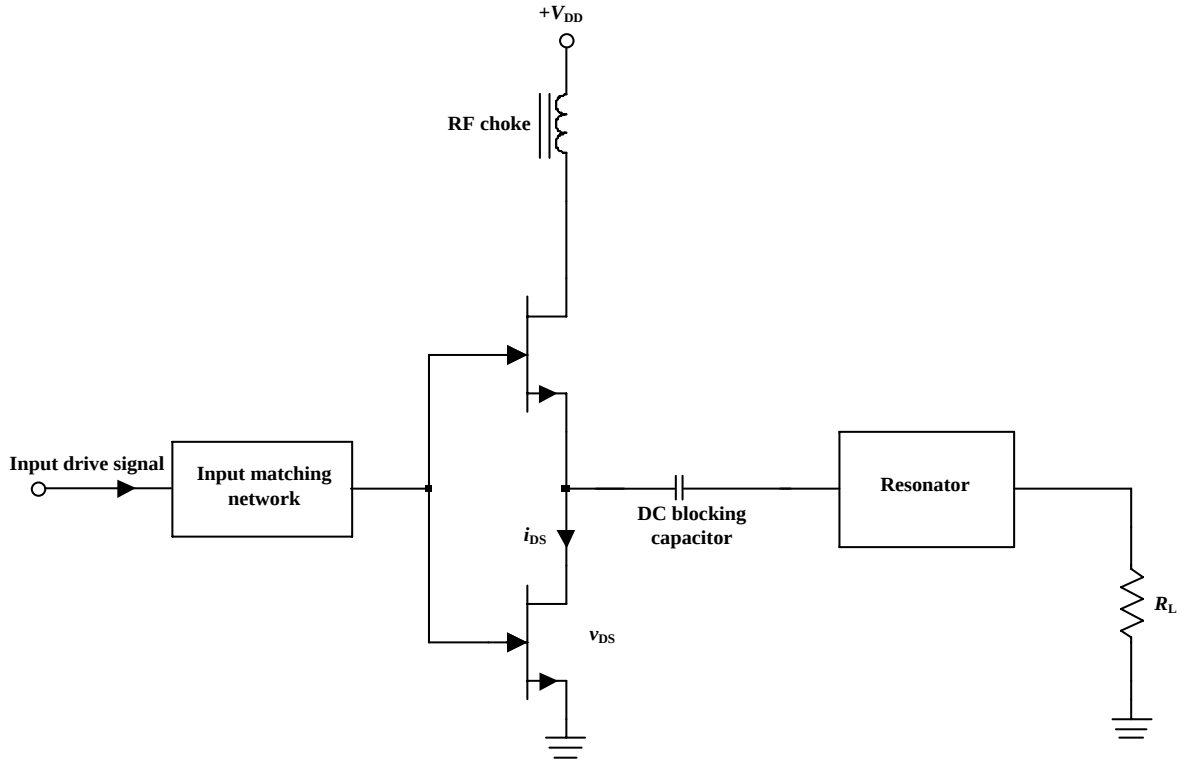



**Figure 13: Basic topology of a VMCD PA (Adapted from Berglund *et al*., 2006: 94)**

A Class-D PA which utilises a parallel resonant circuit is referred to as Current-Mode Class-D (CMCD) PA (Berglund *et al*., 2006: 94-95), an example of which is shown in Figure 14.

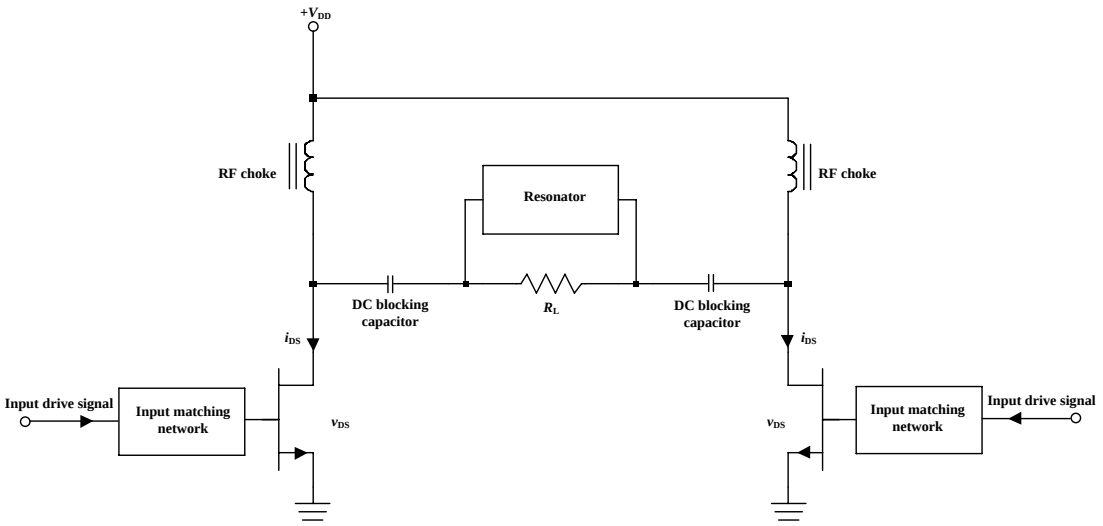



**Figure 14: Basic topology of a CMCD PA (Adapted from Berglund *et al*., 2006: 94)**

Ideally, a Class-D PA can achieve a *PE* of 100 % as there is no overlap between the drain voltage and current waveforms as shown in Figure 15 (Berglund *et al*., 2006:95; Raab *et al*., 2002: 817).

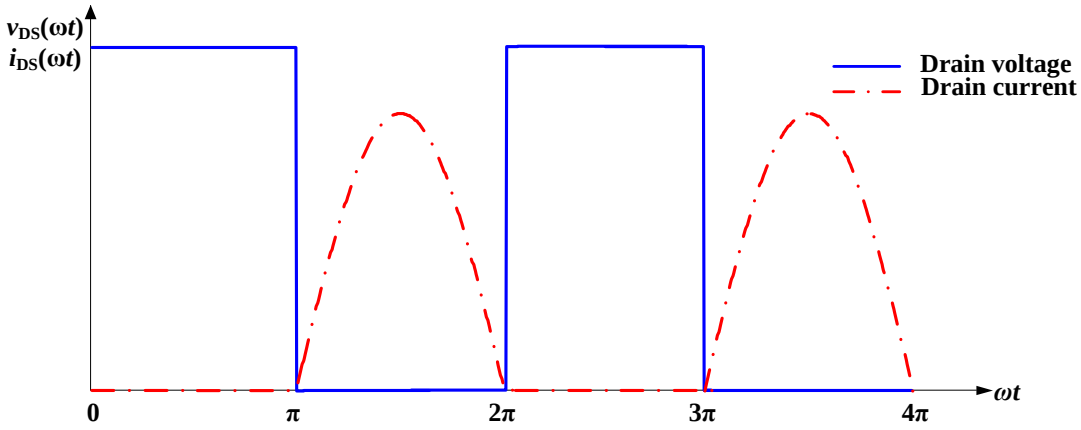



**Figure 15: Drain voltage and current waveforms for a Class-D PA (Adapted from Prodanov & Banu, 2007: 360)**

The main drawback of Class-D PAs is that they require transistors with a high drain break down voltage. They also suffer from losses due to saturation, switching speed, and drain capacitance which become dominant at higher frequencies (Berglund *et al*., 2006:95; Raab *et al*., 2002: 817).

### 2.5.2.2. Class-E Power Amplifiers

Introduced in 1975 by Sokals, Class-E PAs are switching PAs in which the transistor is continuously turned on and off. In their simplest form, Class-E PAs consist of a series resonant circuit at the output port for the purpose of waveform shaping (Ramadan *et al*., 2009:117), as shown in Figure 16.

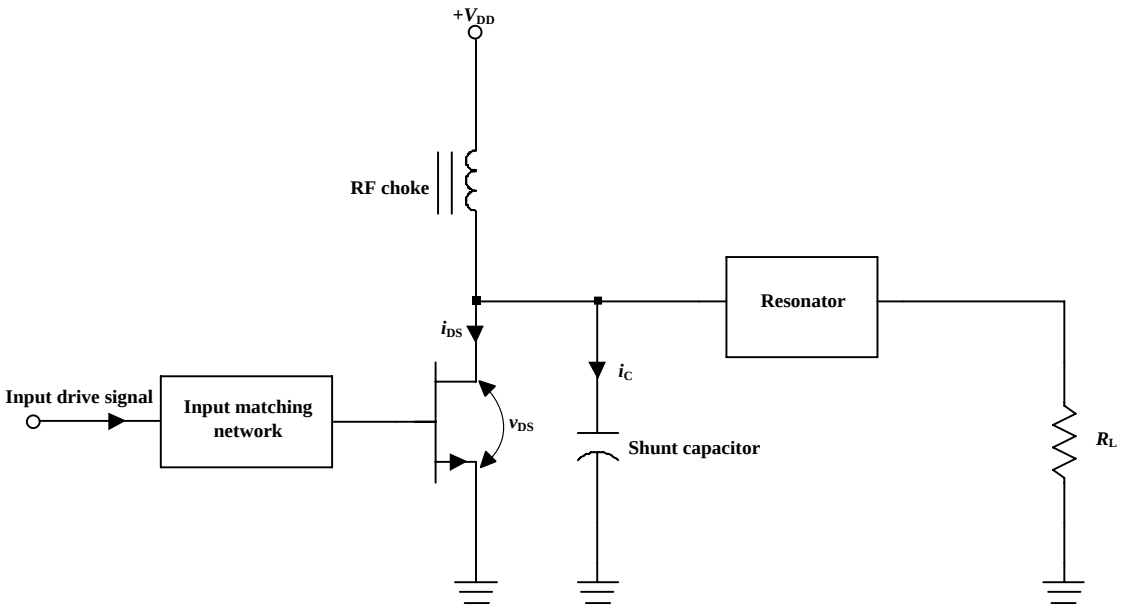



**Figure 16: Topology of a Class-E PA (Adapted from Berglund *et al.*, 2006: 94)**

The shunt capacitor is connected in parallel with the transistor for current wave-shaping, thus making a Class-E PA capable of achieving a *PE* of up to 85 % at microwave frequencies (Berglund *et al.*, 2006:95).

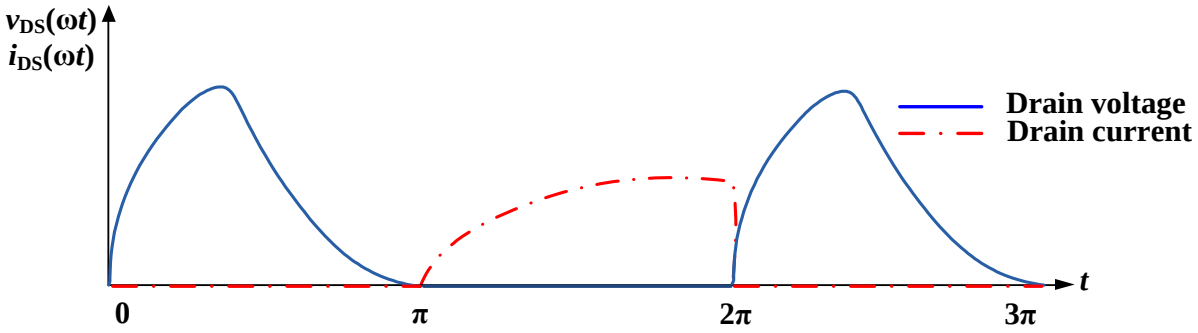



**Figure 17: Drain voltage and current waveforms for a Class-E PA (Adapted from Prodanov & Banu, 2007: 360)**

In an ideal Class-E PA, as the transistor turns on, the drain voltage drops to zero volts, resulting in no overlap between the drain voltage and current, as shown in Figure 17. Hence, the elimination of losses due to the drain capacitance and the reduction of the switching losses which are encountered in a Class-D PA. The resonator provides the necessary termination to ensure that no power is delivered to the load at harmonic frequencies. A theoretical *PE* of 100 % can be obtained with an ideal Class-E PA (Seunghoon, *et al.*, 2012: 89-90; Raab *et al.*, 2002: 817). Figure 18 shows the measured performance parameters for *PE* and $P_{out}$ of a typical Class-E PA.

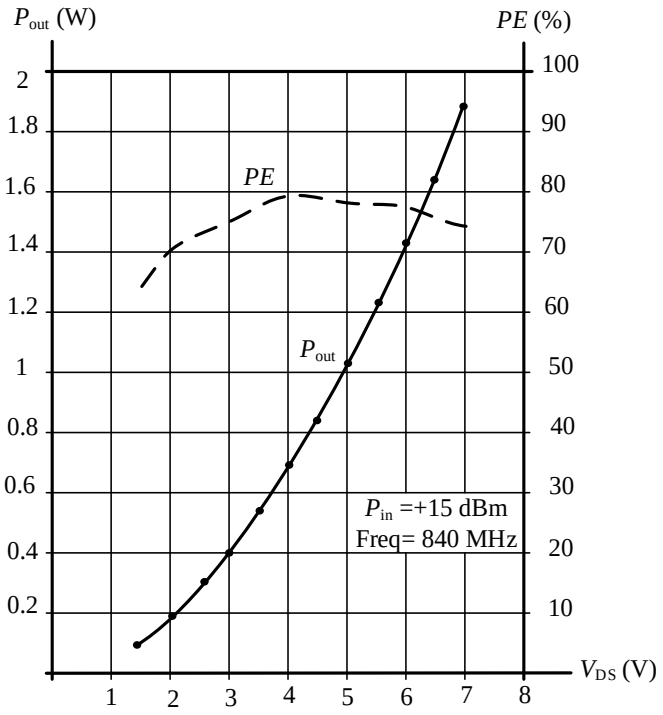



**Figure 18: Measured performance of a Class-E PA (Adapted from Cripps, 2006:199)**

Class-E PAs are widely utilized due to their simple circuit topology when compared to other switching PAs, their relatively high *PE* values, their soft switching which reduces switching losses and their low sensitivity to the circuit component variations. (Ahmed, *et al*., 2013: 153; Kizilbey *et al*., 2013: 8-9; Hasani & Mahmoud, 2008: 1759).

A Class-E PA requires active device with a high break down voltage, since the peak drain voltage can reach up to three times the supply DC drain voltage (Kizilbey *et al*., 2013: 8-9).

According to Seunghoon *et al*., (2012: 89-90) the maximum frequency at which a Class-E PA can operate is limited by the drain capacitance of the active device, the maximum drain current and the DC supply voltage.

$$f_{max} = \frac{I_{DS}}{2\pi^2 C_{out} V_{DS}} \quad \text{Hz} \tag{19}$$

The larger the drain capacitance the lower the maximum frequency of operation of a Class-E PA. It is important to select an active device technology with a lower output capacitance (Kizilbey *et al*., 2013: 8-9).

Several authors among which Ahmed, *et al*., (2013: 158-159) and Seunghoon, *et al*., (2012: 92-95) proposed a new design technique to operate Class-E PAs above the maximum frequency of operation but this resulted in a significant degradation of the *PE*.

### 2.5.2.3. Class-F and Class-F$^{-1}$ Power Amplifiers

The transistor in a Class-F PA is biased the same as that of a Class-B PA, that is, the transistor conducts for half the period of a cycle of the input signal, resulting in a half sine wave current waveform at the drain terminal. The PA is then driven into saturation resulting in the generation of a high power level signal at the drain terminal containing multiple harmonic components. For this

reason, a Class-F PA is often referred to as an overdriven Class-B PA. The output network of a Class-F PA comprises a harmonic resonator which is used to shape the drain waveforms (Sadegh & Thomas, 2015: 39-40; Colantonio *et al*., 2009:268-269; Schmelzer & Long, 2007: 2130; Raab *et al*., 2002: 817).

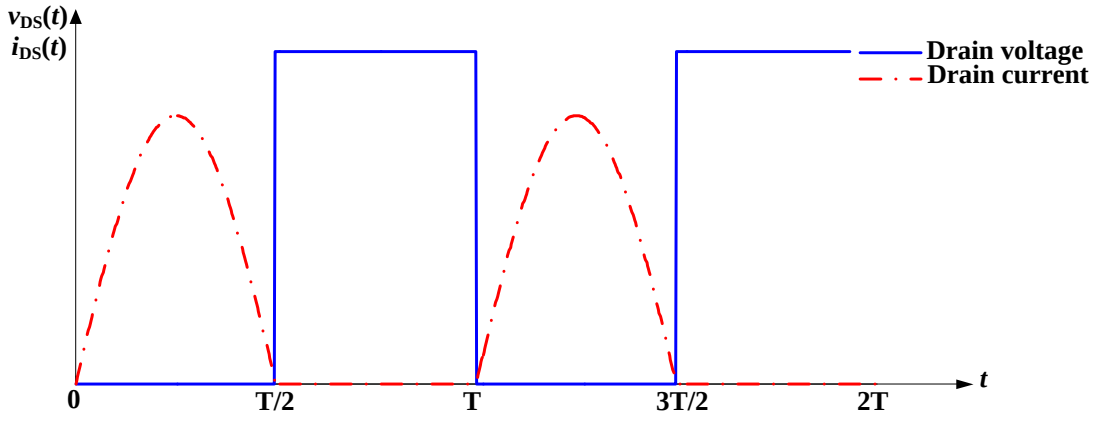



**Figure 19: Drain voltage and current waveforms for a Class-F PA (Adapted from Prodanov & Banu, 2007: 360)**

In an ideal Class-F PA, the square-wave drain voltage waveform consists of an infinite number of odd harmonics and the half sine wave current waveform consists of an infinite number of even harmonics. The drain voltage and current waveforms are shown in Figure 19 above. The *PE* of a Class-F PA depends upon the number of harmonic components actually permitted by the harmonic resonator connected to the drain terminal, and can reach up to 90 % if the fifth harmonic is present (Sadegh & Thomas, 2015: 39-40;Moon *et al*., 2012: 1937; Schmelzer & Long, 2007: 2130; Raab *et al*., 2002: 817).

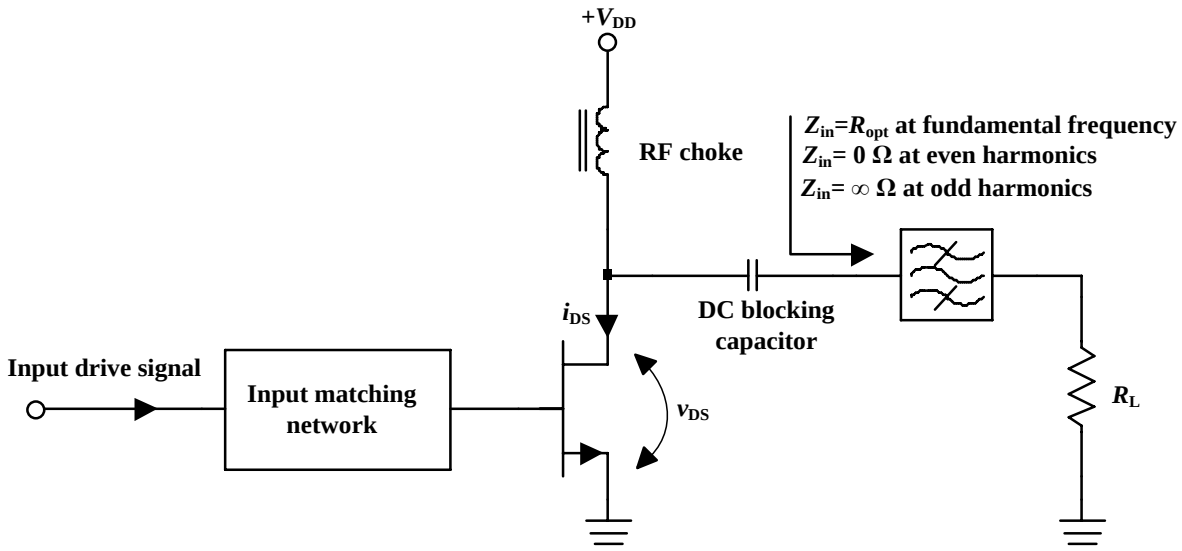



**Figure 20: Basic topology of a Class-F PA (Adapted from Kim *et al*., 2008: 1177)**

The basic topology of a Class-F PA is shown in Figure 20. A Class-$F^{-1}$ PA topology is exactly the same as that of the Class-F PA, but the drain voltage and current waveforms are interchanged. The drain voltage waveform is shaped like a half sine wave and the current waveform is shaped like a square wave (Moon *et al*. 2012: 1937; Wang *et al*. 2011: 1).

## 2.6. Design Principles and Requirements

According to Raab *et al*. (2002: 814-816), no single PA design technique suits all applications. Each application has specific output power and efficiency requirements, thus a different PA design approach is required for each class of amplifier.

The fundamental requirements for the design of the PA in a CubeSat are a high *PAE* and a high output power level. A high output power level is required to reduce the number of amplifier stages, the size and the weight of the transmitter, thus decreasing the manufacturing costs. A high *PAE* is required to increase battery lifetime and facilitate optimal thermal management thereby reducing the operating costs (Colantonio *et al*. 2004: 191; Chiang & Chuang, 1997: 1150).

### 2.6.1. Design Techniques

The goal in the design of a PA is to transform a challenging non-linear design problem into one which can be solved utilizing the most fundamental design tools (Cripps, 2006: 36-37; MacPherson & Whaits, 2007: 12-16).

#### 2.6.1.1. Load-Line Theory

The load-line theory is a useful design technique used as a starting point in the design of a PA by considering the transistor as an ideal voltage controlled current generator. This technique has been used before the development of computer aided design (CAD), to predict the performance of a linear PA (Cripps, 2006: 21-26).

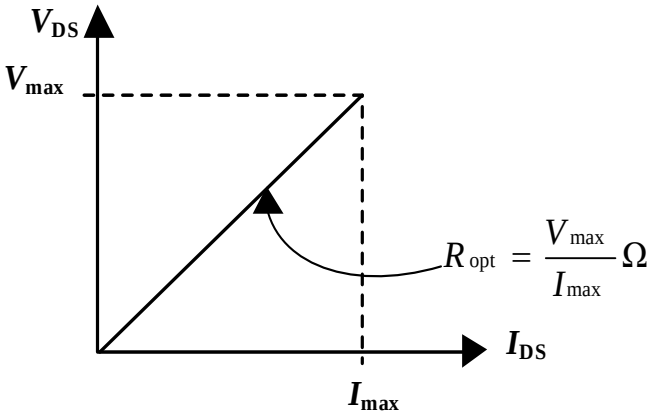



**Figure 21: Load-line match (Adapted from MacPherson & Whaits, 2007: 12-16)**

According to MacPherson & Whaits (2007: 12-16), a PA will deliver maximum power to a load under the condition that the output port of the active device is terminated with an optimum resistance value. Load-line theory can be used to determine the value of this optimum resistance as shown in Figure 21 above.

Load-line theory is used to estimate the performance, that is, the output power and *PE* of a PA under the assumption that the transistor is ideal, meaning that the knee voltage is equal to zero (Sandro *et al*., 2013:1459).

In cases where the knee voltage of the transistor cannot be neglected, load-line theory would lead to both sub-optimal output power and a sub-optimal *PE*. The ratio of the knee voltage to the maximum drain voltage is a determining factor in deciding whether load-line theory can be used to predict the performance of a PA (Sandro *et al*., 2013:1462).

### 2.6.1.2. Load-Pull Technique

Load-pull analysis consists of plotting the performance parameters for output power, *PE* and *PAE* of a transistor, by varying or tuning the impedance presented at the output port of the transistor. The purpose of the load-pull technique is to determine the value of impedance termination required for the transistor to deliver either maximum power or maximum achievable *PE* or a compromise between the two (Cripps, 2006:17-18; Moravek & Hoffmann, 2011: 828).

Load-pull data can be used directly for PA design to achieve maximum output power or maximum *PE* by determining the optimum impedance terminations required for the transistor operation (Zargar *et al*., 2012:1).

Load-pull data can be obtained from large signal simulations. This requires a large signal model of the transistor from the manufacturer. However, the accuracy of these models is far from being acceptable in a practical design (Moravek & Hoffmann, 2011:828; Colantonio *et al*., 2004: 191). The discrepancy of the HEMT changes the phase of the harmonics and degrades the *PE* and the prediction between varying large signal and fixed linear impedance.

Load-pull data can also be obtained by direct measurements as shown in Figure 22. In this case the transistor is fully characterized in terms of output power, *PE* and any other required performance. The cost of the test-bench equipment and the complexity of the measurement set-up are the drawbacks of this method (Yeap, 2004:1; Colantonio *et al*., 2004: 191; Chiang &Chuang, 1997: 1150).

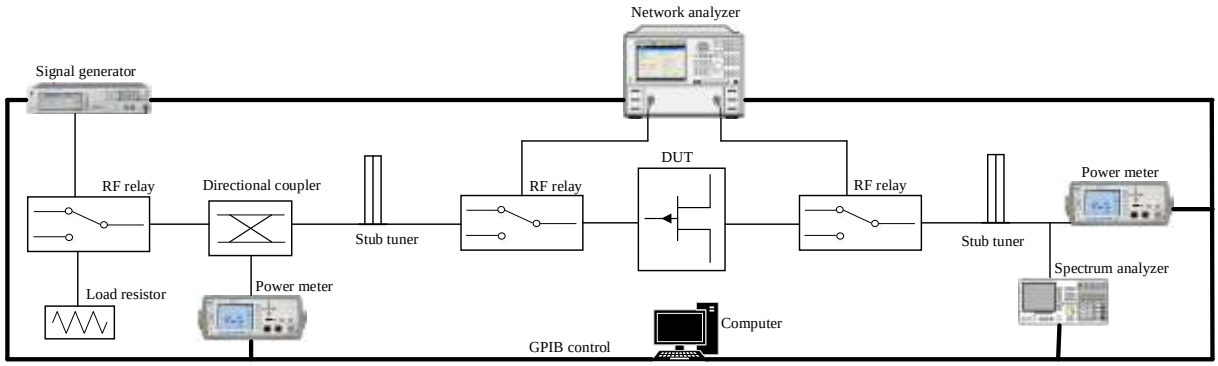



**Figure 22: Load-pull measurement setup (Adapted from Chiang &Chuang, 1997: 1150)**

Cripps (1983: 221), has shown that there is a simple mathematical formulation from which load-pull contours can be generated on the Smith chart. The problem with this approach lies in the fact that the shape of the load contour is not a circle, thus any mathematical formulation should take into account the non-linear behaviour of the transistor.

For the design of a non-linear PA based on shaping and controlling waveforms, it is imperative to measure the load-pull data of the harmonics to obtain optimum impedances at harmonic frequencies (Zargar *et al*., 2012:1).

### 2.6.2. RF Power Device Technology

Silicon LDMOS, GaAs and GaN are the most predominant technologies used in the design of RF PAs. LDMOS transistors are used for high power RF PAs. GaN transistors have a higher power density than GaAs and silicon transistors, resulting in low input and output parasitic capacitor values (Berglund *et al*., 2006:96; Schmelzer & Long, 2007: 2130).

RF power devices such as bipolar junction transistors (BJTs), metal oxide semiconductor field effect transistors (MOSFETs), junction field effect transistors (JFETs), gallium arsenide metal semiconductor field effect (GaAs MESFET), GaN HEMTs, pHEMTs and vacuum tubes are all used in the design of PAs (Raab *et al*., 2002: 816).

Recently, GaN HEMTs are predominantly used for the design of PAs in satellite communication systems due to their high dynamic range, high drain break down voltage, high power density, high thermal dissipation, a superior current density and high carrier mobility. Thus, GaN HEMTs are most suitable for high efficiency PA design operating in switching mode (Ramadan *et al*., 2009:117; Kim *et al*., 2008: 1177).

## 2.7. Summary

**Table 2: Measured performance parameters of various PAs**

| Class | Frequency (GHz) | *PAE* (%) | Output power (W) | Transistor technology | Reference |
|---|---|---|---|---|---|
| AB | 2 | 62 | 3 | GaN HEMT | (Narahashi *et al*., 2007: 1200) |
| C | 1.8 - 2.2 | 57-70 | 20 | GaN HEMT | (Arnous *et al*., 2013:1390) |
| D | 2.35 | 65 | 8.3 | GaN HEMT | (Alfaki *et al*., 2009: 1005) |
| E | 2.5 | 74 | 6.7 | GaN HEMT | (Ghajar & Boumaiza, 2019: 1) |
| F | 2 | 85 | 16.5 | GaN HEMT | (Schmelzer & Long, 2007:2130) |
| $F^{-1}$ | 0.915 | 83.4 | 10.8 | GaN HEMT | (Andrew & Christopher, 2012: 5-6) |

A careful selection of the optimum load impedance and appropriate harmonic terminations are the key challenges in the design of a high *PE* and a high output power PA. A practical *PE* of above 80 % can be achieved with a switched mode PA topology using GaN HEMT devices (Cripps, 2006:172).

## 2.8. Conclusions

The poorer *PE* of a Class-A PA can be improved by reducing the conduction angle of the active device. This results in a decrease in the overlap area of the drain voltage and current thus reducing the power dissipated in the active device and increasing the *PE* of the PA. This occurs in the case of Class-B, Class-AB and Class-C PAs. In linear PAs, it is assumed that the power delivered to the load at harmonic frequencies is negligible because the active device (transistor) is operated in its linear region. However, as the conduction angle is reduced the active device tends to operate in a more non-linear mode, resulting in the generation of non-negligible power levels at harmonic frequencies. The *PE* of a reduced conduction angle PA is limited to below 70 %. This is due the absence of any mechanism to reduce the power delivered to the load at multiple harmonic frequencies and by the fact that minimizing the power dissipated in the active device is not sufficient enough to achieve a high *PE*. It should also be noted that reducing the conduction angle of the active device limits the output power capabilities of a PA.

On the other hand, switching PAs, such as a Class-D and a Class-E PA, use the switching property of the transistor to minimize the power dissipated in it. However, the transistor is not an ideal switch which limits the minimum power dissipation achievable in it. The use of two active devices as in a Class-D PA adds practical complexity to the circuit, thus it is important to determine whether the performance of a Class-D PA is worth the added complexity for a particular application. The practical *PE* of a Class-E PA is limited by the stringent requirements on the frequency of operation, which are difficult to approximate in practice and the fact that an ideal switching operation is not possible. The use of Class-E PAs above the maximum frequency of operation defined by Equation 19, require the use of design techniques that degrade the *PE*.

The use of harmonic resonators connected to the drain terminal in a Class-F and a Class-$F^{-1}$ PA minimize the power delivered to the load at harmonic frequencies of the applied signal. The shape of the waveforms at the drain of a Class-F and a Class-$F^{-1}$ PA suggest that there is no overlap between the drain voltage and the drain current, thus minimizing the power dissipated in the active device. Thus, Class-F and Class-$F^{-1}$ PAs fulfil the two necessary and sufficient conditions for a maximum achievable *PE*.

# Chapter 3

# Class-F and Class-F$^{-1}$ RF Power Amplifiers

## 3.1. Introduction

To maximize the theoretical *PE* of a RF PA, several design techniques and classes of operation have been investigated and developed. A Class-F and a Class-F$^{-1}$ PA are among the classes of operation that fulfil the necessary and sufficient conditions for a maximum *PE* as derived in Chapter 2. Thus these types of PA can achieve a theoretical *PE* of 100 % with an acceptable practical complexity. In this Chapter, the operational conditions of the Class-F and Class-F$^{-1}$ PA are described and a comparison is made between these two classes of PA. An alternative topology of wave-shaping network that meets the Class-F$^{-1}$ operational conditions is then proposed. The analysis presented in this thesis assumes the use of a FET active device but can also be applied to BJT active devices.

## 3.2. Description of a Class-F PA Based on the Drain Waveforms

The design technique for a Class-F PA consists of forcing the drain voltage into a square wave shape and the drain current into a half sine wave shape. This technique causes the drain voltage to be zero as the drain current reaches its maximum value and is maximized when the drain current is at its minimum value. The half sine wave current is a result of the Class-B bias condition (Colantonio *et al*., 2009: 268-270). The basic circuit diagram of a Class-F PA is shown in Figure 23.

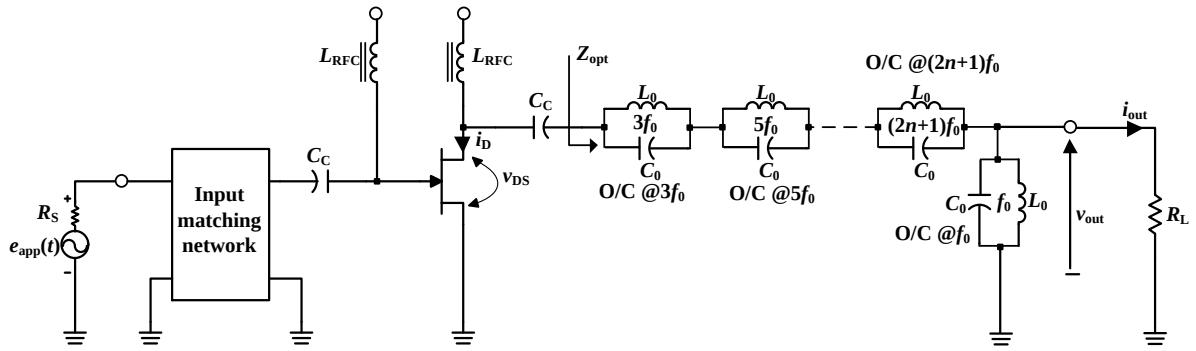



**Figure 23: Basic circuit of a Class-F PA (Adapted from Grebennikov & Sokal, 2007:104)**

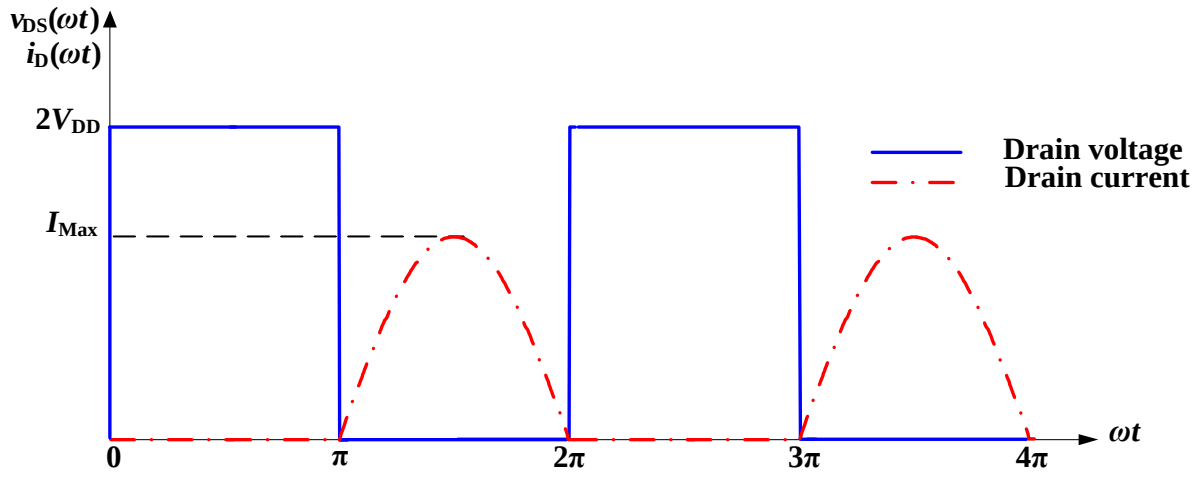



**Figure 24: Ideal drain waveforms of a Class-F PA**

The ideal waveforms of the drain voltage and the drain current are shown in Figure 24 and are mathematical defined by:

$$i_D(\omega t) = \begin{cases} 0 & , \ 0 \le t \le \pi \\ I_{Max} \sin(\omega t) & , \ \pi \le t \le 2\pi \end{cases} \quad \text{A} \tag{20}$$

$$v_{DS}(\omega t) = \begin{cases} 2V_{DD} & , \ 0 \le t \le \pi \\ 0 & , \ \pi \le t \le 2\pi \end{cases} \quad \text{V} \tag{21}$$

These two waveforms do not overlap which results in zero power being dissipated in the active device, thus fulfilling Equation 17 which is the first condition for a maximum *PE*, as derived in Chapter 2.

The drain current waveform can be expressed as a Fourier series given by:

$$i_D(\omega t) = \frac{I_{Max}}{\pi} + \sum_{n=1}^{\infty} I_n \cos(n\omega t) \quad \text{A} \tag{22}$$

where the Fourier coefficient $I_n$ is determined for specific values of $n$ and given by:

$$I_n = \begin{cases} \dfrac{I_{Max}}{2} & n = 1 \\ \dfrac{2\,I_{Max}}{\pi} \dfrac{(-1)^{\frac{n}{2}+1}}{n^2-1} & n \text{ is even} \\ 0 & n \text{ is odd} \end{cases} \quad \text{A} \tag{23}$$

The magnitude spectrum of the drain current is shown in Figure 25:

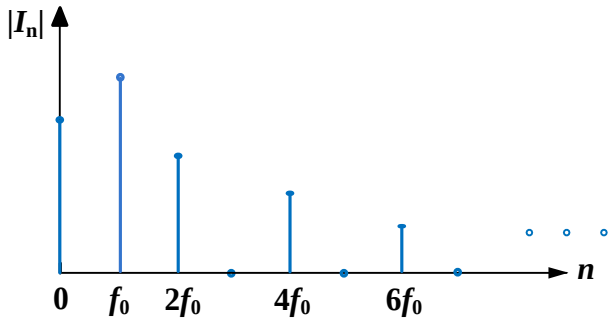



**Figure 25: Magnitude spectrum of a half sine wave**

It should be noted that the magnitude spectrum of the drain current of a Class-F PA consists of the DC component, the fundamental component and even harmonic components of the fundamental frequency. The sum of this infinite number of even harmonics will result in a half sine wave current at the drain of the active device.

The drain voltage waveform can also be expressed as a Fourier series and given by:

$$v_{DS}(\omega t) = V_{DD} + \sum_{n=1}^{\infty} V_n \sin(n\omega t) \quad \text{V} \tag{24}$$

where the Fourier coefficient $V_n$ is determined for specific values of $n$ and given by:

$$V_n = \begin{cases} -\dfrac{4V_{DD}}{\pi} & n = 1 \\ 0 & n \text{ is even} \\ \dfrac{4V_{DD}}{\pi}\dfrac{(-1)^{\frac{n+1}{2}}}{n} & n \text{ is odd} \end{cases} \quad \text{V} \tag{25}$$

The magnitude spectrum of the drain voltage is shown in Figure 26.

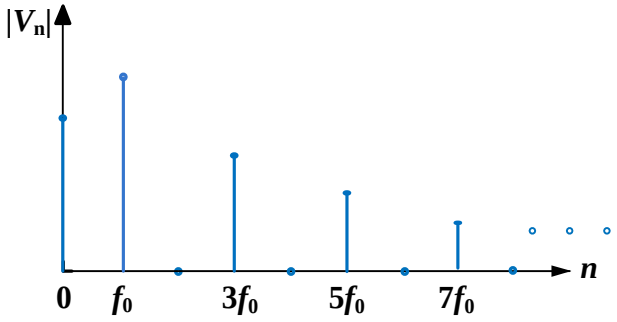



**Figure 26: Magnitude spectrum of a square wave**

It should also be noted that the spectrum of the drain voltage of a Class-F PA consists of a DC component, the fundamental component and odd harmonics components. The sum of the infinite number of odd harmonics will result in a square wave voltage at the drain of the active device.

Figures 25 and 26 show that the Fourier components with the same order *n* are alternately not present. In Equation 18, the product of $V_n$ and $I_n$ , that is, the magnitude spectrums in Figure 25 and 26, result in zero power delivered to the load at all harmonic frequencies ($P_{RFout}$ ($nf$ ) = 0 for $n > 1$), which fulfils the second condition for maximum *PE*, that is, Equation 18.

Thus the Class-F PA meets the necessary and sufficient conditions to achieve a theoretical *PE* of 100 %, which can be proven mathematically as follows:

The amplitude of drain current at the fundamental frequency is given by:

$$I_1 = \frac{I_{Max}}{2} \quad \text{A} \tag{26}$$

The amplitude of drain voltage at the fundamental frequency is given by:

$$V_1 = \frac{4\,V_{DD}}{\pi} \quad \text{V} \tag{27}$$

The output power at the fundamental frequency, assuming zero phase shift between the drain voltage and the drain current is given by:

$$P_1 = \frac{1}{2} V_1 \times I_1 = \frac{4V_{DD}}{2\pi} \times \frac{I_{Max}}{2} = \frac{V_{DD}\, I_{Max}}{\pi} \quad \text{W} \tag{28}$$

For an active device biased in a Class-B mode, the DC power supplied is given by:

$$P_{DC} = V_{DD} \times I_{DC} = \frac{V_{DD}\, I_{Max}}{\pi} \quad \text{W} \tag{29}$$

Thus the theoretical *PE* is given by:

$$PE = \frac{P_1}{P_{DC}} \times 100\ \% = \frac{V_{DD}\, I_{Max}}{\pi} \times \frac{\pi}{V_{DD}\, I_{Max}} \times 100\ = 100\ \% \tag{30}$$

The technique used to fulfil the two necessary and sufficient conditions for a maximum theoretical *PE* raise a number of questions which are:

How does one obtain the necessary harmonic content at the drain of the active device?

How is the harmonic content manipulated to achieve the desired drain waveforms?

Is it necessary to add up an infinite number of harmonics to obtain the desired waveforms?

The answers to these questions are presented in the following section.

According to (Colantonio *et al*., 2009: 268-270), in a PA with a large drive signal, the drain current and voltage waveforms are no longer purely sinusoidal and they exhibit a significant harmonic content due to the physical limits of the drain current and voltage swings of the active device.

The above statement implies that the presence of a significant harmonic content in the signals at the drain of the active device is unavoidable, provided that the drive signal of the PA is large enough.

According to Ohm's law, the amplitudes of the drain voltage and the drain current defined in Equations 23 and 25 respectively are related by the impedance presented to the drain of the active device which is given by:

$$Z_n = \begin{cases} \frac{8}{\pi}\frac{V_{DD}}{I_{Max}} = R_{opt} & n = 1 \\ 0 & n \text{ is even} \\ \infty & n \text{ is odd} \end{cases} \quad \Omega \tag{31}$$

To achieve the required Class-F waveforms as depicted in Figure 24, the drain of the active device must be terminated with the optimum resistance defined in Equation 31 at the fundamental frequency, a short circuit at all even harmonics and an open circuit at all odd harmonics. These conditions are referred to as the operational conditions of a Class-F PA.

The impedances defined in Equation 31 are a function of the shape of the drain waveforms at the drain terminal.

According to (Grebennikov & Sokal, 2007: 95), an infinite number of odd harmonic resonators result in an idealized Class-F mode which has a square wave voltage waveform and a half sine wave current waveform at the device output terminals", as shown in Figures 23 and 24.

However, (Colantonio *et al*., 2009: 268-270), states that the benefit attainable by controlling the higher order harmonic terminations are usually negligible when compared to the resulting increased circuit complexity and hence the resulting increase in losses. Thus, in a practical Class-F PA, only the fundamental and the first two harmonics are controlled, leaving the higher order harmonics terminated through the shunting effect of the parasitic capacitor at the output port of the active device.

However, the lack of contribution by the higher order ($n$>3) harmonics result in a non-negligible overlap between the drain current and voltage that lead to an increase in the power dissipated in the active device and hence a decrease in the maximum achievable *PE*.

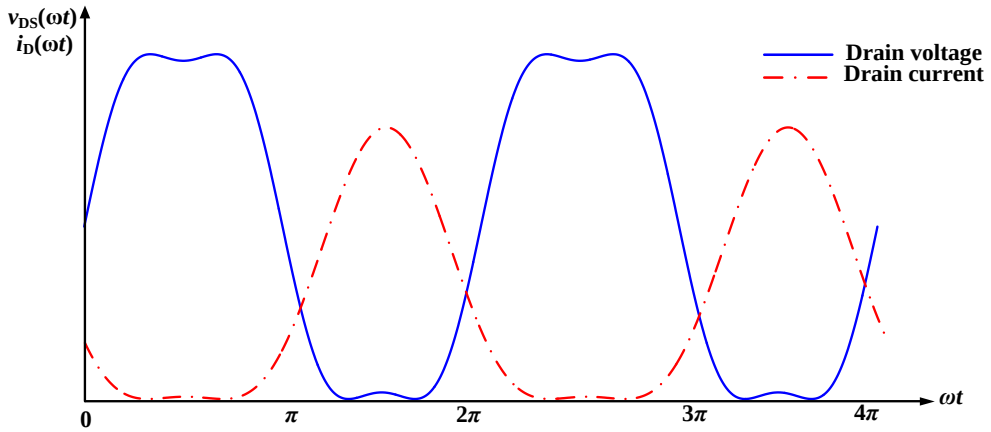



**Figure 27: Drain waveforms of a Class-F PA with only the second and third harmonics present (Adapted from Grebennikov & Sokal, 2007:98)**

## 3.3. Description of a Class-F$^{-1}$ PA Based on the Drain Waveforms

The technique for the design of a Class-F$^{-1}$ PA consists of shaping the drain voltage into a half sine wave and the drain current into a square wave. Thus, for a Class-F$^{-1}$ PA the drain current and voltage are interchanged when compared to the conventional Class-F PA. This is made possible by the fact that the shapes of the drain waveforms are determined by the impedance presented at the drain terminal of the active device. The basic circuit and the ideal drain voltage and current waveforms of a Class- F$^{-1}$ PA are shown in Figures 28 and 29 respectfully.

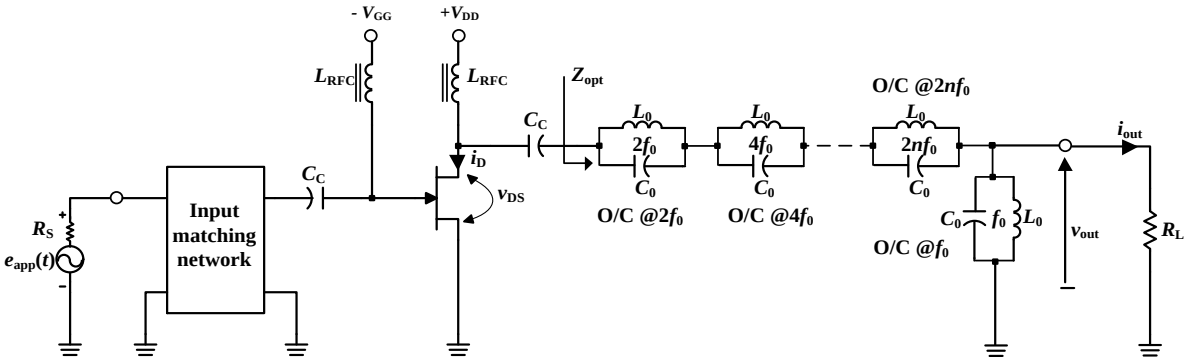



**Figure 28: Basic circuit of a Class-F$^{-1}$ PA (Adapted from Grebennikov & Sokal, 2007:158)**

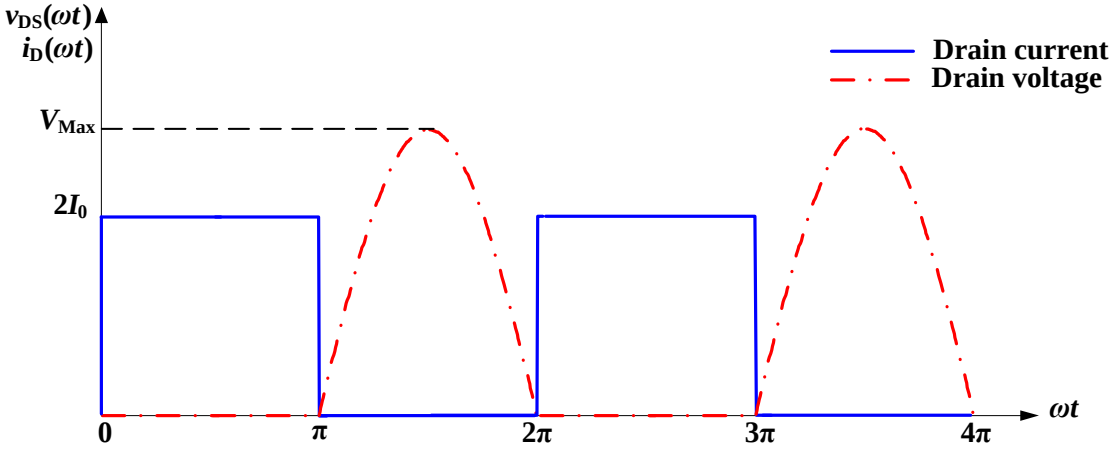



**Figure 29: Ideal drain waveforms of a Class-F$^{-1}$ PA**

The analytic definitions of the drain current and the drain voltage are given by:

$$i_D(\omega t) = \begin{cases} 2I_0\,, & 0 \le t \le \pi \\ 0\,, & \pi \le t \le 2\pi \end{cases} \quad \text{A} \tag{32}$$

$$v_{DS}(\omega t) = \begin{cases} 0\,, & 0 \le t \le \pi \\ V_{Max}\sin(\omega t)\,, & \pi \le t \le 2\pi \end{cases} \quad \text{V} \tag{33}$$

The drain current is zero when the drain voltage reaches its maximum value and then it is maximized when the drain voltage is at its minimum value.

The two waveforms do not overlap, resulting in zero power being dissipated in the active device, thereby fulfilling the first condition for a maximum *PE*, as derived in Chapter 2.

The drain current waveform can be expressed as a Fourier series given by:

$$i_D(t) = I_0 + \sum_{n=1}^{\infty} I_n \sin(n\omega t) \qquad \text{A} \tag{34}$$

Where the Fourier coefficient $I_n$ is determined for specific values of $n$ and given by:

$$I_n = \begin{cases} -\dfrac{4I_0}{\pi} & n = 1 \\ \dfrac{4I_0}{\pi}\dfrac{(-1)^{\frac{n+1}{2}}}{n} & n \text{ is odd} \\ 0 & n \text{ is even} \end{cases} \qquad \text{A} \tag{35}$$

The magnitude spectrum of this square wave drain current is shown in Figure 30.

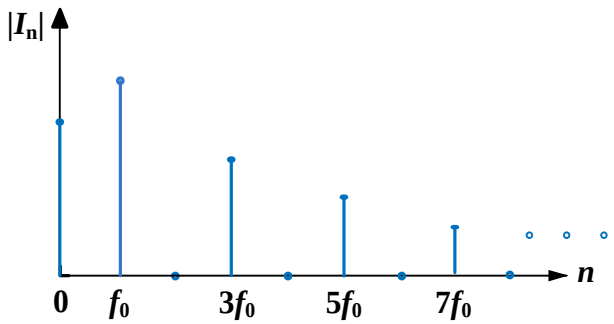



**Figure 30: Magnitude spectrum of the square wave drain current**

It should be noted that the magnitude spectrum of the drain current of a Class-F$^{-1}$ PA consists of the fundamental component and a series of odd harmonic components. The sum of an infinite number of these odd harmonic components will result in a square wave current waveform at the drain of the active device.

The drain voltage waveform can also be expressed as a Fourier series and given by:

$$v_{DS}(\omega t) = \frac{V_{Max}}{\pi} + \sum_{n=1}^{\infty} V_n \cos(n\omega t) \qquad \text{V} \tag{36}$$

Where the Fourier coefficient $V_n$ is determined for specific values of $n$ and given by

$$V_n = \begin{cases} \dfrac{V_{Max}}{2} & n = 1 \\ \dfrac{2\,V_{Max}}{\pi}\dfrac{(-1)^{\frac{n}{2}+1}}{n^2-1} & n \text{ is even} \\ 0 & n \text{ is odd} \end{cases} \quad \text{V} \tag{37}$$

The magnitude spectrum of this half sine wave drain voltage is shown in Figure 31.

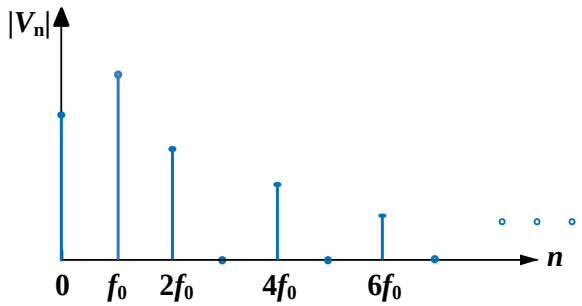



**Figure 31: Magnitude spectrum of the half sine wave drain voltage**

It should be noted that the spectrum of the drain voltage of a Class-F$^{-1}$ PA consists of the fundamental component and a series of even harmonic components. The sum of an infinite number of even harmonics will result in a half sine wave voltage at the drain of the active device.

Figures 30 and 31 show that the Fourier components with the same order $n$ are alternatively not present, resulting in zero power delivered to the load at all harmonic frequencies ($P_{RFout}(nf) = 0$, $n>1$), thereby fulfilling the second condition for a maximum *PE*.

Thus the Class-F$^{-1}$ PA meets the necessary and sufficient conditions to achieve a theoretical *PE* of 100 %, which can be mathematically proved as follows:

The amplitude of drain current at the fundamental frequency is given by:

$$I_1 = \frac{4I_0}{\pi} \quad \text{A} \tag{38}$$

The amplitude of drain voltage at the fundamental frequency is given by:

$$V_1 = \frac{\pi V_{DD}}{2} = \frac{V_{Max}}{2} \quad \text{V} \tag{39}$$

The output power at the fundamental frequency, assuming zero phase-shift between the drain voltage and current, is given by:

$$P_1 = \frac{1}{2} V_1 \times I_1 = \frac{V_{Max}}{4} \times \frac{4I_0}{\pi} = \frac{V_{Max}\, I_0}{\pi} \quad \text{W} \tag{40}$$

For an active device which is biased in Class-B mode, the DC power supplied is given by:

$$P_{DC} = V_{DD} \times I_{DC} = \frac{V_{Max}\, I_0}{\pi} \qquad \text{W} \tag{41}$$

Thus the theoretical *PE* is given by:

$$PE = \frac{P_1}{P_{DC}} \times 100 = \frac{V_{Max}\, I_0}{\pi} \times \frac{\pi}{V_{Max}\, I_0} \times 100 = 100\ \% \tag{42}$$

As in the case of a Class-F PA, the technique used to fulfil the two necessary and sufficient conditions for a maximum theoretical *PE* for a Class-$F^{-1}$ also raise the following questions:

How does one obtain the necessary harmonic content at the drain of the active device?

How is the harmonic content manipulated to achieve the desired drain waveforms?

Is it necessary to add up an infinite number of harmonics to obtain the desired waveforms?

The answers to these questions are presented in the following section.

As in the case of the Class-F PA, the presence of significant harmonic content is unavoidable at the drain of the active device under the condition that the drive signal of the PA is large enough.

According to Ohm's law, the amplitude of the drain voltage and current in Equations 35 and 37 respectfully are related by the impedance presented to the drain of the active device which is given by:

$$Z_n = \begin{cases} \frac{\pi^2}{8}\frac{V_{DD}}{I_0} = R_{opt} & n = 1 \\ 0 & n \text{ is odd} \\ \infty & n \text{ is even} \end{cases} \qquad \Omega \tag{43}$$

In a practical Class-$F^{-1}$ PA, only the fundamental component and the first two harmonics are controlled, thus leaving the higher order harmonics terminated through the shunting effect of the parasitic capacitance at the output port of the active device.

The lack of contribution of the higher order ($n$>3) harmonics result in a non-negligible overlap between the drain current and voltage, as illustrated in Figure 32, which leads to an increase in the power dissipated in the active device, thus a decrease in the maximum achievable *PE*.

According to (Paul & Johannes, 2011:41), reducing the drain current and voltage to only three harmonic components reduces the theoretical maximum *PE* to 90.6 %.

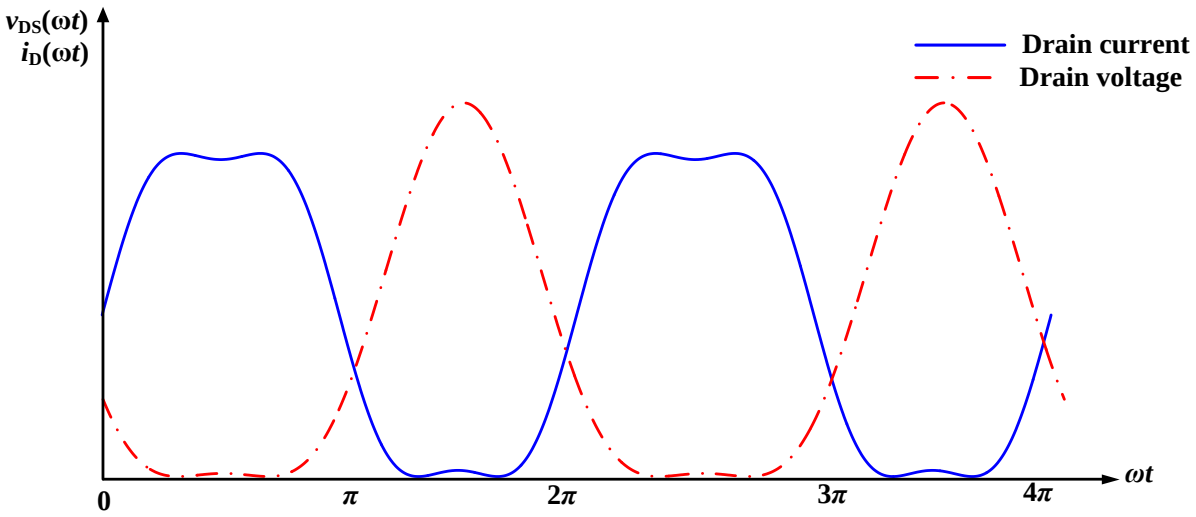



**Figure 32: Drain waveforms of a Class-F$^{-1}$ PA with second and third harmonics (Adapted from Grebennikov & Sokal, 2007: 152)**

## 3.4. Factors Limiting the Maximum *PE*

The maximum achievable theoretical *PE* of a PA is limited by the intrinsic and extrinsic active device parasitic elements such as: the output capacitance which is mostly represented by the drain-source capacitance ($C_{DS}$); the output series bond wire and lead inductance ($L_{out}$) and the output resistance of the active device, all of which set the upper limit for impedance that can be synthesized across the current source (Grebennikov, 2011:69; Colantonio *et al*., 2009: 272; Grebennikov & Sokal, 2007:129-131).

In the case of harmonically tuned PAs, the drain-source capacitance tends to short circuit the device output port at high frequency, thus preventing the required open circuit loading for higher order harmonics. The series output inductance of the active device makes it difficult to implement the required short circuit loading at higher order harmonics.

The ideal drain waveforms for both a Class-F and a Class-F$^{-1}$ PA can only be obtained if the spectral components of both the drain current and voltage have a well-defined magnitude and phase relationship. However, the parasitic elements of the active device affect the phase relationship of the spectral components and thus degrade the *PE* (Colantonio *et al*., 2009: 274).

Another factor that reduces the *PE* of a PA, is the fact that the minimum voltage within an active device is equal to or just above the knee voltage for a given current value (Paul & Johannes, 2011:41).

## 3.5. Class-F vs Class-F$^{-1}$ PA

The consequence of inter changing the drain waveforms of a Class-F PA to obtain a Class-F$^{-1}$ can be seen by comparing Equations 31 and 43. Under the same bias condition, the Class-F$^{-1}$ PA has a higher optimum resistance at the fundamental frequency when compared to that of the Class-F PA. A direct consequence of this observation is that the maximum amplitude of the drain voltage of a Class-F$^{-1}$ can exceed the supply voltage by about three times (Grebennikov & Sokal, 2007: 163-165), resulting in a higher output power level for the Class-F$^{-1}$ PA relative to the Class-F PA. The higher optimum resistance simplifies the output matching circuit by minimizing the impedance transformation ratio,

which is a very important design consideration for a high output power level when the load resistance is sufficiently small (Elisa, *et al*., 2010: 429:431).

A Class-F$^{-1}$ PA requires an active device with a higher breakdown voltage due to a higher drain voltage swing. However, this excess in the maximum drain voltage swing can be advantageous in PAs specifically used in CubeSats which have stringent DC supply voltage constraints. The DC supply voltage can be reduced to obtain a drain voltage swing within the acceptable limits of the active device while still achieving good performance.

When comparing the abovementioned facts, it was decided to design a Class-F$^{-1}$ PA for application in a CubeSat. The next section of this thesis document focuses on the wave-shaping networks used in a Class-F$^{-1}$ PA.

## 3.6. Wave-Shaping Networks for a Class-F$^{-1}$ PA

A wave-shaping network, which is also referred to as a load network or an output matching network, is a filter, the function of which it is to ensure that the drain of the active device of a Class-F$^{-1}$ PA is terminated with the optimum impedance at the fundamental frequency, an open circuit at even harmonic frequencies and a short circuit at odd harmonic frequencies. The wave-shaping network should also absorb the parasitic elements of the active device to minimize their effect on the *PE*.

### 3.6.1. Series Resonant Circuit with a Quarter Wavelength Transmission Line

The basic wave-shaping network for a Class-F$^{-1}$ PA consists of a *RLC* series resonant circuit connected in series with a quarter-wave impedance transformer, as shown in Figure 33 below.

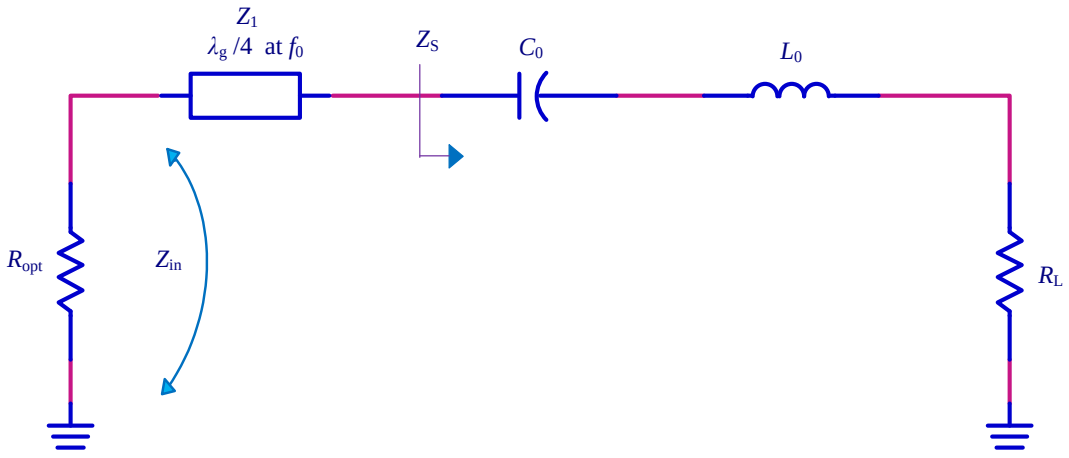



**Figure 33: Quarter-wave impedance transformer with a *RLC* series circuit**

The impedance presented to the quarter-wave impedance transformer is given by Equation 44 as:

$$Z_S = R_L + j\left(\omega L_0 - \frac{1}{\omega C_0}\right) \quad \Omega \tag{44}$$

The plot of the magnitude of $Z_S$ is shown in Figure 34 and illustrates the following properties:

At resonance, $|Z_S(f)|$ is purely resistive and is given by $|Z_S(f)| = R_L\ \Omega$, because the reactive part of Equation 44 adds to zero.
The magnitude of $Z_S$ is high at frequencies below and above the resonant frequency.

At frequencies below the resonant frequency, $|Z_S(f)|$ is capacitive, whereas at frequencies above the resonant frequency, $|Z_S(f)|$ is inductive.

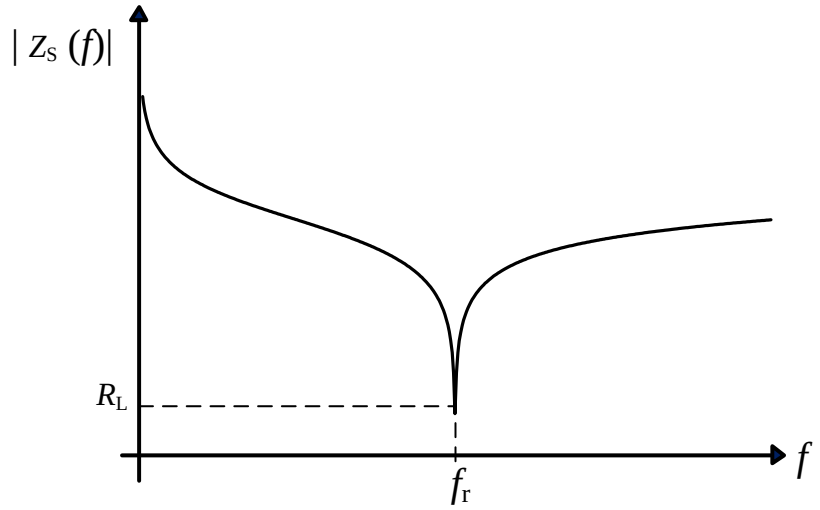



**Figure 34: Magnitude of impedance of a series resonant circuit**

The resonant frequency of a *RLC* series circuit can be calculated using Equation 45.

$$f_r = \frac{1}{2\pi\sqrt{LC}} \qquad \text{Hz} \tag{45}$$

Referring the Figure 33, the quarter-wave impedance transformer is loaded with a purely resistive impedance ($R_L$) at the resonant frequency, which is also the fundamental frequency. The quarter-wave impedance transformer will be loaded with a high impedance at all other frequencies.

At the fundamental frequency ( $f_0$) the impedance presented by the *RLC* series circuit to the quarter-wave transmission line is given by $Z_S = R_L\ \Omega$. Thus, the input impedance of the quarter-wave transmission line, which is also the input impedance of the wave-shaping network, is given by:

$$Z_{in} = \frac{Z_1{}^2}{Z_S} \qquad \Omega \tag{46}$$

To ensure that the load resistance is matched to the optimum resistance, that is, $Z_{in} = R_{opt}$ at the fundamental frequency, the characteristic impedance of the quarter-wave transmission line is given by:

$$Z_1 = \sqrt{R_{opt} \times R_L} \qquad \Omega \tag{47}$$

Since the series resonant circuit presents a high impedance at all harmonic frequencies, that is, at all frequencies off the resonant frequency, $Z_S$ can be considered to be an open circuit at all frequencies off the resonant frequency.

At even harmonic frequencies ($2nf_0$, with $n$ a positive integer and $0 < n < \infty$), the quarter-wave impedance transformer must have an electrical length of $\frac{2n\lambda_g}{4}$ and is terminated with an open circuit since $Z_S$ is high. According to Equation 46 the input impedance of the wave-shaping network, that is $Z_{in}$ , is an open circuit at all even harmonic frequencies.

At odd harmonic frequencies, ($(2n+1) f_0$, where is a $n$ a positive integer and $0 < n < \infty$), the quarter-wave impedance transformer has an electrical length of $\frac{(2n+1)\lambda_g}{4}$ and is terminated with an open circuit since $Z_S$.is high. According to Equation 46 the input impedance of the wave-shaping network must present a short circuit at all odd harmonic frequencies.

To illustrate the behaviour described above, the wave-shaping network in Figure 33 was designed at an operating frequency of 2.2 GHz. The optimum resistance value for a Class-F$^{-1}$ PA was then calculated as 90.428 Ω using Equation 43.

The series inductor $L_0$ was selected to be 1.5 µH and then the series capacitor $C_0$ was calculated as 3.489 fF using Equation 45. The characteristic impedance of the selected quarter-wave transmission line was determined, using Equation 47, as 67.241 Ω. The magnitude of the input impedance and the input reflection coefficient of the designed wave-shaping network were simulated in ADS and are shown in Figure 35.

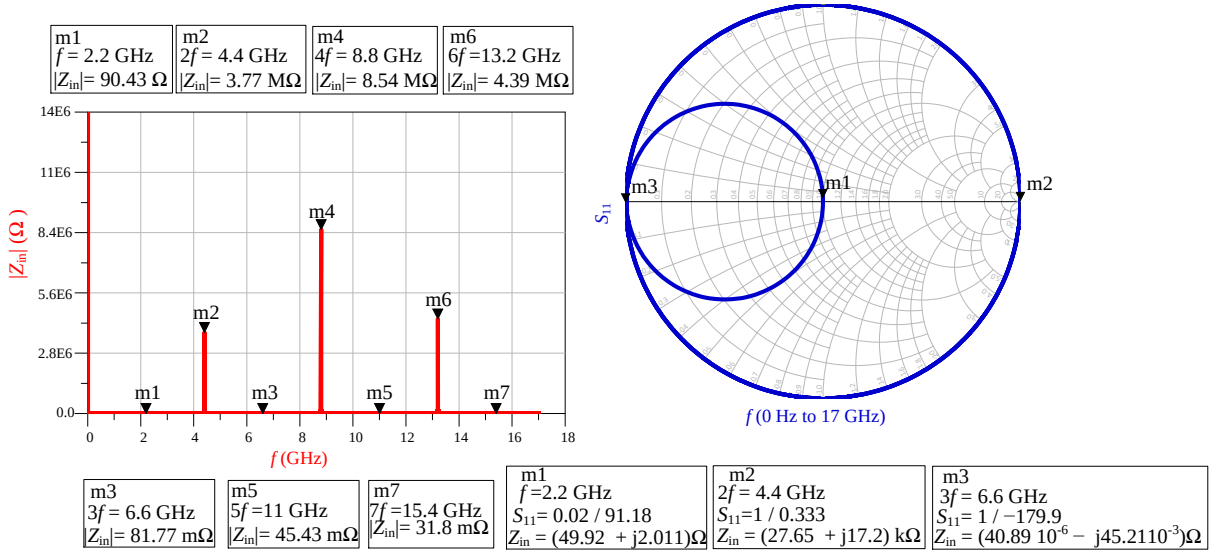



**Figure 35: Magnitude of input impedance and input reflection coefficient of the wave-shaping network**

Referring to Figure 35, markers 2, 4 and 6 show that the magnitude of the input impedances of the wave-shaping network are high enough to be considered as an open circuit at the 2nd, 4th and 6th harmonics. These facts are confirmed by marker 2 on the Smith chart. Markers 3, 5 and 7 show that that the magnitude of the input impedances of the wave-shaping network are low enough to be considered as a short circuit at the 3rd, 5th and 7th harmonics. Again, this is confirmed by marker 3 on the Smith chart. Marker 1 on the spectral plot and on the Smith chart shows that the load resistance is matched to the optimum resistance at the fundamental frequency. Clearly, the wave-shaping network meets the operational conditions of a Class-F$^{-1}$ PA.

However, it should be noted that the value of the series inductor $L_0$ must be high enough for the impedance $Z_S$ presented by the *RLC* series circuit to the quarter-wave transmission line section to

approximate an open circuit condition at all harmonic frequencies. The higher the value of the inductor $L_0$ , the lower the value of the required series capacitor $C_0$.

Higher values of inductors, that is, those in the µH range and lower values of capacitors, that is, those in the fF range, are difficult to manufacture at microwave frequencies and limit the practical implementation of this wave-shaping network.

It should also be noted that the wave-shaping network presented above does not account for the parasitic elements of the active device which will degrade the theoretical *PE* of the PA.

### 3.6.2. Transmission Line Wave-Shaping Networks

Several topologies of wave-shaping networks have been developed to achieve the operational conditions of a Class-$F^{-1}$ PA for many different applications. Most of these wave-shaping networks are reported by (Grebennikov, 2011:58-76) and have been analysed and studied in great detail. In this thesis, a new topology of wave-shaping network is proposed and motivated.

#### 3.6.2.1. The Proposed New Wave-Shaping Topology

The topology of wave-shaping network proposed in this thesis is shown in Figure 36 below.

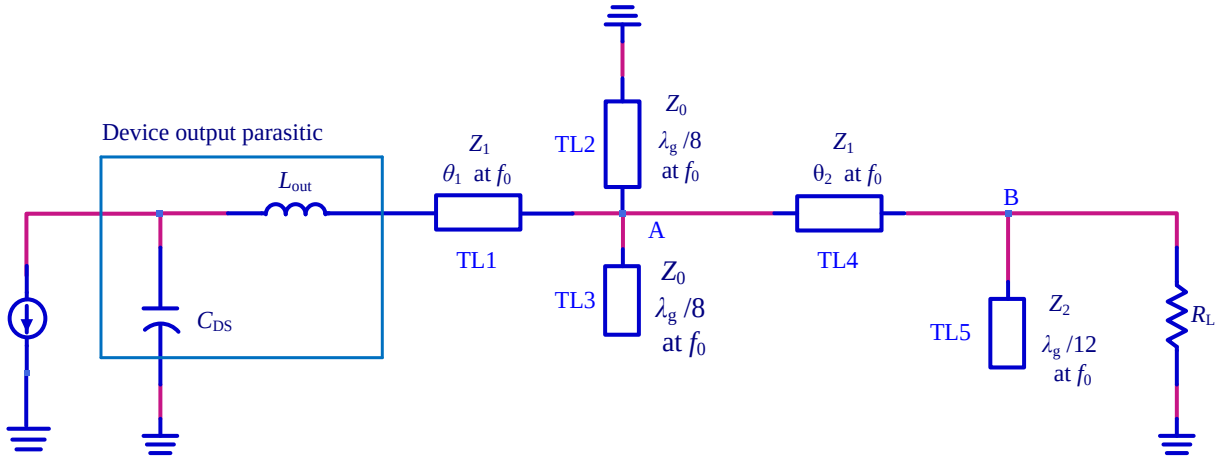



**Figure 36: The proposed new wave-shaping network**

In this topology the short circuited quarter-wave impedance transformer (section) used by (Grebennikov, 2011:70-74) is replaced with an open circuit eighth of a wavelength transmission line in parallel with a short circuited eighth of a wavelength transmission line.

The motivation for this topology is based on a comparison study between the performance of the quarter-wave impedance transformer and the parallel combination of open- and short-circuited eighth of a wavelength stubs. This comparison study was performed by (Mury, *et al*., 2015: 662), the results of which are as follows:

The rejection band of the parallel combination of an open and a short circuit one eighth of a wavelength stub is twice as large as that of the quarter-wave impedance transformer.

The length of the one eighth of a wavelength stub is half that of the quarter-wave section, thus a lower electrical series resistance (ESR) resulting in a better short circuit condition.

The reduced length of the proposed parallel combination of the two one eighth wavelength sections also reduces the physical size of the PA.

The operation the proposed wave-shaping network is described in the following section.

Referring to Figure 36, at the fundamental frequency ( $f_0$), the parallel combination of the short circuited transmission line TL2 and the open circuit transmission line TL3 presents an open circuit condition at point A, thereby reducing the wave-shaping network to the equivalent circuits shown in Figure 37 below. The subsequent lumped element equivalent circuit of that in Figure 37 (a) is shown in Figure 37 (b).

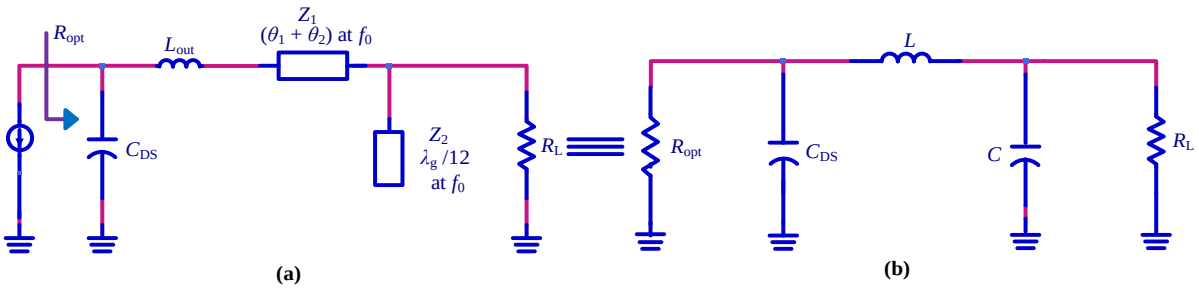



**Figure 37: Equivalent circuit of the wave-shaping network at the fundamental frequency**

Referring to Figure 37 (a), the 12th of a wavelength open circuit shunt stub can be modelled as a shunt capacitor whose value is given by:

$$C = \frac{\tan(30°)}{Z_2 \omega_0} \quad \text{F} \tag{48}$$

and denoted $C$ in Figure 37 (b). The series transmission line, $(\theta_1 + \theta_2)$ shown in Figure 37 (a), can be modelled as a series inductor with a value given by:

$$L = \frac{Z_1 \sin(\theta_1+\theta_2)}{\omega_0} + L_{out} \quad \text{H} \tag{49}$$

and denoted $L$ in Figure 37 (b). $C_{DS}$ and $L_{out}$ represent the parasitic elements of the active device and are provided by the manufacturer.

For the load resistance to match the optimum resistance at the fundamental frequency, the components of the resulting low pass π-type matching network can be calculated using Equations 50 and 51, which are derived in Appendix A.

$$C = \frac{Q_L}{R_L \omega_0} \quad \text{F} \tag{50}$$

$$L = \frac{R_{opt}}{\omega_0} \times \frac{Q_S+Q_L}{Q_S^2+1} \quad \text{H} \tag{51}$$

where the source quality factor $Q_S$ and the load quality factor $Q_L$ are given by Equations 52 and 53 respectfully, assuming that the load resistance is greater than the optimum resistance.

$$Q_S = R_{opt}\omega_0 C_{DS} \tag{52}$$

$$Q_L = \sqrt{\frac{R_L}{R_{opt}}\left(1+Q_S^2\right) - 1} \tag{53}$$

Again referring to Figure 36, at twice the fundamental frequency ($2f_0$), TL2 and TL3 have an electrical lengths of $\frac{\lambda_g}{4}$ each, thus the parallel combination of the short circuited transmission line TL2 and the open circuit transmission line TL3 presents a short circuit condition at point A. The resulting equivalent wave-shaping network is shown in Figure 38.

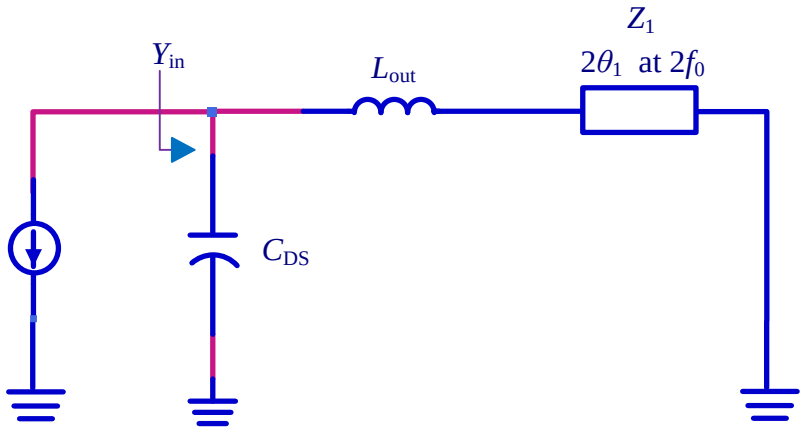



**Figure 38: Equivalent circuit of the wave-shaping network at the second harmonic frequency**

To achieve the required open circuit condition at the drain of the active device, the admittance $Y_{in}$ presented by the wave-shaping network and the parasitic components shown in Figure 38 must be equal to zero Siemens and mathematically expressed as:

$$j2\omega_0 C_{DS} - \frac{1}{j2\omega_0 L_{out} + jZ_1 \tan 2\theta_1} = 0 \quad \text{Siemens} \tag{54}$$

Again referring to Figure 36, at the third harmonic frequency ($3f_0$), TL2 and TL3 behave as at $f_0$ , that is, they present an open circuit condition at point A. The open circuit transmission line section TL5 has an electrical length of $\frac{\lambda_g}{4}$ and thus presents a short circuit condition at point B. The resulting wave-shaping network is equivalent to that shown in Figure 39.

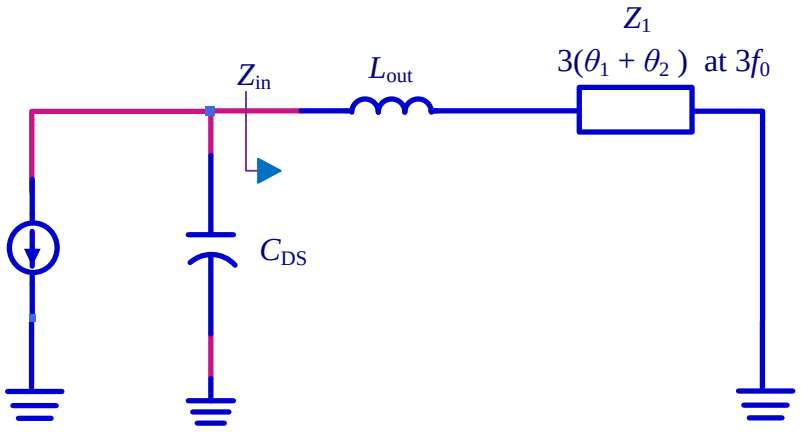



**Figure 39: Equivalent circuit of the wave-shaping network at the third harmonic frequency**

To achieve the required short circuit condition at the drain of the active, the impedance $Z_{in}$ presented by the wave-shaping network and shown in Figure 39, must be equal to zero Ω and mathematically expressed as:

$$j3\omega_0 L_{out} + jZ_1 \tan 3(\theta_1 + \theta_2) = 0 \qquad \Omega \tag{55}$$

For this condition to be true, $\theta_1 + \theta_2$ must be equal to 180° at the third harmonic, thus 60° at the fundamental frequency where the value of $L_{out}$ is considered to be negligibly small.

Manipulating Equations 49, 54 and 55 result in a set of two simultaneous equations with two unknowns, $\theta_1$ and $\theta_2$ as shown by Equations 56 and 57.

$$\sin(\theta_1+\theta_2) + \frac{2\omega_0^2 C_{DS}(L - L_{out})}{4\omega_0^2 C_{DS} L_{out} - 1}\tan(2\theta_1) = 0 \tag{56}$$

$$\sin(\theta_1+\theta_2) - \frac{(L - L_{out})}{3L_{out}}\tan 3(\theta_1+\theta_2) = 0 \tag{57}$$

The solutions of Equations 56 and 57 in terms of $\theta_1$ and $\theta_2$ will give the required electrical lengths of the transmission line sections for the wave-shaping network.

## 3.7. Conclusions

The Class-F and Class-F$^{-1}$ PA mode of operation employs a single technique to fulfil the two necessary and sufficient conditions for a maximum theoretical *PE*. However, the practical *PE* achievable in a Class-F and a Class-F$^{-1}$ PA is limited practically by the difficulty in controlling the infinite number of harmonics present at the drain and the difficulty in implementing open and short circuit impedances at multiple harmonic frequencies. This difficulty is due to the parasitic elements of the active device. Therefore there is a need for a trade-off between the number of harmonics to be controlled, the maximum achievable *PE* and the resultant circuit complexity. In a practical Class-F and Class-F$^{-1}$ PA, controlling only the lower order harmonics is more effective in improving the *PE* performance when compared to trying to control a higher number of harmonic. Due to the advantages

of a Class-$F^{-1}$ PA over a Class-F PA, as presented in section 3.5 of this thesis, the next Chapter will focus on the design a Class-$F^{-1}$ PA, where only the first, second and third harmonic components are controlled to maximise the *PE* using the proposed wave-shaping network as shown in Figure 36.

# Chapter 4

# Design of a Class-F$^{-1}$ PA at 2.2 GHz

## 4.1. Introduction

This Chapter presents the technique and the steps involved in the design of a Class-F$^{-1}$ PA using the Cree CGH40010F GaN power device. An appropriate DC bias point was selected by plotting the DC load-line of the power transistor in ADS. The wave-shaping network proposed in Chapter 3 is used to achieve the operational conditions of a Class-F$^{-1}$ PA. The input impedance of the power device was simulated and matched to the source impedance by means of an input matching network. The stability of the designed PA was analysed using linear and nonlinear simulation software. The layout of the printed circuit board (PCB) was generated within ADS and then EM method of moment (momentum) simulations and optimization were performed on the PCB. The simulated performance parameters of the designed Class-F$^{-1}$ PA were then presented and evaluated.

## 4.2. Specifications of the PA

The specifications of the PA are:

- $PE \geq 75$ % at 2.2 GHz.
- $PAE \geq 72$ % at 2.2 GHz
- $P_{RFout} \geq 40$ dBm at 2.2 GHz.
- $G_L \geq 13$ dB at 2.2 GHz

The above specifications were defined based on the performance of the Class-F$^{-1}$ presented by Grebennikov (2011:58-76).

## 4.3. Selection of an Active Device

As stated in Chapter 2, GaN HEMT power devices are suitable for use in a high efficiency PA. The Cree CGH40010F 10 W GaN HEMT power device was selected for this PA. The manufacturer provided samples and suitable linear and non-linear models of the GaN device. The Cree CGH40010F GaN active device is a very popular choice in state of the art PAs for CubeSat applications as published by Andrew & Christopher, (2012: 1-6). A photograph of the active is shown in Figure 40 below. The characteristics of the device are provided in the datasheet in Appendix C.


**Figure 40: The Cree CGH40010F 10 W GaN HEMT power transistor**

## 4.4. DC Bias Simulations

Ideally, the active device in a Class-F$^{-1}$ PA should be biased to operate near its cut-off region to generate a significant number of harmonics at the drain terminal. In this PA, the active device was biased at a drain current $I_D$ = 250 mA and a drain-source voltage $V_{DS}$= 28 V, as shown in Figure 41.

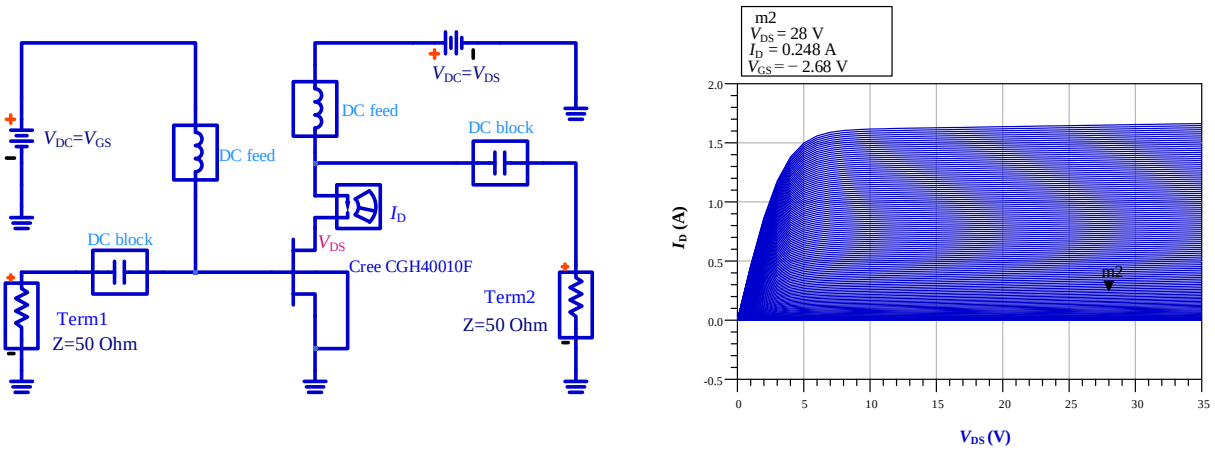



**Figure 41: Selected DC operating point**

## 4.5. Design of the Wave-Shaping Network

The proposed wave-shaping network in the previous Chapter was designed at 2.2 GHz. The optimum resistance value for a Class-F$^{-1}$ PA was determined using the load-line technique. That is, the optimum resistance is the ratio of the drain voltage and drain current at the fundamental frequency. Using Equation 43 gave a value of $R_{opt}$ = 90.428 Ω.

The drain capacitance and lead inductor of the GaN power device were obtained from the manufacturer as $C_{DS}$ = 1.3 pF and $L_{out}$ = 0.653 nH.

By using Equations 50 and 51, the values of the components of the low pass π-matching network were calculated as $C$ = 1.456 pF and $L$ = 4.728 nH respectively. The characteristic impedance of the transmission line TL5 was calculated as $Z_2$ = 28.686 Ω using Equation 48.

The approach to solve equations 56 and 57 in order to determine the appropriate values for $\theta_1$ and $\theta_2$ , was to assume that the parasitic lead inductance of the GaN active device was negligibly small. That is, $L_{out} \approx 0$ nH. The consequence of this assumption is that the maximum electrical length of transmission lines TL1 and TL4 is $\theta_1 + \theta_2 = 60°$. This assumption simplifies equation 49 into that shown in Equation 58 and the solution thereof provides the characteristic impedance values for transmission lines TL1 and TL4.

$$Z_1 = \frac{L\omega_0}{\sin(\theta_1+\theta_2)} \quad \Omega \tag{58}$$

With the assumption that $L_{out} \approx 0$ nH, $Z_1$ is thus a minimum when $\theta_1 + \theta_2 = 60°$ and Equation 58 becomes:

$$Z_1 = \frac{L\omega_0}{\sin(60°)} \quad \Omega \tag{59}$$

The solution for $Z_1$ is an approximation because in reality the parasitic lead inductance is not negligible. However, the approximate value obtained in solving for $Z_1$ allows for the use of simulation software to optimise for the exact value for $Z_1$. The value for $Z_1$ was calculated using Equation 59 as 65.043 Ω.

The electrical length of the transmission lines $\theta_1$ and $\theta_2$ for TL1 and TL4 were calculated using Equations 56 and 57 as 3.961° and 49.375° respectively. The characteristic impedance of the transmission lines TL2 and TL3 was selected as 50 Ω. To verify the theory presented in Chapter 3, the input and output return loss of the equivalent network at the fundamental frequency were simulated and optimised in ADS. The results shown in Figure 42, indicate that the optimum resistance is well matched to the actual load resistance at the fundamental frequency.

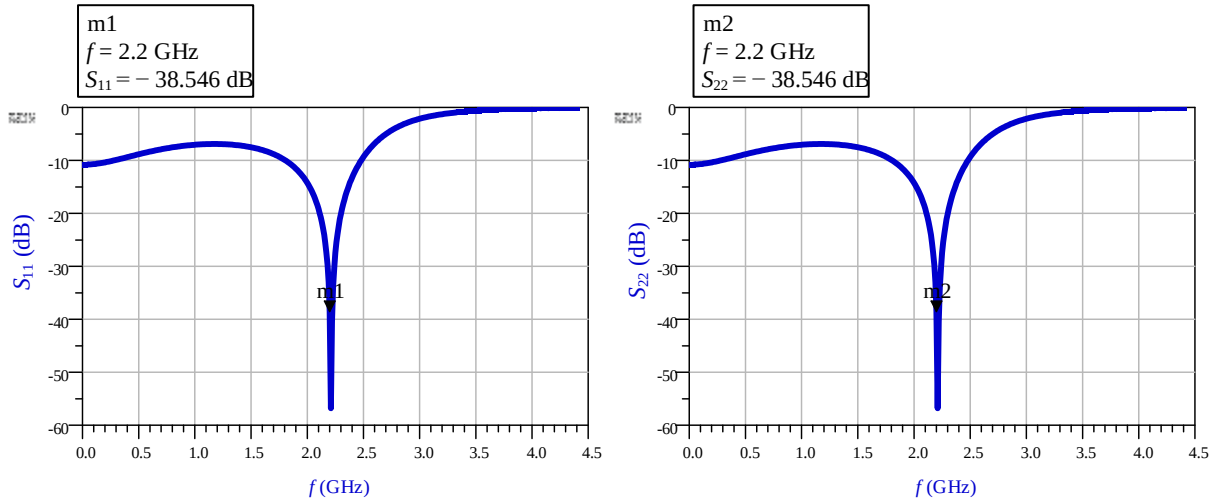



**Figure 42: Simulated input and output return loss at $f_0$**

The selection of the same characteristic impedance for transmission lines TL1 and TL4 was made to simplify the equations used to design the wave-shaping network. Hence, it was necessary to optimize the values of $Z_1$, $Z_2$ , $\theta_1$ and $\theta_2$ using ADS software. The results shown in table 3 indicate a close correlation between the calculated values and the optimized values.

**Table 3: Calculated vs. optimized values**

| Parameters | Calculated values | Optimized values |
|---|---|---|
| $Z_1$ (TL1) | 65.043 Ω | 70.06 Ω |
| $Z_1$ (TL4) | 65.043 Ω | 64.29 Ω |
| $\theta_1$ | 3.961° | 3.97° |
| $\theta_2$ | 49.375° | 47.972° |
| $Z_2$ | 28.686 Ω | 26.486 Ω |

The final optimised wave-shaping network is shown in Figure 43.

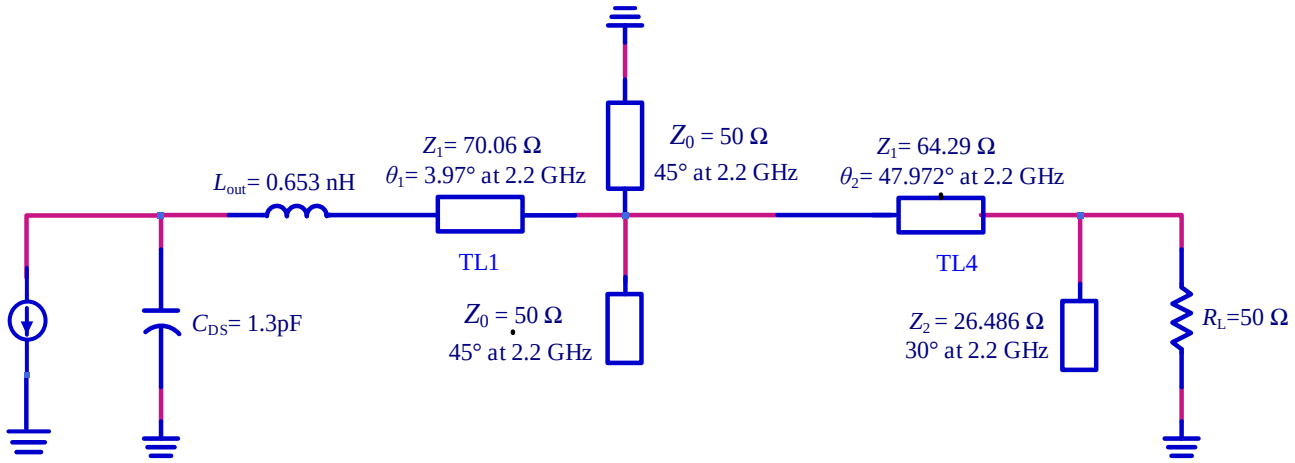



**Figure 43: Final optimised wave-shaping network**

ADS was used to perform the simulations on the wave-shaping network and the results are presented in Figure 44 below.

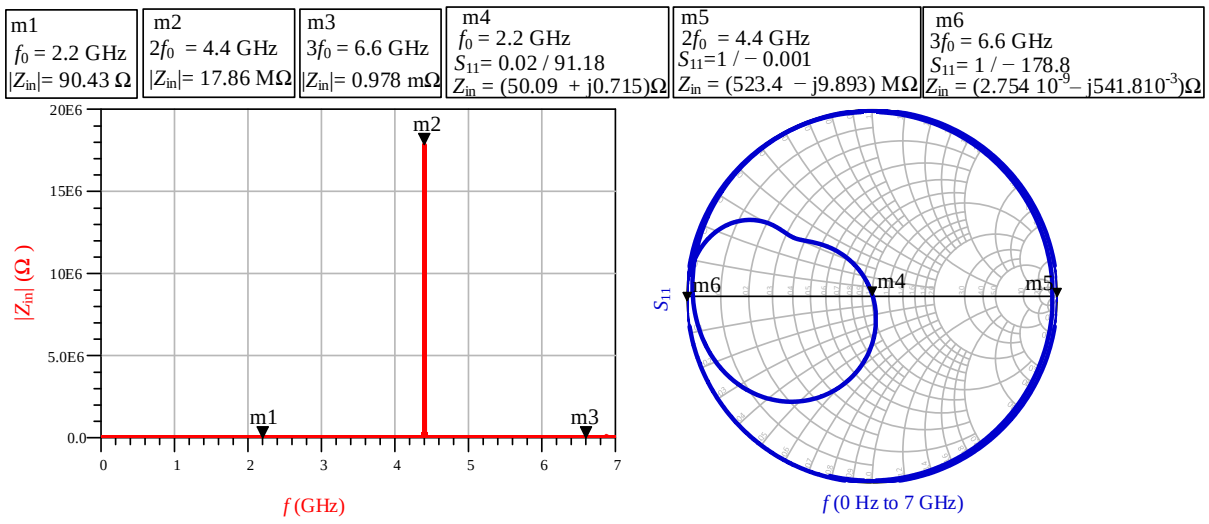



**Figure 44: Simulated input impedance of the wave-shaping network**

The simulated results for the input impedance of the wave-shaping network, which include the effects of the parasitic parameters of the active device, clearly show that the operational conditions of a Class-F$^{-1}$ PA have been achieved. Marker 1 shows that the input impedance of the wave-shaping network is equal to the required optimum impedance of 90.43 Ω for this Class-F$^{-1}$ PA. Marker 4 shows that the load resistance is matched to the optimum impedance at $f_0$ . The input impedance is 17.86 MΩ , which is high enough to be considered an open circuit at $2f_0$ , as shown by markers 2 and 5. The input impedance is 0.978 mΩ which is low enough to be considered a short circuit at $3f_0$ , as shown by markers 3 and 6.

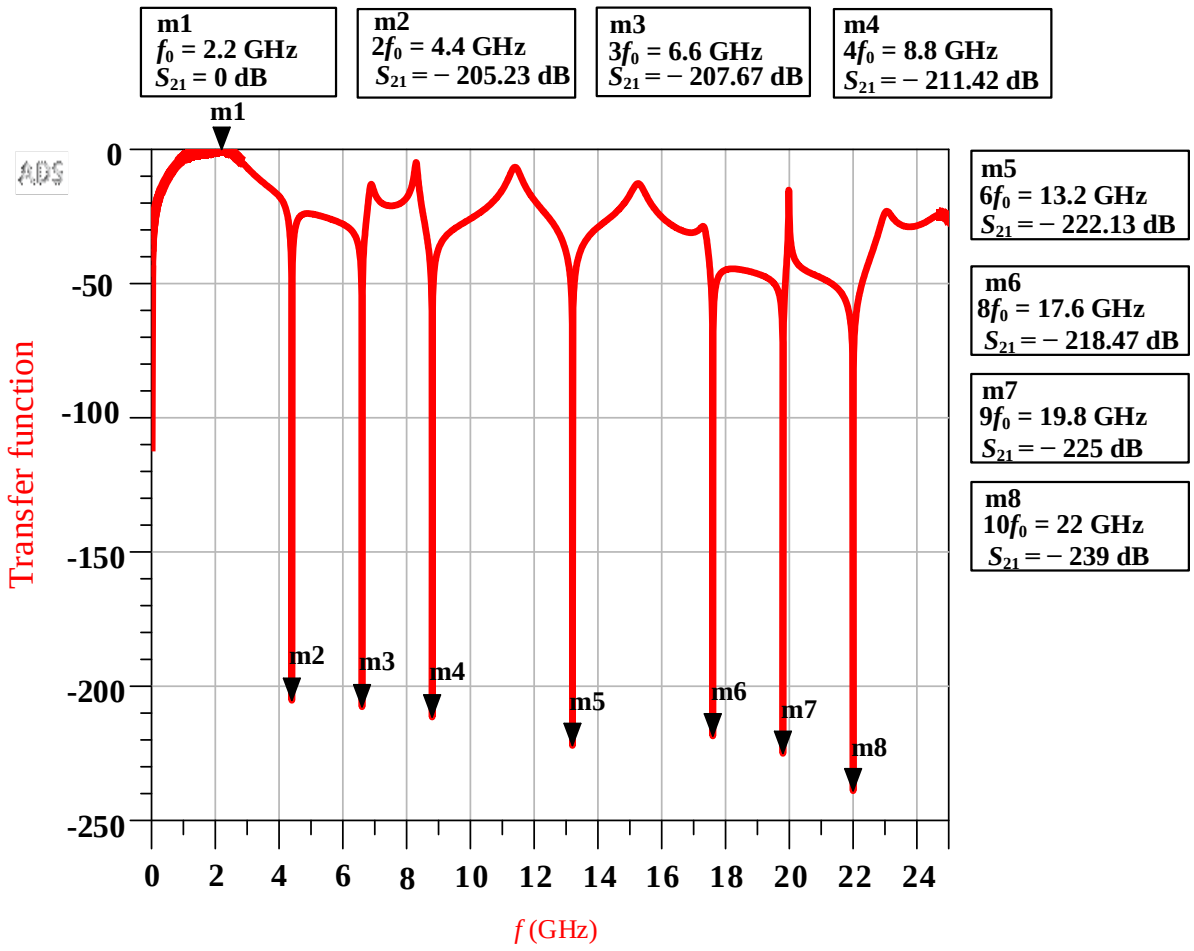



**Figure 45: Simulated transfer function of the wave-shaping network**

The simulated transfer function of the wave-shaping network indicates a maximum attenuation of 205 dB at 2 $f_0$ as shown by marker 2 and 207 dB at 3 $f_0$ as shown by marker 3. These results mean that this PA, with this particular wave-shaping network, exhibits excellent even and odd harmonic suppression and the power delivered to the load at these even and odd harmonic frequencies is significantly minimised. Also clearly indicated in Figure 45, is that the transfer function exhibits 0 dB attenuation at $f_0$ as indicated by marker 1, which means that maximum power available at the drain of the active device will be delivered to the load.

The transfer function of the wave-shaping network at higher harmonic frequencies reveals that the open circuit condition is fulfilled at even harmonic frequencies up to 10 $f_0$ as shown by markers 4, 5, 6 and 8. Hence, the drain voltage of the PA can be expected to be a good approximation of a half sine wave. The short circuit condition of the wave-shaping network occurs only at the 3$^{rd}$ and 9$^{th}$ harmonic frequencies, as shown by markers 3 and 7. Thus, the drain current will not be a good approximation of a square wave due to the lack of the 5$^{th}$ and 7$^{th}$ harmonic components.

## 4.6. Design of the Input Matching Network

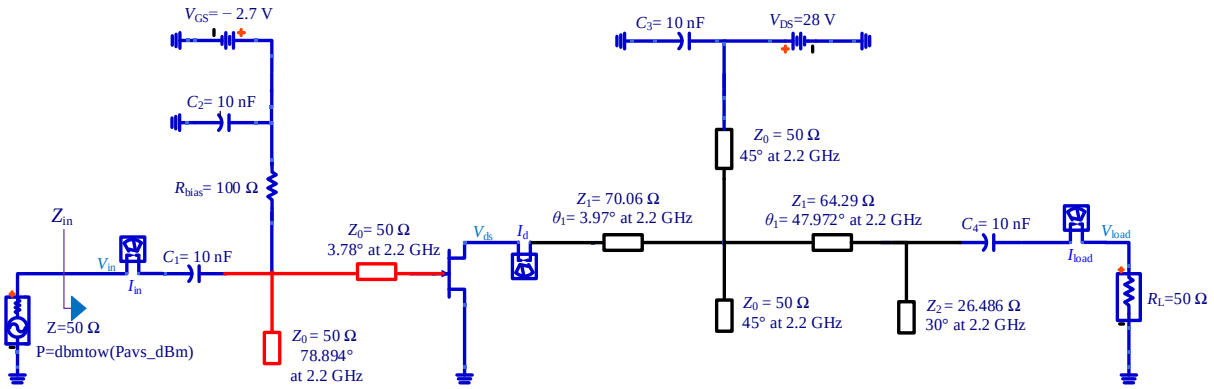



**Figure 46: Initial circuit of the designed PA**

The impedance presented by the input port of the PA to the source, as shown by the arrow in Figure 46, was simulated in ADS as 1.8 + *j* 6.064 Ω at 2.2 GHz and is shown by marker 1 in Figure 47

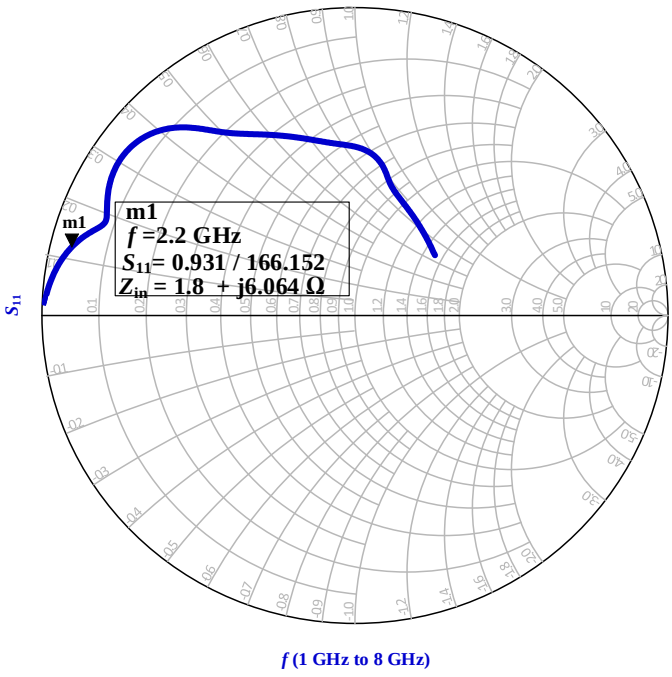



**Figure 47: Simulated input impedance of the PA**

An input matching network was designed to match the impedance presented by the input port of the PA to the 50 Ω source impedance.

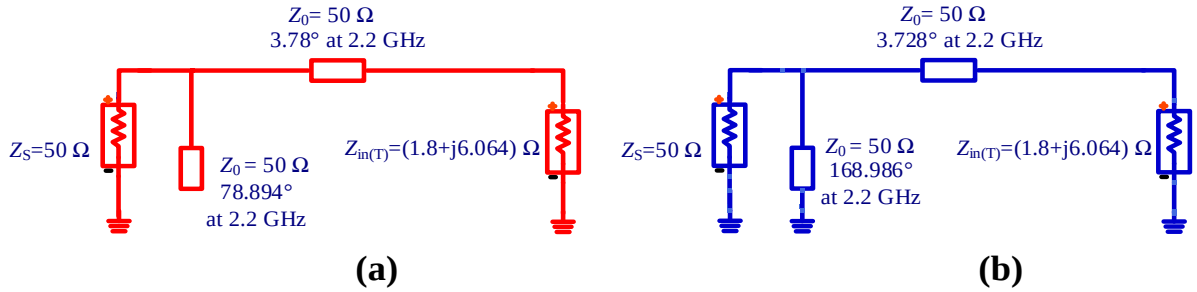



**Figure 48: Topologies of input matching network**

Two solutions were considered for the input matching network namely, a series stub followed by an open circuit shunt stub topology and a series stub followed by a short circuit shunt stub topology, both of which are shown in Figure 48. The appropriate electrical lengths of the transmission line sections were determined using the Smith chart utility within ADS, resulting in the matched conditions illustrated in Figure 49.

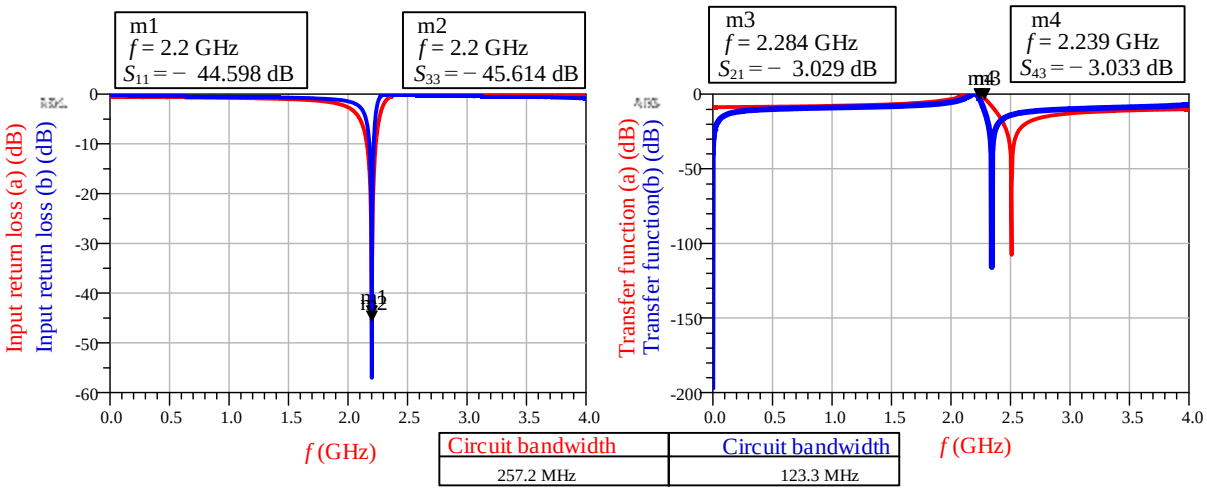



**Figure 49: Input return loss and TF (transfer function) of the input matching networks**

The simulated input return losses show that the input impedance of the PA is well matched to the source impedance for both matching circuit topologies. The maximum available power at the source will be transferred to the input port of the PA, thus providing the necessary large drive signal to achieve the Class-F$^{-1}$ mode of operation.

Comparing the response curves of each matching network shows that the matching network with the open circuit shunt stub has a wider circuit bandwidth relative to that circuit which uses the short circuit shunt stub. This condition is due to the shorter electrical length of the open circuit stub relative to that of the short circuit stub (Pozar, 2012: 234-237). The shorter electrical length of the open circuit shunt stub will result in a physically smaller PA relative to that which uses a short circuit shunt stub. The practical implementation of the short circuit shunt stub requires the use of a capacitor, thus adding slight complexity to the PA.

Thus, for the reasons mentioned above the matching network topology consisting of a series stub followed by an open circuit shunt stub was selected for the input matching network.

## 4.7. Initial Simulated Performance Parameters

The initial circuit schematic of the PA is shown in Figure 50 which clearly illustrates the input matching network, the active device, the wave-shaping network and load and source terminations.

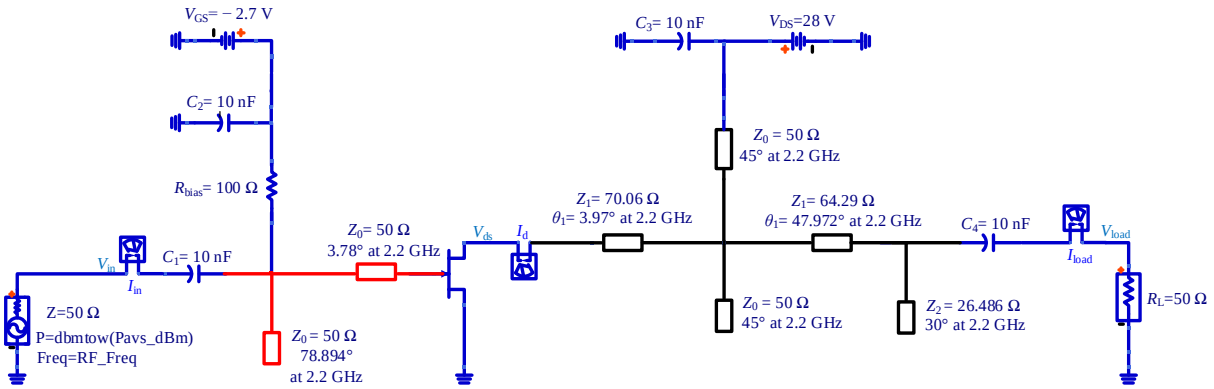



**Figure 50: Initial circuit schematic of the PA with input matching network**

ADS software was used to perform harmonic balance simulations on this circuit. The source power was set to 29 dBm to ensure a large enough drive signal to verify the correctness of design technique employed and the operation of the PA. The simulated drain voltage and current waveforms are shown in Figure 51.

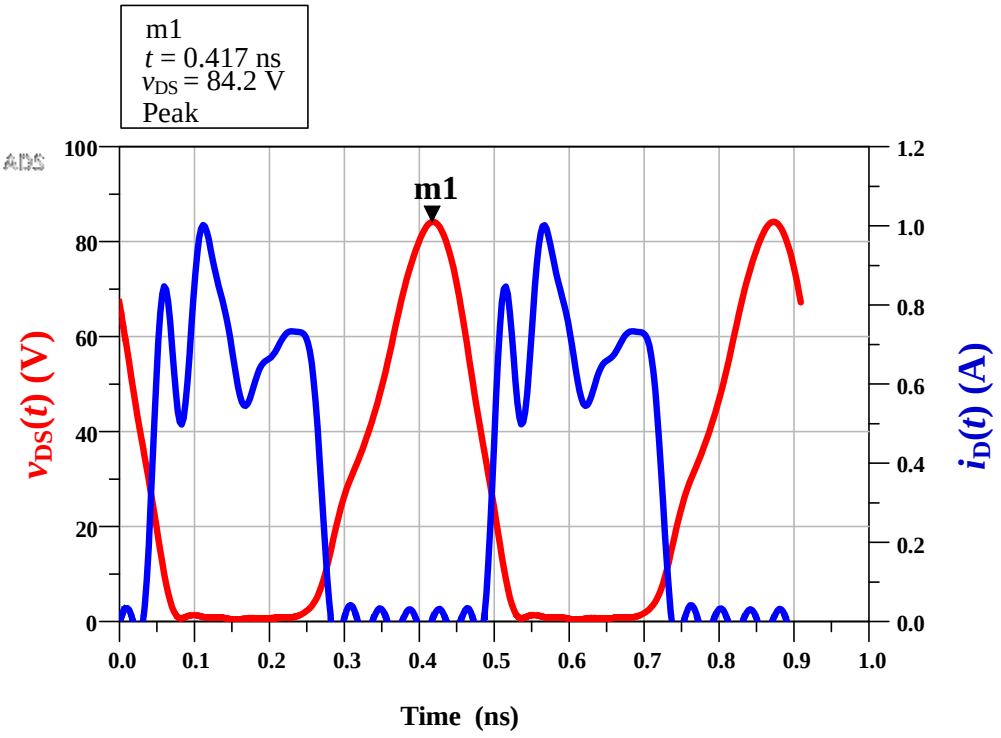



**Figure 51: Simulated drain waveforms**

The shape of these waveforms confirm that the circuit is in fact a Class-$F^{-1}$ PA, that is, the drain voltage is a half sine wave and the drain current resembles a square wave. The half sine wave is as expected due to the open circuit condition in the wave-shaping network being fulfilled at all even harmonic frequencies. The drain current is an approximation of a square wave due to the lack of contribution of the higher order odd harmonic frequency components.

It should also be noted that the peak value of the drain voltage is 84.2 V. This is 3 times higher than the supply voltage which confirms one of the main advantages of the Class-$F^{-1}$ PA as stated in Chapter 3.

The simulated performance parameters for *PE*, *PAE*, $P_{RFout}$ and $P_{DC}$ are shown in Figure 52.

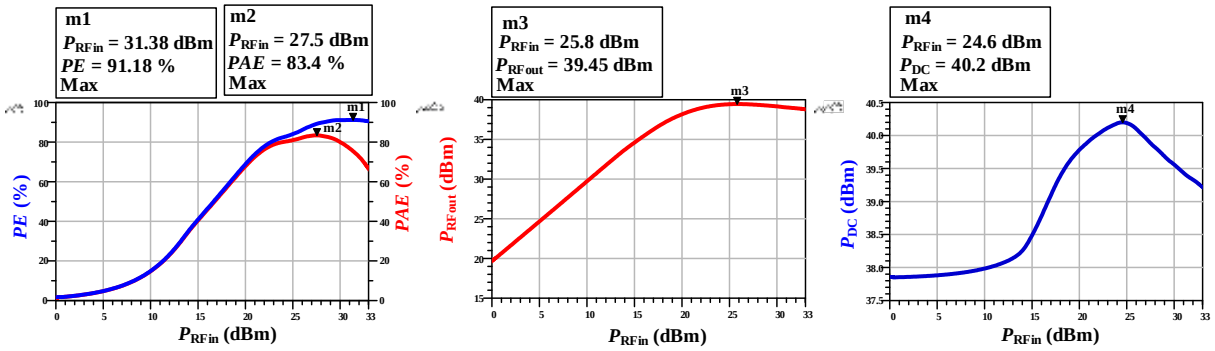



**Figure 52: Initial simulated *PE*, *PAE*, $P_{RFout}$ and $P_{DC}$.**

The simulated results show that the PA has a maximum *PE* of 91.18 % at an input power level of 31.38 dBm as shown by marker 1 and a maximum *PAE* of 83.4 % at an input power level of 27.5 dBm as shown by marker 2. A maximum output power level of 39.45 dBm is delivered to the load as shown by marker 3. The maximum DC power consumed by the PA was 40.2 dBm as shown by marker 4.

This PA has achieved a maximum *PE* just above the theoretical maximum *PE* achievable as stated by (Paul & Johannes, 2011:41). Thus the correctness of the operation of the PA has been verified and hence the design technique employed.

However, the results presented above are obtained under ideal simulation conditions. The practical implementation of the PA requires the use of real world components plus the addition of interconnecting PCB tracks, that is, transmission lines as shown in Figure 53.

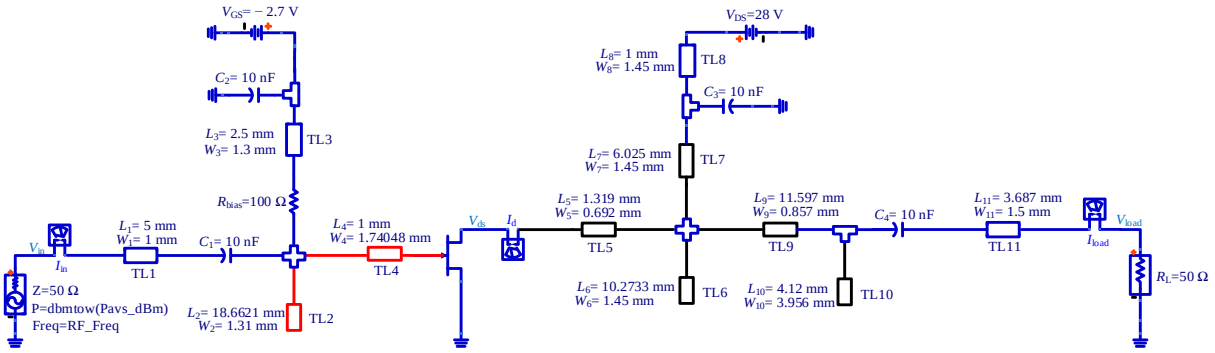



**Figure 53: Final schematic diagram of the designed PA**

The physical width and lengths of the interconnecting transmission line sections were synthesized using the LineCalc tool within ADS. The addition of these interconnecting transmission line PCB tracks necessitated the optimisation of the input matching network and the wave-shaping network to include the effect of the added transmission lines.

## 4.8. PCB Layout and Momentum Simulations.

The physical layout of the actual PCB for the designed PA was generated and edited using the layout program within ADS on Rogers RO4003C substrate and is shown in Figure 54.

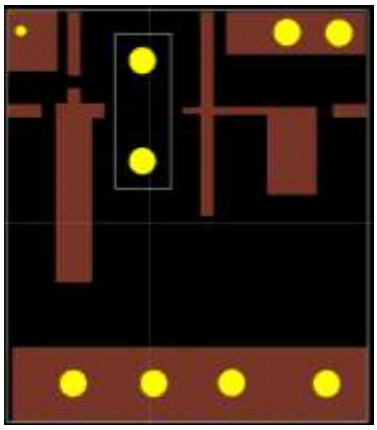


**Figure 54: PCB layout of the designed PA**

A momentum simulation was performed resulting in a generated *S*-parameter model of the actual PCB and substrate used. The layout model of the PCB was then populated with vendor supplied models of the actual components used and this complete circuit was then simulated using the EM method of moment (momentum) in ADS. The simulated performance parameters of the optimized PA circuit, that is, the PA circuit which is as realistically and practically as close to the real world situation as possible, are presented in Figures 55, 56, 57, 58, 59 and 60 below.

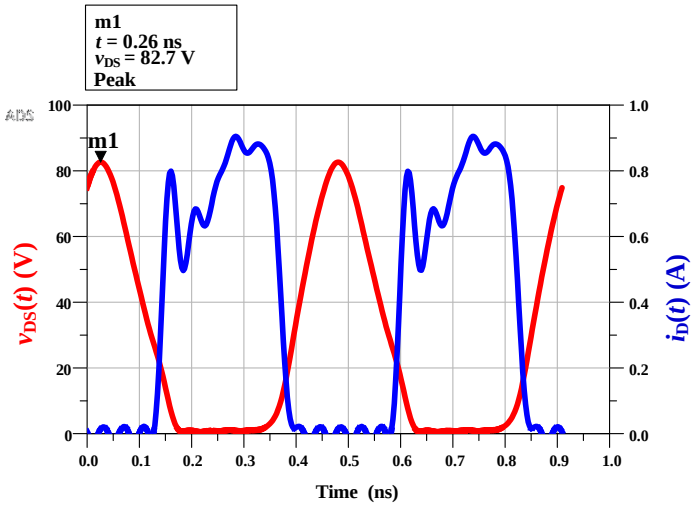



**Figure 55: Simulated drain voltage and current waveforms**

The simulated drain voltage and current waveforms of the optimised layout PA circuit as shown in Figure 55 again confirm the correct operation of a Class-F$^{-1}$ PA.

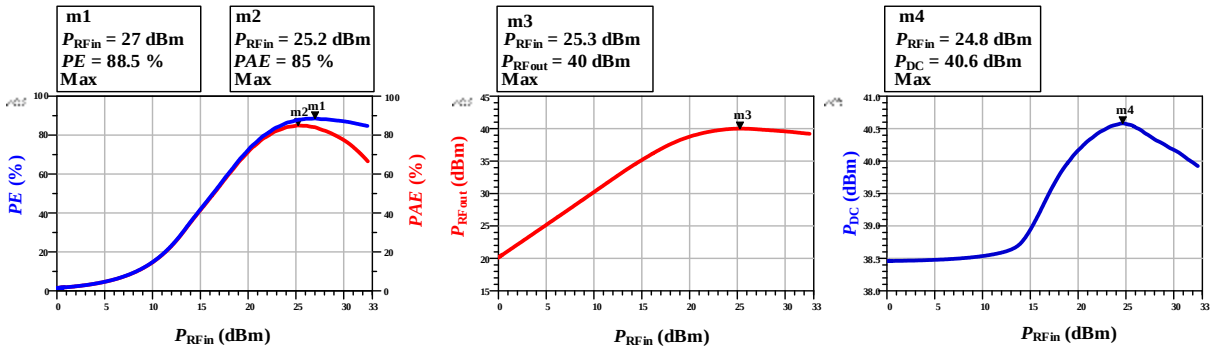



**Figure 56: Simulated *PE*, *PAE*, $P_{RFout}$ and $P_{DC}$**

Figure 56 shows that the optimised PA achieves a maximum *PE* of 88.5 % at an input power level of 27 dBm as shown by marker 1. In other words, 88.5 % of the supplied DC power is converted into useful RF power and only 11.5 % thereof is dissipated as heat. The optimised PA achieves a maximum *PAE* of 85 % as shown by marker 2 in Figure 56 when driven at an input power level of 25.2 dBm. Marker 3 shows that the optimised PA achieves a maximum output power of 40 dBm when driven at an input power of 25.2 dBm. The maximum DC power level consumed by the optimised PA is 40.6 dBm.

In order to determine the degree of compression of the PA when it is driven at a high input power level for maximum *PE*, the $IP_{1dB}$ and the $OP_{1dB}$ performance parameters were evaluated and are shown in Figure 57.

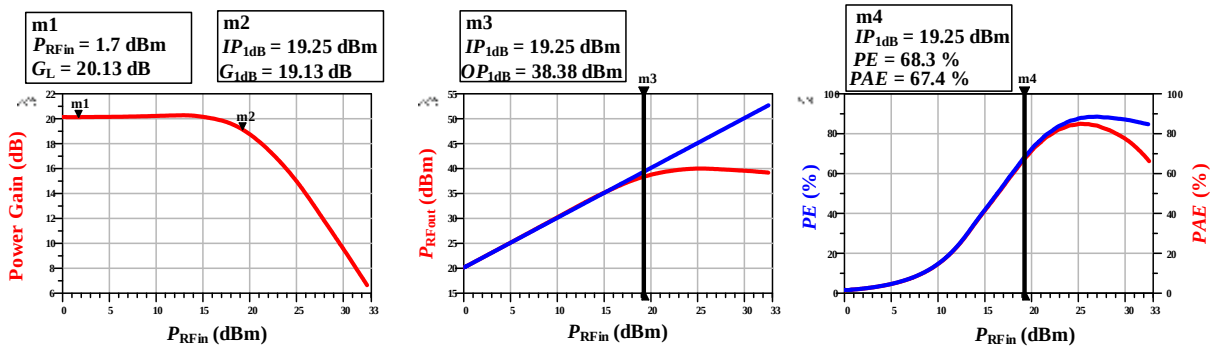



**Figure 57: Simulated $IP_{1dB}$ and $OP_{1dB}$ of the optimised PA**

The $IP_{1dB}$ and $OP_{1dB}$ of the optimised PA are 19.25 dBm and 38.38 dBm as shown by markers 2 and 3 respectively. These results confirm that the maximum *PE* and *PAE* are obtained at input power levels greater than the $IP_{1dB}$ . This confirmation is expected since a high input power level is required to obtain the significant amount of harmonics that are necessary to generate the required Class-F$^{-1}$ drain waveforms (Colantonio *et al*., 2009: 268-270). This optimised PA achieves a *PE* of 68.3 % and a *PAE* of 67.4 % at the $IP_{1dB}$ as shown by marker 4 in Figure 57.

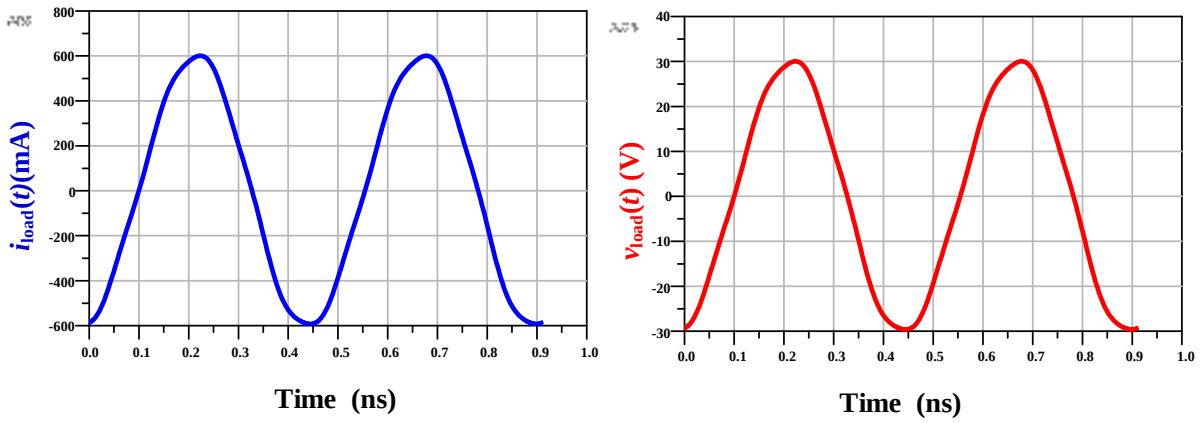



**Figure 58: Simulated load voltage and current waveforms.**

Figure 58 shows the voltage and current waveforms developed across the load. They are almost purely sinusoidal waveforms and are due to the attenuation of the higher order harmonic components in the drain voltage and current waveforms by the wave-shaping network.

To evaluate the bandwidth performance of this PA, the variation in *PE* and in *PAE* were simulated from 2 GHz to 2.4 GHz. The results of this exercise are shown in Figure 59.

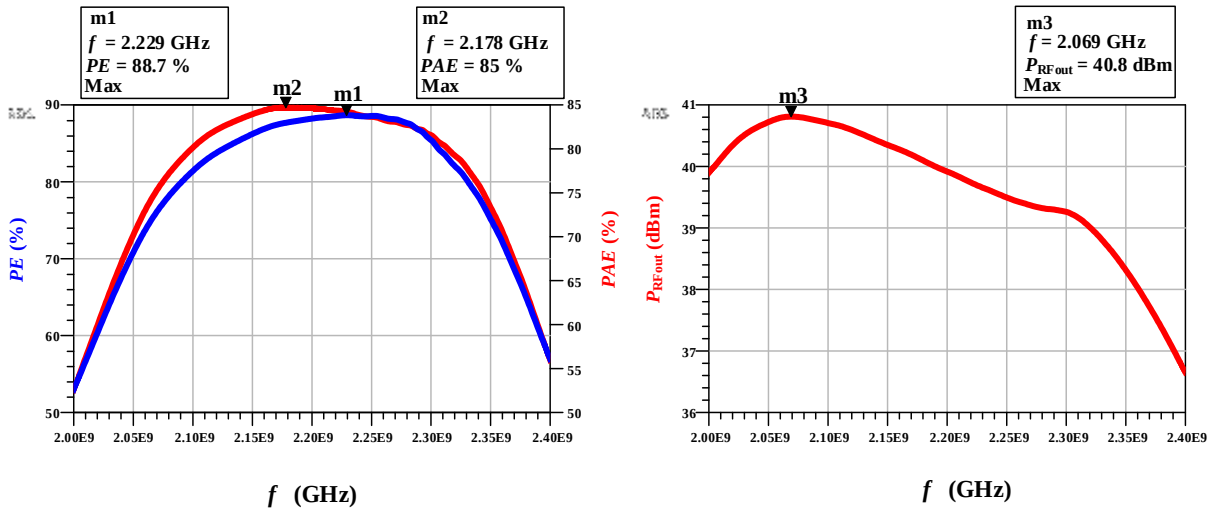



**Figure 59: Simulated performance parameters of the optimised PA vs. frequency**

Figure 59 shows that this PA achieves a *PE* above 80 % and a *PAE* above 75 % from 2.1 GHz to 2.3 GHz, which covers the portion of *S*-band used for a satellite up and downlink communication channel. This PA achieves also a *PE* and *PAE* above 50 % from 2 GHz to 2.4 GHz. An output power above 36.5 dBm is obtained from 2 GHz to 2.4 GHz thus indicating the usefulness of this PA for wider bandwidth applications. A maximum *PE* of 88.7 % is obtained at 2.229 GHz as shown by marker 1 and a maximum *PAE* of 85 % is obtained at 2.178 GHz as shown by marker 2. A maximum output power of 40.8 dBm is obtained at 2.069 GHz as shown by marker 3

The optimised PA was then subjected to power supply stress tests to evaluate the performance under the conditions of power supply variations which are common on a CubeSat. These simulated results are shown in Figure 60.

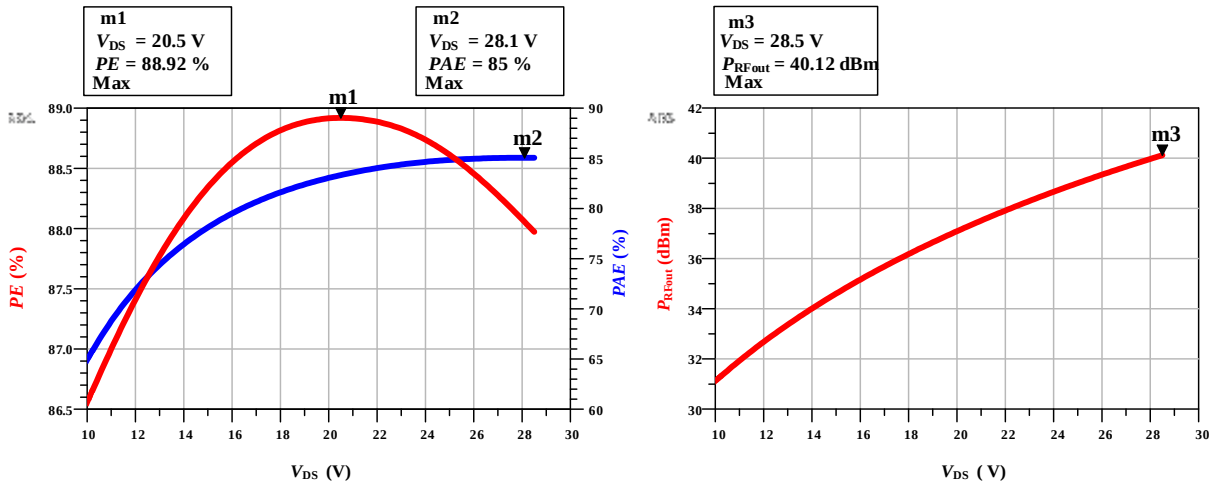



**Figure 60: Simulated performance parameters of the optimised PA vs the DC supply voltage**

The results in Figure 60 show that this PA delivers a *PE* above 86 %, a *PAE* above 60 % and an output power above 31 dBm when the DC supply voltage is swept from 10 V to 28 V. These results show that this PA still performs well above the 25 % *PE* of the existing PA as used on ZACUBE-1 even when the DC supply voltage drops to as low as 10 V.

## 4.9. Stability Analysis of the Class-F$^{-1}$ PA

The instability, that is, the tendency of a PA to oscillate, is a major design consideration that needs to be taken into account during the design stage. The presence of spurious oscillation is due to the existence of feedback loops associated with high level in and out of band gain. The instability observed in a PA depends on the DC bias and the power level of the input signal required to drive the PA (Jeon, *et al*., 2005).

The causes of and an in-depth analysis of instability, including the type of instabilities encountered in a PA, are beyond the scope of the work presented in this thesis. A more detailed analysis of instability in a PA can be found in the work presented by (Suárez & Quéré, 2003), (Jeon, *et al*., 2005) and (Suárez & Ramírez, 2013). However, to obtain accurate information on the stability of a PA early in the design stage, the use of appropriate tools and techniques is required. The work presented in this section focuses on the results of using the stability analysis tool (STAN) software, kindly made available by AMCAD Engineering and developed by CNES and University of Bilbao. This software provided accurate information on the stability of the PA designed in the thesis. These stability parameters were then compared to traditional linear stability criteria to get an indication of the stability of this PA.

### 4.9.1. Linear Stability Analysis

Linear stability techniques consist of determining the stability of a linear two port network such as a small signal amplifier, by investigating factors such as the Rollett stability factor ($K$), the Linville stability factor ($\mu$) and the determinant of the scattering parameters ($\Delta$) of a two port network. The Equations of these factors and resulting conditions for stability are presented below.

$$K = \frac{1 - |S_{11}|^2 - |S_{21}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{60}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{61}$$

An active device is said to be unconditionally stable, that is, the active device can be terminated with any impedance, including and open and a short circuit, without oscillation if the conditions in Equation 62 are simultaneously fulfilled.

$$K > 1 \text{ and } |\Delta| < 1 \tag{62}$$

Otherwise the active device is said to be potentially unstable, that is, the active device might oscillate if terminated in some values of impedance.

The Linville stability factor ($\mu$) is a single and sufficient measure of stability of a two port network. For unconditional stability of an active device, the condition in Equation 63 must be fulfilled.

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1 \tag{63}$$

These factors are used to graphically measure the distance from the centre of the Smith chart to points on an input or output stability circle, representing values of impedances that might cause an active device to oscillate (Dellier, 2012).

It should be noted that the $K$, $\mu$ factors and $\Delta$ are based on the linear $S$-parameters of an active device biased to operate in its linear region. Thus, applying this technique to detect instabilities in a PA which exhibits a nonlinear behaviour might provide misleading results, given that only instabilities depending on the DC bias will be detected. For comparison purposes this technique is used to determine the stability of the designed PA.

The mu(S), stab_fact(S) built in functions in ADS were used with the $S$-parameters simulator to generate plots of the $\mu$ factor and the $K$ factor for the designed PA at frequencies ranging from 0 GHz to 6 GHz.

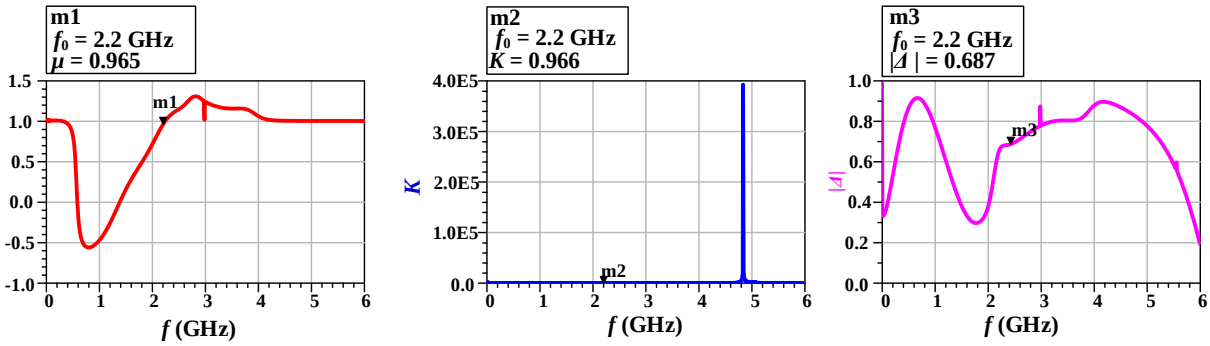



**Figure 61: Simulated stability criteria of the designed PA**

The simulated results shown in Figure 61 shows that the $\mu$ and $K$ factors are less than 1 from 0 GHz to 2.26 GHz and greater than 1 from 2.27 GHz to 6 GHz. Thus, the designed PA is potentially unstable from 0 GHz to 2.26 GHz.

#### 4.9.1.1. Nonlinear Stability Analysis Using ADS and the STAN Tool

In order to obtain meaningful stability parameters by using the STAN tool provided by AMCAD engineering, a particular sequence of steps must be followed.

The first step consists of selecting an appropriate node in the circuit for analysis and then connecting a current source to the selected node. According to (Dellier, 2012), in a simple circuit with clear feedback structure any node can be selected for analysis.

The second step consists of running the appropriate simulation in ADS to obtain the frequency response of the designed PA.

The third and last step consists of plotting the poles and zeros of the transfer function associated with the frequency response of the designed PA using the STAN tool.

The circuit is said to be stable if no pole is located in the right half plane (RHP) of the plotted transfer function. That is, if there are no poles with a positive real part, the PA is deemed stable (Dellier, 2012).

The presence of a pair of complex conjugate poles with positive real parts indicate that the circuit is unstable and the possible start-up of an oscillation at the frequency given by the imaginary part of the poles.

According to (Dellier, 2012), the results of pole and zero identifications can provide poles and zeros located in the same position. This effect is called quasi-cancellation and does not allow a clear determination of whether or not the PA is stable. To avoid quasi-cancellation, it is advised to select the nodes closest to the input and/or output port of the active device for simulation. That is, select the gate and/or the drain of the active device as the nodes for stability simulations of the PA.

The non-linear stability technique is based on the detection of changes in the behaviour of the PA when one or two parameters such as the input power level, the DC bias, the frequency of the input signal and circuit element are varied. Such changes can be observed by analysing the poles and zeros of the transfer function governing the PA. An in depth analysis of this technique is presented by (Suárez & Ramírez, 2013).

A multi-node analysis was performed on the optimised PA to determine if any instability exists, the nature of the instability if any and its location in the circuit. The gate and drain of the active device were selected as nodes for analysis. The frequency of the input signal was swept from 0 GHz to 6 GHz and the input power level was set to 25 dBm. The simulated results generated by the STAN tool are shown in Figure 62.

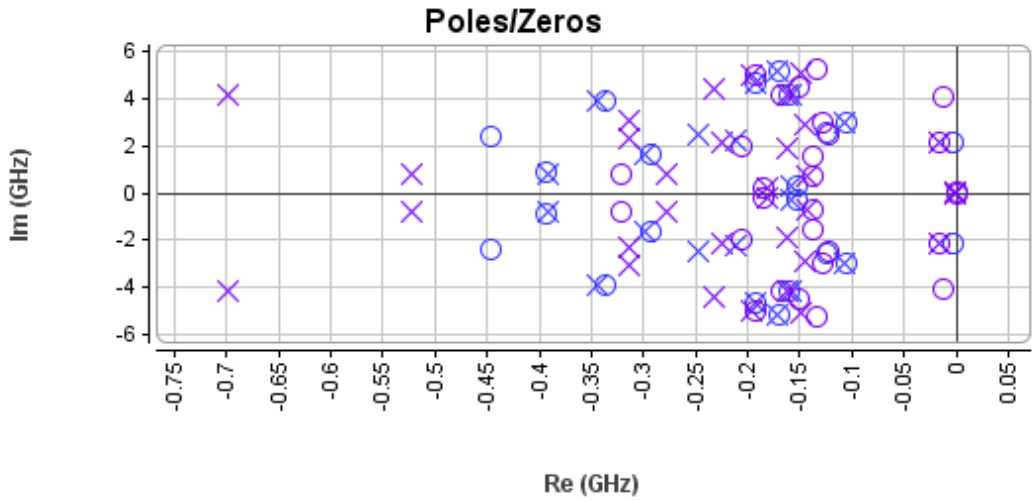



**Figure 62: Plot of poles and zeros in the complex plane of the transfer function of the PA**

There are no poles in the right half of the complex plane thus the PA is deemed stable from 0 GHz to 6 GHz, when driven at an input power level of 25 dBm. However, this multi-node analysis was performed at a single input power level and does not indicate the stability behaviour of the designed PA at other input power levels. Hence the need to sweep the input power level and check the stability of the PA at these different input power levels.

The frequency of the input signal was swept from 0 GHz to 6 GHz and the input power level was swept from 0 dBm to 30 dBm. The results of this identification process are shown in Figure 63.

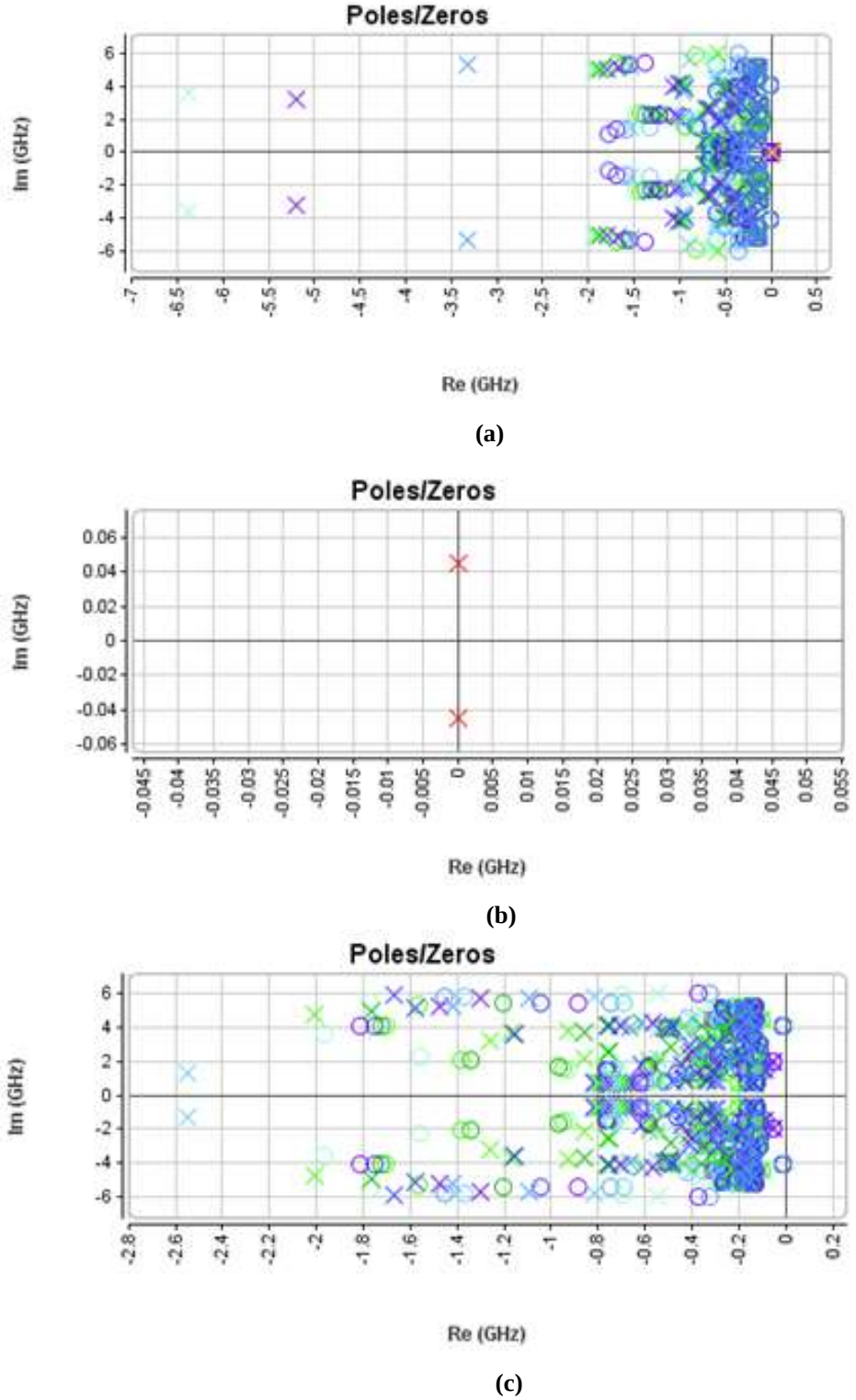



**Figure 63: Poles and zeros in the complex plane for swept input power and frequency**

Figure 63 (a) shows the plot of the PA transfer function poles and zeros as the power is swept from 0 dBm to 30 dBm and the frequency is varied from 0 GHz to 6 GHz. Due to the density of this pole-zero plot it was decided to magnify the area close to zero on the real axis for a more clear and unobstructed view. Figure 63 (b) shows the magnified section of the real and imaginary axis which clearly illustrates the location of unstable poles at a frequency of 50 MHz. To further confirm this

result, the frequency of the input signal was now only swept from 500 MHz to 6 GHz which excludes the 50 MHz frequency at which instability occurs. The results of this simulation shown in Figure 63 (c) which clearly illustrate that there are no poles on the right half of the complex plane and the designed PA is deemed stable from 500 MHz to 6 GHz with the input power level swept from 0 dBm to 30 dBm.

## 4.10. Conclusions

The simulated drain voltage and current waveforms suggest that the designed circuit is indeed a Class-$F^{-1}$ PA which fulfils the necessary and sufficient conditions for a maximum achievable *PE*. Further confirmation is obtained by the simulated efficiencies of a maximum *PE* of 88.7 % at 2.229 GHz and a maximum *PAE* of 85 % at 2.178 GHz. A maximum output power of 40.8 dBm was also simulated at 2.069 GHz.

Moreover, this designed PA delivers a *PE* above 80 %, a *PAE* above 75 % from 2.1 GHz to 2.3 GHz and an output power above 36.5 dBm from 2 GHz to 2.4 GHz.

It was also found that, this PA delivers a *PE* above 86 %, a *PAE* above 60 % and an output power above 31 dBm when the DC supply voltage is swept from 10 V to 28 V. This means that the available supply voltage in a CubeSat will not affect the optimal operation of this PA.

The highest values of *PE* and *PAE* were obtained at a higher input power level, that is, beyond the $IP_{1dB}$ as stated in Chapter 3.

The reason for the excellent performance of this PA lies in the topology of the proposed wave-shaping network which was designed based on the load-line technique.

The linear stability analysis based on the small signal approach using ADS suggested that this PA is unstable from 0 GHz to 2.26 GHz, while the non-linear stability analysis based on the identification of poles and zeros of the transfer function using the STAN tool, suggested that the designed PA is only unstable at 50 MHz. It showed that this PA is stable from 500 MHz to 6 GHz, when driven at an input power level varying from 0 dBm to 30 dBm.

It was found that the non-linear stability analysis of the PA using the STAN tool provided direct ability to analyse the location of poles and zeros and therefore the nature of possible instabilities. The fact that there was a possible instability at 50 MHz is not a serious problem since 50 MHz is way out of the band for which the PA was designed to operate. It will be necessary to confirm the stability of the final constructed PA.

# Chapter 5

# The Constructed Class-$F^{-1}$ PA

## 5.1. Introduction

This Chapter presents the construction of a Class-$F^{-1}$ PA, the design of which was presented in Chapter 4. The required measurement set-up is explained and the measured performance parameters are presented. Then a comparison is made between the specified, simulated and measured performance parameters, as well as for some existing commercial PAs. The constructed PA is shown in Figure 64.

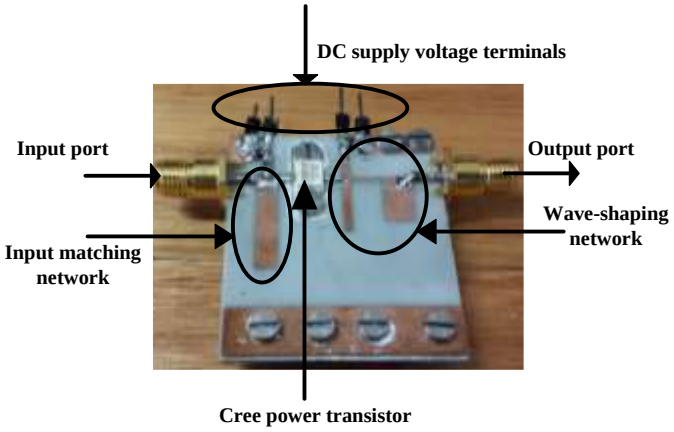



**Figure 64: The constructed PA.**

## 5.2. Measurement Set-Up

The equipment set-up for the measurement of the output power of the PA is shown in Figure 65.

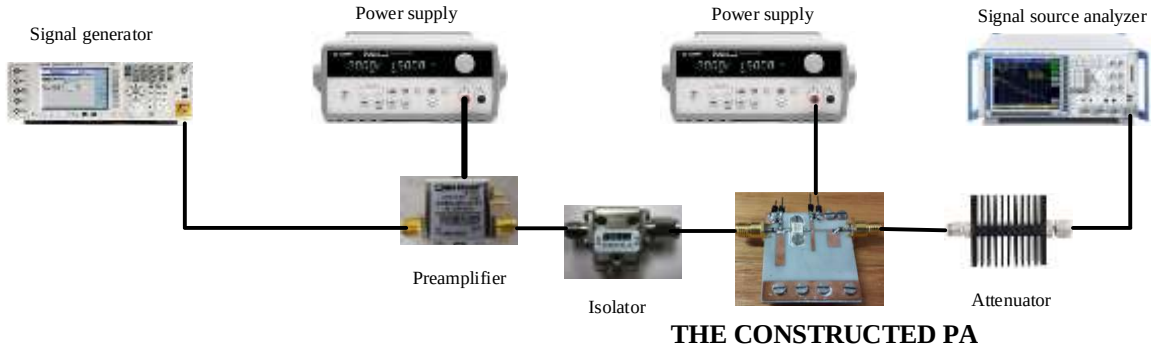



**Figure 65: Equipment set-up.**

An Agilent N9310 RF signal generator, was used to generate the input signal, that is, the power available from the source. The maximum power that the N9310 RF signal generator can deliver is 20 dBm which was not high enough to drive the PA. Therefore a suitable preamplifier was used to increase the level of the drive signal to the PA.

The output power and the power gain of the preamplifier were measured and the results are shown in Figure 66. The preamplifier stage delivers a maximum output power of 35 dBm and an average power gain of 18 dB at 2.2 GHz.

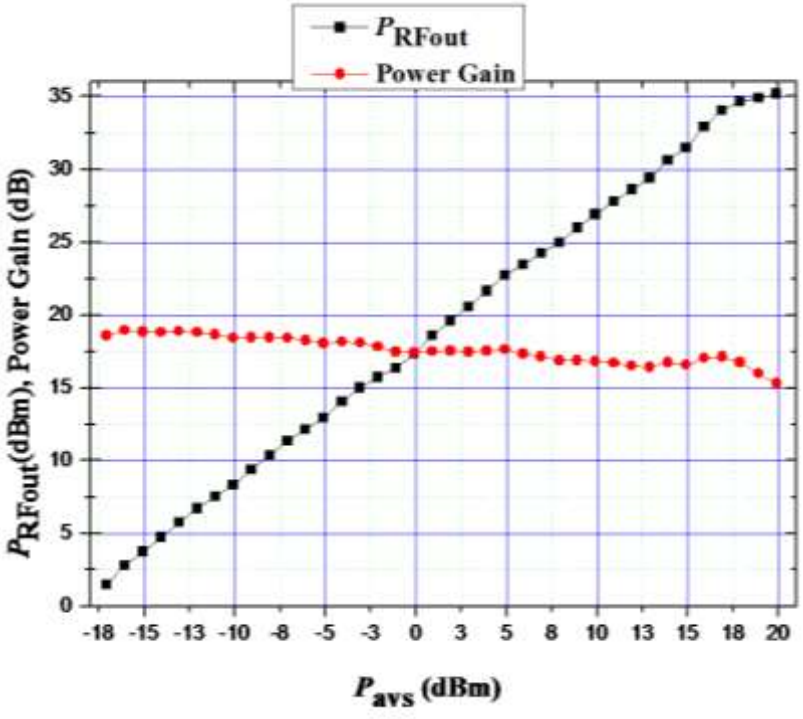



**Figure 66: Measured output power and power gain of the preamplifier**

A Quest SM2023T isolator was used to isolate the output port of the preamplifier from the input port of the PA. The insertion loss, input and output return loss of the isolator were measured at 2.2 GHz with an Agilent vector network analyser (VNA) and the results are shown in Figure 67.

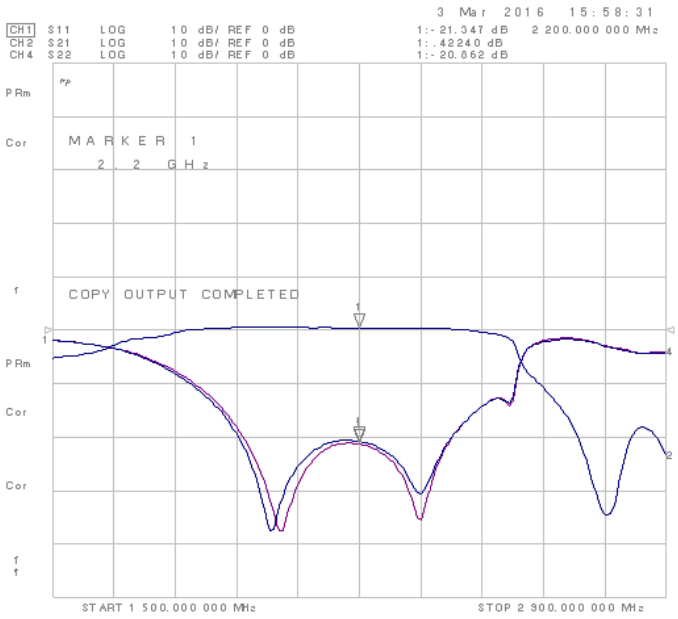



**Figure 67: Measured insertion loss, input and output return loss of isolator**

Figure 67 shows that the isolator has an insertion loss of 0.42 dB at 2.2 GHz, an input return loss of 21.34 dB and an output return loss of 20.66 dB at 2.2 GHz as specified by the manufacturer datasheet.

A Rohde & Schwarz FSUP signal source analyser was used to measure the output power of the PA. A DC to 18 GHz power attenuator was used to decrease the level of the output signal of the PA thus preventing damage to the R&S signal source analyser. The attenuation of the attenuator was measured using the Agilent VNA and the results are shown in Figure 68

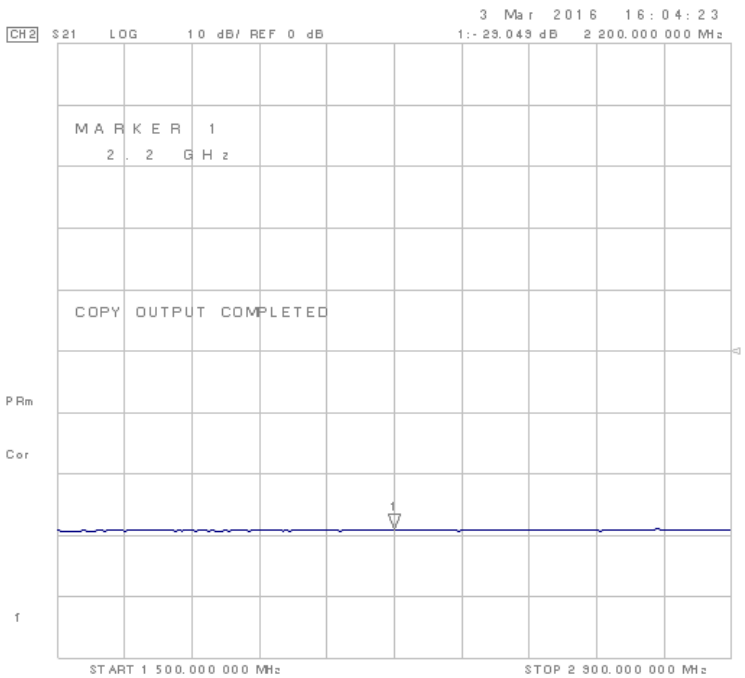



**Figure 68: Measured attenuation**

Figure 68 shows that the attenuator has an attenuation of 29.04 dB at 2.2 GHz, which is 1 dB less than the value specified in the manufacturer datasheet.

The constructed PA was appropriately biased with $V_{DS}$ = 28 V and $V_{GS}$ = −2.7 V. The input signal power was swept from −17 dBm to 17 dBm with steps of 0.1 dBm at 2.2 GHz. For each increment in input power, the DC input power was calculated using Equation 64 and the RF output power was measured on the R&S signal source analyser.

$$P_{DC} = (I_D \times V_{DS}) + (I_G \times V_{GS}) \qquad \text{W} \tag{64}$$

Finally, the *PE* of the PA was calculated using Equation 1and the *PAE* using Equation 2.

## 5.3. Measured Performance Parameters of the PA

The measured *PE* and *PAE* of the PA versus the input power to the PA are shown in Figure 69.

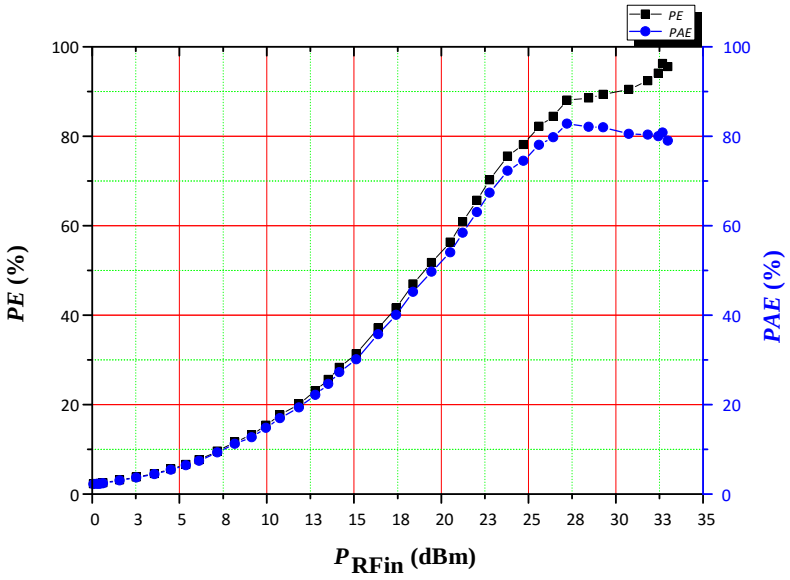



**Figure 69: Measured *PE* and *PAE***

A *PE* of 95 % was measured at an input power level of 33 dBm and a maximum *PAE* of 82 % was measured at an input power level of 28 dBm. In other words, 95 % of the DC power supplied is converted into useful RF power and only 5 % of this DC power is dissipated as heat.

The measured RF output power and the DC power supplied versus the input power to the PA are shown in Figure 70.

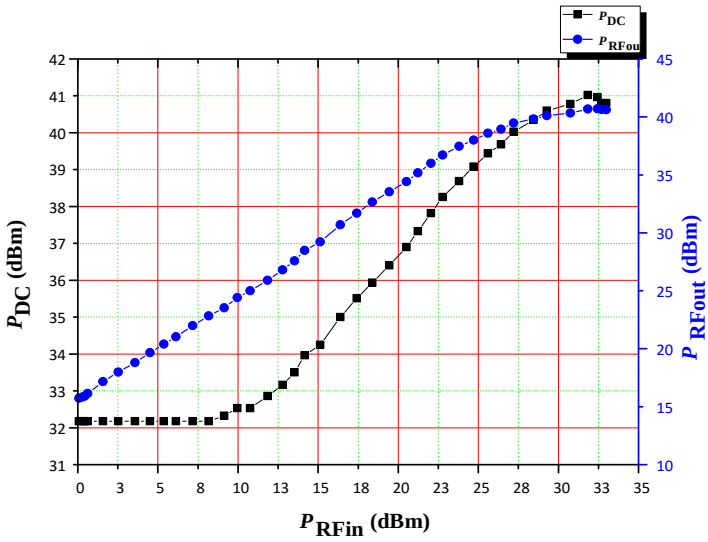



**Figure 70: Measured RF output power and DC input power**

An output power of 40.6 dBm was measured at an input power level of 33 dBm. A maximum DC power of 41 dBm was supplied to the PA at an input power level of 32 dBm.

The power gain and the RF output power versus RF input power are shown in Figure 71

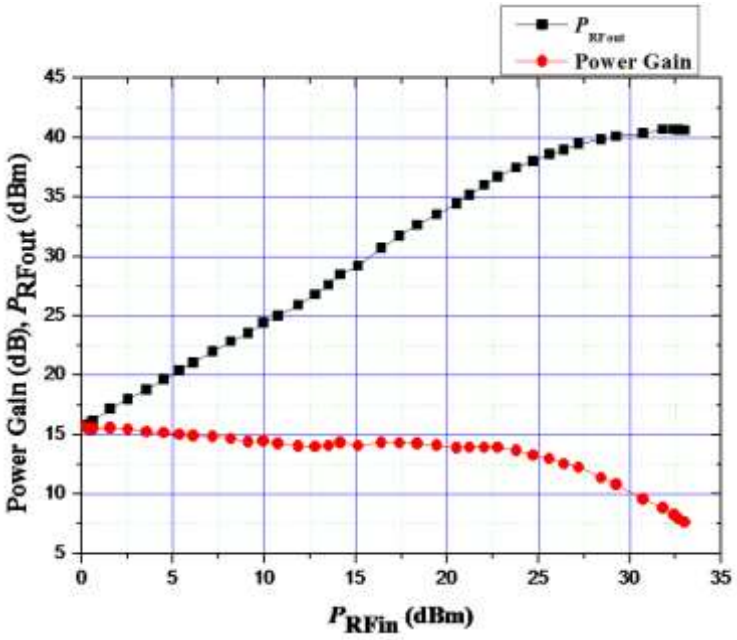



**Figure 71: Measured output power and power gain**

The PA delivers an output power of approximately 37 dBm when still operating in its linear region and an average power gain of close to 15 dB. The PA also delivers a maximum output power of 40.6 dBm at an input power level of 33 dBm.

The performance of the PA was measured when the frequency of the applied signal was varied from 2 GHz to 2.4 GHz. These measurements were performed with the PA being driven by at input power level of 28 dBm. The results are shown in Figures 72 and 73.

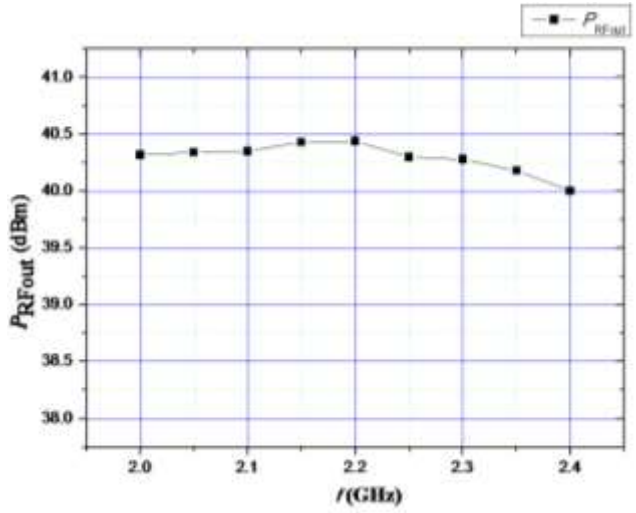



**Figure 72: Measured output power versus the frequency of the applied signal under $P_{RFin}$ = 28 dBm.**

Figure 72 shows that the output power of the PA varies from a minimum of 38 dBm at 2.4 GHz to a maximum of 40.8 dBm at 2.05 GHz.

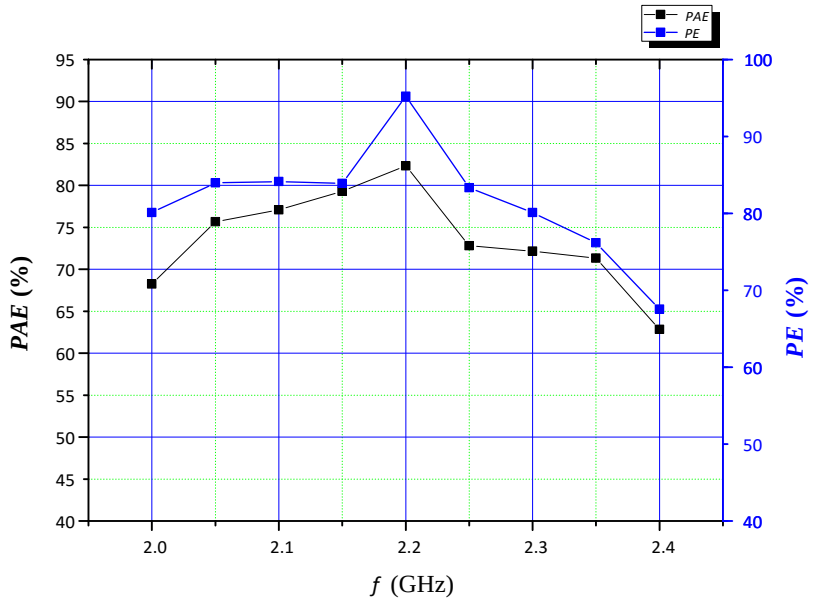



**Figure 73: Measured *PE* and *PAE* versus the frequency of the applied signal under $P_{RFin}$ = 28 dBm**

Figure 73 shows that the *PE* of the PA varies between a minimum value of 68 % at 2.4 GHz and a maximum value of 92 % at 2.2 GHz. The *PAE* of the PA varies between a minimum value of 63 % at 2.4 GHz and a maximum value of 82 % at 2.2 GHz. The PA achieves a *PE* above 80 % and a *PAE* above 70 % from 2.1 GHz to 2.3 GHz which covers the portion of *S*-band used for a satellite up and downlink communication system.

The performance of the PA was measured when the DC supply voltage was varied from 10 V to 28 V and results are shown in Figures 74 and 75. These measurements were performed with the PA being driven at an input power level of 33 dBm.

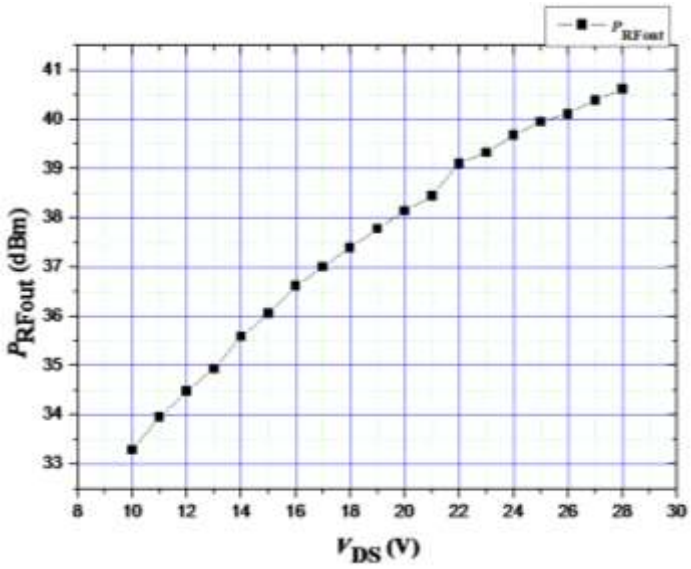



**Figure 74: Measured output power versus the supply voltage**

Figure 74 shows that the constructed PA delivers a minimum output power just above 33 dBm at a DC supply voltage of 10 V and a maximum output power of 40.6 dBm at a DC supply voltage of 28 V

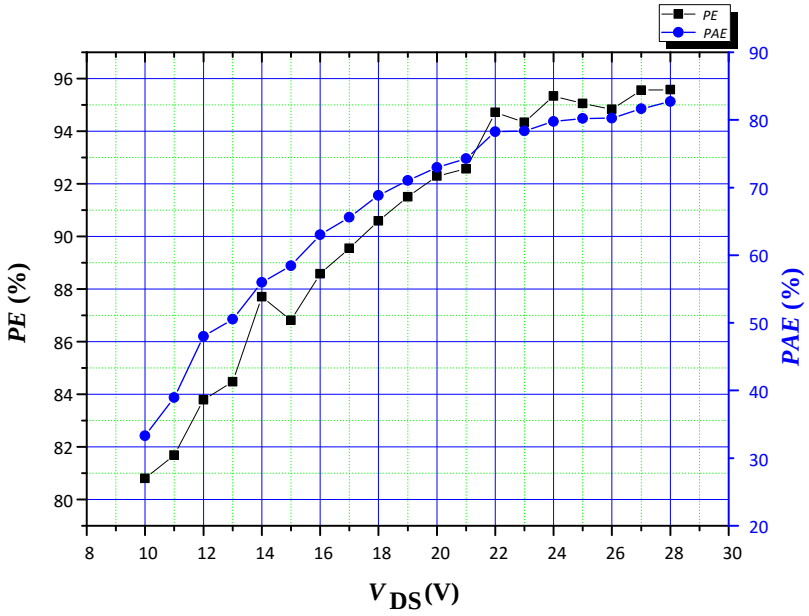



**Figure 75: Measured *PE* and *PAE* versus the DC supply voltage**

Figure 75 shows that the PA delivers a *PE* of just below 81 % with a supply voltage at 10 V. and just above 95 % at 28 V. The *PAE* varies from below 50 % to approximately 82 % when the supply voltage is varied from 10 V to 28 V. This is due to the fact that decreasing the DC supply voltage to the PA causes a significant decrease in the output power level. Since the input power to PA does not change this severely degrades the *PAE*.

## 5.4. Comparisons

The comparison between the specified, simulated and measured performance parameters is presented in Table 4.

**Table 4: Comparison between specified, simulated and measured results**

| Performance parameters | Specified | Simulated | Measured |
|---|---|---|---|
| *PE* (%) | ≥ 75 | 88.5 | 95 |
| *PAE* (%) | ≥ 72 | 85 | 82 |
| Output power (dBm) | ≥ 40 | 40 | 40.6 |
| Power gain (dB) | ≥ 13 | 20 | 14 |

The PA designed and built in this thesis exceeds the specifications and the measured output power and *PAE* correlate well with the simulated output power and *PAE*.

The comparison between the designed and built PA in this thesis and some existing commercial PAs is presented in Table 5.

**Table 5: Comparison between the designed and built PA and existing PAs.**

| Class | Frequency (GHz) | *PE* (%) | *PAE* (%) | Output power (dBm) | Transistor technology | Reference |
|---|---|---|---|---|---|---|
| $F^{-1}$ | 0.915 | - | 83.4 | 40.4 | GaN HEMT | (Andrew & Christopher, 2012: 5-6) |
| $F^{-1}$ | 2.14 | 76 | 72.2 | 41 | GaN HEMT | (Grebennikov, 2011:58-76) |
| $F^{-1}$ | 2.14 | 70.2 | 69.1 | 46 | LDMOSFET | (Grebennikov, 2011:446-456) |
| F | 2 | - | 80.1 | 40.7 | GaN HEMT | (Hwang, *et al*., 2013:1-3) |
| EF | 2.22 | 91 | 80 | 39.5 | GaN HEMT | (Mury, *et al*., 2015: 659-671) |
| A | 2.4 | 25 | - | 33 | GaAs MESFET | ZACUBE-1 |
| $F^{-1}$ | 2.2 | 95 | 82 | 40.6 | GaN HEMT | Safari Mugisho Moïse, 2016 |

## 5.5. Conclusions

A Class-$F^{-1}$ PA was designed, constructed and tested. The performance parameters were measured, the results of which clearly show that the PA delivers a high *PE* (95 %) and high *PAE* (82 %) at an operating frequency of 2.2 GHz. The measured performance parameters also show that the PA delivers a high output power of 40.6 dBm (11.48 W) to the load at an operating frequency of 2.2 GHz.

When compared to one of the highest performing commercially available Class-$F^{-1}$ PA, that is, the PA designed by (Grebennikov, 2011:58-76), the attainment of a *PE* of 95 % is significantly higher than the 76 % achieved by (Grebennikov, 2011:58-76) using exactly the same active device. Similarly, the *PAE* attained by this PA is 82 % which is 10 % higher than the *PAE* achieved by (Grebennikov, 2011:58-76).

The achieved output power of 11.48W is just below the maximum specified saturated power of 13 W specified by the active device manufacturers.

When one considers the PA that is presently being used on ZACUBE-1 which is a Class-A PA with a *PE* of 25 %, this PA will make a significant improvement in overall system efficiency and significantly reduce DC power wastage on-board the satellite. Specifically, the use of this PA on-board future nanosatellites will significantly enhance the *S*-band up and downlink communication system.

The constructed PA did not exhibit any instability at all as was predicted by the non-linear stability analysis. Thus, the non-linear stability analysis using the STAN tool offered an accurate prediction of the stability of a Class-$F^{-1}$ PA which is operating as a non-linear device.

The stability prediction offered by the linear stability analysis using the Rollett stability factor ($K$), the Linville stability factor ($\mu$) and the determinant of the scattering parameters ($\Delta$) was not accurate and is not considered appropriate in the design of a Class-$F^{-1}$ PA.

Finally, the physical size of this PA is significantly smaller (33 mm × 38 mm) relative to others!

# Chapter 6

# Conclusions, Recommendations and Future Work

## 6.1. Final Conclusions

A high efficiency *S*-band Class-$F^{-1}$ PA was designed, built and tested. The proposed topology of the wave-shaping network has enabled the PA to deliver a *PE* of 95 %, a *PAE* of 82 % and an output power of 40.6 dBm at an operating frequency of 2.2 GHz. All of the design specifications that were set out based on the Class-$F^{-1}$ PA designed by (Grebennikov, 2011:58-76) were significantly improved upon.

The performance of this PA over the portion of *S*-band of frequencies used for satellite up and downlink communication make the PA designed and built in this thesis an excellent option for future nanosatellites as well as the ground station transmitter.

## 6.2. Recommendations

The PA designed and built in this thesis requires a large input signal so that it is continuously driven into saturation to achieve the highest *PE* performance. Hence, it is recommended to use a preamplifier with an output power of 33 dBm to drive this PA.

Continuously driving an active device into saturation requires optimum cooling of the active device to maintain its reasonable life span. Thus, to ensure optimum operation of this Class $F^{-1}$ PA an efficient heat dissipation mechanism must be implemented.

## 6.3. Future Work

The restricted space and the designated weight of the CubeSat imposes the use of small circuit components thus the need to reduce the size of any PA used on-board a nanosatellite. Different techniques have been developed for minimising the size of such a PA. Monolithic microwave integrated circuit design techniques are one of the methods that could be used to miniaturise any PA.

In order to integrate this high efficiency PA into the transmitter on-board a satellite, additional electromagnetic interference tests are required to determine how the PA and its location will interact with others circuits within the system.

This PA uses a 50 Ω load impedance for testing purposes. However, the impedance presented by the transmitting antenna on the CubeSat is not necessarily 50 Ω, thus the need to match the output impedance of this PA to that of the transmitting antenna.

Finally, this very high efficiency PA was designed to operate on a transmitter using a linear modulation scheme such as the QPSK modulation scheme. The linearity of the PA was not a major design goal. However, an investigation into methods or design techniques to linearize this PA would be necessary if a non-linear modulation scheme such as QAM is going to be considered.

# Appendix A

Low pass π-type matching network: derivation of Equations 50, 51, 52 and 53

Figure 76 shows a low pass π-type matching network.

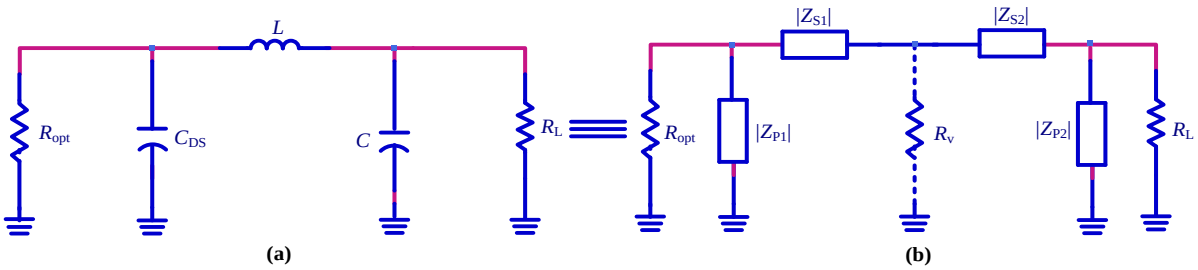



**Figure 76: Low pass π-type matching network**

The low pass π-type matching network, can be designed by splitting the circuit shown in Figure 76(a) into two back-to-back *L* networks with the aid of a virtual resistance $R_V$ as shown in Figure 76(b).

For $R_{opt} > R_L$, the effective quality factor of the network ($Q_{eff}$) is determined by the source section and given by Equation 65.

$$Q_{eff} = Q_S = \sqrt{\frac{R_{opt}}{R_V} - 1} \tag{65}$$

Referring to Figure 76(b), $|Z_{P1}|$ can be calculated from Equation 66, given that the value of $C_{DS}$ in Figure 76(a) is provided by the manufacturer of the active device.

$$|Z_{P1}| = \frac{1}{\omega_0 C_{DS}} \quad \Omega \tag{66}$$

The source quality factor $Q_S$ can now be calculated using Equation 67

$$Q_S = \frac{R_{opt}}{|Z_{P1}|} = \quad R_{opt}\omega_0 C_{DS} \tag{67}$$

which is equal to Equation 52 on page 38.

Referring to Figure 76(b), the virtual resistor $R_V$ can now be determined by equating Equation 65 to Equation 67, resulting in Equation 68.

$$R_V = \frac{R_{opt}}{Q_S^2 + 1} \quad \Omega \tag{68}$$

Referring to Figure 75(b), $|Z_{S1}|$ can now be calculated as per Equation 69:

$$|Z_{S1}| = Q_S R_V = \frac{Q_S\, R_{opt}}{Q_S^2 + 1} \quad \Omega \tag{69}$$

Referring to Figure 76(b), for the load section, the load quality factor $Q_L$ is given by Equation 70

$$Q_L = \sqrt{\frac{R_L}{R_V} - 1} = \sqrt{\frac{R_L}{R_{opt}}\left(1+Q_S^2\right) - 1} \tag{70}$$

which is equal to Equation 53 on page 38

Referring to Figure 76(b), $|Z_{P2}|$ can now be calculated using Equation 71

$$|Z_{P2}| = \frac{1}{\omega_0 C} = \frac{R_L}{Q_L} \qquad \Omega \tag{71}$$

Referring to Figure 76(a), the shunt capacitor can be derived from Equation 71 and is given in Equation 72.

$$C = \frac{Q_L}{R_L \omega_0} \qquad F \tag{72}$$

which is equal to Equation 50 on page 37

Referring to Figure 76(b), $|Z_{S2}|$ can now be calculated as per Equation 73:

$$|Z_{S2}| = Q_L R_V = \frac{Q_L\, R_{opt}}{Q_S^2 + 1} \qquad \Omega \tag{73}$$

Referring to Figure 76(b), the sum of $|Z_{S1}|$ and $|Z_{S2}|$, that is, the sum of Equation 69 and 73 result in

$$|Z_S| = \omega_0 L = |Z_{S1}| + |Z_{S2}| = \frac{R_{opt}(Q_L + Q_S)}{Q_S^2 + 1} \qquad \Omega \tag{74}$$

Referring to Figure 76(a), the series inductor can be derived from Equation 74 as:

$$L = \frac{R_{opt}(Q_L + Q_S)}{\omega_0 (Q_S^2 + 1)} \qquad H \tag{75}$$

which is equal to Equation 51on page 37

# Appendix B

Input impedance of a terminated transmission line

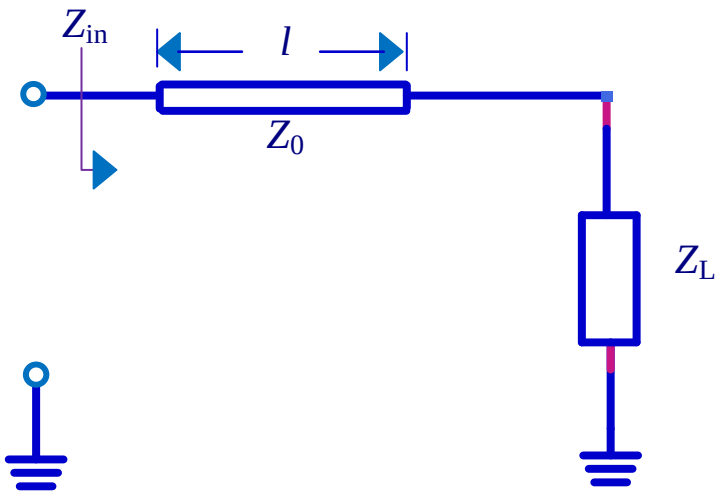



**Figure 77: Terminated transmission line**

Figure 77 shows a transmission line with a characteristic impedance $Z_0$ and a length of $l$ meters. This transmission line is terminated with a load impedance $Z_L$.

The input impedance $Z_{in}$ of this transmission line as a function of its length $l$, is given by Equation 76

$$Z_{in}(l) = \left[\frac{Z_L + jZ_0 \tan \beta l}{Z_0 + jZ_L \tan \beta l}\right] Z_0 \qquad \Omega \tag{76}$$

Equation 76 indicates that the impedance presented by a transmission line is a function of the electrical length $\beta l$ and the load impedance $Z_L$ terminating the transmission line. Some special cases of this Equation are presented below

If the length of the line is a half of a wavelength, that is, $l = \frac{\lambda_g}{2}$ m, then Equation 76 becomes

$$Z_{in}\left(l = \frac{\lambda_g}{2}\right) = \left[\frac{Z_L + jZ_0 \tan \pi}{Z_0 + jZ_L \tan \pi}\right] Z_0 = Z_L \qquad \Omega \tag{77}$$

Equation 77 indicates that the input impedance of a half of a wavelength transmission line is the load impedance in which the transmission line is terminated. Hence, if a half wavelength transmission line is terminated with a short circuit or an open circuit, the input impedance of such a line will be a short circuit or an open circuit.

If the length of the line is a quarter of a wavelength, that is, $l = \frac{\lambda_g}{4}$ m, then Equation 76 becomes

$$Z_{in}\left(l = \frac{\lambda_g}{4}\right) = \left[\frac{jZ_0}{jZ_L}\right] Z_0 = \frac{Z_0^2}{Z_L} \qquad \Omega \tag{78}$$

Equation 78 indicates that if a quarter-wavelength transmission line is terminated with a short circuit, the input impedance of such a line will be an open circuit.

Equation 78 also indicates, that if a quarter-wavelength transmission line is terminated with an open circuit, the input impedance of such a line will be a short circuit.

If the length of the line is an eighth of a wavelength, that is, $l = \frac{\lambda_g}{8}$ m, then Equation 76 becomes

$$Z_{\text{in}}\left(l = \frac{\lambda_g}{8}\right) = \left[\frac{Z_{\text{L}} + jZ_0 \tan\left(\frac{\pi}{4}\right)}{Z_0 + jZ_{\text{L}} \tan\left(\frac{\pi}{4}\right)}\right] Z_0 = \left[\frac{Z_{\text{L}} + jZ_0}{Z_0 + jZ_{\text{L}}}\right] Z_0 \quad \Omega \tag{79}$$

Equation 79 indicates that if an eighth of a wavelength transmission line is terminated with a short circuit, the input impedance of such a line will be purely inductive ($jZ_0\ \Omega$).

Equation 79 also indicates, that if an eighth of a wavelength transmission line is terminated with an open circuit, the input impedance of such a line will be purely capacitive ($-jZ_0\ \Omega$).

# Appendix C

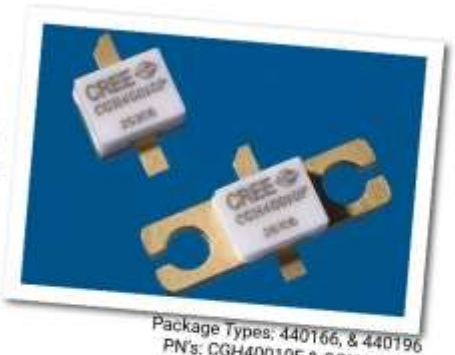
**Datasheet of the Cree CGH40010F GaN Power Device**

CREE

## CGH40010

**10 W, RF Power GaN HEMT**

Cree's CGH40010 is an unmatched, gallium nitride (GaN) high electron mobility transistor (HEMT). The CGH40010, operating from a 28 volt rail, offers a general purpose, broadband solution to a variety of RF and microwave applications. GaN HEMTs offer high efficiency, high gain and wide bandwidth capabilities making the CGH40010 ideal for linear and compressed amplifier circuits. The transistor is available in both screw-down, flange and solder-down, pill packages.



Package Types: 440166, & 440196
PN's: CGH40010F & CGH40010P

### FEATURES

- Up to 6 GHz Operation
- 16 dB Small Signal Gain at 2.0 GHz
- 14 dB Small Signal Gain at 4.0 GHz
- 13 W typical $P_{SAT}$
- 65 % Efficiency at $P_{SAT}$
- 28 V Operation

### APPLICATIONS

- 2-Way Private Radio
- Broadband Amplifiers
- Cellular Infrastructure
- Test Instrumentation
- Class A, AB, Linear amplifiers suitable for OFDM, W-CDMA, EDGE, CDMA waveforms

RoHS COMPLIANT

Rev 4.0 – May 2015

Large Signal Models Available for ADS and MWO

Subject to change without notice.
www.cree.com/wireless

1

## Absolute Maximum Ratings (not simultaneous) at 25˚C Case Temperature

| Parameter | Symbol | Rating | Units | Conditions |
|---|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | 84 | Volts | 25˚C |
| Gate-to-Source Voltage | $V_{GS}$ | -10, +2 | Volts | 25˚C |
| Storage Temperature | $T_{STG}$ | -65, +150 | ˚C | |
| Operating Junction Temperature | $T_J$ | 225 | ˚C | |
| Maximum Forward Gate Current | $I_{GMAX}$ | 4.0 | mA | 25˚C |
| Maximum Drain Current[1] | $I_{DMAX}$ | 1.5 | A | 25˚C |
| Soldering Temperature[2] | $T_S$ | 245 | ˚C | |
| Screw Torque | $\tau$ | 60 | in-oz | |
| Thermal Resistance, Junction to Case[3] | $R_{\theta JC}$ | 8.0 | ˚C/W | 85˚C |
| Case Operating Temperature[3,4] | $T_C$ | -40, +150 | ˚C | |

Note:
[1] Current limit for long term, reliable operation
[2] Refer to the Application Note on soldering at www.cree.com/RF/Document-Library
[3] Measured for the CGH40010F at $P_{DISS}$ = 14 W.
[4] See also, the Power Dissipation De-rating Curve on Page 6.

## Electrical Characteristics ($T_C$ = 25˚C)

| Characteristics | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **DC Characteristics[1]** | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | -3.8 | -3.0 | -2.3 | $V_{DC}$ | $V_{DS}$ = 10 V, $I_D$ = 3.6 mA |
| Gate Quiescent Voltage | $V_{GS(Q)}$ | – | -2.7 | – | $V_{DC}$ | $V_{DD}$ = 28 V, $I_D$ = 200 mA |
| Saturated Drain Current | $I_{DS}$ | 2.9 | 3.5 | – | A | $V_{DS}$ = 6.0 V, $V_{GS}$ = 2.0 V |
| Drain-Source Breakdown Voltage | $V_{BR}$ | 120 | – | – | $V_{DC}$ | $V_{GS}$ = -8 V, $I_D$ = 3.6 mA |
| **RF Characteristics[2] ($T_J$ = 25˚C, $F_0$ = 3.7 GHz unless otherwise noted)** | | | | | | |
| Small Signal Gain | $G_{SS}$ | 12.5 | 14.5 | – | dB | $V_{DD}$ = 28 V, $I_{DQ}$ = 200 mA |
| Power Output[3] | $P_{SAT}$ | 10 | 12.5 | – | W | $V_{DD}$ = 28 V, $I_{DQ}$ = 200 mA |
| Drain Efficiency[4] | $\eta$ | 55 | 65 | – | % | $V_{DD}$ = 28 V, $I_{DQ}$ = 200 mA, $P_{SAT}$ |
| Output Mismatch Stress | VSWR | – | – | 10 : 1 | Ψ | No damage at all phase angles, $V_{DD}$ = 28 V, $I_{DQ}$ = 200 mA, $P_{SAT}$ = 10 W CW |
| **Dynamic Characteristics** | | | | | | |
| Input Capacitance | $C_{GS}$ | – | 4.5 | – | pF | $V_{DS}$ = 28 V, $V_{gs}$ = -8 V, f = 1 MHz |
| Output Capacitance | $C_{DS}$ | – | 1.3 | – | pF | $V_{DS}$ = 28 V, $V_{gs}$ = -8 V, f = 1 MHz |
| Feedback Capacitance | $C_{GD}$ | – | 0.2 | – | pF | $V_{DS}$ = 28 V, $V_{gs}$ = -8 V, f = 1 MHz |

Notes:
[1] Measured on wafer prior to packaging.
[2] Measured in CGH40010-AMP.
[3] $P_{SAT}$ is defined as $I_G$ = 0.36 mA.
[4] Drain Efficiency = $P_{OUT}$ / $P_{DC}$

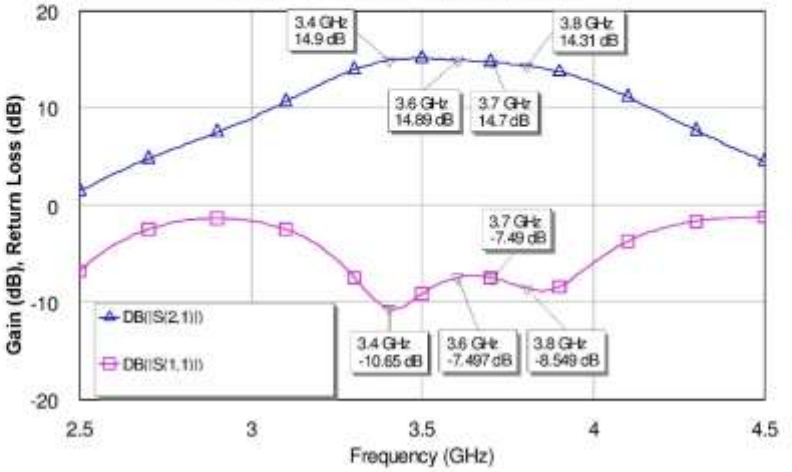




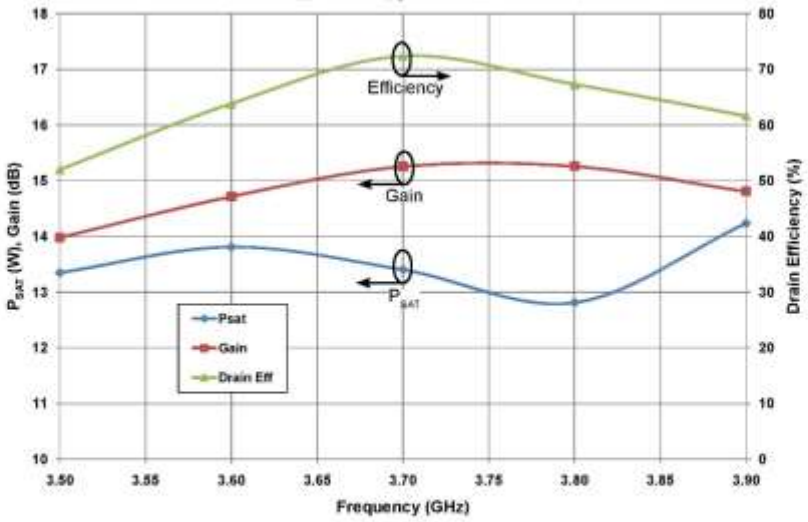
Cree, Inc.
4600 Silicon Drive
Durham, North Carolina, USA 27703
USA Tel: +1.919.313.5300
Fax: +1.919.869.2733
www.cree.com/rf

## Typical Performance

**Small Signal Gain and Return Loss vs Frequency of the CGH40010 in the CGH40010-AMP**




**$P_{SAT}$ Gain, and Drain Efficiency vs Frequency of the CGH40010F in the CGH40010-AMP**
**$V_{DD}$ = 28 V, $I_{DQ}$ = 200 mA**





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4600 Silicon Drive
Durham, North Carolina, USA 27703
USA Tel: +1.919.313.5300
Fax: +1.919.869.2733
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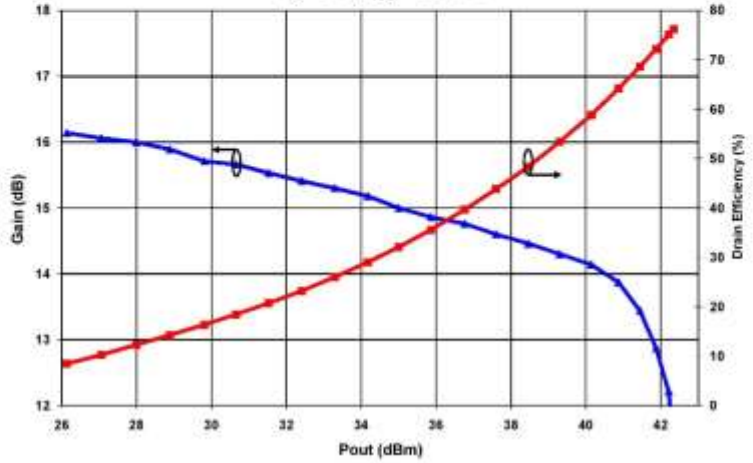
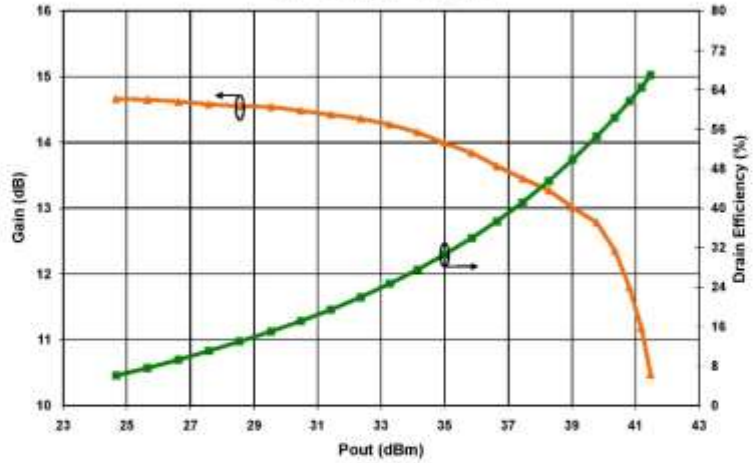
Swept CW Data of CGH40010F vs. Output Power with Source and Load Impedances Optimized for Drain Efficiency at 2.0 GHz
$V_{DD}$ = 28 V, $I_{DQ}$ = 200 mA




Swept CW Data of CGH40010F vs. Output Power with Source and Load Impedances Optimized for Drain Efficiency at 3.6 GHz
$V_{DD}$ = 28 V, $I_{DQ}$ = 200 mA





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4600 Silicon Drive
Durham, North Carolina, USA 27703
USA Tel: +1.919.313.5300
Fax: +1.919.869.2733
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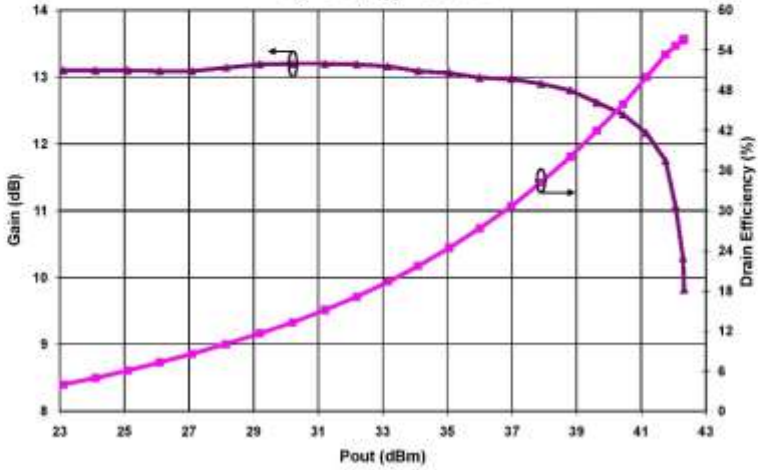
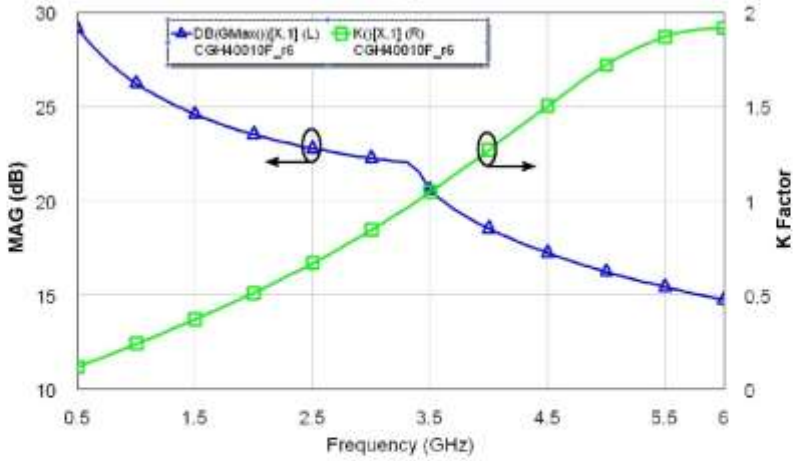
Swept CW Data of CGH40010F vs. Output Power with Source and Load Impedances Optimized for P1 Power at 3.6 GHz
$V_{DD}$ = 28 V, $I_{DQ}$ = 200 mA




Simulated Maximum Available Gain and K Factor of the CGH40010F
$V_{DD}$ = 28 V, $I_{DQ}$ = 200 mA



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4600 Silicon Drive
Durham, North Carolina, USA 27703
USA Tel: +1.919.313.5300
Fax: +1.919.869.2733
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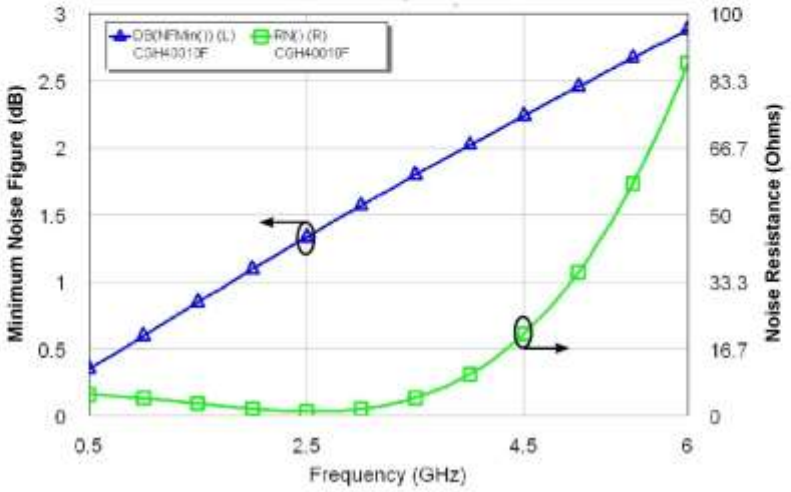
## Typical Noise Performance

**Simulated Minimum Noise Figure and Noise Resistance vs Frequency of the CGH40010F**
**$V_{DD}$ = 28 V, $I_{DQ}$ = 100 mA**




## Electrostatic Discharge (ESD) Classifications

| Parameter | Symbol | Class | Test Methodology |
|---|---|---|---|
| Human Body Model | HBM | 1A > 250 V | JEDEC JESD22 A114-D |
| Charge Device Model | CDM | 1 < 200 V | JEDEC JESD22 C101-C |





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4600 Silicon Drive
Durham, North Carolina, USA 27703
USA Tel: +1.919.313.5300
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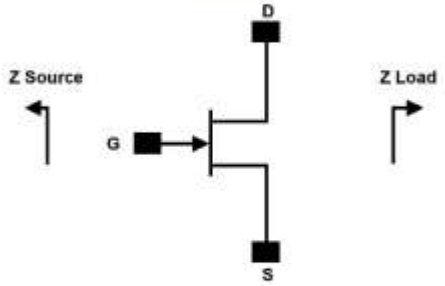
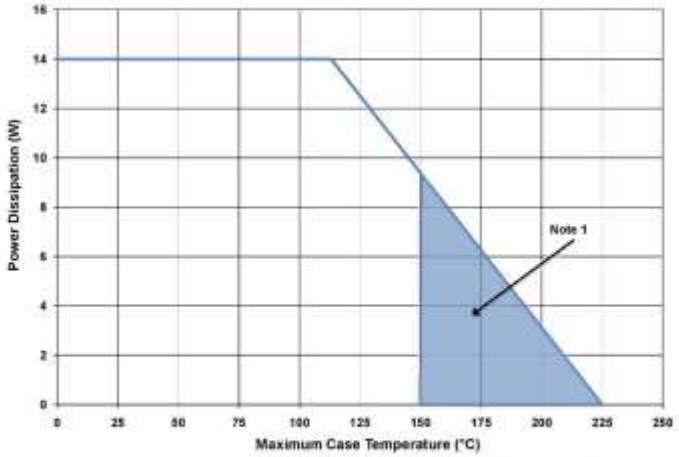
## Source and Load Impedances




| Frequency (MHz) | Z Source | Z Load |
|---|---|---|
| 500 | 20.2 + j16.18 | 51.7 + j15.2 |
| 1000 | 8.38 + j9.46 | 41.4 + j28.5 |
| 1500 | 7.37 + j0 | 28.15 + j29 |
| 2500 | 3.19 - j4.76 | 19 + j9.2 |
| 3500 | 3.18 - j13.3 | 14.6 + j7.46 |

Note 1. $V_{DD}$ = 28V, $I_{DQ}$ = 200mA in the 440166 package.
Note 2. Optimized for power, gain, $P_{SAT}$ and PAE.
Note 3. When using this device at low frequency, series resistors should be used to maintain amplifier stability.

## CGH40010 Power Dissipation De-rating Curve




Note 1. Area exceeds Maximum Case Operating Temperature (See Page 2).





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4600 Silicon Drive
Durham, North Carolina, USA 27703
USA Tel: +1.919.313.5300
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## CGH40010-AMP Demonstration Amplifier Circuit Bill of Materials

| Designator | Description | Qty |
|---|---|---|
| R1,R2 | RES,1/16W,0603,1%,0 OHMS | 1 |
| R3 | RES,1/16W,0603,1%,47 OHMS | 1 |
| R4 | RES,1/16W,0603,1%,100 OHMS | 1 |
| C6 | CAP, 470PF, 5%,100V, 0603 | 1 |
| C17 | CAP, 33 UF, 20%, G CASE | 1 |
| C16 | CAP, 1.0UF, 100V, 10%, X7R, 1210 | 1 |
| C8 | CAP 10UF 16V TANTALUM | 1 |
| C14 | CAP, 100.0pF, +/-5%, 0603 | 1 |
| C1 | CAP, 0.5pF, +/-0.05pF, 0603 | 1 |
| C2 | CAP, 0.7pF, +/-0.1pF, 0603 | 1 |
| C10,C11 | CAP, 1.0pF, +/-0.1pF, 0603 | 2 |
| C4,C12 | CAP, 10.0pF,+/-5%, 0603 | 2 |
| C5,C13 | CAP, 39pF, +/-5%, 0603 | 2 |
| C7,C15 | CAP,33000PF, 0805,100V, X7R | 2 |
| J3,J4 | CONN SMA STR PANEL JACK RECP | 1 |
| J2 | HEADER RT>PLZ .1CEN LK 2 POS | 1 |
| J1 | HEADER RT>PLZ .1CEN LK 5POS | 1 |
| - | PCB, RO4350B, Er = 3.48, h = 20 mil | 1 |
| Q1 | CGH40010F or CGH40010P | 1 |

## CGH40010-AMP Demonstration Amplifier Circuit





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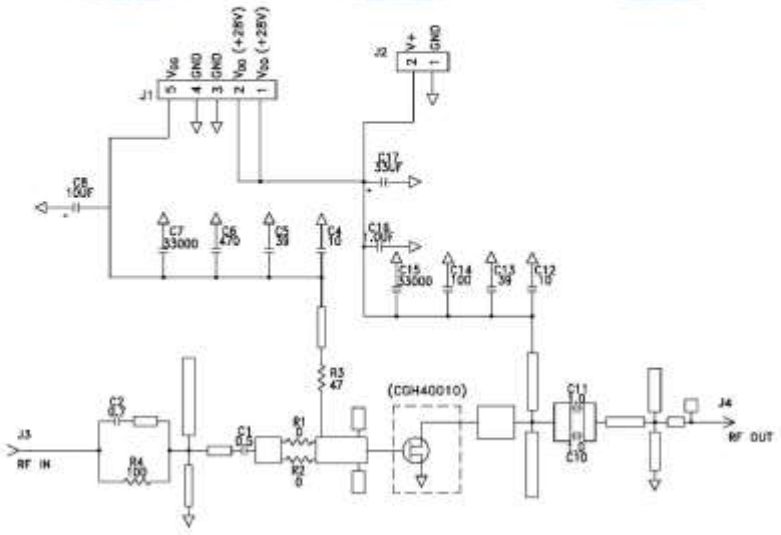
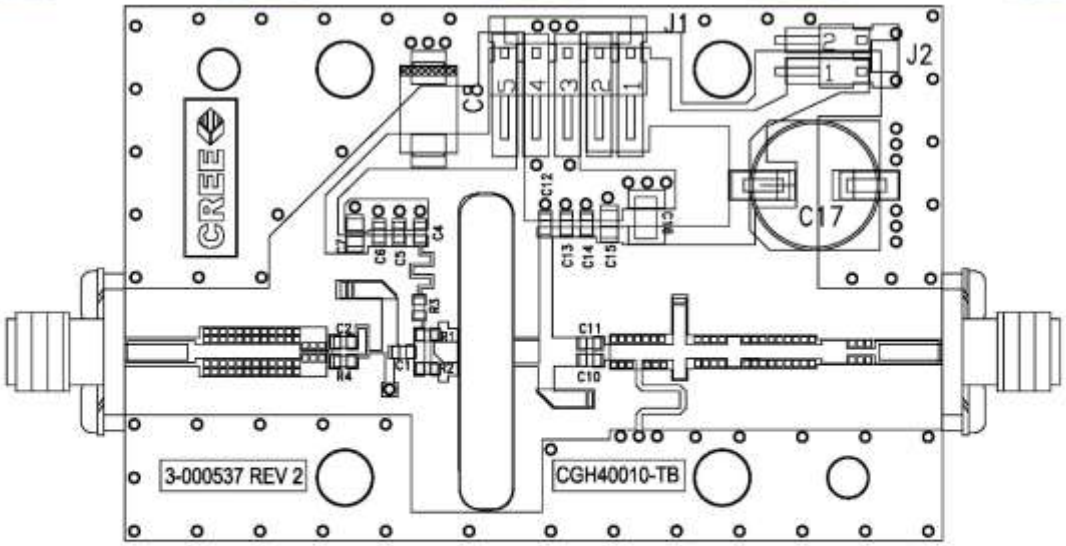
4600 Silicon Drive
Durham, North Carolina, USA 27703
USA Tel: +1.919.313.5300
Fax: +1.919.869.2733
www.cree.com/rf

## CGH40010-AMP Demonstration Amplifier Circuit Schematic




## CGH40010-AMP Demonstration Amplifier Circuit Outline








Cree, Inc.
4600 Silicon Drive
Durham, North Carolina, USA 27703
USA Tel: +1.919.313.5300
Fax: +1.919.869.2733
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## Typical Package S-Parameters for CGH40010
## (Small Signal, $V_{DS}$ = 28 V, $I_{DQ}$ = 100 mA, angle in degrees)

| Frequency | Mag S11 | Ang S11 | Mag S21 | Ang S21 | Mag S12 | Ang S12 | Mag S22 | Ang S22 |
|---|---|---|---|---|---|---|---|---|
| 500 MHz | 0.909 | -123.34 | 17.19 | 108.22 | 0.027 | 21.36 | 0.343 | -90.81 |
| 600 MHz | 0.902 | -133.06 | 14.86 | 101.82 | 0.028 | 15.60 | 0.329 | -98.65 |
| 700 MHz | 0.897 | -140.73 | 13.04 | 96.45 | 0.028 | 10.87 | 0.321 | -104.84 |
| 800 MHz | 0.894 | -146.96 | 11.58 | 91.78 | 0.029 | 6.84 | 0.317 | -109.84 |
| 900 MHz | 0.891 | -152.16 | 10.41 | 87.61 | 0.029 | 3.33 | 0.316 | -113.95 |
| 1.0 GHz | 0.890 | -156.60 | 9.43 | 83.82 | 0.029 | 0.19 | 0.318 | -117.42 |
| 1.1 GHz | 0.889 | -160.47 | 8.62 | 80.31 | 0.029 | -2.66 | 0.321 | -120.40 |
| 1.2 GHz | 0.888 | -163.90 | 7.93 | 77.02 | 0.029 | -5.28 | 0.326 | -123.02 |
| 1.3 GHz | 0.887 | -166.99 | 7.34 | 73.90 | 0.029 | -7.72 | 0.332 | -125.36 |
| 1.4 GHz | 0.887 | -169.80 | 6.82 | 70.92 | 0.029 | -10.01 | 0.338 | -127.51 |
| 1.5 GHz | 0.887 | -172.39 | 6.38 | 68.05 | 0.029 | -12.18 | 0.345 | -129.50 |
| 1.6 GHz | 0.887 | -174.80 | 5.98 | 65.28 | 0.028 | -14.24 | 0.353 | -131.37 |
| 1.7 GHz | 0.887 | -177.07 | 5.63 | 62.59 | 0.028 | -16.21 | 0.360 | -133.15 |
| 1.8 GHz | 0.887 | -179.22 | 5.32 | 59.97 | 0.028 | -18.09 | 0.369 | -134.87 |
| 1.9 GHz | 0.887 | 178.73 | 5.04 | 57.41 | 0.028 | -19.91 | 0.377 | -136.54 |
| 2.0 GHz | 0.888 | 176.76 | 4.78 | 54.89 | 0.027 | -21.66 | 0.385 | -138.17 |
| 2.1 GHz | 0.888 | 174.86 | 4.55 | 52.42 | 0.027 | -23.35 | 0.393 | -139.77 |
| 2.2 GHz | 0.888 | 173.02 | 4.34 | 49.99 | 0.027 | -24.98 | 0.402 | -141.34 |
| 2.3 GHz | 0.888 | 171.23 | 4.15 | 47.60 | 0.026 | -26.56 | 0.410 | -142.90 |
| 2.4 GHz | 0.889 | 169.48 | 3.97 | 45.24 | 0.026 | -28.08 | 0.418 | -144.45 |
| 2.5 GHz | 0.889 | 167.76 | 3.81 | 42.90 | 0.026 | -29.55 | 0.426 | -145.99 |
| 2.6 GHz | 0.890 | 166.07 | 3.66 | 40.59 | 0.025 | -30.98 | 0.434 | -147.53 |
| 2.7 GHz | 0.890 | 164.39 | 3.53 | 38.30 | 0.025 | -32.36 | 0.442 | -149.06 |
| 2.8 GHz | 0.890 | 162.74 | 3.40 | 36.03 | 0.025 | -33.69 | 0.450 | -150.59 |
| 2.9 GHz | 0.891 | 161.10 | 3.28 | 33.78 | 0.024 | -34.97 | 0.458 | -152.12 |
| 3.0 GHz | 0.891 | 159.46 | 3.17 | 31.55 | 0.024 | -36.20 | 0.465 | -153.65 |
| 3.2 GHz | 0.892 | 156.21 | 2.97 | 27.12 | 0.023 | -38.51 | 0.479 | -156.72 |
| 3.4 GHz | 0.893 | 152.96 | 2.79 | 22.73 | 0.022 | -40.63 | 0.493 | -159.80 |
| 3.6 GHz | 0.893 | 149.69 | 2.64 | 18.38 | 0.022 | -42.52 | 0.505 | -162.90 |
| 3.8 GHz | 0.894 | 146.38 | 2.50 | 14.05 | 0.021 | -44.17 | 0.517 | -166.03 |
| 4.0 GHz | 0.894 | 143.03 | 2.38 | 9.72 | 0.020 | -45.56 | 0.527 | -169.19 |
| 4.2 GHz | 0.894 | 139.61 | 2.28 | 5.40 | 0.019 | -46.67 | 0.537 | -172.39 |
| 4.4 GHz | 0.895 | 136.11 | 2.18 | 1.07 | 0.019 | -47.46 | 0.546 | -175.64 |
| 4.6 GHz | 0.895 | 132.53 | 2.09 | -3.29 | 0.018 | -47.90 | 0.554 | -178.95 |
| 4.8 GHz | 0.895 | 128.85 | 2.01 | -7.68 | 0.017 | -47.96 | 0.561 | 177.69 |
| 5.0 GHz | 0.895 | 125.06 | 1.94 | -12.10 | 0.017 | -47.61 | 0.568 | 174.25 |
| 5.2 GHz | 0.895 | 121.15 | 1.88 | -16.58 | 0.016 | -46.84 | 0.573 | 170.72 |
| 5.4 GHz | 0.895 | 117.11 | 1.82 | -21.12 | 0.016 | -45.67 | 0.578 | 167.10 |
| 5.6 GHz | 0.895 | 112.94 | 1.77 | -25.73 | 0.015 | -44.12 | 0.582 | 163.38 |
| 5.8 GHz | 0.895 | 108.62 | 1.72 | -30.42 | 0.015 | -42.30 | 0.586 | 159.54 |
| 6.0 GHz | 0.895 | 104.15 | 1.68 | -35.20 | 0.015 | -40.33 | 0.589 | 155.56 |

To download the s-parameters in s2p format, go to the CGH40010 Product page and click on the documentation tab.





Cree, Inc.
4600 Silicon Drive
Durham, North Carolina, USA 27703
USA Tel: +1.919.313.5300
Fax: +1.919.869.2733
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## Typical Package S-Parameters for CGH40010
## (Small Signal, $V_{DS}$ = 28 V, $I_{DQ}$ = 200 mA, angle in degrees)

| Frequency | Mag S11 | Ang S11 | Mag S21 | Ang S21 | Mag S12 | Ang S12 | Mag S22 | Ang S22 |
|---|---|---|---|---|---|---|---|---|
| 500 MHz | 0.911 | -130.62 | 18.41 | 105.41 | 0.022 | 19.44 | 0.303 | -112.24 |
| 600 MHz | 0.906 | -139.65 | 15.80 | 99.47 | 0.023 | 14.31 | 0.299 | -119.83 |
| 700 MHz | 0.902 | -146.70 | 13.80 | 94.50 | 0.023 | 10.17 | 0.298 | -125.50 |
| 800 MHz | 0.899 | -152.41 | 12.22 | 90.19 | 0.023 | 6.68 | 0.299 | -129.85 |
| 900 MHz | 0.898 | -157.17 | 10.96 | 86.34 | 0.024 | 3.67 | 0.302 | -133.28 |
| 1.0 GHz | 0.896 | -161.24 | 9.92 | 82.82 | 0.024 | 0.99 | 0.305 | -136.05 |
| 1.1 GHz | 0.896 | -164.79 | 9.06 | 79.56 | 0.024 | -1.41 | 0.309 | -138.34 |
| 1.2 GHz | 0.895 | -167.95 | 8.33 | 76.49 | 0.024 | -3.62 | 0.314 | -140.30 |
| 1.3 GHz | 0.895 | -170.80 | 7.70 | 73.57 | 0.023 | -5.66 | 0.320 | -142.01 |
| 1.4 GHz | 0.894 | -173.41 | 7.17 | 70.78 | 0.023 | -7.56 | 0.326 | -143.54 |
| 1.5 GHz | 0.894 | -175.82 | 6.70 | 68.08 | 0.023 | -9.35 | 0.332 | -144.94 |
| 1.6 GHz | 0.894 | -178.09 | 6.28 | 65.47 | 0.023 | -11.05 | 0.338 | -146.24 |
| 1.7 GHz | 0.894 | 179.78 | 5.92 | 62.92 | 0.023 | -12.66 | 0.345 | -147.48 |
| 1.8 GHz | 0.894 | 177.75 | 5.59 | 60.43 | 0.023 | -14.19 | 0.352 | -148.68 |
| 1.9 GHz | 0.894 | 175.81 | 5.30 | 57.99 | 0.023 | -15.65 | 0.358 | -149.84 |
| 2.0 GHz | 0.894 | 173.94 | 5.04 | 55.59 | 0.022 | -17.05 | 0.365 | -150.99 |
| 2.1 GHz | 0.894 | 172.13 | 4.80 | 53.23 | 0.022 | -18.39 | 0.372 | -152.12 |
| 2.2 GHz | 0.894 | 170.37 | 4.58 | 50.91 | 0.022 | -19.67 | 0.379 | -153.26 |
| 2.3 GHz | 0.895 | 168.65 | 4.38 | 48.61 | 0.022 | -20.90 | 0.386 | -154.39 |
| 2.4 GHz | 0.895 | 166.96 | 4.20 | 46.33 | 0.021 | -22.08 | 0.393 | -155.54 |
| 2.5 GHz | 0.895 | 165.30 | 4.03 | 44.08 | 0.021 | -23.20 | 0.400 | -156.69 |
| 2.6 GHz | 0.895 | 163.66 | 3.88 | 41.84 | 0.021 | -24.27 | 0.407 | -157.85 |
| 2.7 GHz | 0.895 | 162.04 | 3.74 | 39.63 | 0.021 | -25.28 | 0.414 | -159.03 |
| 2.8 GHz | 0.895 | 160.43 | 3.60 | 37.43 | 0.020 | -26.25 | 0.420 | -160.22 |
| 2.9 GHz | 0.896 | 158.83 | 3.48 | 35.24 | 0.020 | -27.16 | 0.427 | -161.42 |
| 3.0 GHz | 0.896 | 157.24 | 3.37 | 33.06 | 0.020 | -28.02 | 0.433 | -162.64 |
| 3.2 GHz | 0.896 | 154.06 | 3.16 | 28.74 | 0.019 | -29.57 | 0.446 | -165.13 |
| 3.4 GHz | 0.896 | 150.87 | 2.98 | 24.44 | 0.019 | -30.88 | 0.457 | -167.69 |
| 3.6 GHz | 0.896 | 147.66 | 2.82 | 20.16 | 0.018 | -31.95 | 0.468 | -170.31 |
| 3.8 GHz | 0.897 | 144.41 | 2.68 | 15.89 | 0.018 | -32.76 | 0.478 | -173.00 |
| 4.0 GHz | 0.897 | 141.10 | 2.56 | 11.61 | 0.017 | -33.30 | 0.488 | -175.77 |
| 4.2 GHz | 0.897 | 137.72 | 2.45 | 7.33 | 0.017 | -33.55 | 0.497 | -178.61 |
| 4.4 GHz | 0.897 | 134.26 | 2.35 | 3.03 | 0.017 | -33.50 | 0.505 | 178.47 |
| 4.6 GHz | 0.897 | 130.71 | 2.26 | -1.31 | 0.016 | -33.18 | 0.512 | 175.46 |
| 4.8 GHz | 0.896 | 127.06 | 2.17 | -5.68 | 0.016 | -32.58 | 0.518 | 172.36 |
| 5.0 GHz | 0.896 | 123.30 | 2.10 | -10.09 | 0.016 | -31.74 | 0.524 | 169.16 |
| 5.2 GHz | 0.896 | 119.42 | 2.04 | -14.57 | 0.016 | -30.72 | 0.529 | 165.86 |
| 5.4 GHz | 0.896 | 115.41 | 1.98 | -19.10 | 0.016 | -29.60 | 0.534 | 162.44 |
| 5.6 GHz | 0.896 | 111.26 | 1.92 | -23.71 | 0.016 | -28.46 | 0.537 | 158.89 |
| 5.8 GHz | 0.895 | 106.97 | 1.87 | -28.40 | 0.017 | -27.41 | 0.540 | 155.20 |
| 6.0 GHz | 0.895 | 102.53 | 1.82 | -33.19 | 0.017 | -26.54 | 0.543 | 151.36 |

To download the s-parameters in s2p format, go to the CGH40010 Product Page and click on the documentation tab.





Cree, Inc.
4600 Silicon Drive
Durham, North Carolina, USA 27703
USA Tel: +1.919.313.5300
Fax: +1.919.869.2733
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## Typical Package S-Parameters for CGH40010
## (Small Signal, $V_{DS}$ = 28 V, $I_{DQ}$ = 500 mA, angle in degrees)

| Frequency | Mag S11 | Ang S11 | Mag S21 | Ang S21 | Mag S12 | Ang S12 | Mag S22 | Ang S22 |
|---|---|---|---|---|---|---|---|---|
| 500 MHz | 0.914 | -135.02 | 18.58 | 103.70 | 0.020 | 18.36 | 0.300 | -126.80 |
| 600 MHz | 0.909 | -143.57 | 15.88 | 98.05 | 0.020 | 13.67 | 0.302 | -133.51 |
| 700 MHz | 0.906 | -150.23 | 13.83 | 93.33 | 0.021 | 9.90 | 0.304 | -138.40 |
| 800 MHz | 0.904 | -155.61 | 12.23 | 89.23 | 0.021 | 6.77 | 0.307 | -142.08 |
| 900 MHz | 0.903 | -160.09 | 10.95 | 85.56 | 0.021 | 4.08 | 0.311 | -144.94 |
| 1.0 GHz | 0.902 | -163.93 | 9.91 | 82.21 | 0.021 | 1.71 | 0.314 | -147.23 |
| 1.1 GHz | 0.901 | -167.29 | 9.04 | 79.09 | 0.021 | -0.41 | 0.319 | -149.10 |
| 1.2 GHz | 0.901 | -170.29 | 8.31 | 76.15 | 0.021 | -2.35 | 0.323 | -150.69 |
| 1.3 GHz | 0.900 | -173.00 | 7.69 | 73.35 | 0.021 | -4.12 | 0.328 | -152.07 |
| 1.4 GHz | 0.900 | -175.50 | 7.15 | 70.66 | 0.021 | -5.78 | 0.333 | -153.29 |
| 1.5 GHz | 0.900 | -177.81 | 6.69 | 68.07 | 0.021 | -7.32 | 0.338 | -154.41 |
| 1.6 GHz | 0.900 | -179.98 | 6.27 | 65.54 | 0.021 | -8.77 | 0.344 | -155.44 |
| 1.7 GHz | 0.900 | 177.96 | 5.91 | 63.08 | 0.020 | -10.15 | 0.349 | -156.43 |
| 1.8 GHz | 0.899 | 176.00 | 5.59 | 60.67 | 0.020 | -11.45 | 0.355 | -157.38 |
| 1.9 GHz | 0.899 | 174.12 | 5.30 | 58.30 | 0.020 | -12.68 | 0.361 | -158.30 |
| 2.0 GHz | 0.899 | 172.31 | 5.04 | 55.97 | 0.020 | -13.85 | 0.366 | -159.22 |
| 2.1 GHz | 0.899 | 170.54 | 4.80 | 53.67 | 0.020 | -14.96 | 0.372 | -160.14 |
| 2.2 GHz | 0.900 | 168.83 | 4.58 | 51.40 | 0.020 | -16.01 | 0.378 | -161.06 |
| 2.3 GHz | 0.900 | 167.15 | 4.39 | 49.16 | 0.019 | -17.01 | 0.384 | -161.99 |
| 2.4 GHz | 0.900 | 165.49 | 4.21 | 46.94 | 0.019 | -17.95 | 0.390 | -162.93 |
| 2.5 GHz | 0.900 | 163.87 | 4.04 | 44.73 | 0.019 | -18.85 | 0.396 | -163.88 |
| 2.6 GHz | 0.900 | 162.26 | 3.89 | 42.54 | 0.019 | -19.69 | 0.402 | -164.86 |
| 2.7 GHz | 0.900 | 160.66 | 3.75 | 40.37 | 0.019 | -20.48 | 0.407 | -165.85 |
| 2.8 GHz | 0.900 | 159.08 | 3.62 | 38.21 | 0.019 | -21.21 | 0.413 | -166.86 |
| 2.9 GHz | 0.900 | 157.51 | 3.50 | 36.05 | 0.018 | -21.89 | 0.418 | -167.89 |
| 3.0 GHz | 0.900 | 155.93 | 3.39 | 33.91 | 0.018 | -22.52 | 0.424 | -168.95 |
| 3.2 GHz | 0.900 | 152.79 | 3.18 | 29.65 | 0.018 | -23.61 | 0.435 | -171.12 |
| 3.4 GHz | 0.900 | 149.64 | 3.00 | 25.40 | 0.017 | -24.48 | 0.445 | -173.38 |
| 3.6 GHz | 0.900 | 146.45 | 2.85 | 21.17 | 0.017 | -25.11 | 0.454 | -175.73 |
| 3.8 GHz | 0.900 | 143.23 | 2.71 | 16.93 | 0.017 | -25.51 | 0.463 | -178.17 |
| 4.0 GHz | 0.900 | 139.94 | 2.58 | 12.69 | 0.017 | -25.67 | 0.471 | 179.30 |
| 4.2 GHz | 0.900 | 136.58 | 2.47 | 8.43 | 0.016 | -25.60 | 0.479 | 176.67 |
| 4.4 GHz | 0.899 | 133.14 | 2.38 | 4.15 | 0.016 | -25.32 | 0.486 | 173.94 |
| 4.6 GHz | 0.899 | 129.61 | 2.29 | -0.17 | 0.016 | -24.85 | 0.492 | 171.12 |
| 4.8 GHz | 0.899 | 125.97 | 2.21 | -4.53 | 0.016 | -24.24 | 0.498 | 168.18 |
| 5.0 GHz | 0.898 | 122.23 | 2.13 | -8.94 | 0.016 | -23.54 | 0.503 | 165.13 |
| 5.2 GHz | 0.898 | 118.36 | 2.07 | -13.41 | 0.016 | -22.80 | 0.507 | 161.96 |
| 5.4 GHz | 0.898 | 114.36 | 2.01 | -17.95 | 0.017 | -22.11 | 0.511 | 158.66 |
| 5.6 GHz | 0.897 | 110.22 | 1.95 | -22.56 | 0.017 | -21.54 | 0.514 | 155.22 |
| 5.8 GHz | 0.897 | 105.94 | 1.90 | -27.26 | 0.018 | -21.16 | 0.517 | 151.63 |
| 6.0 GHz | 0.897 | 101.51 | 1.86 | -32.04 | 0.019 | -21.04 | 0.519 | 147.87 |

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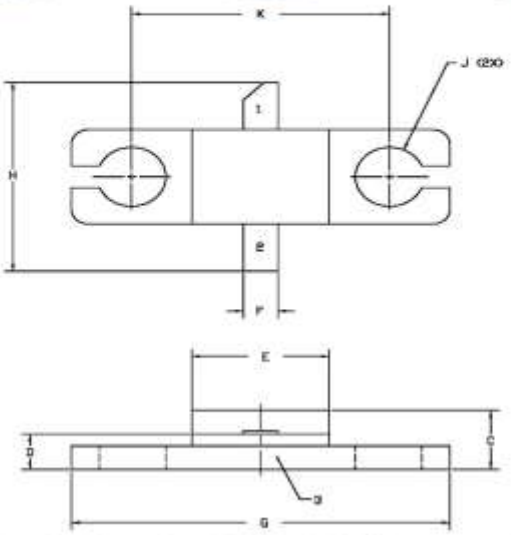
Cree, Inc.
4600 Silicon Drive
Durham, North Carolina, USA 27703
USA Tel: +1.919.313.5300
Fax: +1.919.869.2733
www.cree.com/rf

## Product Dimensions CGH40010F (Package Type — 440166)

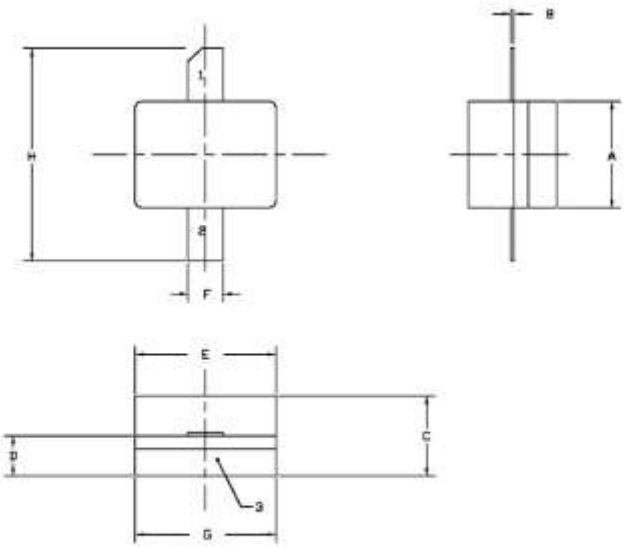



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.005" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF THE PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.
5. ALL PLATED SURFACES ARE NI/AU

| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.155 | 0.165 | 3.94 | 4.19 |
| B | 0.004 | 0.006 | 0.10 | 0.15 |
| C | 0.115 | 0.135 | 2.92 | 3.43 |
| D | 0.057 | 0.067 | 1.45 | 1.70 |
| E | 0.195 | 0.205 | 4.95 | 5.21 |
| F | 0.045 | 0.055 | 1.14 | 1.40 |
| G | 0.545 | 0.555 | 13.84 | 14.09 |
| H | 0.280 | 0.360 | 7.11 | 9.14 |
| J | # .100 | | 2.54 | |
| K | 0.375 | | 9.53 | |

PIN 1. GATE
PIN 2. DRAIN
PIN 3. SOURCE

## Product Dimensions CGH40010P (Package Type — 440196)




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.005" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF THE PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.
5. ALL PLATED SURFACES ARE NI/AU

| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.155 | 0.165 | 3.94 | 4.19 |
| B | 0.003 | 0.006 | 0.10 | 0.15 |
| C | 0.115 | 0.135 | 2.92 | 3.17 |
| D | 0.057 | 0.067 | 1.45 | 1.70 |
| E | 0.195 | 0.205 | 4.95 | 5.21 |
| F | 0.045 | 0.055 | 1.14 | 1.40 |
| G | 0.195 | 0.205 | 4.95 | 5.21 |
| H | 0.280 | 0.360 | 7.11 | 9.14 |

PIN 1. GATE
PIN 2. DRAIN
PIN 3. SOURCE





Cree, Inc.
4600 Silicon Drive
Durham, North Carolina, USA 27703
USA Tel: +1.919.313.5300
Fax: +1.919.869.2733
www.cree.com/rf

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## Product Ordering Information

| Order Number | Description | Unit of Measure | Image |
|---|---|---|---|
| CGH40010F | GaN HEMT | Each |  |
| CGH40010P | GaN HEMT | Each |  |
| CGH40010F-TB | Test board without GaN HEMT | Each |  |
| CGH40010F-AMP | Test board with GaN HEMT installed | Each |  |





Cree, Inc.
4600 Silicon Drive
Durham, North Carolina, USA 27703
USA Tel: +1.919.313.5300
Fax: +1.919.869.2733
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For more information, please contact:

Cree, Inc.
4600 Silicon Drive
Durham, North Carolina, USA 27703
www.cree.com/RF

Sarah Miller
Marketing
Cree, RF Components
1.919.407.5302

Ryan Baker
Marketing & Sales
Cree, RF Components
1.919.407.7816

Tom Dekker
Sales Director
Cree, RF Components
1.919.407.5639





Cree, Inc.
4600 Silicon Drive
Durham, North Carolina, USA 27703
USA Tel: +1.919.313.5300
Fax: +1.919.869.2733
www.cree.com/rf

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