Cape Peninsula
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Mitigating Interference from Switch-Mode Power Supplies in Sampling Receivers

by

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Declaration

I, Muammar Slamdien, declare that the contents of this thesis represent my own unaided work, and that the thesis has not previously been submitted for academic examination towards any qualification. Furthermore, it represents my own opinions and not necessarily those of the Cape Peninsula University of Technology.

13 March 2017

Signed **Date**

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Abstract

This thesis reports on the research and development of techniques applied to mitigate interference from switch-mode power supplies in sampling receivers and also more specifically for FMCW radar receiver applications. During the system testing phase of an FMCW Radar at Reutech Radar Systems (RRS), it was found that a large false target was emerging on the Range-Doppler Map (RDM). It was concluded that the problem was originating from interference caused by the switch-mode power supplies (SMPS), which supply DC power to the radar receiver subsystem. This then created the need for a new DC power supply, which is able to minimize the interference, as well as, mitigate the effects of the interference caused by the switching of the power supply. The mitigation techniques and power supply development was divided four main sections, namely, research, simulation, design and evaluation. The research involved obtaining background information on sampling receivers, sampling theory, Range-Doppler Processing, switch-mode power supplies, their effects and mitigation thereof. In the simulation phase, the research was utilised to simulate the various interference mitigation techniques. A power supply PCB was then designed in the design phase to practically illustrate the techniques being utilised. Lastly, during evaluation, this PCB was evaluated against the criteria set out in the research phase. The results demonstrated that the technique of synchronising the PWM clock to the Sampling frequency and SRF yielded a significant reduction in the SMPS noise on the Range-Doppler Map.

Table of Contents

List of Illustrations and Tables

List of Illustrations

List of Tables

Glossary

Terms/Acronyms/Abbreviations	Definition/Explanation
ADC	**Analog to Digital Converter**
DC	**Direct Current**
EMI	**Electromagnetic Interference**
ESR	**Equivalent Series Resistance**
FFT	**Fast Fourier Transform**
FMCW	**Frequency Modulated Continuous Wave**
HMI	**Human Machine Interface**
IC	**Integrated Circuit**
IF	**Intermediate Frequency**
LAN	**Local Area Network**
MOQ	**Minimum Order Quantity**
MOSFET	**Metal-Oxide-Semiconductor Field-Effect Transistor**
PCB	**Printed Circuit Board**
PLL	**Phase-Lock Loop**
PWM	**Pulse Width Modulation**
QC	**Quality Control**
RADAR	**Radio Detection and Ranging**
RDM	**Range Doppler Map**
RDP	**Range-Doppler Processing**
RF	**Radio Frequency**
RRS	**Reutech Radar Systems**
RTSA	**Real-Time Spectrum Analyser**
SMPS	**Switch-Mode Power Supply**
SRF	**Sweep Repetition Frequency**

Chapter 1
Introduction

During the system testing phase of an FMCW Radar at Reutech Radar Systems (RRS) in 2013, it was found that a large false target was clearly emerging on the Range-Doppler Map (RDM) after the Range-Doppler processing of the radar data. After many weeks of relentless troubleshooting, it was concluded that the problem was originating from interference caused by the switch-mode power supplies (SMPS), which supply DC power to the radar receiver subsystem.

This then created the need to design, manufacture, test and integrate a new DC power supply for the radar receiver subsystem. This new power supply needed to be able to minimize the interference itself, as well as, mitigate the effects of the interference caused by the switching of the power supply. It also needed to be designed specifically for use in a portable radar system.

1.1 Statement of Research Problem

The main challenge is to develop a design methodology or approach which will enable the conformance to all the electrical requirements for the power supply, while at the same time, minimising the loss of the integrity of the final sampled signal.

DC power supplies, which comply with military specifications, and are able to conform 100% to industry's electrical and mechanical requirements are typically not available off-the-shelf. This means that a custom PCB needs to be developed according to this methodology for this application.

This custom PCB must be developed to effectively mitigate the adverse effects induced by the SMPS, without compromising their functionality or reliability. In FMCW radar, for example, this will result in the minimum loss of sensitivity at certain (affected) target ranges/velocities, hence making a much more effective and sensitive radar system.

1.2 Background to the Research Problem

FMCW radar receivers typically down-convert received signals to an intermediate frequency (IF). The IF is often in the same frequency range as the switching regulators, which usually operate between 100 kHz and 10 MHz. The receivers typically incorporate significant gain at these frequencies. The gain may be as high as 50-80 dB (to increase sensitivity), and this gain is increased even further during signal processing. The switching noise can then be interpreted as data. In an FMCW system, for example, a constant frequency in the IF band will be interpreted as a target at a specific range. In Figure 1, a range-Doppler map can be seen without SMPS interference.

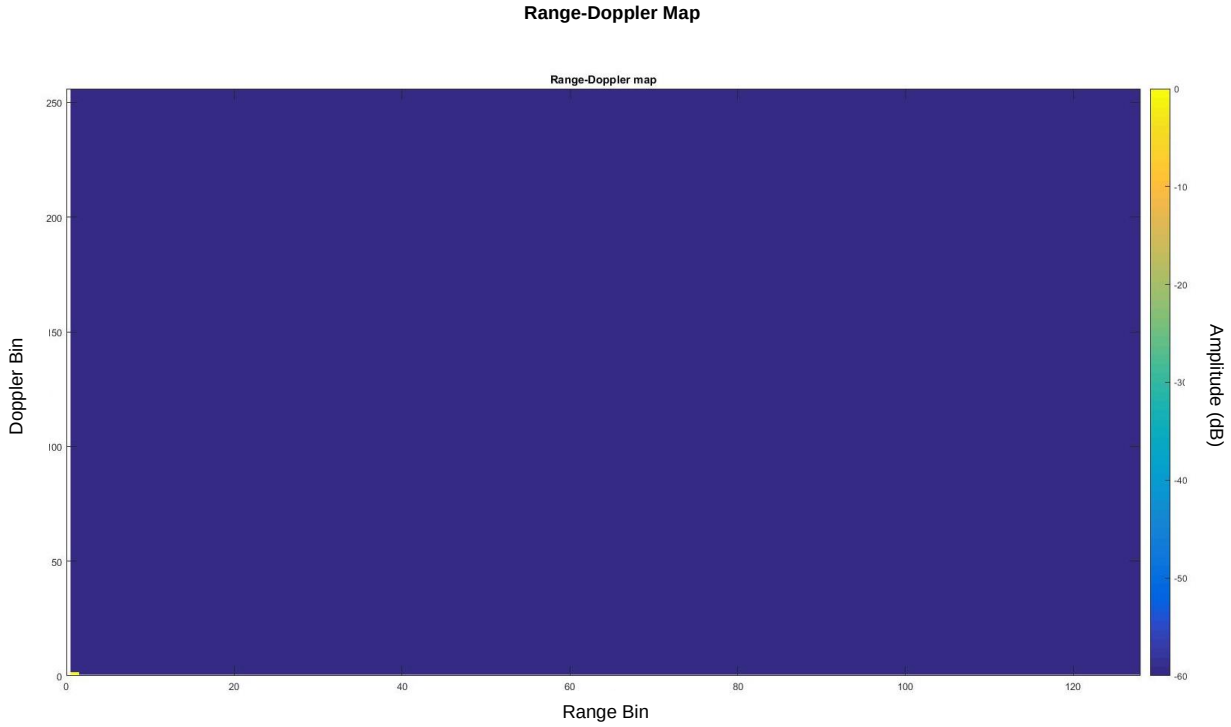

Figure 1: Typical FMCW Radar Range-Doppler map without SMPS Interference

In

Figure 1, the Range-Doppler map is free of clutter (interference), and the all-round sensitivity of the radar system should not be compromised. This means that the radar should operate according to its specifications. In Figure 2, a Range-Doppler map can be seen with SMPS interference.

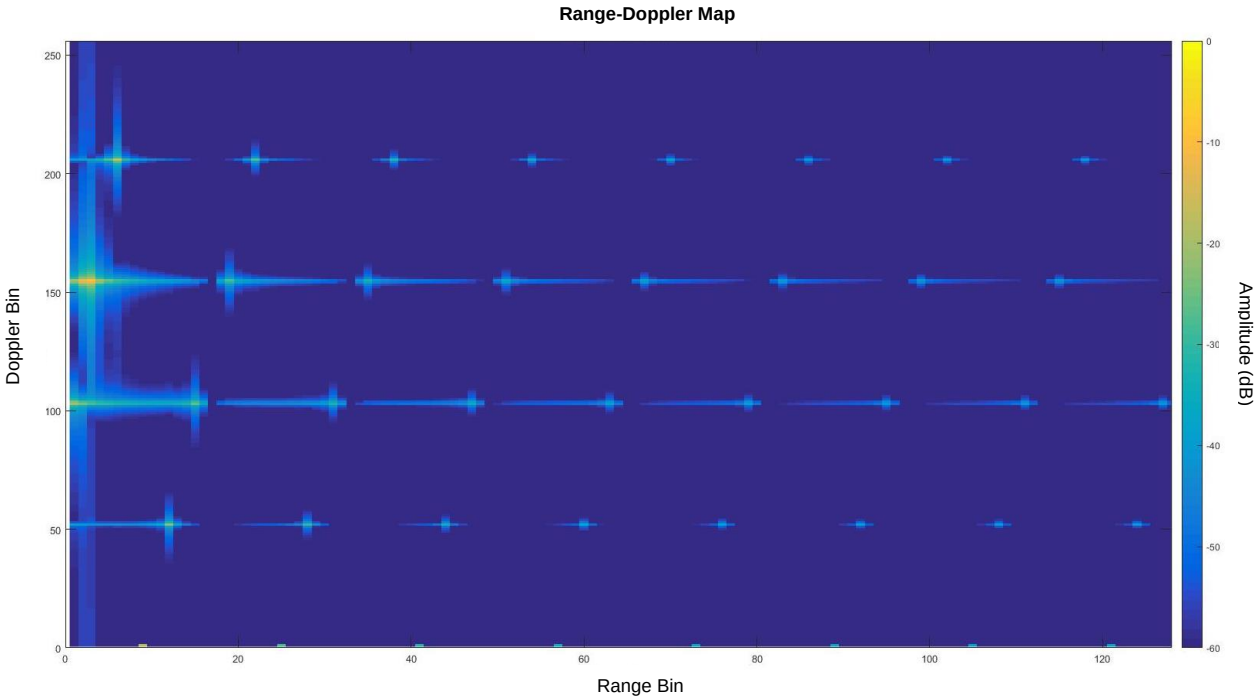

Figure 2: Typical FMCW Radar Range-Doppler map with SMPS Interference

In Figure 2, the simulated SMPS frequency is at 1.6 x SRF (Sweep Repetition Frequency), which equates to about 781Hz, and corresponds roughly to Doppler bin 155, after taking aliasing into account. The SMPS interference and its harmonics appear to be multiple targets at various ranges and velocities; this will dramatically decrease radar sensitivity in the affected areas. This means that the radar may not operate according to its specifications, and could have devastating results for the operator. This issue necessitated the need to mitigate this SMPS interference.

1.3 Aims and Objectives

For the DC switch-mode power supply PCB development, the primary objectives are to effectively integrate it with the receiver subsystem, design for equal to or better efficiency than a typical off-the-shelf SMPS. The PCB also needs to be able to reduce SMPS EMI for sampling receiver applications, minimize Radar Data distortion and eliminate the “false targets” on the RDM caused by SMPS EMI. Lastly, the PCB must meet all military and industry specifications.
The core research questions are as follows:

- Can the unit be effectively integrated with the receiver subsystem?
    - The unit must provide the required voltage and load current for the receiver subsystem.
    - The efficiency of unit must be equal to or better than a typical off-the-shelf SMPS.
- Can a DC power supply PCB be developed which mitigates the effects of the switch-mode power supplies?
    - The PCB must be able to greatly reduce the SMPS EMI, by producing a clean, synchronous output.
    - The PCB must be able to minimize the processed Radar data distortion, due to the SMPS switching frequency and its harmonics, when viewed by Real-Time Spectrum Analysis
    - The PCB must be able to eliminate “false targets” on the RDM caused by the SMPS frequency
- Can the PCB be designed to comply with the military and industry specifications?
    - The PCB must be designed according to Military Specifications.
    - The PCB must be designed according to Industry Specifications.

1.4 Approach to the problem

The research approach would start off by looking at sampling receivers in general, followed by FMCW Radar systems, as a typical example of a system using sampling receivers. The radar receiver subsystem and its power supply will then be looked at, with particular focus on power supply options. The power supply options will look mainly at linear vs. SMPS’s, its operation, topologies, power supply effects and techniques to mitigate these effects. The best mitigation techniques will then be selected and further research will be done into them.

1.5 Delineation of Research

The fields of scholarship which are to be included in the literature review, otherwise referred to as the boundaries (or delimitations) of the literature review are illustrated in Figure 3.

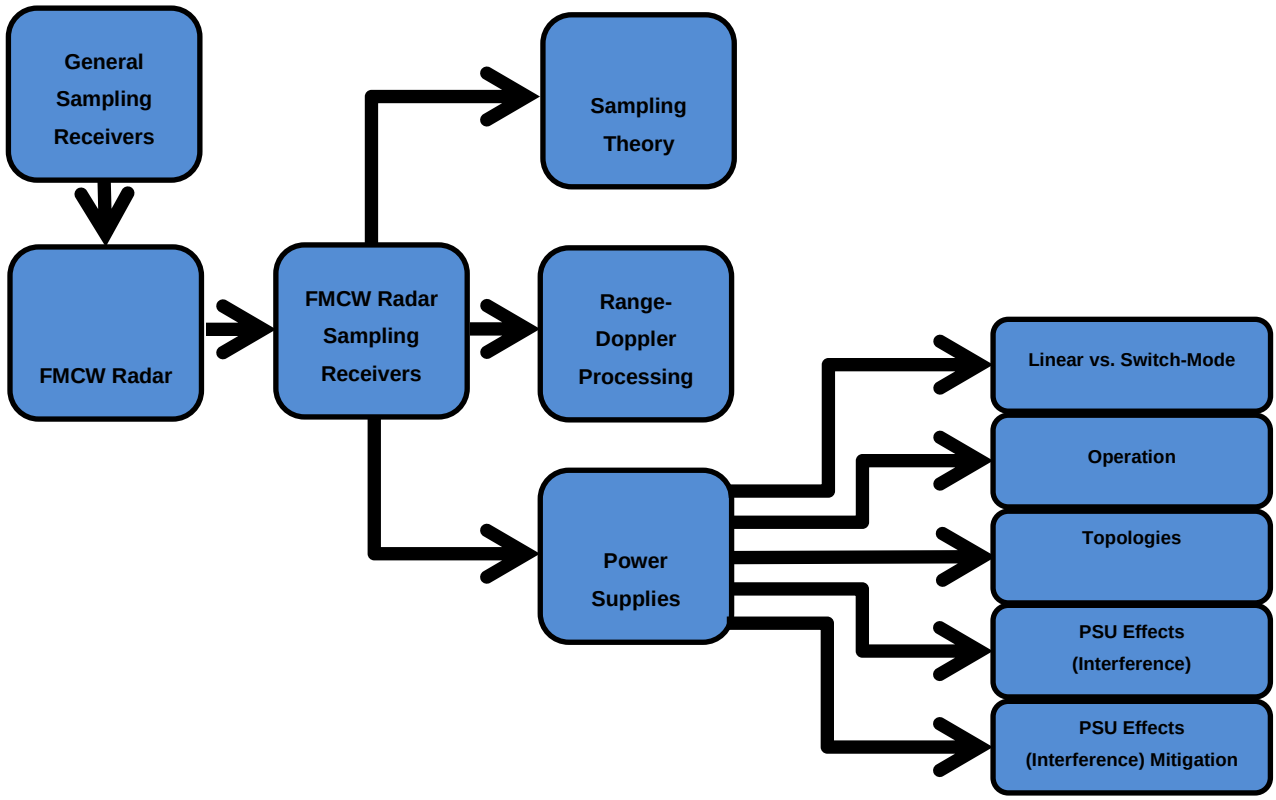

Figure 3: Literature to be reviewed

As illustrated in Figure 3, the literature review would initially look at sampling receivers in general; this will be followed closely by FMCW Radar systems, as a typical example of a system which makes use of sampling receivers. The radar receiver subsystem and its power supply will then be looked at, and the primary focus will be on power supply options. The power supply options will look mainly at linear vs. SMPS's, its operation, topologies, power supply effects and techniques to mitigate these effects. The best mitigation techniques (for this application) will be selected and further research will be done into them. In parallel with the power supply research, additional research will be done into sampling theory and range-Doppler processing, and how they link up with the interference and its mitigation. Lastly, a summary of the main points which have emerged from the literature research will be provided. The EMI (interference) to be reduced will be limited to the Power supply generated conducted EMI and not radiated EMI. The radiated EMI shall be mitigated by the use of proper shielding etc. in the Receiver unit design, which is out of the scope of this study.

1.6 Thesis Structure

The layout of the remaining part of this thesis is as follows:

Chapter 2: FMCW radar sampling receivers will be looked as an example of a sampling receiver application. The power supply design for these receivers will be the primary focus of this chapter. It looks at linear vs. SMPS's, its operation, topologies, power supply effects and techniques to mitigate these effects. Sampling theory and Range-Doppler Processing for sampling receiver applications will also be reviewed in detail. The chapter will be concluded with a summary of the main points which have emerged from the literature research.

Chapter 3: In this chapter, the two interference mitigation approaches, namely, synchronising the SMPS frequency to a multiple of the sampling frequency and to a multiple of the SRF will be evaluated. The evaluation will be done by means of simulation, using Matlab.

Chapter 4: The technical design specifications of the SMPS PCB will be outlined in this chapter. The main aspects of the design specification to be discussed include the receiver subsystem integration, SMPS interference mitigation, and military and industry compliance.

Chapter 5: The PCB design procedure will be documented here. This Chapter will discuss the PCB schematic design, along with detailed component calculations. It will also outline the PCB layout procedure, as well as, the assembly of the PCB and its final inspection.

Chapter 6: In this chapter, the answers to the research questions will be stated (whether or not the goals have been achieved and why). Things such as the purpose of the experiment, experiment setup and procedures will be indicated in this chapter. Finally, a summarised version of the results and observations will also be provided for each section.

Chapter 7: This chapter outlines the conclusions and recommendations for future work on this study. It will also summarise the findings (of the research questions) and demonstrate whether or not the research objectives have been met.

Chapter 2
Literature review

Today, the applications for sampling receivers are not just limited to radar systems, but have moved in to other fields such as: communications receivers, test and measurement equipment, wireless infrastructure equipment and it can even be used for medical imaging applications (Texas Instruments, n.d.). In the majority of the applications, minimum interference is required for maximum accuracy, this makes mitigating SMPS interference critical (Texas Instruments, n.d.). FMCW radar receivers will be reviewed, as a typical application for a sampling receiver.

2.1 FMCW Radar

In order to fully understand the radar sampling receiver subsystem and its power supply, it is imperative to first look at the system in its entirety; hence, the basic operating principles of a FMCW radar system will be reviewed.

What makes the FMCW (Frequency Modulated Continuous Wave) radar technique different from the more established pulsed radar technique is that it is utilised for obtaining target range data by transmitting a frequency modulated continuous electromagnetic signal, rather than making use of special pulse timing techniques. The FMCW radar basic operating principle is graphically illustrated in **Figure 4** (Siversima, 2011) (Stove, 1992) (Skolnik, 1980).

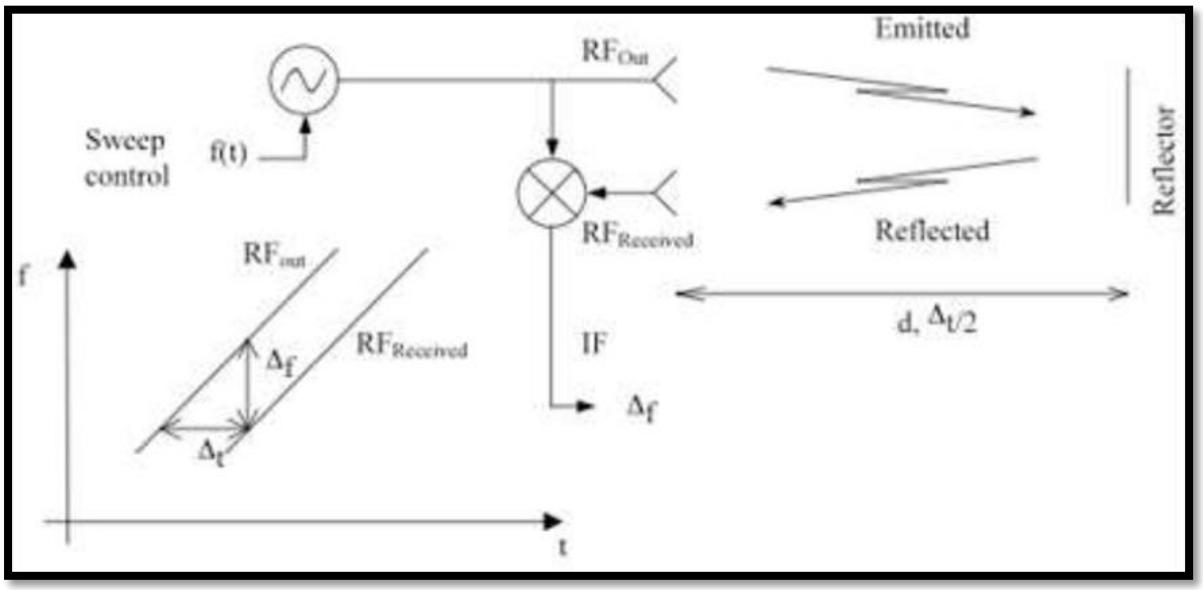

Figure 4: FMCW Radar Basic Operating Principle (Siversima, 2011)

Figure 4 is a "schematic" representation of the FMCW radar basic operation. The system operates as follows: the frequency of the transmitted signal is modulated (varied) over time, while keeping constant amplitude, hence, generating a linear frequency sweep across a pre-determined bandwidth. The simplest and most commonly used frequency modulation pattern for the transmitted signal is the saw-tooth function. The transmitted RF (Radio Frequency) signal will be reflected off the target, back to the radar (Siversima, 2011) (Griffiths, 1990).

The reflected RF signal, received by the radar will be a replica of the transmitted signal, delayed by the propagation delay (2 ways). The propagation delay is given by $\tau = \frac{2r}{c}$, where r is the target range, and c is the wave propagation velocity in free space. The received RF signal is then mixed with the transmitted signal, producing a new signal, which indicates the difference in frequency between the received and transmitted signal. The instantaneous difference in frequency, called Δ*f*, caused by the time of flight to and from the target, will be in the low frequency IF (Intermediate Frequency) range and may be used to determine the target's range (after the application of signal processing). In other words, the frequency delta is directly proportional to the target range (Griffiths, 1990) (Siversima, 2011).

FMCW radar systems are being utilised for a broad variety of applications. Some applications include naval tactical navigational radar, gun-fire control radar, and it is even used for some automotive radar systems. Additionally, due to the nature of operation of the FMCW system, it has proved to be more reliable, less expensive, and less complex than the pulsed radar systems, making them the radar of choice for many applications (Stove, 1992).

2.2 FMCW Radar Sampling Receivers

The primary function of an FMCW radar sampling receiver is to receive the reflected RF signal, from the target (via the antenna). This received RF signal will then be mixed with the transmitted RF signal, to produce the difference in frequency between the two signals, known as Δf, which provides the mechanism to calculate the target range (as discussed in section 2.1) (Griffiths, 1990) (Skolnik, 1980).

More critically, though, is that the radar sampling receiver is able to detect these reflected RF signals from the target in the presence of interference, noise and clutter. The receiver must not only filter out the unwanted signals, but also amplify the desired ones for signal processing. The requirement to provide sufficient gain, phase and amplitude stability, dynamic range and be as robust as possible, makes receiver design very complicated (Skolnik, 1980).

At X-band frequencies, which are often used for FMCW radar, the external noise entering via the antenna is low (relative to VHF, UHF and other low-microwave frequencies), making the internal noise generated by the receiver (and the rest of the radar) itself the main issue to focus on. The primary objective is to maximise the signal-to-noise ratio of the receiver output signal. In order to achieve this, a matched filter is utilised, which produces the required frequency response of the IF (output) section of the receiver (Skolnik, 1980) (A. M. Ponsford, 1988).

In the next section, the various options for the design of the FMCW Radar Receiver Power Supply will be reviewed, and the most appropriate solutions will be selected for the application at hand.

2.3 FMCW Radar Receiver Power Supplies

In this section, the focus will be on determining whether to use a linear or SMPS for the application. The operation principle of the selected power supply will be researched, as well as, which topology will be best suited for the application. Lastly, possible effects (interference) caused by the power supply, along with their mitigation techniques will be researched.

The power supply will be utilised in a portable radar system. The radar will most likely run off DC battery power, hence, good power supply efficiency is very important. This radar will also be handheld, i.e. very compact. That implies many space restrictions, meaning the power supply needs to be as compact as possible.

2.3.1 Linear Power Supplies vs. Switch-Mode Power Supplies

The aim is now to look at the advantages and disadvantages of both linear power supplies and SMPS's, and then select which type will be the most appropriate for the required application. The more traditional linear power supplies will be reviewed first in this section.

Linear Power Supplies

Advantages:

- Simple to use, and easy to design (Laureniu Teodorescu, 2014)
- No switching interference generated, due to there being no switching elements (Linear Technologies, 2013)
- Faster Transient response than SMPS (Linear Technologies, 2013)

Disadvantages:

- High power dissipation in device (Kuo-Bin ILiu, 1999)
- Low Efficiency (Laureniu Teodorescu, 2014)
- High heat dissipation in device (Brown, 1990)
- Use of heatsink a necessity (Brown, 1990)
- Low Power Density (Large size) (Linear Technologies, 2013)

From the list of disadvantages of linear power supplies discussed, it is evident that there are quite a few drawbacks, which leads us to the review of the advantages and disadvantages of the SMPS as an alternative.

Switch-Mode Power Supplies

Advantages:

- Low power dissipation in device (Linear Technologies, 2013)
- High efficiency (Laureniu Teodorescu, 2014)
- Low heat dissipation in device (Brown, 1990)
- High power density (Compact size) (Linear Technologies, 2013)

Disadvantages:

- More complex to design than a linear power supply (Laureniu Teodorescu, 2014)
- Switching interference generated by switching elements (Dunfan Ye, 2011)
- Slower Transient response than Linear power supply (Linear Technologies, 2013)

Conclusion

The use of a linear power supply will eliminate the interference created by a SMPS. The disadvantages of a linear power supply is that they dissipate an excessive amount of power and this makes them inherently inefficient, and along with the excessive power dissipation also comes excessive heat dissipation. The heat will have to be countered with the use of a heatsink, which will increase the size of the power supply dramatically. Due to the portable radar system requiring its power supply to be as efficient and as compact as possible, the use of a SMPS is preferable for this application (due to its high efficiency and compact size). Using a SMPS will, however, leave the system susceptible to noise generated in the Intermediate Frequency (IF) range, as a result of its switching nature (Laureniu Teodorescu, 2014) (Linear Technologies, 2013) (Kuo-Bin ILiu, 1999) (Brown, 1990) (Dunfan Ye, 2011).

2.3.2 Switch-Mode Power Supplies

For the current application, the input voltage, from the Radar Power Distribution Unit, needs to be stepped down to the voltage level required by the Receiver subsystem. Since it was concluded in section 2.3.1, that the SMPS is the best type of power supply for this application, we will hence be reviewing the step down SMPS.

Basics of the step down converter (Buck converter)

As suggested by the name, the step down (buck) converter produces a lower output voltage, than its input voltage. The buck converter in its simplest form consists of a switch, diode, inductor, and a capacitor. The buck regulator operates in two states (during continuous mode), the on-state, meaning the switch is closed, as well as the off-state, when the switch is open. The basic circuit in the on-state is illustrated in Figure 5 (Radio-Electronics, n.d.) (Mohan, et al., n.d.).

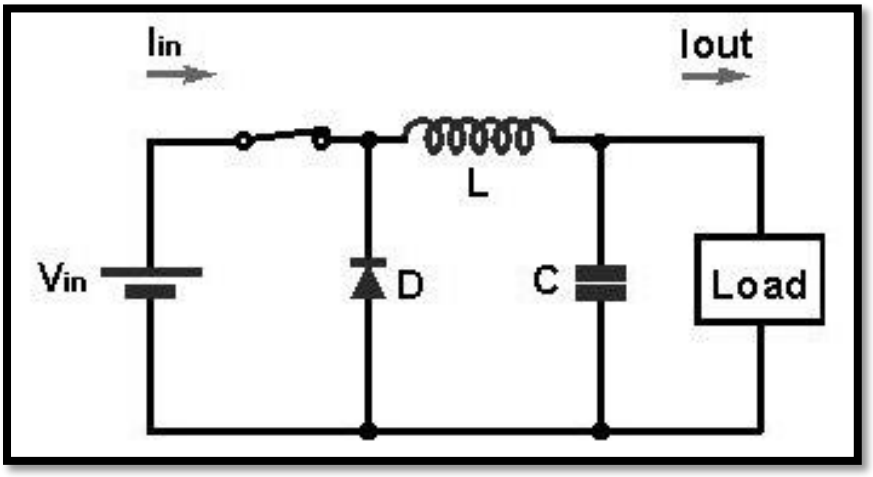

Figure 5: Basic Buck Regulator (on-state) (Radio-Electronics, n.d.)

Figure 5 illustrates the buck regulator in the on-state. During the time when the switch is closed, the diode is in reverse bias, and will not conduct. The input power source will then provide energy to the load and inductor. At this point, the voltage Vin-Vout appears across the inductor. According to the inductor equations, the inductor current rises according to $\Delta I_l = \frac{V_{in}-V_{out}}{L}$. Next we look at the buck regulator in the off-state in Figure 6 (Radio-Electronics, n.d.) (Mohan, et al., n.d.) (Kwasinski, 2014).

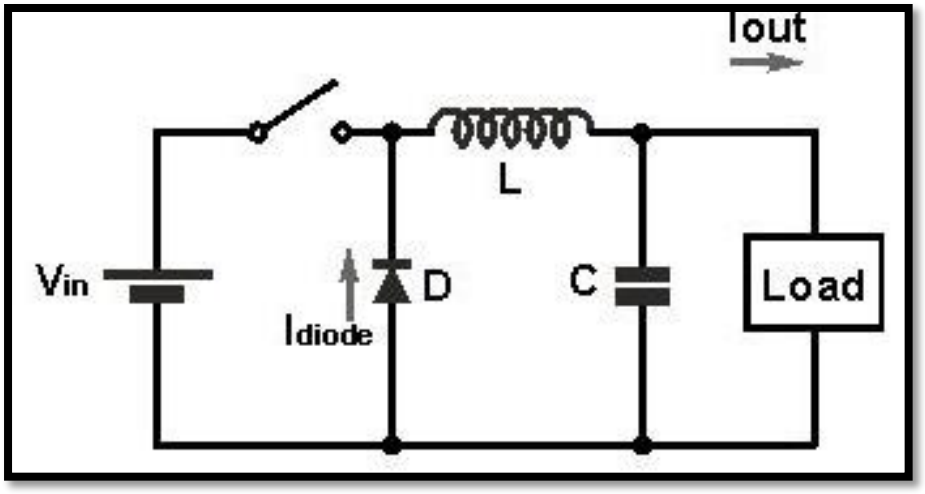

Figure 6: Basic Buck regulator (off-state) (Radio-Electronics, n.d.)

Figure 6 illustrates the buck regulator in the off-state. During the time when the switch is open, the diode is in forward bias, and will be conducting. Since the diode then completes the circuit by forming the return path ($I_{diode} = I_{out}$), the current continues to flow to the load, as the inductor will attempt to maintain a constant current. The open switch means the polarity across the inductor is now reversed, and the current through the inductor will decrease with a gradient equal to $\frac{-V_{out}}{L}$ (Radio-Electronics, n.d.) (Mohan, et al., n.d.) (Kwasinski, 2014).

The combined effect of this circuitry is that, as oppose to the output being a large square wave (across the load), there is a DC output with a small (high frequency) ripple voltage. The function of the output capacitor is to provide voltage "inertia" and hence filter this ripple voltage and make it as small as possible (It is essentially a smoothing capacitor). The output DC voltage level would vary according to $V_{OUT} = V_{IN}\frac{t_{on}}{T}$, where t_{on} is the time that the switch is on and T is the period of the switching waveform (Learnabout electronics, n.d.) (Kwasinski, 2014).

The basic buck converter topology is the simplest form of a step-down DC-DC converter SMPS topology, and is thus one of the most widely used in industry. The basic step down (buck) converter SMPS is illustrated in Figure 5 and Figure 6. Section 2.3.2 - Operation also explains the converter operation in detail. This simple topology is highly efficient, and very compact in size, due to the use of only the essential components. Additionally, the use of only the essential components means rapid design times and keeps the component procurement costs to a minimum (Laureniu Teodorescu, 2014) (Linear Technologies, 2013).

Series Parallel Resonant converter

The half bridge series parallel resonant converter seen in Figure 7, combine the positive attributes of both the series resonant converter and the parallel resonant converter. This converter is best suited for higher voltage applications, while we will have a very low input voltage of 12V. In order for it to be the most efficient, it needs to operate at its resonant frequency, which may be quite restricting in our application. The use of so many components (especially the transformer) increases the cost, size and design time dramatically (Yang, 2002).

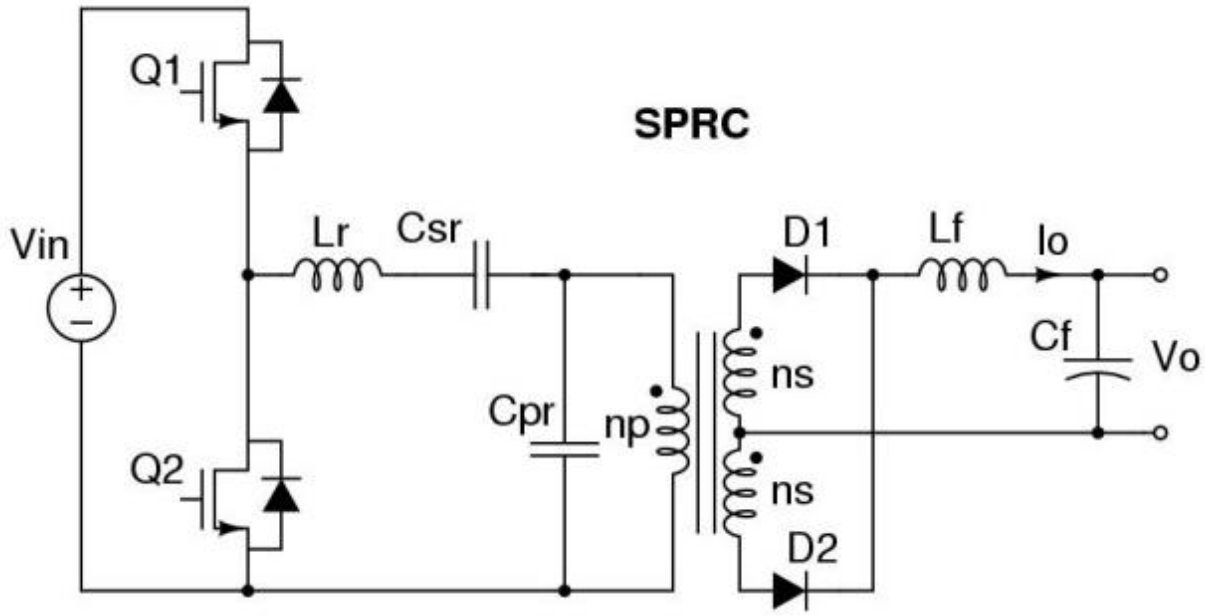

Figure 7: Half bridge series parallel resonant converter (Yang, 2002)

Quasi-Resonant converter

Figure 8 illustrates a simplified version of the Quasi-Resonant zero-current switching DC-DC converter. Historically, high switching losses (at high switching frequencies) was the main problem with these converters. With the introduction of the zero-current switching (ZCS) mechanism, they are now able to switch up to 1MHz. The efficiency of these converters is quite high and they are very stable, making them well suited for the application. The problem is that this converter is expensive to mass produce, and designing to comply with the space constraints will be very difficult (Marchetti, n.d.).

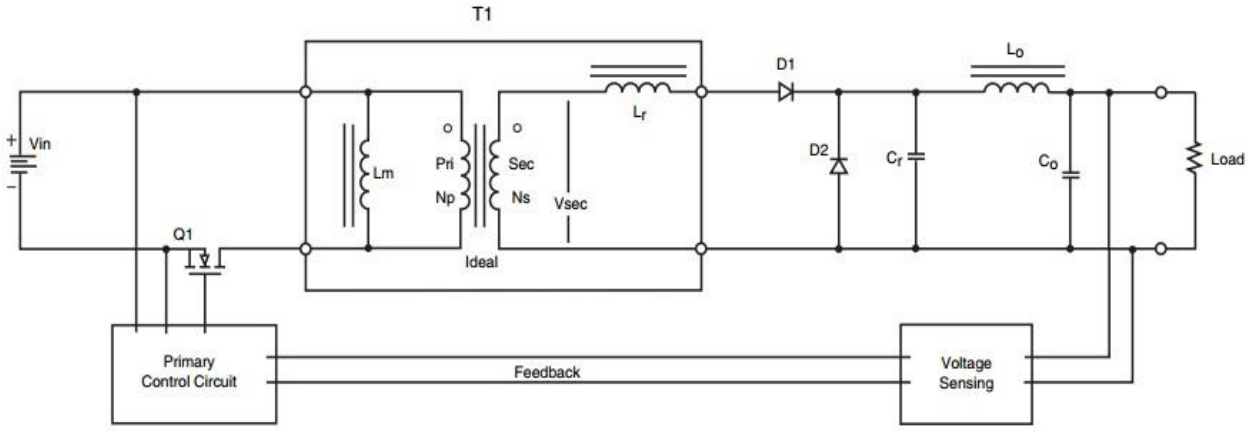

Figure 8: Quasi-Resonant zero-current switching DC-DC converter (Marchetti, n.d.)

Multi-phase converter

A basic multi-phase converter is shown in Figure 9, with N number of phases. This topology is ideal for high current applications. With this converter, the fundamental frequency gets multiplied by the amount of phases used. The advantage is that this will reduce the output voltage ripple, which lowers the requirement for output capacitance. In turn, this makes it possible to use small inductances, which improves the transient response. Overall the converter EMI may be greatly reduced with this topology. With our application, though, we require a very low output current. We would need double or triple the size and cost of the circuit to achieve this lower EMI, as it will essentially be equivalent to two or three basic buck converters. Unfortunately, this dramatic increase in size and cost does not warrant the advantage of the reduced EMI, and marginal gain in efficiency (Hegarty, 2007) (Xu, 2002).

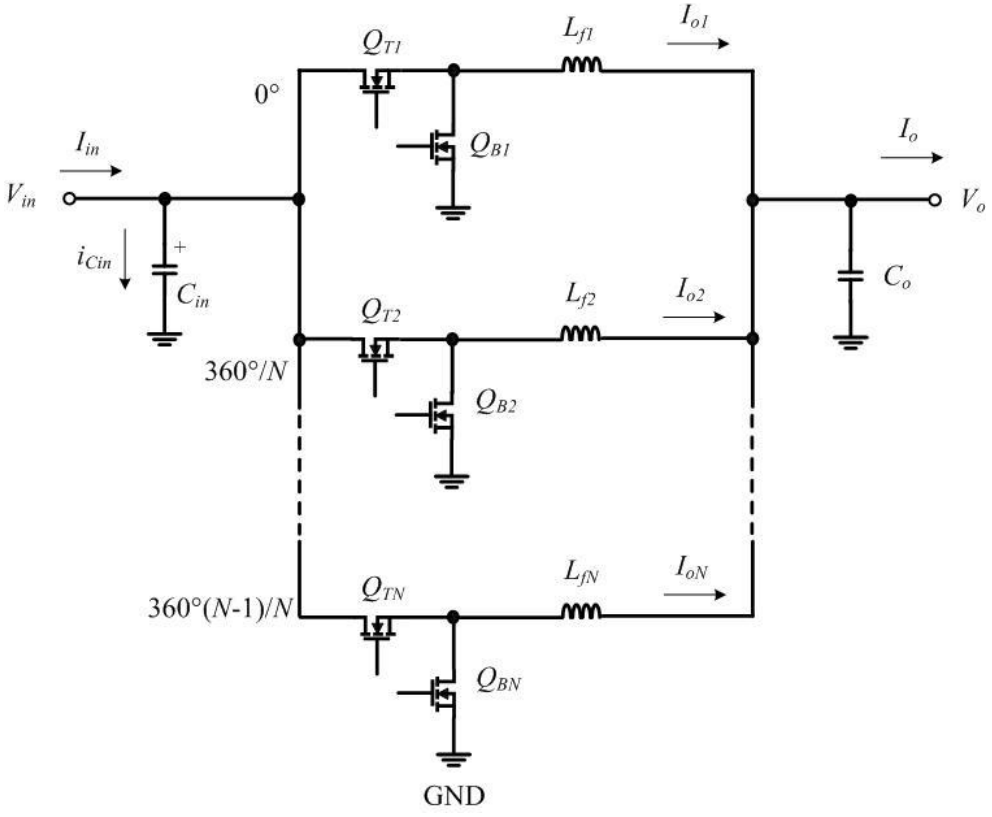

Figure 9: N-phase interleaved Multi-phase converter (Hegarty, 2007)

Ćuk converter

The Ćuk Converter seen in Figure 10 has a very similar operating principle to the buck-boost converter. Similarly to the buck-boost, it is also able to step up or down the input voltage. The capacitor C1 is mainly responsible for the storing and transferring of energy form the input to the output. This converter has no magnetic elements, which helps keep the physical size small. The efficiency is also high, and the cost will only be moderately more than a basic buck. The only advantage of this topology over the basic buck is that it can step up and down. For our application we will only be stepping down the voltage, making this topology "over-kill" for the application (Mohan, et al., n.d.) (Wael A Y Salah, 2006).

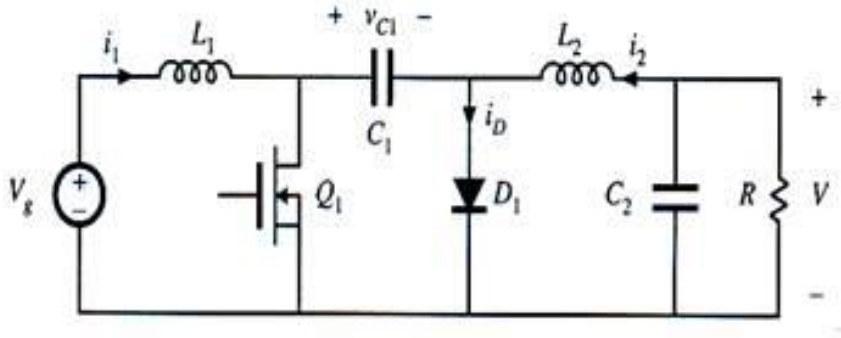

Figure 10: Ćuk Converter (South Virginia University, n.d.)

Conclusion

From the research, it can be concluded that the use of a basic buck converter topology would be best suited for the application. This is mainly due to its very high efficiency, few components, and lack of magnetic elements, which makes it compact in size, and inexpensive to procure or develop (Laureniu Teodorescu, 2014) (Linear Technologies, 2013).

The problem, in our application, is that the SMPS's generally operate in the Intermediate frequency (IF) range and the desired output frequencies of the receiver subsystem are also in the IF range. This means that the receiver matched filter will not filter out the SMPS interference, if it manages to propagate through to the receiver output stage. As a direct result, the signal processesor may interpret this SMPS interference as data, causing it to be displayed as a target on the Range-Doppler map. This false target is highly undesirable, as it desensitises the radar, in that specific area. The challenge is now to find a method of mitigating the interference introduced by the SMPS, in order to eliminate the false targets. This will be reviewed in the next section (Ho-En Liao, 2013).

2.3.3 The Effect of Switch-Mode Power Supplies on Sampling Receivers

This section covers the effects of SMPS's, which could adversely affect sampling receivers. It also provides good insight into exactly what effects are most important to mitigate.

The buck converter SMPS requires a rapid rectangular switching action in order to be as efficient as possible. The problem is that this rapid switching action produces a large spectrum of noise. The noise can be divided into two main categories i.e. radiated EMI and conducted EMI (Sulekh Chand, 2006).

The conducted EMI is mainly due to the switching nature of the SMPS. During switching, changes in current $\left(\frac{dI}{d_t}\right)$ and voltage $\left(\frac{dV}{d_t}\right)$ are experienced. These continuously changing parameters generate a huge amount of interference in the RF spectrum. The largest contributor to the IF spectrum interference is, however, the switching of the converter itself (Mee & Teune, 2002) (Miloudi, et al., 2012).

Energy at the fundamental frequency (the converters switching frequency), as well as several of its harmonics, propagates (via conduction) onto electrical interconnecting harnesses, and thus get transferred between subsystems (Sulekh Chand, 2006) (Mee & Teune, 2002).

Receivers typically down-convert the received signal to IF, which can typically be in a similar frequency range to the SMPS frequency. The receivers also incorporate a lot of gain at these frequencies (to increase the receiver sensitivity), and this gain is increased even further during signal processing. The switching interference may then be interpreted as data (van der Merwe, 2015) (Ho-En Liao, 2013).

In an FMCW radar system, for example, a constant frequency in the IF band will be interpreted as a target. So if the switching interference is interpreted as radar data, the "false" target has the potential to mask a "real" target, if they are in close proximity on the Range-Doppler Map (RDM). This is obviously highly undesirable, and it is thus imperative to mitigate the switching interference. The mitigation techniques are discussed in detail in the next section (van der Merwe, 2015).

2.3.4 Mitigation of the Effect of Switch-Mode Power Supplies on Sampling Receivers

In this section we look at various techniques that may be used to mitigate the effects of SMPS's on sampling receivers (discussed in the section 2.3.3). The best technique will then be selected and the additional considerations that need to be made when designing the PCB will also be discussed in detail.

Technique 1- Linear Power Supply after SMPS output

The first technique is the use of a linear power supply after the output of the SMPS. This technique was previously utilised in (A. Fazzi, 1996) and is illustrated in a block diagram in Figure 11.

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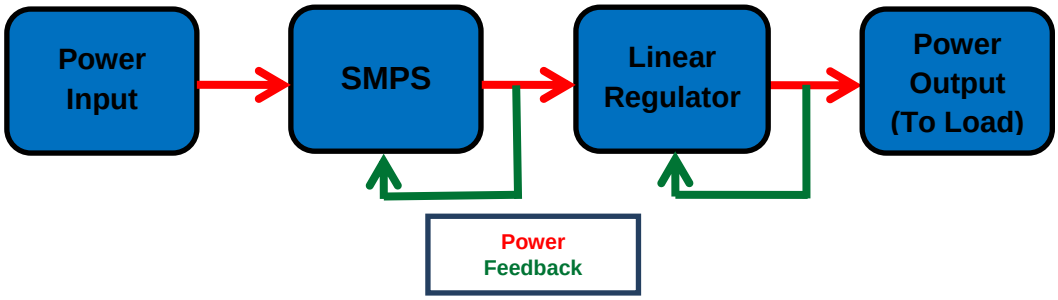

Figure 11: Technique 1 - Linear Power Supply after SMPS output

The method of using a linear power supply after the output of the SMPS is shown in

Figure 11 11. The idea behind this technique is to be able to achieve the benefits of both types of power supplies, meaning, the efficiency of a SMPS combined with the low noise, accurate output of a linear power supply (A. Fazzi, 1996).

This technique has proven to work well to eliminate the conducted switching interference (generated by the SMPS) on the Receiver subsystem input power lines (i.e. power supply output lines) (Linear Technologies, 2013).

The down side is that there is still the possibility that the SMPS switching interference may propagate to the receiver subsystem via other ground loops, either by conduction only or by radiation and then conduction onto other electrical interfaces (Sulekh Chand, 2006).

There will also still be minimum dropout voltage on the linear regulator which is essentially lost as heat, this means reduced efficiency. The added linear regulator circuitry will also increase the size and cost of the power supply PCB (Linear Technologies, 2013) (Laureniu Teodorescu, 2014).

Technique 2 – Synchronising to the Sample Frequency

In this technique, the idea is to synchronise the SMPS frequency to the sampling frequency of the receiver subsystem (or a multiple thereof). By doing this, the aim is to effectively "hide" the SMPS frequency after it has been sampled (digitised) by the receiver's analog to digital converter (ADC). This approach has previously been used in audio and other systems (which do analog to digital conversion), in order to prevent unwanted mixing products and interference. (Pefhany, 2014).

To understand this concept, one needs to understand the basics of sampling theory. Firstly, the nyquist sampling theorem states that the sampling frequency should be at least twice the frequency being measured to avoid aliasing i.e. $f_{sam} \geq 2 \times f_{measured}$. The nyquist frequency is given by $f_n = f_{sam} \div 2$ (Olshausen, 2000) (National Instruments, 2016).

The easiest way to explain aliasing is with a practical example. If the sample frequency is 2kHz, this gives a nyquist frequency of 1kHz. If we use a measured frequency is 0,75kHz, the nyquist sampling theorem will be satisfied and the digitised resultant frequency will be given by $f_{digital} = f_n - |f_{measured} - f_n|$ which is 0,75kHz in this case (Olshausen, 2000) (Indiana University, 2013).

If we do not satisfy the nyquist sampling theorem, on the other hand, and measure a frequency of 1,5kHz, the digitised resultant frequency will be 0,5kHz. In this case the signal aliased around the nyquist frequency according to $f_{digital} = f_n - |f_{measured} - f_n|$ (Olshausen, 2000) (Indiana University, 2013).

From this literature, we see that, theoretically, if your SMPS frequency is equal to the sampling frequency of the receiver subsystem (or a multiple thereof), it should aliase back to 0Hz (DC) after digitisation, according to $f_{digital} = f_n - |f_{measured} - f_n|$. This makes this technique extremely desirable, as it will effectively "hide" the SMPS frequency after it has been sampled (digitised), hence mitigating the interference caused by the SMPS (National Instruments, 2016) (Indiana University, 2013).

Finally, with the application of this approach, a synchronous buck converter package will need to be utilised. This technique will also only be relevant when the sampling frequency is lower or equal to the switching frequency. Further investigation into this technique will be done in section 2.4.

Technique 3 – Synchronising to the Sweep Repetition Frequency (SRF)

With Technique 2, the problem is that, in some cases the switching frequency cannot be controlled to be a multiple of the sampling frequency. This is due to the sampling frequency often being higher than typical switching frequencies. In this instance technique 2 may not be implemented.

In Technique 3, we review the idea of synchronising the SMPS frequency to the Sweep Repetition Frequency of the signal processor. The sweep repetition frequency is typically much lower than the sample frequency, thus making it easier to synchronise with. This approach has been used previously in many wireless communication systems, not necessarily for SMPS synchronisation, but for the synchronisation of other subsystems, in order to prevent signal processing errors due to interference (Salous, 2008).

In order to grasp this concept, one needs to understand the basics of the Range-Doppler Processing (RDP) performed by the signal processor. The RDP technique is specifically used for FMCW radar systems. Generally, how RDP works is that two Fast Fourier Transforms (FFT's) are applied to the receivers output signal. The first is the range FFT, which is done to determine the targets range. The second is the bank of Doppler FFT's, which is done to determine the targets velocity. The velocity is calculated by the change in phase of the target, i.e. zero change means the target is stationary (Aljasmi, 2002).

So essentially, we want to synchronise the SMPS frequency to the sweep repetition frequency of the Doppler FFT. This means every time the sweep is performed, the phase of the SMPS frequency will remain unchanged (zero phase-shift) relative to the sweep repetition frequency of the Doppler FFT. This approach produces a predictable response (stationary target in FMCW systems). This stationary target may then be filtered out (along with other stationary targets and noise) in the post-processing filtering (van der Merwe, 2015) (Peter Deacon, 2011).

Finally, with the application of this approach, a synchronous buck converter package will also need to be utilised. This technique may also be used in conjunction with technique 2. This technique can thus be concluded to be well suited for the portable radar application, as it would also effectively "hide" the SMPS frequency on the Range-Doppler Map (RDM). Further investigation into technique 3 (RDP) will be done in section 2.5.

Technique 4 – Pulse Width Modulation (PWM)

The Pulse Width Modulation Technique is also known as the “spread spectrum technique”. This “spread spectrum technique” has been utilised successfully by (Lin, 1993).

The mode of operation of this technique is to vary the switching frequency of the SMPS, by changing the SMPS switch gate driver PWM frequency continuously over a certain range of frequencies. Compared to a fixed switching frequency, this would then greatly reduce the conducted EMI and its harmonics, when viewed by spectral analysis. In simple terms, the energy generated by the SMPS’s switching, would spread across the spectrum, rather than being the clearly defined peaks seen when using a fixed switching frequency (Mainali, 2010).

The issue with this technique is that the modulating parameters can cause significant side effects, like additional noise generated due to the frequency variation and poor converter output regulation. Additionally, since the switching frequency will be “random”, it becomes much less predictable, and harder to trace back to. This technique would also require additional circuitry to generate the “random” PWM frequency, which in turn increases the size and cost of the SMPS (Mainali, 2010) (Lin, 1993).

To summarise, this approach may have significant benefits, but they are unfortunately still out-weighed by the side-effects for the portable radar application at hand. It would hence not be feasible to implement this technique in this study.

Conclusion

With the use of a linear regulator after the SMPS, there is still the possibility switching interference propagatation via other interfaces (Sulekh Chand, 2006). This technique also compromises the overall efficiency, and the added linear regulator circuitry increases the size and cost of the power supply PCB, hence this is deemed unsuitable for the application (Linear Technologies, 2013) (Laureniu Teodorescu, 2014).

The techniques of synchronisation to the sampling frequency and SRF makes a lot of sense to evaluate for the application at hand, as it will effectively “hide” the SMPS frequency after it has been sampled (digitised), hence mitigating the interference caused by the SMPS (National Instruments, 2016) (van der Merwe, 2015) (Indiana University, 2013).

Using the technique of synchronisation to the SRF produces a predictable response i.e. stationary target in FMCW systems. This stationary target may then be filtered out (along with other stationary targets and noise) in the post-processing filtering, making this technique feasible for further investigation (van der Merwe, 2015) (Peter Deacon, 2011).

From here, the approach that will be adopted will be to control the switching frequency of the converter, by using a buck converter IC package with a “synchronisation input”. This will allow the SMPS switching frequency to be controlled by an external clock, in order to synchronize it either to a multiple of the sampling frequency and or to the SRF of the radar. These two techniques will be investigated further in sections 2.4 and 2.5 respectively. The next section covers the considerations that need to be made when doing the PCB design; these considerations will be applied in conjunction with the techniques discussed in section 2.3.4.

PCB Design Considerations

According to (Mee & Teune, 2002), (Sulekh Chand, 2006) and (Linear Technologies, n.d.) The conducted EMI of a SMPS may be greatly reduced by giving special attention to the following areas during the SMPS PCB design:

1. Minimising loop areas in the PCB layout.
2. Reduce the parasitic inductance and capacitance by careful placement of components.
3. Ensure sufficient filtration of the input and output.
4. Use Low ESR capacitors for input and output filtration.
5. Minimise trace inductance (avoid unnecessarily long tracks).
6. Segregate the signal ground, power ground and GND return layers.
7. Use ground pours (flood) all unused areas with copper on all the layers.

Point 6 and 7 are particularly important, in that they will greatly change the layout design of the PCB. Given that a basic buck converter SMPS PCB consists of relatively few components, the layout may easily be done on a 2-layer board.

In this case though, there are quite high $\left(\frac{dI}{d_t}\right)$ transients in the power path that must be kept isolated from the GND return path. This means, ideally, the power ground, GND return and signal ground layers should be kept separate. They may then be connected via a common, low noise reference point (a Kelvin connection). This makes the use of a 4-layer board preferable for this application (Mee & Teune, 2002).

The next section looks at general sampling theory, which ties in with the Technique 2 – Synchronising to the Sample, discussed in this section.

2.4 Sampling Theory

This section provides a background to sampling theory and explains how the manipulation of the frequency of the SMPS may be used to exploit the Nyquist frequency of the sampling frequency. This section ties in with the technique of synchronising the SMPS frequency to a multiple of the sample frequency in section 2.3.4. This method is only relevant when the sampling frequency is lower or equal to the switching frequency.

Figure 12 illustrates analog signals in the frequency domain; this is essentially the "real life" input data to be sampled by the Analog to Digital Converter (ADC), or Δ*f* from the Receiver subsystem in FMCW radar for example (National Instruments, 2016).

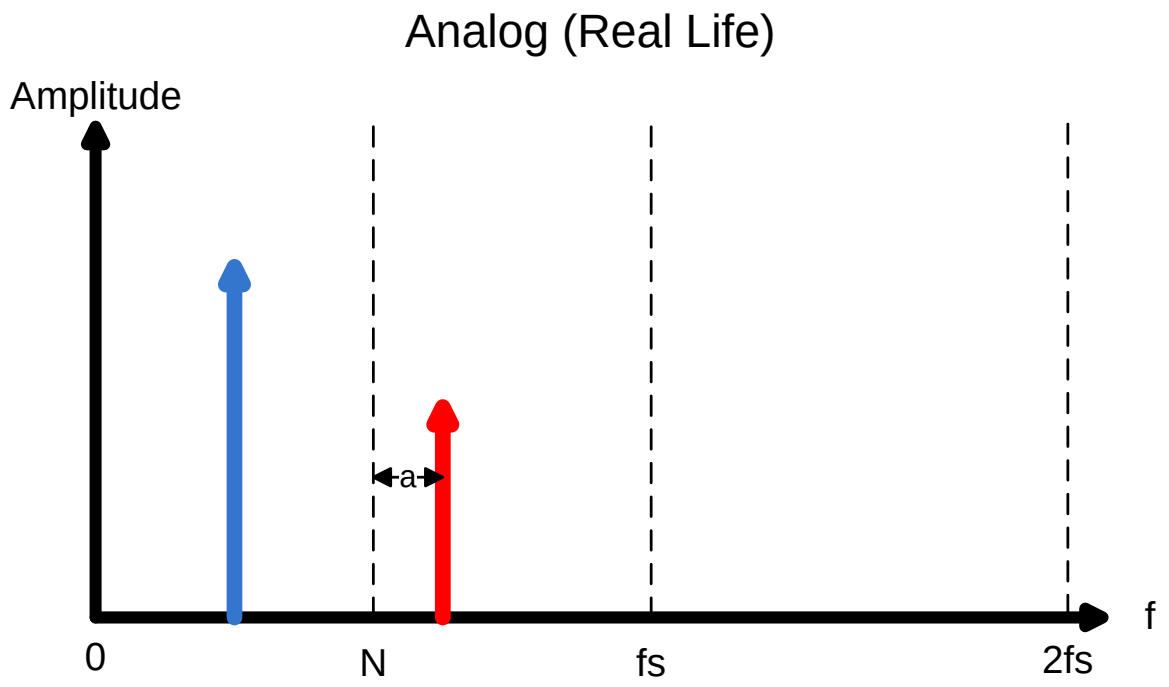

Figure 12: Analog signals in the frequency domain (National Instruments, 2016) (Olshausen, 2000)

In Figure 12, 2 signals are shown, the blue signal being below the Nyquist frequency and the red signal above the Nyquist by a frequency "a". These are the analog signals which will be sampled. The post-digitisation results (sampled signals) are shown in Figure 13 (Olshausen, 2000) (National Instruments, 2016).

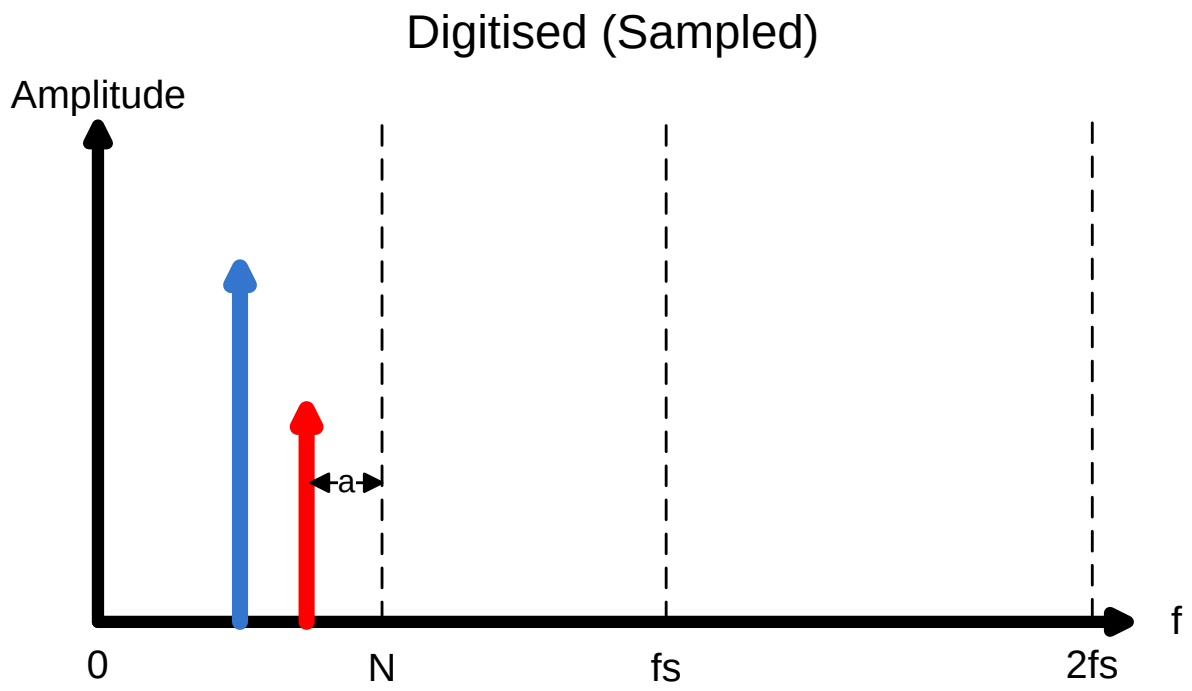

Figure 13: Digitised/Sampled signals in the frequency domain (Indiana University, 2013) (Olshausen, 2000)

Figure 13 shows the sampled signals in the frequency domain. The frequency of the blue signal has remained unchanged, but the red signal has "folded back" and is now less than the Nyquist frequency by "a". This process is known as aliasing (Olshausen, 2000) (Indiana University, 2013) (National Instruments, 2016).

What can be deduced from the above literature, is that if $f_{SMPS} = N \times f_{Sampling}$, then the SMPS frequency will aliase to DC or 0Hz. Another example of this phenomenon is graphically illustrated in Figure 14.

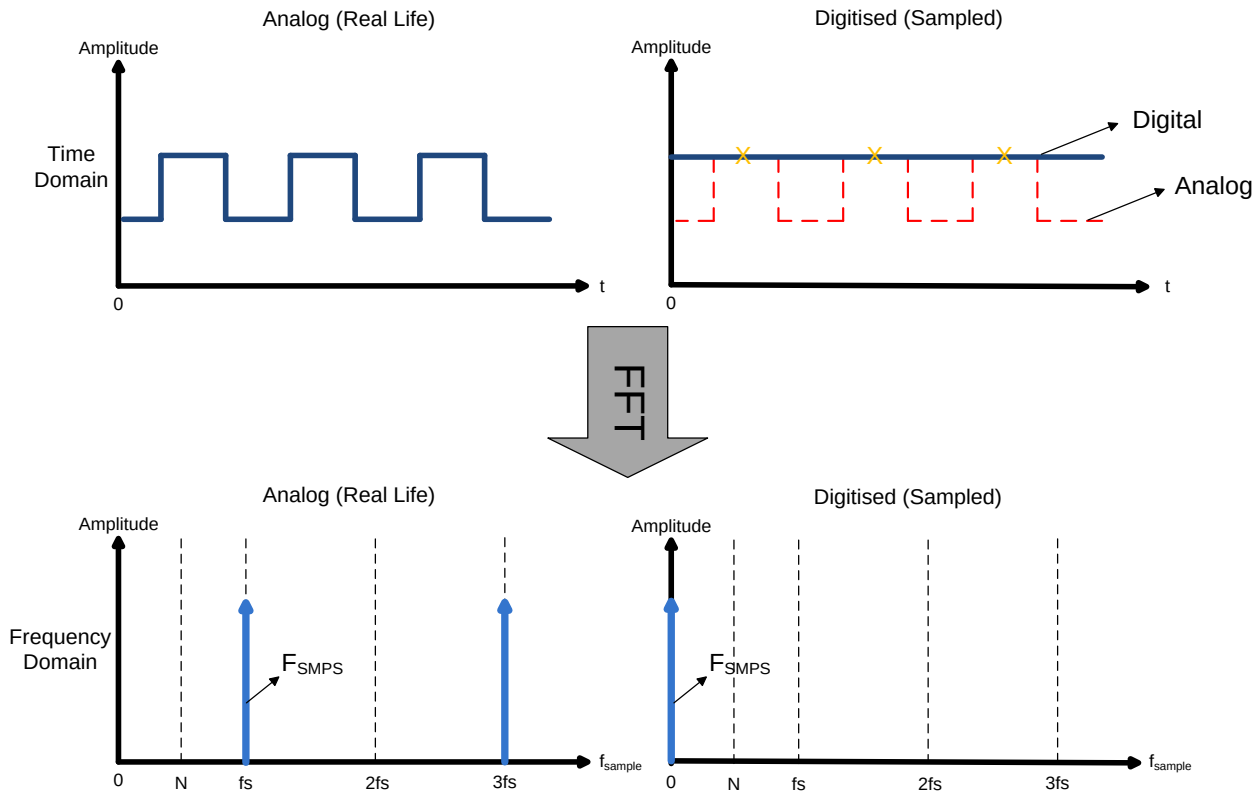

Figure 14: Example of the exploitation of the Nyquist frequency (Indiana University, 2013)

Figure 14 shows an example of a typical switching signal from a SMPS – a square wave. It illustrates this signal in analog form and after digitisation (sampling), in both the time and frequency domains (van der Merwe, 2015).

The top left shows the signal in analog form and the top right show the same signal after digitisation (both in the time domain). Due to, in this case, $f_{SMPS} = 1 \times f_{Sampling}$, the sampled result is DC or 0Hz (van der Merwe, 2015) (Indiana University, 2013).

The bottom graphs show the frequency domain after an FFT has been applied. Here it is clear that $f_{SMPS} = 1 \times f_{Sampling}$, and the harmonics generated will naturally be at $3 \times f_{Sampling}$ and $5 \times f_{Sampling}$ etc. This means that the harmonics will also be a multiple of the sampling frequency, and hence, all of these frequencies will aliase to DC or 0Hz, as can be seen in the bottom right graph. This effectively "hides" the SMPS frequency at DC for sampling receiver applications, and makes the implementation of the technique ideal for our study (van der Merwe, 2015).

2.5 Range-Doppler Processing (RDP)

In this section basic Range Doppler Processing is explained in more detail. This section ties in with the technique of synchronising the SMPS frequency to the Sweep Repetition Frequency (SRF) in section 2.3.4. In the case where the switching frequency cannot be controlled to be a multiple of the sampling frequency (the sampling frequency is often higher than typical switching frequencies), this approach may be applied. This method is illustrated in Figure 15.

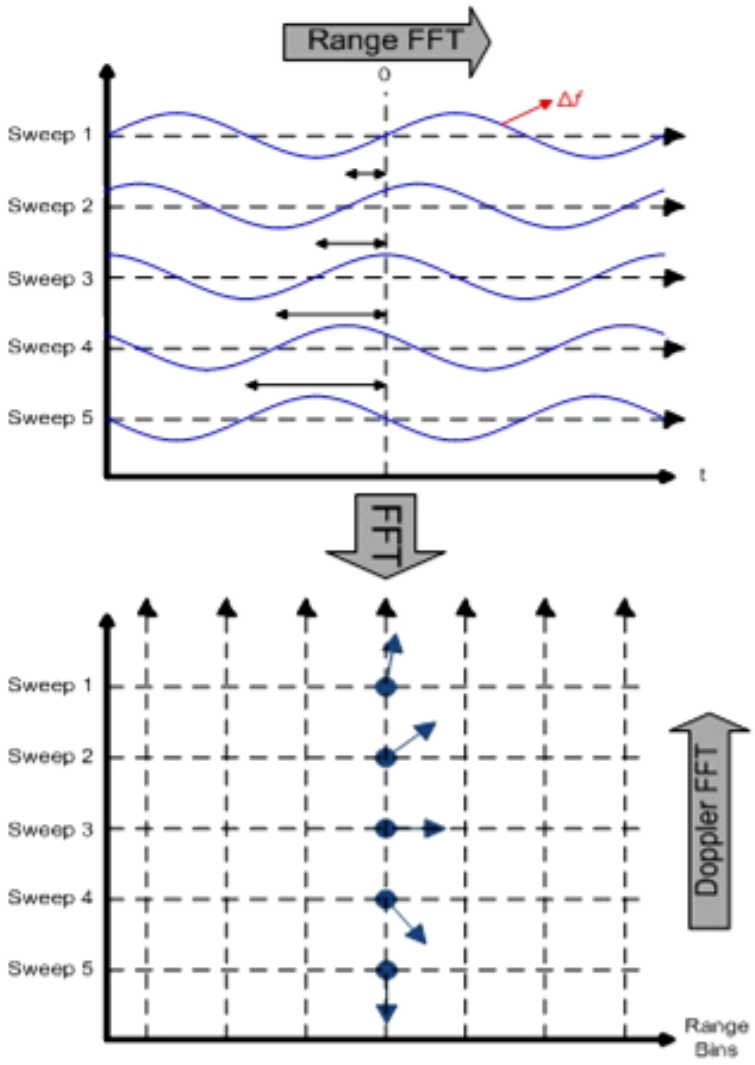

Figure 15: Example of Range-Doppler Processing (Thomas Wagner, 2013)

Figure 15 shows the Range-Doppler Processing of radar data from the receiver subsystem. At this point another FFT is performed, and the resultant Range-Doppler Map can be seen in Figure 16.

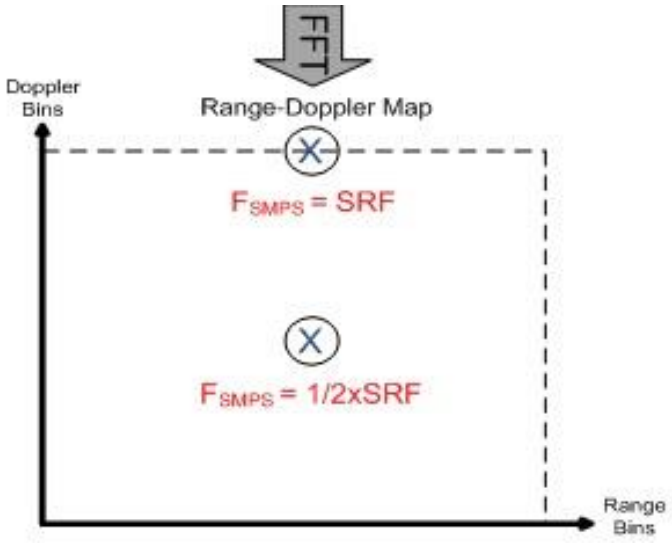

Figure 16: Example of a Range-Doppler Map (RDM) (Thomas Wagner, 2013)

The top graph in Figure 15 illustrates how the phase of Δ*f* from the radar receiver subsystem (in section 2.1) changes as a target approaches or moves away from the radar. After a (horizontal) range FFT is applied to the top graph, the bottom graph is obtained. The bottom graph then also illustrates this phase shift (sweep by sweep), as a clock-wise or anti-clock-wise rotation of the arrows. When a Doppler FFT is applied to the bottom graph (vertically), the resultant is the RDM in Figure 16, on which the target will be a peak, with the vertical location associated with its velocity and the horizontal location associated with its range. This means that when an asynchronous SMPS switching frequency filters through to signal processor, it will be interpreted as moving target, as every time a sweep is performed, it will sample the SMPS switching frequency at a "random" phase (Aljasmi, 2002) (van der Merwe, 2015) (Thomas Wagner, 2013).

However, if the SMPS switching frequency is synchronised to the SRF, the sweep will sample the SMPS switching frequency at the same phase continuously. This approach causes the SMPS switching frequency to be interpreted as a stationary target, at the edge of the RDM, which is a much more desirable and predictable outcome, as it will always appear at the same location on the RDM (rather than continuously hopping around). This can be seen in Figure 16, which shows a RDM and illustrates $f_{SMPS} = SRF$ and $f_{SMPS} = \frac{1}{2} \times SRF$ (van der Merwe, 2015).

From the literature, it can thus be concluded that the use of this method is well suited to the portable radar application, as it interprets the SMPS frequency as a stationary target, at the edge of the RDM, and effectively mitigates the effects of the SMPS interference.

2.6 Industry and Military Compliance

In this section, the reasons for industry and military compliance will be stated. The particular standards to be followed throughout the design procedure will also be listed. Since Reutech Radar Systems is at the forefront of Radar technology, and a supplier of systems to many industry and military clientele, we ensure that by default we design all hardware for military and industry compliance. For the current design only standards relevant to the PCB design, assembly, and harnessing will be reviewed.

For the PCB design, RRS utilises the Altium design rule check to ensure industry and military compliance. The Altium design rule check is a powerful feature which verifies that the logical and physical integrity of the design is compliant to industry and military specifications. Parameters such as such as minimum clearance, tolerances and many others will be verified with this tool (Howie, 2015).

IPC standards provide the best practices for the electronics industry, and also give guidelines for the entire supply chain, from procurement of components to the assembly of electronics. These standards are accepted worldwide as the benchmark specification for aerospace, industry and military grade electronic products, hence the IPC standards are used by RRS as a guideline to design and build in compliance with Military and Industry Specifications (IPC, n.d.).

The following IPC standards will be considered during the design procedure:

- The RRS PCB Pre-Assembly Checklist - to verify that the bare PCB is manufactured and delivered as per the QC (Quality Control) PCB workmanship inspection criteria from IPC-A-600F-Acceptability of Printed Boards Standard. (IPC, 1999).
- The RRS PCB Assembly Checklist - to verify that the PCB was assembled according to IPC-J-STD-001E - Requirements for Soldered Electrical and Electronic Assemblies (IPC, 2014).
- The RRS PCB Assembly Final Inspection Checklist - to verify that the PCB workmanship is in compliance with the inspection criteria from IPC-A-600F-Acceptability of Printed Boards Standard (IPC, 1999).
- The IPC/WHMA-A-620 - Requirements and Acceptance for Cable and Wire Harness Assemblies shall be used to verify that the system integration harnesssing has been done according to IPC specifications (IPC, 2002).

All of the specifications (standards) mentioned above will need to be adhered to strictly, in order to ensure that the final product of the PSU design is fully compliant to industry and military specifications.

2.7 Literature Review Conclusion

Based on the literature reviewed, the SMPS, with the basic buck converter topology is the best option for this application. The mitigation of SMPS interference was found to be critical for sampling receivers and even more so for FMCW radar applications. The bulk of the interference is due to the switching of the power supply itself.

The best approach to minimise this interference is to give special attention to the PCB layout, as well as, either making sure that:

- When switching f > sampling f: Switching frequency is a multiple of the sampling frequency
- When switching f < sampling f: Switching frequency is synchronized to the SRF

The application of both of these techniques simultaneously, should theoretically yield the best outcomes, simply because, the “false target” will then be stationary in range and Doppler. Lastly, all of the Altium design rule check and IPC specifications will be followed strictly, to ensure that the PCB which is designed is industry and military compliant.

Chapter 3
Interference Mitigation Approach Evaluation

The two interference mitigation approaches discussed in Chapter 2, namely, synchronising the SMPS frequency to a multiple of the sampling frequency, as well as, synchronising it to a multiple of the SRF will be evaluated in this chapter. The evaluation will be done by means of simulation, using Matlab.

3.1. Synchronising the SMPS to a multiple of the Sampling Frequency

The Matlab setup below was utilised to perform the simulation of the synchronisation of the SMPS to a multiple of the sampling frequency. The objective of the simulation is to determine if the technique can be used as an effective SMPS interference mitigation approach. The Matlab code can be found in Appendix A – Matlab Simulation Code.

Time Setup

- Set the sample rate to 200kHz
- Set the sample time interval to the inverse of the sample rate ($T = \frac{1}{f}$)
- Set the stop time to 50µs (to view 3 full cycles)
- Set high resolution time vector and sampled time vector parameters
- Set the number of high resolution samples and (time vector) samples
- Setup the frequency of Signal investigated (SMPS Frequency) to 60kHz (default)
- Setup the initial phase of signal investigated (in rad)

Signal Setup

- Setup the Sin waveform
- Setup the sampled Sin waveform

FFT Setup

- Perform an FFT function on the Sin Waveform (to change to Frequency domain)
- Perform an FFT function on the Sampled Sin Waveform (to change to Frequency domain)
- Setup the High resolution frequency vector and sampled frequency vector

Plot Setup

- Setup the time domain plot
- Setup the frequency domain plot
- Setup the graph axis parameters

3.1.2. Investigated Signal (SMPS Frequency) at 60 kHz

Time Domain:

In Figure 17 the analog signal at 60 kHz (which is the SMPS frequency) is shown in the time domain. The sampled interval (at 200 kHz) is shown as red plots, which is superimposed on the 60 kHz signal.

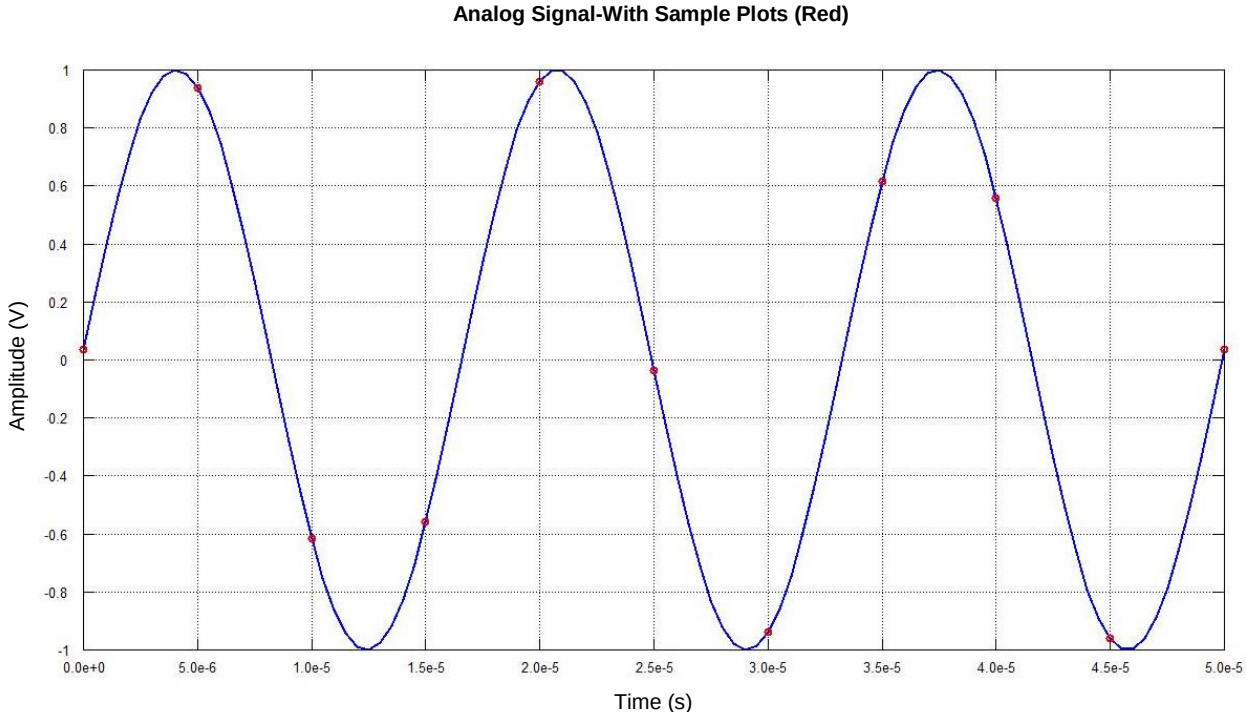

Figure 17: Analog and Sampled Signals in the Time Domain

Figure 17 shows the 60 kHz sinwave (SMPS frequency) in blue, with the sampled signal plots superimposed on it, in red. In this case a t_end of 0.05e-3 was used (instead of 5e-3), in order to zoom in, so that the Sin wave is more clearly defined.

Frequency Domain:

In Figure 18, the FFT'd analog and sampled (digital) signals (at 60 kHz) are shown in the frequency domain. The frequency domain view can also be referred to as a spectrum analysis view.

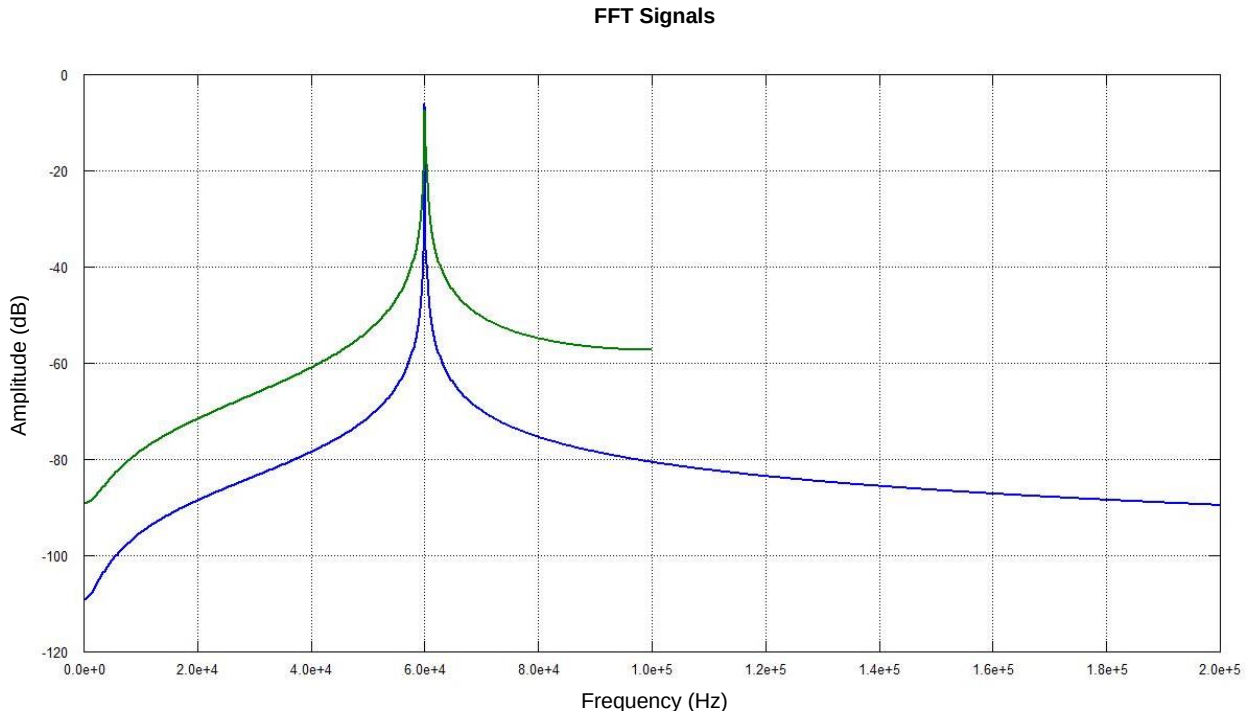

Figure 18: 60 kHz Analog and Sampled Signals in the Frequency Domain

Figure 18 shows the analog 60 kHz signal (SMPS frequency) in blue and the sampled signal in green, in the frequency domain. In this case the t_end was changed back to 5ms in order to see the entire frequency range.

Since the sampling frequency is 200 kHz, the Nyquist frequency is 100 kHz. From Figure 18, we can see that if the SMPS frequency (60 kHz in this case) is lower than the Nyquist frequency, it will be interpreted correctly as 60 kHz after sampling. This will however change when the SMPS frequency is between the Nyquist and sampling frequencies. This phenomenon will be investigated next.

3.1.3. Investigated Signal (SMPS Frequency) at 140 kHz

Frequency Domain:

In Figure 19, the FFT'd analog and sampled (digital) signals, which have now been changed to at 140 kHz, are shown in the frequency domain (shown in spectrum analysis view).

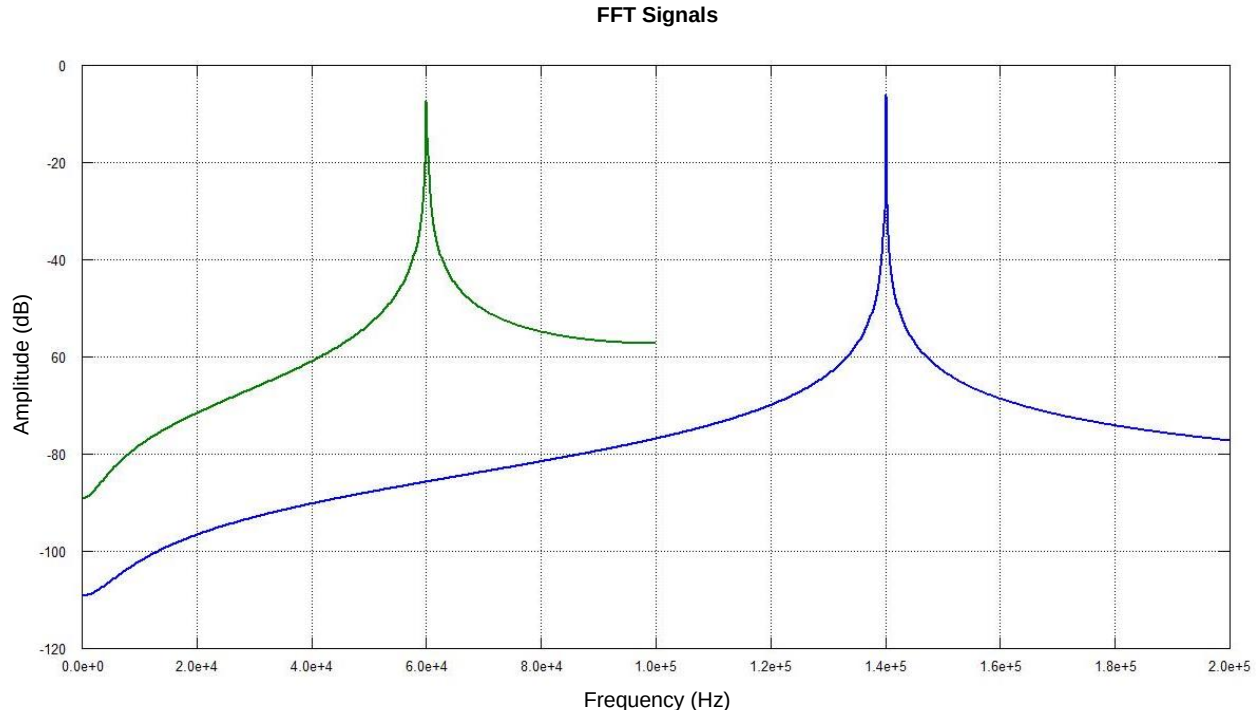

Figure 19: 140 kHz Analog and Sampled Signals in the Frequency Domain

Figure 19 shows the analog 140 kHz signal (SMPS frequency) in blue and the sampled signal in green, in the frequency domain. The setup remains the same as before, with the fo (SMPS frequency) changed to 140 kHz.

From Figure 19, we can see that if the SMPS frequency (140 kHz in this case) is between the Nyquist and sampling frequencies, after being sampled (digitised) it aliases around the sampling frequency. Therefore, in this case, the sampled signal aliases back to 60 kHz, and will hence be incorrectly interpreted.

3.1.4. Synchronising to Sampling Frequency Conclusion

Using the data from 3.1.2 and 3.1.3, it is clear that the Nyquist Frequency may be exploited in order to mask the SMPS frequency. We may now attempt to "hide" the SMPS frequency, by making it equal to a multiple of sampling frequency. In Figure 20 the FFT'd analog and sampled signals (at 200 kHz or 1 x f_{SAMPLE}) are shown in the frequency domain.

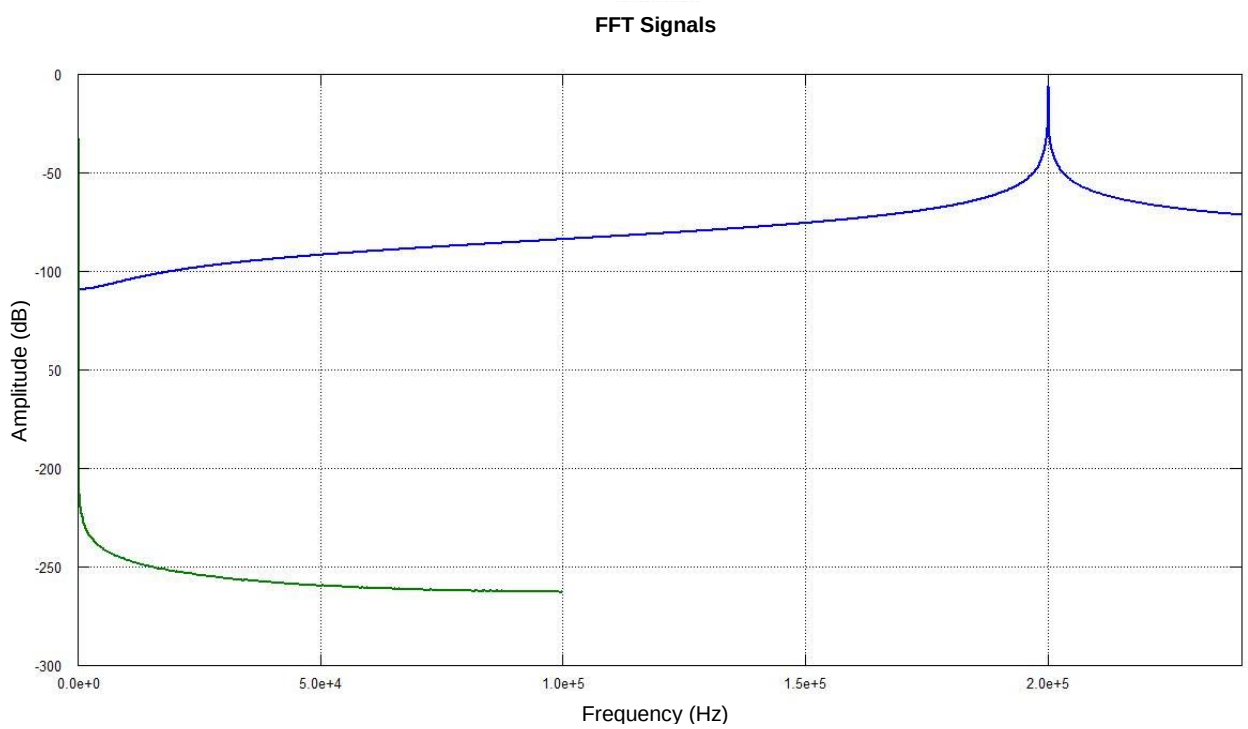

Figure 20: 200 kHz Analog and Sampled Signals in the Frequency Domain

Figure 20 shows the analog 200 kHz signal (SMPS frequency) in blue and the sampled signal in green, in the frequency domain. The setup remains the same as before, with the fo (SMPS frequency) changed to 200 kHz.

From Figure 20, we can see that when the SMPS frequency is equal to a multiple of the sampling frequency (1 x f_{SAMPLE} in this case), the sampled signal aliases back to 0Hz or DC and is effectively "hidden". Thus, this technique can be concluded to be an effective SMPS interference mitigation approach.

3.2. Synchronising the SMPS to the SRF of the Signal Processor

The Matlab setup below was utilised to perform the simulation of the synchronisation of the SMPS to the SRF of the signal processor. The objective of the simulation is to determine if the technique can be used as an effective SMPS interference mitigation approach. The Matlab code can be found in Appendix A – Matlab Simulation Code.

Time Setup

- Setup the sample rate to 200kHz
- Set the sample time interval to the inverse of the sample rate ($T = \frac{1}{f}$)
- Set the sweep repetition interval
- Set the sweep repetition frequency ($SRF = \frac{1}{SRI}$)
- Set the total duration (Burst)
- Setup the sampled time vector
- Set the Freq of Signal investigated (an integer means it is synchronized)
- Set the Initial phase of Signal investigated (in rad)

Signal Setup

- Setup signal (single vector)
- Reshape the signal into burst (256x256)

FFT Setup

- Perform a Range FFT (horizontal direction)
- Perform a Doppler FFT (vertical direction)

RDM Plot Setup

- Setup the plot
- Setup the graph axis parameters
- Setup the colour scaling
- Setup the labels

3.2.1. Investigated Signal (SMPS Frequency) ≠ a multiple of the SRF

In Figure 21, the Range-Doppler Map (RDM) can be seen with the SMPS frequency at a frequency equal to 5,123 times the SRF of the radar signal processor (i.e. asynchronous with the SRF).

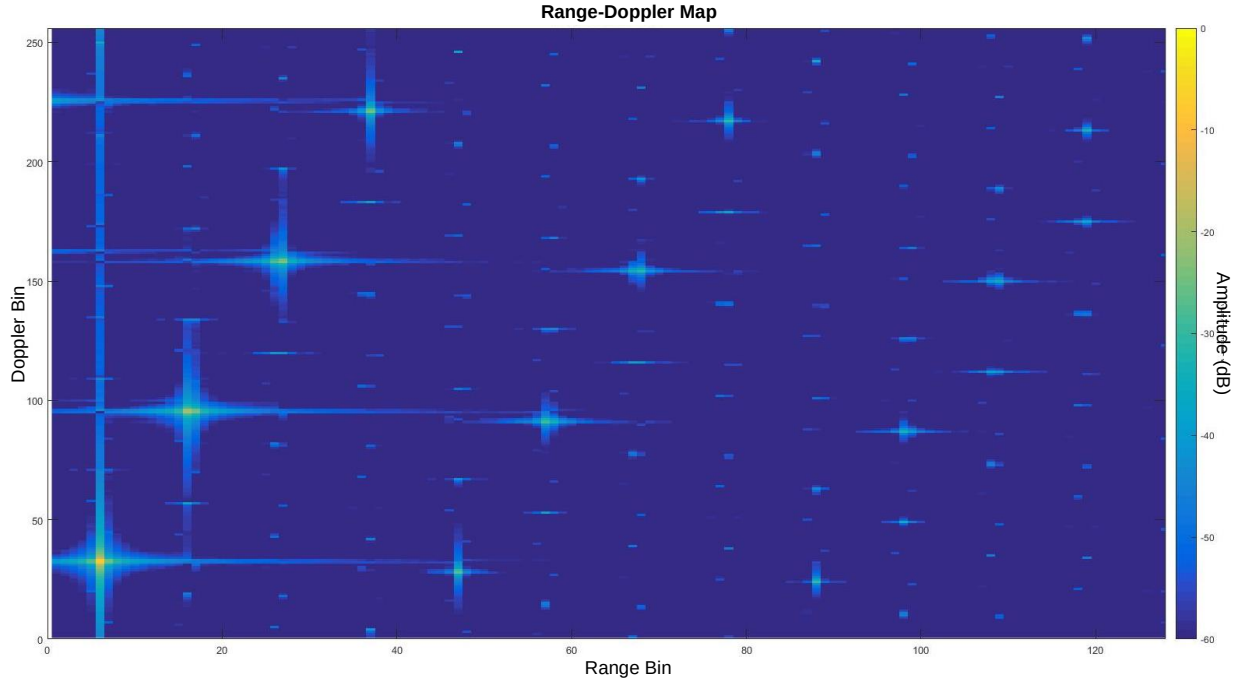

Figure 21: RDM with Investigated signal at 5,123 times the SRF

Figure 21 shows the RDM with the SMPS frequency (fo) not equal to a multiple of the SRF (i.e. 5,123 x SRF). With an asynchronous SMPS frequency, it is clear that after a range and Doppler FFT has been performed, the SMPS frequency and its harmonics are interpreted as moving targets on the RDM. This desensitises the radar completely, as one is not able to distinguish between real and false targets. Section 3.2.2 will illustrate the RDM with a SMPS frequency synchronised to a multiple of the SRF.

3.2.2. Investigated Signal (SMPS Frequency) = a multiple of the SRF

In Figure 22 the Range-Doppler Map (RDM) can be seen with the SMPS frequency at a frequency of 5 times the SRF of the radar signal processor (i.e. synchronous with the SRF).

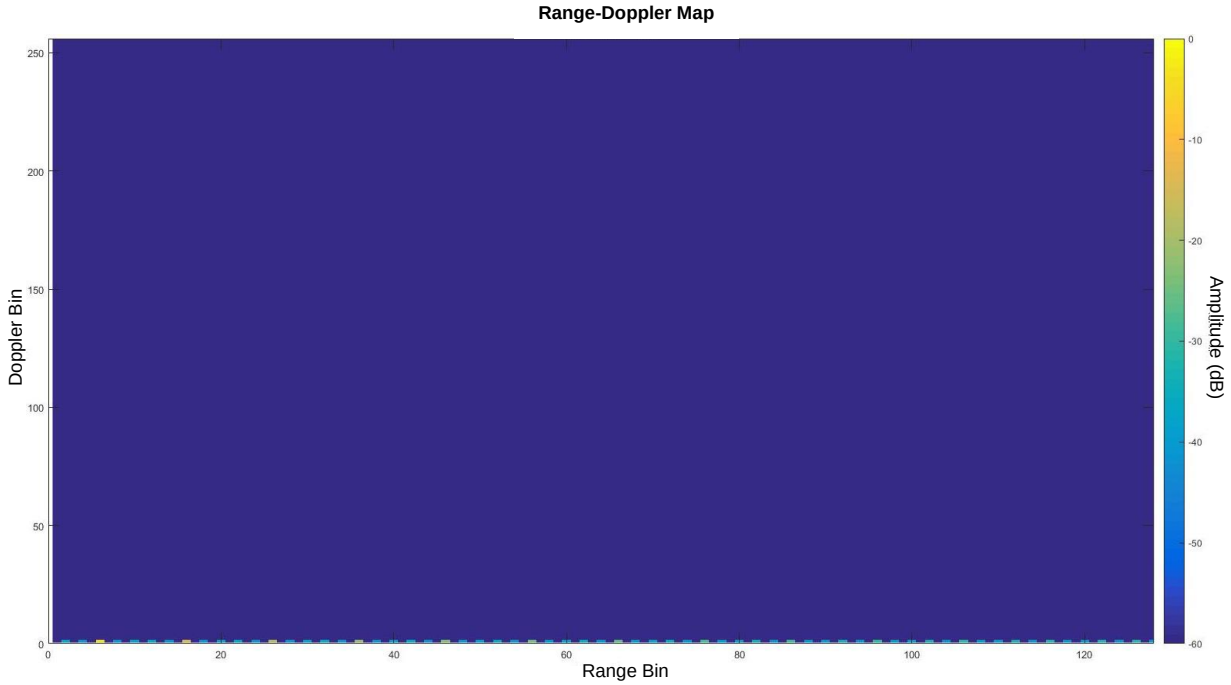

Figure 22: RDM with Investigated signal at 5 times the SRF

Figure 22 shows the RDM with the SMPS frequency (fo) equal to a multiple of the SRF (i.e. 5 x SRF). With a synchronous SMPS frequency, it is clear that after a range and Doppler FFT has been performed, the SMPS frequency and its harmonics are no longer interpreted as moving targets on the RDM. They can be seen at zero-Doppler at various range bins at the bottom of the figure. Since they are at zero-Doppler, it means they will be interpreted as stationary targets, which are filtered out during signal processing, meaning it is not a problem for radar applications.

3.2.3. Synchronising to SRF Conclusion

Section 3.2.1 and 3.2.2 have thus proven that synchronisation of the SMPS frequency to a multiple of the SRF is also an effective SMPS interference mitigation approach.

3.3. Interference mitigation approach evaluation conclusion

The simulations done in this chapter have proven that synchronising to a multiple of the sampling frequency, as well as, to a multiple of the SRF are both effective SMPS interference mitigation approaches. Synchronisation to the SRF still yielded stationary targets at zero-Doppler though, which is not a problem for radar applications (filtered out during signal

processing), but is still undesirable. In order to eliminate this issue and obtain the benefits of both approaches, we must ensure that the SMPS frequency is equal to both a multiple of the sampling frequency and a multiple of the SRF. The results of the implementation of both approaches can be seen in Figure 23.

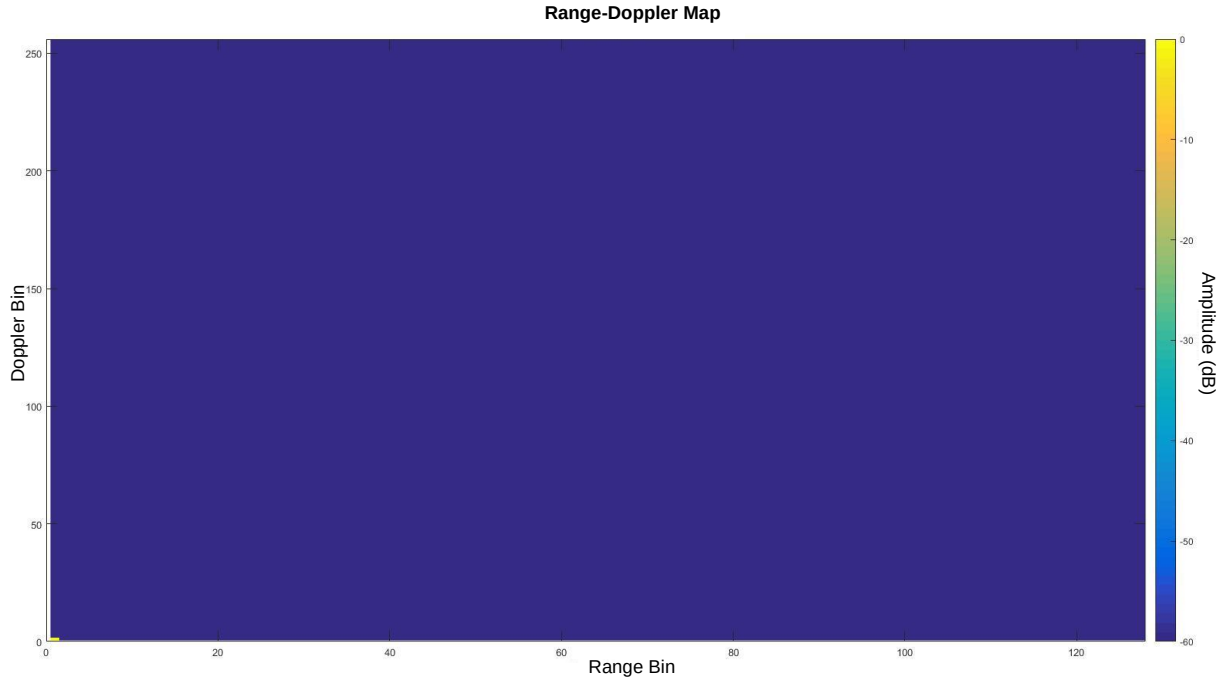

Figure 23: SMPS frequency synchronised to a multiple of the sampling frequency and SRF

The simulation in Figure 23 shows that the implementation of both approaches (synchronising to a multiple of the sampling frequency and SRF) yields no false targets at all. The application of these techniques in a real SMPS should thus provide the required interference mitigation.

Chapter 4
Design Specification

The design specifications of the SMPS PCB, which incorporates the approaches evaluated in Chapter 3 will be outlined in this chapter. The main aspects of the design specification to be discussed include the receiver subsystem integration, SMPS interference mitigation, and military and industry compliance. The operational block diagram of the PCB is shown in Figure 24.

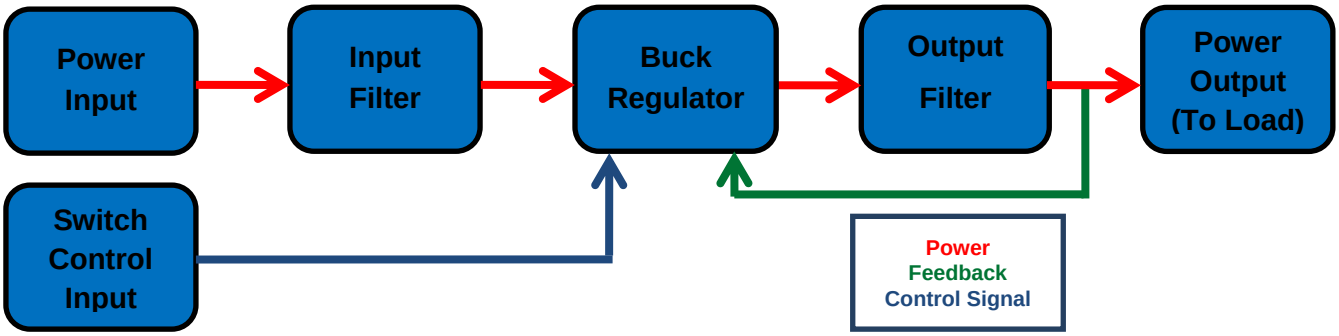

Figure 24: PCB operational block diagram

4.1. Receiver Subsystem Integration

The Radar Power Distribution Unit shall be able to provide 108mA at 12V DC (nominal) to the input of the SMPS PCB. The Radar Power Distribution Unit design is beyond the scope of this study, and thus, only its output (which is fed to the SMPS PCB) is of interest. A power connector interface shall be incorporated on the SMPS PCB to connect to the Radar Power Distribution Unit.

The function of the buck regulator is to step down the input voltage to the required level. The buck regulator shall down-convert the 12V 108mA input to a 5,4V 200mA output (these are at nominal conditions). The output rise time (time to complete the transient phase) shall be less than or equal to 6ms. A feedback mechanism shall be implemented to ensure output regulation. The efficiency of the converter is expected to be better than 90%.

4.2. SMPS Interference mitigation

The function of the input filtration circuitry is to minimise the high frequency noise on the input power lines, which may be from the Radar system power distribution unit or due to noise pick-up during power transmission to the SMPS. Ideally, a common mode filter should be incorporated,

along with a low-pass filter circuit, to ensure that the input power to the SMPS PCB is as clean as possible.

The function of the switch control input is to provide an input clock signal for the buck regulator to synchronise to. This signal shall be sourced either from the Radar receiver subsystem or signal processor, depending on which approach is utilized. A RF SMA Connector interface shall be incorporated on the SMPS PCB to connect to the switch control input. The buck regulator shall be able to synchronise its switching frequency to the switch control input (in order to implement the approaches discussed in Chapter 3).

The function of the output filtration circuitry is to minimise the noise on the output power lines. Ideally, a low-pass filter circuit should be incorporated, to minimise the output voltage ripple and ensure that the output power to the load is as clean as possible.

4.3. Military and Industry Specification Compliance

The Altium Design Rule Check shall be enforced to ensure compliance to military and industry tolerances and clearances etc. (Altium, 2015).

The RRS PCB Pre-Assembly Checklist shall be used to verify that the bare PCB is manufactured and delivered as per the QC (Quality Control) PCB workmanship inspection criteria from IPC-A-600F-Acceptability of Printed Boards Standard and thus also compliant with military and industry specifications. (IPC, 1999).

The RRS PCB Assembly Checklist shall be used to verify that the PCB was assembled according to IPC-J-STD-001E - Requirements for Soldered Electrical and Electronic Assemblies, and hence also compliant with military and industry specifications (IPC, 2014).

The RRS PCB Assembly Final Inspection Checklist shall be used to verify that the PCB workmanship is in compliance with the inspection criteria from IPC-A-600F-Acceptability of Printed Boards Standard, and subsequently with military and industry specifications (IPC, 1999).

The IPC/WHMA-A-620 - Requirements and Acceptance for Cable and Wire Harness Assemblies shall be used to verify that the system integration harnesssing has been done according to IPC, military and industry specifications (IPC, 2002).

Chapter 5
Design Procedure

This Chapter will discuss the PCB schematic design, and simulation, along with detailed component calculations. It will also outline the PCB layout procedure, as well as, the assembly of the PCB and its final inspection.

5.1. Circuit Design and Simulation

This section covers the buck converter selection and PCB schematic design, which includes the component calculations and selection, as well as, the actual schematic design using Altium design software. The simulation of the design, using LTspice is also included in this section. The operational block diagram of the PCB is shown in Figure 25.

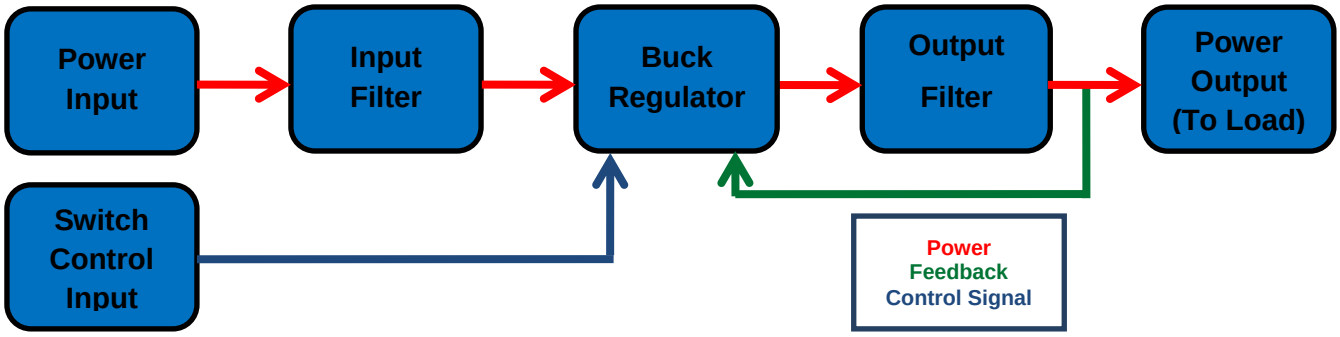

Figure 25: PCB operational block diagram

The requirements for the power input, buck regulator, switch control input and power output are already a specified (in Chapter 4). In this section, the buck converter needs to be selected. The component calculations need to be done specifically for that Buck regulator setup and the input and output filtration mechanisms must be designed. After this the circuit will be simulated to verify correct operation.

5.1.1. Buck Converter Selection

Since it was determined in Chapter 2 that a single stage synchronous buck converter IC package would be best suited for this application, the next step is now to select the best package. As discussed in Chapter 4, the buck regulator shall down-convert the 12V 108mA input to a 5,4V 200mA output. The output rise time (time to complete the transient phase) shall be less than or equal to 6ms. A feedback mechanism shall be implemented to ensure output regulation. The efficiency of the converter is expected to be better than 90%. The buck regulator also needs to be able to synchronise its switching frequency to the switch control input in order to implement the approaches discussed in Chapter 3. The different Buck Converter options are listed and compared in Table 1.

Table 1: Buck Converter Options

Buck Converter Options			
	LM21305	**LTC3601**	**MAX5099**
Cost	R48,40	R35,20	R39,07
Max Input Voltage	18V	15V	19V
Max Output Current	5A	1,5A	2A
Ideal Rise Time	+/-1.5ms	+/- 2.1ms	+/- 1ms
Output Tracking (Feedback)	Yes	Yes	Yes
Efficiency	≈77% (at 200mA Output)	≈90% (at 200mA Output)	≈55% (at 200mA Output)
Ext Clock Synchronization	Yes	Yes	Yes
Short-Circuit Protection	Yes	Yes	Yes
Soft-Start Mechanism	Yes	Yes	Yes
Lead Time	7 Working Days	0 (in RRS stores)	7 Working Days
Narrated from	(Texas Instruments, n.d.)	(Linear Technologies, n.d.)	(Maxim Integrated, n.d.)

From Table 1, we can see that these IC's are all well suited, but we require efficiency equal to or better than a typical off-the-shelf SMPS, which is approximately 90%. Thus, due to its very high efficiency and because it is available in RRS's stores, the LTC3601 has been found to be the best suited package for this application. In the next section, the component calculations will be done for the LTC3601 package (Huffman, n.d.).

5.1.2. Component Calculations

This section covers the component calculations for the LTC3601 buck converter package. Figure 26 shows the provisional schematic design without any component values. This will be the basis for the component calculations.

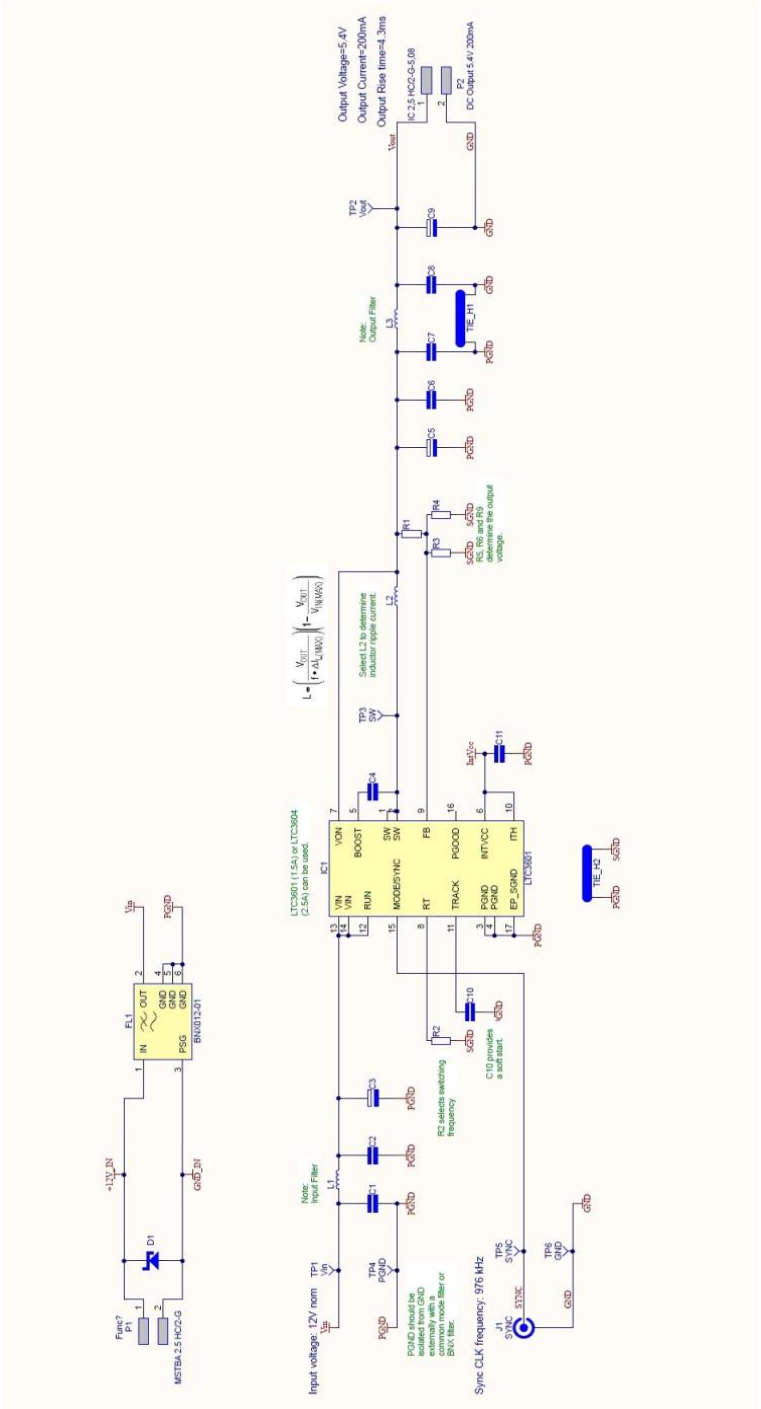

Figure 26: PCB Schematic with no component values

5.1.2.1 Buck Regulator Timing Resistor

The first step is to calculate the Timing resistor value for the intended switch control input frequency. The intention is to synchronise the SMPS to a multiple of the Sampling Frequency (195 kHz), as well as, to a multiple of the SRF (677 Hz). 976 kHz would satisfy both requirements in this case i.e. 5 x fs and 1440 x SRF.

Therefore:

$$R_{RT=}\frac{3.2\times10^{11}}{f_o}=\frac{3.2\times10^{11}}{976kHz}=327.868k\Omega$$ (Linear Technologies, n.d.)

Hence, a 330kΩ resistor is selected.

5.1.2.2 Output Inductor and Output Ripple Current

The next step is to calculate the output inductor ripple current, in order to determine the output inductor value to be used. According to (Linear Technologies, n.d.), to start off with, an acceptable setting for the ripple current is 40% of $I_{out(max)}$.

Therefore:

$$\Delta I_{l(MAX)}=0.4\times I_{OUT(MAX)}=0.4\times1.5A=0.6A$$ (Linear Technologies, n.d.)

With this we may calculate the output Inductor value:

$$L_{=}\left(\frac{V_{OUT}}{f\times\Delta I_{l(MAX)}}\right)\left(1-\frac{V_{OUT}}{V_{IN(MAX)}}\right)=\left(\frac{5.4V}{976kHz\times0.6A}\right)\left(1-\frac{5.4V}{12V}\right)$$ (Linear Technologies, n.d.)

$$=5.07\times10^{-6}H$$

The closest COTS inductor found was a 4.7µH output inductor.

5.1.2.3 C_{IN} Selection

The input capacitance C_{IN} is required to filter the trapezoidal wave current at the drain of the Buck regulator IC top power MOSFET. It is recommended to use low ESR capacitors, rated for the maximum RMS current, to limit voltage transients (Linear Technologies, n.d.).

The maximum RMS current is as follows:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT(V_{IN}-V_{OUT})}}}{V_{IN}} = 200mA \times \frac{\sqrt{5.4(12-5.4)}}{12}$$ (Linear Technologies, n.d.)

$$= 99.499mA$$

This means that a low ESR input capacitor is required with an I_{RMS} rating above 150mA (including 50% safety margin). A 33uF (300mΩ ESR) capacitor with this I_{RMS} rating will thus be suitable. An additional low pass filter will also need to be included in the input filtration mechanism; this will be discussed later in this chapter.

C_{OUT} Selection

The value of the output capacitor is primarily influenced by the ESR required to minimise the output voltage ripple and load step transients. The output voltage ripple is a maximum at V_{INMAX}, since ΔI_L increases with the input voltage (Linear Technologies, n.d.).

It is calculated as follows:

$$\Delta V_{OUT} < \Delta I_L \left(ESR + \frac{1}{8 \times f \times C_{OUT}}\right)$$ (Linear Technologies, n.d.)

Since both ΔV_{OUT} and C_{OUT} are unknown, C_{OUT} must first be selected. In this case C_{OUT} was selected to be a parallel combination of a 33µF (300mΩ ESR) and a 10µF (100mΩ ESR) capacitor.

Thus:

$$\Delta V_{OUT} < 0.6A \left(0.4 + \frac{1}{8 \times 976kHz \times 43\mu F}\right) < 241mV$$ (Linear Technologies, n.d.)

This means, with this setup, $V_{OUT} = 5.4V \pm 120.894mV\ (Worst\ case)$

Since the design specification says that $V_{OUT}\ (shall) = 5.4V \pm 150mV\ (Worst\ case)$, this C_{OUT} is acceptable for the application. An additional low pass filter will also need to be included in the input filtration mechanism; this will be discussed later in this chapter.

Input and Output Low-Pass Filter Design

In order to filter out high frequency signals from the supply (input) and to the load (output), a low pass filter must be added to the input and output of the circuit. Ideally signals above 50kHz should be attenuated.

The formula for the cut-off frequency is as follows:

$$f_C = \frac{1}{2\pi\sqrt{LC}}$$ (Mohan, et al., n.d.)

If L is selected as 1µH, then:

$$C = \frac{\left(\frac{1}{2\pi \times f_C}\right)^2}{L} = \frac{\left(\frac{1}{2\pi \times 50kHz}\right)^2}{1\mu H} = 10.132\mu F \approx 10\mu F$$ (Mohan, et al., n.d.)

The final Low-pass filter design can be seen in Figure 27: Low-Pass Filter DesignFigure 27.

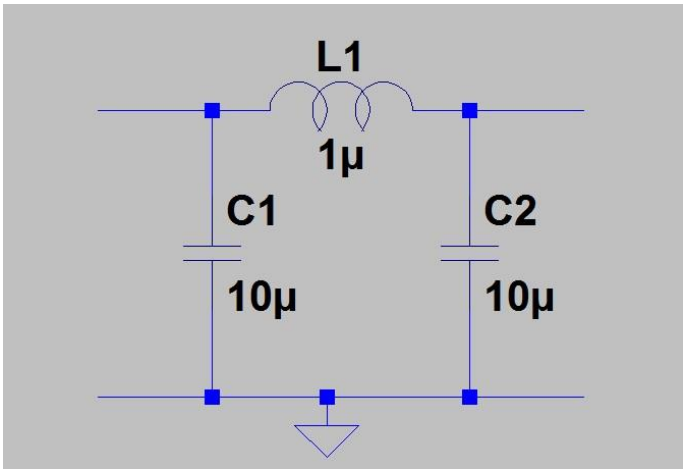

Figure 27: Low-Pass Filter Design

Output Voltage Programming

The required output voltage is set by means of manipulating the Voltage on the Feedback pin of the Buck regulator IC, this is a simple voltage divider mechanism.

According to (Linear Technologies, n.d.) $V_{OUT} = 0.6\left(1 + \frac{R1}{R2}\right)$.

If R1 is selected to be 100kΩ $\quad 5.4V = 0.6\left(1 + \frac{100k\Omega}{R2}\right)$

Therefore:

$$R2 = \left(\frac{100k\Omega}{\frac{5.4}{0.6} - 1}\right) = 12.5k\Omega$$

This can be achieved by using a 15kΩ and 75kΩ resistor in parallel.

Soft Start

The soft start function of the Buck regulator IC, allows for a controlled output voltage ramp rate during start-up. This function ensures that the output current to the load also ramps up in a controlled fashion, thereby preventing damage to the load, due to power surges. By connecting a capacitor to ground from the Track pin, one is able to adjust the rise time (Linear Technologies, n.d.).

The design specification allows for a 6ms rise time, so we will aim for about a 4,3ms rise time in the design.

According to (Linear Technologies, n.d.), $t_{ss} = 430000 \times C_{TRACK}$

For a 4,3ms rise time:

$$C_{TRACK} = \frac{t_{ss}}{430000} = \frac{4.3ms}{430000} = 10nF$$

Therefore a 10nF capacitor shall be utilised.

Boost Capacitor

The boost capacitor is used to generate a rail voltage above the input voltage. It is charged when the bottom power MOSFET is turned on, and is used to supply the transient current needed during the rest of the cycle. A 100nF Capacitor is suitable for most applications (Linear Technologies, n.d.).

Internal V_{CC}

The buck regulator IC produces a 3,3V supply voltage for its internal circuitry. This must be de-coupled to ground via the $INTV_{CC}$ Pin with a minimum of 1uF. For this reason, a 2,2uF Capacitor shall be used (Linear Technologies, n.d.).

Error Amplifier Output and Switching Regulator Compensation (ITH)

External compensation is not required for this application, therefore, this pin will simply be connected to $INTV_{CC}$ in order to utilise the Buck regulator IC's default internal compensation (Linear Technologies, n.d.).

GND Return Path Filtering

In order to assist in the mitigation of $\left(\frac{dI}{d_t}\right)$ transients in the power path, a 33µF capacitor shall be placed across V_{OUT} and GND.

Segregation of the signal ground, power ground and GND return layers

As previously discussed in the PCB Design Considerations section, the Power Ground and Signal Ground, as well as, the Power Ground and GND return nets, will be kept separate and connected to a common, low noise reference point (a Kelvin connection). The aim is to isolate the $\left(\frac{dI}{d_t}\right)$ transients in the power path from the GND return path (Mee & Teune, 2002) (Linear Technologies, n.d.)**.**

5.1.3. Schematic Design (Altium)

Since the component values have now been determined, the next step is doing the schematic design, using the Altium designer software. According to literature (Mee & Teune, 2002) and (Linear Technologies, n.d.), in order to greatly reduce the EMI of a SMPS, one must ensure sufficient input and output filtration, use low ESR capacitors for the filtration, and segregate signal ground, power ground and GND return layers. The application of these techniques will be verified at the end of the schematic design procedure. Figure 28: PCB Schematic DesignFigure 28 and Figure 29 shows the completed schematic design. Due to size and resolution constraints, the design had to be split, in order to clearly view on an A4 document. The merged version can be seen in Appendix B – Complete Schematic Design.

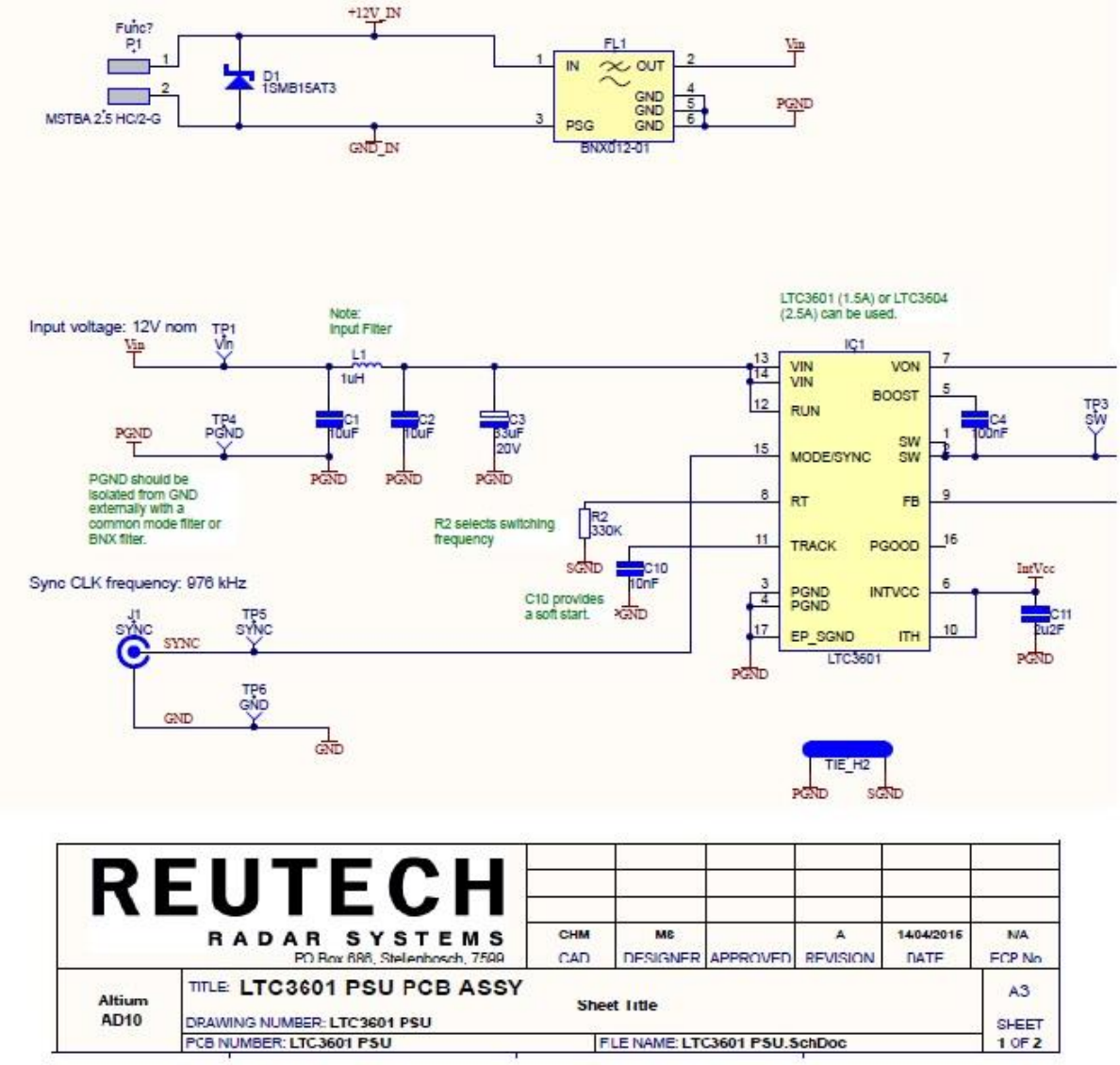

Figure 28: PCB Schematic Design – Left Side

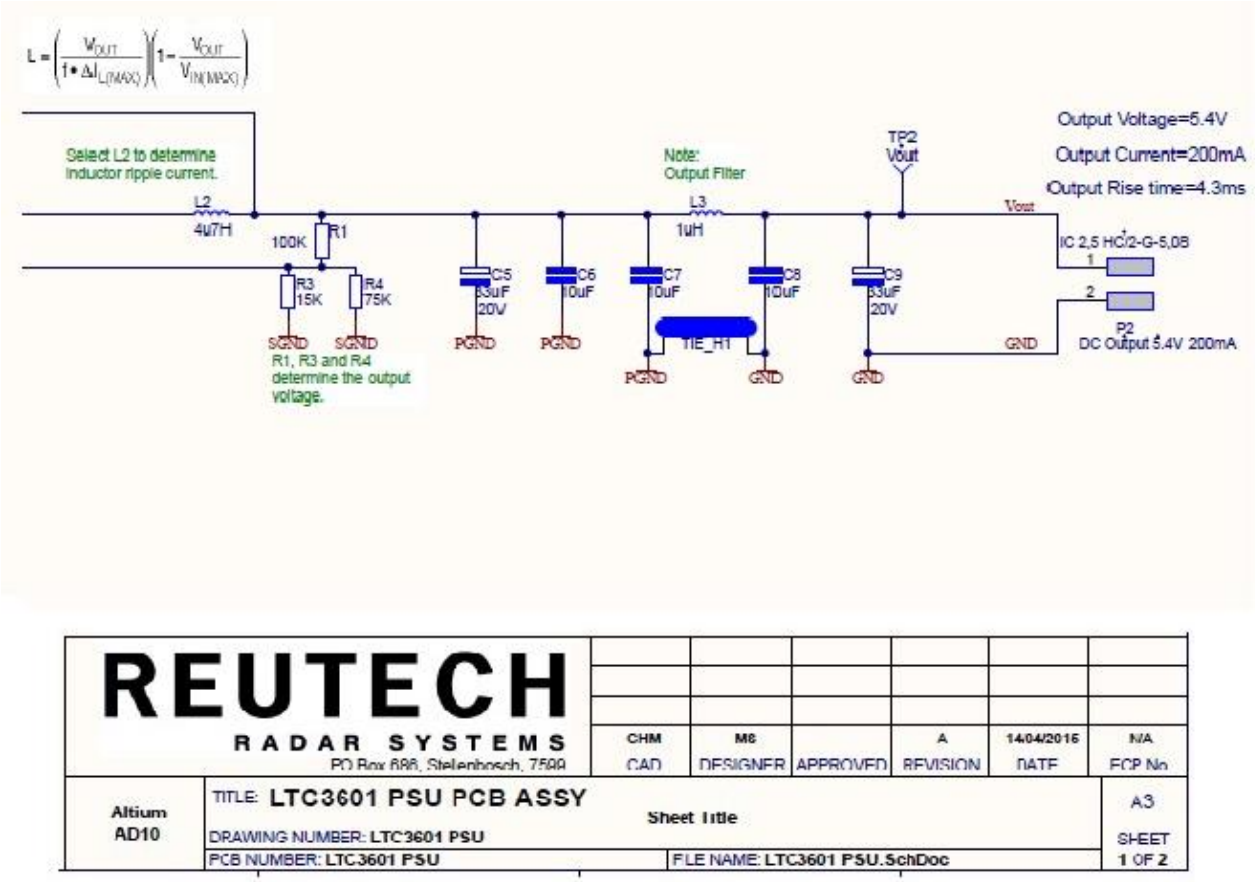

Figure 29: PCB Schematic Design - Right Side

According to literature (Mee & Teune, 2002) and (Linear Technologies, n.d.), the following areas must be given special attention in order to greatly reduce the EMI of a SMPS, they have been tabulated in “checklist” form in Table 2.

Table 2: Schematic Design EMI Mitigation Techniques (Mee & Teune, 2002) and (Linear Technologies, n.d.)

Schematic Design EMI Mitigation Techniques		
No.	**Technique**	**Implementation**
1	Ensure sufficient filtration of the input and output.	Done
2	Use Low ESR capacitors for input and output filtration.	Done
3	Segregate the signal ground, power ground and GND return layers.	Done

According to Table 2, all the techniques have been implemented. Next the circuit design will be simulated using LTspice simulation software.

5.1.4. Schematic simulation

Using LTspice simulation software, it is possible to accurately predict the characteristics of the circuit. This tool will be used to verify that that the circuit performs all the required functions, i.e. produces the correct output voltage and current for the given input. The output rise time and synchronisation to the sync input will also be verified. The simulation schematic can be seen in Figure 30, and the simulation command setup in Figure 31.

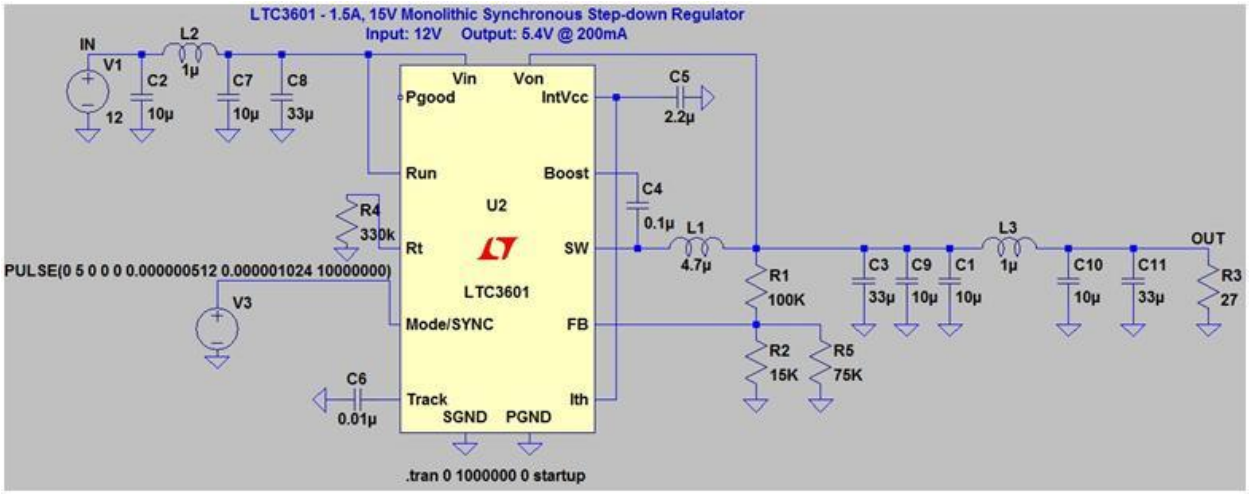

Figure 30: Simulation Schematic

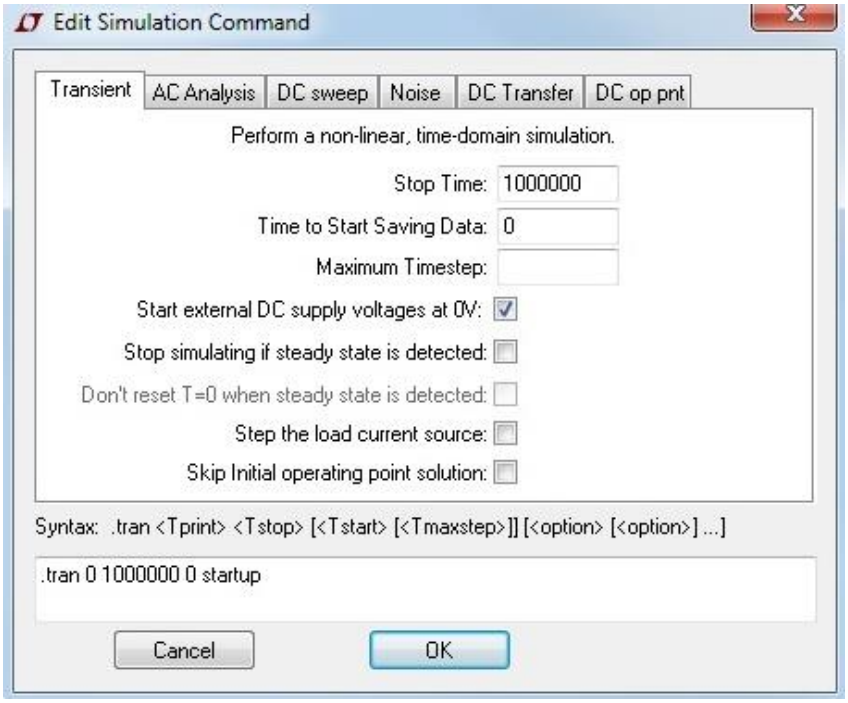

Figure 31: Simulation Command Setup

Upon completion of this setup, the simulation can now be run; the results are shown and discussed in Figure 32, Figure 33, and Figure 34.

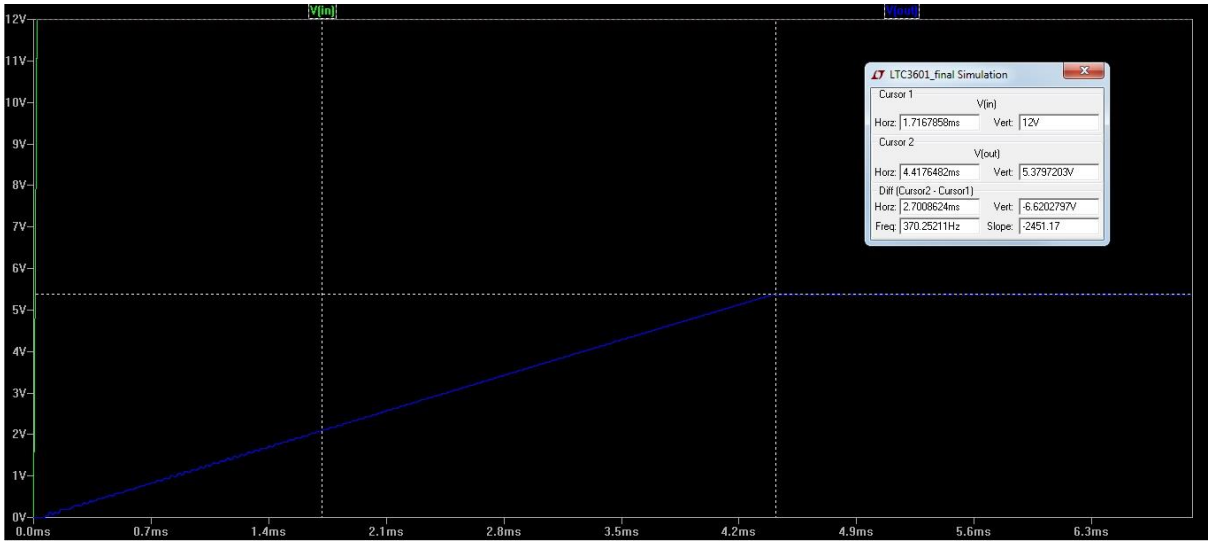

Figure 32: Input Voltage, Output Voltage and Output Rise Time

Figure 32 illustrates that with the simulated input voltage at 12V, the circuit produces an output of 5,38V (target 5,4V), with an output rise time of 4,4ms (target 4,3ms). Therefore, this is a desirable result.

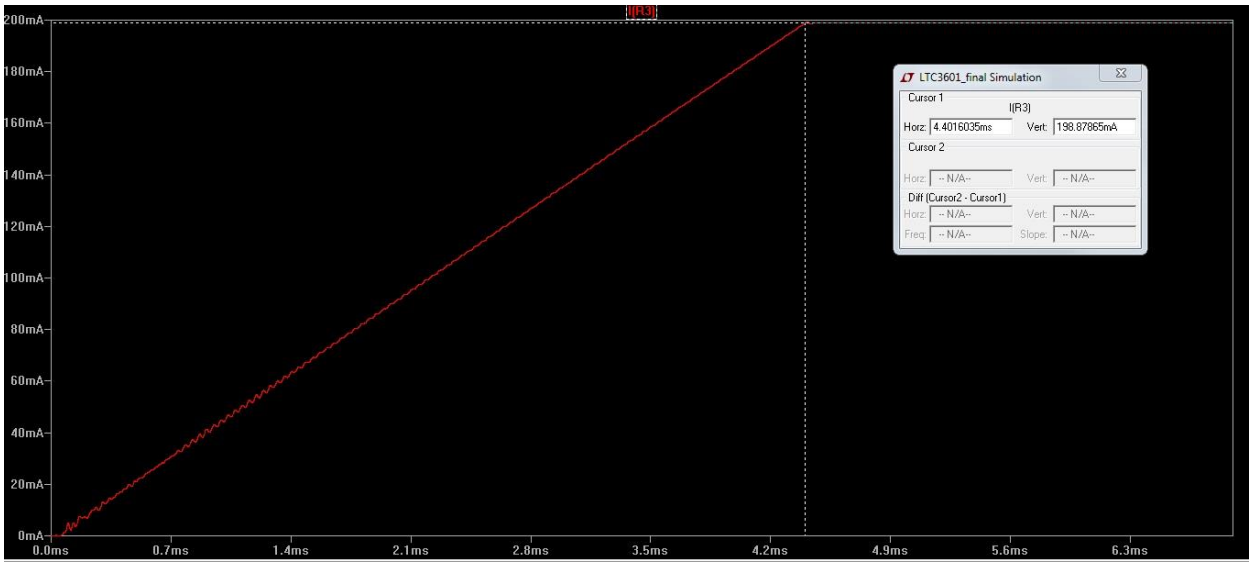

Figure 33: Output Current

Figure 33 shows that the simulated output current is equal to 198.89mA. Since the target output current equal to 200mA, the result is satisfactory for the required application.

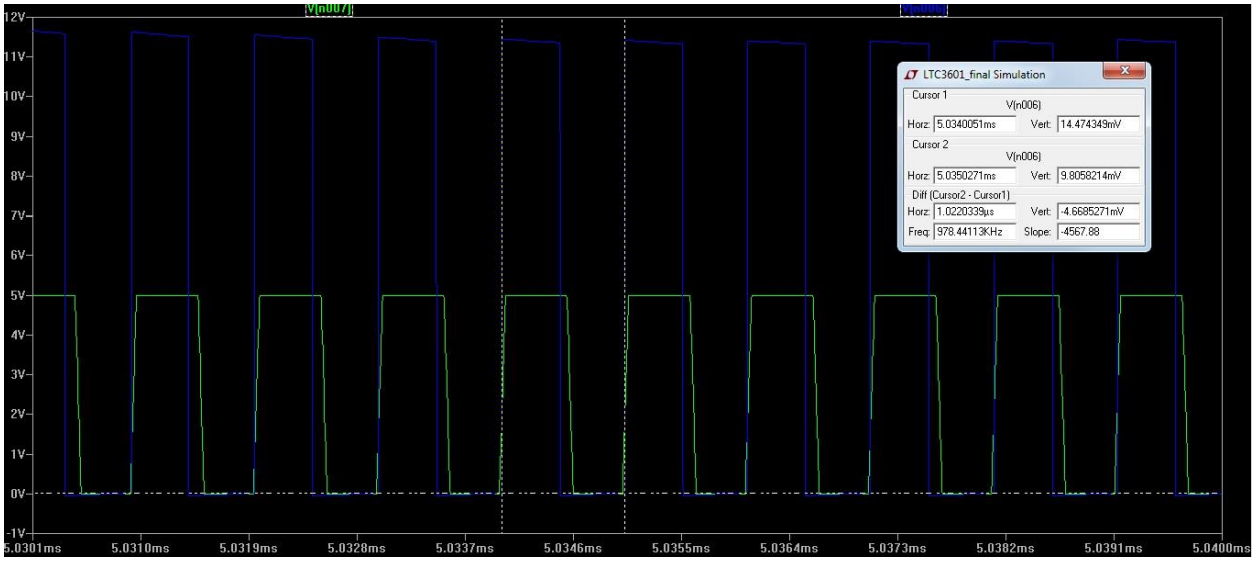

Figure 34: Synchronisation (Sync Input vs Voltage Output)

From Figure 34, it can be seen that the Switching output (Blue) is synchronised to the Synchronisation Input (Green) at a frequency 976KHz.Therefore, this is a desirable result.

5.2. PCB Layout

Doing the PCB layout, using Altium designer software is the next phase of the PCB design. This section documents the PCB layout procedure, including the provisional layout, routing, manufacture, pre-assembly inspection.

5.2.1. PCB Layout (Altium)

Provisional layout

According to literature (Mee & Teune, 2002) and (Linear Technologies, n.d.), in order to greatly reduce the EMI of a SMPS, the loop areas in the PCB layout need to be minimised, the parasitic inductance and capacitance must be reduced by the careful placement of components. Long tracks should be avoided to minimise trace inductance, and the signal ground, power ground and GND return layers must be segregated. The use of ground pours is also highly recommended. The application of these techniques will be verified at the end of the PCB layout design procedure. The provisional layout was completed in Altium designer, see Figure 35 for the 3D model.

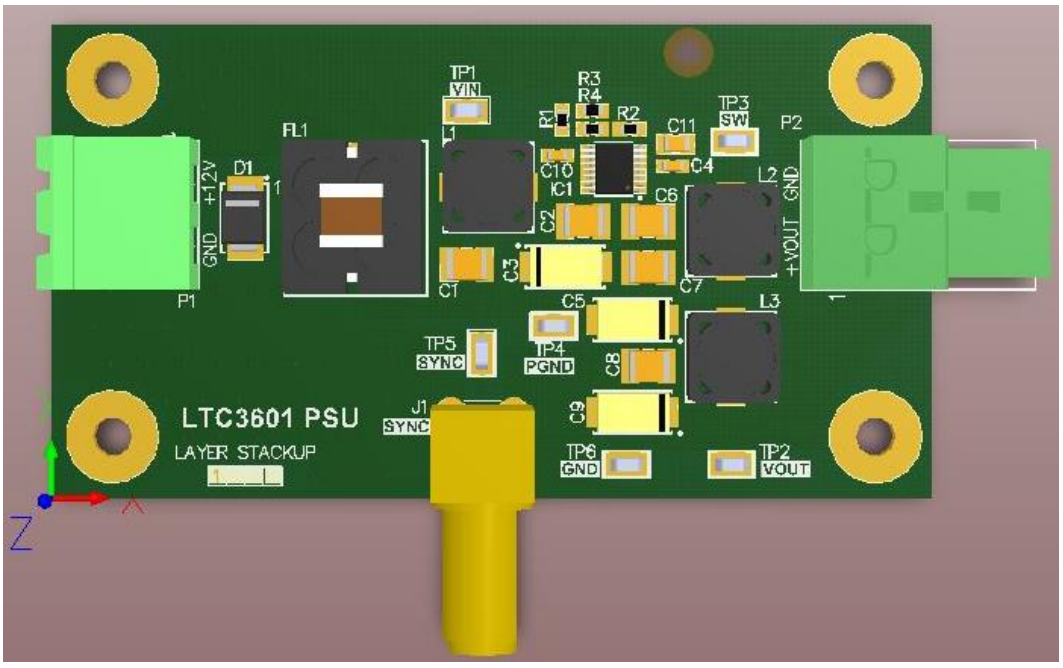

Figure 35: PCB Provisional Layout (3D Model) Top View

Figure 35 shows the provisional PCB layout. In the case where, during routing, it is found that the provisional layout is not ideal, the layout will be changed for ease of routing. In this case, however, the provisional layout remained unchanged.

5.2.2. Routing

The provisional layout of the PCB is then sent to GMOS Interconnect for the routing of the tracks. The four PCB layers can be seen in Figure 36, Figure 37, Figure 38, and Figure 39, respectively.

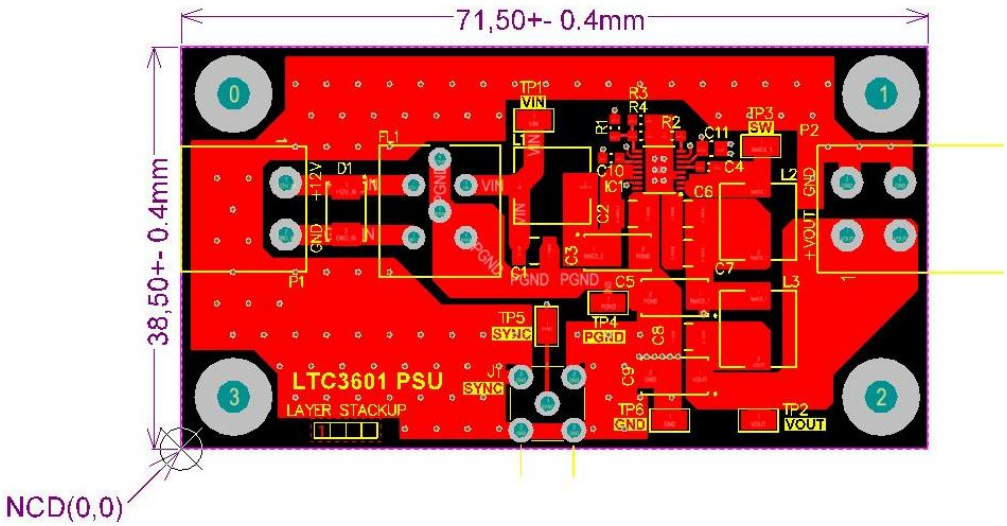

Figure 36: Layer 1-Top Layer

The top layer, seen in Figure 36, is used mainly for routing the input and output power tracks. Additionally, it is also used for routing the power ground or “dirty ground” tracks.

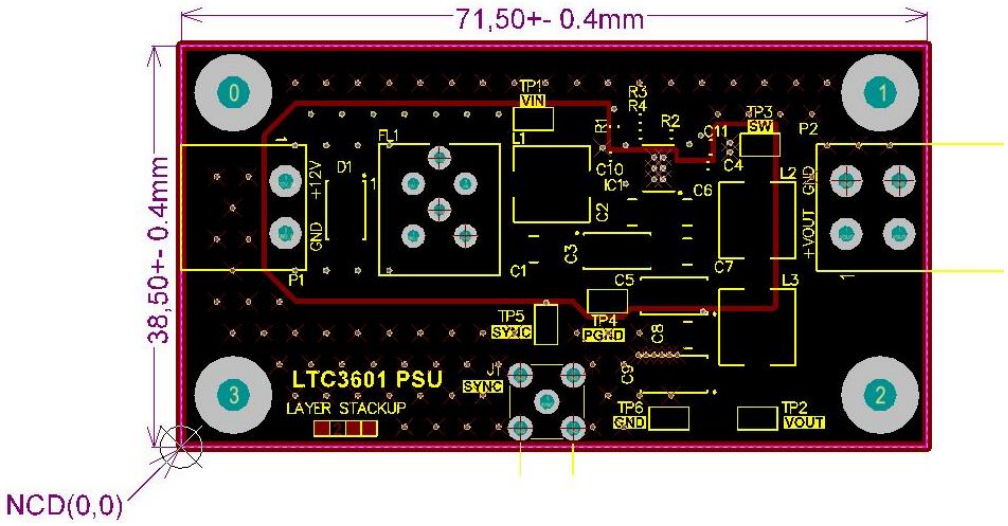

Figure 37: Layer 2-Power GND

The power ground layer seen in Figure 37 is used as ground for all the possible noise inducing areas on the PCB. Some of these include the input power ground, as well as the first stage of

the output filtration, which usually has the most noise. This “dirty ground” layer needs to be separated from the signal ground and GND return (output ground) to avoid interference.

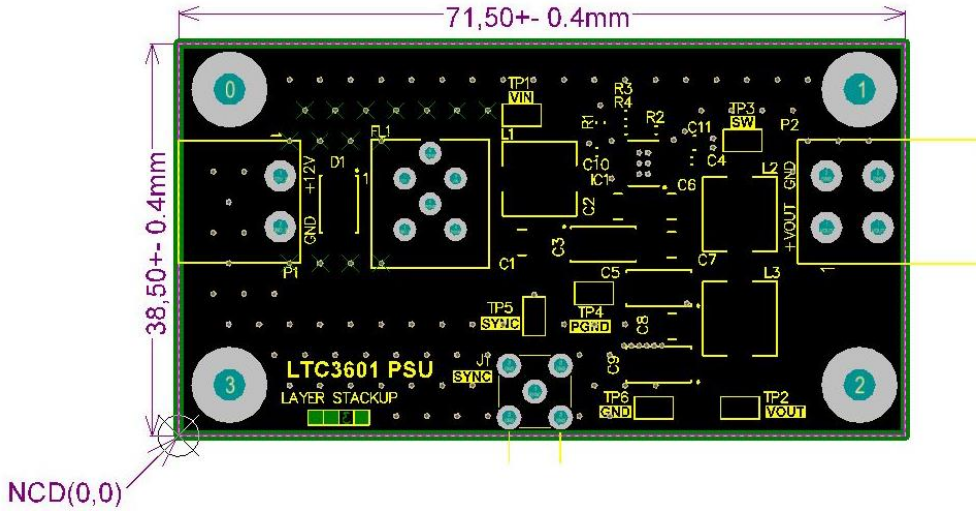

Figure 38: Layer 3-Signal GND

The signal ground layer seen in Figure 38 is used as ground for all the reference signal circuitry, such as the output voltage programming resistors and the switching frequency selection resistor. As this circuitry may be sensitive to noise, the signal ground is only connected to the power ground via a low noise reference point (Kelvin connection), to avoid the high $\left(\frac{dI}{d_t}\right)$ transients in the power path.

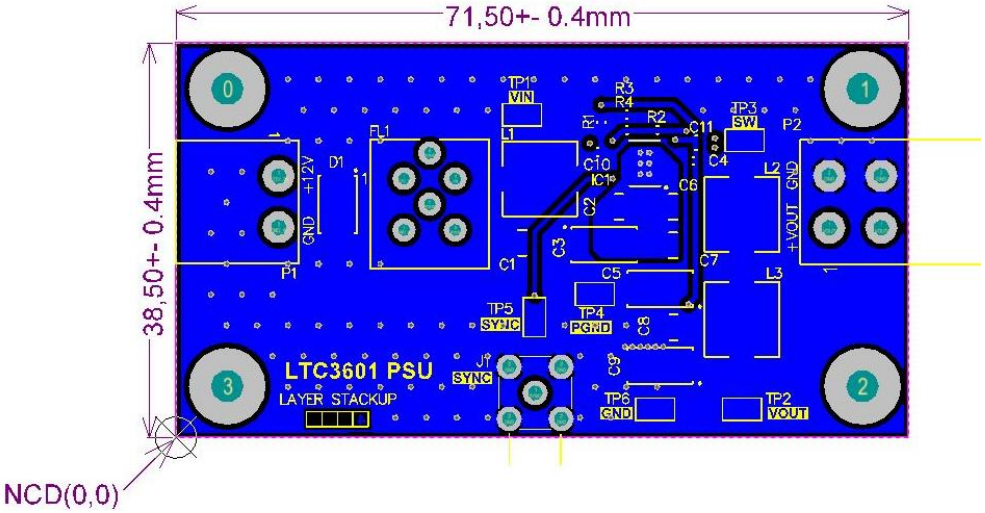

Figure 39: Layer 4-Bottom Layer

The bottom layer, seen in Figure 39, is used for routing the sync clock and all the reference signal circuitry, such as the output voltage programming resistors and the switching frequency selection resistor etc. This is also the “clean” ground to be used for the “clean” GND return path. As with the signal ground, this GND return is only connected to the power ground via a low noise reference point (Kelvin connection), to avoid the high $\left(\frac{dI}{d_t}\right)$ transients in the power path.

Now that the routing is complete, the layout and routing PCB design EMI mitigation techniques application must be verified. The EMI mitigation techniques implementation verification has been tabulated in a “checklist” form in Table 3.

Table 3: PCB Design EMI Mitigation Techniques (Mee & Teune, 2002) and (Linear Technologies, n.d.)

PCB Design EMI Mitigation Techniques		
No.	**Technique**	**Implementation**
1	Minimising loop areas in the PCB layout	Done
2	Reduce the parasitic inductance and capacitance by the careful placement of components	Done
3	Minimise trace inductance (avoid unnecessarily long tracks)	Done
4	Segregate the signal ground, power ground and GND return layers	Done
5	Use ground pours (flood) all unused areas with copper on all the layers	Done

As can be seen in Table 3, all the techniques have been implemented. Upon completion of the routing, the PCB assembly data-pack was compiled and then thoroughly scrutinised in the design reviews. Once the data-pack is approved, it can then be sent for manufacture.

5.2.3. Manufacturing

The data-pack was sent to Trax, who were responsible for manufacturing the PCB. Unfortunately, Trax is only able manufacture a minimum of one sheet, in this case, 8 PCB's could fit on one sheet, and hence a minimum order quantity of 8 PCB's was applied. The total cost for the manufacturing was R5047.40, with a 2 week delivery lead time. The manufactured board can be seen in Figure 40 and Figure 41.

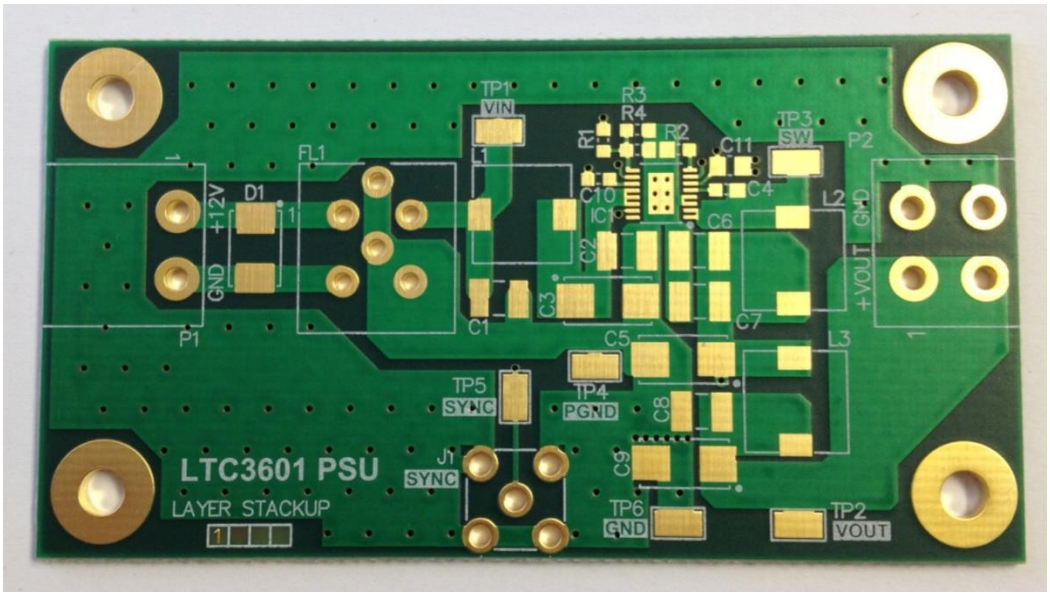

Figure 40: Manufactured (bare) PCB-Top Layer

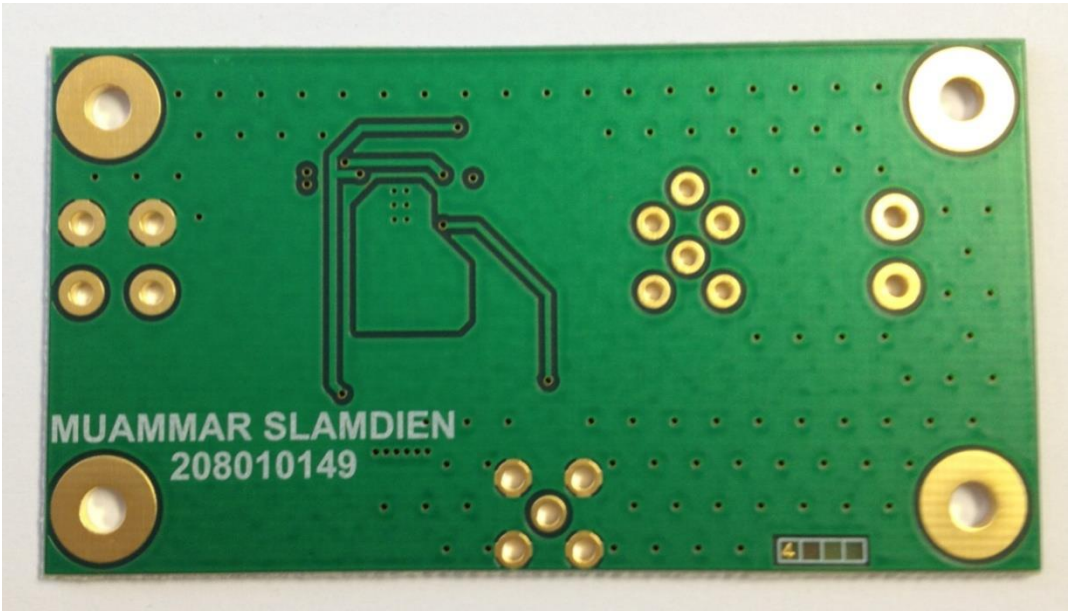

Figure 41: Manufactured (bare) PCB-Bottom Layer

Figure 40 and Figure 41 shows the bare PCB, upon delivery from Trax. Now that the PCB has been received, it must be put through pre-assembly inspection, before the assembly can take place.

5.2.4. Pre-assembly inspection

The bare PCB goes through a pre-assembly inspection to avoid spending many hours on labour to assemble, only to find out that there was an inherent defect with the bare PCB itself. The RRS PCB pre-assembly checklist can be seen in Table 4.

Table 4: RRS PCB Pre-Assembly Checklist (IPC, 1999)

RRS PCB Pre-Assembly Checklist		
No.	**Inspection**	**Compliance**
1	PCB's Supplied in a moisture free sealed package	✓
2	Manufacturers QC Documents supplied with PCB's	✓
3	Inspect (Against cutting and drilling document) PCB size, thickness, bow and twist.	✓
4	Inspect (Against cutting and drilling document) PCB Finish; solder mask, and silkscreen	✓
5	Inspect (Against cutting and drilling document) PCB Plating and etching	✓
6	Inspect (Against cutting and drilling document) PCB Drill hole sizes	✓
7	Confirm correct substrates or material has been used	✓
8	Inspect PCB layer stack-up order	✓
9	Engrave unique serial number on each PCB (for production units)	N/A
10	Check for Shorts	✓

This checklist is as per the QC (Quality Control) PCB workmanship inspection criteria from IPC-A-600F-Acceptability of Printed Boards Standard (IPC, 1999). This standard is internationally recognised, and has comprehensive criteria for producing high quality PCB's. Additionally, it also ensures compliance to military and industry standards (IPC, n.d.). Since all the applicable criteria comply, the PCB can now be assembled.

5.3. PCB Assembly

After the bare PCB is inspected (pre-assembly checklist), the components can then be soldered on to it, this is referred to as the PCB Assembly, and the details of this procedure will be highlighted in this section. The PCB shall be assembled according to the standard IPC-J-STD-001E - Requirements for Soldered Electrical and Electronic Assemblies (IPC, 2014). The PCB assembly drawing can be seen in Figure 42.

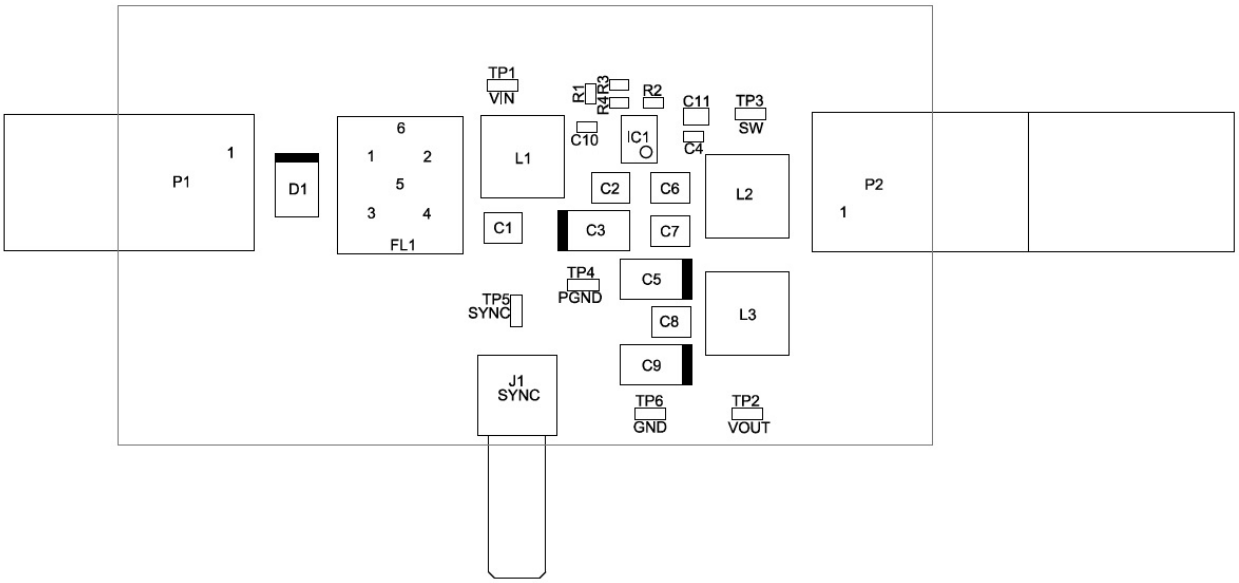

Figure 42: PCB Assembly Drawing

The PCB was assembled according to the standard IPC-J-STD-001E - Requirements for Soldered Electrical and Electronic Assemblies (IPC, 2014). This standard describes, in detail, the techniques and verification criteria for producing high quality interconnections, and has become the premier authority for electronics assembly around the globe. Following this standard also ensures compliance to Military and Industry standards, by default (IPC, n.d.). The final PCB Assembly can be seen in Figure 43.

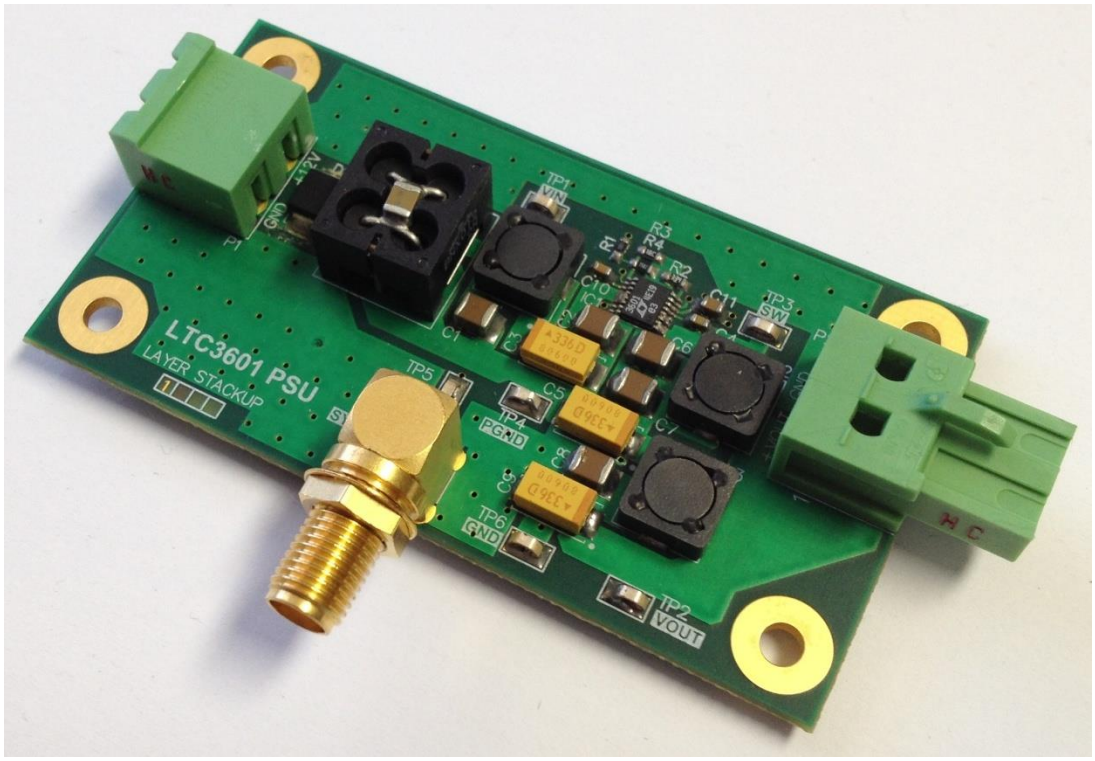

Figure 43: Final PCB Assembly

Figure 43 shows the completed PCB assembly, with all the components and interfaces populated. Next, it must be verified that the PCB was assembled according to the standard IPC-J-STD-001E - Requirements for Soldered Electrical and Electronic Assemblies (IPC, 2014).The RRS PCB Assembly Checklist can be seen in Table 5.

Table 5: RRS PCB Assembly Checklist

RRS PCB Assembly Checklist		
No.	**Inspection**	**Compliance**
1	PCB assembled according to IPC-J-STD-001E - Requirements for Soldered Electrical and Electronic Assemblies (IPC, 2014)	✓

As can be seen in Table 5, the PCB assembly process has complied with the requirements on the RRS PCB assembly checklist. Now that the assembly has been completed, and it has passed the RRS PCB assembly checklist, the PCB can go for Final Inspection.

5.4. PCB Assembly Final Inspection

After assembly, the PCB goes though a final inspection (based on the standard IPC-A-600F-Acceptability of Printed Boards) before the testing/evaluation can commence. The final inspection checklist can be seen in Table 6 (IPC, 1999).

Table 6: RRS PCB Assembly Final Inspection Checklist

RRS PCB Assembly Final Inspection Checklist		
No.	**Inspection**	**Compliance**
1	PCB Assembly complies with PCB Drawing	✓
2	PCB Assembly complies with PCB Parts List	✓

This checklist is as per the QC PCB workmanship inspection criteria from IPC-A-600F-Acceptability of Printed Boards Standard (IPC, 1999). Since all the criteria comply, the PCB can now be evaluated. The evaluation procedure is documented in Chapter 6.

Chapter 6
Experimental Evaluation

In this chapter, the answers to the research questions will be stated (whether or not the goals have been achieved and why). As aforementioned in Chapter 1, the research questions are as follows:

- Can the unit be effectively integrated with the receiver subsystem?
    - The unit must provide the required voltage and load current for the receiver subsystem.
    - The efficiency of unit must be equal to or better than a typical off-the-shelf SMPS.

- Can a DC power supply PCB be developed which mitigates the effects of the switch-mode power supplies?
    - The PCB must be able to greatly reduce the SMPS EMI, by producing a clean, synchronous output.
    - The PCB must be able to minimize the processed Radar data distortion, due to the SMPS switching frequency and its harmonics, when viewed by Real-Time Spectrum Analysis
    - The PCB must be able to eliminate “false targets” on the RDM caused by the SMPS frequency

- Can the PCB be designed to comply with the military and industry specifications?
    - The PCB must be designed according to Military Specifications.
    - The PCB must be designed according to Industry Specifications.

Things such as the purpose of the experiment, experiment setup and procedures will be indicated in this chapter. Finally, a summarised version of the results and observations will be provided for each section.

6.1. Receiver subsystem integration evaluation

The purpose of this experiment is to evaluate whether the PSU PCB can be effectively be integrated with the receiver subsystem. The output voltage and current will be tested, along with the efficiency of the unit. The setup block diagram and picture can be seen in Figure 44 and Figure 45 respectively.

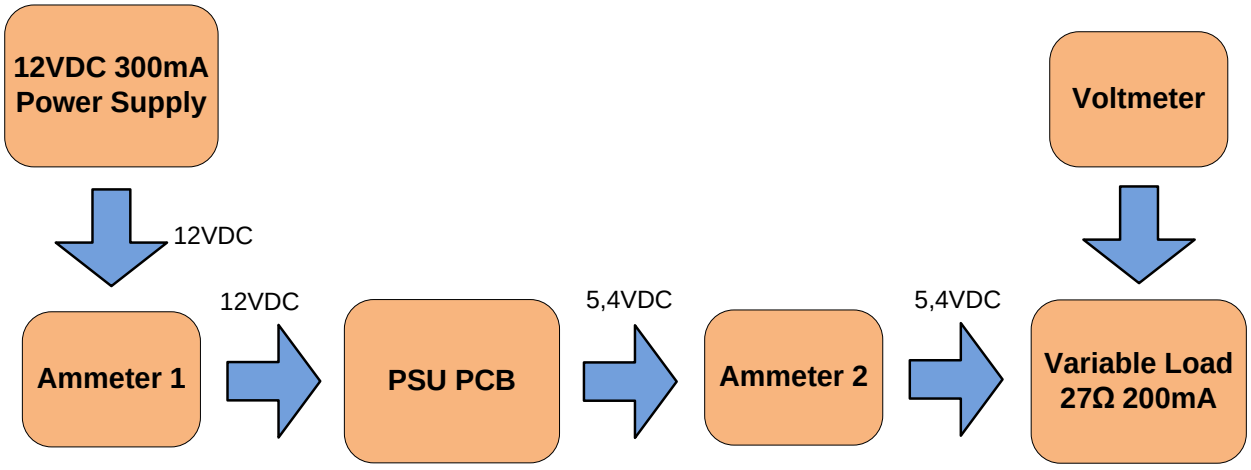

Figure 44: Receiver subsystem integration Test setup block diagram

Figure 44 shows the receiver subsystem integration test setup in a block diagram form. This block diagram can be used to replicate the test setup if need be. Figure 45 shows the receiver integration evaluation setup.

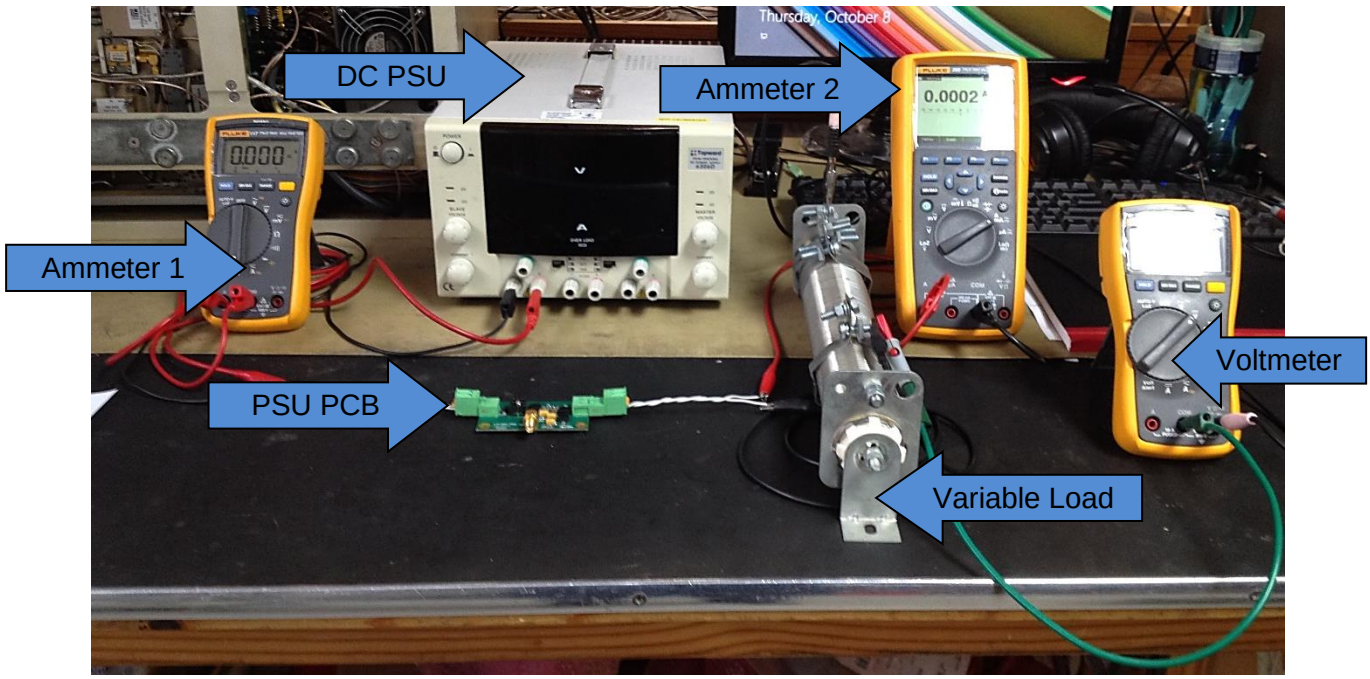

Figure 45: Receiver integration evaluation setup

The receiver integration evaluation setup shown in Figure 45 is essentially a graphical illustration of the block diagram in Figure 44. This will also aid in replicating the test setup.

6.1.1. Procedure

1) Set the DC Power supply to 12V and current limit at 300mA
2) Connect the test setup as illustrated in Figure 44 and Figure 45.
3) Adjust the Variable Load to 27Ω
4) Switch on the DC Power supply.
5) Measure the output current using Ammeter 2 (Adjust Variable load until 200mA)
6) Measure the output voltage using Voltmeter 1
7) Measure the input current using Ammeter 1
8) Tabulate results

6.1.2. Results

Table 7 illustrates the test results for the Receiver Subsystem Integration Evaluation; in other words, it shows the voltage, current, power and efficiency measurements taken.

Table 7: Receiver Subsystem Integration Evaluation

Receiver subsystem integration evaluation			
	Requirement	**Measured**	**Compliance**
Vin	12V ± 0.1V	12.04V	✓
Iin	≤ 108mA	95mA	✓
Vout	5.4V ± 0.1V	5.44V	✓
Iout	200mA ± 10mA	194.2mA	✓
Output Rise Time	≤ 6ms	4.4ms	✓
Pin	≤ 1.283W	1.144W	✓
Pout	≤ 1.155W	1.056W	✓
η (Efficiency)	≥90%	92.31%	✓

From Table 7 it is clear that the PSU PCB complies fully with the voltage, current, and efficiency requirements specified in Chapter 4 for the Receiver Subsystem Integration phase.

6.1.3. Conclusion

Since the PSU PCB was found to be in full compliance with voltage, current, and efficiency requirements for the Receiver Subsystem Integration, it was then integrated with the Receiver Subsystem. Pictures of the integrated unit can be seen in Figure 47 and Figure 48 in the next section, where the interference mitigation capabilities will be evaluated.

6.2. Interference mitigation evaluation

The purpose of this experiment is to evaluate whether the PSU PCB can mitigate the effects of the switch-mode power supplies by greatly reducing the SMPS EMI, by producing a clean, synchronous output., as well as, by minimising Radar data distortion, due to the SMPS switching frequency and its harmonics and by eliminating subsequent “false targets” on the RDM. The integrated receiver subsystem setup block diagram and pictures can be seen in Figure 46, Figure 47 and Figure 48 respectively.

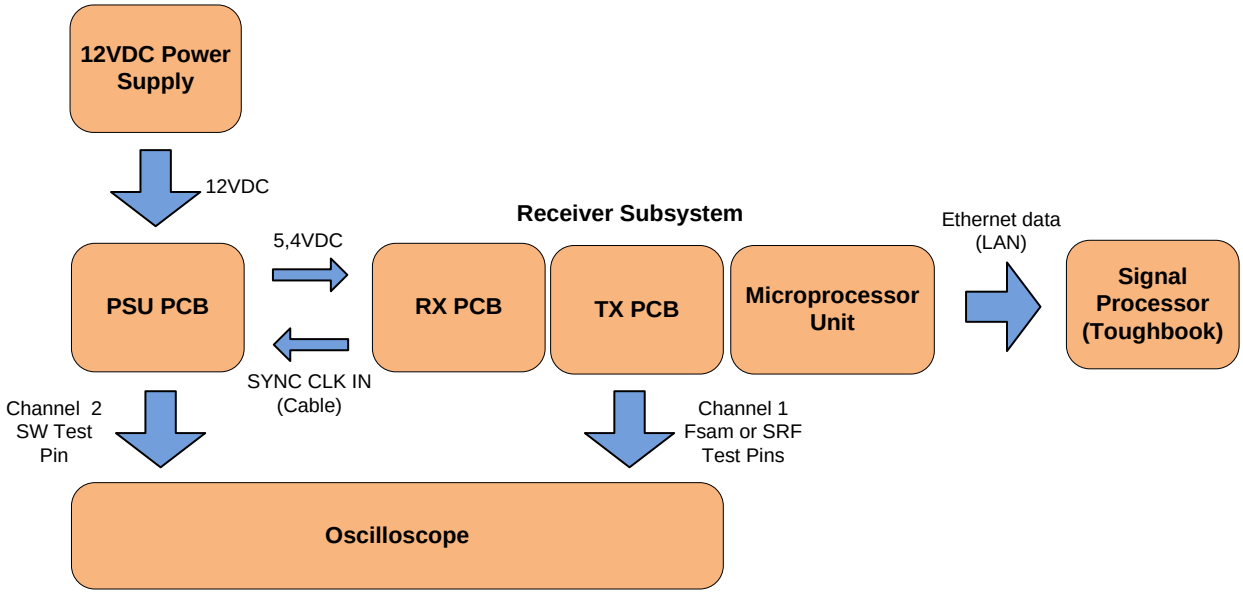

Figure 46: Interference mitigation Test setup block diagram

Figure 46 shows the Interference mitigation test setup in a block diagram form. This block diagram can be used to replicate the test setup if need be. Figure 47 shows the integrated receiver subsystem for Interference mitigation evaluation setup.

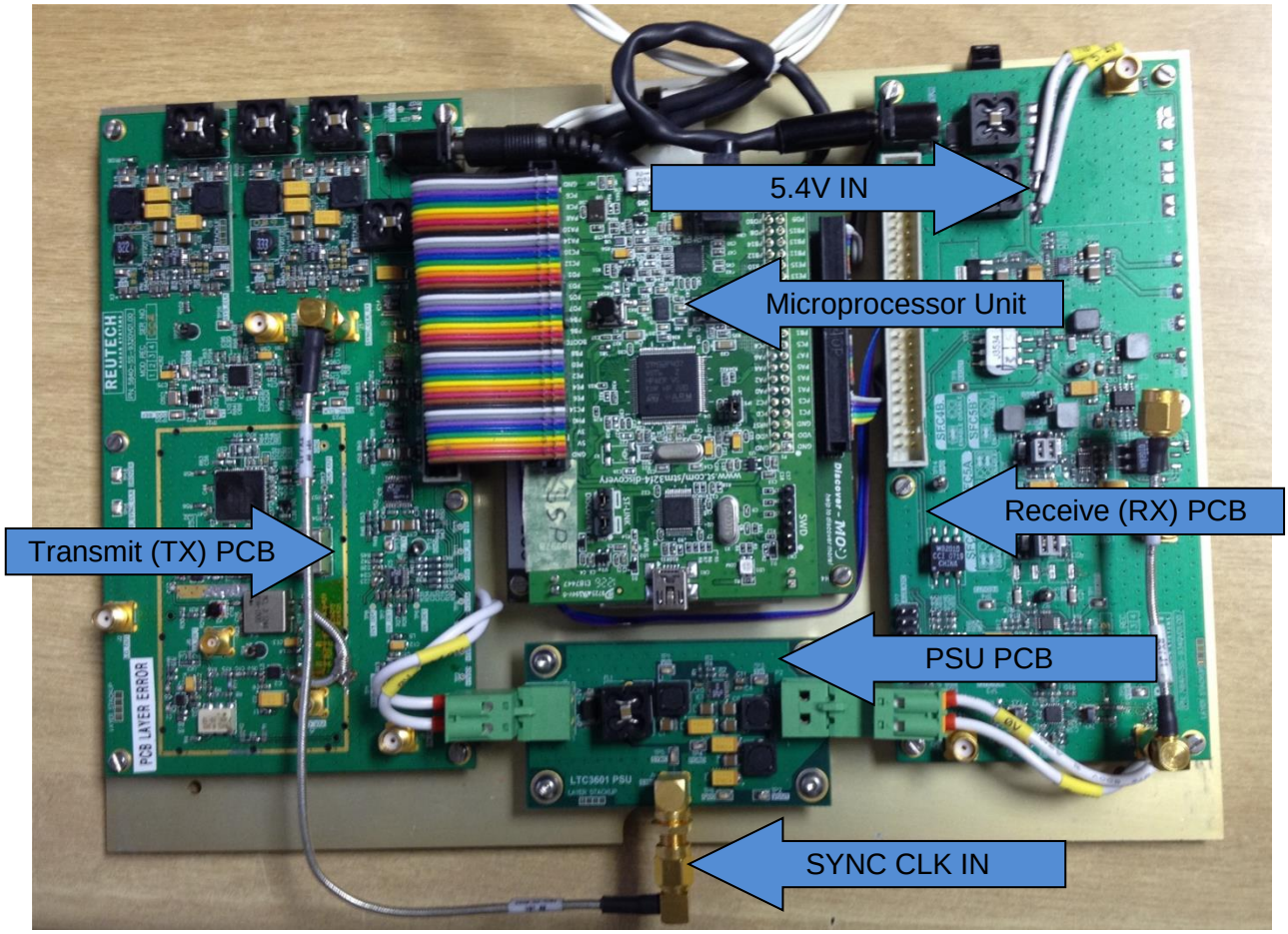

Figure 47: Integrated receiver subsystem for Interference mitigation evaluation setup

The receiver subsystem is shown in Figure 47, with the PSU PCB integrated. The purpose of the integration is for evaluating the interference mitigation techniques implemented in the PCB design.

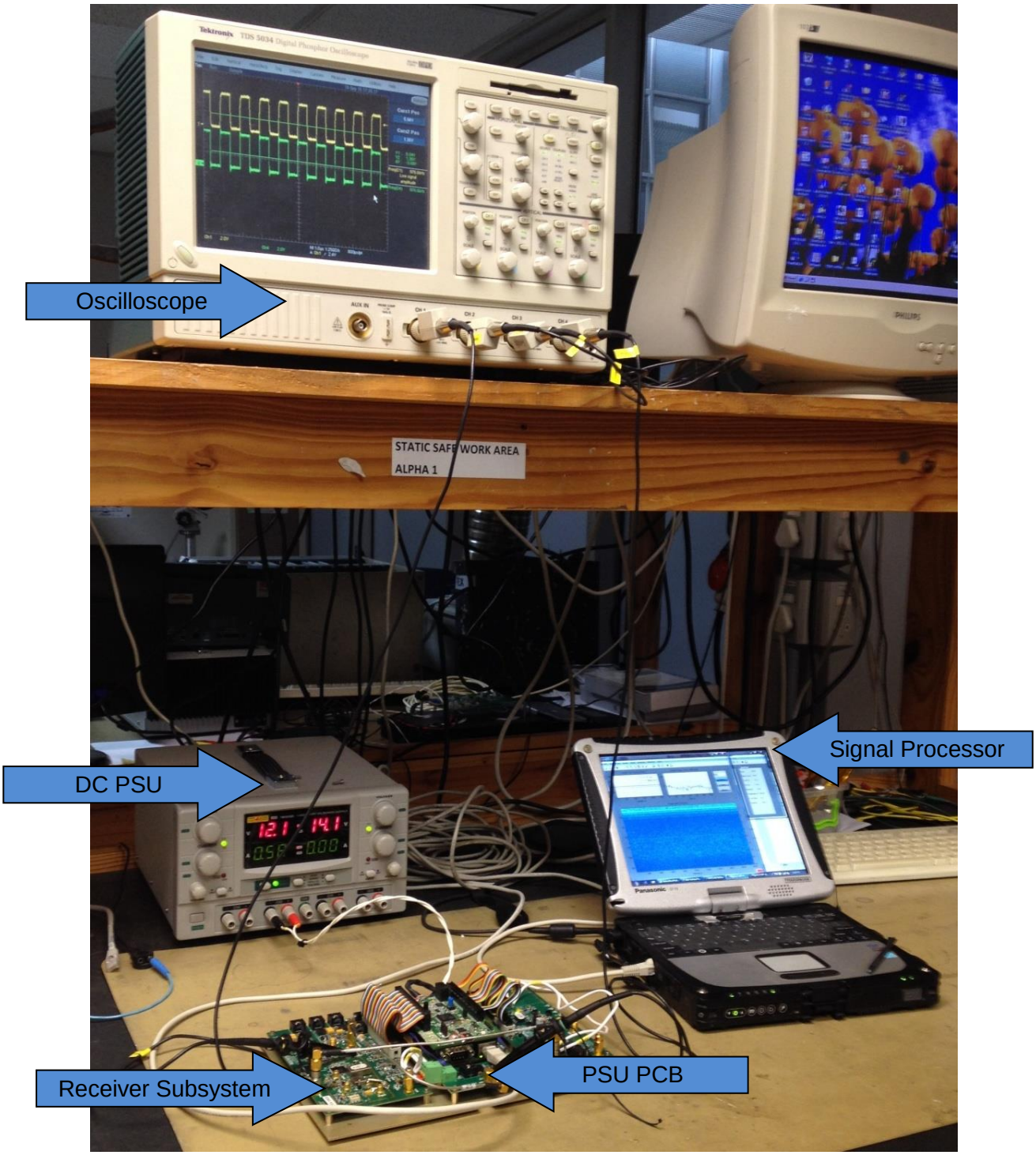

Figure 48: Interference mitigation evaluation setup

Figure 48 is essentially a graphical illustration of the block diagram in Figure 46. Once again, this illustration will aid in replicating the test setup if it becomes necessary.

6.2.1. Synchronisation to Sample Frequency and SRF Evaluation Procedure and Results

The purpose of this experiment is to determine if the PCB is able to greatly reduce the SMPS EMI, by producing a clean output which is synchronised to both the sample frequency and SRF.

Synchronisation evaluation procedure

1) Connect the setup as shown in Figure 46, Figure 47 and Figure 48 (without connecting the SYNC CLK IN cable)
2) Connect Channel 1 probe of the oscilloscope to the F_{SAM} test pin (for the sample frequency) on the T_X PCB
3) Connect Channel 2 probe of the oscilloscope to the SW test pin on the PSU PCB
4) Connect the 12V DC from the DC bench power supply
5) Adjust the oscilloscope scaling to an appropriate scale
6) Compare the signals and take a screenshot
7) Connect the SYNC CLK IN cable
8) Compare the signals and take a screenshot
9) Move Channel 1 probe of the oscilloscope to the SRF test pin (for the SRF) on the T_X PCB
10) Adjust the oscilloscope scaling to an appropriate scale
11) Compare the signals and take screenshots

Synchronisation evaluation results

Figure 49 illustrates the PSU PCB output voltage, while it is Asynchronous to the sample frequency (meaning that there is no SYNC CLK signal connected to the PCB).

Figure 49: PSU PCB output Asynchronous to sample frequency (No SYNC CLK)

It is clear in Figure 49, that the PSU PCB's output is Asynchronous to sample frequency. This is due to the SYNC CLK input is not being connected and the PCB is therefore going into "burst-mode". Initially, the PCB still remained semi-synchronous, even when no SYNC CLK input was connected, this is due to the Timing resistor (R_{RT}) being set to 330kΩ, which defaults the switching frequency to 976kHz (the same as the SYNC CLK frequency), with no SYNC CLK Input. For the purpose of demonstration, we would like the PCB to be asynchronous, with no SYNC CLK Input. For this reason R_{RT} was changed to a 390kΩ, which results in an Asynchronous 820,5kHz and forces the PCB into "burst-mode". Next, the SYNC CLK is connected and the PSU PCB's output Synchronises to the sample frequency, this is shown in Figure 50.

Figure 50: PSU PCB output Synchronous to sample frequency (SYNC CLK connected)

In Figure 50, the output of the PSU PCB has synchronised to the sample frequency, with the SYNC CLK input being reconnected. The output frequency of the PSU PCB is 976kHz, 5 times the sample frequency of 195kHz, this means it is a multiple of the sampling frequency, which is compliant to the approach discussed in section 3.1. Next, the PSU PCB's output is compared to the SRF in Figure 51 and Figure 52.

Figure 51: PSU PCB output Synchronous to SRF View 1

The PSU PCB output is shown to be synchronised to the SRF in Figure 51. The time scale was then adjusted, for a better view of the switching frequency; this is shown in Figure 52.

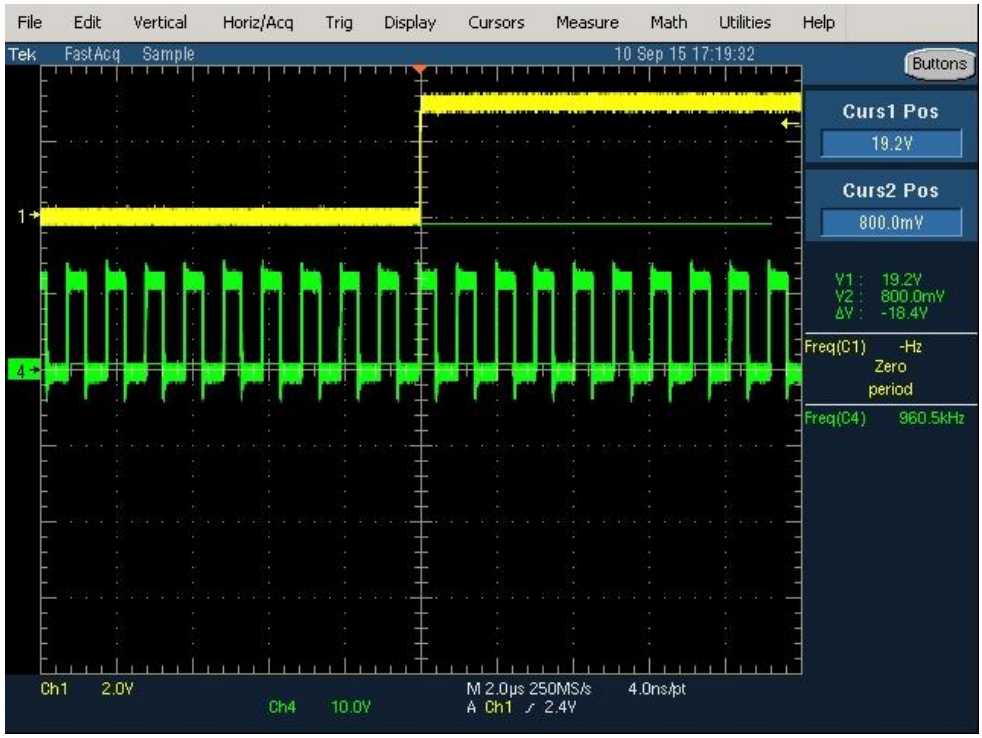

Figure 52: PSU PCB output Synchronous to SRF View 2

Figure 51 and Figure 52 shows the PSU PCB's output Synchronous to the SRF. Unfortunately due to the large frequency delta, 2 screenshots were required to show synchronism. The output frequency of the PSU PCB remains at 976 kHz, 1440 times the SRF of 677 Hz; this means it is a multiple of the SRF, which is compliant to the approach discussed in section 3.2.

Synchronisation evaluation conclusion

Since the output of the PSU PCB was found to be clean, and because it was able to synchronise to both the sample frequency and the SRF, it can be concluded that the PSU PCB is able to greatly reduce the SMPS EMI, by producing a clean, synchronous output and that the synchronisation evaluation was thus successful. The Radar Data evaluation and results follow in the section.

6.2.2. Real-Time Spectrum Analysis Evaluation Procedure and Results

The purpose of this experiment is to evaluate if the PCB is able to minimize the processed Radar data distortion, due to the SMPS switching frequency and its harmonics. The processed Radar data will be viewed by means of Real-Time Spectrum Analysis (RTSA).

Real-Time Spectrum Analysis evaluation procedure

1) Connect the setup as shown in Figure 46, Figure 47 and Figure 48
2) Connect the 12V DC from the DC bench power supply
3) Connect the LAN cable from the Receiver subsystem to the signal processor (Tough book)
4) Setup the IP address on the Tough book
5) Launch the Radar HMI
6) Command the HMI to stream data
7) Run the Radar Matlab script to view processed Radar data in RTSA mode

Note: Some steps have purposefully been left out of this procedure, due to company confidentiality.

Real-Time Spectrum Analysis evaluation results

Figure 53 shows a processed Radar data set with the PSU PCB synchronous and asynchronous, viewed in RTSA mode. Real-Time Spectrum Analysis (RTSA) essentially takes the raw radar data (in the time-domain) and transforms it into the frequency domain by applying an FFT algorithm. In this case, a horizontal Range FFT has been applied, producing the Range Bin vs. Sweep Graphs seen in Figure 53, Figure 54, and Figure 55 (Tektronix, 2009).

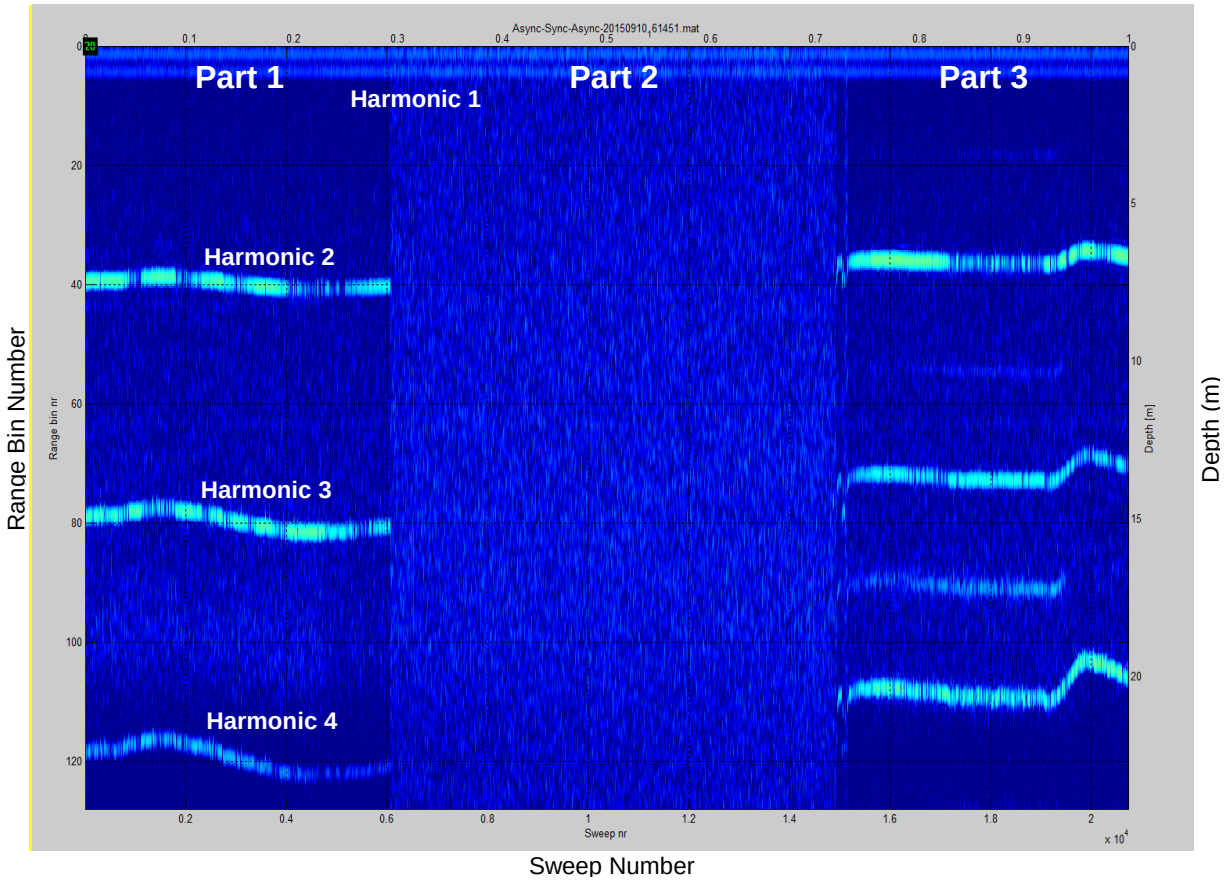

Figure 53: RTSA of Radar Data – PSU PCB Asynchronous and Synchronous combined

In Figure 53, for part 1 of the data set, the SYNC CLK has been removed and the PSU PCB's output is not synchronised. For this reason, we can see distorted radar data coming through, because of the SMPS output frequency and its harmonics.

For part 2 of the data set, the SYNC CLK has been connected and the PSU PCB's output is now synchronised. For this reason, we can see that all the distorted radar data has now stopped coming through. This part clearly illustrates the exploitation of the Nyquist frequency (Synchronising to the sample frequency investigated in section 3.1). We can see that when the PCB is synchronised, the SMPS frequency and its harmonics aliases to 0Hz (Range Bin 0). Since there is no target (large peak or defiant bands) being sensed by the Radar, this then increases the radar sensitivity, which enhances ambient noise, hence giving the appearance of more noise over the full spectrum.

For part 3 of the data set, the SYNC CLK has again been removed and the PSU PCB's output is not synchronised once again. For this reason, the distorted radar data returns, because of the

SMPS output frequency and its harmonics. Figure 54 illustrates a processed radar data set which contains only asynchronous data.

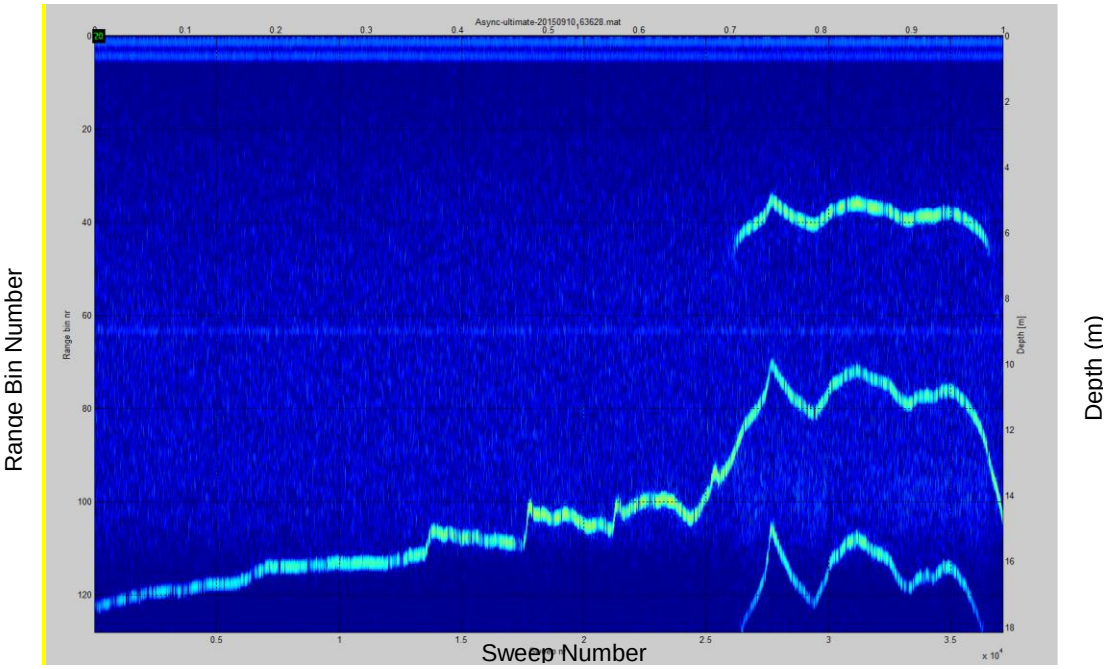

Figure 54: RTSA of Radar Data – PSU PCB Asynchronous

In Figure 54, we see a real-time spectrum analysis view of the radar data, with the PSU PCB asynchronous. Figure 55 illustrates a processed radar data set which contains only synchronous data.

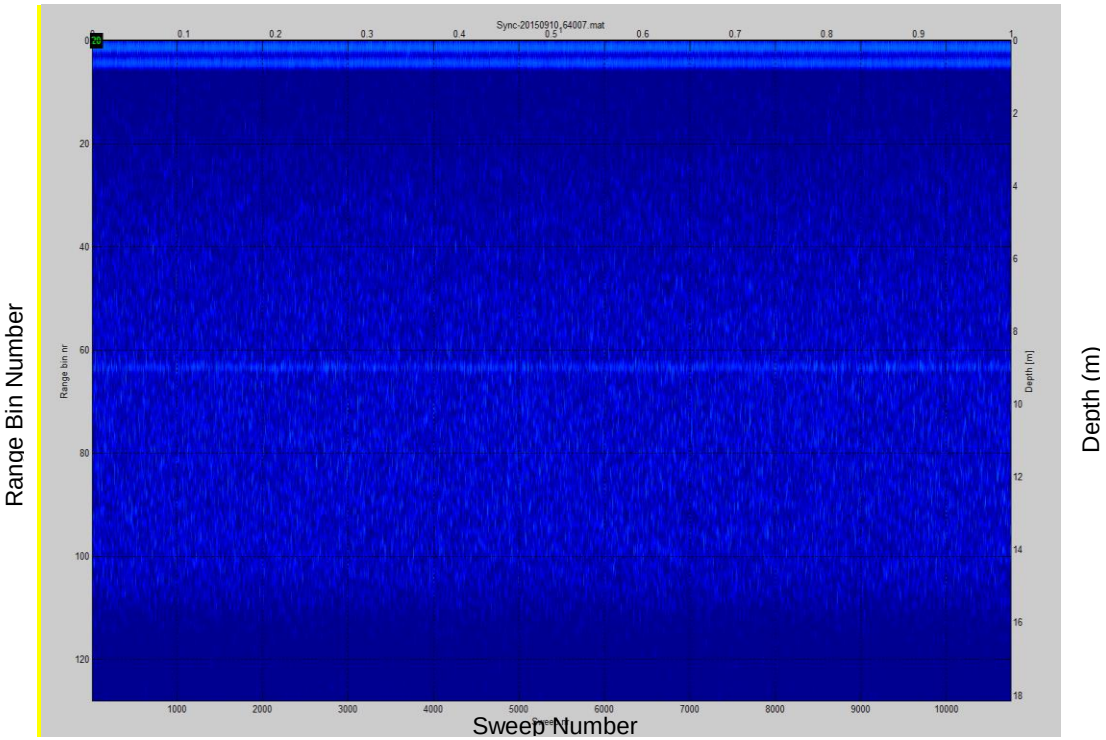

Figure 55: RTSA of Radar Data – PSU PCB Synchronous

Figure 54 and Figure 55 illustrate the same concept discussed after Figure 53, with the difference being that their data sets contain only asynchronous and synchronous data respectively.

Real-Time Spectrum Analysis evaluation conclusion

From this experiment, it is clear that the PSU PCB minimizes all processed radar data distortion (viewed by RTSA), caused by the SMPS switching frequency and its harmonics, when it is synchronised to the sample frequency and SRF (SYNC CLK connected). In the next section, the raw radar data sets will again be processed using Matlab in order to generate RDM's.

6.2.3. Range-Doppler Map Evaluation Procedure and Results

The purpose of this experiment is to convert the raw radar data sets into RDM's, using Matlab. The RDM's will then be analysed to evaluate whether the PSU PCB is able to eliminate "false targets" on the RDM's caused by the SMPS frequency.

Range-Doppler Map evaluation procedure (Matlab setup)

The Matlab setup below was utilised to process the raw Radar Data into the form of range-Doppler maps. The Matlab code can be found in Appendix C – Range-Doppler Map Generation in Matlab

Loading Data

- Load the desired file

Doppler Bin and Trace Window Setup

- Use second data set and 1 trace per column
- Setup Doppler Bin Size
- Set Trace Window Starting Point

Burst Setup

- Isolate 1 burst, 1 trace per row
- Set Burst to start at Trace Window Starting Point
- Set Burst to stop at Doppler Bin Size

FFT Setup

- Apply Range FFT in a Horizontal direction
- Apply Doppler FFT in a Vertical direction

RDM Plot Setup

- Setup the plot
- Setup the graph axis parameters
- Setup the colour scaling
- Setup the labels

Range-Doppler Map evaluation results

The RDM is essentially the RTSA Radar data in section 6.2.2 (which only had a range FFT applied to it in the Horizontal direction), with an additional Doppler FFT applied to it in the Vertical direction. Figure 56 shows the radar RDM with the PSU PCB not synchronised.

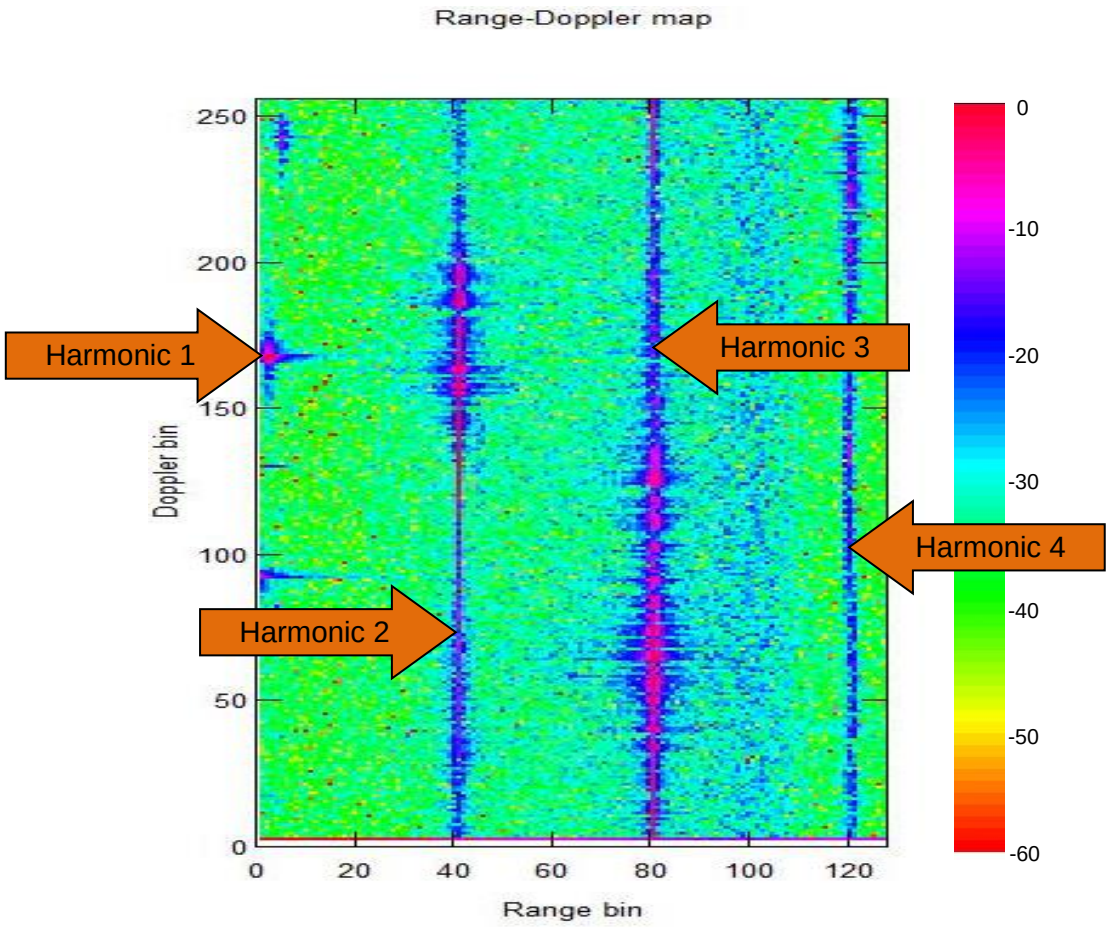

Figure 56: Radar RDM – PSU PCB Asynchronous

From Figure 56, it can be seen that with the PSU PCB Asynchronous, there is interference caused by the SMPS frequency and its harmonics around range bin 5, 40, 80 and 120. This corresponds to Figure 53, where the interference was also prevalent at range bin 5, 40, 80 and 120. This is to be expected, as the RDM is essentially a snapshot of part 1 of Figure 53, with a Doppler FFT applied to it. As discussed in Section 6.2.1, the default Asynchronous SMPS frequency is around 820,5kHz (and also in burst-mode). From this we can determine what we are actually seeing on the RDM.

$Range\ Bin\ No. = \frac{SMPS\ Freq}{\frac{Freq}{Range\ bin}}$, and with the $\frac{Freq}{Range\ bin} = \frac{195.3Hz}{256} = 736.98Hz/RB$ (for this System)

This makes the Asynchronous Frequency $Range\ Bin\ No. = \frac{820.5kHz}{736{,}98Hz/RB} = Range\ Bin\ 1113$

Range Bin 1113 is out of the range viewed in Figure 56 (which only goes up to Range Bin 120). This means that the interference viewed is actually aliased ("folded-back") Harmonics of the SMPS carrier frequency at 820,5kHz.

Additionally, the reason that the interference seems to be "smudging" on the RDM is as a result of the SMPS being in burst–mode. Burst-Mode causes the SMPS carrier frequency and subsequently its harmonics, to be unstable and constantly vary in frequency (range) and Doppler (velocity). Figure 57 shows the radar RDM with the PSU PCB synchronised.

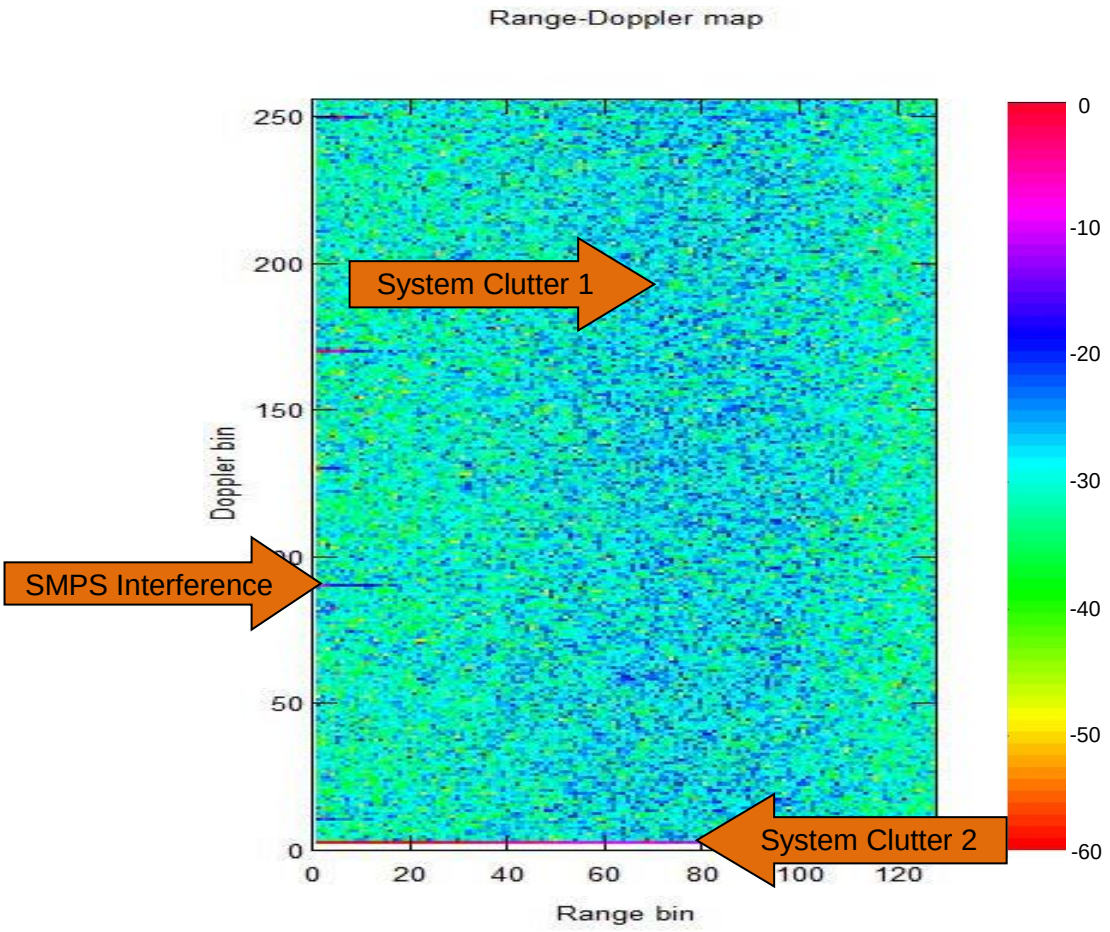

Figure 57: Radar RDM – PSU PCB Synchronous

In Figure 57, we see that with the PSU PCB synchronised, the interference caused by the SMPS frequency and its harmonics have now been dramatically reduced, this is due to the following reasons:

- Synchronising to the sample frequency causes the interference frequencies to aliase to 0Hz i.e. in Range bin 0

- Synchronising to the SRF causes the interference frequencies to be in phase with the SRF and hence fall into Doppler bin 0

Observations made, that would not have been seen in the simulation in Chapter 3:

- The system clutter 1 is because there is no target (large peak) being sensed by the Radar, this then increases the radar sensitivity, which enhances ambient noise.
- The system clutter 2 is inherent system noise. The mean of the system noise is very close to 0, thus placing it in Doppler bin 0.
- The SMPS interference is due the SMPS output frequency jitter, this is discussed further below.

The SMPS buck regulator IC has an internal Phase-Lock Loop (PLL) circuit which "locks" the SMPS output frequency to the SYNC CLK input. This mechanism inherently produces some jitter of the SMPS output frequency (relative to the SYNC CLK input), this means that the actual $f_{SMPS} = f_{SYNC\ CLK} \pm \Delta Hz$. Since synchronisation of the SMPS to the SYNC CLK input (which is a multiple of the Sample frequency) causes the interference frequencies to aliase to 0Hz i.e. in Range bin 0, therefore, the interference frequencies will now actually aliase to Range bin 0 $\pm \Delta RB$.

The ΔRB (or ΔHz) is continuously changing, which leads to the "smudging" effect observed in Figure 57 between Range Bin 0 and Range Bin 20. The continuous variation in the ΔHz also introduces a varying phase shift between sweeps and thus a Doppler component. This Doppler component and its harmonics can hence be seen emerging in Doppler at Doppler-Bin 90, 170, and 250.For the current application, the radar will not be looking at very close in targets; hence, the desensitisation below Range Bin 20 does not affect the system integrity, and is still acceptable.

Range-Doppler Map evaluation conclusion

In this experiment, the PSU PCB was able to successfully eliminate majority of the "false targets" on the RDM, caused by the SMPS frequency. The system clutter encountered, was as expected, and the minor SMPS interference was deemed acceptable. The SMPS jitter interference mitigation is not part of this study, but may be a feasible area for future research. In the next section the PSU PCB will be evaluated for military and industry specification compliance.

6.3. Military and Industry compliance evaluation

The purpose of this experiment is to evaluate whether the PSU PCB complies with the military and industry specifications, as indicated previously in Chapter 4 - Design Specification.

6.3.1. Procedure

In order to evaluate for military and industry specification compliance, at a PCB and schematic level, Altium design rule check is utilised, and at an assembly level, IPC soldering and harnessing standards are followed, the verification of these procedures follow in this section (IPC, 2014) (IPC, 2002).

6.3.2. Results

The setup for the Altium design rule check can be seen in Figure 58 . This is a standard setup which is used for all RRS's PCB products designed using the Altium designer software.

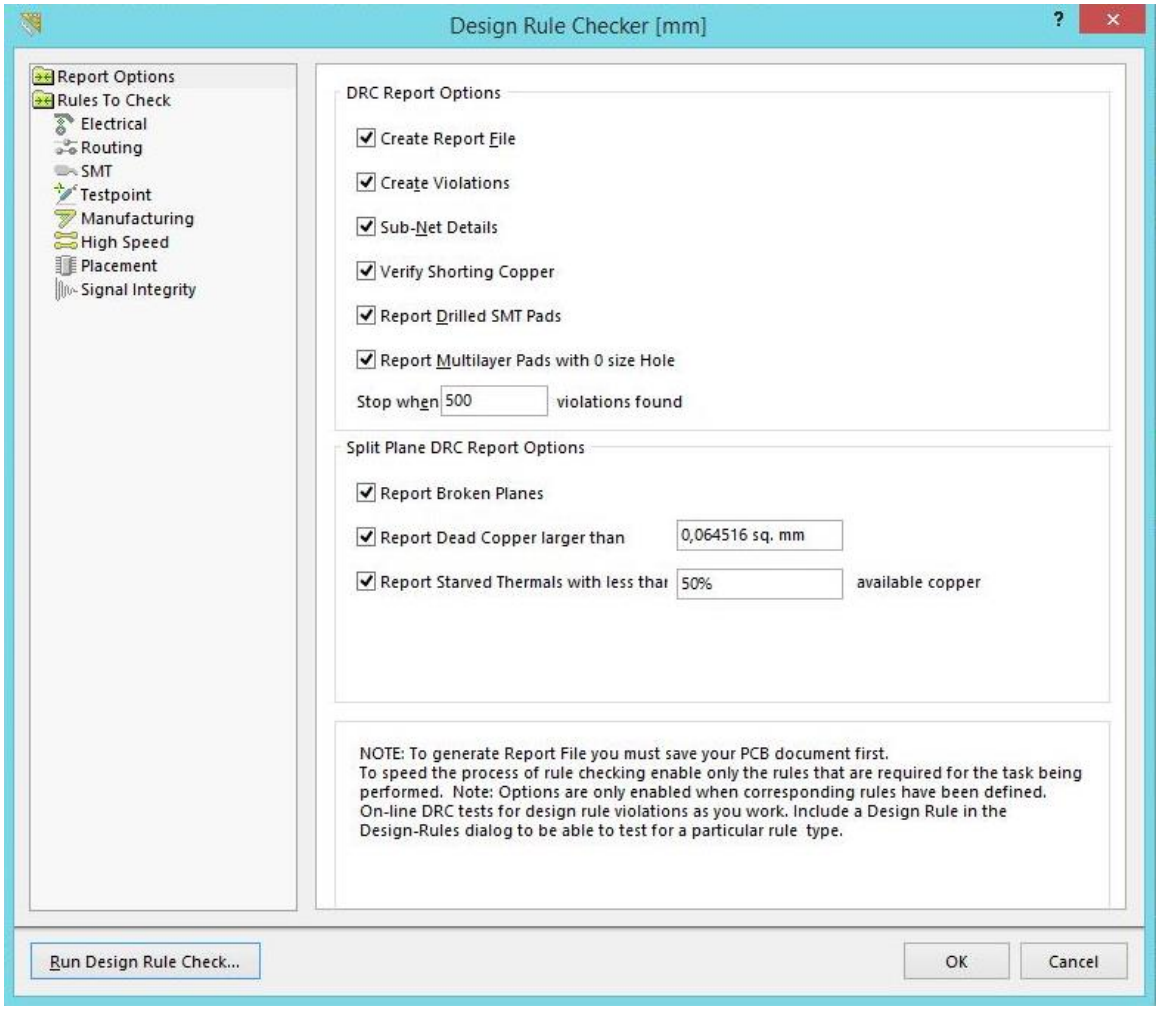

Figure 58: Altium design rule check setup

Once the setup has been completed, the design rule check will be run. A screenshot of the results of the Altium design rule check for the PSU PCB design can be seen in Figure 59.

Altium Designer

customize

Design Rule Verification Report

Date : 08/10/2015
Time : 10:36:06 AM
Elapsed Time : 00:00:01
Filename : C:\Users\mslamdien\Desktop\LTC3601 PSU.PcbDoc

Warnings : 0
Rule Violations : 0

Summary

Warnings	Count
Total	0

Rule Violations	Count
Clearance Constraint (Gap=0.5mm) (innamedpolygon('Bot-GND')),(All)	0
Short-Circuit Constraint (Allowed=Yes) (InNet('PGND')),(InNet('SGND') or Innet('GND'))	0
Clearance Constraint (Gap=0mm) (InNet('PGND')),(InNet('SGND') or Innet('GND'))	0
Minimum Annular Ring (Minimum=0.15mm) (All)	0
Clearance Constraint (Gap=0.5mm) (OnLayer('Keep-Out Layer')),(All)	0
Hole Size Constraint (Min=0.15mm) (Max=4mm) (Disabled)(All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm) (Entries=4) (Isvia)	0
Clearance Constraint (Gap=0.2mm) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.5mm) (Conductor Width=0.5mm) (Air Gap=0.25mm) (Entries=4) (Ispad)	0
Total	0

Figure 59: Altium design rule check results for PSU PCB

As can be seen in Figure 59, at a PCB and schematic level, there are no Warnings and no Rule Violations, meaning the PSU PCB complies with all the industry and military specification design rule checks done in Altium. In Table 8 we summarise the Altium Design rule verification results, as well as, verify that the IPC soldering and harnessing standards were followed during the PSU PCB assembly and integration procedure (IPC, 2014) (IPC, 2002).

Table 8: PSU PCB Design and Assembly Altium/IPC Procedure Verification

PSU PCB IPC Procedure Verification		
No.	**Inspection**	**Compliance**
1	Altium Design Rule Check enforced to ensure compliance to military and industry tolerances and clearances etc.	✓
2	RRS PCB Pre-Assembly Checklist used to verify that the bare PCB is manufactured and delivered as per the QC (Quality Control) PCB workmanship inspection criteria from IPC-A-600F-Acceptability of Printed Boards Standard and thus also compliant with military and industry specifications. (IPC, 1999).	✓
3	The RRS PCB Assembly Checklist used to verify that the PCB was assembled according to IPC-J-STD-001E - Requirements for Soldered Electrical and Electronic Assemblies, and hence also compliant with military and industry specifications (IPC, 2014).	✓
4	The RRS PCB Assembly Final Inspection Checklist used to verify that the PCB workmanship is in compliance with the inspection criteria from IPC-A-600F-Acceptability of Printed Boards Standard, and subsequently with military and industry specifications (IPC, 1999)	✓
5	The IPC/WHMA-A-620 - Requirements and Acceptance for Cable and Wire Harness Assemblies used to verify that the system integration harnesssing has been done according to IPC, military and industry specifications (IPC, 2002).	✓

In Table 8 we see that the PSU PCB design has passed the Altium Design Rule Check. The assembly procedure has been done according to IPC standards, and the Receiver subsystem Integration Harnessing has also followed IPC protocol (IPC, 2014) (IPC, 2002).

6.3.3. Conclusion

Since the Altium design rule check and IPC standards are accepted worldwide for aerospace, industry and military grade products, we can conclude that the PSU PCB was designed and built in compliance with Military and Industry Specifications. The next chapter will provide the conclusions for this study, as well as recommendations for future work (IPC, n.d.).

Chapter 7
Conclusions and recommendations

The PSU PCB was found to be in compliance with voltage and current requirements for the Receiver Subsystem Integration. The efficiency was determined to be 92.31%, which is better than a typical off-the-shelf SMPS (90%) (Huffman, n.d.).

The measured output of the PSU PCB was found to be clean, and because it was able to synchronise to both the sample frequency and the SRF, it can be concluded that the PSU PCB is able to greatly reduce the SMPS EMI, by producing a clean, synchronous output.

With the PSU PCB synchronised to the sample frequency and SRF (SYNC CLK connected). It is clear, that the PSU PCB is able to minimise all processed radar data distortion (while viewed by RTSA), caused by the SMPS switching frequency and its harmonics.

The PSU PCB was able to successfully eliminate majority of the “false targets” on the RDM, caused by the SMPS frequency. The system clutter encountered, was as expected, and the minor SMPS interference was deemed acceptable. The SMPS jitter interference mitigation was beyond the scope of this study, but it unveiled itself to be a feasible area for future research.

The PSU PCB was found to be compliant with the Altium design rule check and IPC standards. Since these are accepted worldwide for aerospace, industry and military grade products, we can conclude that the PSU PCB was designed and built in compliance with Military and Industry Specifications (IPC, n.d.).

Since the buck converter (LTC3601) has a maximum switching frequency of 4MHz, in future, for applications with higher sampling frequencies, an alternative converter with a higher switching frequency should be considered (Linear Technologies, n.d.).

The approach developed in this study, i.e. to synchronise the PSU to a system SYNC CLK, may in future be utilised to synchronise other interference generating radar sub-systems such as the Ethernet clock etc.

The technique may also be applied outside of Radar systems, in other electronic sampling systems which perform digitisation of the input data. Some examples are Vector Network Analysers, Spectrum analysers, Oscilloscopes, and many other types of electronic equipment which use Analog to Digital Converters (ADC’s).

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Appendices

Appendix A – Matlab Simulation Code

Synchronising the SMPS to a multiple of the Sampling Frequency (3.1) Setup

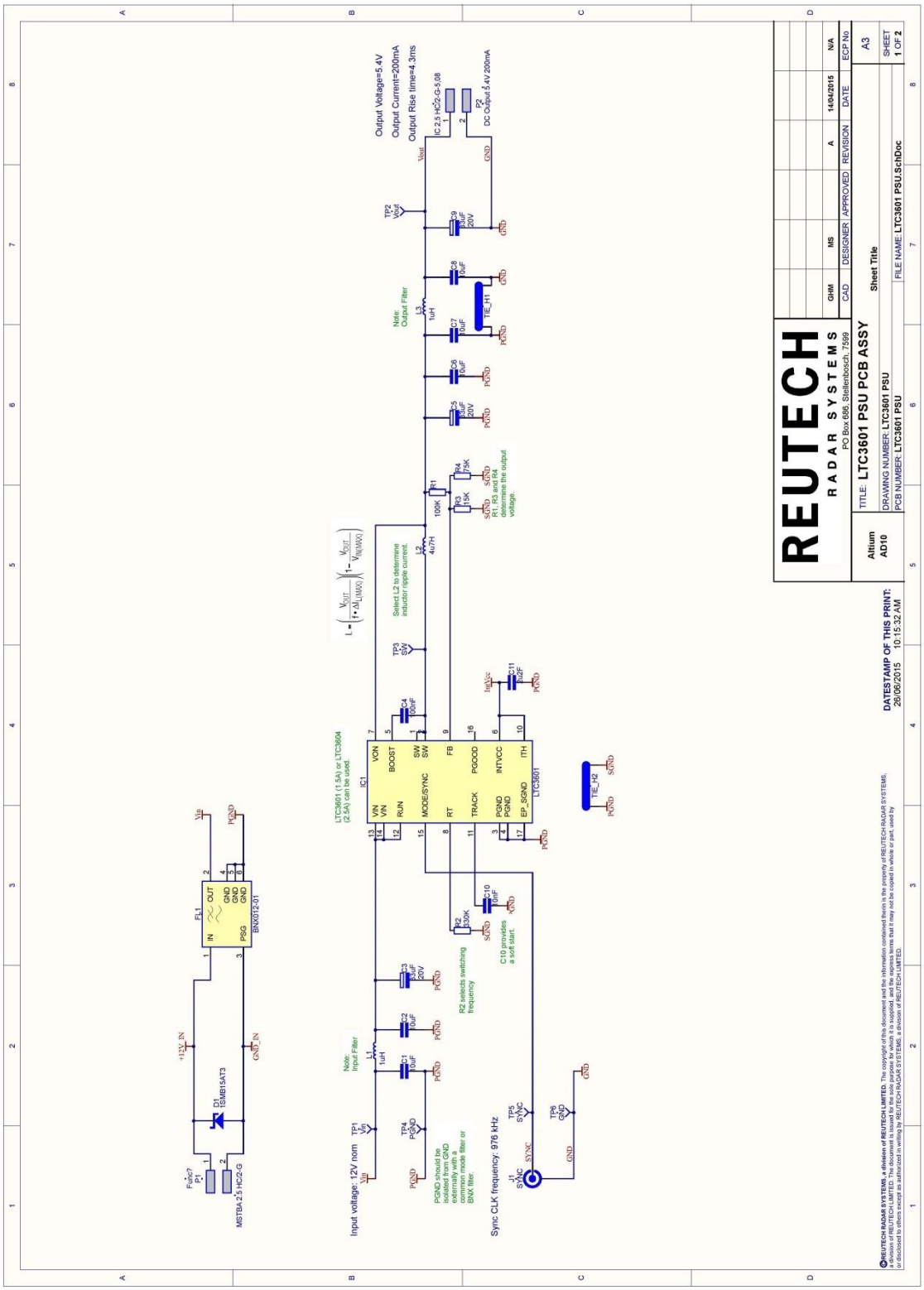
```
% Setup time-------------------------------------
fsample = 200e3;                    % Sample rate (frequency)
Tsample = 1/fsample;                % Sample time interval
t_end    = 0.05e-3;                 % Simulation Stop time
t        = 0   :Tsample/10   : t_end;   % High resolution time vector (for analog signal)
ts       = 0   :Tsample      :t_end;    % Sampled time vector (for sampled/digital signal)
N        =  size (t,2);             % Number of High resolution samples (for analog signal)
Ns       =  size (ts,2);            % Number of samples (for sampled/digital signal)
f0       = 60e3;                    % Freq of (SMPS) Signal investigated
phi0     = 2/180*pi;                % Initial phase of (SMPS) Signal investigated in radians
% Setup signal-----------------------------------
sig      = sin(2*pi*f0*t + phi0);           % Creating analog signal (Sin wave)
sigs     = sin(2*pi*f0*ts + phi0);          % Creating sampled/digital signal (Sin wave)
%sigs    = sign(sin(2*pi*f0*ts + phi0));    % Use to change to a square wave
% FFT-------------------------------------------------
Sig    = 1/N*fft(sig);                      %FFT applied to analog signal
Sigs   = 1/Ns*fft(sigs);                    %FFT applied to sampled/digital signal
f  = 0: 1/t_end : fsample*10;               % High res freq vector step size and end time
fs = 0: 1/t_end : fsample;                  % Sampled freq vector step size and end time
% Plot-----------------------------------------------
figure (1);                                 %Plot figure 1
plot (t,sig,'b-',ts,sigs,'ro','linewidth',2);   %Set up graph axis
grid on                                     %View grid lines
title ('Analog Signal-With Sample Plots (Red)');   %Add graph title
xlabel ('time [s]');                        %Add x-axis label
```

```
ylabel ('Amplitude [V]');                %Add y-axis label

figure (2);                              %Plot figure 2

plot                                     %Set up graph axis
(f(1:N/2),20*log10(abs(Sig(1:N/2))),'b',fs(1:Ns/2),20*log10(abs(Sigs(1:Ns/2))),'g','linewidth',2);

grid on                                  %View grid lines

xlim ([0 200e3]);                        %Set x-axis limit

title ('FFT Signals');                   %Add graph title

xlabel ('Frequency [Hz]');               %Add x-axis label

ylabel ('Amplitude [V]');                %Add y-axis label

%axis ([0 200e3 -50 100]);               %Set axis limits (if desired)
```

Synchronising the SMPS to the SRF of the Signal Processor (3.2) Setup

```
% Setup time----------------------------------------------------------
fsample = 200e3;                          % Sample rate (frequency)
Tsample = 1/fsample;                      % Sample time interval
SRI     = 256*Tsample;                    % Sweep repetition interval
SRF     = 1 / SRI;                        % Sweep repetition frequency
Burst   = 256 * SRI;                      % Total burst duration
ts      = 0   :Tsample      :(Burst-Tsample);   % Sampled time vector (for sampled/digital signal)
f0      = 5*SRF %fsample*1;       % Freq of (SMPS) Signal investigated (integer=synchronized)
phi0    = 2/180*pi;               % Initial phase of (SMPS) Signal investigated in radians
% Setup signal (single vector)-----------------------------------
sig    = sin(2*pi*f0*ts + phi0);          % Creating sampled/digital signal (Sin wave)
sig    = sign (sig);                      % Changing into a square wave
% Reshape into burst (256x256)-----------------------------------
sigBurst = (reshape (sig,256,256))';      %Reshaping into a burst
% FFT------------------------------------------------------------------
sigBurstR   = 1/256*fft(sigBurst,256,2);        % FFT in Range (horizontal direction)
sigBurstD   = 1/256*fft(sigBurstR,256,1);       % FFT in Doppler (Vertical direction)
% Plot-----------------------------------------------------------------
figure (1);                               %Plot figure 1
imagesc(20*log10(abs(sigBurstD)));        %Display image with scaled colours
axis ([0 128 0 256]);                     %Set axis limits
clim([-60 0]);                            %Set colour limits
axis xy                                   %View x and y axis
xlabel ('Range bin');                     %Add x-axis label
ylabel ('Doppler bin');                   %Add y-axis label
title ('Range-Doppler map')               %Add graph title
```

Appendix B – Complete Schematic Design



Appendix C – Range-Doppler Map Generation in Matlab

```
% Load Data---------------------------------------------------------------

load('C:\Async-Sync-Async-20150910_161451.mat');          %Load Radar data

% Use A2D1                    % 1 trace per column, i.e. to get first trace: A2D1(:,1)

% Setup Doppler Bin Size and Trace Window Starting Point-----

DoppN  = 256;                              %Set Doppler bin size

Tracestart = 8410;                         %Set Trace start point

% Isolate 1 burst, trace per row-----------------------------------------

Burst = (double(A2D1(:,Tracestart + (1:DoppN))))'; % Isolating 1 burst

% FFT---------------------------------------------------------------------

BurstR   = 1/256*fft(Burst,256,2);         % Range FFT (Horizontal direction)

BurstD   = 1/256*fft(BurstR,DoppN,1);      % Doppler FFT (Vertical direction)

% Plot--------------------------------------------------------------------

figure (1);                                %Plot figure 1

imagesc(20*log10(abs(BurstD)));            %%Display image with scaled colours

xlim ([0 128]);                            %Set x-axis limit

axis ([0 128 0 DoppN]);                    %Set axis limits

clim ([-60 0]);                            %Set colour limits

axis xy                                    %View x and y axis

xlabel ('Range bin');                      %Add x-axis label

ylabel ('Doppler bin');                    %Add y-axis label

title ('Range-Doppler map')                %Add graph title
```