Cape Peninsula
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THE IEC61850 STANDARD-BASED PROTECTION SCHEME FOR POWER TRANSFORMERS

by

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DECLARATION

I, Bwandakassy Elenga Baningobera, declare that the contents of the thesis represent my own unaided work, and that the thesis has not previously been submitted for academic examination towards any qualification. Furthermore, it represents my own opinions and not necessarily those of the Cape Peninsula University of Technology.

	23rd August 2018
Signed	**Date**

ABSTRACT

Transformer Differential and overcurrent schemes are traditionally used as main and backup protection respectively. The differential protection relay (SEL487E) has dedicated harmonic restraint function which blocks the relay during the transformer magnetizing inrush conditions. However, the backup overcurrent relay (SEL751A) applied to the transformer protection does not have a harmonic restraint element and trips the overcurrent relay during the inrush conditions. Therefore, to prevent the malfunction caused by the transformer magnetizing inrush current, a novel harmonic blocking method is developed, implemented and tested in the RSCAD simulation environment. The IEEE 14 bus transmission system is considered as a case study. The IEEE 14 bus system is modelled and simulated in the DIgSILENT and RSCAD simulation environments respectively. The developed harmonic blocking scheme is implemented in the Hardware-In-the-Loop (HIL) simulation environment using Real-Time Digital Simulator and numerical protection IEDs. The developed scheme uses the Harmonic Blocking element (87HB) of the transformer differential relay (SEL487E) to send an IEC61850 GOOSE-based harmonic blocking signal to the backup overcurrent relay (SEL751A) to inhibit it from tripping during the transformer magnetizing inrush current conditions. The hardwired and GOOSE simulation results are analysed for the transformer differential protection and the backup overcurrent protection schemes for internal, external events and transformer magnetizing inrush current conditions. The simulation results proved that the IEC61850 standard-based protection scheme is faster than the hardwired. Therefore, the speed and reliability are improved using the IEC61850 standard-based GOOSE applications to the transformer digital protective relaying system.

Keywords: Transformer protection, Overcurrent protection, Current differential protection scheme, Transformer magnetizing inrush current, Harmonic blocking, IEC 61850 standard, Substation communication, GOOSE, Hardware in the loop simulation.

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- All my CSAEMS colleagues for their support.

DEDICATION

This thesis is dedicated to my grand-mother **NGAMBOU Marie-Louisette** and the entire family. Further dedication goes to my best friend **Rochy EWOUYA** and my fiancée **Dominique MAVOUNGOU.**

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GLOSSARY

Terms/Abbreviations	Definition/Explanation
AcSELerator Architect	A software for substation communications networks using the IEC 61850 MMS and GOOSE protocols required to configure message publications and subscriptions.
AcSELerator Quickset	A software tool for engineers to configure, commission and manage SEL devices for power system protection, control, metering and monitoring.
Algorithm	A step by step procedure for solving a problem or accomplishing some task, especially by a computer.
Artificial Neural Network (ANN)	Interconnected group of artificial neurons that uses a mathematical or computational model for information processing based on a connectionist approach to computation.
ATP	Alternative Transient Program
B-H Loop	Hysteresis loop that shows the relationship between the induced magnetic flux density (B) and the magnetizing force (H).
CID	Configured IED Description file
Current Transformer (CT)	A transformer for use with meters and/or protection devices in which the current in the secondary winding is, within prescribed error limits, proportional to and in phase with the current in the primary winding.
DAC	Digital Analogue Converter
DFT	Discrete Fourier Transform
DIgSILENT	Power systems modelling, analysis and simulation software for applications in generation, transmission, distribution and industrial systems.
DWT	Discrete Wavelet Transform
EMTP	Electromagnetic Transient Program
External fault	System faults are external to the transformer protection zone.
FFT	Fast Fourier Transform
Fuzzy logic	A form of many-valued logic in which the truth values of variables may be any real number between 0 to 1.
GOOSE	**Generic Object-Oriented Substation Event** where any format of data, such as status, value, etc. is grouped into an IEC61850 dataset and transmitted within a time period of a few milliseconds.
GTFPI	Gigabit-Transceiver Front Panel Interface
HIL	Hardware-In-the-Loop simulation is a technique that is used

	for testing control systems.
HV	High Voltage
ICD	IED Capability Description file
IEC	International Electrotechnical Commission
IEC 61850	A communication standard used for the realization of automation in the substation. It is a part of the International Electro-technical Commission's (IEC) Technical Committee 57 (TC57)
IED	**Intellectual Electronic Device** is a microprocessor-based controller used to protect power system equipment.
IEEE	Institute of Electrical and Electronics Engineers.
Internal fault	Transformer faults that occur inside the transformer protection zone.
LG	Single-phase-to-ground fault
LLG	Double-phase-to-ground fault
LLLG	Three-phase-to-ground fault
LV	Low Voltage
Method	The procedures and techniques characteristics, orderly arrangement of parts or steps to accomplish an end.
MMS	IEC 61850 – Manufacturing Message Specification
Network	The apparatus, equipment, plant and buildings used to convey, and control the conveyance of electricity to customers excluding any connection assets.
Numerical relays	Multifunctional devices using numerical algorithms that can easily duplicate any of the protection functions with simple software modifications.
Omicron CMC 356/256plus	Universal relay test set and commissioning tool.
Power system	Integration of the functions of the generation, transmission and distribution.
Protection system	A system, which includes equipment, used to protect facilities from damage due to an electrical or mechanical fault or due to certain conditions of the power system.
Reliability	The possibility of a system, performing its function sufficiently for the period of time intended, under the encountered operating conditions.
RSCAD	Power system simulation software designed specifically for interfacing with the RTDS simulator hardware to perform real-time digital simulations.

RTDS	Real-Time Digital Simulator
SCD	Substation Configuration Description file
SCL	Substation Configuration Language is defined by the IEC 61850 standard for configuration of substation devices/apparatus.
SEL	Schweitzer Engineering Laboratories
SEL-751A	Feeder protection relay
SEL-487E	Current differential protection relay
S-winding	CT secondary current inputs for transformer primary windings.
Test Universe	A software tool for parameter related testing of protection and measurement devices in power systems.
TMIC	Transformer Magnetizing Inrush Current
Transformer	A device that steps down or up the voltage of alternating current.
Transient	A sudden, brief increase in current or voltage in a circuit that can damage sensitive components and instruments.
T-winding	CT secondary current inputs for transformer secondary windings.
Voltage transformer (VT)	A transformer for use with and/or protection devices in which the voltage across the secondary terminals is, within prescribed error limits, proportional to and in phase with the voltage across the primary terminals.
WI	Waveform identification

CHAPTER ONE
INTRODUCTION

1.1 Introduction

Power transformers of medium and large sizes are very critical and vital components for power systems. Due to its significance and cost, its protection needs to be appropriately addressed (Tripathy M. et al., 2010). Transformer protection should be fast and reliable. To provide early cautioning of electrical failures and prevent disastrous losses, appropriate monitoring of power transformer should be selected. This results in the damage limit and the reliability improvement of the power supply (Tripathy M. et al., 2010). The requirements of the protective relays (Tripathy M. et al., 2007) include dependability (no missing operations), security (no false tripping), speed of operation (short fault clearing time) and stability. Therefore, a transformer differential relay is used to meet the protection requirements of the medium and large power transformers. The differential scheme approach compares the currents at the primary and secondary on the protected zone of the transformer by calculating and monitoring a differential current. In case the computed value of the differential current is greater than the set value, this indicates an internal fault.

A switching-in or an external fault recovery can cause a sudden change in the input terminal voltage of a transformer and the large current drawn by the transformer from the supply is known as inrush current. Energising a transformer which is in parallel with a transformer that is already in service can cause a similar magnetizing inrush condition, known as “sympathetic inrush”. The inrush condition results in the saturation of the transformer core. Magnetizing inrush current that arises in a transformer is identified by comparing the polarity and magnitude of residual flux which does not correspond to polarity and magnitude of an ideal instantaneous value of steady-state flux. Magnetizing inrush current can be as high as ten times of full load current (Tripathy M. et al., 2010).

The inrush condition phenomenon would typically cause the trip element of the transformer differential to mis-operate, if not adequately blocked or restrained. Transformer inrush currents usually are rich in harmonics in general and in second harmonic particularly. The second-harmonic ratio is traditionally used for transformer

differential protection in order to block or restrain the differential trip elements during transformer magnetizing inrush current conditions (Guo X. et al., 1992).
Presently there are three types of schemes that are being used for the magnetizing inrush current determination (Paraskar S. and Beg M., 2011):

- First scheme makes use of data obtained from the transformer incoming currents only. The method is based on the principle of second harmonics restraint.
- Second scheme makes use of information that is obtained from the transformer terminal voltage variation. This method is based on the voltage restraint principle.
- Third scheme makes use of information that is obtained from both the transformer's currents and voltages. This method is based on the flux characteristic principle using the low-voltage acceleration criterion.

This thesis used the first scheme which is the second harmonic restraint method for magnetizing inrush current determination. Extra reliability to the power system is provided by the backup overcurrent protection schemes. Backup overcurrent relaying scheme is attached to the main protection with its own relaying system. The primary role of the backup overcurrent relay is to operate in case of any failure or tripping of the circuit breakers due to the main protection.
The main protection which is the transformer differential scheme may fail due to (Manuel Bolotinha, 2014):

- The mechanical defect of moving regions of the transformer differential relay,
- Transformer differential relay DC supply failure
- Tripping pulse of the transformer differential relay failure to the breaker
- Current or voltage supply failure to the transformer differential relay from CT or VT circuits

However, this thesis is not considering the above failure conditions of the transformer differential scheme. In this specific situation, another type of protection called backup overcurrent relaying scheme is applied. Hence, backup overcurrent relaying scheme has every configuration setting separate from the main transformer differential protection. The reason is the backup overcurrent relay must not fail to operate in case of the failure of the main protection scheme. As a backup overcurrent protection scheme, it must be

slower in action than the main differential protection one, so that it should only work in case the main differential protection scheme of the transformer fails.

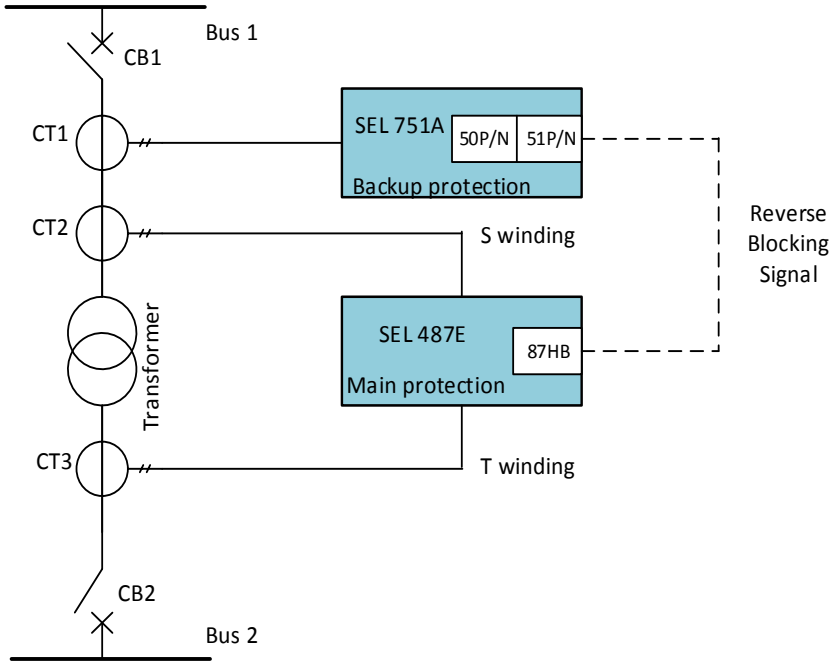


Figure 1.1: Reverse harmonic blocking scheme for transformer protection

With reference to Figure 1.1, the transformer differential relay has the magnetizing inrush current function, which blocks the differential relay from tripping for inrush conditions. Nevertheless, the overcurrent relay employed as backup protection to the transformer differential protection scheme does not have the inrush current function, and it will trip during inrush conditions. This thesis used the differential relay SEL-487E as the main protection and backup overcurrent protection SEL-751A. In order to restrain SEL 751A overcurrent relay from tripping during inrush conditions, a blocking scheme based on second harmonic restraint current is employed. The second harmonic restraint scheme uses the harmonic blocking element (87HB) of the SEL-487E to send a blocking signal to the SEL 751A to inhibit it from tripping during inrush current conditions.

The IEEE 14-bus system is simulated in the DIgSILENT and RSCAD software environments to generate a fault and inrush current conditions. The lab-scale test bench setup is implemented to test the phase percentage differential protection schemes using SEL-487E IED and omicron CMC 356 test injection device. The demonstration of the IEC 61850 standard-based reverse harmonic blocking scheme is implemented in the

CSAEMS laboratory using omicron test injection device CMC 356, SEL-487E and 751A protection IEDs. Finally, implementation and testing of the IEC 61850 standard-based hardware-in-the-loop simulation are performed using RTDS and protection IEDs. The hardware-in-the-loop simulation is conducted for external and internal faults and inrush current conditions.

1.2 Awareness of the problem

The electrical power network is an integration of generation, transmission and distribution. The subsections of the transmission are achieved through the application of the power transformers. Transformers are utilised to step up or down the voltages of an alternating quantity in the electric power systems. Transformers are one of the most essential elements of the power systems. Transformers with 1 MVA and above are equipped with differential relays to detect internal faults in power transformers (Brian Gladstone, 2004). High speed, reliable and highly sensitive are the requirements of the protection scheme. Differential relaying principle is based on the fact, that any fault within the protected zone of the transformer would cause the current entering the zone of protection to be different from the current leaving. Therefore, the two currents (primary and secondary) at the zone of protection are compared, and a trip signal is issued when the differential current exceeds the predetermined set value.

Inrush current condition is described as the instantaneous high input current drawn by a transformer when its core is energised and saturated; the inrush current has a short duration, frequently milliseconds (Brian Gladstone, 2004). Transformer magnetizing inrush current is a phenomenon that depends on time, and it is caused by several coincidental sets of conditions happening when the transformer is switched on.

There are three categories of transformer inrush currents which are: energisation inrush, recovery inrush and sympathetic inrush (Brian Gladstone, 2004). The first, energisation inrush occurs when a system voltage is reapplied to a transformer which was previously de-energised. The recovery inrush condition is the result of the restoration of a transformer voltage after having been interrupted by a short circuit on the system. And finally, sympathetic inrush can be a result of the operation of two or more transformers connected in parallel; by switching on the second transformer when the first one has already been energised.

The transformer core is nonlinear which is the cause of the inrush, and its intensity depends on the instance of the sinusoidal voltage at which it is switched on as well as on the characteristics of the ferromagnetic core such as its residual magnetism and its magnetization curve (Kang Hae-Gweon et al., 2014). Consequently, it is not classified as a fault on the power system. To prevent the malfunction caused by the transformer magnetizing inrush current, only the transformer differential protection scheme has the second harmonic blocking function. On the other hand, the backup overcurrent protection IED at the primary winding side of transformer protective relaying system has the risk of mal-operation due to the inrush current and not able to detect the magnetizing inrush conditions in comparison with the differential scheme.

Therefore, ***the awareness of the research problem is to develop a new method to mitigate the mal-operation of the backup overcurrent protection scheme of the power transformer during inrush conditions.*** This research thesis developed an IEC 61850 standard-based second harmonic restraint scheme which transmits the GOOSE blocking a signal from the transformer differential relay (SEL-487E) to the backup overcurrent relay (SEL-751A) during inrush current conditions.

1.3 Problem statement

For internal faults, the transformer differential protection scheme must operate very fast, and it must not respond to the magnetizing inrush current conditions. Over the years, several algorithms have been developed in order to increase the operation speed of a transformer differential relay for internal fault conditions and also to increase its reliability against inrush current conditions (Delshad M. and Fani B., 2007).

Modern digital transformer differential relays contain algorithms which are based on the harmonic content of differential current processing (Delshad M. and Fani B., 2007). They are separated into two primary groups. The first group consists of a method which directly recognises a fault from the behaviour of differential current. The second group is based on harmonic processing and generally uses the ratio of the second harmonic to the fundamental part of differential currents (Delshad M. and Fani B., 2007).
During inrush conditions, the backup overcurrent protection of transformer operates due to a high level of transformer magnetizing inrush currents (Tripathy M. et al., 2010).

Problem statement: ***The conventional backup overcurrent protection scheme of the power transformers produces a false trip signal due to transformer magnetizing inrush current conditions. Therefore, it is necessary to develop a test bench setup and implement the IEC 61850 GOOSE interlock message signal to be transferred from the transformer differential relay to the backup overcurrent relay in order to block the tripping of the backup overcurrent relay during the inrush conditions.***

1.3.1 Sub-problems

I. Investigate the performance of the transformer differential protection scheme for internal and external fault conditions.

II. Investigate the performance of the backup overcurrent relay for transformer magnetizing inrush current conditions.

1.4 Research aim and objectives

1.4.1 Aim

When fuses or relays are used for transformer protection, it is necessary that the device carries the magnetizing inrush current and provides protection against overloads and short circuits. If the characteristics of the magnetizing inrush for transformer can be calculated efficiently and accurately, then the problem of selecting the proper protective device is simplified. The differential protection is employed as the unit protection for power transformers. The research problem aims to investigate the malfunctioning of the overcurrent relay which is used as a backup protection of the power transformer during a magnetizing-inrush current condition.

Aim: ***To develop and implement a hardware-in-the-loop digital protection scheme using IEC61850 standard-based GOOSE interlock messaging for power transformers. Compare the simulated results of the hardwired and IEC 61850 standard-based protection scheme for power transformers.***

1.4.2 Objectives

The objectives of the research work include review, developing a new algorithm, implementation, simulation, and hardware-in-the-loop simulation as follows:

i. To provide a literature review on the design philosophies of the transformer protection schemes.
ii. To investigate the transformer differential protection scheme using DIgSILENT environment.
iii. To implement a lab-scale setup to test the transformer differential and second harmonic restraint schemes.
iv. To implement a lab-scale setup using IEC 61850 standard-based GOOSE interlock message signals for transformer magnetizing inrush current conditions.
v. To implement a hardware-in-the-loop simulation using RTDS and protective IEDs based on the IEC 61850 standard-based GOOSE interlock message signals for the transformer magnetizing inrush current conditions.
vi. To compare hardwired and IEC 61850 GOOSE message-based simulation results of the transformer protection schemes.

1.5 Hypothesis

The protection malfunction caused by the backup overcurrent relay due to transformer magnetizing inrush current conditions is corrected and improved by developing and implementing a reliable IEC 61850 standard-based protection scheme for the power transformers. Hardware-in-the-loop digital protection scheme based on harmonic blocking GOOSE interlock messaging is implemented and tested in the real-time simulation environment using RTDS and protective relays.

1.6 Delimitation of the research

This research project consists of the following:

i. Model the IEEE 14-bus power systems and perform the engineering configuration setting and testing the percentage differential protection of a three-phase power transformer in DIgSILENT PowerFactory and RSCAD simulation environments respectively.
ii. Implement and test the IEC 61850 standard-based harmonic blocking scheme for a power transformer.
iii. The second harmonic restraint used for the current differential scheme

iv. Simulation and analysis of the results for internal, external and inrush current conditions on the power transformer.

This research did not consider the following:

i. Investigation on the protection of small-sized distribution transformers and pole mounted transformers is not part of this research project.
ii. The generator-transformer unit protection scheme is not part of the investigation of this research work.
iii. Sympathetic inrush current condition on the parallel connected transformers is not part of this research project.
iv. Investigation of the voltage differential scheme is not part of the study

1.7 Motivation of the research project

The differential principle was introduced by connecting an inverse-time overcurrent relay in parallel with the secondaries of the two current transformers on either side of the transformer. However, the differential principle suffered a lot of drawbacks involving for through fault (external event) conditions (Harlow J. H., 2004). It led to the development of the percentage differential principle for power transformer protection.

New and improved core material designs power transformers for lower losses and older units produce a small amount of the second harmonic in their magnetizing currents during energization. When the second harmonic setting level falls below the traditional 15 or 20 percent, transformer differential protection has security problems (Guo X. et al., 1992).

Differential protection and backup overcurrent protection are the most proficient internal faults protection for the power transformer. The differential protection uses differential currents, which result from the difference between HV side and LV side currents and overcurrent uses only primary current. Energization of transformers causes inrush current passing through the transformer coils (Samet Haidar et al., 2015). The inrush current is a harmonic rich current including slowly decaying DC component (Samet Haidar et al., 2015) because of transformer core saturation which leads to overcurrent relay mal-operation.

The differential transformer protection uses a conventional technique based on the second harmonic restraint; however, the overcurrent relay does not have in-built

computation for harmonic function in order to discriminate between an internal fault and inrush currents. This leads to the trip of the elements of the backup overcurrent relay due to transformer magnetizing inrush current conditions which affect the power systems stability.

Therefore, the research project was motivated to develop a new method to prevent the malfunction of the backup overcurrent relay due to the transformer magnetizing-inrush current conditions.

1.8 Assumption

The implementation of the research project work is to be conducted based on the following assumptions:

- The differential protection scheme is applied to power transformers with the capacity of 1 MVA or more.
- The S (E87S) and T (E87T) windings of the transformer protection relay (SEL-487E) are used in the engineering configuration of the differential protection scheme.
- CTs connection for S and T windings compensation is calculated using ABC phasor rotation.
- The main differential protection relay should operate faster than the backup overcurrent relay.
- The IEC 61850 standard-based harmonic blocking scheme for power transformer leads to the development of the digital substation protective scheme.
- IEC 61850 GOOSE communication is faster than the hardwired based communication.
- The results obtained from the hardware-in-the-loop test are the more realistic representation of the transformer protection scheme since the simulation is conducted in real-time using RTDS and protection IEDs.

1.9 Methodology

The research aim is to investigate hardwired and IEC 61850 GOOSE applications to the transformer protection schemes.

The test bench setup provides the lab scale illustration of how the physical power transformer is protected by using differential protection (SEL-487E), and backup overcurrent (SEL-751A) relays as shown in Figure 1.2. The current signals (CT2 and CT3) on both (LV and HV) sides of the power transformer are injected into the S and T windings current channels of the SEL-487E using the OMICRON test injection device. The CT1 current signals are injected into the SEL-751A current channels. Each end of the power transformer is connected to the switching device circuit breakers (CB1 and CB2) respectively. For internal events, the SEL-487E and SEL-751A IEDs current coils are energised and send trip signals to the binary contact of the test injection device as shown in Figure 1.2. The pickup and trip signal of the circuit breakers are represented using the binary signal connected to the output port (OUT101) of the SEL-487E and (OUT102 and OUT103) of the SEL-751A, which are mapped to the binary inputs 1 and 2 of the test injection device as shown in Figure 1.2.

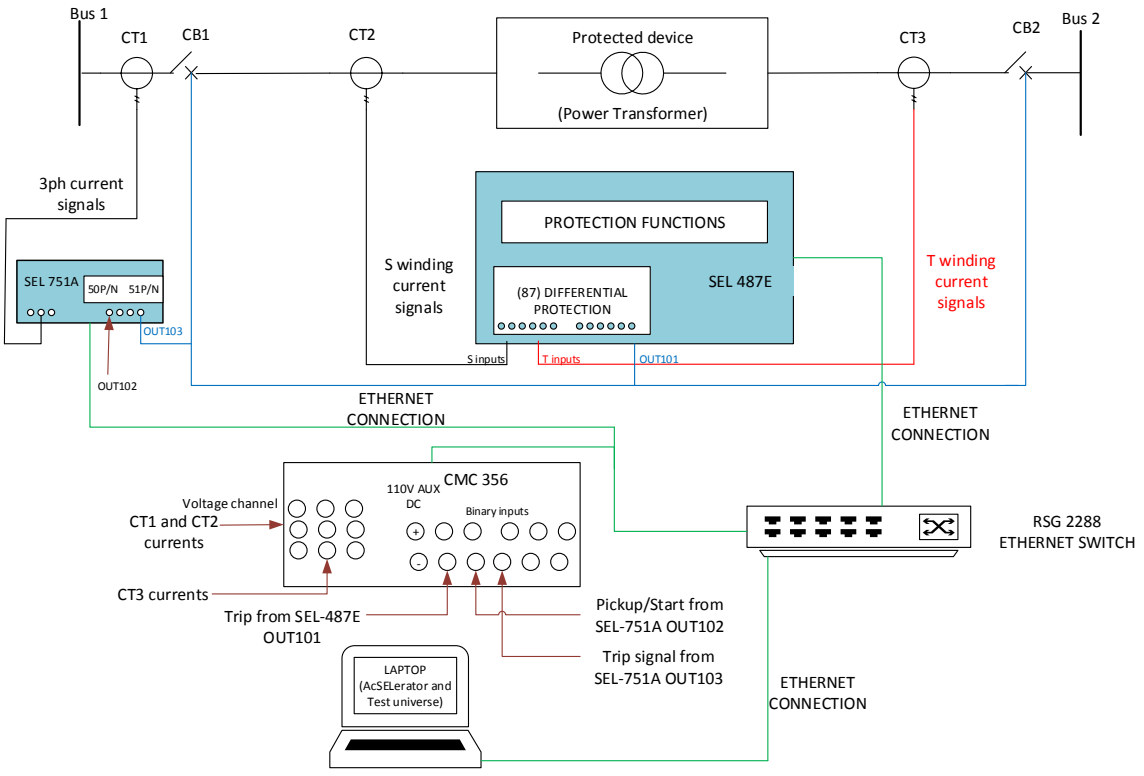


Figure 1.2: Transformer differential and overcurrent protection scheme test bench

The research methods that are employed in achieving the research aim are as follows:

1.9.1 Literature review

The literature review identified the several methods available for power transformers protection such as differential protection, overcurrent and transformer magnetisation inrush currents detection. The transformer protection literature review is done by reading the book chapters on transformer protection, relay manuals, published journal and conference papers. Therefore, a detailed literature review is conducted using Google search databases.

1.9.2 Data collection

The IEEE 14 bus transmission system is used as a case study in this research work. The data of the IEEE 14 bus system are given from Table 4.1 to Table 4.5 in chapter 4 of this thesis. A thorough simulation is conducted in DIgSILENT and RTDS environments in order to collect the data pertaining to transformer magnetizing inrush conditions and differential protection scheme.

1.9.3 Simulation

The simulation study was carried out using DIgSILENT PowerFactory and RTDS softwares. The power transformer protection scheme is investigated for external, internal and inrush current conditions. Short circuit analysis is performed for the IEEE 14-bus transmission system in both DIgSILENT and RTDS environments.

The numerical relay configuration setting tools such as Quickset AcSELerator used for the protection configuration, Architect used for IEC 61850 GOOSE configuration and Omicron test universe software used for the test injection device configuration.

1.10 Implementation of the reverse harmonic blocking scheme lab-scale bench setup

The aim of this research work is to develop and implement a reliable power transformer protection scheme using harmonic blocking based on IEC 61850 GOOSE application to overcome the false tripping of the backup overcurrent relays during magnetizing inrush current conditions. The lab scale engineering configuration setting for transformer protection is performed using AcSELerator Quickset software in order to read, modify/create and write protection settings onto the IEDs. AcSELerator Architect is used for IEC 61850 GOOSE engineering configurations to establish a communication between IEDs, and the test Universe software is used for engineering configuration of

the Omicron CMC 356 test injection device. Implementation, testing and simulation of the IEC 61850 standard-based harmonic blocking scheme for power transformer is performed using RTDS, SEL 487E, SEL 751A protective IEDs and OMICRON test injection device.

1.11 Hardware-in-the-loop simulation

The developed IEC 61850 GOOSE-based harmonic blocking scheme for the power transformer is implemented and tested in a hardware-in-the-loop simulation using physical IED SEL 487E and RSCAD version of the software overcurrent relay in Real-Time Digital Simulator (RTDS). The modelling and hardware-in-the-loop simulation are performed using RSCAD software. COMTRADE fault events files within the RSCAD runtime environment and the signals from the physical IED are used to analyse the simulation results of the transformer protection scheme for internal, external and inrush current conditions.

1.12 Thesis chapters breakdown

The thesis has eight chapters and two appendices as follows:

1.12.1 Chapter One

This chapter describes the research aim and objectives, awareness of the problem, motivation of the research, problem statement, subproblems, hypothesis, delimitation of research, project assumptions, research design and methodology, thesis chapter breakdown and conclusion.

1.12.2 Chapter Two

This chapter presents the literature review on transformer failures, transformer internal and external faults, application of Discrete Fourier and Wavelet transforms for a protective relaying system, digital signal processing algorithms for transformer protection, IEC 61850 standard-based Generic Object-Oriented Substation Event (GOOSE) messages applications to transformer protection and conclusion.

1.12.3 Chapter Three

This chapter focuses on a detailed power transformer protection theory which includes the ideal and practical transformer, transformer sequence impedances, transformer

differential protection scheme and restricted earth fault schemes and mechanical fault detection devices for the power transformer.

1.12.4 Chapter Four

This chapter presents the protective relaying system for the power transformer. This chapter investigates the transformer differential protection scheme for internal and external fault conditions using DIgSILENT simulation software. The backup overcurrent relay of the transformer is investigated for both symmetrical and unsymmetrical events and inrush current conditions in the DIgSILENT software simulation environment.

1.12.5 Chapter Five

This chapter describes the implementation of the differential and overcurrent protection schemes for power transformers using numerical relays. It provides the transformer differential protection configuration setting of the SEL-487E IED, backup overcurrent relay configuration setting of the SEL-751A and Omicron test universe configuration setting for both differential and overcurrent protection functions. The numerical relay simulation results of the transformer protection schemes are provided, and finally, the test bench simulation results are compared with DIgSILENT ones.

1.12.6 Chapter Six

This chapter provides the implementation of an IEC 61850 standard-based harmonic blocking scheme for a power transformer using SEL 487E and SEL 751A protective IEDs and OMICRON test devices. The scheme uses the harmonic blocking element (87HB) of the SEL 487E to send a blocking signal to the SEL 751A to inhibit it from tripping during inrush conditions.

1.12.7 Chapter Seven

This chapter provides the implementation of the Hardware-In-the-Loop (HIL) simulation of the reverse harmonic blocking scheme for the protective relaying system. The HIL simulation is conducted to test the transformer differential protection scheme for internal, external and inrush current conditions.

1.12.8 Chapter Eight

The key findings and the thesis deliverables are summarised in this chapter. The recommendations and future scope of the work are discussed in this chapter.

1.12.9 Appendix A

This appendix describes the data for IEEE 14-Bus system. The IEEE 14 Bus System consists of 14 buses (nodes), 5 generators, 11 loads, 16 lines, 5 transformers and one shunt capacitor.

1.12.10 Appendix B

This appendix shows all the engineering configuration settings of the SEL-487E and SEL-751A IEDs. The configuration provides the detailed information of the harmonic blocking protection scheme.

1.13. Conclusion

This chapter provided the research questions, the awareness of the research problem, research aim and objectives and the research methodology.

Chapter Two presents an extensive literature review of the various methodologies used to detect the transformer magnetizing inrush currents. Digital signal processing algorithms, IEC 61850 GOOSE applications and hardware-in-the-loop simulations for the protective relaying system are reviewed.

CHAPTER TWO
LITERATURE REVIEW

2.1 Introduction

A power transformer is a vital and expensive component for power systems. The power transformer protection is provided in general by digital protective relays, and they are appropriate for transformers of all applications.

A literature survey has revealed that different transformer connections and configurations, inrush current, current transformer saturation, speed and stability are the factors that make the transformer protection scheme complicated. Making use of digital technology, researchers have made progress in developing artificial intelligence algorithms for microprocessor-based relays.

Transformer magnetizing inrush current usually flows for a short period in the system until flux conditions are back to normal when a transformer is energised. It is first due to energisation of an unloaded transformer or voltage recovery (Blume L.F., 1951) and (Karsai K. et al., 1987). The inrush current resembles the internal fault, and its amplitude can be as high as a short-circuit current, for this reason, it is necessary to study and analyse it under various conditions in order to apply the settings of a protective relaying system for transformers (Jamali M. et al., 2011).

The literature review provides the investigation which includes the transformer protection for internal and external faults, digital signal processing algorithms for power transformer protection, IEC 61850 standard-based protection schemes for power transformers and hardware-in-the-loop simulation for protective relay testing.

The first section of the literature review investigates transformer internal and external faults in a power transformer. The investigation provides the review summary of the following internal faults such as earth faults, core faults, inter-turn faults, phase-to-phase faults and transformer tank faults. The external faults such as overloading, system faults, overvoltage and under frequency operation are reviewed.

The second section of the review provides the application of discrete Fourier and wavelet transform techniques for the protective relaying system. The literature review of the digital signal processing algorithms such as artificial neural network, fuzzy logic,

artificial intelligence-based algorithms for the power transformer protective relaying system is provided in that section.

The last section of the literature review provides the overview of the IEC 61850 standard for substation, automation system for monitoring, protection and control of the power systems using the digital relaying systems. This section reviews the IEC 61850 standard-based protection schemes for power transformers. And finally, the hardware-in-the-loop simulation review such as open loop and closed loop testing using the IEDs and RTDS is investigated in this chapter.

2.2 Literature review overview

Figure 2.1 provides a graph for the number of papers reviewed starting from 1931 up to 2018. These papers are selected according to the field of protection in power systems and focusing on the history of power transformer protection.

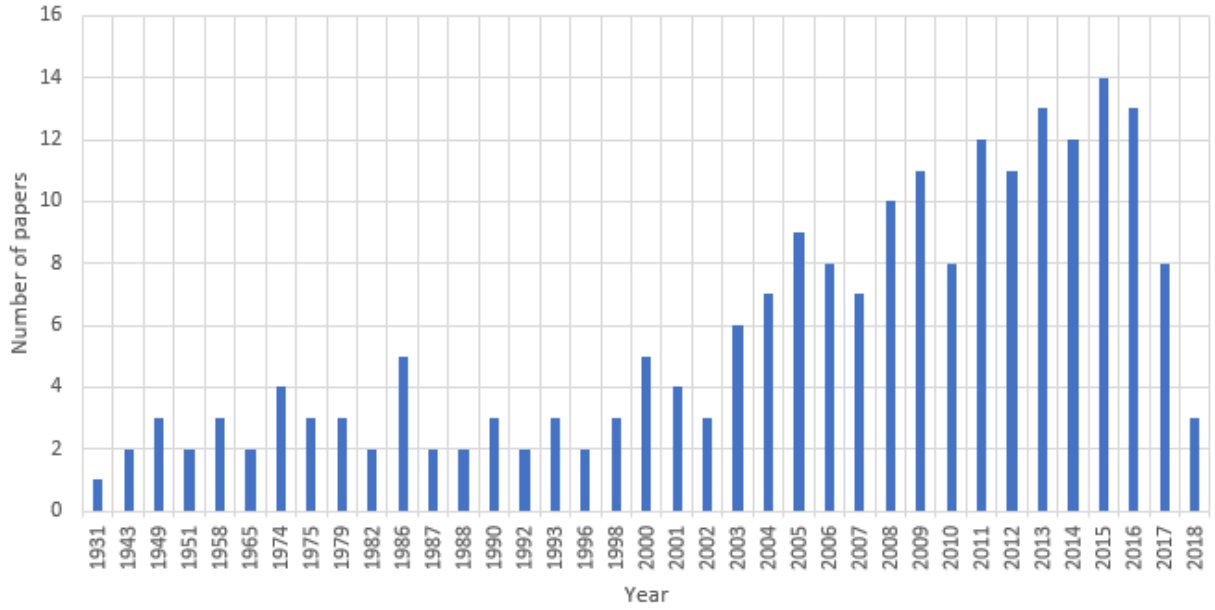


Figure 2.1: Number of papers versus publication years

From the graph above, it can be seen that from the year 1931 up to August 2018. The literature review list has two hundred and eleven papers from journals, books, standard and user manuals that focus on the field of transformer protection. The graph also shows that during the years 2014, 2015 and 2016 the number of transformer protection published papers reaches its peak. In the year 2000, the research investigation on the digital protection for power transformer started to increase. After 2000, the researchers

constantly focused on the digital protection for the transmission lines and transformers. Because of the cost, the distribution transformers were neglected.

The internal transformer faults versus the number of papers published are shown in Figure 2.2.

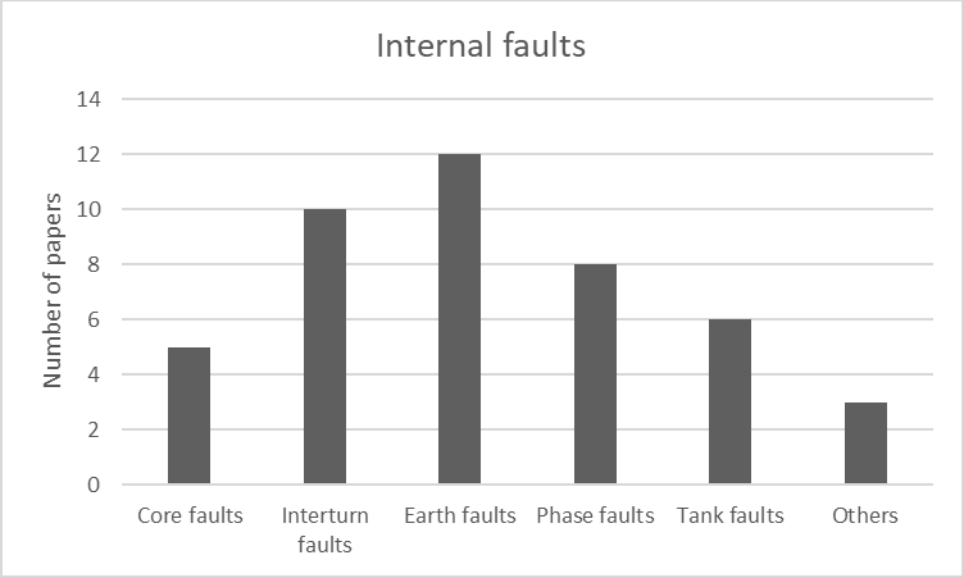


Figure 2.2: Internal faults versus the number of papers

Figure 2.3 shows the reviewed number of papers versus type for transformer external faults.

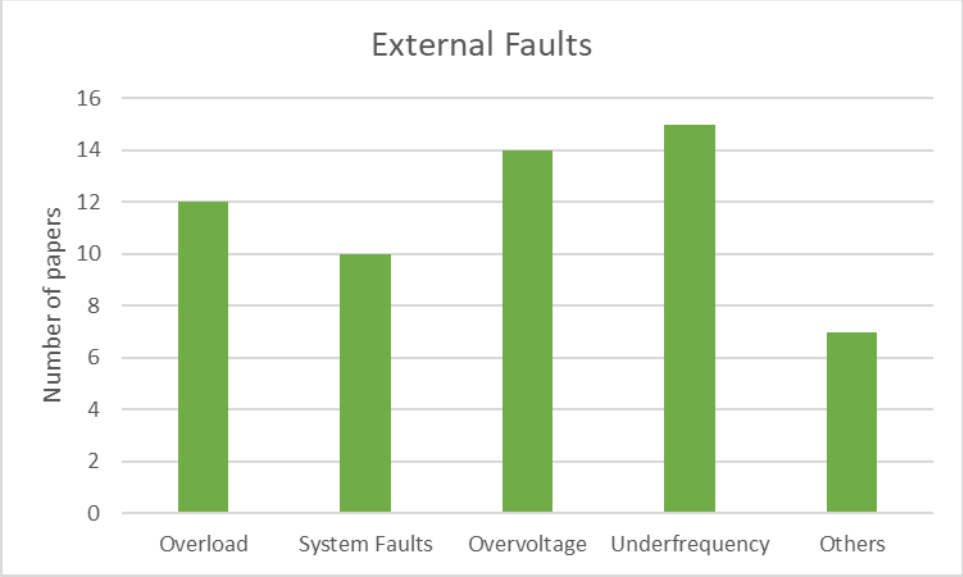


Figure 2.3: External faults versus the number of papers

Figure 2.4 shows the computational intelligence techniques used in the transformer protective relaying system versus the number of papers.

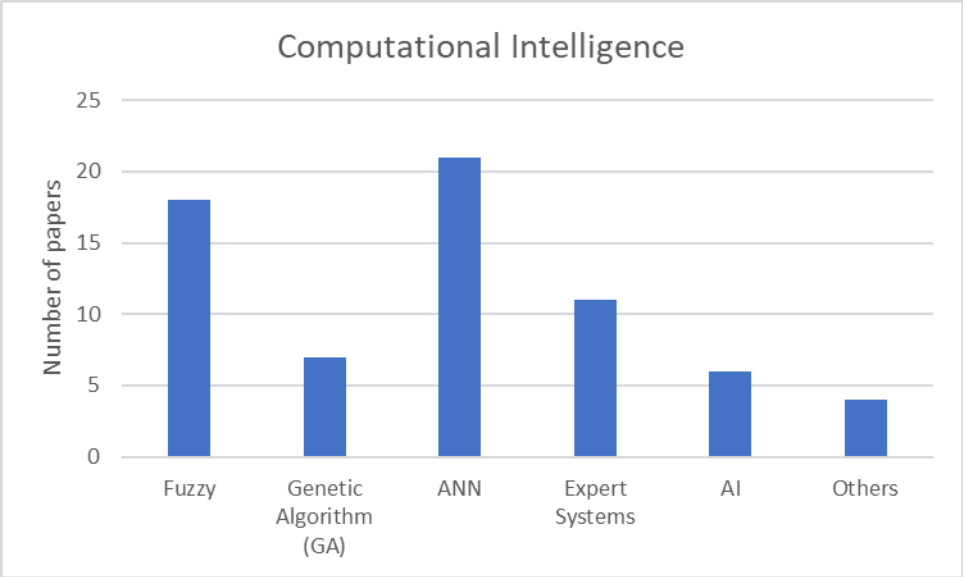


Figure 2.4: Computational intelligence techniques versus the number of papers

The IEC 61850 standard-based protective relaying system versus the number of papers reviewed is shown in Figure 2.5.

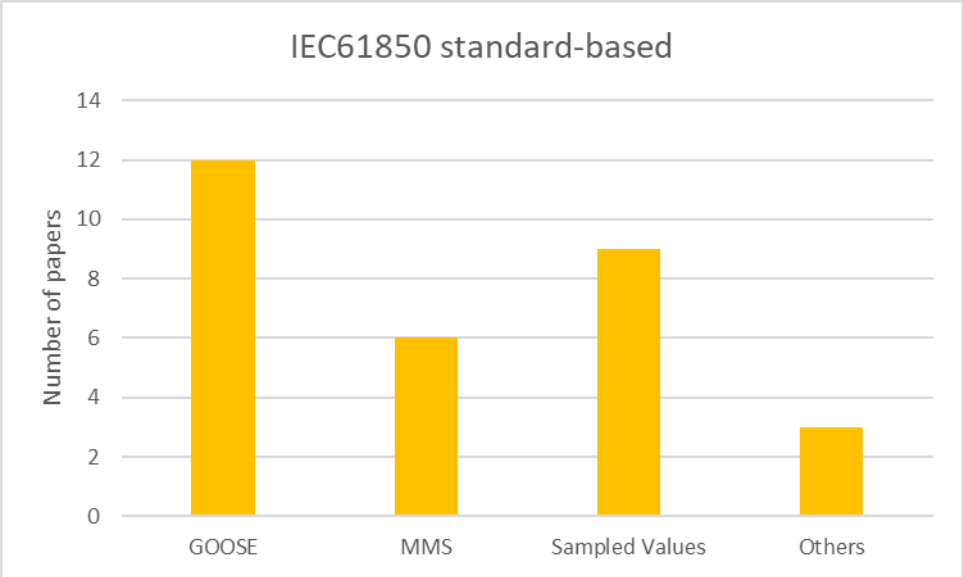


Figure 2.5: IEC61850 standard-based protective relaying system versus the number of papers

2.3 Transformer internal and external faults

The stability of the power system depends on the unfailing operation of several individual components within the network. Transformers are one of the essential and vital units in the transmission and distribution levels of a power system. It is exposed to many different types of faults which may cause interruptions in power supply; which therefore, result in severe economic losses as well as social impacts (Thangavelan M. et al., 2015).

A short circuit can be defined accordingly to the following three characteristics (Prévé, 2006). They are:

1. Their origin, it can be happening due to the mechanical, electrical and operating error such as closing a switching device by mistake.

2. Their location, the short circuit may be generated inside or outside of equipment.

3. Their duration

Faults in power transformers are generally classified into internal and external faults. Internal faults are:

- Winding failures due to short circuits (turn-turn faults, phase-phase faults, phase-ground, open winding)
- Core faults (core insulation failure, shorted laminations)
- Terminal failures (open leads, loose connections, short circuits)
- On-load tap changer failures (mechanical, electrical, short circuit, overheating)
- Transformer tank faults

External faults are abnormal conditions such as over fluxing, overloading, overvoltage and system faults.

Table 2.1 provides possible fault conditions in a power transformer and their protection philosophy.

Table 2.1: Transformer faults and protection philosophies

Internal faults conditions	Protection philosophy
Winding phase-phase, phase-ground faults	Differential (87T), overcurrent (51,51N), restriction ground fault protection (87RGF)
Winding inter-turn faults	Differential (87T), Buchholz relay
Core insulation failure, shorted laminations	Differential (87T), Buchholz relay, sudden pressure relay
Tank faults	Differential (87T), Buchholz relay, tank-ground protection
External faults conditions	**Protection philosophy**
Overloads	Thermal (49)
Overvoltage	Overvoltage (59)
Over fluxing	Volts/Hz (24)
External system short circuits	Time overcurrent (51, 51G), instantaneous overcurrent (50, 50G)

2.3.1 Internal fault

Transformer internal faults can arise from the deterioration of winding insulation due to overheating or mechanical failure. When there is an internal fault, the transformer must be disconnected as fast as possible from the system because a prolonged arc in the transformer may cause oil fire (Mehta, V. and Mehta, R., 2009). Therefore, a protective relaying system is very necessary for internal faults.

A fault on a transformer winding is controlled in magnitude by the following factors:

- Source impedance
- Neutral earthing impedance
- Transformer leakage reactance
- Fault voltage
- Winding connection

One of the most successful methods for power transformers protection is the differential protection. The differential relay compares the currents measured by the current transformers on the primary and secondary sides of the power transformer. This scheme is based on the principle that the current entering the transformer under normal conditions is equal to the current leaving it. If a differential current exists, the relay will produce a trip signal to trip both circuit breakers simultaneously on the primary and secondary sides of the power transformer.

In 1941, author (Hayward, 1941) proposed a new type of relays using the principle of harmonic restraint, which can distinguish between the magnetizing-inrush current and the internal fault current by their difference in the waveform shape. Authors (Sachdev et al., 1989) proposed a new digital algorithm to detect winding faults in single-phase and three-phase transformers. This algorithm is suitable to measure winding currents. Various operating conditions were simulated to test the algorithm. In 1997, (Yabe, 1997) presented a new method to discriminate internal fault current from inrush current. To avoid unnecessary trip caused by the magnetizing inrush current, the second harmonic component is used to block the differential relays on the power transformers. The next section describes the internal faults with the different types of transformer connections.

2.3.1.1 Internal phase to phase faults in power transformer

Phase to phase fault between two different phases or three-phase fault affects each of the three phases equally. These are very severe faults and infrequently occur in power transformers (Tarang Thakur, 2016). This causes high currents to flow into the transformer, and this will require the operation of the protective equipment to prevent the damage to the power transformer.

Phase to phase and three-phase faults in the power transformer are not very frequent. If such a fault does happen, it will give rise to a considerable current to operate instantaneous overcurrent relay on the primary side as well as the differential relay (Alstom Grid, 2011).

According to the author (Prévé C., 2006), line to line make up 15% and double line to ground and three-phase faults make up 5% each of power transformer faults.

2.3.1.2 Internal earth faults in a star connected winding with neutral point earthed through an impedance

The most common internal faults in power transformers are earth faults according to the authors (Horowitz & Phadke, 2008). Author (Prévé C., 2006) mentioned that the most common internal faults in the power transformer are earth faults which make up to 80% of power transformer faults.

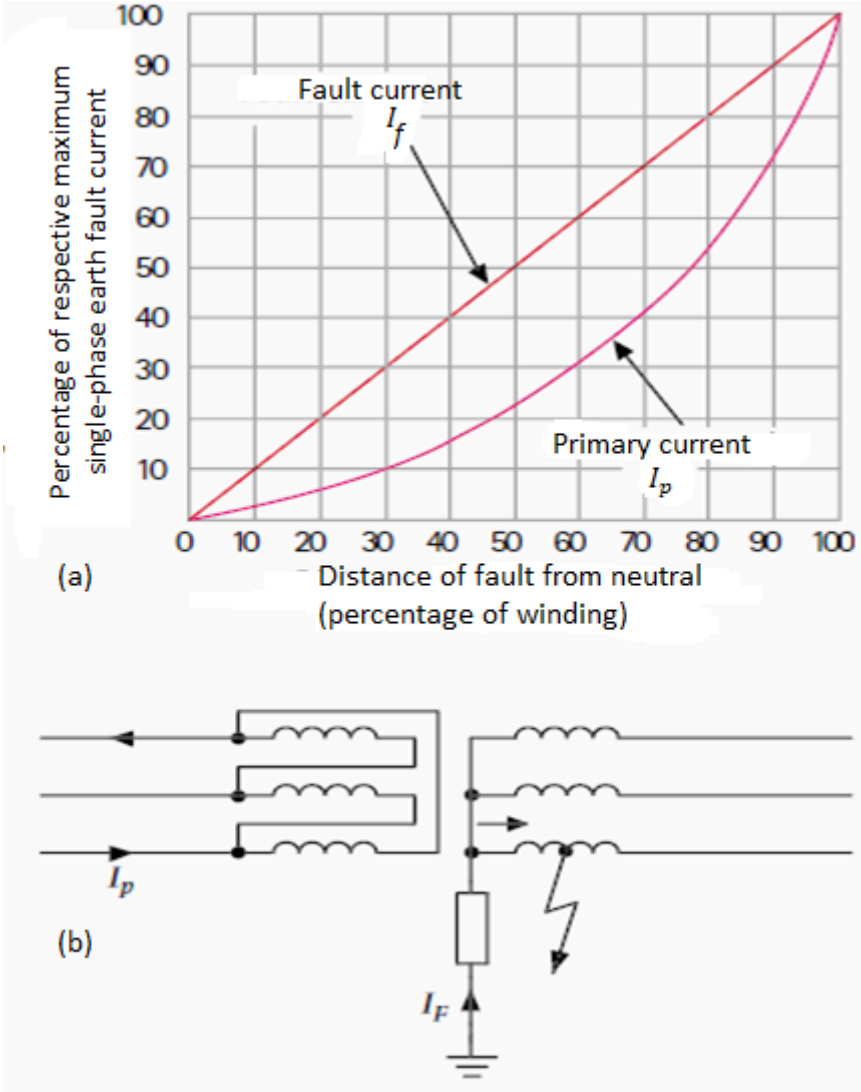


Figure 2.6: Earth fault current in resistance-earthed star winding (Alstom Grid, 2011)

The winding earth fault current depends on the earthing impedance value and is also proportional to the distance of the fault from the neutral point as shown in Figure 2.6, since the fault voltage will be directly proportional to this distance. (Alstom Grid, 2011). Therefore, the corresponding primary current will depend on the transformation ratio

between the primary winding and the short-circuited secondary turns. This also varies with the position of the fault, so that the fault current in the transformer primary winding is proportional to the square of the fraction of the winding that is short-circuited.

In the characteristic curve shown in Figure 2.6 above, the x-axis represents the distance of the fault from neutral in percentage and y-axis represents the maximum single-phase fault current in percentage (I_f).

The earth fault current is shown in Figure 2.6(a) where the primary current is approximately proportional to the square of the fraction of winding short-circuited by fault position and neutral of the winding. A variation of fault current with respect to neutral point is shown in Figure 2.6(a). The fault current increases with respect to the increase in the distance from the neutral point.

Figure 2.7 shows the differential protection combined with a restricted earth fault for an earthed or a limiting impedance earthed transformer.

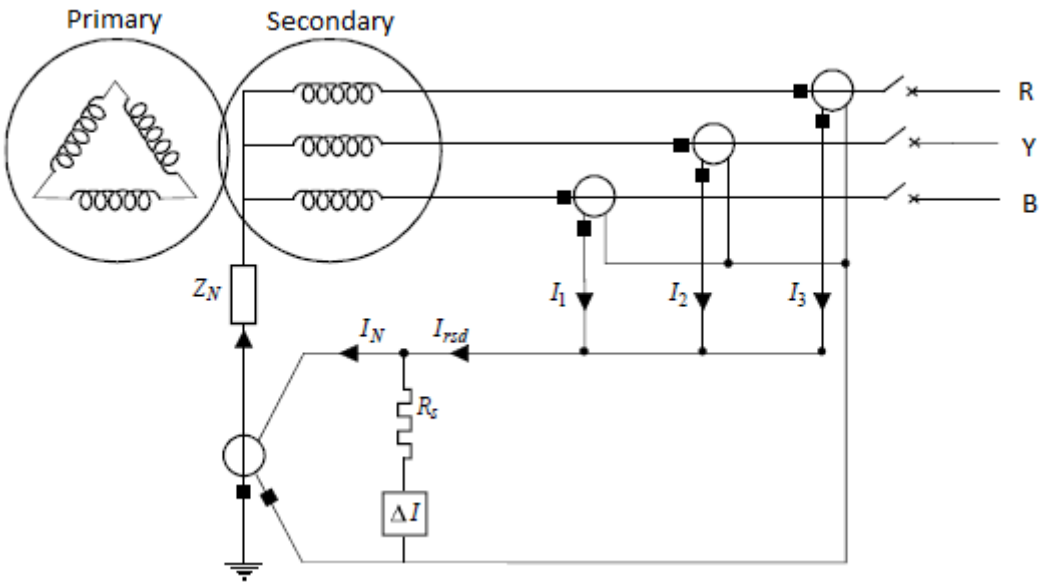


Figure 2.7: The restricted earth fault differential protection of a directly earthed transformer (Prévé C., 2006)

During normal operating conditions, the sum of the currents of the three phases is equal to the residual current Irsd. It is also equal to the earth fault current flowing through the CTs as shown in Figure 2.7.

2.3.1.3 Internal earth faults in a star connected winding with neutral point solidly earthed

In this particular case, the earthing impedance is ideally equal to zero. The fault current is controlled mainly by the leakage reactance of the winding, which varies in a complex manner with the position of the fault. The variable fault point voltage is also an essential factor, as in the case of impedance earthing. For faults close to the neutral end of the winding, the reactance is very low, which results in the highest fault currents. (Alstom Grid, 2011).

Figure 2.8 below shows the differential protection combined with restricted earth fault for a solidly earthed transformer.

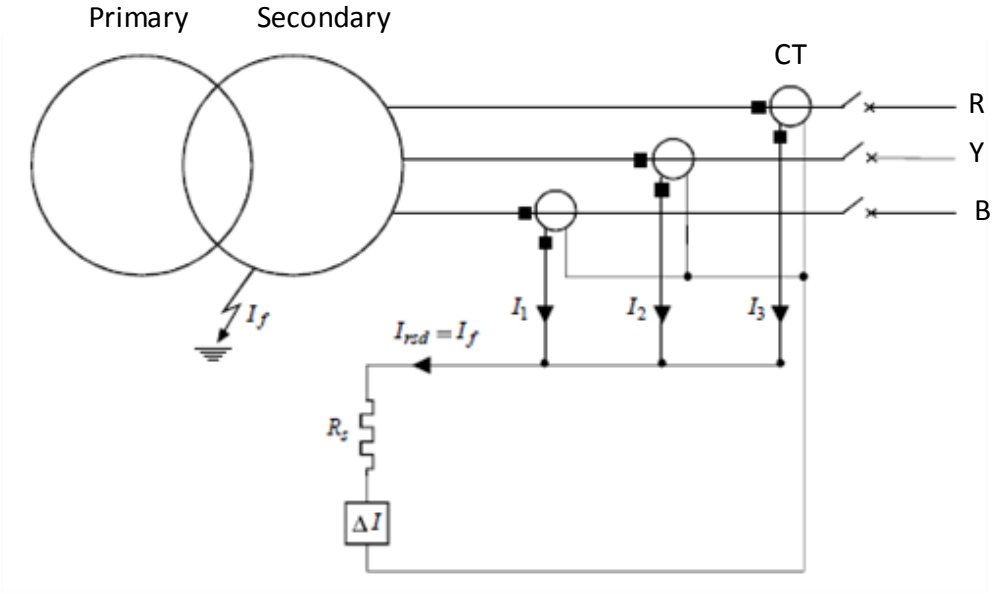


Figure 2.8: Restricted earth fault differential protection for a solidly earthed transformer (Prévé C., 2006)

When there is a ground fault outside the transformer protected zone, the residual current Irsd is zero, and there will be no current circulating in the differential relay. And when there is a ground fault inside the transformer protected zone, the fault current is equal to the residual current and therefore, there will be a current flowing in the differential relay.

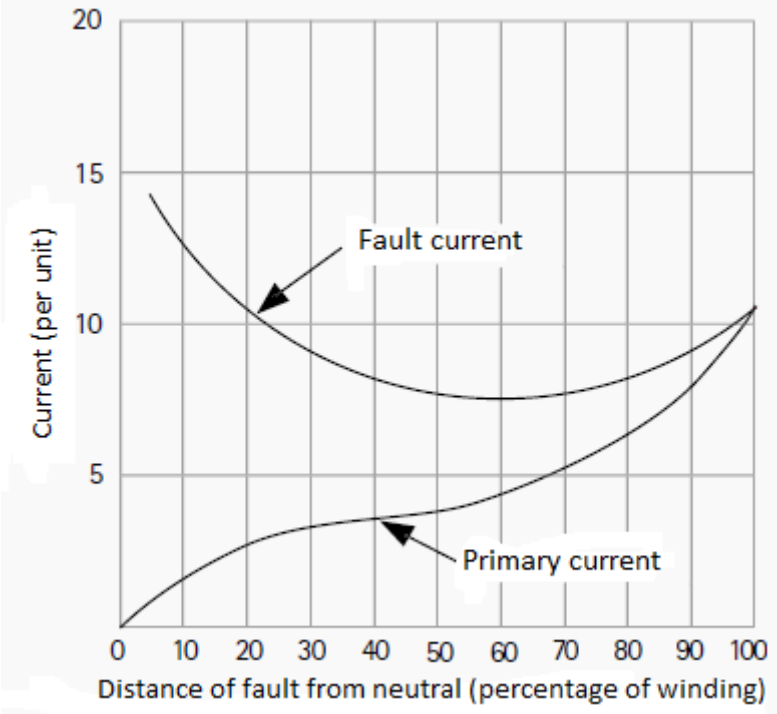


Figure 2.9: Earth fault current in solidly earthed star winding (Alstom Grid, 2011)

The variation of fault current with fault position is shown in Figure 2.9. For secondary winding faults, the primary winding fault current is determined by the variable transformation ratio; as the secondary fault current magnitude stays high throughout the winding, the primary fault current is large for most points along the winding.

2.3.1.4 Delta-connected winding

No part of a delta-connected winding operates with a voltage to earth of less than 50% of the phase voltage. The range of fault current magnitude is, therefore, less than for a star winding. The actual value of fault current depends on the method of system earthing; it should also be remembered that the impedance of a delta winding is particularly high to fault currents flowing to a centrally placed fault on one leg (Alstom Grid, 2011). The impedance can be expected to be between 25% and 50%, based on the transformer rating, regardless of the normal balanced through-current impedance. (Alstom Grid, 2011).

Figure 2.10 below shows the scheme of the Merz-Price circulating-current used for the protection of a three-phase power transformer with delta-to-delta connection against internal faults (phase-to-phase and phase-to-ground). The CTs are connected in star on

both sides of the transformer. Such connections are made because of the phase difference compensation between the primary and the secondary of the power transformer (Mehta, V. and Mehta, R., 2009).

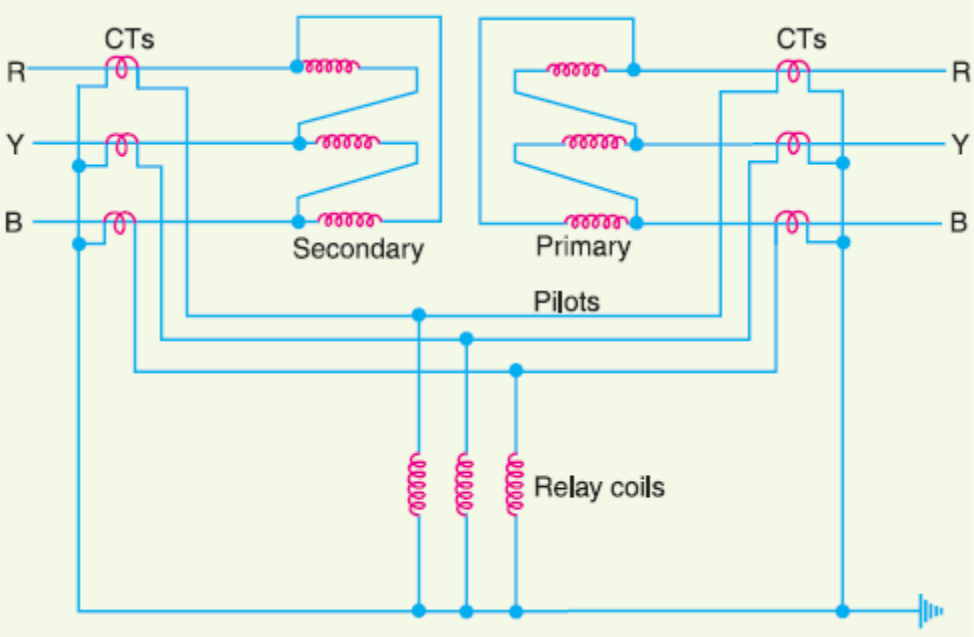


Figure 2.10: Three-phase delta/delta transformer protection connection (Mehta, V. and Mehta, R., 2009)

During normal operating conditions, the secondary currents of the CTs must be identical. Thus, the currents entering and leaving the pilot wires at both sides of the transformer must be identical, and no current should flow through the relay coils. When a phase-to-ground or a phase-to-phase fault occurs, the secondary currents of CTs will no longer be the same, and a differential current will be flowing through the relay coils which will operate the breakers on both sides of the transformer. The region between the CT on the primary side and the CT on the secondary side of the power transformer defines the protected zone

2.3.1.5 Literature review on the differential protection schemes using harmonic restraint methods

Author (Tripathy M. et al. 2005), provides five different methods, namely, (1) Harmonic Restraint (HR), (2) conventional Waveform Identification (WI), (3) Fuzzy logic, (4) Wavelet analysis, and (5) Artificial Neural Network (ANN) to discriminate between magnetizing inrush and internal fault conditions.

Harmonic Restraint is a typical way of restraining a trip. It is assumed that magnetizing-inrush contains a high level of second harmonic currents which is the HR principle of operation. The HR method uses the magnitude of the second harmonic in the differential current and compares it to the magnitude of the fundamental frequency component. The tripping of the differential element is blocked as soon as the ratio exceeds the set threshold.

The HR method (Sidhu T.S. and Sachdev M.S., 1992) is based on the fact that the second harmonic (sometimes fifth) component of the magnetizing inrush current is considerably larger than a typical fault current.

The authors (Phadke A.G., and Thorp J.S., 1983) proposed a flux-restrained differential current for power transformer protection. In 1990, (Verma H.K. and Kakoti G.C., 1990) presented an algorithm, based on HR, using discrete hartley transform. Different advanced digital filtering algorithms such as Kalman filtering (Murty Y.V. and Smolinski W.J., 1990), Fourier-based method (Rahman M.A. and Jeyasurya B., 1988), etc., are used in HR differential protection schemes. However, the HR-based method sometimes fails to prevent false tripping due to high second harmonic components during internal faults. Low second-harmonic components are generated during magnetizing inrush of the transformers having modern core material (Shin M.C. et al., 2003). Therefore, the techniques based on detection of the second/fifth harmonic component may not be a proper method to discriminate between the inrush and fault condition on power transformers.

2.3.1.6. Transformer inter turns fault

The literature review investigation shows that 70% to 80% of the modern transformer failures are due to winding inter-turn faults (Gajic Z., 2012). Winding inter-turn faults occur as a result of winding insulation failure due to thermal, electrical and mechanical stress, leading to turns of the same winding shorting each other. If this fault is not cleared as quickly as possible, it may develop into a more severe and costly to repair fault involving the transformer iron core.

The author (Gajic Z., 2012) proposes that turn to turn faults can be detected using the Buchholz relay, however the time stamp to detect the internal fault is in the range of hundreds of milliseconds to even seconds, which allows the fault to develop into a much more serious fault (Gajic Z., 2012). According to the author (Rockefeller G., 2007), phase differential relays may detect a winding inter-turn fault, owing to the fact that it

alters the transformer turns ratio creating an unbalance. However, this unbalance is not detectable for a relatively few numbers of shorted turns.

The voltage stresses between winding turns become so large, it cannot sustain the stress, causing insulation failure between inter turns of the transformer winding. Very large number of power transformer failure arise from fault between turns. Inter turn fault may also occur due to mechanical forces between turns originated with an external short circuit (Rockefeller G., 2007).

Figure 2.11 shows the corresponding data for a typical transformer of 3.25% impedance with the short-circuited turns symmetrically located in the centre of the winding. It is observed that a small inter-turn short-circuit results in a heavy fault current and the primary current is small, because of the high ratio of transformation between the whole winding and the short-circuited turns. It may cause some consequent problems such as melting and deformation of the winding, deterioration of insulation due to the temperature rising and it may also cause explosions.

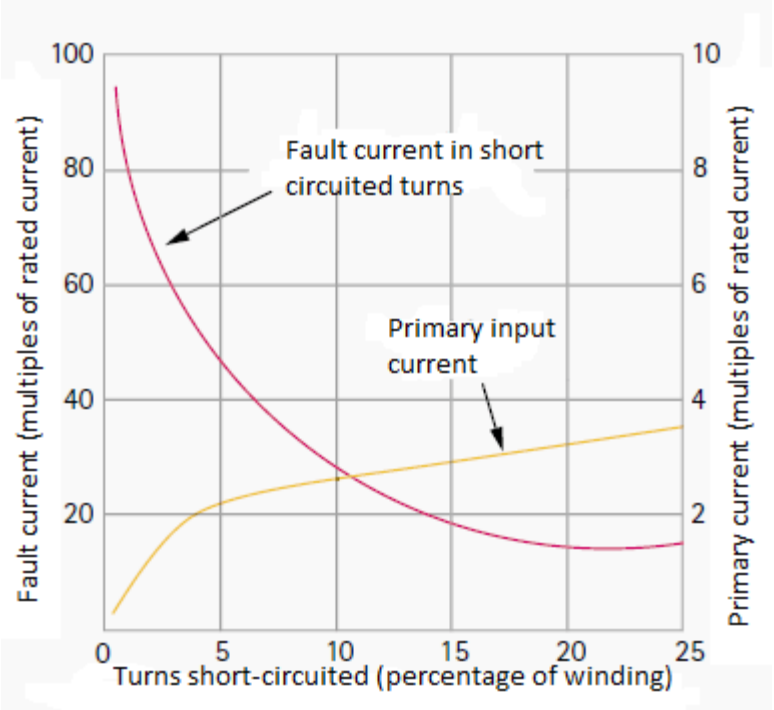


Figure 2.11: Interturn fault current with the number of turns short-circuited (Alstom Grid, 2011)

In reference (Afkar H. and Vahedi A., 2015) the authors used Frequency Response Analysis (FRA) to detect inter-turn faults within a power transformer. The FRA algorithm compares the frequency response of the transformer during faulted and healthy

conditions and determines whether or not a fault exists within the transformer. According to reference (Afkar H. and Vahedi A., 2015), each transformer winding has a unique transform function and frequency response which is very sensitive to changes that occur in the structure of the winding such as resistance, capacitance or inductance variation. Bearing in mind that these changes merely happen because of a winding fault inside the power transformer, it is possible to detect inter-turn faults by continuously monitoring the frequency response of each winding.

The authors (F. Haghjoo and M. Mostafaei, 2016) proposed the detection of the interturn faults by monitoring the flux linkage on each phase winding. Linkage Flux Based (LFB) method utilizes separate multi-turn windings search coils infolded around the core legs of the transformer with precise intervals to measure the linkage magnetic flux in different places. Under no fault conditions, the core flux passing each transformer leg induces equal voltages in all sensing coils installed on the same leg, however once inter-turn faults occur the core flux in the faulty region reduces. This result is an increase in the leakage flux, which in turn results in different voltages being induced in the sensing coils wound on that specific core. The proposed a method (LFB) does not suffer from the effects of magnetizing inrush, CT saturation, tap changer operation and CT transformation errors. However, it does not offer much flexibility in the sense that for large transformers where the method needs to be incorporated into the transformer from the design phase, any problems experienced with the system means that the transformer needs to be overhauled and sent back to the factory to have its windings removed and the problem sorted out, as compared to the normal differential where a problem experienced say with the CTs would merely require a change of CTs and the system is back online (F. Haghjoo and M. Mostafaei, 2016).

According to authors (González G.D. et al., 2004), when a turn to turn short circuit occurs in a transformer, a circulating current is established in the delta winding, and superimposes itself over the positive sequence current. The zero-sequence current, however, is not in phase with any of the positive sequence currents or voltage, since it widely changes as the short circuit resistance drops. It then follows that the zero-sequence current is nearly in opposing phase with voltage in the damaged coil when the short circuit resistance is relatively high value. Therefore, by matching this circulating zero sequence current to the positive sequence current, a turn to turn fault may be detected. However, the authors do not explain how to implement this scheme for an ungrounded wye transformer.

The author (Gajic Z., 2008) proposed that the phase differential element is incapable of detecting low-level faults, such as turn to turn faults. The author, therefore, recommended that if the differential element would look into the phase angle shift between the two currents measured at the transformer terminals, minor faults such as turn to turn would be detected. The author proposed as low as 3 to 5 degrees, yielding a very sensitive turn to turn fault detection.

2.3.1.7. Transformer core fault

In any portion of the core, if the lamination of the core is damaged, or bridged by any conducting material, sufficient eddy current is caused to flow; hence, this part of the core becomes overheated. Occasionally, insulation of bolts (used for tightening the core lamination together) as shown in Figure 2.12 fails, it also permits sufficient eddy current to flow through the bolt causing overheating (Alstom Grid, 2011).

Figure 2.12 shows a three-phase transformer with each phase placed in a different column.

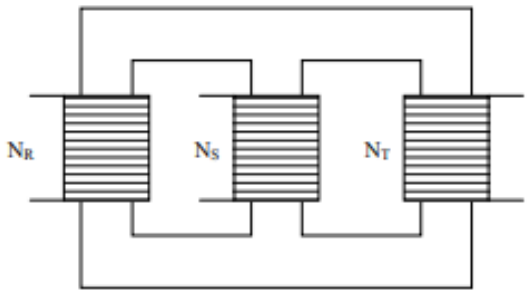


Figure 2.12: Three-phase transformer core (Prévé C., 2006)

The additional core loss, although causing severe local heating, does not produce a remarkable change in input current and cannot be detected by the normal electrical protection. However, it is crucial to detect the core fault before a major fault can be created. In an oil-immersed transformer, core heating sufficient to cause winding insulation damage also causes breakdown of some of the oil with an accompanying evolution of gas. This gas escapes to the conservator and is used to operate a Buchholz relay.

The authors (Pleite J. et al., 2006), proposed the diagnosis of a core fault in a power transformer using Frequency Response Analysis (FRA) technique. The authors developed a three-phase magnetic core model that provides the relations among the raw frequency response and the different parts inside the three-phase power transformer.

With this model, several effects of the magnetic core are recognised through its various parameters. This model has the capability of offering a physical meaning of the different effects inside the transformer. In this way, the internal state of the transformer and the information inside the transformer can be known employing an external measurement using the Frequency Response through the proposed model.

According to the authors (Pandya A. and Parekh B., 2014), the core phase winding short faults can be detected using Sweep Frequency Response Analysis (SFRA) technique. The authors first tested the healthy transformer using SFRA, and they confirmed that the SFRA technique traced power transformer healthy condition. To carry out the practical simulation of the transformer damages, the authors performed nine simulation tests on the power transformer at TAP 1 for the phase winding short circuit fault. The SFRA technique can effectively trace and detect the core phase winding short circuits in star connected and delta connected transformers. The only problem with this technique is that, the fault is falsely detected in all the phases in delta connected transformer, when the fault only occurs in one phase of the winding and the core.

2.3.1.8. Transformer tank fault

Loss of oil through tank leaks ultimately produces a dangerous condition, either because of a reduction in winding insulation or overheating on load due to the loss of cooling (Alstom Grid, 2011). Overheating may also occur due to prolonged overloading, blocked cooling ducts due to oil sludging or failure of the forced cooling system.

The mineral oil is used to cool the power transformers and to dissipate the heat loss to the outside air which is generated from the core and winding parts. If the oil or the other insulation material loses its dielectric properties due to oil pollution or ionization, an electrical arc may occur in an oil-filled transformer, and a large volume of gas is generated by the arc decomposing the oil under high heat, this results in the rapid increase of tank pressure (Kawamura T., et al, 1988). This produces pressure waves that spread inside the oil and interact with the tank structure. This wave and structure interaction ultimately leads to the tank rupture and possible transformer explosion.

To protect the transformer from tank faults, the authors (Janicek F. et al., 2004) suggest a protection principle which consists of connecting the transformer frame with the earthing system through a current transformer (CT) as shown in Figure 2.13. The overcurrent protection relay is then connected to the CT output terminals. This protection scheme will operate in case of any fault; when there is voltage on the transformer frame,

the current will flow from frame to ground through the CT (Janicek F. et al., 2004). Therefore, the transformer tank must be insulated from the ground.

Figure 2.13 shows the tank earth leakage protection of the transformer. This type of transformer protection is designed to protect a transformer against internal faults between a winding and the frame. Author (Prévé C., 2006) recommends this scheme for the transformer of more than 5 MVA power rating. This type of protection used an overcurrent relay, and it is installed on the transformer frame earthing connection as shown in Figure 2.13.

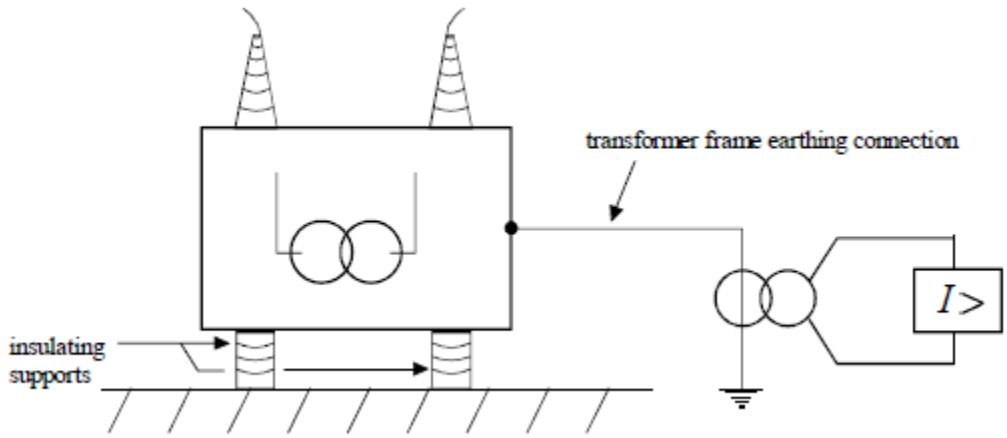


Figure 2.13: Transformer tank earth leakage protection (Prévé C., 2006)

2.3.1.9. External faults in power transformer

In the power transformer protection, through-fault is the system faults that are outside the transformer protected zone. It is a recognised perception that the protection zone for the transformer differential relay is characterised by the location of the CTs secondaries (Talebi M, and Unludag Y., 2018). This section discusses the transformer external faults due to i) overload, ii) system faults, iii) overvoltage and iv) under frequency.

i. Overload

Transformer overloads can be caused by the power systems events and operator actions (Ferrer H.J. and E.O. Schweitzer III, 2010). More often, this is caused by the increase in the number of instantaneously loads connected to the transformer or by the increase of the power demand for one or more loads. Transformer overload increases the copper losses in transformer windings which subsequently causes the temperature to rise. Transformer overload must have limited periods.

According to the authors (Yasuoka J. et al., 2005), a transformer can be overloaded for the periods lasting from 15 minutes to 4 hours which is the allowable short-term overload. These periods allow the transformer to be cooled naturally.
Author (Prévé C., 2006), proposed several specific protection schemes against overloads. They are:

- The temperature monitoring of the dielectric for liquid-insulated transformers (ANSI code 38-49T); the alarm threshold must be set at 80°C. De-energisation or the off-loading threshold of the power transformer must be set at 90°C;
- The windings temperature of a dry type power transformers (ANSI code 38-49T), this is done by using a thermal probe detecting an abnormal rise in temperature;
- Thermal overload protection (ANSI code 49)

ii. System faults

The system faults may occur in a single-phase to ground, phase-to-phase or three-phase-to-ground of the electrical power systems. The fault current overheats the transformer and causes the copper loss in the feeder connected to the transformer. This copper loss causes an overheating inside the power transformer. The same thing with large through-faults which produce severe mechanical stresses in the power transformer. There is no protective relaying provided for these system faults, and generally, thermal equipment is used to sound the alarm or control the banks of fans.

iii. Overvoltage

Overvoltage conditions in a transformer can be divided into two types (Alstom Grid, 2011): transient surge voltage and power frequency overvoltage. Transient overvoltages arise from events such as switching operation, system faults, and lightning disturbances which are accountable to create inter-turn faults.

Power frequency overvoltage is caused by the sudden disconnection of the load. And in its turn, the power frequency overvoltage creates an increase in stress on the insulation which is proportional to the flux increase. The flux rise effect then establishes the iron loss rise and an excessively increase in magnetising current. This leads to the overheating of the core bolts and damages the winding insulation.

To protect the power transformer against overvoltages, the overvoltage protection (ANSI code 59) is used. The protection element is triggered if one of the phase voltages is

higher than the set threshold (Vset). According to (Prévé C., 2006), Vset should be set at 1.1 Vn with a time delay of approximately 1 second.

iv. Under frequency

Under frequency is caused by the power supply frequency variations, overloads if a limited power source is supplying the network, generator frequency regulator when it is faulty and when a generation plant is cut off from an interconnected network (Prévé C., 2006).

Similar to the overvoltage, when the system frequency is reduced it has an impact with respect to flux density. A power transformer is permitted to work with a certain amount of overvoltage and the equivalent frequency increase, but the transformer should not be operating with a high voltage input at a low frequency (Alstom Grid, 2011).

Under frequency protection scheme (ANSI code 81) uses a comparison between a threshold frequency and the network frequency. During overloading conditions, the following procedure to be followed according to (Prévé C., 2006):

- Loads shedding when there is an overload event. This is done by cutting off the power to non-priority consumers;
- The network to be cut up into a few sub-networks to overcome problems that concern the stability of the machines. When this is the situation, it is better to cut off the power supply to the motors;
- The power supply to a plant fitted with large asynchronous motors to be cut off in case of a network micro-cut event.

Table 2.2 provides the overview of the pattern recognition technique for discriminating between the magnetizing inrush current and internal faults in three-phase power transformers.

Table 2.2: Review overview of the pattern recognition techniques for power transformers

Paper	Aim	Artificial Intelligence method used	Protection	Simulation / Hardware implementation	Benefits
Nosseir, A. Attia, A., 2008	Discriminate between the inrush current and the internal fault condition based on the transformer magnetizing characteristics within one short cycle.	A method for discrimination between inrush current and internal faults based on the power transformer magnetization characteristics and Artificial Neural Networks (ANN).	Transformer differential protection	Simulation using EMTP-ATP program on a three-phase transformer.	The proposed method helps the differential relay to recognize inrush and internal fault and provides a trip signal in case of internal faults.
Panda, C., Garlapti, V.K., 2010	A wavelet-based algorithm, for distinguishing between magnetizing inrush and internal faults of the power transformer.	The proposed technique consists of a pre-processing unit based on Continuous Wavelet Transform (CWT) in combination with an Artificial Neural Network (ANN) to detect and classify the faults.	Transformer differential protection	ATP/EMTP	The proposed technique is fairly fast, computationally efficient and intelligent enough to accurately discriminate between magnetizing inrush, normal and faults in the transformer.
Lu, Z. Tang, W. H., 2009	A Morphological Decomposition Scheme (MDS) to discriminate fault current and inrush	The ratio of the Power Spectrum (PS) second harmonic to the PS fundamental based autoregressive process	Differential protection for power transformers.	ATP simulation software	Morphological Decomposition Scheme can distinguish between internal faults and inrush with low second harmonic components.

	current.	is used for inrush identification			
Delshad, M. Fani, B., 2007	Neuro-fuzzy differential algorithm consists of considering the ratio and the difference phase angle of the second harmonic to the fundamental component of differential currents under various conditions.	A new algorithm based on Neuro-Fuzzy for differential protection of the power transformer.	Differential protection of the power transformer	A power system has been modelled in PSCAD/EMTDC, and these obtained results are used to train the neural network. The proposed neural network is a feed forward back propagation network that is simulated by MATLAB software. The proposed Neuro Fuzzy is trained by obtained data from the simulation of the power system under different faults and switching conditions.	This method has high sensitivity to the fault detection and recognizes fault conditions from inrush current conditions about half cycle after the occurrence of disturbance. The proposed algorithm does not have any coefficients or threshold values. But with modern transformers, due to the improvement of core steel. These traditional approaches are likely to mal-operate in case of magnetizing inrush with low second harmonic contents and internal faults with high second harmonic components.
Zengping, Wang Jing, M.A., 2005	Identify the magnetizing inrush current and short circuit current caused by internal faults.	Self-Correlation Function (SSCF) formed with the sinusoidal current. The magnitude of a similar coefficient	Differential protective relays	Electrical Power Dynamic Laboratory (EPDL) is used for simulation. The sampled data are analysed by correlation	This method is useful in distinguishing inrush from internal faults of a transformer.

		can distinguish the short-circuit current and the inrush current		function principle in the Digital Signal Processing (DSP) and the self-correlation function of the sampled data is calculated.	
Chen, MingJie Li, G., 2008	To discriminate between low-level internal faults and the magnetizing inrush.	Transformer protection based on the artificial neural network model.	Transformer differential protection.	EMTP simulations and the MATLAB Neural Network Toolbox.	The proposed method can recognise internal faults within a half cycle of their occurrence, with apparent fault features and less threshold value.
Feng, X. L. Tan, J. C., 2006	Transient current signals at both sides of a transformer are first captured and then analysed using wavelet transform, from which the Modular Maxima (MM) are derived and subsequently used to discriminate between magnetizing inrush current and fault currents.	A new approach for transformer protection based on wavelet transformation	Transformer differential protection	Real-Time Digital Simulator (RTDS) simulations were carried out to cover various transformer operational conditions such as magnetizing inrush with multiple closing angles of a circuit breaker, different fault types on either side of a transformer, fault currents under CTs saturation, during server fault conditions. The wavelet transform	The new wavelet algorithm is simple, reliable, accurate, immune to CT's saturation, and can perform correctly for the worst cases where an internal fault occurs when a transformer is energised without load.

				then analyses the sampled current signals of both sides of a transformer.	
Geethanjali, M. Slochanal, S.M.R., 2005	A new approach for classifying transient phenomena in power transformers is implemented using a differential protection scheme.	ANN architectures were trained using Back Propagation Algorithm (BPA) and combining BPA with wavelet transforms and Neural Networks (WNN).	Transformer differential protection	The wavelet transform is applied for the analysis of power transformer transient phenomena. The proposed scheme has been realised through two different Artificial Neural Network (ANN) architectures (one is used as an Internal Fault Detector (IFD), and another one is used as a Condition Monitor (CM))	Combined WWN provides high operating sensitivity for internal faults and remains stable for other operating conditions of the power transformer.
Abniki, H. Monsef, H., 2010	A new methodology for discrimination between inrush currents and internal faults for a three-phase power transformer.	Inductance-based scheme for power transformer protection. This method calculates the differential inductance of every phase of the transformer and compares it with a threshold.	Transformer differential protection	PSCAD/EMTDC simulation software	The proposed technique can offer responses in protection and accurately discriminate between inrush currents and internal faults. But the method is not fast enough to detect inrush current with low second harmonic components.

Hamilton, Randy, 2013	Analyse factors affecting the second harmonic ratio in inrush current and harmonic restraint methods.	Methods using harmonic restraint, wave-shape recognition, and Artificial Neural Networks (ANN) have been proposed to discriminate magnetizing inrush and internal faults.	Differential protection.	MATLAB/ Simulink simulation software.	The restraint current with harmonic provides good dependability while maintaining the security for differential protection.
Mokryani, G. Haghifam, M. R., 2010	The S-Transform based Probabilistic Neural Network (PNN) classifier for recognition of inrush current.	S-transform is used for feature extraction, and PNN is used for classification.	Transformer differential protection.	Inrush current data and other transients are obtained using EMTP program. Using this method inrush current can be discriminated from other transients such as capacitor switching, load switching and single phase to ground fault.	The simulation results reveal that the combination of S-Transform and PNN can effectively detect inrush current from other events.
Zaman, M.R. Rahman, M.A., 1998	Experimental testing of the Artificial Neural Network based protection for power transformer in order to distinguish between magnetizing inrush and internal fault currents of a power transformer.	Differential protection algorithm is based on Artificial Neural Network (ANN), and it is independent of the harmonic contents of the differential current. The network is trained using ANN back-	Transformer differential protection	The processing is performed using the DS-1102 Digital Signal Processor (DSP). A program is written in C language for this purpose. The software loads the values of the weights and biases of	The method neither depends on the transformer equivalent circuit model nor the harmonic contents of the differential currents. It makes the decision based on current signature verification. For modern transformers with

		propagation algorithm.		the ANN required for the processing of the tripping decision	unpredictable harmonic components, this method would be more effective.
Shi, D. Y. Buse, J., 2011	Discriminating between the magnetizing inrush and the internal fault of a power transformer	Mathematical Morphology (MM) and ANN, is proposed to solve this problem. Firstly, an MM based stage is used to extract shape features from differential currents, then after a scaling pre-processing which removes magnitude information and fed into an artificial neural network (ANN).	Differential transformer protection.	This method has been implemented by using MATLAB and evaluated on the data obtained from PSCAD/EMTDC simulation.	The MM based feature extraction is an effective way to reduce network complexity and increase identification speed.

2.4 Digital signal processing algorithms for protective relaying system

The operation and analysis of signals are carried out by Digital Signal Processing in either discrete or continuous time (Prandoli & Vetterli, 2008). To analyse and select the characteristic features of measured electrical quantities, signal processing is used in power systems.

2.4.1 Application of Discrete Fourier Transform and waveform transform techniques for protective relaying system

The Discrete Fourier transform (DFT) is the most commonly utilised algorithm in Intelligent Electronics Devices (IEDs) for the phasors estimation of the voltage as well as the current signals which the numerical relays use to make necessary decisions. Because the power system is an inductive and resistive combination, during the fault event a decaying-exponential transient component, known as decaying dc offset, is created in the current signal in addition to the fundamental frequency component, harmonics, and noise (Dadash Zadeh M.R. and Zhiying Zang, 2013). A decaying DC offset is described as a signal that is not periodic and has a comparatively wide range frequency spectrum at lower frequencies. Undesirable errors in the form of overshoot and decaying oscillations resulting in the magnitude and angle of the estimated phasor because of the conventional full-cycle DFT which cannot efficiently reduce the lower frequency components (Dadash Zadeh M.R. and Zhiying Zang, 2013).

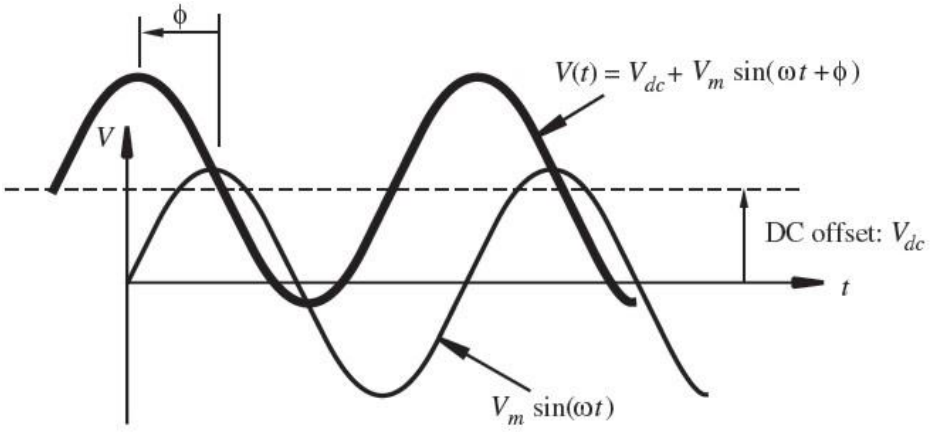


Figure 2.14: Decaying DC offset (Kiprane and Bedekar, 2016)

Voltage waveforms are shown in Figure 2.14 in the steady-state conditions. In these conditions, the current lags the voltage by $90°$ because in power systems the load is

predominately inductive. However, when the switching is at the positive direction, and zero crossing of voltage waveform gives rise to maximum DC offset in the current.

Fault current contains a DC offset component which can affect the performance of the differential relay. Pickup level of the differential relay and its operating time can be affected due to DC offset component. Especially in electromechanical ones which are not digitally embedded with new modern techniques of digital filtering for the removal of the DC component from fault current. A second effect is that there could be a possibility of saturation in CT which may distort the original waveforms (Kiprane R and Bedekar P., 2016).

To extract the fundamental components and second and fifth harmonic contents, there are many algorithms available (Rahman, M.A. and Jayasuryan B., 1988). The Discrete Fourier Transform (DFT) is a powerful tool which could be utilised to extract these components. It could also be used to discriminate accurately between the internal fault and magnetizing inrush currents in power transformers.

2.4.2 Wavelet transform

The authors (Gómez-Morante and Nicoletti D., 1999) introduced for the first time to use the wavelet for differentiating between internal fault and magnetizing inrush current. The scheme is based on the distribution of energy of the signals in both frequency and time domains. For inrush current, the discriminate function is greater than zero. For an internal fault, the discriminate function is smaller than zero. The technique is based on the definition of the discriminant function W(x).

$$W(x) = d_A(x) - d_1(x) \tag{2.1}$$

The classification rule is stated as follows:

$$\text{If } \begin{cases} W(x) < 0 \ classify\ x\ as\ an\ internal\ fault \\ W(x) > 0 \ classify\ x\ as\ an\ inrush\ current \end{cases} \tag{2.2}$$

Figures 2.15 and 2.16 show that the discriminant function W(x) is greater than zero for inrush currents and less than zero for internal fault currents.

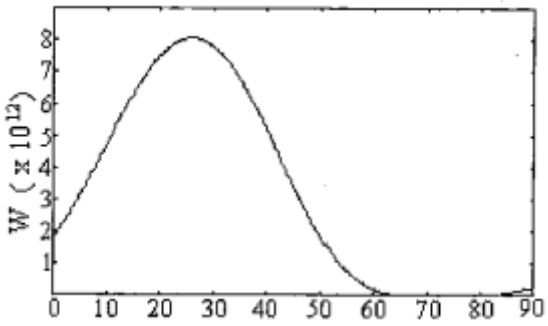


Figure 2.15: Wavelet discriminant function for inrush currents (Gómez-Morante and Nicoletti D., 1999)

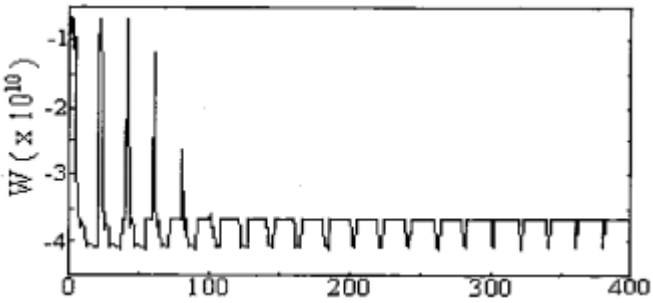


Figure 2.16: Wavelet discriminant Function for internal faults currents (Gómez-Morante and Nicoletti D., 1999)

Author (Eissa M.M., 2005) uses a wavelet packet method to discriminate between external and internal faults to the zone of protection of a power transformer. The proposed technique is also used to distinguish between the internal transformer faults and inrush currents. The prefault voltage (v) and fault current (i) signals are used by the wavelet technique as a directional signal as shown in Figure 2.17.

This wavelet technique is presented in Figure 2.17, one signal SaL is utilised for the technique analysis and the results of feature extraction from the coefficients of the wavelet corresponding to the Input Signal (IS) SaL are calculated at some frequency band (level-3 and db1 wavelet function). The directional signal DS which differentiates between external and internal faults is computed from the coefficient W_{30}. The technique has a negative and a positive threshold value. The technique identifies the external fault in the event that the Directional Signal (DS) is lower than the negative threshold value. And the technique identifies a forward fault, if the DS is higher than the positive threshold value.

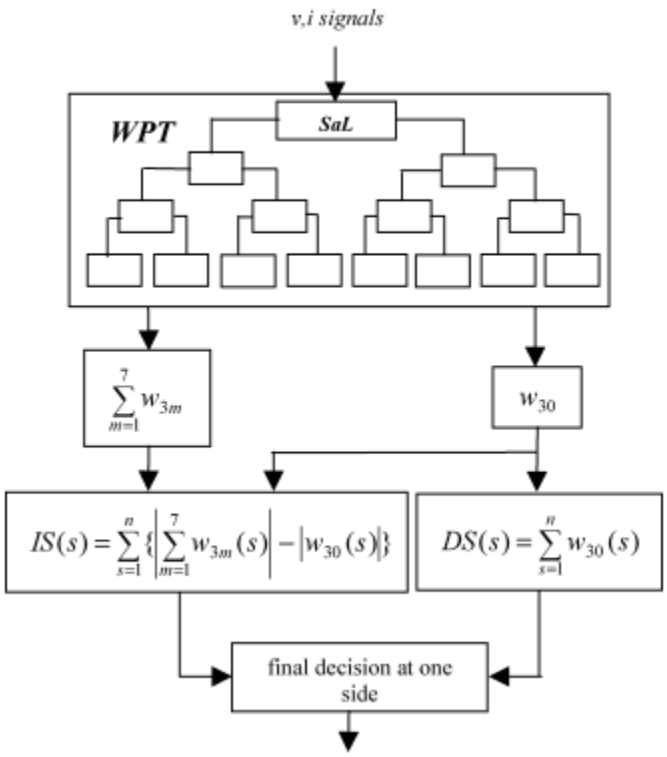


Figure 2.17: Wavelet technique arrangement (Eissa, 2005)

To distinguish between the internal fault and inrush current, a sum of the different coefficients of the wavelet from window 1 to window 7 is used. The sum value is compared with the wavelet coefficient in window 0. The level of the inrush current signal is characterised by this value. For the differentiation procedure, this value is compared with the coefficient of the wavelet W_{30}. Input Signal (IS) is used to discriminate between internal faults and inrush current, and Directional Signal (DS) is used to distinguish between external and internal faults.

Authors (Vahidi B. et al., 2010) and (Rasoulpoor M. and Banejad M., 2013) used correlation method and Discrete Wavelet Transform (DWT) coefficient for transformer differential protection. Offline and online operations comprise the wavelet algorithm. In offline operation of the algorithm, the discrete wavelet transform is utilised to decompose the known signal of the inrush current, and in on-line operation, differential currents are captured at 10 kHz sampling rate for internal fault conditions and inrush current by comparison with the predetermined value. Then the signal which is unknown is decomposed using the discrete wavelet transform. While, authors (Rasoulpoor M. and Banejad M., 2013) proposed a wavelet technique, if the number of dips in each

correlation coefficient is greater than 1.0, it means it is inrush current identification or else it is an internal fault current.

Authors (A.A. Hossam Eldin and M.A. Refaey, 2011) proposed a method for distinguishing the different types of currents in a power transformer. The proposed technique consists of five level of resolution discrete wavelet transform. The third and fourth level coefficients details of the discrete wavelet transform are evaluated by the algorithm.

In order to control the maloperation of a differential protection scheme for a three-phase power transformer caused by the ultra-saturation phenomenon, authors (Noshad B. et al., 2014) presented a wavelet transform method based on Discrete Wavelet Transform (DWT) and Clarke's Transform. The ultra-saturation phenomenon takes place during the energisation of a loaded power transformer. To extract the information of the transient signal in frequency and time domain, the input signals are analysed by Discrete Wavelet Transform (DWT). The energy coefficients and the standard deviation of coefficients are utilised to discriminate between the phenomena of transient in this method. The authors (Oliveira et al., 2014) used DWT based on wavelets coefficient spectral energy in order to distinguish between external and internal faults, inrush currents and emerging internal faults.

The Wavelet Packet Transform (WPT) is used to distinguish between internal faults current and inrush current, and it is noted that both the magnetizing inrush and normal currents do not have any frequency component in the highest sub-band (dd) (S. A. Saleh and M. A. Rahman, 2003).

Authors (S. A. Saleh and M. A. Rahman, 2003) used WPT based on second level details as a signature to diagnose the current signals flowing through the power transformer. The WPT algorithm is implemented offline. When there is inrush current condition, a second level detail is less than zero. While, when there is an internal fault a second level detail is greater than zero.

In 2010, S. A. Saleh and M. A. Rahman included neutral resistance-grounded power transformers and capacitive loads shown in Figure 2.18. The results of the experiment provided no substantial impact of grounding type, loading type, and/or CT saturation on the Wavelet Packet Transform (WPT) performance.

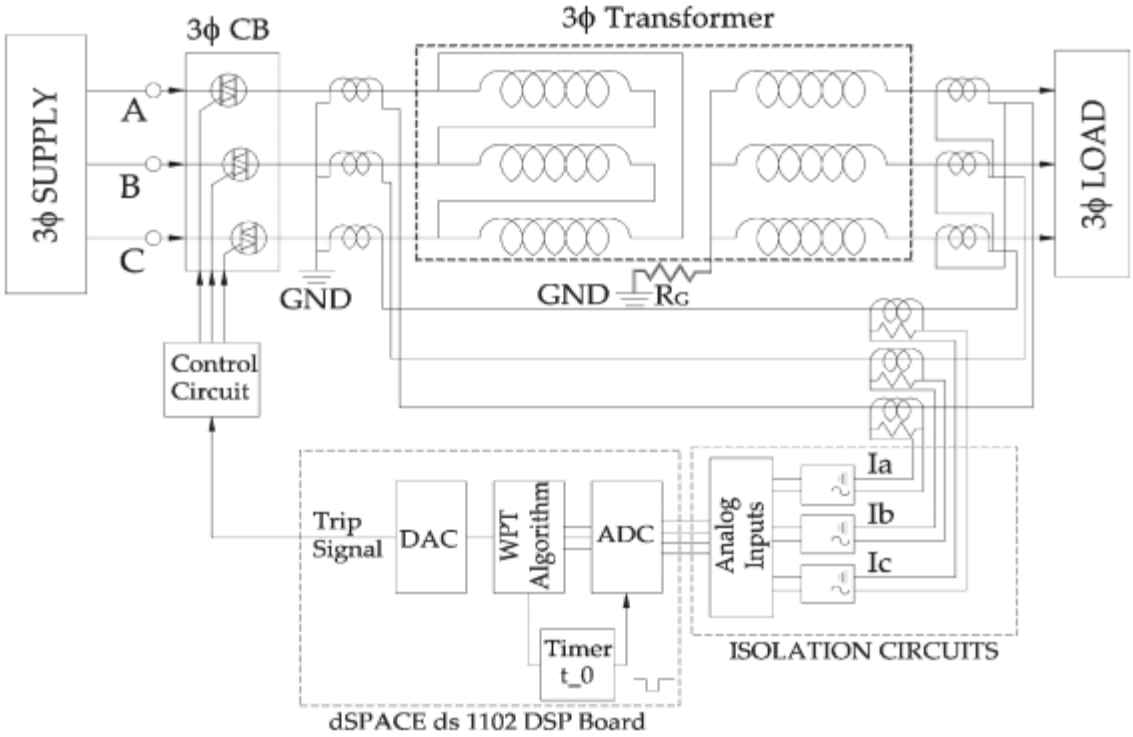


Figure 2.18: Neutral resistance-grounded power transformers and capacitive loads (Saleh S.A and Rahman M.A, 2010)

A Wavelet Packet Transform (WPT) based transformer differential relay using Butterworth Passive (BP) filters was introduced in 2011 by authors (S. A. Saleh et al., 2011).

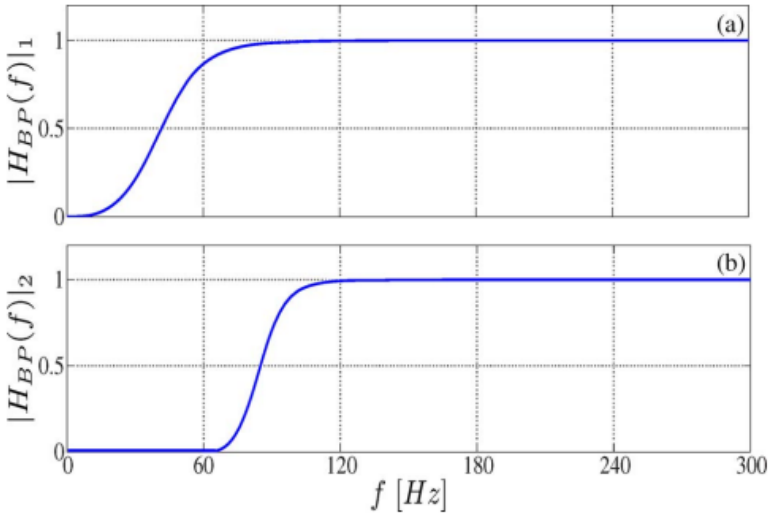


Figure 2.19: Magnitude responses of the BP HPFs for two cascaded stages (Saleh et al., 2011)

The design of the Butterworth Passive filters aims to extract the second-level details comprising of high-frequency components of differential currents for the fault currents detection and analysis. This method tested for both offline and online performances. The case study proved that the BP-filter WPT-based transformer differential scheme response for all the cases was half a cycle based on a 60-Hz system (4–7ms) as shown in Figure 2.19. The reason behind the BP filters selection is their essential abilities to offer monotonic and ripple-free magnitude responses and their capability to provide a precise estimation of the WPT-associated digital filters.

Authors (S. A. Saleh et al., 2012), developed a technique based on the synchronously rotating reference frame (dq) axis transformation of the three-phase differential current signals and technique of the WPT hybrid as shown in Figure 2.20. Using dq-WPT, only 1st level sub-band frequencies of the dq axis component of the three-phase differential currents is essential to deliver enough information in analysing the current flowing in the power transformer.

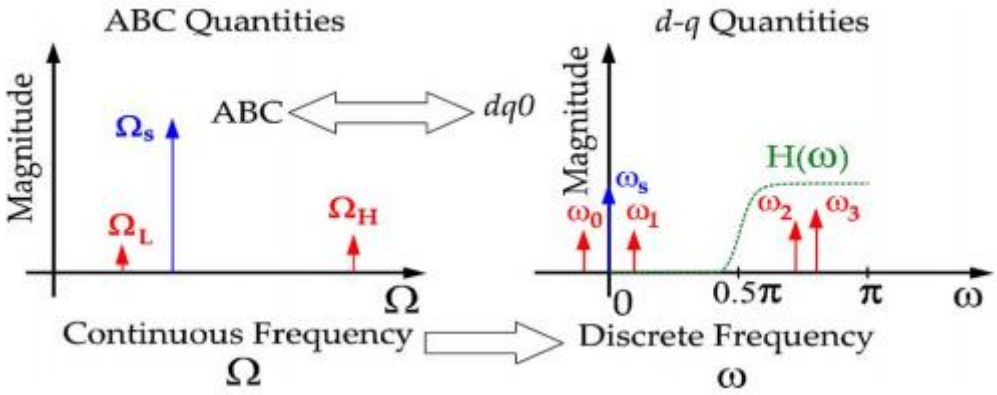


Figure 2.20: Relocating frequency components present in 3ph quantities as a result of the abc-to-dq0 transformation (S. A. Saleh et al., 2012)

The advantages of this signal processing technique are; changing the sinusoidal signals to dc signals which simplify the implementation, no percentage characteristics required to discriminate between the internal faults and inrush conditions, insensitive to the non-periodicity of the signal.

2.4.3. Artificial Neural Network (ANN) for transformer protection

The history of neural networks started in 1943 by authors (McCulloch and Pitt, 1943) where they described a formal calculation of networks which involved simple computing

elements. These basic ideas developed by the authors were later used to form the basis of artificial neural networks. Author (Donald Hebb, 1949), developed the 'Hebbian learning rule' for self-organised learning. He discovered that if two connected neurons were active at the same time, then the connection between them is proportionally strengthened. This means the more frequently particular neurons are activated, the greater the weight between them (i.e., learning by weight adjustment). In 1958, author (Rosenblatt, 1958) invented the perceptron model which was able to solve pattern classification problems through supervised learning. In contrary to the previous author, the authors (Minsky and Papert, 1969) proved the limitations of the single layer perceptron mathematically compared to multi-layered systems and investigated its weaknesses in computation.

The author (Werbos, 1974) developed and introduced the back-propagation algorithm in 1974 to train the network data sets. In 1982, author (Hopfield, 1982) used the idea of energy function to formulate a new way of understanding the computation performed by recurrent networks with symmetric synaptic connections. He developed a new class of neural networks with feedback, which is well known as Hopfield Networks.

Authors (Rumelhart et al., 1986) proposed a back-propagation learning algorithm in 1986. To increase the speed of training of the back-propagation algorithm, it was later modified by many researchers. Authors (Broomhead and Lowe, 1988), described a procedure for designing feed-forward networks using radial basis functions, which provides an alternative to multilayer perceptrons.
According to (Preeti and Sharma S., 2016) training is grouped into three categories:

- **Supervised Training:** Training by a teacher.
- **Unsupervised Training:** There is no external instructor or critic to supervise the training procedure.
- **Reinforced Training or Neurodynamic Programming:** The training of the input and output mapping is completed using a continuous interaction with the environment in order to reduce a scalar index of performance.

The objective for the Artificial Neural Network training is to obtain minimum deviation between the actual outputs and the targeted outputs.

The ANN efficacy relies on the quality of training specified. In (Smith S.W., 1998), pattern reorganisation-based waveform diagnosis method is utilised to train the network using ANN for transformer protection.

Figure 2.21 shows the traditional architecture of the neural networks. It has three layers which are fully inter-connected; they are input, hidden and output. One or more nodes are included in each layer, represented in the diagram by small circles. The flow of information from one node to the next is indicated by the lines between the nodes. Because they only convey the values from a single input to the multiple outputs, the input nodes are passive. Figure 2.22 shows the nodes of the hidden and output layers which are active and are multiplied by weights. The weights applied in the hidden and output nodes determine the output of the neural network.

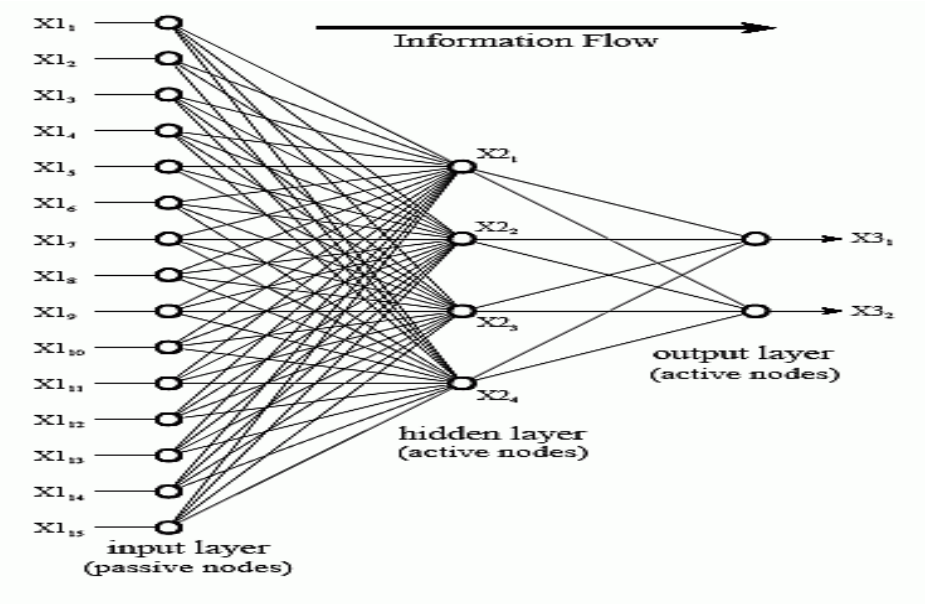


Figure 2.21: Neural network architecture (Smith S. W., 1998)

Where:

$X1_1$ to $X1_{15}$ are the passive nodes

$X2_1$ to $X2_4$ are the hidden nodes

$X3_1$ to $X3_2$ are the active nodes

Figure 2.22 shows the information flow of the neural network. A weight (w_N) multiplies each input, and then they are summed. A single value is produced which passes through "s" shaped non-linear function called a sigmoid. The variables: X_1; X_2... X_7 hold the data

to be assessed (Smith S. W, 1998). All the input values are reproduced and then sent to all of the hidden nodes, and it is named as a fully interconnected structure.

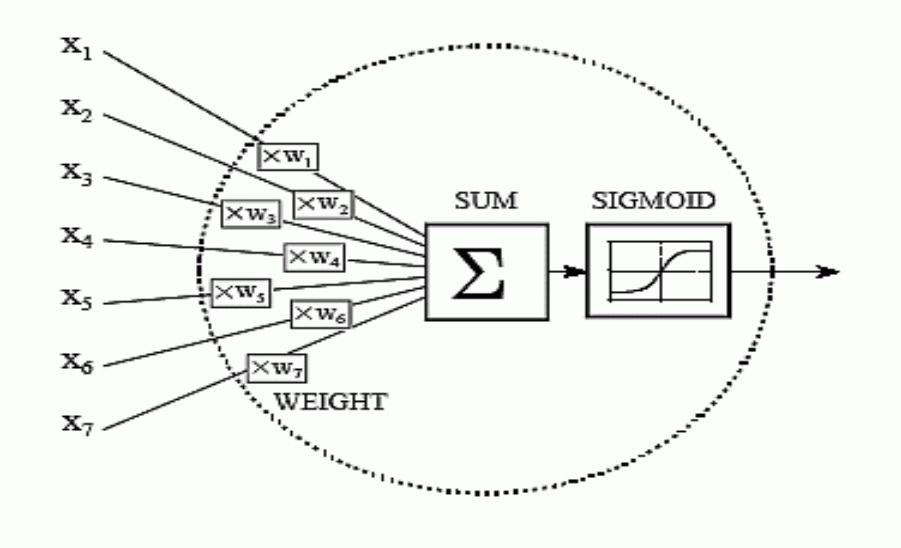


Figure 2.22: Neural network active node (Smith S. W., 1998)

The layers number and number of nodes per layer can be randomly selected in Artificial Neural Networks depending on the application. The structure of the three-layer with a maximum of a few hundred input nodes is used by most applications such as security assessment, modelling and identification, load forecasting, pattern recognition, contingency analysis, fault detection, etc. (Smith S. W., 1998).

Since the ANN development, the approach study of waveform identification is improved. The reason is that it is robust, fast and easier to implement compared to the approach of the conventional waveform (Tan and Tang, 2004). Because of its learning stability with different topologies and its good simplification capability, the ANN is being utilised in the field of protection of the power system about thirty years ago. According to authors (Tripathy et al., 2005), the multilayer feedforward neural network (MFFNN) is used by the majority of the researchers with back propagation learning technique for transformer protective relaying system. In 2003, authors (Moravej et al., 2003) proposed for power transformer protection another ANN model named as the radial basis function neural network (RBFNN).

Artificial Neural Network can be utilised to differentiate between internal fault and inrush currents based on the analysis of the wave shape of current signals. The feed forward back propagation algorithm is used to train ANNs (Mao P. and Aggarwal R, 2001). The

decision of layers number in neural networks is done appropriately. Main advantages of the ANN are their ability to recognise current waveforms for different operating conditions of a transformer.

2.4.4 Application of fuzzy logic for power transformer

In 1965, authors Lotfi A. Zadeh and Dieter Klaua introduced fuzzy sets to deal with the uncertainty of events and as an extension of the classical notion of set. In 1995, the fuzzy logic technique was first introduced to solve the problems of power systems (Ross T.J., 1995). Consequently, the theory of the fuzzy set is considered as a simplification of a theory of the classical set. In this fuzzy set, an element of the universe either belongs to the set, or it does not. Therefore, the association degree of an element is crisp.
The most common types of membership functions are (Ali M. et al., 2015):

- Triangular
- Trapezoidal
- Gaussian
- Generalized bell
- π-Shaped Membership Function
- S-Shaped Membership Function

After 1990, it can be noticed that researchers started with the development of the differential protection scheme for power transformer using fuzzy logic. Authors (Aziz A. et al., 2009), outline that during the transformer magnetizing inrush condition the second harmonic frequency component in modern transformers declined significantly due to improvement in core steel. For this reason, the maloperation possibility for traditional approaches such as transformer differential protection and overcurrent protection increased in the event of the magnetizing inrush current with a low second harmonic component.

A protective relaying algorithm based on the fuzzy can prevent the transformer differential protection maloperation during transformer magnetizing inrush conditions with low second harmonic component and internal faults with high second harmonic component (Iswadi H. and Redy M., 2007). The sensitivity of the fault detection for protective relays increase significantly and operate within half cycle. Therefore, a fuzzy

logic method is identified as a quite reliable and speedy for transformer protective relaying system.

The fuzzy logic method was used by authors (Rad et al., 2011), to detect internal fault events in differential zones of the transformer protection. In order to achieve that, some criteria were considered such as overexcitation, inrush current, CT saturation and CT mismatch by using suitable fuzzy membership functions and criteria. The simulation results of the fuzzy logic showed that protective relaying system operated appropriately for internal and external faults events and was capable of detecting the fault in less than half a cycle which improves the performance of the protection system satisfactorily.

2.5 IEC 61850 standard for substation automation

The power system consists of power generation, transmission and distribution systems and its main function is to generate, transmit/distribute and provide energy to the end-user (Kim et al., 2005). Therefore, the electric utility goal is to complete these responsibilities using a system which is fully automated, integrated and remotely supervised demanding “minimal human intervention”. A standardised communication in substations provided by IEC 61850 “Communication networks and systems in substations” using both state-of-the-art communication technology and powerful object modelling with high-level engineering support.

IEC 61850 standard provides an internationally recognised method of local and wide area data communications for substation and system-wide protective relaying, integration, control, monitoring, metering and testing functions (Miles and A Redfern, 2009). It contains built-in capabilities for data sharing and high-speed control over a communication network, which eliminates most of the hardwiring. The standard can be used between the station level computer and the bay level devices and the primary equipment communication. Additionally, it provides a way for protective relays to interlock and inter-trip. The convenience of Ethernet with the security is combined which is essential in the substations (Miles and A Redfern, 2009). Intelligent Electronic Device (IED) can now send and receive "GOOSE" (Generic Object-Oriented Substation Event) messages for peer to peer relay communications, send fault records automatically, and communicate to IEC 61850 station masters, over a high-speed LAN, (Local Area Network) will reduce cost by eliminating conventional hardwiring.

2.5.1 Benefits of IEC 61850 standard

The benefits of the IEC61850 standard in the distributed power system environment includes (Mackiewicz R., 2006):

- Reduced installation and maintenance expenditure by self-describing equipment that minimizes manual configuration.
- Engineering configuration and commissioning with regulated object models and naming conventions for all equipment that excludes manual structure and mapping of I/O indicators to variables of the power system.
- Reduced time required to construct and use new and revised devices employing regulated configuration files.
- Reduced wiring expenditure while enabling further progressive protection capabilities through the deployment of peer-to-peer messaging for point-to-point transfer of information between devices and a fast process bus which allows distribution of instrumentation indicators between devices.
- Reduced communication framework expenditure by employing freely accessible TCP/IP and Ethernet technology.
- A comprehensive function sets for reporting, data access, event logging, and control satisfactory for most applications
- Ultimate adaptability for users who prefer an expanding number of flexible products to be utilised as interoperable system components

Overview of the different parts of the IEC 61850 standard is provided in Table 2.3:

Table 2.3: Overview of the different parts of the IEC 61850 standard

Part # of the IEC61850 standard	Title
1	Introduction and overview
2	Glossary of terms
3	General requirements
4	System and project management
5	Communication requirements for functions and device models
6	Configuration Description Language for communication in electrical substations related to IEDs
7	Basic communication structure for substation and feeder

	equipment
7.1	- Principles and Models
7.2	- Abstract Communication Service Interface (ACSI) (GOOSE)
7.3	- Common Data Classes (CDC)
7.4	- Compatible logical node classes and data classes
8	Specific Communication Service Mapping (SCSM)
8.1	- Mappings to MMS (ISO/IEC 9506 – Part 1 and Part 2) and ISO/IEC 8802-3
9	Specific Communication Service Mapping (SCSM)
9.1	- Sampled Values over the serial unidirectional multidrop point-to-point link
9.2	- Sampled Values over ISO/IEC 8802-3
10	Conformance Testing

To restrain the overcurrent maloperation relay during inrush current conditions, a reverse blocking scheme based on harmonic currents is employed in this thesis. In harmonic blocking scheme, the differential relay is configured to transmit a GOOSE signal with the reverse harmonic blocking signal and the overcurrent IED is configured to subscribe to the GOOSE message which belongs 7.2 of the IEC 61850 standard.

2.5.2 IEC 61850 Physical communication system

In a power system, they are three levels of functions (Skendzic et al., 2007): a) Process, b) Bay, and c) Station functions as shown in Figure 2.23. In the process level, high voltage devices are connected such as power transformers, circuit breakers, voltage transformers, etc. High voltage devices usually are hardwired by way of copper cable to bay level. Data such as analogue input and output information which contains current and voltage transformer outputs are transferred, as well as trip signals from protective relays. In Figure 2.23, numbers one to ten shows the logical interfacing between station, bay, and process levels, where number four and five show the interfacing amongst process and bay level. Number one and six show protection and control-data transfer amongst station and bay level.

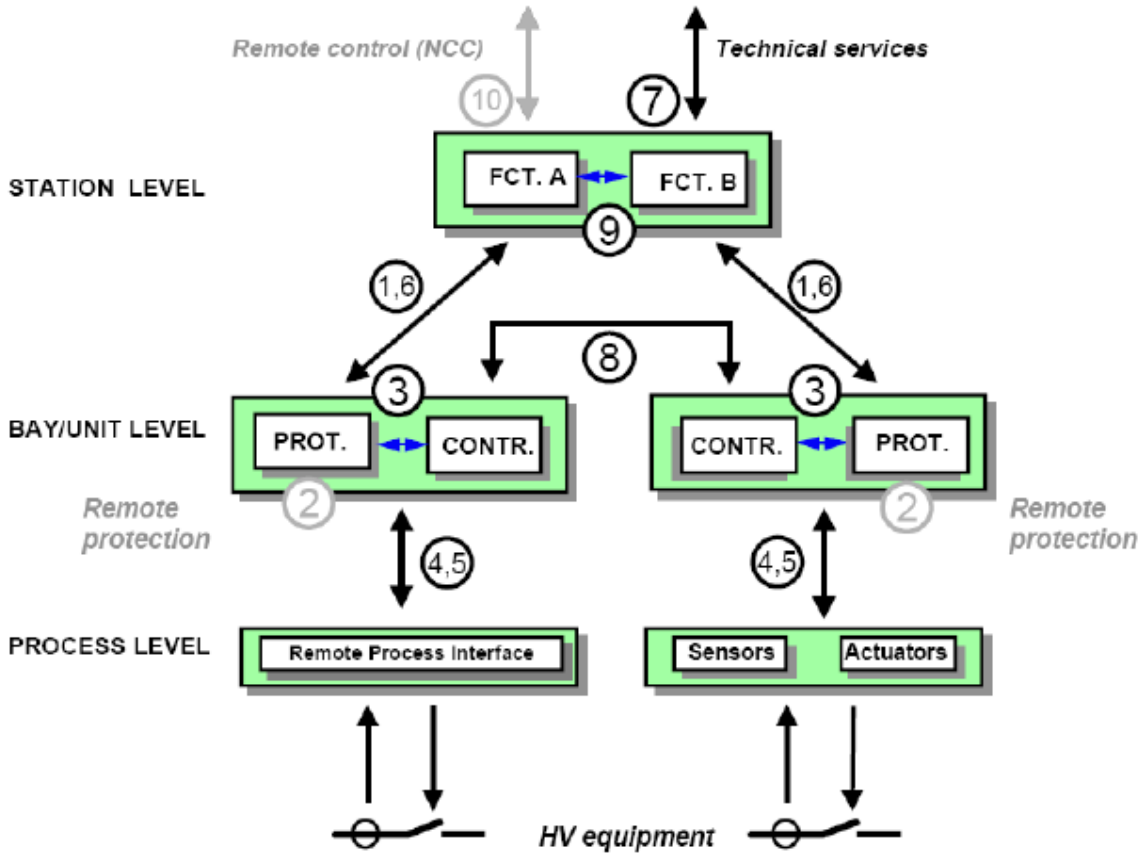


Figure 2.23: Logical interfacing between station, bay, and process levels (Skendzic et al., 2007)

Logical Interfaces as illustrated in Figure 2.23 and have the following functions (Skendzic et al., 2007):

1. Protection – information transfer amongst station and bay level
2. Protection – information transfer amongst remote protection and bay level
3. Information exchange within a bay level
4. VT and CT spontaneous information transfer amongst bay and process levels
5. Control- information transfer amongst bay and process level
6. Control- information transfer amongst station and bay level
7. Information transfer between the remote workplace of engineers and substation
8. Direct information exchange amongst the bays, especially for fast functions such as interlocking
9. Information transfer within station level
10. Control information exchange amongst a remote-control centre and substation

Merger units are used to connect process bay devices such as intelligent sensors over the network via LAN technology (Skendzic et al., 2007). Protection, control, and monitoring devices such as intelligent electronic devices are connected in bay level. Bay level devices can communicate between the bay and the substation levels using IEC 61850-7-2 GOOSE messaging services. Interface eight shows bay to bay communication or horizontal communication. Communication between various functions within a single IED is shown by interface three. Currently, bay level devices communicate with station level devices via IEC 61850 however, communication between the process and bay level devices are via hardwiring. The station computer, database, and communication technology are contained in the station level. Data transfer between IEDs in the station bus is already possible, and more time-critical messages at process level devices are transferred by utilising the process bus. Presently, Merging Units (MUs) have to be used to interface signal outputs since substation high voltage devices (CTs and VTs) are not intelligent devices. The purpose of the MU is to gather analogue signals and convert it in digital form which can be used by protection and control IEDs over the network. Hardwiring is reduced extensively by using Mus (Skendzic et al., 2007).

2.5.3 Substation configuration language

Substation Configuration Language (SCL) files were made available within the IEC 61850 to standardise the describing communications capabilities method within IEDs. The SCL files are classified into four types, they are: i) System Specification Description (SSD), ii) IED Capability Description (ICD), iii) Substation Configuration Description (SCD), and iv) Configured IED Description (CID) files (Adamiak and Mackiewicz, 2004). The four files are built in the same format and method, but different scopes depending on the requirement. There are more than a few situations where the accessibility of a formal description language can bring a lot of benefits to users which are outside the IEC 61850 client applications, yet the client can extract the configuration of an IED if it is connected to that IED via a network (Adamiak and Mackiewicz, 2004).

The SCL file makes some configuration between the IED and the IEC 61850 client very simple, or server of the IEC 61850, specifical integration of Logical Nodes (LNs) and Generic Substation Event (GSE) messages. At first, it was assumed that these SCL files would be better collected straightforwardly from the IEDs, basically a self-description method. Nevertheless, it was rapidly apprehended those system designers hardly ever

have each specific IED at their possession during the implementation of the configuration settings phase. Design engineers work at their desks, whereas the IEDs are at the substation or panel shop (Dolezilek, 2005). Consequently, SCL files are distributed through electronic storage, email and directly from the IED.

2.5.4 IEC 61850 standard-based generic object-oriented substation event (GOOSE) messages

GOOSE is based on the asynchronous to report the status of the functional elements of the IED to other peer devices configured to receive it during the configuration stages procedure of the substation integration (Apostolov, A. et al. 2003). It is utilized in the replacement of the hardwired control signal communication between IEDs for protection and interlocking purposes and; therefore, it is faster, highly reliable and more sensitive. The associated IEDs configured to receive the message should use the containing information to take the appropriate action or to determine what is the protection response for the state change given.

The appropriate action decision to GOOSE messages and the intelligence in the IED configured to receive the GOOSE message determine what action to carry out if the message time is out because of the communication failure. Based on GOOSE messages, it can also be used to trigger recording from different protection or power quality monitoring IEDs (Apostolov, A. et al. 2003).

2.5.5 Review on IEC 61850 standard-based transformer protection schemes

IEC 61850 standard has developed two types of models based on peer-to-peer communication, which are Sampled Values (SV) and Generic Object-Oriented Substation Event (GOOSE). IEC 61850 has magnificent features such as high priority, great flexible and reliable mechanism for the fast transmission events of the substation (trips commands, alarms or indications) (Daboul M. et al., 2015).

Authors (Liu K. et al., 2008) used the Phase-Locked Loops (PLL) technology to propose a novel current differential protection scheme. The scheme solves the problem of delay-non-determinism, and it also establishes a research platform to show the delay-non-determinism problem using the OPNET Modeller. The proposed method analyses the transferring time delay of sampled values from Non-Conventional Instrument Transformer (NCIT) to the differential protection IED using the IEC 61850 standard

network. In this research work, Phase-Locked Loops (PLL) technology is used to implement the time synchronisation between Merging Unit (MU) and IEDs.

In 2009, authors (Vicente et al., 2009) presented a new protection scheme based on IEC 61850-7-2 GOOSE communication. The proposed scheme uses analogue measurements (current and voltage) and digital signals between differential (87) and distance (21) protection functions. As soon as a location of the faulted equipment is identified, it is isolated by the proposed new protection scheme in a coordinated manner entirely by sending a trip signal to both local and remote breakers. Using the IEC 61850 standard technology, every single IED of the proposed scheme also detects the faulted adjacent line, and it sends a trip signal remotely to the corresponding breaker.

The impact of network traffic and sampling synchronisation error on the performance of the transformer differential protection based on IEC 61850 standard was investigated and compared to conventional hardwired connections by authors (Ingram et al., 2014). To test the transformer differential protection performance caused by synchronisation error between Merging Units (MU), a testbed of precision time protocol (PTP) clocks, protection IED, merging units, and Ethernet switches to be investigated are shown in Figure 2.24. IEC 61850 GOOSE communication is used to trip Circuit Breakers (CB), report the tap changer position and transduce differential current measurements.

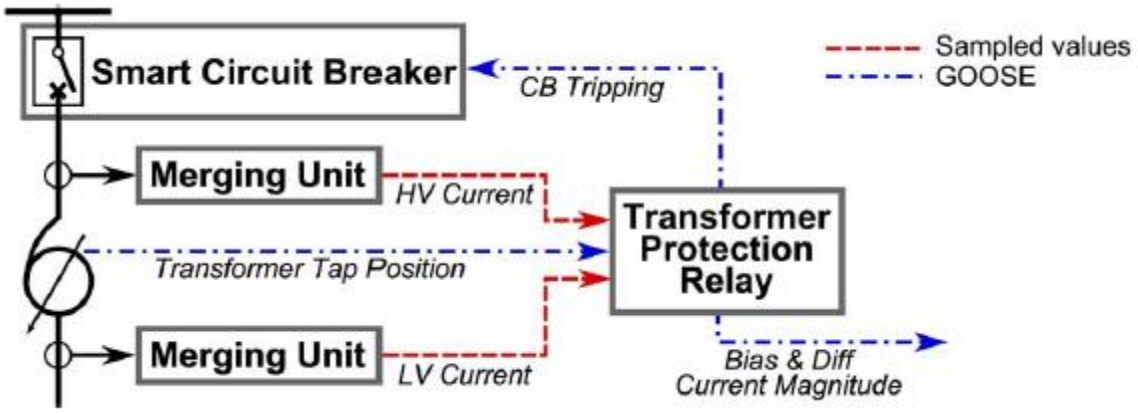


Figure 2.24: Transformer differential protection using IEC 61850 standard-based GOOSE message (Ingram et al., 2014)

In 2013, authors (Sichwart et al., 2013) used the IEC 61850 standard to implement the Load Tap Changer (LTC) control for the power transformer. The proposed method includes a Merging Unit (MU) providing voltage measurements using GOOSE message

to the control unit and an Actuator Module (AM) configured to receive the IEC 61850 GOOSE message from the control in order to operate the LTC motor. Preferably, the voltage measurements must be communicated using the Sampled Values messages (Sichwart et al., 2013).

According to authors (Z. Gajic et al., 2010), transformers connected in parallel with On-Load Tap-Changer (OLTC) can be controlled using the analogue GOOSE messages from the IEC 61850 standard between the regulators. The protection and control of each power transformer are provided by dedicated IED. The two IEDs of the proposed scheme have two logical nodes each. The OLTC mechanism is represented by the first logical node and it integrates functionalities such as OLTC mechanism supervision tap position reading, and the manual and automatic raise and lower issued commands to the OLTC mechanism. The regulator itself is represented by the second logical node and integrates functionalities such as voltage measurement and supervision, circulating current measurement and compensation, line drop compensation, timing etc.

2.5.6 Overview of the IEC 61850 Edition 1 and 2 features

IEC 61850 first edition was introduced in the early 2000s as a communication standard for substation automation (Adamiak and Mackiewicz, 2004). IEC 61850 has been a success since then across the world market, and it characterises the base for state-of-the-art substation automation systems.

The IEC 61850 Edition-I standard has been a massive contribution to the methods of communications and information exchange within substation automation systems. For its connectivity, the IEC 61850 standard uses an Ethernet network along with the use of high-speed switches. The standard provides a solution for interoperability between IEDs from different vendors faced by Substation automation design engineers (Khavnekar et al., 2015).

IEC 61850 standard features include (Ralph Mackiewicz, 2006):

- Data modelling
- Reporting Schemes
- Fast Transfer of events
- Setting Groups
- Sampled Data Transfer
- Commands

- Data Storage

There are a lot of reasons behind the IEC 61850 standard evolution to come to the second edition. It was a big success for most of the interoperability projects, but it moreover appeared that there still were some technical issues for the IEC 61850 first edition implementation. Interoperability issues which were found during those tests were named as TISSUES (Technical Issues) (Dawidczak et al., 2011). **The changes from First Edition to Edition 2 are grouped as (Schimmel R., 2014): Data model, Communication and SCL.**

2.5.7 Review discussion on the IEC 61850 standard-based protection for power transformer

As we are into the age of digital, accurately thousands of digital and analogue data points are available in one Intelligent Electronic Device (IED), and bandwidth of the communication is no more considered a limiting factor. Subsequently, a key component of a system of the communication is the capability to describe themselves from both a data and services (communication functions that an IED performs) perspective. Other "key" requirement includes (Ralph Mackiewicz, 2006):

- High-speed IED to IED communication
- Networkable throughout the utility enterprise
- High-availability
- Guaranteed delivery times
- Standard-based
- Multi-vendor interoperability
- Support for voltage and current samples data
- Support for file transfer
- Auto-configurable / configuration support
- Support for security

The IEC 61850 standard Applications such as Sampled Values and GOOSE messages are used for transformer protection. In this thesis, the implementation of the reverse harmonic blocking scheme using IEC 61850 standard-based GOOSE message is achieved. The scheme uses the Harmonic Blocking element (87HB) of the differential IED to send a blocking signal to the backup overcurrent IED during transformer magnetizing inrush current conditions.

With compliance of the IEC61850 requirements and benefits, the Table 2.4 review overview of the power transformer protection using IEC 61850 standard.

Table 2.4: Review overview of the transformer protection using IEC 61850 standard-based protection schemes

Paper	Aim	Protection	Communication and Protocol	Simulation / Hardware implementation	Benefits / Drawbacks
Vicente et al., 2009.	Transformer differential protection scheme based on IEC61850 standard.	Transformer differential (87) and distance protection (21)	IEC 61850-7-2 GOOSE	The scheme has been modelled and implemented in a protection simulation software CAPE (Computer-Aided Protection Engineering). This tool is designed for relay configuration settings and coordination.	The performance of the IEC 61850 based differential protection scheme is improved the system reliability, selectivity, security and dependability.
David M. E. Ingram, et al., 2014.	An investigation of process bus protection performance, since the in-service behaviour of multifunction process buses, is mostly unknown.	Transformer differential protection.	IEC 61850-8-1, IEC 61850-9-2 and GOOSE. Ethernet was used for all sampled value measurements, circuit breaker tripping, transformer tap-changer position reports, and precision time protocol synchronisation is	A lab scale substation automation system based on a Real Time Digital Simulator (RTDS). The transformer differential protection relay ABB RET670 with 9-2LE (sampled value) and conventional copper (CT/VT) inputs.	Transformer differential protection performance is compared with conventional hardwired and Ethernet-based signalling. The effect of sampling synchronisation error and network traffic on transformer differential protection performance was assessed.

			used merging unit sampling.		
Nelli Sichwart, 2012	Transformer Monitoring and control.	IEC 61850-based Load Tap Changer (LTC) control method.	IEC 61850-7-2 GOOSE Messaging.	- A load tap changing power transformer with 500kV on the high voltage side and 169kV on the low voltage side. The LTC is located on the high voltage side and allows for 17 tap positions. - SEL-2414 Transformer Monitor serves as the control unit and processes the voltage measurements, deciding whether to operate the LTC and when necessary issuing a command to raise or lower the transformer tap. -The SEL-2411 Programmable Automation Controller used to implement both MU and AM.	The major advantage of the proposed GOOSE messaging based LTC control solution is available for protection and automation devices in the power industry.
Z. Gajic, et al., 2010	Protection and control for the whole substation are done by using IEC 61850 Standard. The control of parallel transformers	Transformer differential protection, backup overcurrent protection and transformer control.	IEC 61850 analogue GOOSE messages (Sampled Values).	All power transformer protection functions like 87T, 87N, 50/51, 50N/51N, 49 as well as OLTC control function (90) are integrated into a single device. Two transformers can operate in	The advantage of using IEC 61850, it does not require an additional proprietary the communications interface, but can be implemented on an existing IEC 61850-8-1 infrastructure already present in

	with On-Load Tap Changer (OLTC) using IEC 61850 analogue GOOSE messages between the regulators.			parallel; the OLTC control is based on the minimizing circulating current principle. In this substation, there are two 20MVA, 110/20kV, YNd5 transformers with OLTC.	the substation. Each power transformer has a dedicated IED which provides integrated protection and control for the transformer. The OLTC control functionality is implemented in accordance with IEC 61850 Standard. Thus, two logical nodes, namely YLTC and ATCC, are available in each of the two IEDs.
Liu, Kun Dong, Xinzhou, 2008	Analyse the time delay of transferring sampled values from Non-Conventional Instrument Transformer (NCIT) to IEC61850 based differential relay.	Current differential protection.	IEC61850 based digital substation	MU (Merging Unit) between NCIT and protection IEDs. This equipment can receive the sampled value from NCIT, and output data to protection IEDs accordance with IEC 61850 high-speed data.	To sacrifice the operating time of protection is the most serious drawback in the PLL scheme.
Kuffel, Rick Ouellette, Dean, 2010	Implementation of the IEC 61850 GOOSE messaging on a real-time simulator using the GTNET card.	Transformer differential protection and distance protection	GOOSE messaging, IEC 61850 standard and IEEE C37.2011	The effectiveness of the RTDS simulator used as a testing tool. Sampled values of the voltage and current signals are sent via Ethernet to perform closed loop tests.	Understanding how a protection system responds to IEC 61850 data and its importance. It provides engineers confidence that the system will behave acceptably.

2.6 Review on protective relaying testing using hardware-in-the-loop (HIL) and Real-Time Digital Simulator (RTDS)

In 1991, RTDS Technologies Inc. launched the first commercial Real-Time Digital Simulator using Digital Signal Processor (DSP) (RTDS, 2014). The RTDS was interfaced to the controller of a high voltage direct current converter in order to assess its performance. A combination of both analogue and digital parts was used in that simulator. RTDS has grown since then and become one of the broadly utilised commercial real-time simulators. Authors (Devaux et al., 1998) presented the first small-scale digital simulator to test the equipment of the power system in real-time based on the multipurpose standard of the parallel computer system, known as the Digital Transient Network Analyzer (DTNA). The DTNA could simulate phenomena of the electromagnetic transient up to 3 kHz, electromechanical transients and ac/dc interactions. Using this simulator, different types of equipment, controllers and components including power electronic-based controllers could also be modelled and simulated.

The HIL testing with protective relays is performed using two test models. They are: open loop testing and closed-loop testing. Next section discusses these test models in detail.

2.6.1 Open-loop testing

The power system is modelled in the RSCAD software suite of RTDS, and the protective relay open-loop testing is simulated in real-time. The secondary currents from the CTs are sent to the numerical relay behaving like a controller through the amplifier. The responses of the relay are monitored on its front panel. This is an open loop test because the signals from the hardware relay are not fed back to the RTDS.

According to authors (Marttila et al., 1996), the open loop mode can be used to test some equipment for protection and control, in this type of test case the feedback to the modelled system from the equipment response is not necessary. This test is applicable where it is assumed that the equipment's action timing, in response to events of the power system, does not impact the equipment's response to consequent changes in the power system. Figure 2.25 below shows the open loop test arrangement.

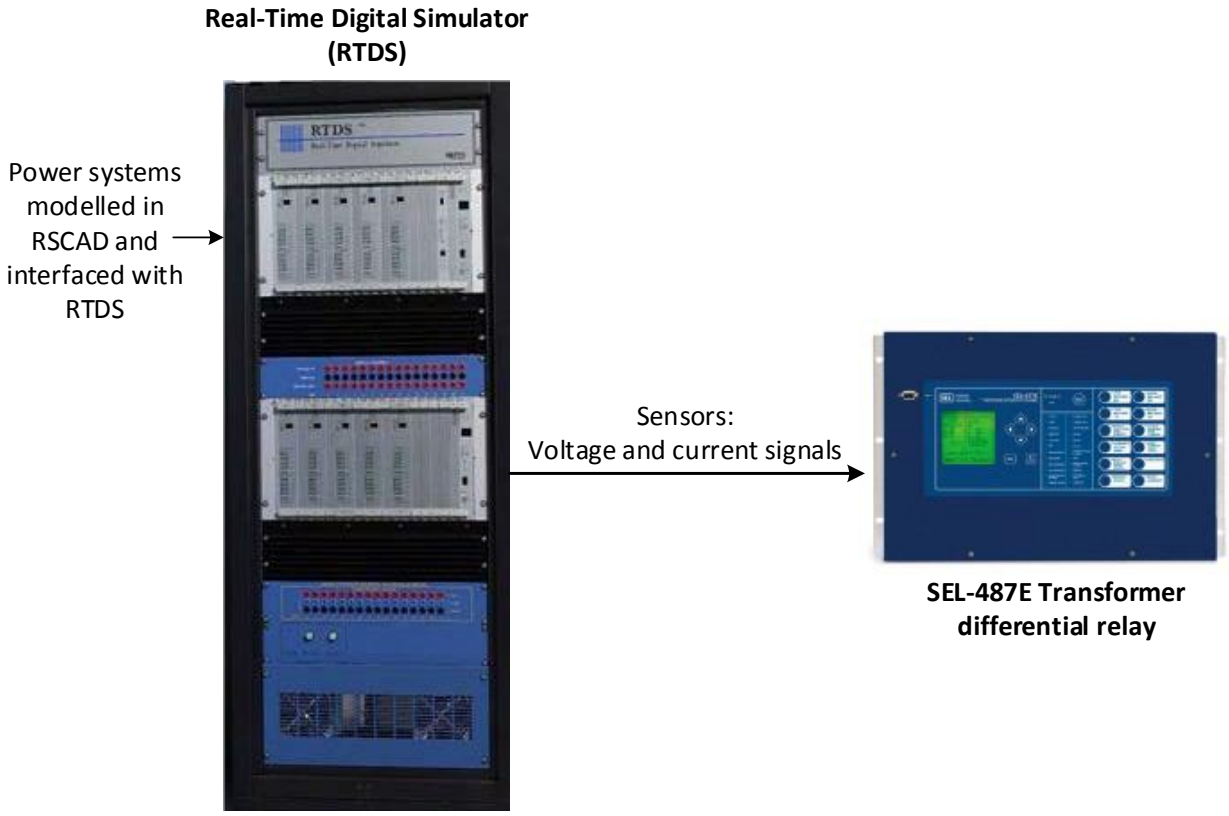


Figure 2.25: Open-loop testing arrangement using RTDS and protective relaying system

As shown in the above Figure 2.25, the terrestrial power system is simulated in the RTDS and the currents, which are drawn by the CTs, are sent to the device under test, which is a transformer protective relay. The faults are incepted on the power system, and the trip signals are observed on the front panel of the relay. The importance of the open loop testing lies in reducing the errors of the responses and also helps to modify the transformer differential protective relay settings before conducting the closed-loop test.

2.6.2 Closed-loop testing

Closed-loop testing allows detailed testing and investigations to be carried out for the performance of protective relays under highly-realistic conditions (McLaren et al., 1992). Once the open loop test has been done, and the responses from the protective relay are reliable, the implementation of the closed loop test can be done. For the closed-loop testing, the protective relay response signals (actuator: trip signals) are fed back to the RTDS, and this allows the monitoring of the trip signals, and circuit breaker status by the

user through the window of the Run Time in RSCAD software environment. The Figure 2.26 below shows the closed loop hardware-in-the-loop test arrangement.

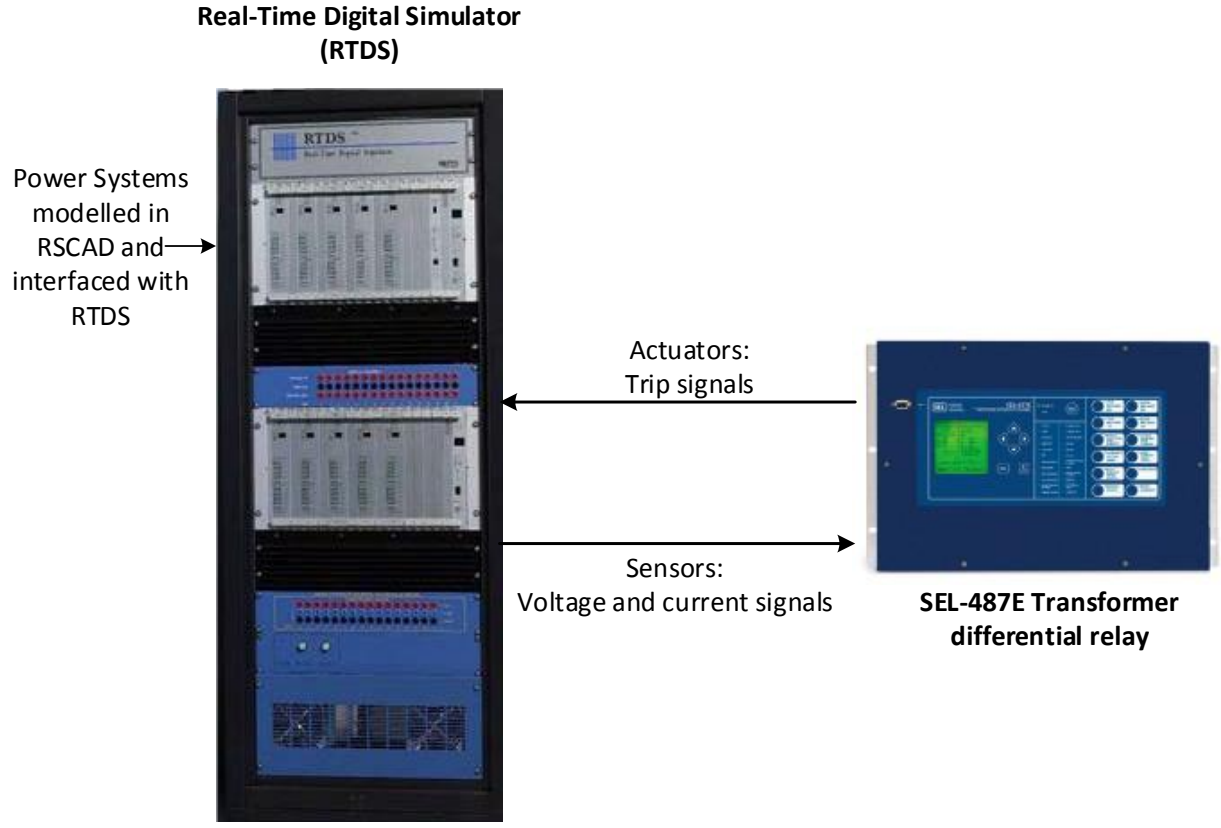


Figure 2.26: Closed-loop testing arrangement using RTDS and protective relaying system

As shown in the above Figure 2.26, RTDS is used to simulate the power system test case. The secondary currents from the CTs are sent to the SEL-487E transformer differential relay through the sensors, and the response signals (actuators: trip signals) from the IED are fed back to the RTDS through actuators. The basic idea behind closed loop hardware-in-the-loop testing is the behaviour monitoring of the SEL-487E transformer differential relay when interfaced to the RTDS and analyse the real-time simulation results.

6.2.3 Review discussion on HIL testing of the protective relaying system

The RTDS provides one of the most effective and advanced means available for protection systems testing. The protection equipment connected in open-loop or closed-loop mode since the simulation runs in real time with the power system model.

Authors (Roekman et al., 2004) presented the results of an extensive study using Real-Time Digital Simulator (RTDS) based on Indonesian 500 kV shunt compensation network. Around two hundred case studies with the different combination of the various type of the faults, inception angles and fault resistances were simulated using closed-loop testing in order to evaluate the relay performance.

According to the author (De Oliveira, 2008), testing the numerical distance relay using Real-Time Digital Simulator (RTDS) provides to user larger reliability, the maximum performance and functionality are obtained then apply to the power transmission system. The author analysed the performance of the numerical distance relay for the 500 kV transmission lines of CEMIG (Energy Company of Minas Gerais-Brazilian Energy Utility).

RTDS was used by authors (Jung et al., 2000) to construct a test model on the double circuit transmission line and perform the relay configuration settings and testing. The authors concluded that the RTDS is suitable for the commissioning of relay because the Voltage Transformer (VT) and Current Transformer (CT) secondary voltages and currents respectively are as same level as actual power systems.

In 2004, author (Rigby, 2004) developed a procedure to conduct closed-loop testing of the overcurrent IEDs using the RTDS. The simulation results helped to discover the modelling issues and the hardware requirements for closed-loop testing.

The high penetration of Distributed Generation (DG) causes protection issues in distribution networks. Authors (Papaspiliotopoulos et al., 2014), investigated this challenge by implementing Controller Hardware-in-the-loop (CHIL) to test the protective relays and Power Hardware-in-the-loop (PHIL) of the PV inverter and wind energy system. These simulation tests helped to verify the impact of the DG on protection schemes.

The secondary current and voltage provided to the protective relay through GTAO and amplifiers, the relay response is connected to the actual power systems. The functions of the protection respond to the power system events by providing trip or reclose signals. The relay feedback signals are used for breakers operation modelled in the simulation.

Table 2.5: Review overview of the hardware-in-the-loop testing using RTDS and protective relays

Paper	Aim	Method used	Protection	Simulation / implementation Hardware /software	Benefits
R.J. Marttila et al., 1996	The closed-loop test setup for testing a feeder relay, a power system stabiliser, and a circuit breaker controller.	Closed-loop testing of the protection scheme using RTDS.	Overcurrent protection.	RSCAD and RTDS	The detail requirements in utilising the real-time digital simulator in three closed-loop test applications have been provided.
De Oliveira, 2008	Performance analysis of numerical distance protection schemes of high voltage transmission lines, more specifically in the 500 kV transmission lines of CEMIG (Energy Company of Minas Gerais-Brazilian Energy Utility)	A Real-Time Digital Simulator (RTDS) was used in a closed loop simulation. Therefore,	Distance protection.	RTDS, RSCAD and distance protection IED using Siemens 7SA612. The tripping and reclosing commands for the circuit breakers were sent directly to the simulator.	The Real-Time Digital Simulation results provide larger reliability for the numerical distance Relays users.
Roekman et al., 2004	An extensive study of evaluating the performance of the numerical distance relay using modern real-time digital simulator based on	Closed-loop testing of the protection scheme using RTDS.	Distance protection.	PSCAD and RTDS. Almost 200 cases with the different combination of various fault types, position, inception angles and fault	The real-time simulation practice is helpful to validate the protection algorithm and to test the simulations on various fault types that may

	Indonesian 500 kV shunt compensation network.			resistances are essential to evaluate relay transient performance using the closed-loop testing tool.	occur in an actual power system.
Jung et al., 2000	A test model on the double circuit transmission line is constructed using RTDS, and the relay engineering configuration settings are performed.	Closed-loop testing.	Distance protection and line differential protection.	RTDS and PSCAD.	Real-Time Digital Simulator (RTDS) is suitable for approval test before commissioning the relays because various types of faults can be simulated, and tests can be performed at the values of CT currents and PT secondary voltages.
Rigby, 2004	Develop a procedure to conduct a closed loop testing of overcurrent relays using the real-time digital simulator.	Closed-Loop testing on the real-time simulator.	Overcurrent protection.	RTDS, SEL 311C and Quickset AcSELerator.	RTDS simulation provided the modelling issues and hardware requirements associated with closed-loop relay testing.
Rigby, 2007	Describe the test system configured to demonstrate automated closed-loop testing of the relays in a	Close loop testing used for the system which comprises two parallel 400 kV lines fed from sources	Distance protection.	RSCAD, RTDS and SEL 311C.	The automated approach to test a protection scheme on a real-time simulator is

	simple protection scheme.	behind system impedances at each end.			best suited to identifying fault scenarios of interest.
Papaspilioto poulos, et al., 2014	Discuss the new protection to challenge issues in distribution networks owing to the high penetration of DG.	Controller Hardware-in-the-Loop (CHIL), used to test the control logic executed in a relay and Power Hardware-in-the-Loop (PHIL) is tested for PV inverter, wind energy system.	Feeder Overcurrent protection.	RTDS, RSCAD, SEL-587, SEL-311B and AcSELerator Quickset.	The challenging issues of protection blinding and sympathetic tripping in distribution networks due to the high penetration of DG were analysed and the HIL simulation is performed. The severe impact of these phenomena on existing protection schemes was verified in a simplified 5- bus distribution grid.

2.7 Conclusion

The literature review analyses the various techniques used for transformer protection. Digital algorithms for transformer protection schemes in terms of speed, stability, security and dependability have placed a considerable burden and responsibility among protection engineers. The overcurrent relay used as a backup protection of digital transformer protection has not been subjected to active research, and little work has been reported on the development of computational intelligence algorithms that prevent it from tripping during inrush conditions. Most proposed transformer protection schemes developed by the previous researchers focused on the main current differential relay. The review has focused on the external and internal faults and inrush current conditions. The digital protection algorithms that were proposed in the past for protecting power transformers have been focused on using transformer differential protection. Most of the research work reviewed is concentrating on solving the differentiation between inrush current and internal faults on the main transformer protection relay and failed to focus on backup overcurrent. Most of the researchers generally used five different methods named as Harmonic Restraint (HR), Fuzzy logic, conventional Waveform Identification (WI), Artificial Neural Network (ANN) and Wavelet analysis to distinguish between internal fault and magnetizing inrush current conditions.

The application of protective (IED's) that comply with the IEC 61850 standard has proven to be the solution to reliable protection to the power system. The IEC 61850 is a new communication standard that permits the development of a new variety of control and protection applications that result in substantial benefits compared to the conventional hardwired solutions. It reliably supports interoperability between the control devices and protective relays from different manufacturers in the substation. This is important to achieve interlocking substation level, protection and control functions and to improve the numerical relays efficiency applications.

This literature review chapter investigated power transformer protection for external and internal faults conditions. The review analysed the Discrete Fourier and wavelet transform techniques and digital signal processing algorithms for transformer protective relaying system. Finally, the review provided investigation on the IEC 61850 standard for substation automation system and IEC 61850 standard-based GOOSE message applications for power transformers. The IEC 61850 protocol is an innovative approach that requires a new way of thinking about substation automation that will result in a very significant improvement in both cost and performance of electric power systems.

Therefore, this research work is focused on IEC 61850 standard-based reverse harmonic blocking method to prevent the backup overcurrent relay from tripping during inrush current conditions.

Chapter three presents the theoretical aspects of transformer protection schemes.

CHAPTER THREE
THEORETICAL OVERVIEW OF ELECTRICAL AND MECHANICAL PROTECTION OF POWER TRANSFORMERS

3.1 Introduction

Transformer failures can be very expensive such as the cost of repairing the transformer, the cost of energy not delivered because of transformer unavailability, and the possible additional cost on spreading damage to adjacent equipment or of a significant power system blackout.

Transformers failures are also dangerous. Internal and external faults and other abnormal operating conditions, such as overload, overexcitation, overvoltage and mechanical stress due to loading on transformers. The transformer protection schemes should disconnect the protected device before extensive damage occurs and/or power system. In addition to protection elements, transformer protection relays should also provide thermal and through-fault monitoring functions.

This chapter provides the theoretical overview of an i) electrical and ii) mechanical protection of a power transformer. The electrical protection of a transformer includes differential protection, negative sequence percentage differential protection, combined differential and restricted earth protection and the backup overcurrent protection schemes. The electrical protection schemes are summarised below:

- The differential protection scheme to provide high-speed clearing of internal transformer faults and to achieve high security for external faults and transformer energisation or overexcitation conditions;
- Negative sequence differential protection scheme to provide sensitive detection of turn-to-turn faults;
- Combined differential and restricted earth fault protection scheme to detect ground faults, with greater sensitivity to faults near the transformer neutral;
- Transformer overexcitation protection scheme to prevent transformer damage during system islanding or other abnormal system conditions;
- Overcurrent protection scheme to prevent exceeding the transformer through-fault capability;

The mechanical protection of a transformer includes Buchholz relay, pressure protection and thermal protection. Summary of the mechanical protection scheme is given below.

- Buchholz and sudden-pressure relays to provide sensitive detection of faults internal to the tank;
- Thermal protection of a transformer to monitor overload and excessive through-fault condition.

It is necessary to understand the principles of the ideal transformer (lossless), practical transformer and its sequence impedances (positive, negative and zero) before processing to the mechanical and electrical protection schemes for power transformers. Next section discusses the principles of the ideal transformer.

3.2 Ideal transformer

An ideal transformer is one that is assumed to be lossless, implying that it has 100% efficiency. A schematic representation of an ideal transformer is shown in Figure 3.1 below.

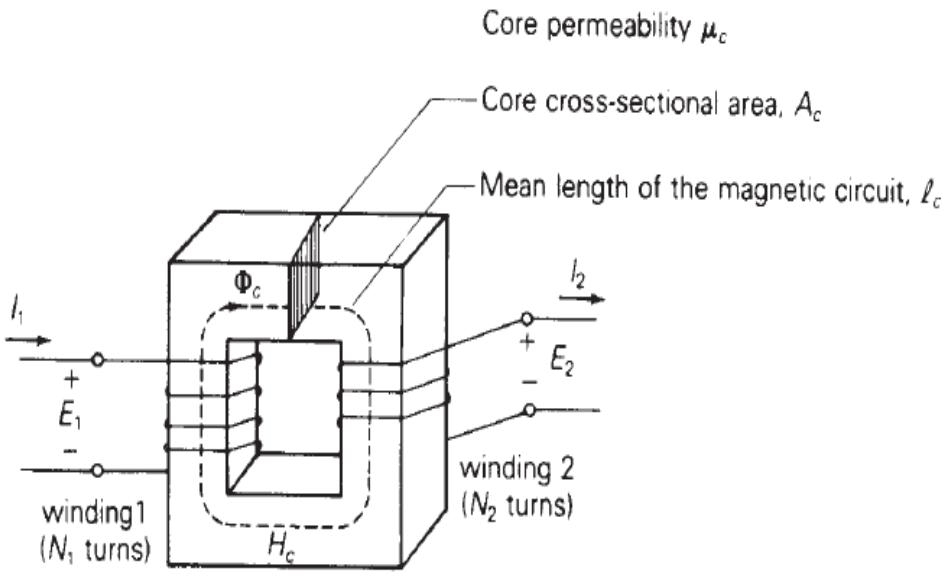


Figure 3.1: Ideal Transformer (Fallis A., 2013)

Where:

E_1 – voltage applied to the primary winding of the transformer

E_2 – voltage at secondary terminals of the transformer

I_1 – current flowing through the primary winding of the transformer

I_2 – current flowing through the secondary winding of the transformer

N_1 – number of turns on the primary winding

N_2 – number of turns on the secondary winding

μ_c – core permeability

A_c – core cross-sectional area

l_c – mean length of the magnetic circuit

An ideal transformer assumed to be operating under sinusoidal steady state excitation condition having zero winding resistance and zero I^2R losses (Fallis A., 2013). It is assumed to have the following characteristics:

- An infinite core permeability, which corresponds to zero core reluctance.
- It has no leakage flux, implying that the entire flux is confined to the core and links both windings.
- It has zero core losses.

It is worthwhile to keep in mind that a practical transformer is completely different from an ideal transformer (Fallis A., 2013), and it possesses the following characteristics:

- The windings possess resistance, and thus I^2R losses exist.
- The core permeability is finite, and consequently, core reluctance exists.
- Magnetic flux is not entirely confined to the core; hence there is leakage flux.
- Real and reactive power losses exist in the transformer core.

The fundamental operating principle of all transformers regardless of size and application is based on two laws:

1. Faraday's law of electromagnetic induction which states that an EMF will be induced in any electrically conductive material placed within a time-varying magnetic field.
2. Lenz's law which states that a wire carrying an alternating current will set up an alternating magnetic field around it.

The principle of operation of a transformer can be summarised as follows: When the primary winding of the transformer is connected to an alternating current source, it will draw a small excitation current i1 from the source. This current is responsible for setting up the mutual alternating flux Φc in the transformer's core. This mutual alternating flux extends to the secondary winding and induces an EMF E_2 in it. The EMF is proportional to the primary voltage and the proportionality constant is given by the ratio of number of turns N_2 in the secondary winding to the number of turns N_1 in the primary (Harlow J.H., 2004). It should, however, be noted that the primary and secondary windings of the transformer are not connected electrically but magnetically coupled (Babiy M. et al., 2011).

The following Equation describes the EMF induced in the secondary winding:

$$E_2 = N_2 \frac{d\emptyset_C}{dt} \tag{3.1}$$

Where:

N_2 – number of turns on the secondary winding of the transformer.

Φ_C – mutual magnetic flux through one turn of the coil.

The instantaneous value of the sinusoidal flux Φ is given by:

$$\Phi = \Phi_{max} sin(\omega t) \tag{3.2}$$

Substituting Equation (3.1) into (3.2) the induced EMF in the secondary winding is given by Equation (3.3) as follows:

$$E_2 = N_2 \frac{d\emptyset}{dt} = \omega N_2 \Phi_{max} cos(\omega t) \tag{3.3}$$

Where:

ω – angular frequency

Φ_{max} – maximum magnetic flux in the transformer core

For an ideal transformer (Babiy M. et al., 2011), it is accepted that the induced voltage E_2 in the secondary windings of the transformer is equivalent to the measured voltage V_S at secondary terminals, assuming that the windings have zero/negligible resistance which results to negligible/zero internal voltage drop.

3.3 Practical transformer

The major difference between the ideal transformer and practical transformer lies merely in the analysis of eddy, hysteresis, I^2R losses and magnetic flux in the core of the transformer. Of course, an ideal transformer does not exist; it is merely a theoretical representation of a lossless practical transformer.

As described in previous section 3.2, an application of voltage to the primary windings of the transformer will cause a magnetizing current flow in the primary winding. This current sets up a flow of magnetic flux in the core which results in losses occurring in steel (Harlow J.H., 2004). These losses comprise of two components termed, "eddy" and "hysteresis" losses.

Hysteresis loss is caused by the continuous reversal of flux in the magnetic circuit, while Eddy loss is caused by “eddy currents” circulating within the steel core. These

Eddy currents are induced by the flow of magnetic flux normal to the width of the core and can be controlled by reducing the thickness of the steel lamination or by applying a thin insulating coating (Harlow J.H., 2004).

The mathematical representation of the Eddy current loss is given in Equation 3.4

$$W_e = KW^2B^2 \; watts \tag{3.4}$$

Where:

W_e – energy lost due to eddy currents in watts

W – thickness of the core lamination material in mm

K – constant

B – flux density in Webber

From Equation (3.4) we can see that if a solid core were used in a power transformer, the losses and the temperatures inside the transformer would be very high. For this reason, cores are usually made up of very thin laminated steel or iron sheets with thicknesses ranging from 0.23 to 0.28mm (Harlow J.H., 2004). This has the effect of reducing the individual sheets of steel normal to the flux and thereby decreasing the losses. The equivalent circuit of a practical transformer is shown in Figure 3.2.

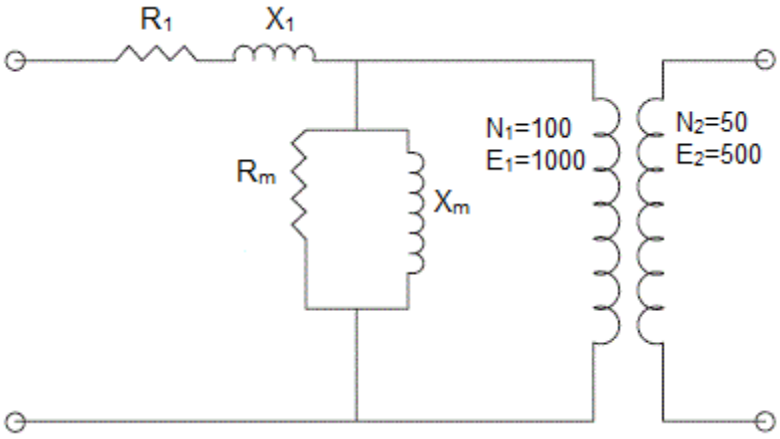


Figure 3.2: Equivalent circuit of a practical transformer (Harlow J.H., 2004)

In Figure 3.2, Rm represents the core losses, Xm the excitation characteristics, R_1 and X_1 the equivalent impedance of the transformer. When a small magnetizing current, which is generally accepted to be about 0.5% of the load current flows in the primary winding, a small voltage drop will occur across the resistance of the winding and a small inductive drop across the inductance of the winding. However, these voltage drops are very small in relation to the applied terminal voltage and can be neglected in the practical case, however, it influences the voltage regulation.

The practical (losses) and ideal (lossless) transformers output and efficiency depend upon the internal core design and materials used. In summary, a design of the ideal transformer is not practically feasible. However, the latest modern core design will help to achieve the maximum efficiency and minimum transformer losses.

The sequence impedances (positive, negative and zero) will influence the fault current level according to the type and location of the fault on the power system. Therefore, these sequence impedances provide the design criteria for the protection devices which include the instrument transformer ratings and protection relay settings.

It is necessary to have proper core design and protection settings in order to maintain the maximum efficiency and ensure 100% transformer protection during disturbances.

Next section discusses in detail the sequence impedances, electrical and mechanical protection schemes for transformers.

3.4 Power transformer sequence impedances

Impedances present in the transformer as a result of positive, negative and zero currents flowing in the transformer windings are called, positive Z_1, negative Z_2 and zero Z_0 sequence impedances (Babiy M. et al., 2011). Since transformers maintain a constant impedance even with reversed phase rotation, their positive and negative sequence impedances are equal to each other (Mehta, V. and Mehta, R., 2009). This value is determined through a short circuit voltage test, and it is the same percentage impedance printed on the nameplate of the transformer.

The zero-sequence impedance, on the other hand, is however dependent upon the neutral path of the transformer. If a through circuit for earth current to flow is present on the power transformer, the resulting zero sequence impedance will be equal to the positive and negative sequence impedances; otherwise, it will be infinite (Mehta, V. and Mehta, R., 2009).

A power transformer's primary and secondary windings can either be connected in a wye (Y) or delta (∆) configuration. It then follows that a transformer can be configured in four possible configurations namely: Y-Y, Y-∆, ∆-Y or ∆-∆.

Since the flow of zero sequence currents in a power transformer is dependent on the availability of a through circuit to earth, the combination in which a transformer is configured plays a vital role in the flow of zero sequence currents and consequently

on the resulting zero sequence impedance. Possible transformer configurations and their effect on the zero-sequence impedance of a power transformer are shown in Figures 3.3 to 3.9 respectively.

It should be noted that a delta connection on either side of the Y-Δ or Δ-Y configured power transformer introduces a 30° phase shift between the quantities on either side of the transformer. For example, in Y-Δ configured transformer, the quantities on the delta side of the transformer will lead those on the Y side of the transformer with an angle of 30°.

3.4.1 Zero sequence impedance of a Y-Y transformer

In a Y-Y connected transformer, if both primary and secondary windings are grounded, a through circuit to earth exists, and consequently, zero sequence currents flow in both windings of the transformer as depicted by the zero-sequence impedance diagram given in Figure 3.3.

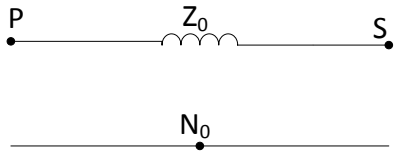


Figure 3.3: Zero sequence impedance of a Y-Y transformer

Where: P – Primary terminal
S – Secondary terminal
Z_o – Zero sequence impedance
N_o – Zero sequence neutral

If one of the windings either on the primary or secondary side of the transformer is not grounded, then zero sequence currents will not flow in that winding, and the resulting impedance is zero. It should, however, be noted that zero sequence currents will flow in the grounded winding and consequently a zero-sequence impedance will exist in that respective winding. Figure 3.4 depicts a Y-Y transformer with the secondary winding grounded and the primary winding left ungrounded.

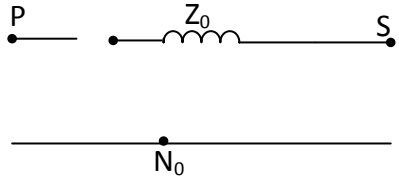


Figure 3.4: Zero sequence impedance of a Y-Y transformer with only the secondary winding grounded

3.4.2 Zero sequence impedance of a Δ-Δ transformer

In a delta-delta connected transformer, zero sequence currents will only circulate inside the delta connected winding and will not enter the power system network. Therefore, it means that during unsymmetrical fault calculations the zero-sequence impedance of a delta-delta transformer is not considered to be part of the total circuit impedance. Figure 3.5 shows the zero-sequence impedance diagram of a delta-delta transformer connection.

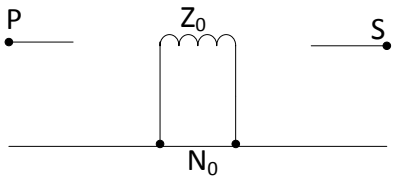


Figure 3.5: Zero sequence impedance network of a delta-delta transformer

3.4.3 Zero sequence impedance of a Y-Δ transformer

In a wye-delta connected transformer, if the wye winding is grounded then zero sequence currents will circulate through the delta winding. In this configuration, primary zero sequence currents from the rest of the power system will flow because of the earth return path on the wye side of the transformer. During unsymmetrical fault calculations, the zero-sequence impedance of this transformer will be considered part of the total circuit impedance but only up to the wye winding. Consequently, the zero sequence impedances of other network components connected on the delta winding of the transformer will not be considered part of the total circuit impedance because the zero sequence currents will never leave the delta winding. Figure 3.6 below depicts zero sequence network of the Y-Δ transformer.

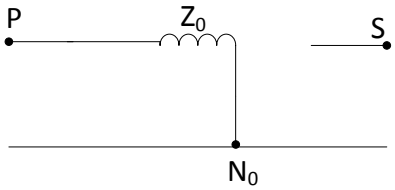


Figure 3.6: Zero sequence impedance for a Y-Δ transformer with wye grounded

If the wye winding of a Y-Δ transformer is not grounded, no zero sequence currents will flow in the transformer, and the equivalent circuit reflects an infinite impedance as shown in Figure 3.7.

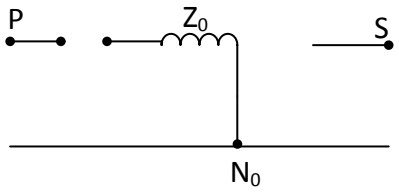


Figure 3.7: Zero sequence impedance for a Y-Δ transformer with an ungrounded wye

3.4.4 Zero sequence impedance of a Δ-Y transformer

In a delta-wye connected transformer, if the wye winding is grounded then zero sequence currents will circulate through the delta winding. In this configuration, secondary zero sequence currents will flow from the rest of the power system because of the earth return path on the wye side of the transformer. Therefore, the zero sequence impedances of other network components connected on the delta winding of the transformer will not be considered part of the total circuit impedance because the zero sequence currents will never leave the delta winding. Zero sequence network of the Δ-Y transformer is shown in Figure 3.8.

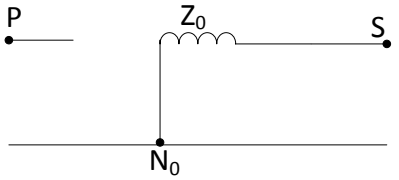


Figure 3.8: Zero sequence network of the Δ-Y transformer with wye grounded

If the wye winding of a Δ-Y transformer is not grounded, no zero sequence currents will flow in the transformer, and the equivalent circuit reflects an infinite impedance as shown in Figure 3.9.

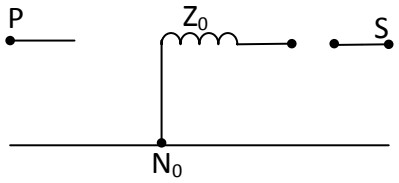


Figure 3.9: Zero sequence network of the Δ-Y transformer with an ungrounded wye

Transformer winding configuration plays an important role to find the total impedance with respect to the fault type and the location of the fault on the power system network.

Next section of this chapter discusses the electrical protection schemes for transformers which includes current differential, negative sequence, restricted earth fault, magnetizing inrush current, overexcitation, CT saturation and overcurrent.

3.5 Transformer Overcurrent Protection

"Overcurrent protection is common for transformers for phase or ground faults. This is either as the primary protection for smaller units or any unit without differential protection or as backup protection on larger units protected by differential relays. For transformer sizes of about 5 MVA and below, primary fuses or inverse-time-overcurrent relays may be used. At higher voltages, distance relays provide backup protection for the transformer and associated circuits" (Blackburn J.L. and Domin T.J., 2006). Because these devices can operate well outside the transformer protection zone, their application and setting are a combination of transformer and associated system protection.

Figure 3.10 shows the overcurrent protection for a 1 MVA transformer. Overcurrent relays respond to the magnitude of the input current and will operate when this magnitude exceeds the pre-set level (pick-up level). When this level is exceeded, the relay will close its trip contacts and energise the circuit breaker trip coils (Rockefeller G., 2007).

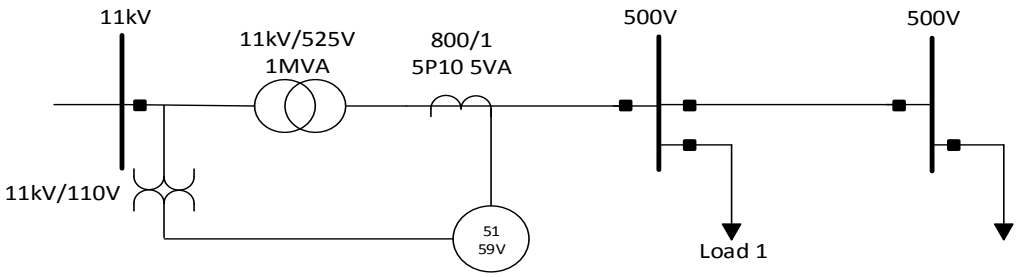


Figure 3.10: Overcurrent protection for power transformer

"Instantaneous overcurrent relays must be applied to supplement differential or overcurrent protection and provide protection for heavy primary transformer faults. They must be set in such a manner that they do not operate on magnetizing inrush (unless a harmonic restraint is used), on the maximum short-time load (cold-load), or on the maximum secondary three-phase fault. A typical overcurrent setting would be 150%-200% of the greatest of these currents" (Blackburn J.L. and Domin T.J., 2006). This may limit their operation on primary faults. The ground relays must be set above the maximum zero-sequence unbalance that can exist chiefly as the result of single-phase loading.

On the other hand, the overcurrent relays or fuses should protect the transformers against damage from through faults. High fault current passing through the transformer can cause thermal as well as mechanical damage. High temperatures

can accelerate insulation deterioration. Their physical forces from high currents can cause insulation compression, insulation water, and friction induced displacement in the windings.

3.6 Transformer differential protection scheme

The differential protection, also known as the Merz-Price circulating current principle is the most satisfactory scheme for protecting power transformers.

Figure 3.11 below shows a typical current differential relay connection diagram of a two-winding transformer.

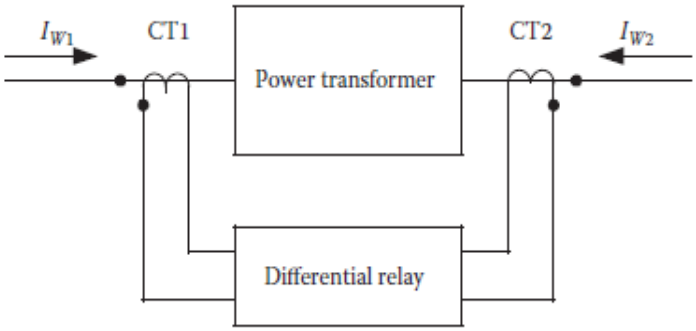


Figure 3.11: Differential protection of a two-winding power transformer (Harlow J.H., 2004)

The differential element compares the operating current with the restraining current. The operating current I_{OP} can be obtained as the phasor sum of the currents entering the protected zone. The differential current can be calculated using Equation (3.5). Under normal operating conditions their vector sum will be zero, and the operating current I_{OP} will be zero.

$$I_{OP} = |I_{W1} + I_{W2}| \tag{3.5}$$

Where:

I_{W1} and I_{W2} - currents flowing in the secondaries of the two current transformers.

According to reference (Harlow J.H., 2004), there is no standard way of calculating the restraining current. The most common methods to calculate the restraining currents are as follows:

$$I_{RT} = k|I_{W1} - I_{W2}| \tag{3.6}$$

$$I_{RT} = k(|I_{W1}| + |I_{W2}|) \tag{3.7}$$

$$I_{RT} = max(|I_{W1}|, |I_{W2}|) \tag{3.8}$$

Where

k is a compensation factor usually taken to be 1 or 0.5

I_{RT} is the restraining current

Figure 3.12 shows a typical differential relay characteristic curve (SEL-487E instruction manual, 2012).

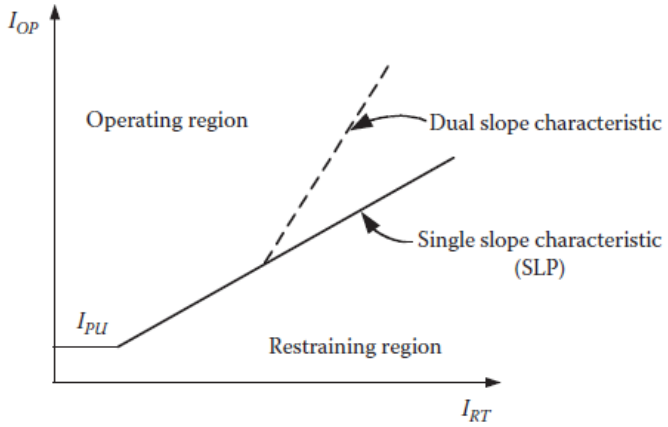


Figure 3.12: Differential relay with a dual slope characteristic

In Figure 3.12 above, the minimum pickup current of the relay is defined by the straight line labelled I_{PU}, with the relay operating region located above the slope and the restraint region below the slope. The dual slope (shown by dotted lines on Figure 3.12) provides added security against tripping during heavy through faults and CT saturation condition (Harlow J.H., 2004).

The drawback of the traditional differential protection scheme is its inability due to its insensitivity to detect low-level fault currents for a turn to turn fault conditions. According to reference (Gajic Z., 2008), the minimum pickup current for the differential relay is traditionally set between 30 to 40% on the operate-restraint characteristic curve. However, at fault inception, a minor turn to turn fault may only cause a differential current of about 15% which is not significant enough to operate the differential relay (Gajic Z., 2008).

However, with many complicating factors which are not encountered within the generator application. These obscuring factors are briefly summarised below:

- In the differential scheme, two currents (primary and secondary) are to be compared; however, these currents are never the same due to the transformer turns ratio; therefore, identical current transformers cannot be used as they will produce a differential current and operate the relay even under no fault conditions. Thus, the CT ratios have to be chosen carefully

such that their secondaries will carry identical currents (Mehta, V. and Mehta, R., 2009).

- Depending on the power transformer connection, either delta-star or star-delta there is usually a 30-degree phase shift between the primary and secondary currents of the power transformer. Because of this phase shift, a differential current will exist even if CT's of the correct turns ratio are used. This phase shift can be corrected by reversing the CT connections such that, if the power transformer is connected Star-Delta, the CT's are connected Delta-Star and vice-versa (Mehta, V. and Mehta, R., 2009). ***In modern numerical relays, the phase shift can be compensated by a Compensation Factor (CF) in the relay software settings, and it is not necessary to reverse the current transformer connections (SEL-487E instruction manual, 2012).***
- As a means for regulating voltage, most transformers are equipped with an online/on-load tap changer. When the tap changer, adjusts from one position to the other, it will cause a differential current to flow through the relay even under normal operating conditions (Mehta, V. and Mehta, R., 2009). This problem can, however, be overcome by adjusting the turns-ratio of the current transformer on the side of the power transformer provided with a tap changer.
- Another obscuring factor to consider in the transformer differential protection is the magnetizing inrush current. When a transformer is energized after it has been disconnected from the supply, a high magnetizing/inrush current flows into the transformer. Since this inrush represents a current going into the transformer without a corresponding current leaving the circuit, it is seen as a differential current by the relay. The magnetization inrush current condition is discussed in section 3.7.1 of this chapter.

While the traditional phase differential relay is undoubtedly effective for the phase to phase and phase to ground faults, it still leaves the transformer vulnerable to low-level faults; thus, a more effective way of protecting the transformer against these minor faults need to be employed. Therefore, the next section provides a detailed explanation of the negative sequence percentage differential protection scheme.

3.6.1 Combined differential and restricted earth fault scheme

"Implementation of a combined differential/REF protection scheme is made easy if a numerical relay with software ratio/phase compensation is used. All compensation is made internally in the relay. Where software ratio/phase correction is not available,

either a summation transformer or auxiliary CTs can be used." The combined differential and restricted earth fault scheme using summation CTs and auxiliary CTs are shown in Figure 3.13 and Figure 3.14 respectively, and its characteristics curve shown in Figure 3.15.

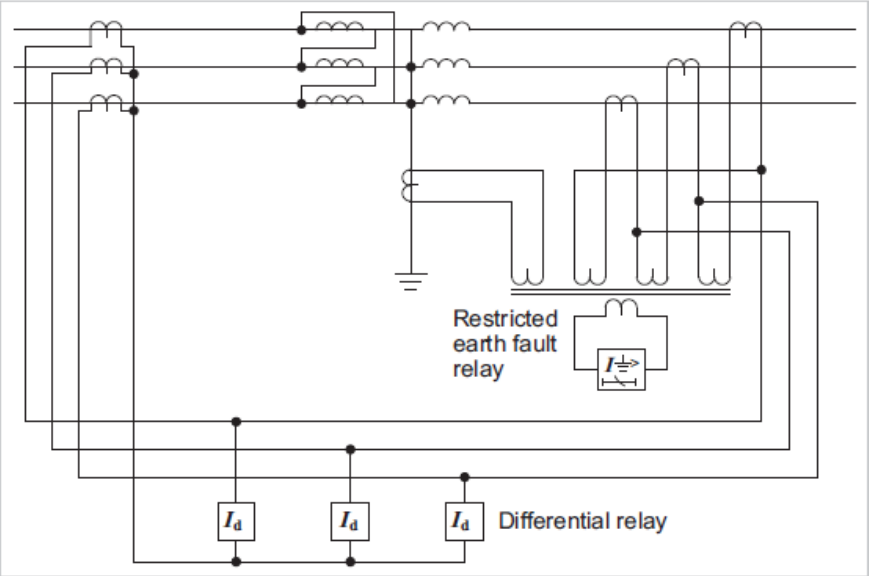


Figure 3.13: Combined differential and earth fault protection using a summation current transformer (Alstom Grid, 2011).

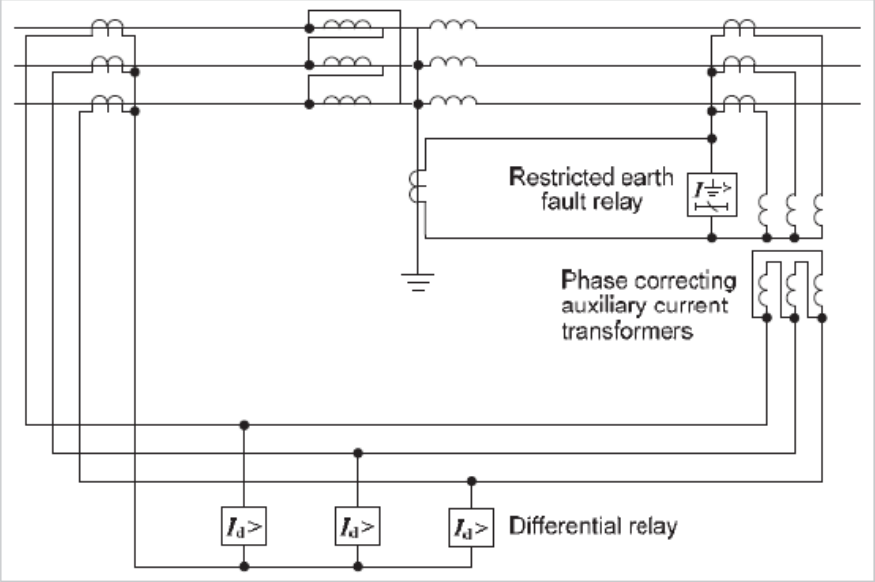


Figure 3.14: Combined differential and restricted earth fault protection using auxiliary CTs (Alstom Grid, 2011).

The settings calculations must be done very carefully, because the only substantial disadvantage of the Combined Differential/REF scheme is the restricted earth fault element operation for large internal faults along with this differential scheme (Alstom Grid, 2011).

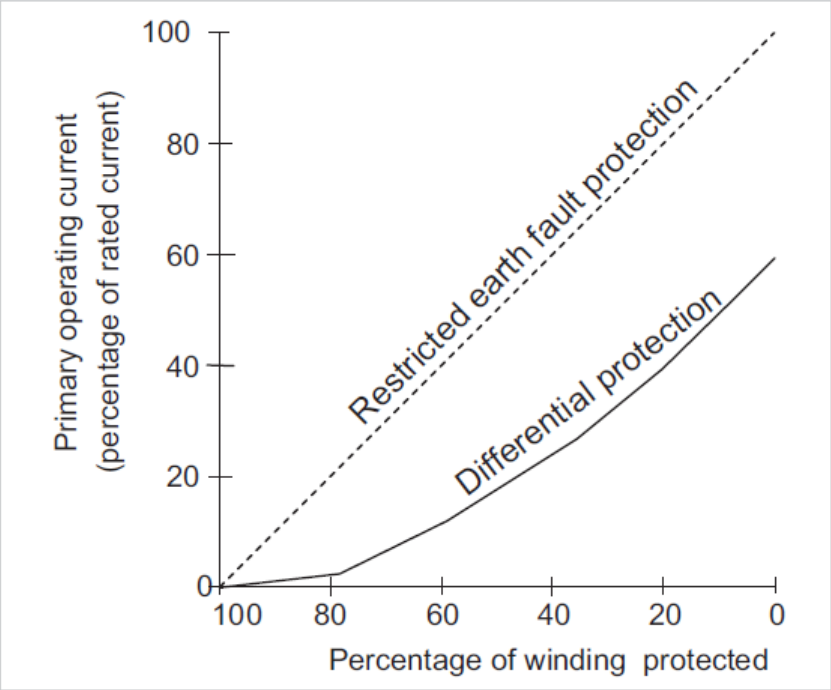


Figure 3.15: Combined differential and restricted earth fault protection characteristics

The advantages of using restricted earth fault lead to the protection system being regularly used in combination with an overall differential system. (Alstom Grid, 2011).

3.6.2 Negative sequence percentage differential protection scheme

In a balanced system, negative sequence currents do not exist. The existence of negative sequence currents in a 3-phase system presents asymmetry and is symptomatic of an abnormal condition in the power system (Mehta, V. and Mehta, R., 2009). Negative sequence currents have opposite phase rotation to positive sequence currents; hence the magnitude of negative sequence components cannot exceed that of the positive sequence components, else the phase sequence of the system would be reversed (Mehta, V. and Mehta, R., 2009).

The successful implementation of the negative sequence current based differential scheme (Gajic Z., 2008) is based on the theory of symmetrical components as follows:

- The source of negative sequence currents is at the point of fault
- Negative sequence currents flow through the negative sequence network
- Like any other currents in the network, negative sequence currents obey Kirchhoff's first law

The comparison of the traditional phase differential element and the negative sequence differential element for a fully loaded transformer is illustrated with a characteristic differential curve given in Figure 3.16.

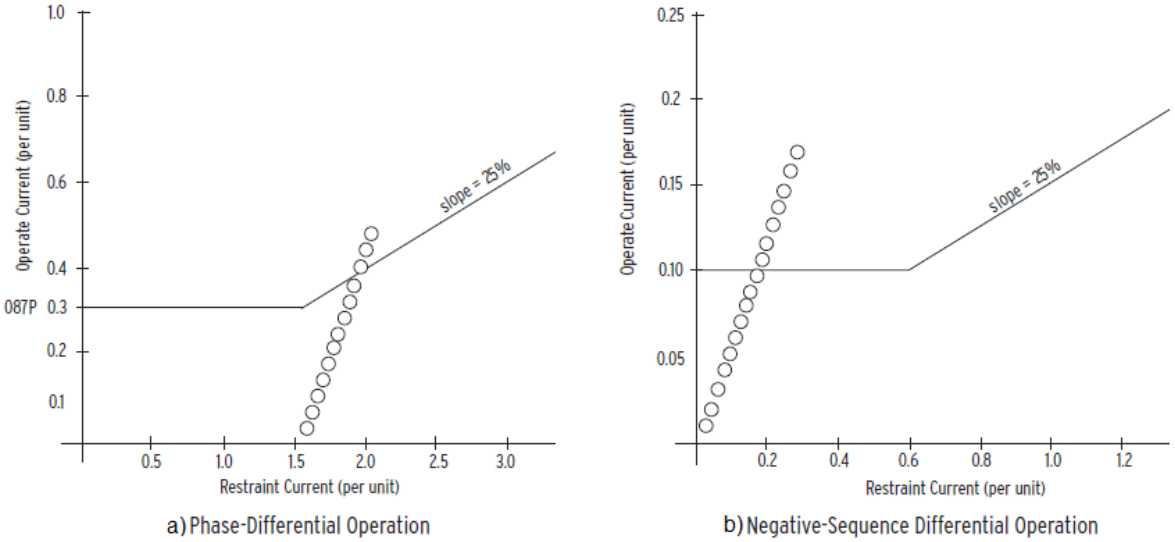


Figure 3.16: Negative sequence versus Phase differential operation (SEL-487E instruction manual, 2012)

In Figure 3.16(a), the dotted graph is a trajectory of winding inter-turn fault involving only 2% of the complete transformer winding. It should also be noted that the transformer is fully loaded at the time of fault inception. From Figure 3.16 it can be seen that the phase differential element only issues an operation command when the current reaches approximately 0.4 per unit, while the negative sequence element operates at around 0.1 per unit.

Figure 3.17 illustrates the flow of negative sequence currents in the differential protection during an external fault condition.

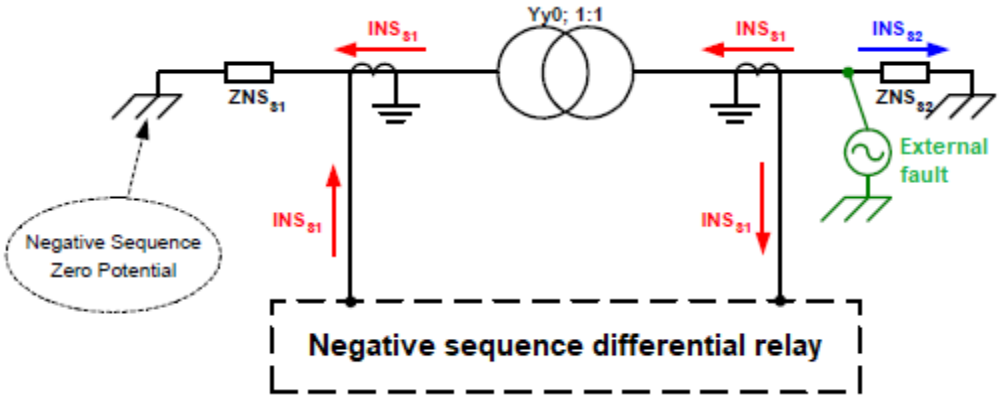


Figure 3.17: Negative sequence current flow in a differential relay during an external fault (Gajic Z., 2008)

Where:

ZNS_{S1} and ZNS_{S2} – negative sequence source impedances

INS_{S1} and INS_{S1} – negative sequence currents flowing into the transformer

From Figure 3.17 the fictitious negative sequence source is located outside the differential protection zone. The negative sequence currents on either side of the transformer will, however, have opposite directions, which is an important distinction employed in the internal/external fault discriminator in determining the position of the fault (Gajic Z., 2008). Figure 3.18 illustrates the flow of negative sequence currents for an internal fault to the power transformer.

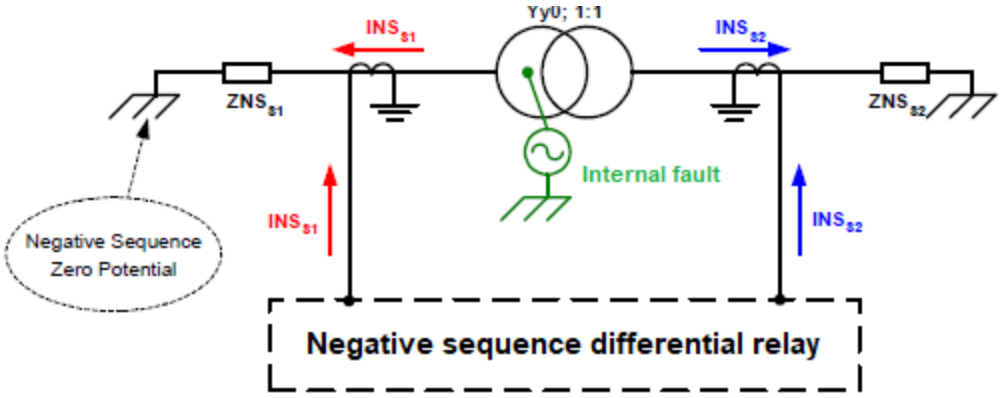


Figure 3.18: Negative sequence currents flow in a differential relay during an internal fault (Gajic Z., 2008)

Figure 3.18 shows the fictitious negative sequence source located within the power transformer. This implies that negative sequence currents will flow out of the faulted transformer on both sides. Theoretically the internal/external fault discriminator in the differential relay sees these currents as having a phase shift of zero, however, in reality, a slight phase displacement might occur between these currents owing to the likelihood of having different negative sequence impedance angles for the source equivalent circuits on the two power transformer sides (Gajic Z., 2008).

A negative sequence percentage differential relay performs the directional comparison, the magnitude of the two negative sequence currents must exceed a certain pre-set limit. This limit is usually set between 1% to 20% of the differential protection in order to prevent incorrect operation of the differential algorithm and to guarantee stability during transformer energization (Gajic Z., 2008). Once both negative sequence current phasors exceed the pre-set limit, the directional comparison is done to determine the location of the fault. The internal/external fault

discriminator will declare an internal fault if the phase shift between the two currents is between 120 and 240 degrees (Gajic Z., 2008).

The following is correct about negative sequence currents (Gajic Z., 2008).

- Negative sequence currents do not exist during three-phase symmetrical fault conditions
- Transformer configuration (Yd or Dy) does not inhibit the flow of negative sequence currents through a power transformer
- Like the positive sequence component, the negative sequence component is always transformed adequately to the other side of the transformer irrespective of it phase angle shift and type of external disturbance
- During heavy loading conditions, the resulting increase in restraint current renders the phase differential element even less sensitive than it already is to detecting winding inter-turn faults (SEL-487E instruction manual, 2012).

However, the negative sequence currents are not affected by loading conditions, and they can be used to provide sensitive and reliable protection against winding turn to turn faults inside a power transformer.

3.7 Factors affecting differential protection for transformers

When applying for differential protection, several factors must be considered (Ferrer H.J.A. and Edmund O. Schweitzer III, 2010):

- Magnetizing inrush current
- Overexcitation
- CT saturation
- Different voltage levels; hence, the current transformers are of different types, ratios, and performance characteristics.
- Phase shifts in wye–delta -connected banks.
- Transformer taps for voltage control.
- Phase shift or voltage taps in regulating transformers.

3.7.1 Magnetizing inrush current

“Transformer energization is a typical event where the magnetizing inrush current is a problem. The excitation voltage on one winding of a transformer is increased from 0V to maximum voltage when the transformer is being energized. The transformer core usually saturates, with the amount of saturation as determined by the transformer design, the remnant flux in the core, system impedance, and the point on the voltage

wave. The current required to supply this flux could be as much as forty times the full load of the transformer rating" (Hunt et al. 2007).

In a three-phase circuit, some inrush will always occur in one or two and generally all three phases, with the voltages at $120°$ apart, although it may or may not be maximum or zero in one of the phases.

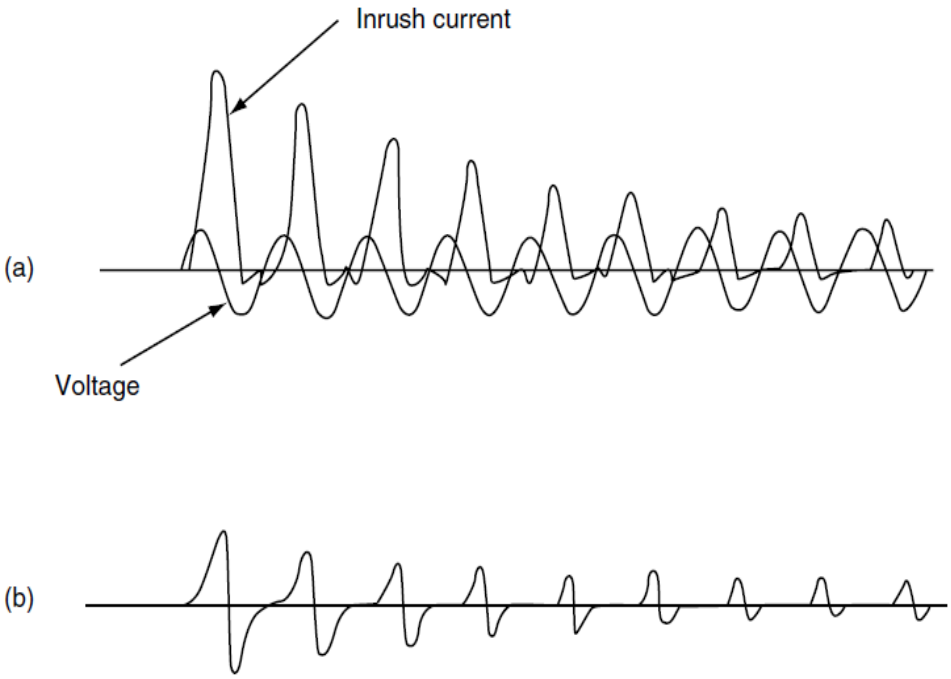


Figure 3.19: Typical magnetizing inrush current of the transformers: (a) A-phase current to wye-connected windings; (b) A-phase current to delta-connected windings (Blackburn J.L. and Domin T.J., 2006).

Figure 3.19 shows a typical magnetizing inrush current trace when a transformer bank is energised from either the wye - or delta- connected terminals. The literature review study indicated that "the second-harmonic component of the inrush wave was 15% or more of the fundamental current. In recent years, improvements in core steel and design are resulting in transformers for which all inrush current harmonics are less, with possibilities of the second harmonic being as low as 7%" (Blackburn J.L. and Domin T.J., 2006).

According to reference (Sonnemann W.K. et al., 1958), magnetizing inrush occurs in a transformer whenever the polarity and the magnitude of the residual flux do not agree with the polarity and magnitude of the ideal instantaneous value of the steady state flux. Figure 3.20 illustrates this phenomenon.

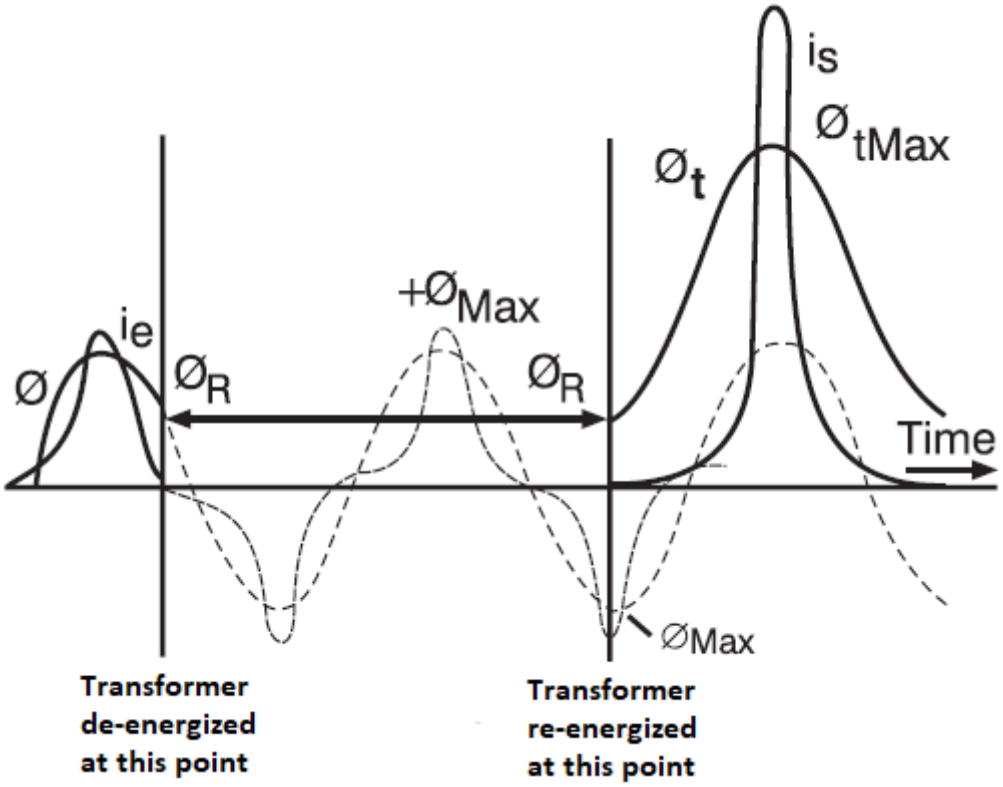


Figure 3.20: Transformer energisation waveform (G. Rockefeller, 2007)

Where:

I_S – inrush current

I_e – steady state current

Φ_R – residual flux

Φ_t – steady state flux at the point in time of energisation

From Figure 3.20 it can be seen that at the point in time of energisation, the steady-state flux is at its negative peak while the residual flux is positive. The combination of these two produces a transient current that is much greater than the steady-state current. Figure 3.21 illustrates the energisation at the point in time where the state exactly matches the residual flux.

In Figure 3.21, it can be seen that the steady state flux at the instant of energisation matches the residual flux, and so no transient/inrush current flows.

Possible causes of magnetizing inrush currents include transformer energisation, voltage recovery after clearing an external fault, and energisation of a transformer in parallel with a transformer that is already in service.

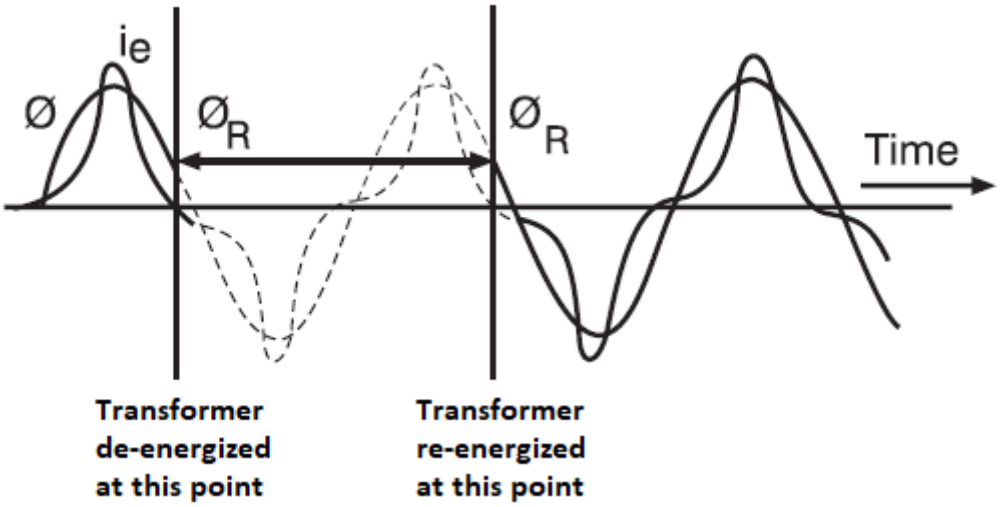


Figure 3.21: Transformer energisation without inrush (G. Rockefeller, 2007)

The magnitude of the inrush current is dictated by some factors which includes: the type of magnetic material used in the manufacturing of the transformer core, the residual flux in the power transformer at the instant of switching, and the size of the power transformer. Because the inrush current is rich in harmonics, particularly the 2nd harmonic, the filtered differential element uses the harmonic blocking to restrain the differential element from operating during transformer energisation (SEL-487E instruction manual, 2012).

3.7.1.1 Magnetizing inrush current during through fault condition

An external fault could considerably reduce the system voltage, and as a result, reduce the transformer excitation voltage. When the fault is cleared, the excitation voltage will return to the system at a normal voltage level. The restoring of the voltage could force a DC offset on the flux linkages, which will result in a magnetizing inrush current. At this point, the magnetizing inrush current will be less than that of the energisation, as there is no remnant flux present in the core. Therefore, the current measured by the differential relay will be quite linear due to the presence of the load current and could result in a low level of second harmonic currents.

3.7.1.2 Sympathetic inrush current

Energizing a power transformer can cause sympathetic magnetizing inrush current to flow in a parallel transformer that is already energised as shown in Figure 3.22. By energizing the second transformer, voltage drop across the resistance of the line feeding (source) the transformer is experienced. This voltage drop can cause saturation in the transformer that is already energised, in the negative direction.

This saturation causes the magnetizing inrush current to provide the flux. In this case, the magnitude of the magnetizing inrush current is usually not as severe as in the other cases. The inrush and sympathetic current waveforms are shown in Figures 3.22(a) and 3.22(b) respectively where I_1 is the inrush current and I_2 is the sympathetic inrush current.

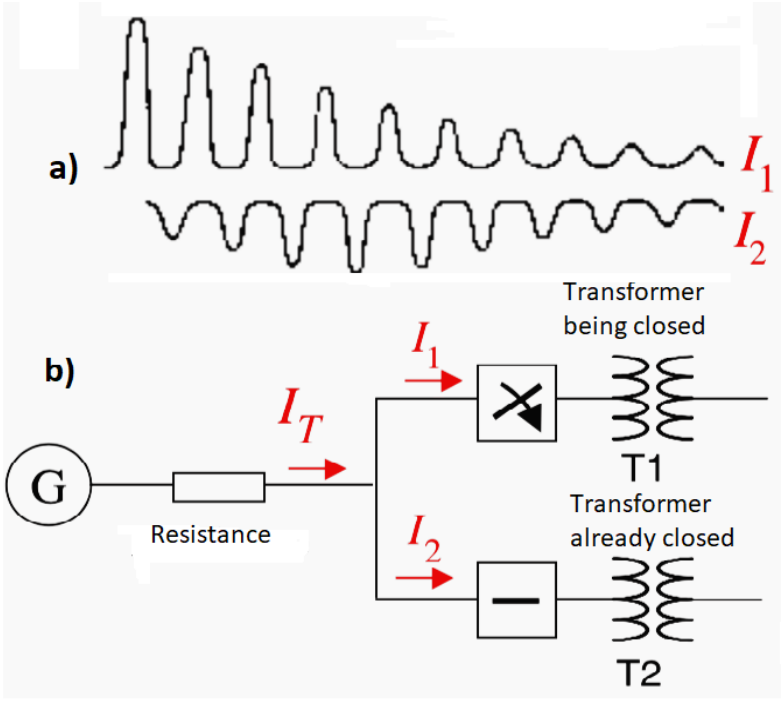


Figure 3.22: a) typical waveforms of inrush and b) sympathetic inrush electrical circuit connection (H. Bronzeado and R. Yacamini, 1995)

3.7.2 Overexcitation

The flux level within a transformer is proportional to the voltage applied to the transformer and inversely proportional to the frequency of the applied voltage.

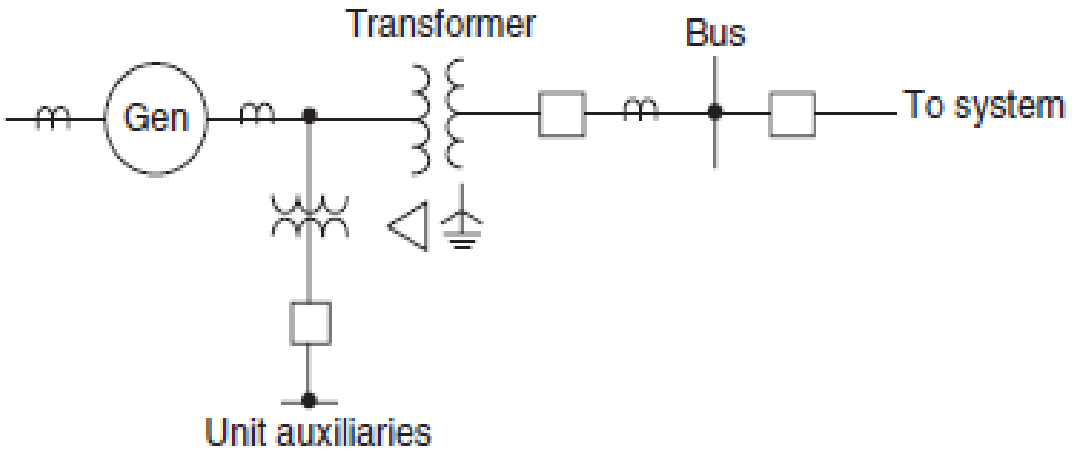


Figure 3.23: Unit generator-transformer connected

When the overexcitation condition occurs, the transformer core becomes saturated resulting in a build-up of heat with eventual damage to the transformer.

“Generator unit transformers are especially subject to overexcitation as such transformers are directly connected to the generator terminals. Voltage and frequency at the generator terminals are subject to voltage and frequency variations, especially during start-up of the generator” (Blackburn J.L. and Domin T.J., 2006).

Overexcitation protection should consist of relaying that is capable of directly responding to the level of excitation that exists such as volts/hertz relaying.

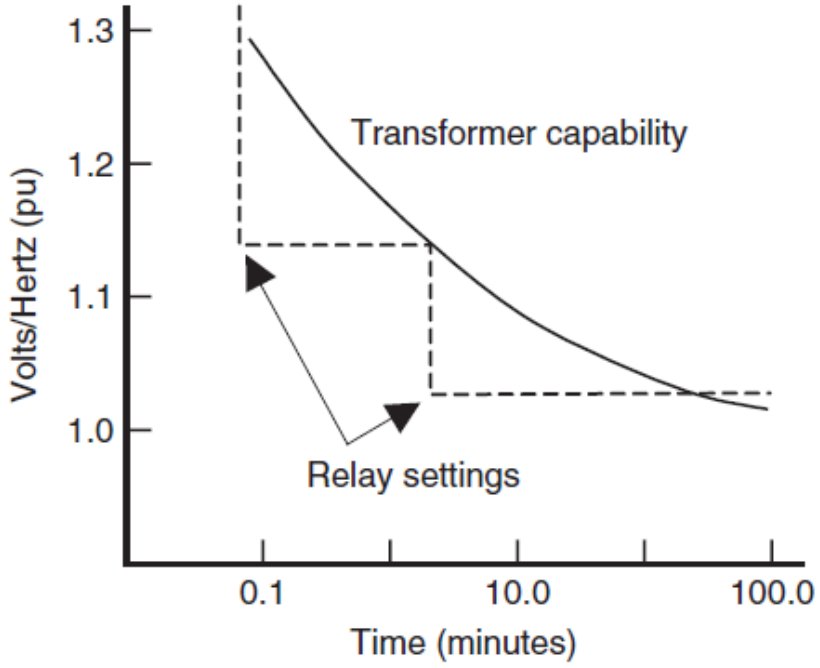


Figure 3.24: Volts/hertz curves of the transformer (Stanley H. Horowitz and Arun G. Phadke, 2008)

A typical capability curve is shown in Figure 3.24. Many volts/hertz relays have two settings, a lower setting for alarm and a higher setting which may be used for tripping (Horowitz and Phadke, 2008). The magnetic cores of generators and transformers should operate at or below rated flux density to keep thermal losses and dielectric stresses within acceptable boundaries. The magnetic flux in generators and transformers is directly proportional to the applied voltage and inversely proportional to the operating frequency. A volts-per-hertz element (24) can provide generator and transformer overexcitation protection. The generator protection relays offer the following types of characteristics for the volts-per-hertz protection element:

1. Definite-time characteristic
2. Dual-level definite-time characteristic
3. Inverse-time characteristic
4. Combination of definite-time and Inverse-time characteristics.

“Transformer differential relays are subjected to operation on high transformer excitation current. However, the operating characteristic of the relay on such current does not correlate well with transformer overexcitation limit characteristics. As such, it is not practical to use differential relaying as a means to protect transformers against overexcitation. On the downside, transformer differential relays are subject to operating on overexcitation current at levels below in which may cause damage to the transformer. Moreover, the operation of differential relay caused by overexcitation condition could confuse to post-disturbance investigations” (Blackburn J.L. and Domin T.J., 2006).

Therefore, larger transformers, for which overexcitation is a concern, should be equipped with dedicated overexcitation protection and associated differential relaying should be blocked from operating for the overexcitation condition.

3.7.3 CT Saturation

When a fault occurs, it might cause a CT to saturate if it is not adequately sized to handle the fault current. According to reference (Rockefeller G., 2007), saturation of CTs happens in terms of the AC and DC components of the current passing through it. The AC saturation effect refers to the inability of the CT to reproduce the symmetrical current conditions faithfully, while the DC saturation effect refers to the saturation that occurs when the current contains the decaying DC component associated with a fault or magnetizing inrush. Figure 3.25 shows an AC waveform obtained from the secondary side of a saturated current transformer (SIEMENS, 2007).

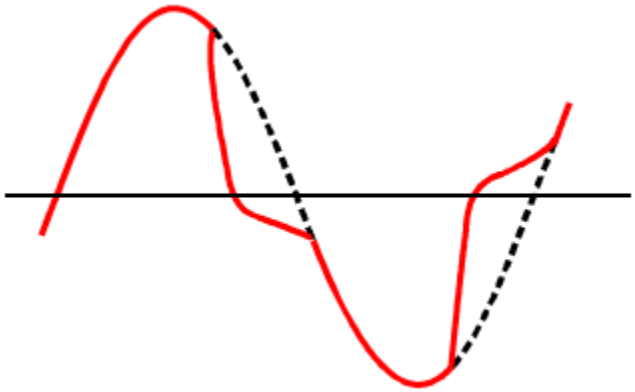


Figure 3.25: AC saturation waveform (SIEMENS, 2007)

In Figure 3.25, it can be seen that the CT is unable to reproduce the complete AC sinusoidal waveform. Figure 3.26 shows a current waveform obtained from the secondary side of a current transformer saturated with DC component (SIEMENS, 2007).

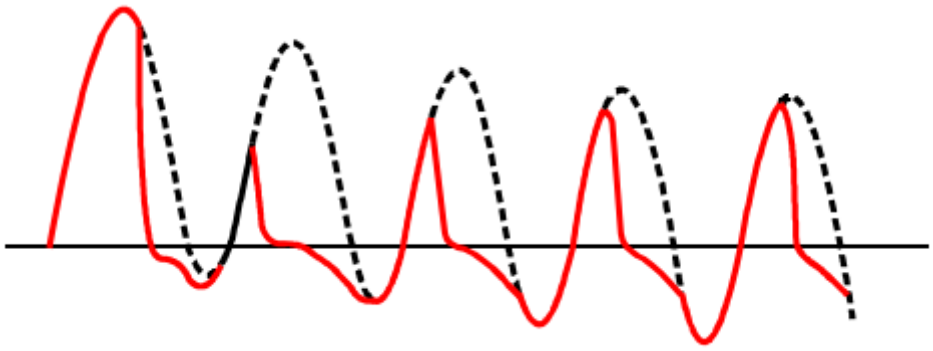


Figure 3.26: Current transformer DC saturation (SIEMENS, 2007)

According to reference (Gajic Z., 2008), a CT that experiences negligible distortion under symmetrical AC conditions might become saturated and give a heavily distorted output which contains a quite high level of the second harmonic component. Therefore, a delayed operation of the restrained differential protection on internal faults might occur.

“Current transformer saturation associated with transformer differential relaying causes several concerns about such relaying (Blackburn J.L. and Domin T.J., 2006):

- CT saturation on external faults can cause incorrect operation of differential relaying due to the operating current that can result from the distorted secondary current waveforms that exist during such conditions.
- The harmonics contained in secondary currents of a saturated current transformer may delay operation of transformer differential relaying on internal transformer faults.”

Therefore, proper selection of current transformers will minimise exposure to the problems listed above. Design features of transformer differential relay also address CT saturation problem.

Next section discusses the mechanical protection of the transformer which includes Buchholz and sudden pressure relay principles and thermal protection schemes.

3.8 Mechanical fault-detection for transformers

"The accumulation of gas or changes in pressure inside the transformer tank are good indicators of internal faults. The Buchholz and sudden pressure relay devices are recommended, wherever they can be applied, as excellent supplementary protection. They are frequently more sensitive and operate on light internal faults that are not detected by differential or other relays. However, it is important to recognise that their operation is limited to problems inside the transformer tank" (Ferrer H.J.A. and Edmund O. Schweitzer III, 2010). They will not operate for faults in the transformer bushings or the connections to the external CTs. Therefore, the protection zone of these devices is only within the tank, on the contrary of the differential protective zone given in Figure 3.11.

3.8.1 Buchholz relay

"Gas detection devices can be applied only to transformer units built with conservator tanks. For these units with no gas space inside the transformer tank, a gas accumulator device commonly known as the Buchholz relay is connected between the main and the conservator tanks. It collects any gas rising through the oil. One part of the relay accumulates gas over time to provide a sensitive indication of low-energy arcs. It is used generally to set off an alarm, as tolerable operating conditions may generate gas. The other part responds to heavy faults, forcing the relay to open at high velocity and used to trip in parallel with the other transformer protection" (Ferrer H.J.A. and E.O. Schweitzer III, 2010).

Buchholz relay is a gas-actuated relay installed on oil-immersed transformers for the protection against internal faults of all kind including incipient faults such as winding insulation failure, core heating and fall of oil level due to leaking joints (Mehta, V. and Mehta, R., 2009). The Buchholz relay, usually installed in the pipe connecting the conservator to the main tank, would issue an alarm in the case of an incipient fault and immediately disconnect the transformer from the supply in the case of a severe fault event. Figure 3.27 shows the internal arrangement of a Buchholz relay.

The operation of the Buchholz relay can be summarised as follows:

- During incipient faults, the heat generated causes decomposition of some transformer oil in the main tank. The decomposition containing more than 70% hydrogen gas Hydrogen gas is very light, it rises to the top of the tank and tries to get into the conservator, however in the process it gets trapped in the upper part of the Buchholz relay chamber. After a predetermined amount of gas has accumulated, it will possess enough energy to exert sufficient pressure on the float, causing it to tilt the mercury switch and close the alarm circuit (Mehta, V. and Mehta, R., 2009).

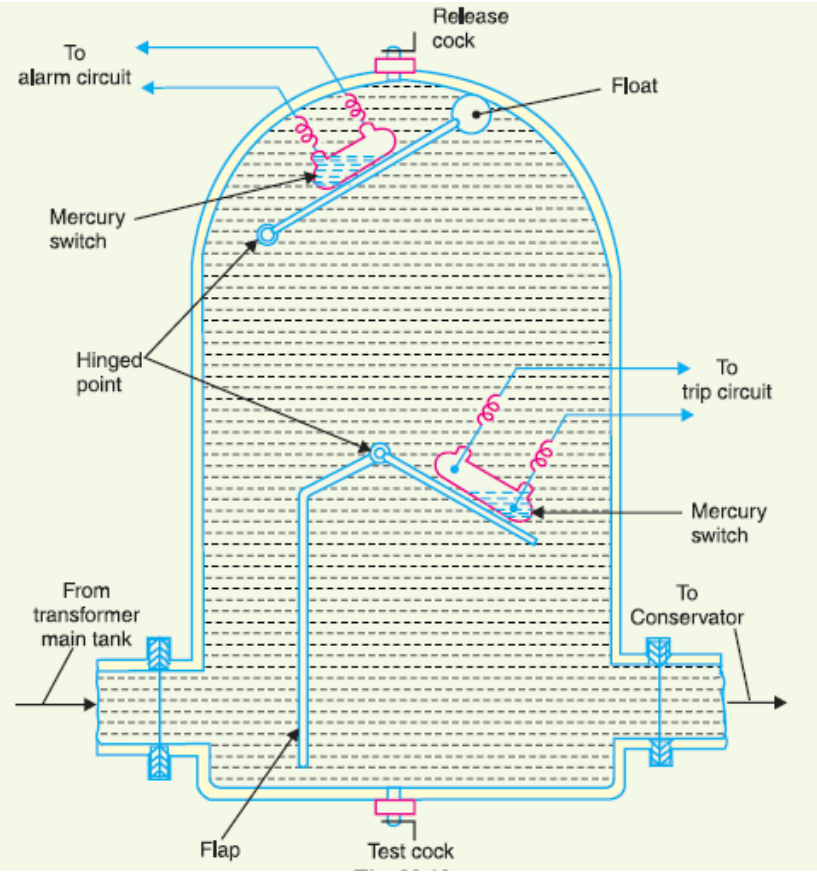


Figure 3.27: Buchholz relay internal arrangement (Mehta, V. and Mehta, R., 2009)

- If a severe internal fault occurs, a significant amount of gas is produced in the main tank. Because this gas possesses so much expulsive force, it forces some of the oil out of the main to tank into the conservator tank via the Buchholz relay. In doing so, the oil passing through the Buchholz relay tilts the flap to close the contacts of the mercury switch. This then completes the trip circuit, sending a trip signal to the circuit breaker and the transformer gets disconnected from the supply (Mehta, V. and Mehta, R., 2009).

3.8.2 Sudden pressure relay

“Sudden pressure device shown in Figure 3.28 is applicable to oil-immersed transformers and operates on sudden changes in the gas above the oil or sudden changes in the oil itself. Both have equalising means for slow changes in pressure, which occur with loading and temperature changes. They are sensitive to both low and high energy arcs within the transformer and have inverse-time characteristics: fast for high fault currents and slow for low fault currents” (Ferrer H.J.A. and E.O. Schweitzer III, 2010). They can be used to trip with the contacts in parallel to the differential protection and other relay trip contacts, while they can be used to initiate an alarm if desired.

“Incorrect operations of sudden pressure relays have been experienced on faults external to the transformer. This is the main reason that some users have been reluctant to connect sudden pressure relays to trip. False trips are usually associated with faults that result in high fault current through the transformer. Such faults can cause movement of materials (gas or oil) within the transformer, which results in an operation of the sudden pressure relay. This is more likely to occur on older transformers in which the structural integrity of the bracings within the transformer has weakened over time” (Ferrer H.J.A. and E.O. Schweitzer III, 2010). Sudden pressure relay is shown in Figure 3.28

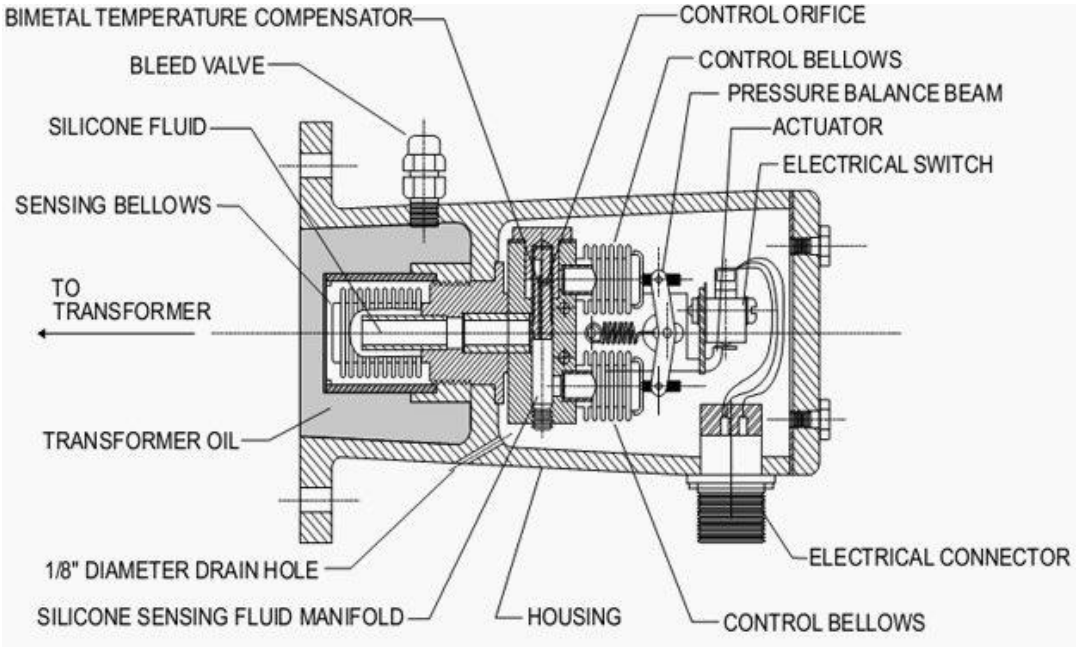


Figure 3.28: Sudden pressure relay

“One strategy that can be used to address this problem is to supervise the sudden pressure relay with a fault detector relay. The fault detector relay blocks tripping by

sudden pressure on heavy faults, which may result in false trips. Their ability to detect and isolate the transformer on low-level arcing faults before failure, preventing major internal damage, is a major benefit of applying sudden pressure relays" (Ferrer H.J.A. and E.O. Schweitzer III, 2010).

3.8.3 Transformer thermal protection

"Thermal protection is usually supplied as a part of the transformer. Generally, it is used for monitoring and initiating an alarm, but may be used for tripping. Transformers can become overheated when overloaded beyond design limits. Such overloads are likely to occur when the system is highly loaded or during emergency-operating conditions. When thermal devices operate under such conditions, it is felt best to alert operators to the condition so that remedial actions can be initiated. Tripping under such conditions is not recommended as immediate damage to the transformer is unlikely and removing a transformer from service when the power system is under stress can lead to more severe operating problems. Tripping is sometimes incorporated into the thermal protection scheme when a malfunction in the transformer cooling system (i.e., fan or pump failure) is detected in conjunction with the operation of thermal devices" (Horowitz and Phadke, 2008).

In order to detect overheating to detect overheating of the oil, tank, tank terminals, failures of the cooling system, hot spots etc., several types of thermal indicators can be used. These devices may initiate forced- cooling equipment.

3.9 Common failures in power transformer

It is generally believed that failures internal to a transformer occur when a transformer component or structure is no longer able to withstand the stresses imposed on it during operation (Ding H. et al., 2009). While in operation, the power transformer suffers the impact of thermal, mechanical, chemical, electrical and electromagnetic stress during normal and transient conditions which result in the following factors:

- The reduction in dielectric strength
- The reduction in mechanical strength
- Reduction in the thermal integrity of the current carrying circuit (i.e. the ability to withstand extended overloads)
- Reduction in electromagnetic integrity

When the operating stress exceeds the withstand strength of the transformer with respect to any one of the above properties, a failure ultimately occurs. Table 3.1 provides the summary of the different transformer failures (Ding H. et al., 2009).

Table 3.1: Common transformer failures

System, Component	Possible Defect	Fault and Failure Mode
Dielectric system • Major insulation • Minor insulation • Leads insulation • Electrostatic screens	• Abnormal oil ageing • Abnormal paper ageing • Partial Discharges • Excessive water • Oil contamination • Surface contamination	Flashover due to: • Excessive paper ageing • Destructive partial discharges • Creeping discharges • Localised surface tracking
Mechanical system • Clamping • Windings • Leads support	• Loosing winding clamping	Failure of solid insulation due to: • Failure of leads support • Winding displacement (radial, axial, twisting)
Electromagnetic circuit • Core • Windings • Structure insulation • Clamping structure • Magnetic shields • Grounding circuit	• Circulating current • Leakage flux • Ageing laminations • Loosing core clamping • Floating potential • Shor-circuit	Excessive gassing due to: • General overheating • Localised overheating • Arcing/sparking discharges • Short-circuited turns in winding conductors
Current-carrying circuit • Leads • Winding conductors	• Bad joint(s) • Bad contacts • Contact deterioration	Short-circuit due to: • Localised overheating

From Table 3.1, this thesis only considers the failures on the electromagnetic circuit due to short-circuited turns in winding conductors and the DIgSILENT simulation results for this case is given in chapter 4.

3.10 Conclusion

This chapter provided a theoretical overview of the electrical and mechanical protection for a power transformer such as differential, negative-sequence differential, transformer overcurrent protection, Buchholz relay and sudden-pressure relays to provide sensitive detection of internal faults to the transformer tank and monitoring of the transformer during thermal overload and excessive through-fault current conditions.

Protection of a transformer against damage due to the failure to clear an external fault should always be carefully considered. This damage usually manifests itself as internal, thermal, or mechanical damage caused by fault current flowing through the transformer. Through-faults that can cause damage to the transformer include restricted faults or those some distance away from the station such as the system short circuits. The fault current, in terms of the transformer rating, tends to be low approximately 0.5 to 5.0 times transformer rating (Rockefeller G., 2007) and the bus voltage tends to remain at relatively high values. The fault current can be superimposed on load current, making up the thermal load on the transformer.

Overcurrent relays are used for transformer backup; their sensitivity can be limited because they should be set above maximum load current. Separate ground relays may be applied with the phase relays to provide better sensitivity for some ground faults.

“When overcurrent relays are applied to the high-voltage side of transformers with two or more windings, they should have pickup values that will permit the transformer to carry its rated load current plus a margin for overload. Overcurrent relays on individual transformers may require pickup levels greater than twice the forced cooled rating of the transformer to avoid tripping” (IEEE, 2008). Higher pickup levels result in a loss of backup protection sensitivity. Improper pickup setting of the overcurrent relay will lead to its tripping during the inrush current conditions.

Several factors influence the decision to determine what kind of backup protection is required for the transformer. Significant factors are the i) clearing remote faults, ii) the cost effectiveness to provide the zone of protection, iii) the transformer rating and location of the transformer, and iv) the utility general protection philosophies.

The next chapter provides the implementation of the transformer differential protection scheme using DIgSILENT Power Factory simulation tool.

CHAPTER FOUR
DIGSILENT IMPLEMENTATION OF THE DIFFERENTIAL AND OVERCURRENT PROTECTION SCHEMES FOR POWER TRANSFORMER

4.1 Introduction

A power transformer is a very valuable and vital link in a power transmission system. High reliability of the transformer is essential to avoid disturbances in the transmission of power. A high-quality power transformer should be adequately designed and supplied with suitable protective relays and monitors the power system in a very reliable manner. The author (R. Nylen, 1988) suggested that less than one fault in one hundred transformers per year can be expected. When a fault occurs in a transformer, the damage usually is severe. The transformer has to be transported to a workshop and be repaired, which takes considerable time. To operate a power transmission system with a transformer out of service is always difficult. Frequently, the impact of a transformer fault is more severe than a transmission line outage. The three-phase power transformer protection with the rating power above 5 MVA is protected using a differential relay and a back-up protection with an overcurrent relay.

This chapter presents the DIgSILENT simulation and analysis of the protective relaying system for the power transformer. The transformer differential protection is implemented using SEL-487E and SEL-751A with an overcurrent relay as a back-up protection in the DIgSILENT software environment.

The performance of the transformer protective relaying system is studied through simulations of the external and internal faults and inrush current conditions. The IEEE 14-Bus transmission system is selected as a case study. The IEEE 14-Bus test case represents a portion of the American Electric Power System (in the Midwestern US) as of February 1962. IEEE systems are used by researchers to implement and test the innovative ideas and concepts using the power system simulation software tools.

Figure 4.1 shows the single line diagram of the IEEE 14-Bus system. The considered IEEE 14 Bus System consists of 14 buses (nodes), 5 generators, 11 loads, 16 lines, 5 transformers and one shunt capacitor, three 2-winding transformers (Trf2, Trf3 and Trf4) connected at Bus 7, Trf5 and Trf1 are connected at Bus 4 and Bus 5 respectively as shown in Figure 4.1.

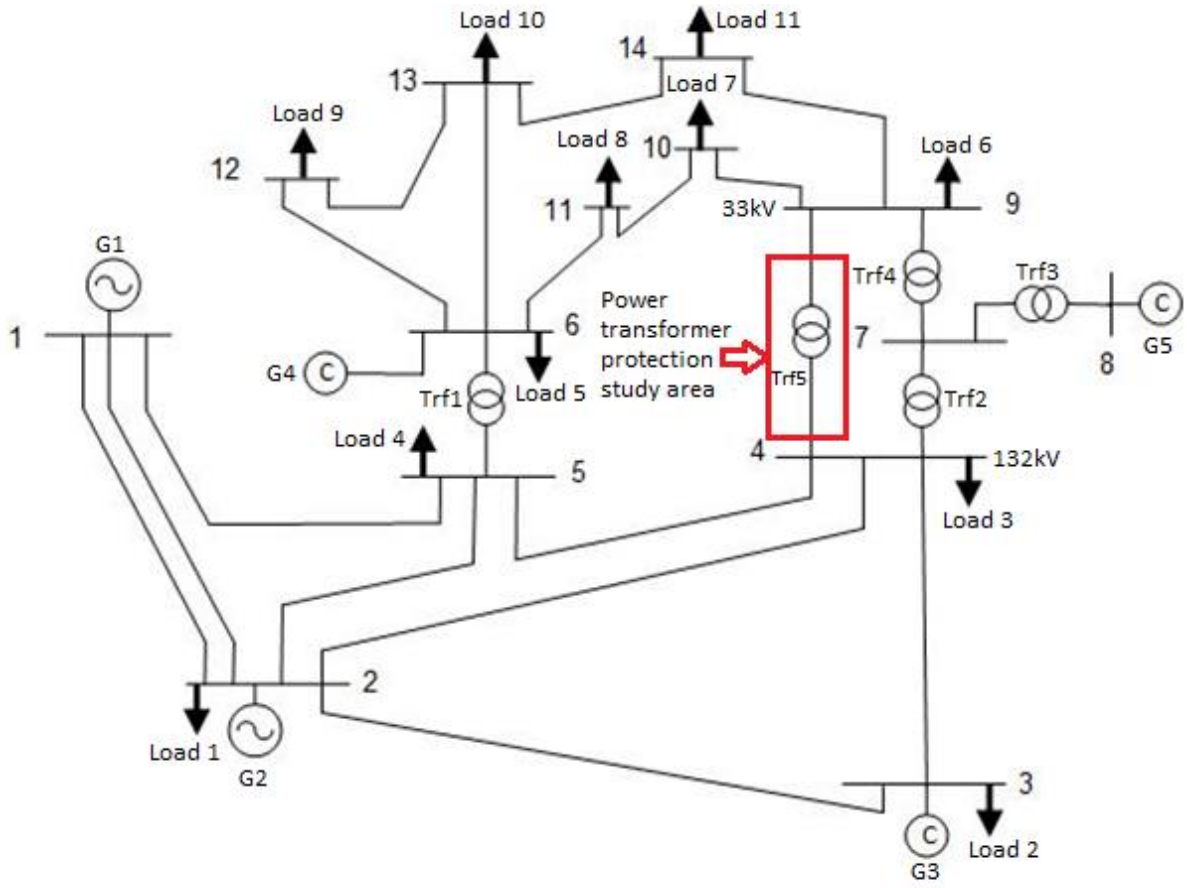


Figure 4.1: Single-line diagram of the IEEE 14-Bus system

4.2 IEEE 14-Bus system

The input data of the IEEE 14 bus system is given in Tables 4.1,4.2 and 4.3 respectively. Table 4.1 presents the magnitudes of the bus voltages in rated and per unit values. The buses which consist of the generators and loads are also given in Table 4.1.

Table 4.1: IEEE 14-Bus network bus data

Bus data							
Bus no.	**V(pu)**	**V_{rated} (kV)**	**δ (deg)**	**P_G (MW)**	**Q_G (MVar)**	**P_L (MW)**	**Q_L (MVar)**
1	1.06	132	0	232.9	-16.8	-	-
2	1.04	132	-5	40	43.1	21.7	12.7
3	1.01	132	-12.7	-	23.9	94.2	19
4	1.02	132	-10.4	-	-	47.8	-3.9
5	1.02	132	-8.8	-	-	7.6	1.6
6	1.07	33	-13.9	-	10.1	11.2	7.5
7	1.06	1	-13.6	-	-	-	-

8	1.09	11	-13.6	-	18.8	-	-
9	1.05	33	-15.3	-	-21.0	29.5	16.6
10	1.05	33	-15.3	-	-	9	5.8
11	1.05	33	-15.3	-	-	3.5	1.8
12	1.06	33	-14.6	-	-	6.1	1.6
13	1.06	33	-14.6	-	-	13.5	5.8
14	1.02	33	-17.1	-	-	14.9	5

Table 4.2 provides the bus type, voltage and power capabilities of the generators and condensers of the considered IEEE 14 bus system.

Table 4.2: Generator and condenser input data of the IEEE 14-Bus system

Generator and condenser				
Generator Name	**Bus Type**	**Voltage in p.u.**	**Minimum capability in MVA**	**Maximum capability in MVA**
Gen_0001	Slack	1.060	-	-
Gen_0002	PV	1.045	-40.0	50.0
Gen_0003	PV	1.010	0.0	40.0
Gen_0006	PV	1.070	-6.0	24.0
Gen_0008	PV	1.090	-6.0	24.0

Table 4.3 provides the transmission line parameters of the IEEE 14 bus system

Table 4.3: Transmission line parameters of the IEEE 14-Bus system

Line Name	**Impedance in polar form** $Z\angle\delta$		**Impedance in rectangular form** $Z = R + jX$	
	Z1(Ω)	δ	**R1(Ω)**	**X1(Ω)**
L1-2-01	21.69739	71.86478	6.753542	20.61956
L1-2-02	21.69739	71.86478	6.753542	20.61956
L1-5	39.98651	76.38279	9.414187	38.8625
L2-5	31.88047	71.8651	9.922968	30.29685
L2-4	32.34747	71.75926	10.12509	30.722
L2-3	35.45266	76.64742	8.187537	34.49428
L3-4	32.00595	68.60462	11.67582	29.80027
L4-5	7.697139	72.40999	2.326104	7.337246
L6-12	3.090643	64.33693	1.33849	2.785771
L6-13	1.591062	63.07893	0.7203735	1.41864
L6-11	2.400311	64.4743	1.034332	2.166021

L12-13	3.244373	42.1376	2.405819	2.176693
L13-14	295.567	63.84204	130.2999	265.2957
L10.-11	2.274501	66.86842	0.8935243	2.091643
L9-10	0.9832489	69.37118	0.3464109	0.9202054
L9-14	3.253584	64.82103	1.384228	2.944439

Table 4.4 provides the load demand of the IEEE 14-Bus system

Table 4.4: Load demand of the IEEE 14-Bus system

Load demand			
Load Name	**Bus No**	**P in MW**	**Q in Mvar**
Load_0002	Bus_0002	21.7	12.7
Load_0003	Bus_0003	94.2	19.0
Load_0004	Bus_0004	47.8	-3.9
Load_0005	Bus_0005	7.6	1.6
Load_0006	Bus_0006	11.2	7.5
Load_0009	Bus_0009	29.5	16.6
Load_0010	Bus_0010	9.0	5.8
Load_0011	Bus_0011	3.5	1.8
Load_0012	Bus_0012	6.1	1.6
Load_0013	Bus_0013	13.5	5.8
Load_0014	Bus_0014	14.9	5.0

Table 4.5 provides the transformer data of the IEEE 14-Bus system

Table 4.5: Transformers data of the IEEE 14-Bus system

Transformers data							
Transformer Name	**From Bus**	**To Bus**	**HV in kV**	**LV in kV**	**R in p.u.**	**X in p.u.**	**Transformer turns ratio**
Trf_0004_0007	4	7	132.0	1.0	0.0	0.20912	0.978
Trf_0004_0009	4	9	132.0	33.0	0.0	0.55618	0.969
Trf_0005_0006	5	6	132.0	33.0	0.0	0.25202	0.932
Trf_0007_0008	7	8	11.0	1.0	0.0	0.17615	0.000
Trf_0007_0009	7	9	33.0	1.0	0.0	0.11001	0.000

4.3 Load flow study of the IEEE 14-Bus system

Load flow study was used to determine if the system voltages remained within specified limits of +/- 10% as per IEEE/IEC standard under normal operating conditions and check whether the transformers and transmission lines are overloaded. With the use of a simplified notation of a single-line diagram, it is easy to analyse the normal steady-state operation of the power systems focusing on various aspects of parameters such as voltages, voltage angles, real power and reactive power.

Transformer protection relay is connected between bus 4 and 9 in the considered study area. The transformer differential relay SEL-487E is connected between bus 4 and 9 as shown in Figure 4.1 and 4.6 respectively. The overcurrent relay SEL-751A is considered as the backup protection and is connected on the primary side of the step-down transformer 132 to 33kV. The steady state performance of the IEEE 14-bus system is analysed by conducting the load flow study and monitor the system voltage levels and current magnitudes on the protected zone (between bus 4 and 9) of the considered IEEE 14-bus system.

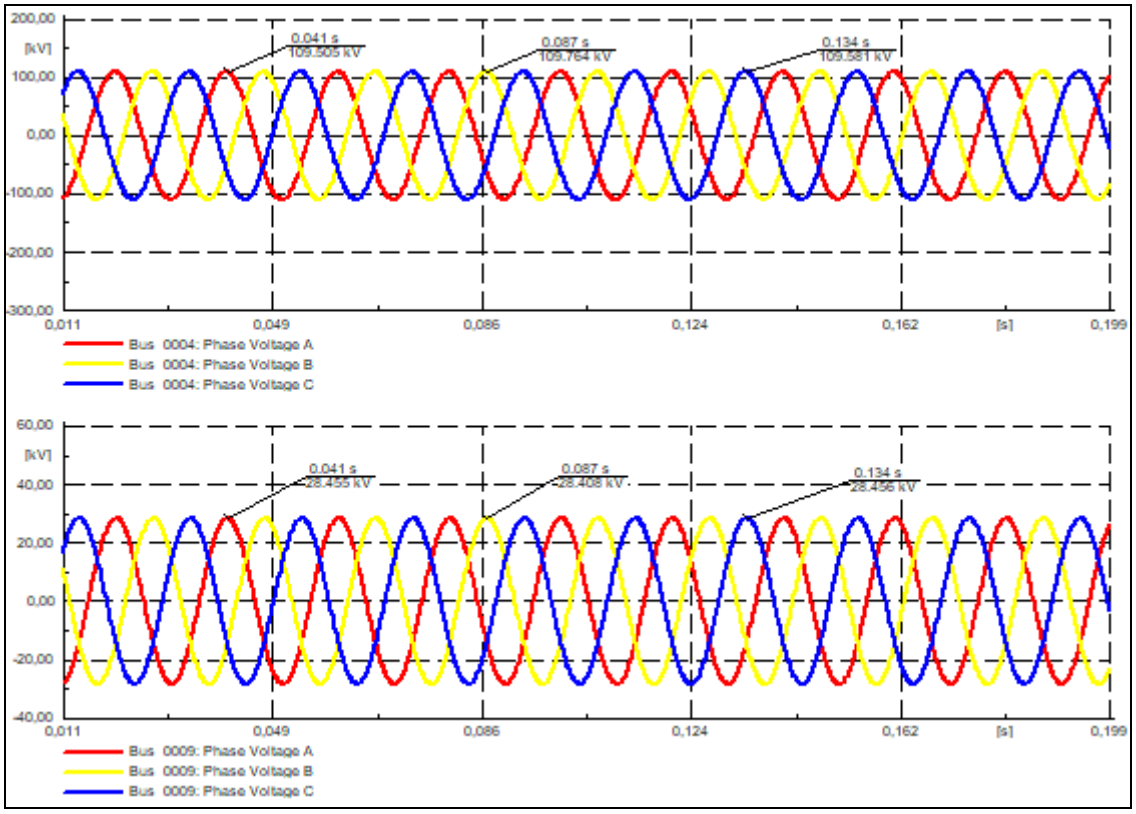


Figure 4.2: Three-phase voltages at Bus 4 and Bus 9 during normal operating conditions of the transformer

Figure 4.2 shows the RMS magnitude of the phase voltages at buses 4 and 9 which correspond to $V_L = 109.505 \times \frac{\sqrt{3}}{\sqrt{2}} = 134.12\,kV$ and $V_{pu} = \frac{134.12}{132} = 1.016\,pu$ and $V_L = 28.455 \times \frac{\sqrt{3}}{\sqrt{2}} = 34.85\,kV$ and $V_{pu} = \frac{34.85}{33} = 1.056\,pu$ for bus 4 and bus 9 respectively.

The load flow is successfully executed, and the results of the three phase voltages are shown in Figure 4.2 above, where phase A is represented in red, phase B in yellow and phase C in blue. The results show that the voltages and currents are balanced with a 120 degrees phase shift, and it is recorded during the normal system operating condition of the IEEE 14-Bus transmission system. Table 4.6 provides the voltage profile of the IEEE 14-bus system; it shows that voltage profile deviation of the calculated load flow results is within +/-10% tolerance limit according to the IEEE standard 141-1993 voltage criteria (IEEE standard, 1994).

Table 4.6: Bus voltage load flow results of the IEEE 14 bus system

Grid: Grid	System Stage: Grid	Study Case: 01 - Load Flow Case Origin	Annex: / 4

	rtd.V [kV]	Bus - voltage [p.u.]	[kV]	[deg]	Voltage - Deviation [%] −10 −5 0 +5 +10
Bus_0001	132,00	1,060	139,92	0,00	
Bus_0002	132,00	1,045	137,94	-4,98	
Bus_0003	132,00	1,010	133,32	-12,72	
Bus_0004	132,00	1,019	134,46	-10,32	
Bus_0005	132,00	1,020	134,67	-8,78	
Bus_0006	33,00	1,070	35,31	-14,22	
Bus_0007	1,00	1,062	1,06	-13,37	
Bus_0008	11,00	1,090	11,99	-13,37	
Bus_0009	33,00	1,056	34,86	-14,95	
Bus_0010	33,00	1,051	34,69	-15,10	
Bus_0011	33,00	1,057	34,88	-14,80	
Bus_0012	33,00	1,055	34,82	-15,08	
Bus_0013	33,00	1,050	34,66	-15,16	
Bus_0014	33,00	1,036	34,18	-16,04	

Figure 4.3 depicts the voltage profile of the IEEE 14-bus system. In Figure 4.3, the bus number on the x-axis and the voltage magnitude in per unit on the y-axis. The voltage at the majority of the buses are within the maximum (1.1 pu) and minimum (0.9 pu), i.e. 10% tolerance limit. However, the voltage at bus 8 has a magnitude of 1.09 which is very close to 1.1pu; therefore, a warning signal may be generated and sent to the control operator for corrective action.

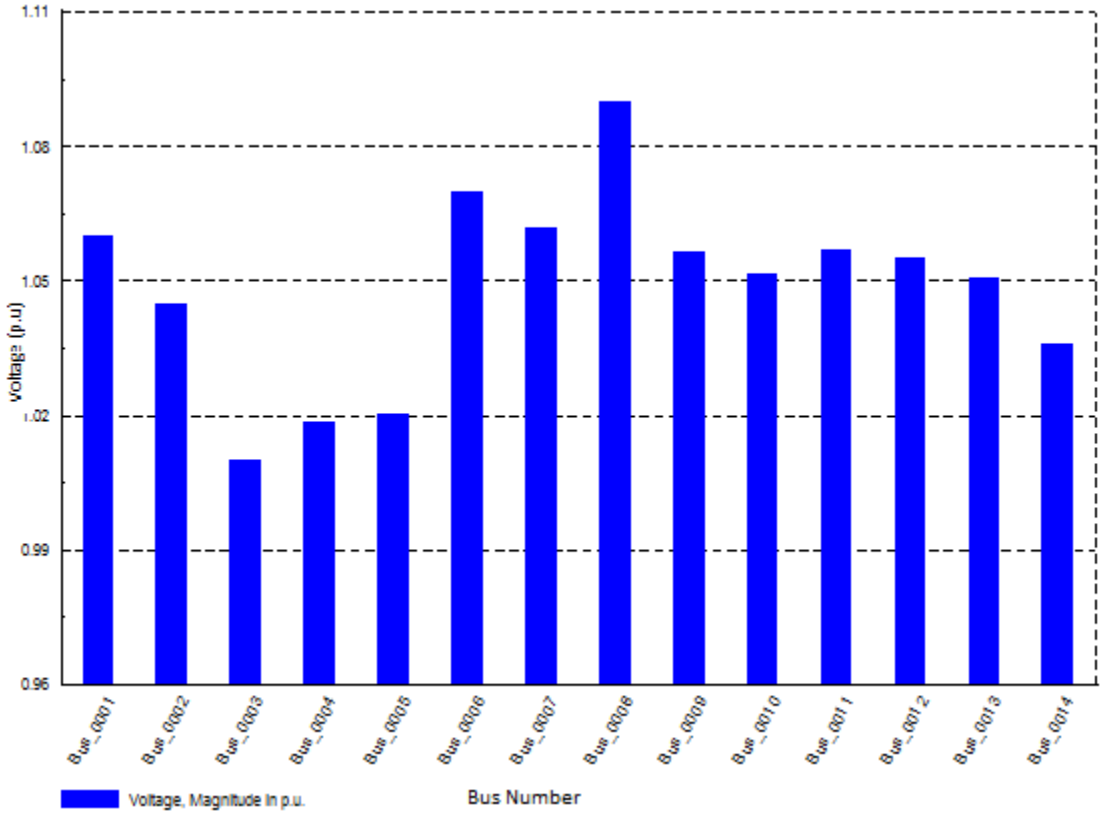


Figure 4.3: Voltage profile of the IEEE 14-Bus network

Table 4.7 shows the load flow simulation result of the IEEE 14 bus system

Table 4.7: DIgSILENT simulation results of the IEEE 14-Bus system

	Bus results						
Bus no.	**V(pu)**	**Vactual**	**δ(deg)**	**PG**	**QG**	**PL**	**QL**
1	1.06	139.9	0	232.9	-16.8	-	-
2	1.04	137.9	-5	40	43.1	21.7	12.7
3	1.01	133.3	-12.7	-	23.9	94.2	19
4	1.02	134.3	-10.4	-	-	47.8	-3.9
5	1.02	134.6	-8.8	-	-	7.6	1.6
6	1.07	35.3	-13.9	-	10.1	11.2	7.5
7	1.06	1.1	-13.6	-	-	-	-
8	1.09	12	-13.6	-	18.8	-	-
9	1.05	34.7	-15.3	-	-21.0	29.5	16.6
10	1.05	34.6	-15.3	-	-	9	5.8
11	1.05	34.8	-15.3	-	-	3.5	1.8
12	1.06	34.9	-14.6	-	-	6.1	1.6
13	1.06	34.8	-14.6	-	-	13.5	5.8
14	1.02	33.7	-17.1	-	-	14.9	5

Active, reactive and apparent power load flow results of the IEEE 14-Bus system are shown in Table 4.8 for the normal system operating conditions.

Table 4.8: Grid summary of the IEEE 14-Bus system

Grid component	Active Power (P) in MW	Reactive Power (Q) in MVar	Apparent power (S)
Generation	272.39	78.50	283.47
Load	259.00	73.50	269.23
Grid Losses	13.39	26.20	-
Line charging	-	-28.30	-
Compensation cap	-	-21.20	-
Installed Capacity	300.00	-	-

Table 4.9 provides load flow results of the generators real and reactive powers during normal system operating conditions

Table 4.9: Load flow results of generators

Name of the generator	Active power in MW	Reactive power in MVar
Gen_0001	232.39	-16.89
Gen_0002	40.00	42.40
Gen_0003	0.00	23.39
Gen_0006	0.00	12.24
Gen_0008	0.00	17.36

From gird summary, it is observed that the IEEE 14-Bus power system has a total load demand of 259MW which is supplied through generators 1 and 2 of 232.39MW and 40MW respectively as given in Table 4.9.

Table 4.10 provides the load results of the transmission lines of the IEEE 14-bus system

Table 4.10: Load flow results of the transmission lines

Name of the line	Active Power in MW (P_{losses})	Reactive Power in Mvar (Q_{losses})	Capacitive Loading in Mvar	Line Current in KA (I_l)
L1-2-01	2.1474	3.6318	2.9246	0.3263
L1-2-02	2.1474	3.6318	2.9246	0.3263
L1-5	2.7638	6.0843	5.3248	0.3121

L2-3	2.3202	5.1494	4.6256	0.3067
L2-4	1.6770	1.1062	3.9824	0.2352
L2-5	0.9023	-0.8712	3.6260	0.1738
L3-4	0.3714	-2.6120	3.5598	0.1018
L4-5	0.5165	0.2990	1.3303	0.2727
L6-11	0.0547	0.1146	0.0000	0.1328
L6-12	0.0717	0.1492	0.0000	0.1336
L6-13	0.2115	0.4166	0.0000	0.3129
L9-10	0.0131	0.0348	0.0000	0.1123
L9-14	0.1168	0.2484	0.0000	0.1677
L10-11	0.0123	0.0288	0.0000	0.0678
L12-13	0.0062	0.0057	0.0000	0.0294
L13-14	0.0536	0.1091	0.0000	0.0980

4.4 Short circuit simulation

The power system short circuit simulation is a three-phase short circuit, one-phase grounded, two-phase short circuit, two-phase grounded, one-phase break, two-phase break or complex faults. Results of short-circuit analysis may help to determine the following factors (Sushil Kumar Soonee, 1983):

1) The magnitude of the fault current
2) Circuit breaker capacity
3) Rise in voltage in a single line due to ground fault
4) Residual voltage and relay settings
5) Interference due to the power line

The power transformer short-circuit can cause outrage and time to recover the system depends on the components failure (winding or transformer auxiliary components) and the duration of the maintenance. Therefore, it is important to study and understand the short-circuit behaviour of the power transformer by analysing the main protection (differential) and backup protection (overcurrent) within the protected zone of the equipment. This thesis used DIgSILENT power factory simulation tool to analyse differential and overcurrent protection schemes.

The circuit diagram for the different types of faults and a description of the various short-circuit type is given in Figure 4.4.

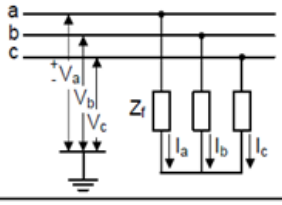
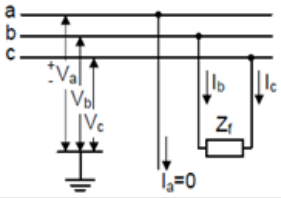
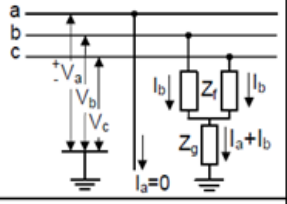
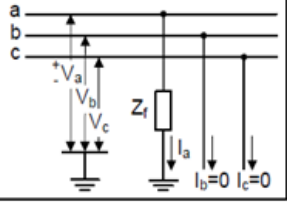
Fault	Circuit diagram of the fault point	Boundary conditions	Description
Three-phase SC		$I_a+I_b+I_c=0$ $V_a=Z_f\ I_a$ $V_b=Z_f\ I_b$ $V_c=Z_f\ I_c$	• Connection of all conductors with or without simultaneous contact to ground • Symmetrical loading of the three external conductors • Calculation on a single-phase basis
Line-to-line SC		$I_a=0$ $I_b=-I_c$ $V_b-V_c=Z_f\ I_b$	• Unsymmetrical loading • All voltage non-zero • SC current higher than in a three-phase SC near-to generator
Double line-to-ground SC		$I_a=0$ $V_b=(Z_f+Z_g)I_b+Z_g\ I_c$ $V_c=(Z_f+Z_g)I_c+Z_gI_b$	• The leakage current flowing to ground is a capacitive ground fault current
Single line-to-ground SC		$I_b=I_c=0$ $V_a=Z_f\ I_a$	• Very frequent occurrence in low voltage networks

Figure 4.4: Different types of short circuit faults in the three-phase network (IEC International Standard 60909, 2001)

The DIgSILENT simulation tool has functions such as coordination of protection equipment for system planning and protection relay settings for system operations. Once the power system is modelled and all parameters of the network are defined then, next step is to calculate the required short circuit current levels using DIgSILENT simulation tool. Different case studies are developed with the utilisation of a Single-Line-Diagram (SLD). The short circuit location and its requirements are chosen. The initial three-phase short circuit current I''_k, single phase to earth short circuit current I''_{kl}, and the peak short circuit current of the system operation are simulated and taken into consideration. The initial short circuit current I_p is considered as the sum of an AC symmetrical and DC decaying components. The maximum and minimum short circuit current values are calculated using the IEC 60909 standard. The short circuit power S''_k is calculated using Equation (4.5). The equations used to represent the short-circuit current and apparent power are given in Equations (4.2) and (4.5) respectively (IEC International Standard 60909, 2001).

$$I''_k = \frac{cV_n}{\sqrt{3}\,Z_k} \tag{4.1}$$

$$I''_{kl} = \frac{\sqrt{3}cV_n}{Z_{k(1)}+Z_{k(2)}+Z_{k(0)}} \quad 4.2)$$

$$k = 1.02 + 0.98e^{\frac{-3}{X/R}} \quad (4.3)$$

$$I_p = k \times \sqrt{2}\, I''_k \quad (4.4)$$

$$S''_k = \sqrt{3}\, I''_k\, V_n \quad (4.5)$$

Where:

I''_k is the initial symmetrical short-circuit current;

I_p is the peak short-circuit current;

k is the constant factor;

c is the voltage factor;

V_n is the nominal voltage at the short circuit location;

Z_k is the equivalent short-circuit impedance;

$Z_{k(1)}$ is the equivalent positive sequence short-circuit impedance;

$Z_{k(0)}$ is the equivalent zero sequence short-circuit impedance;

$Z_{k(2)}$ is the equivalent negative sequence short-circuit impedance;

R is the resistance of the network;

X is the reactance of the network.

Next section of the chapter presents the differential protection scheme for the power transformer. The simulation is conducted using the DIgSILENT power factory software, and the results are analysed for different system operating conditions.

4.5 Transformer differential protection scheme in DIgSILENT power factory simulation environment

The differential protection scheme is investigated in the DIgSILENT simulation environment using the SEL 487E relay model, where its applied to a 100MVA, 132kV/33kV transformer as the primary line of protection. The IEEE 14 bus system is simulated in DIgSILENT Power factory, and the network diagram is shown in Figure 4.5 below.

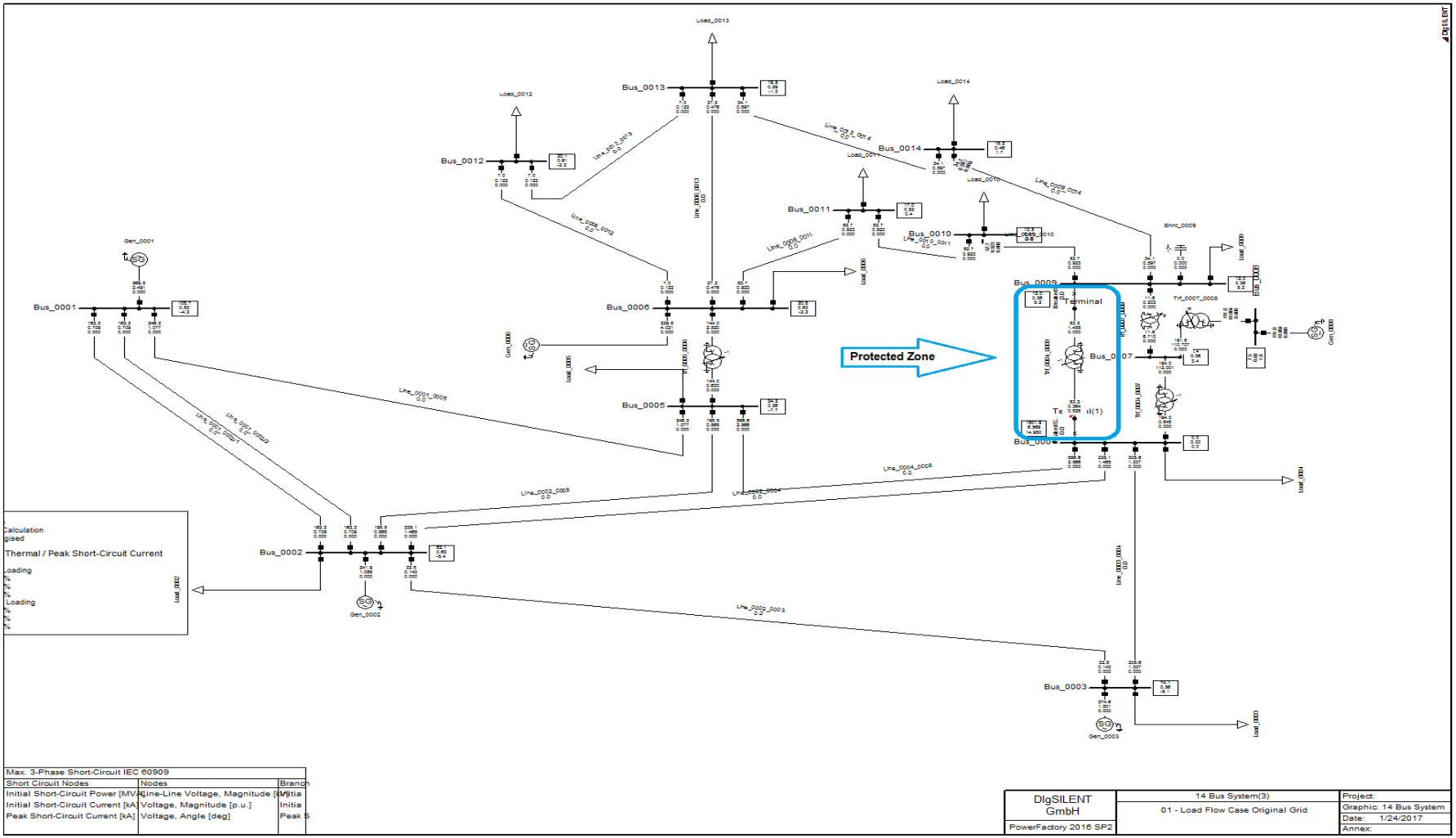


Figure 4.5: IEEE 14-Bus system in DIgSILENT simulation environment

Note that the differential protection zone encircled in blue colour on Figure 4.5 below. The SEL 487E differential relay model is connected to the primary side (Bus 4) of the transformer and has current transformer inputs of 400/1 as ratio given in Table 4.11. For this application, only T and S windings of the 487E are employed in the differential protection study. The S winding is adopted as CT input to the relay on the power transformer primary winding and the T winding as CT input to the relay on the secondary winding.

CT secondary current for any one of the five windings (S, T, U, W, X) are either 1A, or 5A (all three phases 1A or 5A) can be selected from SEL-487E. For neutral windings (the three inputs of Winding Y), the CT secondary current for each of the three inputs can be separately selected. Although each three-phase winding (S, T, U, W, and X) can be either 1A or 5A, and the Y-windings either 1A or 5A on a per-phase basis, the SEL-487E supports only the combinations.

Transformer ratio 33kV:132kV = 0.25, with $I_{HV} = 437.38A$ and $I_{LV} = 1749.55A$

Primary and secondary CTs 400/1:1600/1 = 0.25

CT ratios are not perfect match for transformer winding ratio therefore, correction factors for CTs can be chosen based on current ratings of the transformer (settings in SEL-487E differential relay).

- HV: 400/437.38 = 0.914
- LV: 1600/1749.55 = 0.914

Table 4.11: SEL-487E power transformer differential relay Settings

Description	Release Threshold	Restraint 1st Slope Threshold	Restraint 2nd Slope Threshold	Restraint 1st Slope	Restraint 2nd Slope	Unrestrained Differential Threshold
Differential Element setting	0.50 p.u	_	_	35%	75%	8.0 p.u
Transformer Tap Settings	Tap 1	Tap 2	Tap 3	Tap 4	Tap 5	Max Rated Power
	5.8 A	5.8 A	31.0 A	31.0 A	20.0 A	100.0 MVA
Description	Current Transformer Ratio	Nominal terminal line-line voltage		Current Transformer connection		Vector group
S Meas→Wd Adapter	400	132kV		Y		_
T Meas→Wd Adapter	1600	33kV		Y		_

The phase shift can be compensated in SEL-487E; therefore, CTs on both sides can be connected in star. The settings applied to the SEL487E are given in Table 4.11. It should, however, be noted that current transformers with CT ratios of 400/1 and 1600/1 have been used on the 132kV and 33kV winding of the transformer respectively as given in Table 4.12, the mismatch has been compensated for internally in the CT measuring adapter block.

A CT Adapter block is used where the ratio of a CTs supplying the SEL-487E differential relay is placed in order to be normalised because the CTs are located at different voltage levels of the transformer differential protection and where a vector rotation may be introduced due to the winding arrangement.

Table 4.12: Instrument Transformer settings on the S and T winding slots

Protection Device	Location	Branch	Manufacturer	Model	CT	Slot	Ratio [pri.A/sec.A]
Relay Model	Substation 4	From bus 4 to bus 9	Schweitzer	SEL487E-1A	132KV CT @ SS04	S Ct	400A/1A
					132KV CT @ SS04	S Ct-3I0	400A/1A
					Current Transformer	T Ct	1600A/1A
					33KV CT @ SS04	T Ct-3I0	1600A/1A

In order to understand the DIgSILENT simulation case studies and its results presented in this chapter, the single line diagram of the transformer protection is shown in Figure 4.6, which is extracted from the IEEE 14-Bus system given in Figure 4.1.

Please take note; it is necessary to connect a node between busbar and HV and LV sides of the transformer respectively as shown in Figure 4.6. The reason for that, these terminal node points help to create internal faults within the zones of protection, and without these node points, it is not feasible to create internal transformer faults in the DIgSILENT simulation environment.

Therefore, a fault at bus 4 and bus 9 on HV and LV sides of the transformer respectively is considered as an external fault whereas a fault at terminal 1 and 2 is considered as an internal fault.

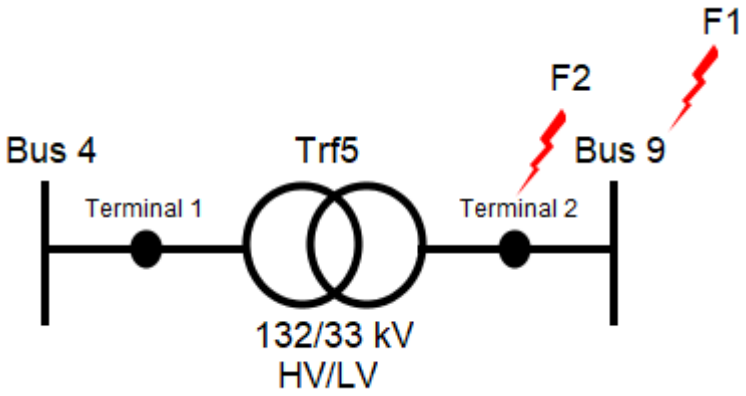


Figure 4.6: Single diagram of the transformer protection

Where:

F1: Transformer external fault

F2: Transformer internal fault

Terminal 1: Node point connected between bus 4 and HV side of the transformer

Terminal 2: Node point connected between bus 9 and LV of the transformer

4.5.1 External faults

Based on the operational philosophy of the differential protection scheme, a fault outside of the protected zone should not operate the differential relay. To validate this point, an EMT simulation involving through faults on the LV side of the transformer at bus 9 is conducted.

The performance of the differential protection scheme is investigated for three type of external fault case studies. These are (i) three-phase, (ii) two-phase and (iii) single-phase to ground external faults all at bus 9.

Table 4.13: DIgSILENT simulation case studies for external transformer faults

Type of fault	Fault location	Measured voltage and current at fault location
Three-phase (LLL)	External fault (F1) at bus 9	i) V and I signals measured at bus 9 ii) V and I signals measured at LV side of the transformer
Two-phase (LL)	External fault (F1) at	i) V and I signals measured at bus 9

	bus 9	ii) V and I signals measured at LV side of the transformer
Single-phase to ground (LG)	External fault (F1) at bus 9	i) V and I signals measured at bus 9 ii) V and I signals measured at LV side of the transformer

I. External three-phase fault at bus 9

The total simulation time is set 0.2 seconds, the three-phase fault being introduced into the network at 0.1 seconds and cleared at 0.15 seconds which are shown in x-axis in Figure 4.7. The external three-phase to ground fault at bus 9 is introduced, and the fault current and voltage on the power transformer is studied through the EMT simulation, and the results are shown in Figure 4.7 below.

The three-phase external fault at bus 9 produced a current magnitude of 23.412kA as shown in Figure 4.7. It is discernible from the results provided in Table 4.14 that the fault current does not trip the differential relay during through fault.

For a three-phase external fault at LV side of the transformer connected at bus 9 has the peak fault current magnitude of 6.009kA as shown in Figure 4.8 below. It is also interesting to note the distorted voltage waveform resulting from transformer inrush current as the system recovers to fault clearing as shown in Figure 4.8.

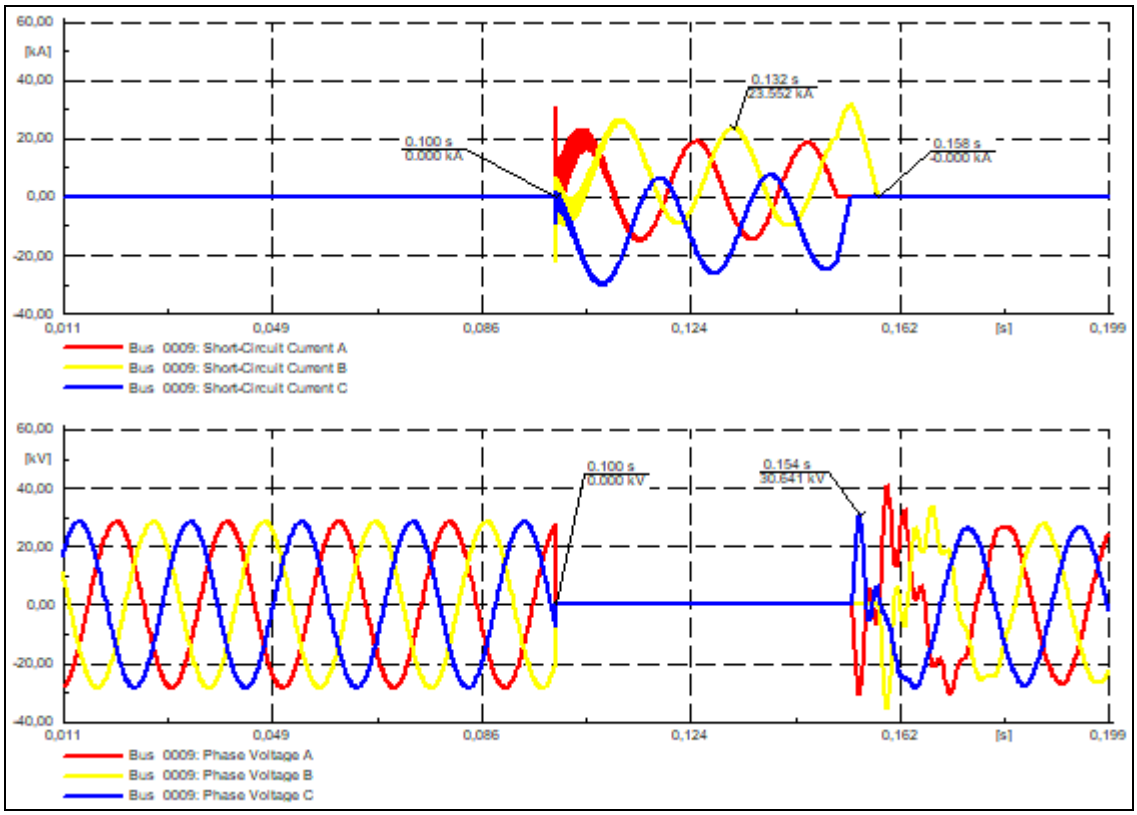


Figure 4.7: Voltage and current signals measured at bus 9 for a 3ph external fault

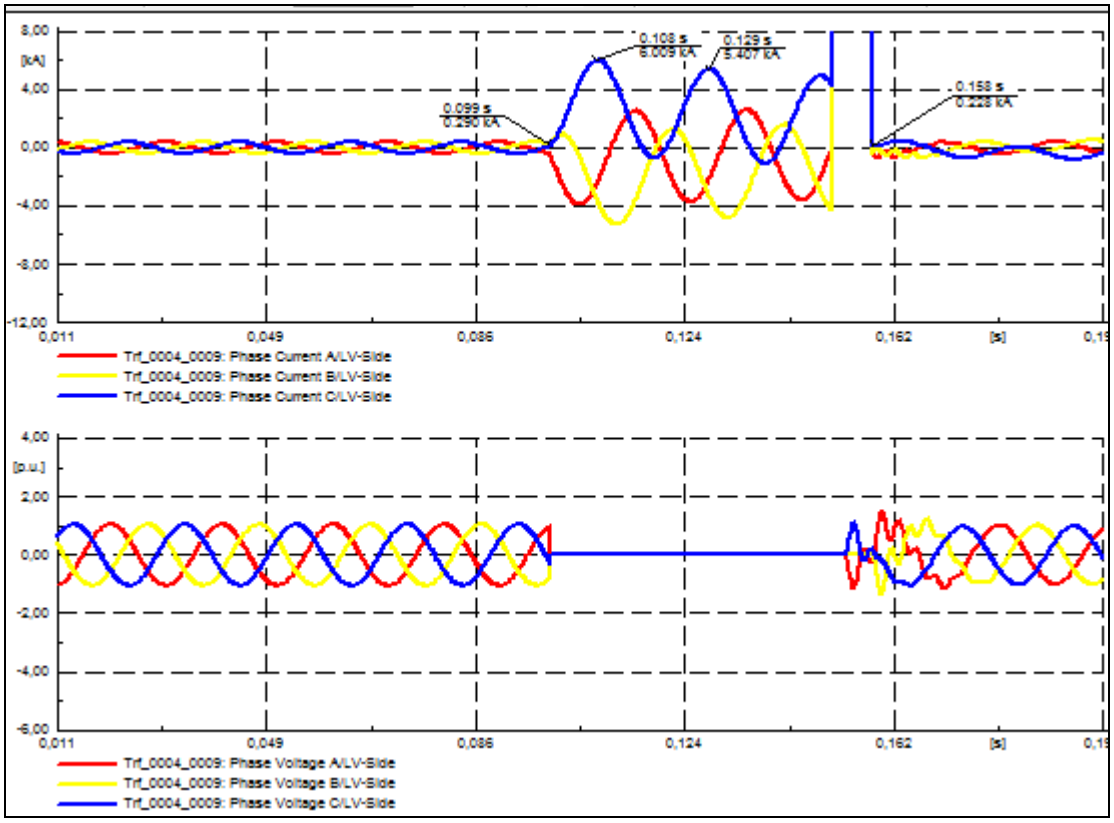


Figure 4.8: Voltage and current signals for a 3ph external fault on LV side of the transformer

Table 4.14 below provides SEL-487E trip and clearing times for an external three-phase fault. It is noted that 9999.99s means that the relay did not trip for the external fault condition on the LV side of the transformer.

Table 4.14: SEL-487E differential relay response to an external three-phase fault

SEL 487E	Relay Type : SEL 487E-1A				
S Ct : 132KV CT @ bus4	Location : Busbar	: Bus_0004	/	Ratio	: 400A/1A
	Branch	: Breaker/Switch(1)		Connection	: Y
	Cubicle	: Cub_1(2)			
S Ct-3I033KV CT @ bus9	Location : Busbar	: Bus_0009	/	Ratio	: 1600A/1A
	Branch	: Breaker/Switch		Connection	: Y
	Cubicle	: Cub_1(2)			
T Ct : 33KV CT @ bus9	Location : Busbar	: Bus_0009	/	Ratio	: 1600A/1A
	Branch	: Breaker/Switch		Connection	: Y
	Cubicle	: Cub_1(2)			
T Ct-3I033KV CT @ bus9	Location : Busbar	: Bus_0009	/	Ratio	: 1600A/1A
	Branch	: Breaker/Switch		Connection	: Y
	Cubicle	: Cub_1(2)			
U Ct : 33KV CT @ bus9	Location : Busbar	: Bus_0009	/	Ratio	: 1600A/1A
	Branch	: Breaker/Switch		Connection	: Y
	Cubicle	: Cub_1(2)			
U Ct-3I033KV CT @ bus9	Location : Busbar	: Bus_0009	/	Ratio	: 1600A/1A
	Branch	: Breaker/Switch		Connection	: Y
	Cubicle	: Cub_1(2)			
W Ct : 33KV CT @ bus9	Location : Busbar	: Bus_0009	/	Ratio	: 1600A/1A
	Branch	: Breaker/Switch		Connection	: Y
	Cubicle	: Cub_1(2)			
X Ct : 33KV CT @ bus9	Location : Busbar	: Bus_0009	/	Ratio	: 1600A/1A
	Branch	: Breaker/Switch		Connection	: Y
	Cubicle	: Cub_1(2)			
Logic : Logic			yout	: 9999,999 s	
Breaker	Cubicle	Branch	Busbar	/ Substation	Fault Clearing Time
Breaker/Switch(1)	Cub_2	Breaker/Switch(1)	Terminal_1	/	9999,999 s
				/	

Figure 4.9 below shows the operating characteristic of the differential relay. It is clear from the current differential plot that the relay did not experience any differential

currents. The stabilising current, in this case, was 729.94A and the trip time is 9999.999s which means the relay did not trip.

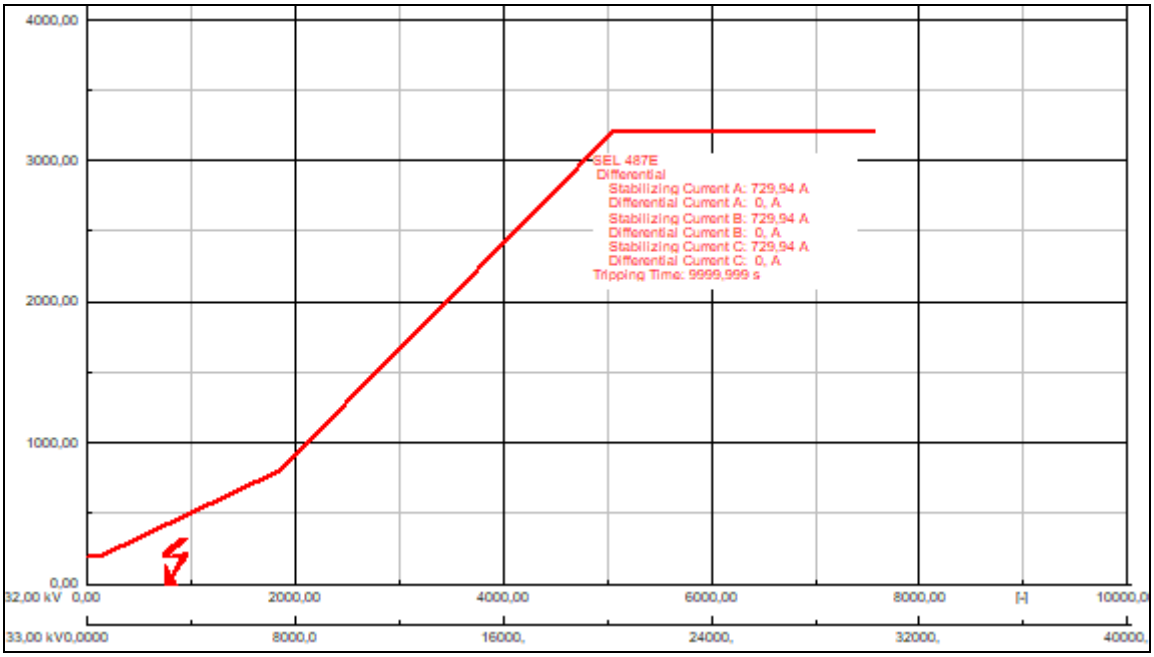


Figure 4.9: SEL-487E transformer differential plot for a 3ph external fault at bus 9

II. External two-phase fault

The two-phase external fault is conducted at bus 9 on the LV side of the power transformer. The current and voltage signals measured at bus 9 is obtained from the EMT simulation, and the results are shown in Figure 4.10 below.

The two-phase-to-ground external fault on the bus 9 produced a current magnitude of 25.285kA, and the voltage was reduced to 14.104kV as shown in the Figure 4.10. It is also discernible from the results provided in Table 4.15 that the fault current does not trip the differential relay.

From Figure 4.11 below, the peak fault current magnitude of 5.025kA on LV side of the transformer at bus 9 for two-phase external fault.

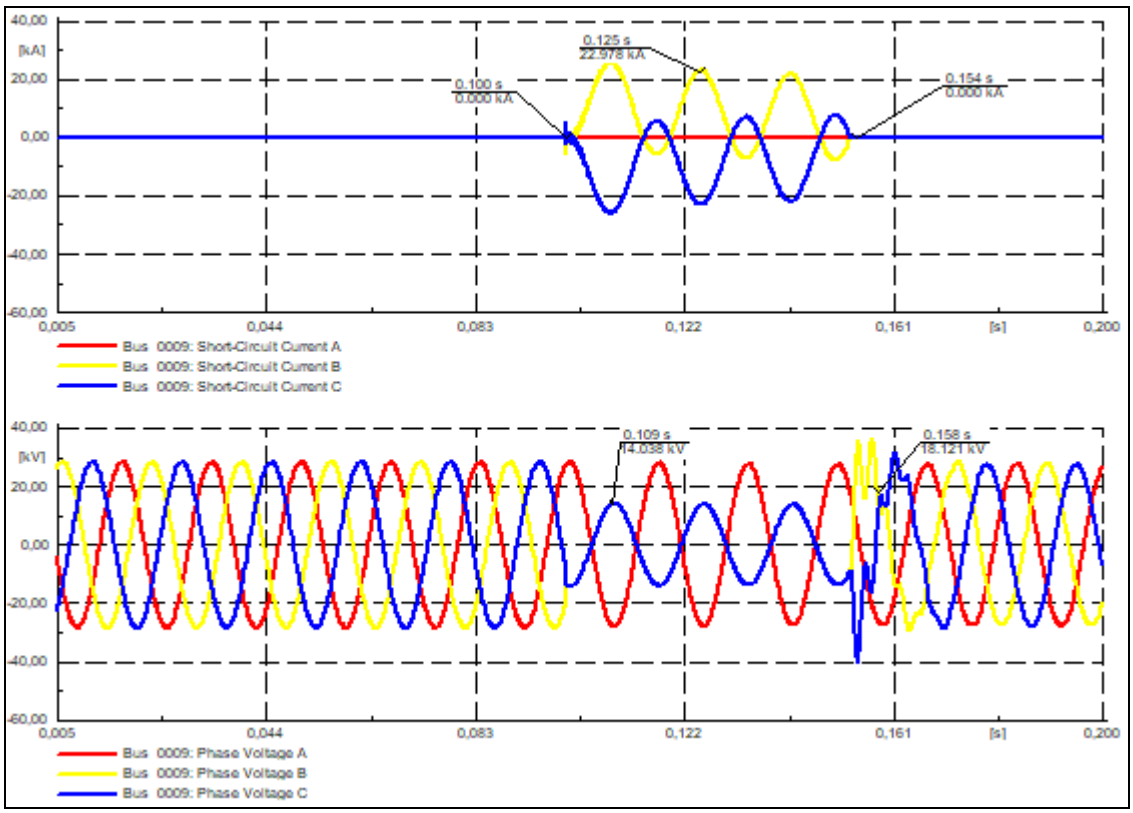


Figure 4.10: Voltage and current signals measured at bus 9 for a two-phase external fault

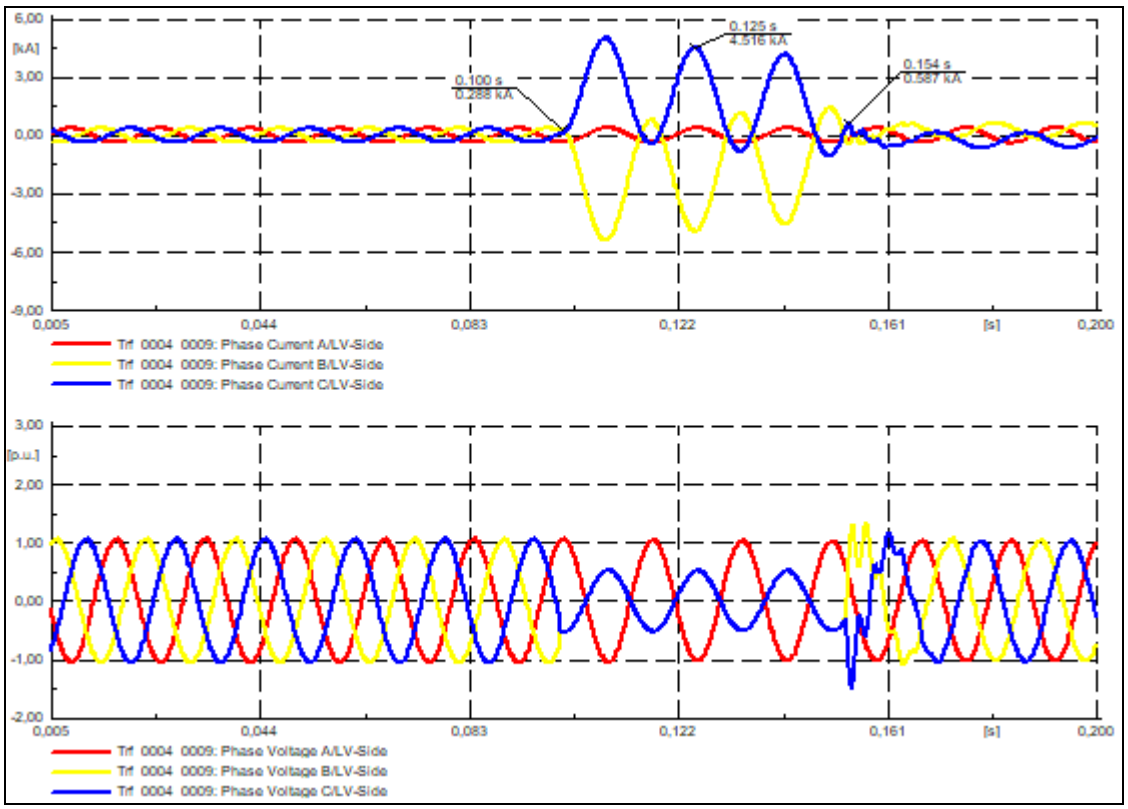


Figure 4.11: Voltage and current signals on the LV side of the transformer for a two-phase external fault

Table 4.15 below provides SEL-487E differential relay trip and clearing times for an external two-phase fault. The relay did not trip for an external two-phase fault.

Table 4.15: SEL-487E differential relay response to an external two-phase fault

SEL 487E	Relay Type	: SEL 487E-1A				
S Ct : 132KV CT @ bus4	Location	: Busbar	: Bus_0004	/	Ratio	: 400A/1A
		Branch	: Breaker/Switch(1)		Connection	: Y
		Cubicle	: Cub_1(2)			
S Ct-3I033KV CT @ bus9	Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
		Branch	: Breaker/Switch		Connection	: Y
		Cubicle	: Cub_1(2)			
T Ct : 33KV CT @ bus9	Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
		Branch	: Breaker/Switch		Connection	: Y
		Cubicle	: Cub_1(2)			
T Ct-3I033KV CT @ bus9	Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
		Branch	: Breaker/Switch		Connection	: Y
		Cubicle	: Cub_1(2)			
U Ct : 33KV CT @ bus9	Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
		Branch	: Breaker/Switch		Connection	: Y
		Cubicle	: Cub_1(2)			
U Ct-3I033KV CT @ bus9	Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
		Branch	: Breaker/Switch		Connection	: Y
		Cubicle	: Cub_1(2)			
W Ct : 33KV CT @ bus9	Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
		Branch	: Breaker/Switch		Connection	: Y
		Cubicle	: Cub_1(2)			
X Ct : 33KV CT @ bus9	Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
		Branch	: Breaker/Switch		Connection	: Y
		Cubicle	: Cub_1(2)			
Logic : Logic				yout	: 9999,999 s	
Breaker	Cubicle	Branch	Busbar	/ Substation	Fault Clearing Time	
Breaker/Switch(1)	Cub_2	Breaker/Switch(1)	Terminal_1	/	9999,999 s	
				/		

Figure 4.12 below shows the operating characteristic of the differential relay for two-phase external fault. It can be observed from the current differential plot that the relay did not experience any differential currents. The stabilising current, in this case, was 1.4A, 631.64A and 633.02A on phases A, B and C respectively. The trip time is 9999.999s, which means the relay did not trip.

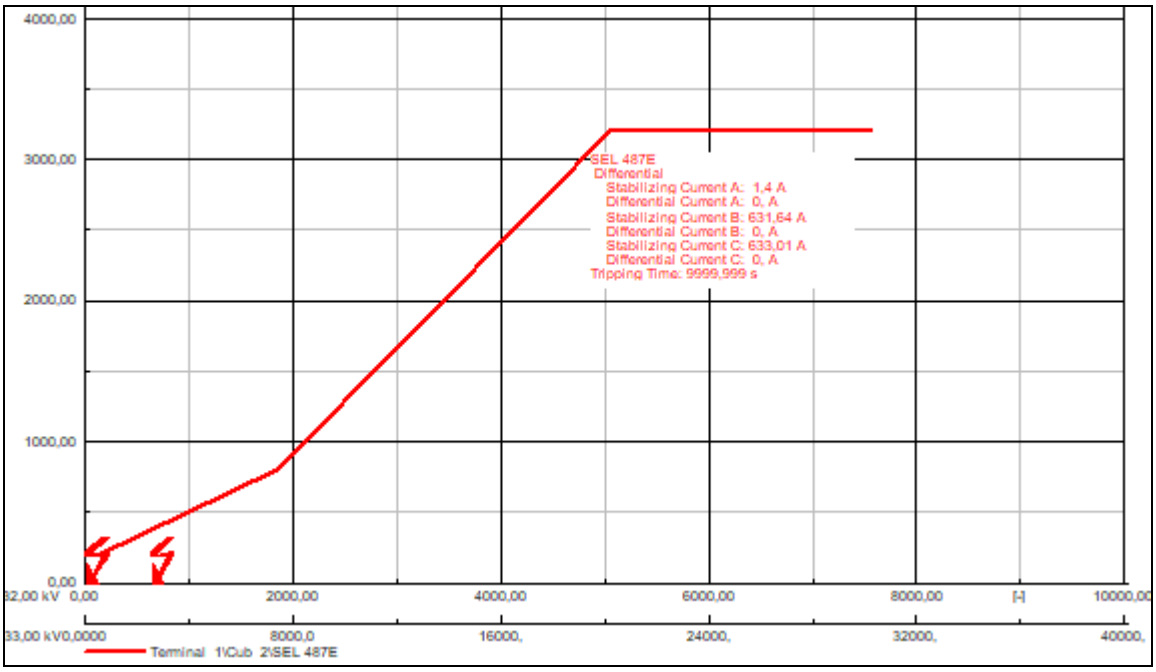


Figure 4.12: SEL-487E transformer differential plot for a two-phase external fault

III. External single phase to ground fault

The external single-phase-to-ground fault is conducted at bus 9 on LV side of the power transformer at bus 9 from and the EMT simulation results obtained is shown in Figure 4.13 below.

The single-phase-to-ground external fault at bus 9 produced a current magnitude of 31.315 kA, and the voltage was reduced to 0kV as shown in Figure 4.13. It is also discernible from the results provided in Table 4.16 that the fault current does not trip the differential relay during single phase to ground fault on external zone of transformer protection.

From Figure 4.14 below, the peak fault current magnitude of 1263.294kA is obtained for an external single-phase to ground fault at bus 9 on LV side of the transformer.

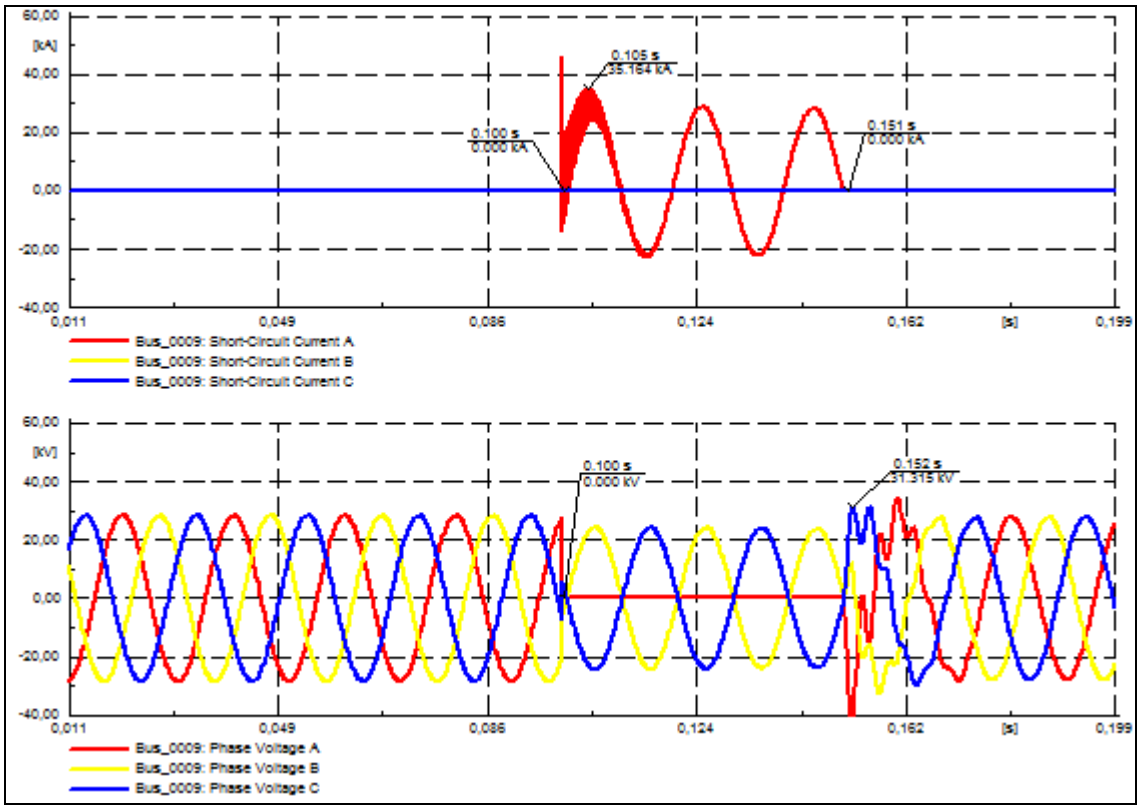


Figure 4.13: Voltage and current signals measured at bus 9 for a single phase external fault

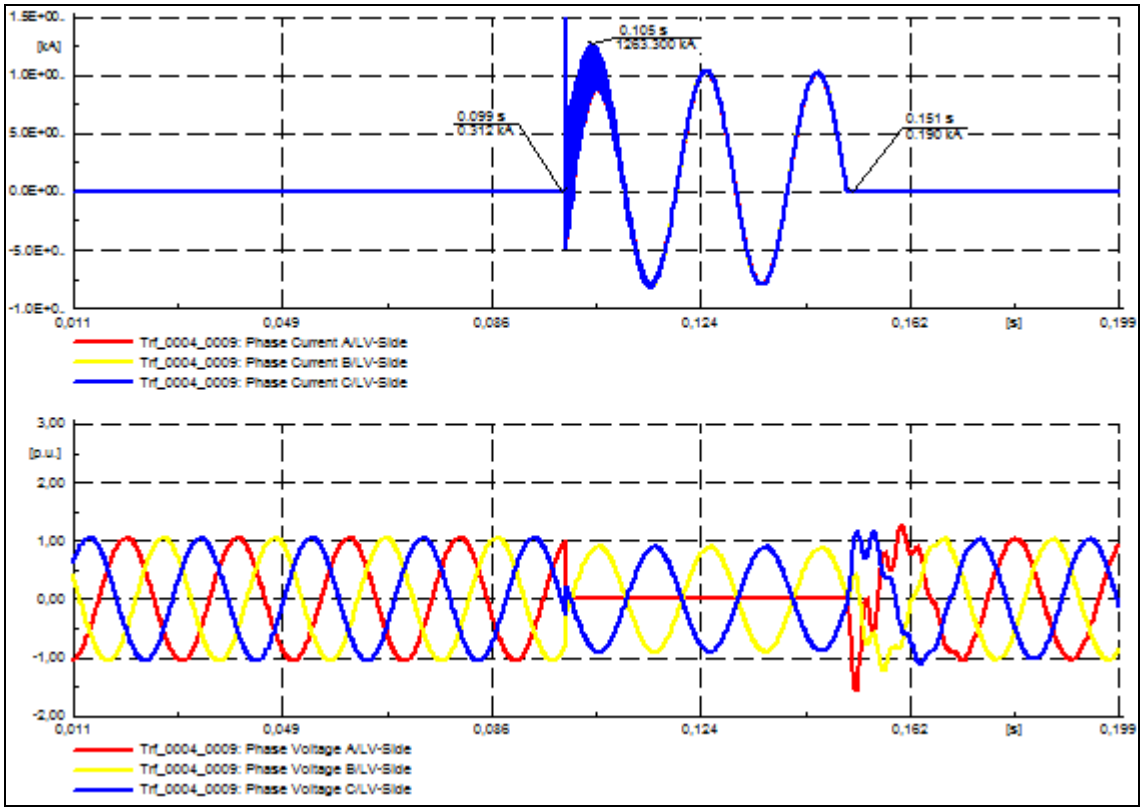


Figure 4.14: Voltage and current signals on the LV side of the transformer for an external single-phase-to-ground fault

Table 4.16 below provides SEL-487E differential relay trip and clearing times for an external single-phase to ground fault. The relay did not trip for an external single-phase to ground fault.

Table 4.16: SEL-487E differential relay response to an external single-phase fault

SEL 487E		Relay Type	: SEL 487E-1A				
S Ct : 132KV CT @ bus4	Location	: Busbar	: Bus_0004	/		Ratio	: 400A/1A
		Branch	: Breaker/Switch(1)			Connection	: Y
		Cubicle	: Cub_1(2)				
S Ct-3I033KV CT @ bus9	Location	: Busbar	: Bus_0009	/		Ratio	: 1600A/1A
		Branch	: Breaker/Switch			Connection	: Y
		Cubicle	: Cub_1(2)				
T Ct : 33KV CT @ bus9	Location	: Busbar	: Bus_0009	/		Ratio	: 1600A/1A
		Branch	: Breaker/Switch			Connection	: Y
		Cubicle	: Cub_1(2)				
T Ct-3I033KV CT @ bus9	Location	: Busbar	: Bus_0009	/		Ratio	: 1600A/1A
		Branch	: Breaker/Switch			Connection	: Y
		Cubicle	: Cub_1(2)				
U Ct : 33KV CT @ bus9	Location	: Busbar	: Bus_0009	/		Ratio	: 1600A/1A
		Branch	: Breaker/Switch			Connection	: Y
		Cubicle	: Cub_1(2)				
U Ct-3I033KV CT @ bus9	Location	: Busbar	: Bus_0009	/		Ratio	: 1600A/1A
		Branch	: Breaker/Switch			Connection	: Y
		Cubicle	: Cub_1(2)				
W Ct : 33KV CT @ bus9	Location	: Busbar	: Bus_0009	/		Ratio	: 1600A/1A
		Branch	: Breaker/Switch			Connection	: Y
		Cubicle	: Cub_1(2)				
X Ct : 33KV CT @ bus9	Location	: Busbar	: Bus_0009	/		Ratio	: 1600A/1A
		Branch	: Breaker/Switch			Connection	: Y
		Cubicle	: Cub_1(2)				
Logic : Logic					yout		: 9999,999 s
Breaker	Cubicle	Branch	Busbar	/	Substation		Fault Clearing Time
Breaker/Switch(1)	Cub_2	Breaker/Switch(1)	Terminal_1	/			9999,999 s
				/			

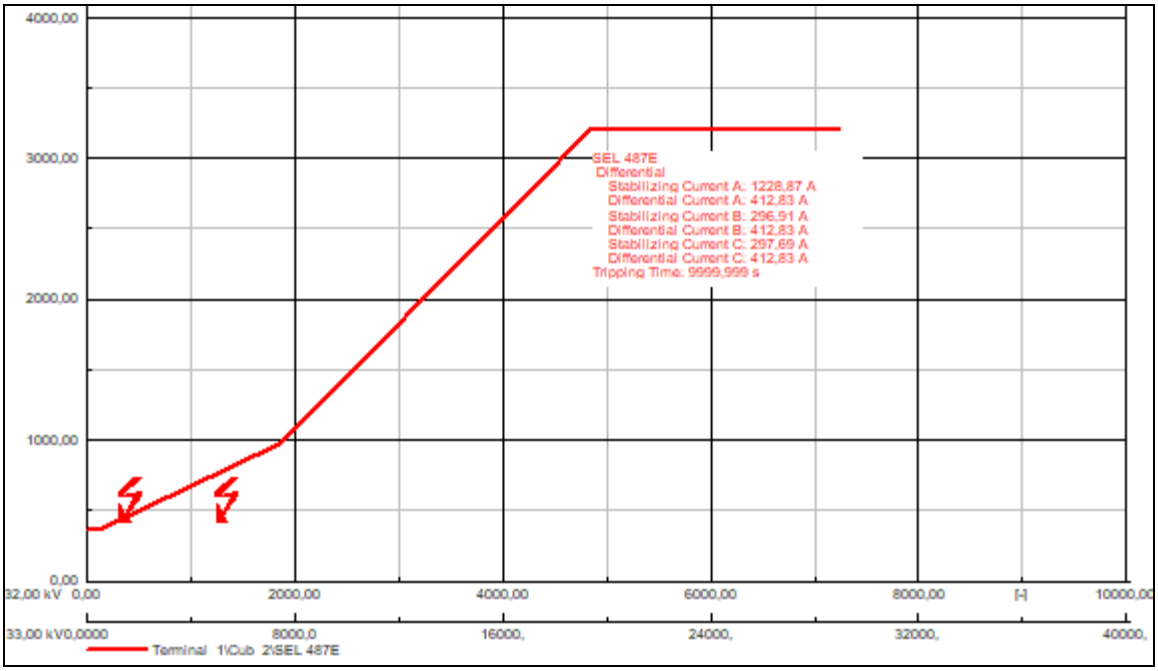


Figure 4.15: SEL-487E differential plot for an external single-phase-to-ground fault

Figure 4.15 above shows the operating characteristic of the differential relay for a single-phase-to-ground fault at bus 9 on LV side of the transformer. It is observed from the current differential plot that the relay experienced differential currents because of a large fault current is drawn by the transformer for a single-phase to ground fault of 412.83A. The stabilising current, in this case, was 1228.87A, 296.91A and 297.69A on phases A, B and C respectively. The trip time is 9999.999s which means the relay did not trip for an external single-phase to ground fault.

4.5.2 Internal faults

In this case study, an internal fault is applied within the zone of protection, and the simulation results are analysed. In order to analyse the internal fault scenarios, an EMT simulation is conducted on LV side of the transformer at terminal 2 which is a node connected between the busbar and the transformer to make the electrical connection between the breaker and transformer.

The performance of the differential protection scheme is investigated for four types of internal faults. They are (i) three-phase internal fault at terminal 2 of the power transformer at bus 9, (ii) Line-to-line internal fault, (iii) Double-line-to-ground internal fault, (iv) Single-line to ground internal fault. This section discusses the transformer internal fault case studies results.

Table 4.17: DIgSILENT simulation case studies for internal transformer fault

Type of fault	Fault location	Measured voltage and current at fault location
Three-phase (LLL)	Internal fault (F2) at terminal 2	i) V and I signals measured at terminal 2 ii) V and I signals measured at LV side of the transformer
Two-phase (LL)	Internal fault (F2) at terminal 2	i) V and I signals measured at terminal 2 ii) V and I signals measured at LV side of the transformer
Double-phase to ground (LLG)	Internal fault (F2) at terminal 2	i) V and I signals measured at terminal 2 ii) V and I signals measured at LV side of the transformer
Single-phase to ground (LG)	Internal fault (F2) at terminal 2	i) V and I signals measured at terminal 2 ii) V and I signals measured at LV side of the transformer

I. Three-phase fault at terminal 2 on the LV the power transformer

This case study aims to investigate the differential relay performance for a three-phase fault on the power transformer. The total EMT simulation time is set to 0.2 seconds, and the three-phase transformer fault is introduced at 0.1 seconds and cleared at 0.15 seconds. The results obtained from the Electro-Magnetic Transient (EMT) study for the 3ph internal fault are shown in the Figures 4.16, 4.17 and 4.18 respectively.

The internal three-phase fault at terminal 2 produced a current magnitude of 26.954kA as shown in the Figure 4.16 below which causes the differential relay to trip at 0.015 seconds as shown in Table 4.18.

Figure 4.17 below shows the peak fault magnitude of 6.009kA current for internal three-phase to ground fault LV side of the transformer connected at bus 9. It is observed that differential the relay trips approximately 0.015s for the internal fault on LV side of the transformer at bus 9.

Table 4.18 below provides SEL-487E differential relay trip and clearing times for an internal three-phase fault on LV side of the transformer connected at bus 9.

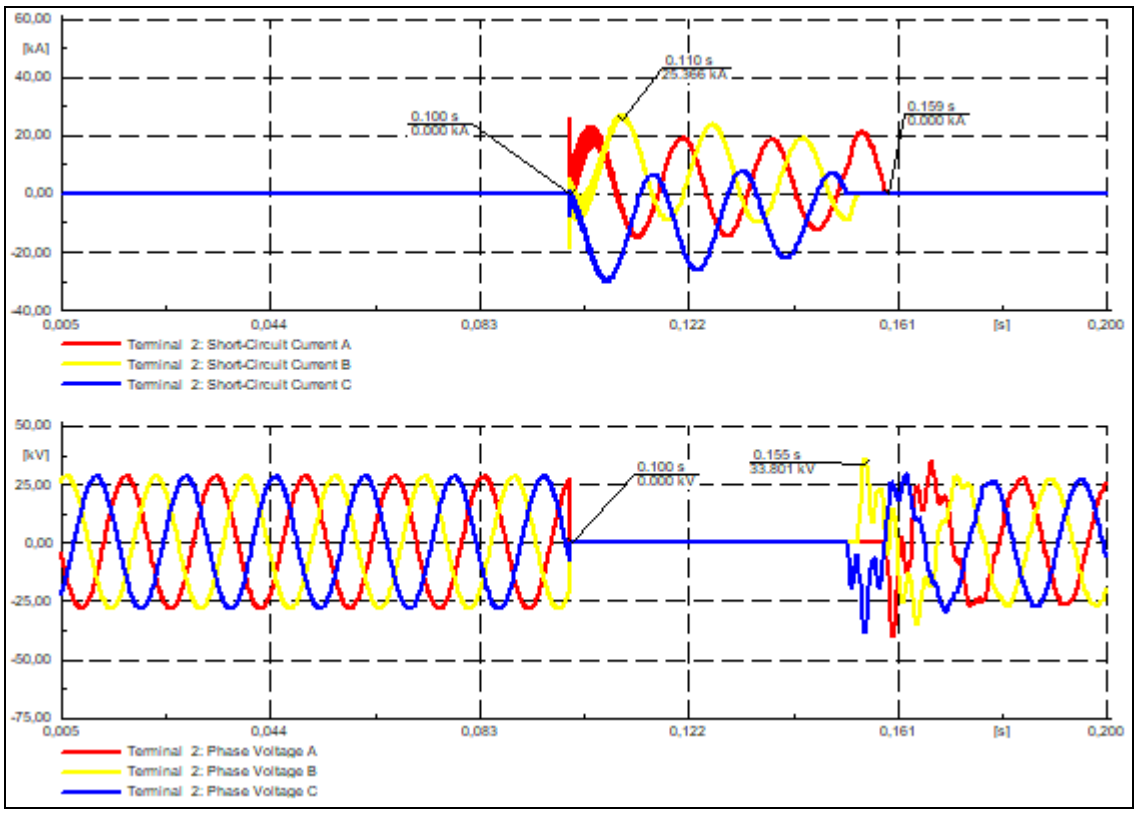


Figure 4.16: Voltage and current signals measured at terminal_2 for a 3ph internal fault

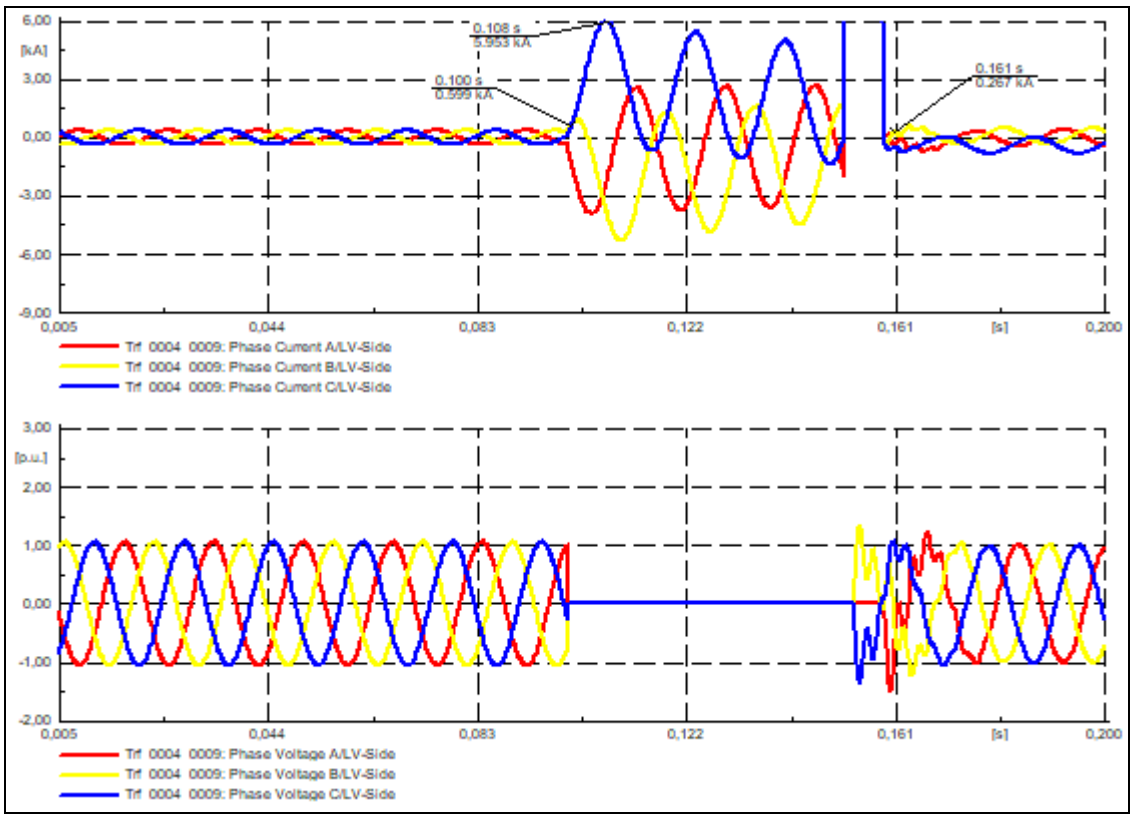


Figure 4.17: Voltage and current signals transformer for an internal three-phase fault

Table 4.18: SEL-487E differential relay response to an internal three-phase fault

SEL 487E		Relay Type	: SEL 487E-1A				
S Ct : 132KV CT @ bus4		Location	: Busbar	: Bus_0004	/	Ratio	: 400A/1A
			Branch	: Breaker/Switch(1)		Connection	: Y
			Cubicle	: Cub_1(2)			
S Ct-3I033KV CT @ bus9		Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
			Branch	: Breaker/Switch		Connection	: Y
			Cubicle	: Cub_1(2)			
T Ct : 33KV CT @ bus9		Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
			Branch	: Breaker/Switch		Connection	: Y
			Cubicle	: Cub_1(2)			
T Ct-3I033KV CT @ bus9		Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
			Branch	: Breaker/Switch		Connection	: Y
			Cubicle	: Cub_1(2)			
U Ct : 33KV CT @ bus9		Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
			Branch	: Breaker/Switch		Connection	: Y
			Cubicle	: Cub_1(2)			
U Ct-3I033KV CT @ bus9		Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
			Branch	: Breaker/Switch		Connection	: Y
			Cubicle	: Cub_1(2)			
W Ct : 33KV CT @ bus9		Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
			Branch	: Breaker/Switch		Connection	: Y
			Cubicle	: Cub_1(2)			
X Ct : 33KV CT @ bus9		Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
			Branch	: Breaker/Switch		Connection	: Y
			Cubicle	: Cub_1(2)			
Logic : Logic					yout	:	0,015 s
Breaker	Cubicle	Branch		Busbar	/ Substation	Fault Clearing Time	
Breaker/Switch(1)	Cub_2	Breaker/Switch(1)		Terminal_1	/		0,015 s
					/		

The current differential plot for the three-phase internal fault is shown in Figure 4.18. It is observed that the differential currents are 3301.04A and the stabilising current is 1651.85A, and the differential relay tripped at 0.015s.

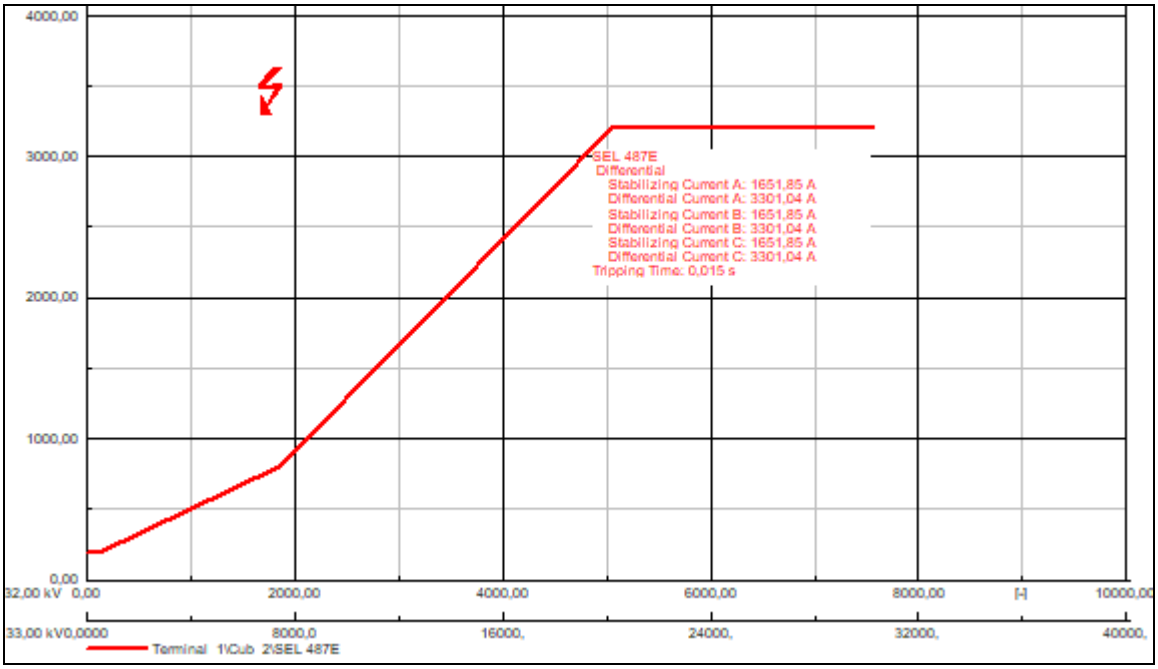


Figure 4.18: SEL-487E transformer differential plot for an internal three-phase fault

II. Internal phase-to-phase fault

The aim of this case study is to investigate the differential relay operational characteristic for an internal double phase short-circuit. The results obtained from the EMT simulation for the L-L fault is shown in Figures 4.19, 4.20 and 4.21 respectively.

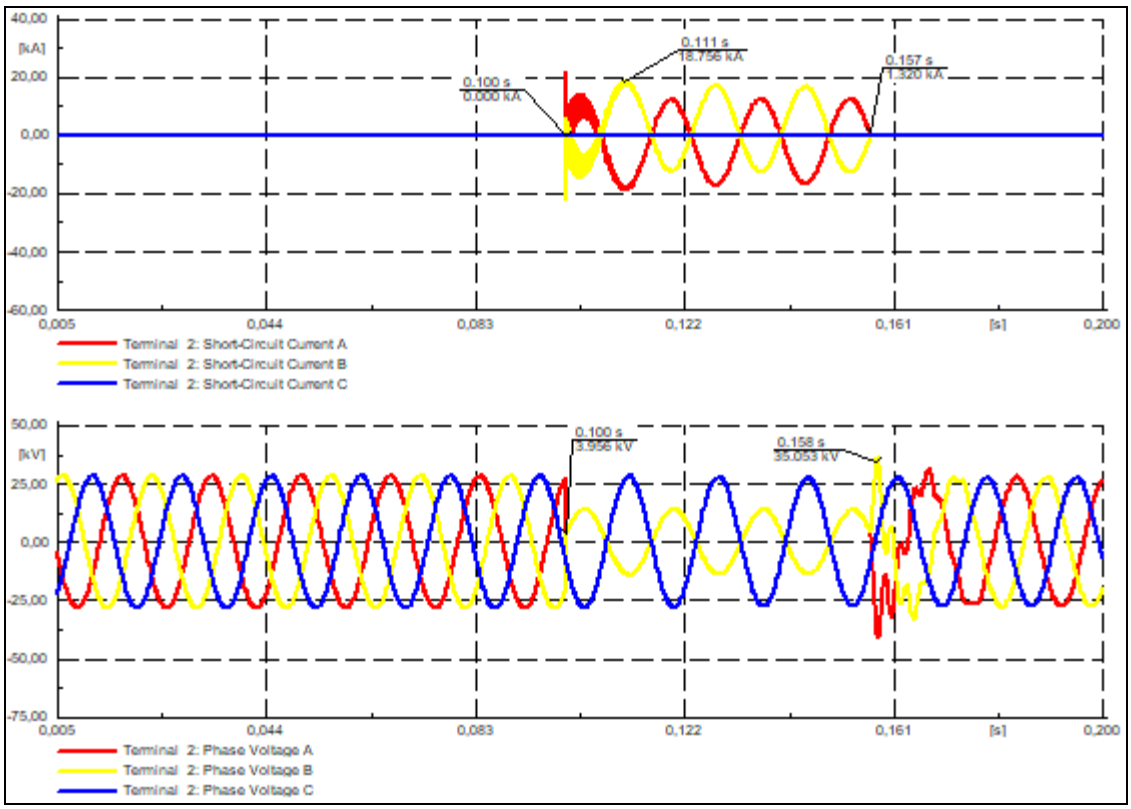


Figure 4.19: Voltage and current signals measured at terminal_2 for an internal phase-to-phase fault

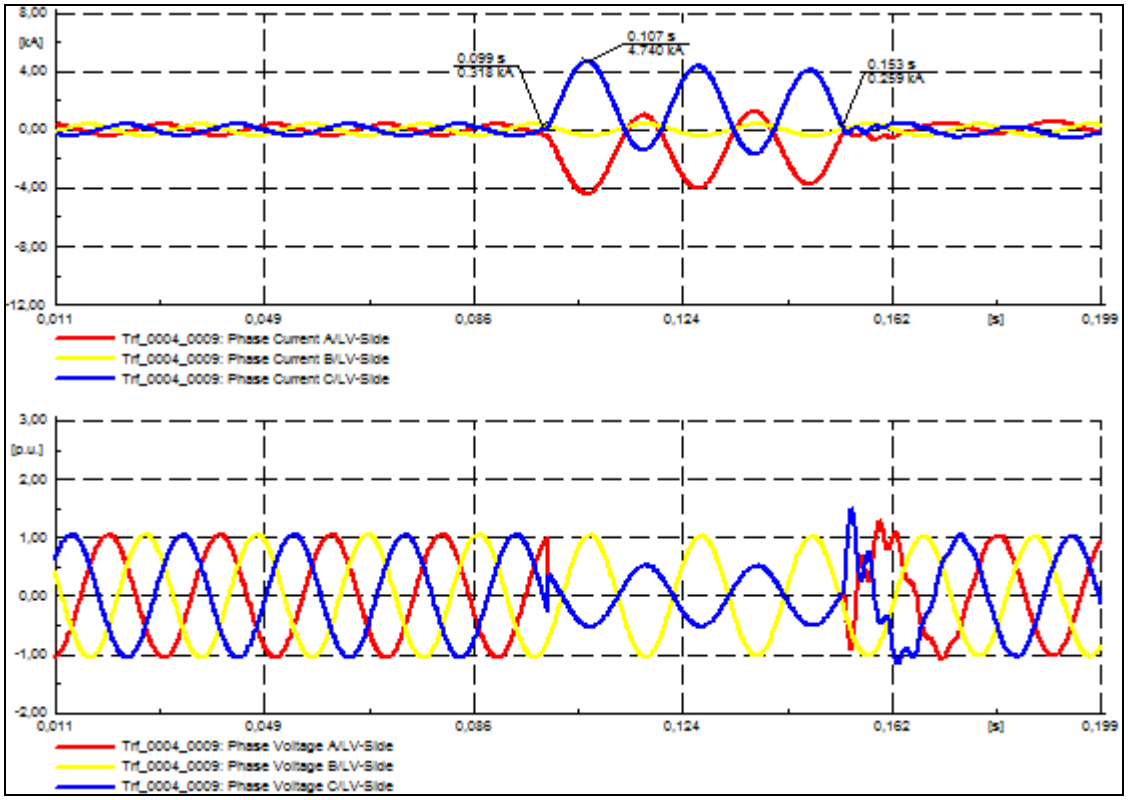


Figure 4.20: Voltage and current measured signals from the transformer for an internal phase-to-phase fault

The EMT simulation is set to 0.2 seconds. The L-L fault is introduced at terminal 2 on the low voltage side of the transformer at bus 9 between the blue and red phase at 0.1 seconds and cleared at 0.15 seconds. The internal L-L event created a fault current magnitude of 18.286kA as shown in Figure 4.19. From Figure 4.20 above, the peak fault current magnitude of 4.740kA for internal two-phase at terminal 2 on the LV side of the transformer at bus 9 and the differential relay trips at 0.015s.

The differential relay clears the internal event at 0.015s as shown in Table 4.19.

Table 4.19: SEL-487E differential relay response for an internal two-phase fault

SEL 487E	Relay Type	: SEL 487E-1A				
S Ct : 132KV CT @ bus4	Location	: Busbar	: Bus_0004	/	Ratio	: 400A/1A
		Branch	: Breaker/Switch(1)		Connection	: Y
		Cubicle	: Cub_1(2)			
S Ct-3I033KV CT @ bus9	Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
		Branch	: Breaker/Switch		Connection	: Y
		Cubicle	: Cub_1(2)			
T Ct : 33KV CT @ bus9	Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
		Branch	: Breaker/Switch		Connection	: Y
		Cubicle	: Cub_1(2)			
T Ct-3I033KV CT @ bus9	Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
		Branch	: Breaker/Switch		Connection	: Y
		Cubicle	: Cub_1(2)			
U Ct : 33KV CT @ bus9	Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
		Branch	: Breaker/Switch		Connection	: Y
		Cubicle	: Cub_1(2)			
U Ct-3I033KV CT @ bus9	Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
		Branch	: Breaker/Switch		Connection	: Y
		Cubicle	: Cub_1(2)			
W Ct : 33KV CT @ bus9	Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
		Branch	: Breaker/Switch		Connection	: Y
		Cubicle	: Cub_1(2)			
X Ct : 33KV CT @ bus9	Location	: Busbar	: Bus_0009	/	Ratio	: 1600A/1A
		Branch	: Breaker/Switch		Connection	: Y
		Cubicle	: Cub_1(2)			
Logic : Logic				yout	: 0,015 s	
Breaker Cubicle	Branch		Busbar	/ Substation	Fault Clearing Time	
Breaker/Switch(1) Cub_2	Breaker/Switch(1)		Terminal_1	/	0,015 s	
				/		

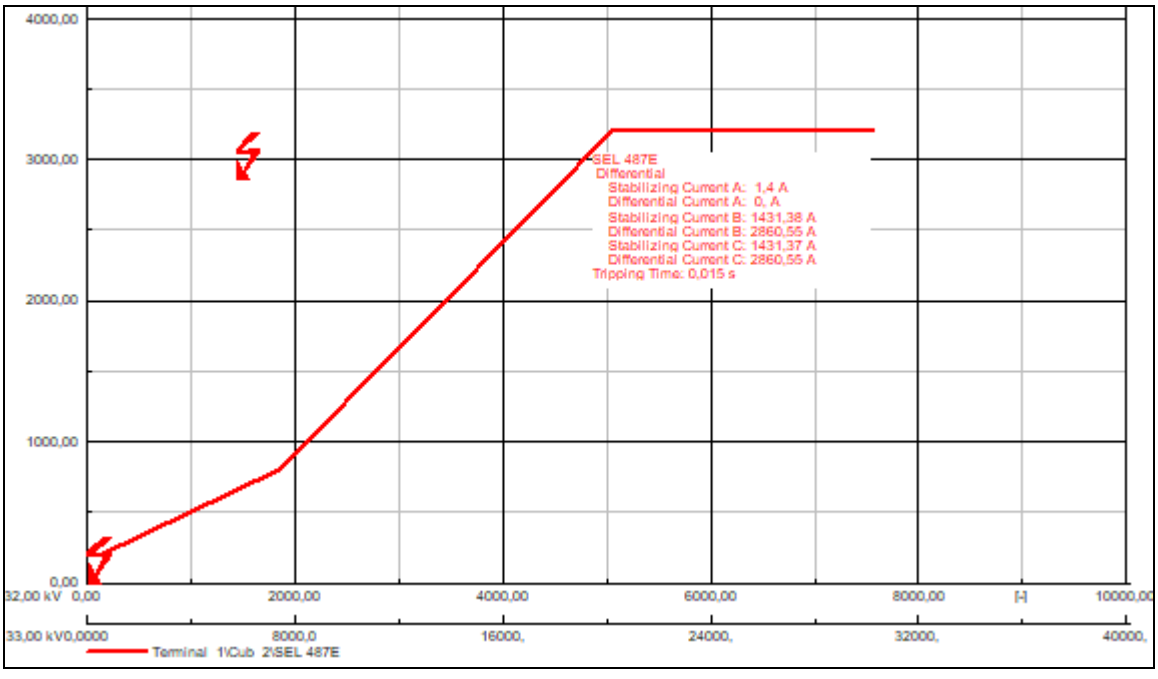


Figure 4.21: SEL-487E transformer differential plot for an internal phase-to-phase fault

The current differential plot is shown in Figure 4.21. It is observed that the differential currents on phases B and C of 2880.55A. The stabilising current is 1.4A, 1431.38A and 1431.37A on phases A, B and C respectively and the differential relay tripped at 0.015s.

III. Internal double phase to ground (LLG) event

This case study aims to investigate the operational characteristic of the transformer differential relay for an internal double phase to ground fault. Since the transformer is considered to be balanced, it is acceptable to study only two of the three phases. After computing the initial conditions, the LLG fault is introduced onto the T windings at 0.1 seconds and cleared at 0.15 seconds. The total duration of the EMT simulation is 0.2 seconds and the results obtained are depicted in Figures 4.22, 4.23 and 4.24 respectively.

As depicted in the Figure 4.22 below, the LLG fault produced a high current magnitude of 50.266kA. It is also evident from Figure 4.22 that a significant amount of transformer magnetizing inrush current (TMIC) is present in the network immediately after fault clearance.

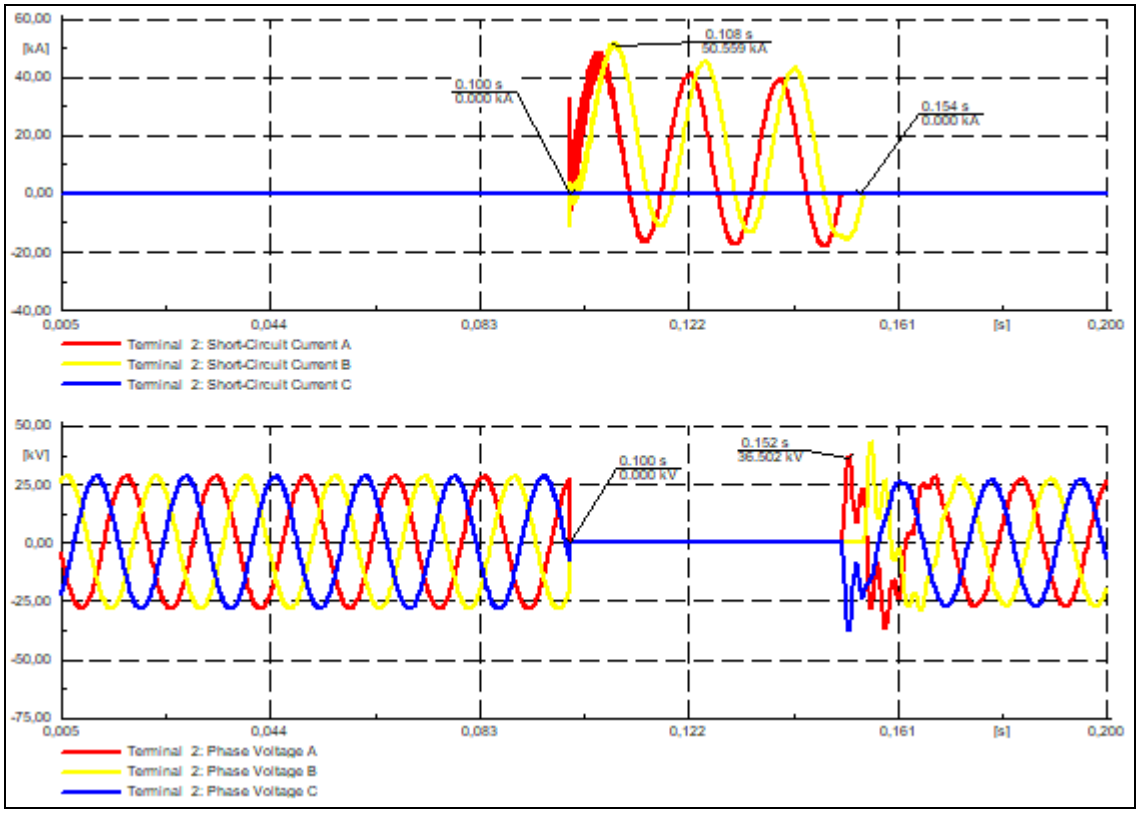


Figure 4.22: Voltage and current signals at terminal_2 for an internal double-phase fault

Figure 4.23 below shows the peak fault current magnitude of 3146.261kA on the LV side of the transformer at bus 9 for internal phase-to-phase-to-ground fault.

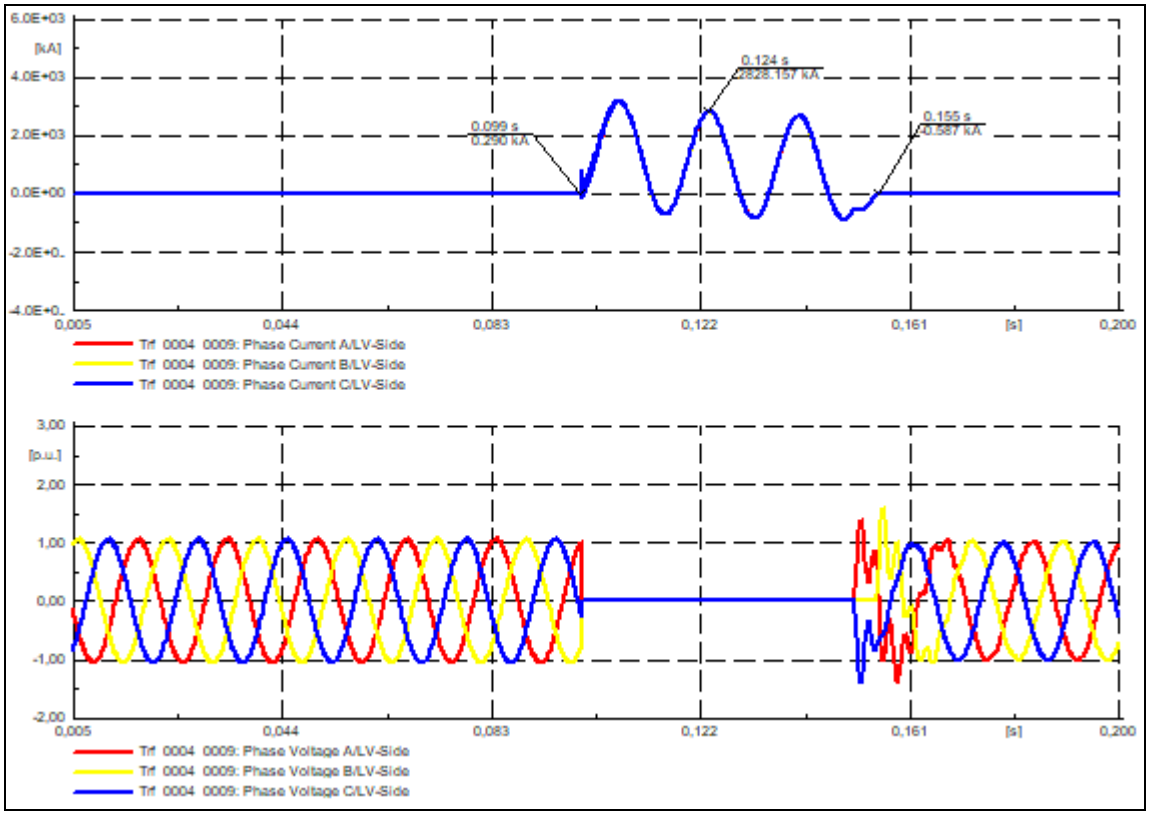


Figure 4.23: Voltage and current measured signals from the transformer for an internal phase-to-phase-to-ground fault

Table 4.20 below provides SEL-487E differential relay trip and clearing times for an internal LLG fault.

Table 4.20: SEL-487E differential relay response to an internal two-phase-to-ground fault

SEL 487E	Relay Type	: SEL 487E-1A					
S Ct : 132KV CT @ bus4	Location	: Busbar	: Bus_0004	/		Ratio	: 400A/1A
		Branch	: Breaker/Switch(1)			Connection	: Y
		Cubicle	: Cub_1(2)				
S Ct-3I033KV CT @ bus9	Location	: Busbar	: Bus_0009	/		Ratio	: 1600A/1A
		Branch	: Breaker/Switch			Connection	: Y
		Cubicle	: Cub_1(2)				
T Ct : 33KV CT @ bus9	Location	: Busbar	: Bus_0009	/		Ratio	: 1600A/1A
		Branch	: Breaker/Switch			Connection	: Y
		Cubicle	: Cub_1(2)				
T Ct-3I033KV CT @ bus9	Location	: Busbar	: Bus_0009	/		Ratio	: 1600A/1A
		Branch	: Breaker/Switch			Connection	: Y
		Cubicle	: Cub_1(2)				
U Ct : 33KV CT @ bus9	Location	: Busbar	: Bus_0009	/		Ratio	: 1600A/1A
		Branch	: Breaker/Switch			Connection	: Y
		Cubicle	: Cub_1(2)				
U Ct-3I033KV CT @ bus9	Location	: Busbar	: Bus_0009	/		Ratio	: 1600A/1A
		Branch	: Breaker/Switch			Connection	: Y
		Cubicle	: Cub_1(2)				
W Ct : 33KV CT @ bus9	Location	: Busbar	: Bus_0009	/		Ratio	: 1600A/1A
		Branch	: Breaker/Switch			Connection	: Y
		Cubicle	: Cub_1(2)				
X Ct : 33KV CT @ bus9	Location	: Busbar	: Bus_0009	/		Ratio	: 1600A/1A
		Branch	: Breaker/Switch			Connection	: Y
		Cubicle	: Cub_1(2)				
Logic : Logic					yout	:	0,015 s
Breaker	Cubicle	Branch	Busbar	/	Substation	Fault Clearing Time	
Breaker/Switch(1)	Cub_2	Breaker/Switch(1)	Terminal_1	/			0,015 s
				/			

The current differential plot for LLG internal fault is shown in Figure 4.24. The LLG fault produces a differential current of 5019.75A, and 5019.96A on phases B and C respectively and the differential relay trips at 0.015 seconds as shown in Table 4.20. Although phase A winding experienced a differential current of 479.26A, the restraint current was higher; therefore, the phase A differential element did not assert.

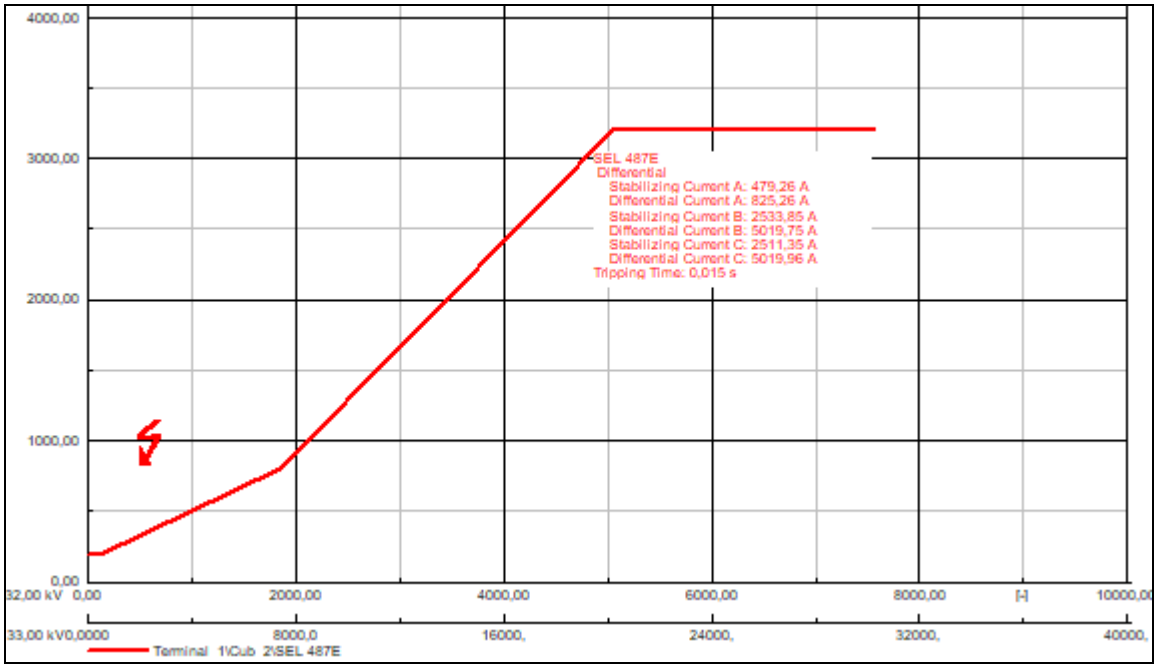


Figure 4.24: SEL-487E transformer differential plot for an internal double-phase to ground fault

IV. Internal Single-phase-to-ground (LG) fault

The aim of this case study is to investigate the operational characteristic of the transformer differential relay for an internal single phase to ground fault. The transformer is considered to be balanced and it is acceptable to study only one phase and adapt the same results for the two other phases. The EMT simulation is set to 0.2 seconds. The fault is introduced at 0.1 seconds and cleared at 0.15 seconds. The results obtained from the EMT simulation for LG fault are shown in Figures 4.25, 4.26 and 4.27 respectively.

As depicted in the Figure 4.25 below, the internal LG fault resulted in a current magnitude of 35.030kA in the yellow phase. Harmonics signals are shown in the blue and yellow phases as the system tries to recover from the internal LG internal fault.

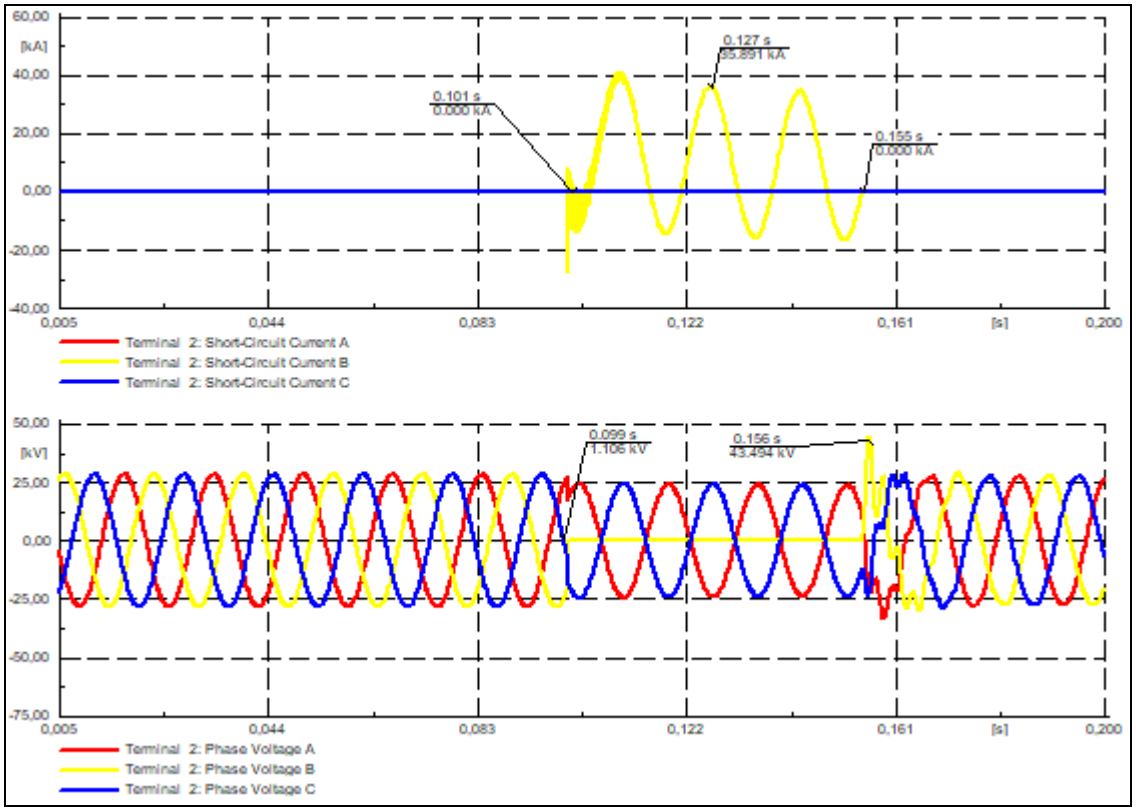


Figure 4.25: Voltage and current signals measured at terminal_2 for an internal single-phase to ground fault

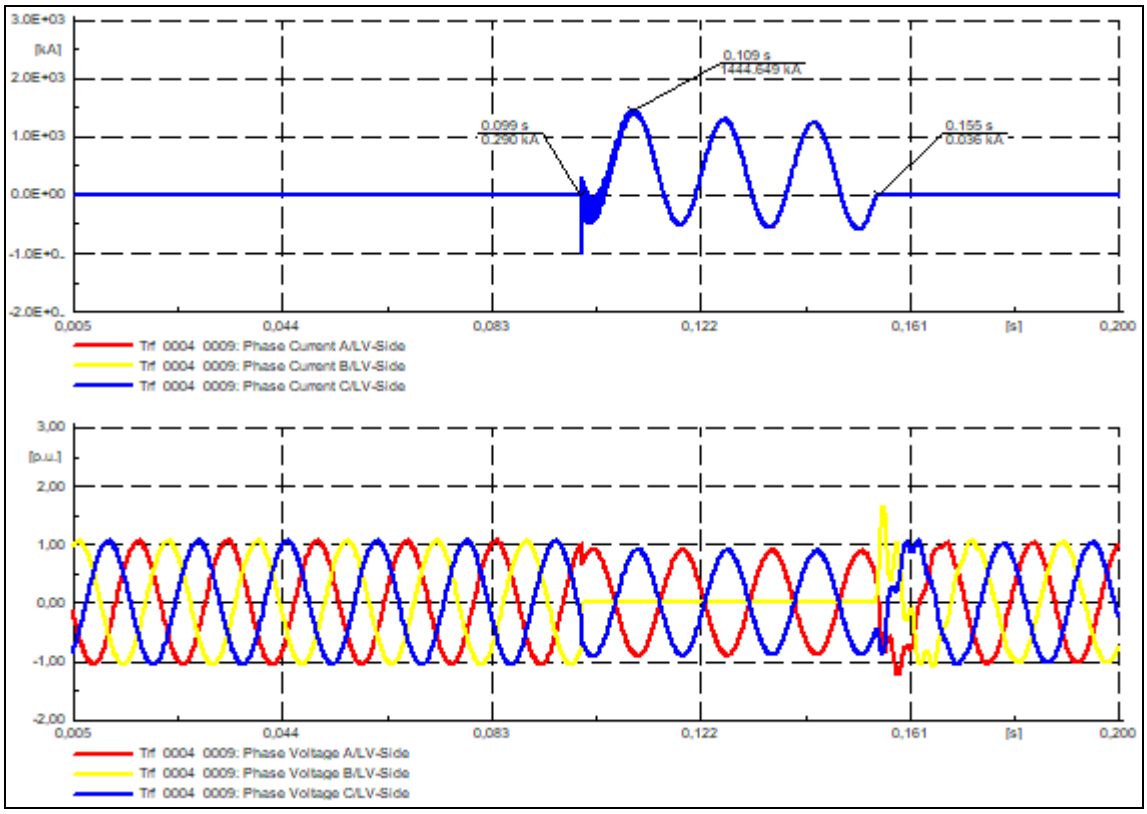


Figure 4.26: Transformer voltage and current signals for an internal single-phase to ground fault

From Figure 4.26 above, the peak fault current magnitude of 1444.649kA is produced for internal single-phase to ground fault at bus 9.

Table 4.21 below provides SEL-487E differential relay trip and clearing times for an internal LG fault.

Table 4.21: SEL-487E protection relay response to an internal two-phase-to-ground fault

SEL 487E	Relay Type : SEL 487E-1A				
S Ct : 132KV CT @ bus4	Location : Busbar	: Bus_0004	/	Ratio	: 400A/1A
	Branch	: Breaker/Switch(1)		Connection	: Y
	Cubicle	: Cub_1(2)			
S Ct-3I033KV CT @ bus9	Location : Busbar	: Bus_0009	/	Ratio	: 1600A/1A
	Branch	: Breaker/Switch		Connection	: Y
	Cubicle	: Cub_1(2)			
T Ct : 33KV CT @ bus9	Location : Busbar	: Bus_0009	/	Ratio	: 1600A/1A
	Branch	: Breaker/Switch		Connection	: Y
	Cubicle	: Cub_1(2)			
T Ct-3I033KV CT @ bus9	Location : Busbar	: Bus_0009	/	Ratio	: 1600A/1A
	Branch	: Breaker/Switch		Connection	: Y
	Cubicle	: Cub_1(2)			
U Ct : 33KV CT @ bus9	Location : Busbar	: Bus_0009	/	Ratio	: 1600A/1A
	Branch	: Breaker/Switch		Connection	: Y
	Cubicle	: Cub_1(2)			
U Ct-3I033KV CT @ bus9	Location : Busbar	: Bus_0009	/	Ratio	: 1600A/1A
	Branch	: Breaker/Switch		Connection	: Y
	Cubicle	: Cub_1(2)			
W Ct : 33KV CT @ bus9	Location : Busbar	: Bus_0009	/	Ratio	: 1600A/1A
	Branch	: Breaker/Switch		Connection	: Y
	Cubicle	: Cub_1(2)			
X Ct : 33KV CT @ bus9	Location : Busbar	: Bus_0009	/	Ratio	: 1600A/1A
	Branch	: Breaker/Switch		Connection	: Y
	Cubicle	: Cub_1(2)			
Logic : Logic			yout	:	0,015 s
Breaker	Cubicle	Branch	Busbar	/ Substation	Fault Clearing Time
Breaker/Switch(1)	Cub_2	Breaker/Switch(1)	Terminal_1	/	0,015 s
				/	

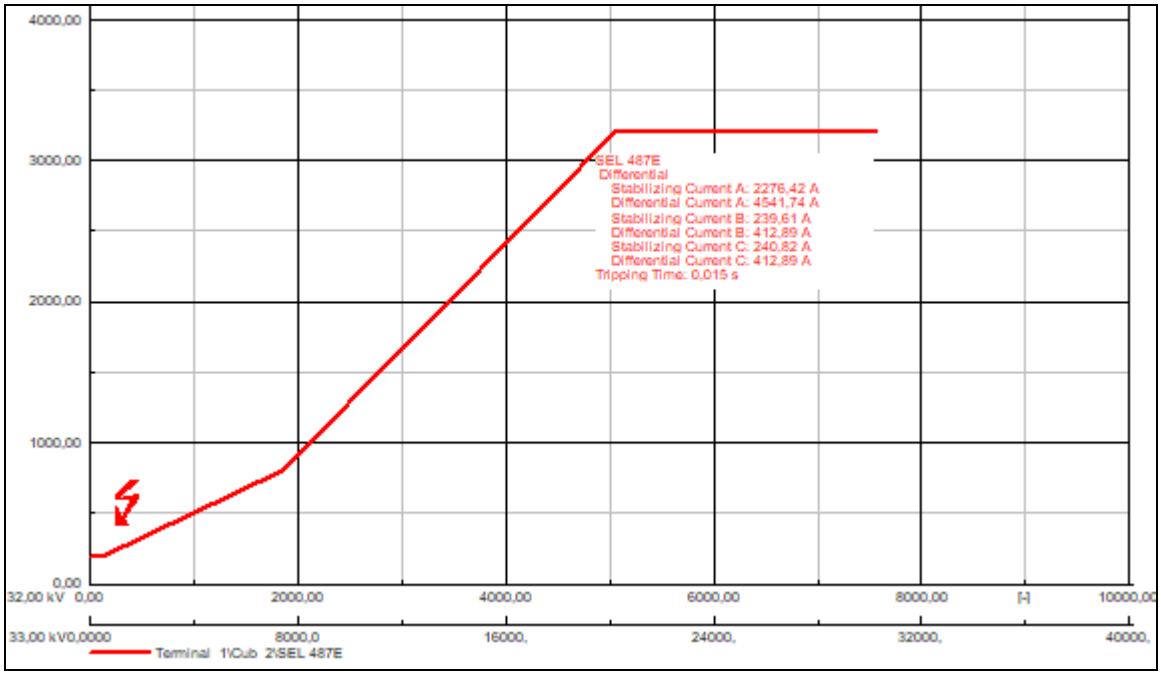


Figure 4.27: SEL-487E differential plot for an internal single-phase to ground fault

The current differential plot for the internal LG fault is shown in Figure 4.27. It is observed that differential currents of 4541.74A on phase A and of 412.89A on phases B and C respectively. The stabilising current is 4541.74A on phase A,

239.61A and 240.82A on phases B and C respectively. As shown in the Figure 4.27, the differential current in the red (A) phase was higher than the stabilizing current, and the differential relay tripped at 0.015s.

In summary, the transformer internal and external faults scenarios are studied, and the performance of the differential relay is observed through the DIgSILENT simulation results. Next section provides the implementation of the overcurrent scheme in the DIgSILENT simulation environment.

4.6 Overcurrent protection scheme in the DIgSILENT PowerFactory software environment

This section provides the engineering configuration and performance of the overcurrent protection elements which is used as backup protection for the power transformer, the main protection (differential) and the backup (overcurrent) are shown in Figure 4.28.

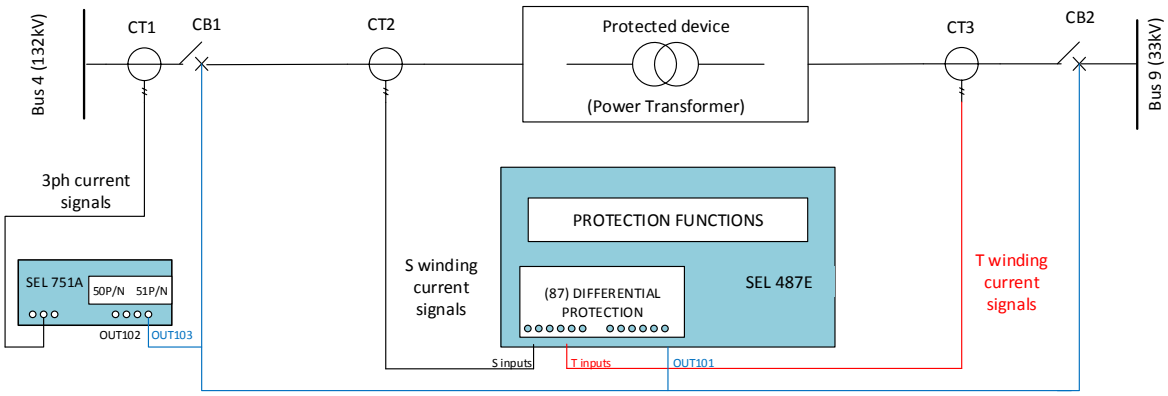


Figure 4.28: Transformer protection scheme using SEL-487E and SEL-751A

Operating time of the overcurrent relay defined by IEC 60255 and IEEE C37.112. The process follows the same steps for the next upstream relay and is repeated until the settings of the farthest up relay are calculated. Operating time defined by IEC 60255 and IEEE C37.112 are given in Equation (4.6):

$$t = \frac{k\,(\beta)}{\left(\frac{I}{I_s}\right)^{\alpha} - 1} + L \tag{4.6}$$

Where:

t Relay operating time in seconds

k Time dial, or time multiplier setting

I Fault current level in secondary amperes

IS Tap or pickup current selected

L constant

α Slope constant

β Slope constant

Table 4.22 provides the constant values of the parameters for curves defined by IEEE C37.112 and IEC 60255 standard. The pickup current and time multiplier settings are calculated by studying the transient fault condition on the IEEE 14-bus system. These transients study provide the pickup and time dial setting for the overcurrent elements as given in Tables 4.23 and 4.24 for the phase and residual elements respectively.

Table 4.22: IEEE and IEC constants for standards of overcurrent relays

IDMT curve description	Standard	α	β	L
Moderately inverse	IEEE	0.02	0.0515	0.114
Very inverse	IEEE	2	19.61	0.491
Extremely inverse	IEEE	2	28.2	0.1217
Inverse	US-CO8	2	5.95	0.18
Short-time inverse	US-CO2	0.02	0.02394	0.01694
Standard inverse	IEC	0.02	0.14	
Very inverse	IEC	1	13.5	
Extremely inverse	IEC	2	80.0	
Long-time inverse	IEC	1	120	

Tables 4.23 and 4.24 define the characteristic for the different overcurrent stages. They contain an IEC Normal Inverse and Definite Time scheme with different stages for a phase and residual overcurrent elements.

Table 4.23: Phase elements overcurrent relay parameters

Phase Elements Active	Name	Tripping characteristic	I Pick-up	Time	Reset ratio	Direction
Yes	I #1 Phase	IEC Normal Inverse	0.25 Iref	0.10	0.95	Non-Directional
Yes	I #2 Phase	IEC Definite Time	2.0 Iref	0.01	0.95	Non-Directional

Table 4.24: Residual elements relay parameters

Residual Elements Active	Name	Tripping characteristic	I Pick-up	Time	Reset ratio	Direction
Yes	I #1 Phase	IEC Normal Inverse	0.10 Iref	0.10	0.95	Non-Directional
Yes	I #2 Phase	IEC Definite Time	0.3 Iref	0.05	0.95	Non-Directional

In order to investigate the performance of the backup overcurrent protection scheme for the power transformer, five case studies were simulated in DIgSILENT PowerFactory. The following scenarios are simulated, and the performance of the overcurrent relay is studied, they are:

1) Case study One – Three phase fault at 132kV on the primary winding of the power transformer
2) Case study two – Double phase fault at 132kV on the primary winding of the power transformer
3) Case study three – Single phase to ground fault at 132kV on the primary winding of the power transformer
4) Case study four – Double phase to the ground at 132kV primary winding of the power transformer
5) Case study five – Transformer magnetisation inrush condition

4.6.1 Case study one: three-phase fault at 132kV on the primary side of the power transformer

The aim of this case study is to investigate the SEL751A overcurrent relay characteristics to a three-phase short circuit on the primary (132kV) winding of the power transformer. Technically the transformer differential protection is supposed to clear the three-phase fault without the option of the overcurrent element operation. However, it should be noted that this study case is conducted with the differential protection scheme out of service to simulate a situation in which a complete failure of the differential protection scheme exists, and in this case, the overcurrent protection scheme should provide backup for the power transformer.

The EMT simulation is set to 0.2 seconds. The fault is introduced into the network at 0.1 seconds and cleared at 0.15 seconds. The fault currents and voltage waveforms obtained from the Electromagnetic Transient (EMT) simulation are shown in Figure 4.29.

In Figure 4.29, the subplot at the top shows the current signals behaviour prior to and during the fault condition, and the subplot beneath indicates the voltage signals. It is evident from Figure 4.29 that the voltage in all the three phases is zero when the three-phase fault current is introduced in the network. Magnetisation inrush is also experienced as the system recovers from the fault.

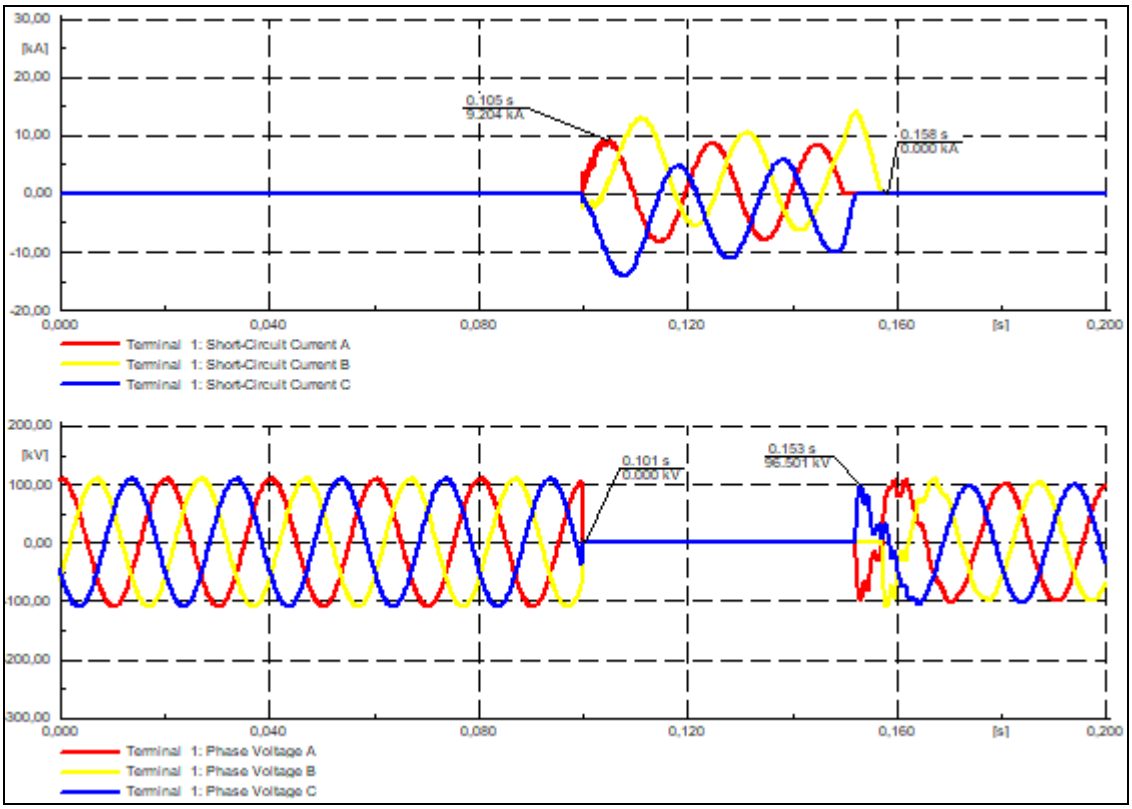


Figure 4.29: Terminal_1 current and voltage signals for a three-phase fault at HV side of the transformer

Table 4.25: SEL-751A relay response for a three-phase short-circuit

```
| SEL 751A                        Relay Type : SEL 751-1A                                                                  |
|   Ct    : 132KV CT @ bus4       Location   : Busbar       : Bus_0004          /                 Ratio       : 400A/1A    |
|                                              Branch       : Breaker/Switch(1)                   Connection  : Y          |
|                                              Cubicle      : Cub_1(2)                                                    |
|   CoreCt: Current Transformer   Location   : Busbar       : Terminal(1)       /                 Ratio       : 1600A/1A   |
|                                              Branch       : Trf_0004_0009                       Connection  : Y          |
|                                              Cubicle      : Cub_1                                                       |
|   51P1    : 51P1                ( IEC: I>t   ANSI: 51   )          Current  [sec.A]       [pri.A]          Tripping Time |
|     Current Setting :   0,220 sec.A     88,00 pri.A   0,220 p.u.      A :    15,517        6206,91             0,199 s  |
|     Time Dial       :   0,100     Time Shift :   1,000                B :    15,517        6206,91                      |
|     Characteristic  :   C1 - IEC Class A (Standard Inverse)           C :    15,517        6206,91                      |
|   50P1    : 50P1                ( IEC: I>>   ANSI: 50   )          Tripping Current       [pri.A]          Tripping Time |
|     Pickup Current  :   2,000 sec.A    800,00 pri.A   2,000 p.u.      A :    15,517        6206,91             0,020 s  |
|     Time Setting    :   0,000 s                                       B :    15,517        6206,91                      |
|     Total Time      :   0,020 s                                       C :    15,517        6206,91                      |
|   51G1    : 51G1                ( IEC: IE>t  ANSI: 51N  )          Tripping Current       [pri.A]          Tripping Time |
|     Current Setting :   0,100 sec.A    160,00 pri.A   0,100 p.u.             0,000          0,00           9999,999 s  |
|     Time Dial       :   0,100     Time Shift  :   1,000                                                                |
|     Characteristic  :   C1 - IEC Class A (Standard Inverse)                                                            |
|   50G1    : 50G1                ( IEC: IE>>  ANSI: 50N  )          Tripping Current       [pri.A]          Tripping Time |
|     Pickup Current  :   0,300 sec.A    480,00 pri.A   0,300 p.u.             0,000          0,00           9999,999 s  |
|     Time Setting    :   0,000 s                                                                                         |
|     Total Time      :   0,020 s                                                                                         |
|   Logic     : Logic                                                                  yout            :     0,020 s      |
|     Breaker           Cubicle      Branch                 Busbar              / Substation       Fault Clearing Time  |
|      Breaker/Switch(1) Cub_2        Breaker/Switch(1)      Terminal(1)         /                            0,020 s  |
|   Closing Logicclosing Logic          Tripping Block:                                 Tripping        :  9999,999 s      |
|     Breaker           Cubicle      Branch                 Busbar              / Substation       Fault Clearing Time  |
|      Breaker/Switch(1) Cub_2        Breaker/Switch(1)      Terminal(1)         /                            0,020 s  |
```

Table 4.25 provides the tripping times of the overcurrent relay for a three-phase fault. Definite-Time element operated at 0.020 seconds and inverse time overcurrent element at 0.199 seconds. It also shows the fault currents on both primary and secondary of the CT connected at the HV of the transformer and they are in this case

6206.91A and 15.517sec.A respectively for all the three phases. The ground element did not trip, and its trip time is 9999.999 seconds for the tripping time.

Table 4.26: Summary of the 50P1 and 51P1 tripping times for a three-phase fault at HV side of the transformer

SEL 751A Overcurrent Relay							
51P1				50P1			
Overcurrent element setting	**Threshold value**	**Measured value**	**Tripping time**	**Overcurrent element setting**	**Threshold value**	**Measured value**	**Tripping time**
Pickup	0.22 sec. A	15.517 sec A	0.199s	Pickup	2.0 sec A	15.517 sec A	0.020s
TMS	0.10			TMS	0.00		
Curve	C1			Curve	C1		

A time overcurrent curve of the SEL-751A relay is used to analyse the performance of the overcurrent relay. Inverse time overcurrent and Definite Time (DT) curves are used to analyse the overcurrent relay response for the three-phase fault. Figure 4.30 shows the time overcurrent curve and tripping times of the relay and Table 4.26 gives a summary of individual overcurrent element operating times.

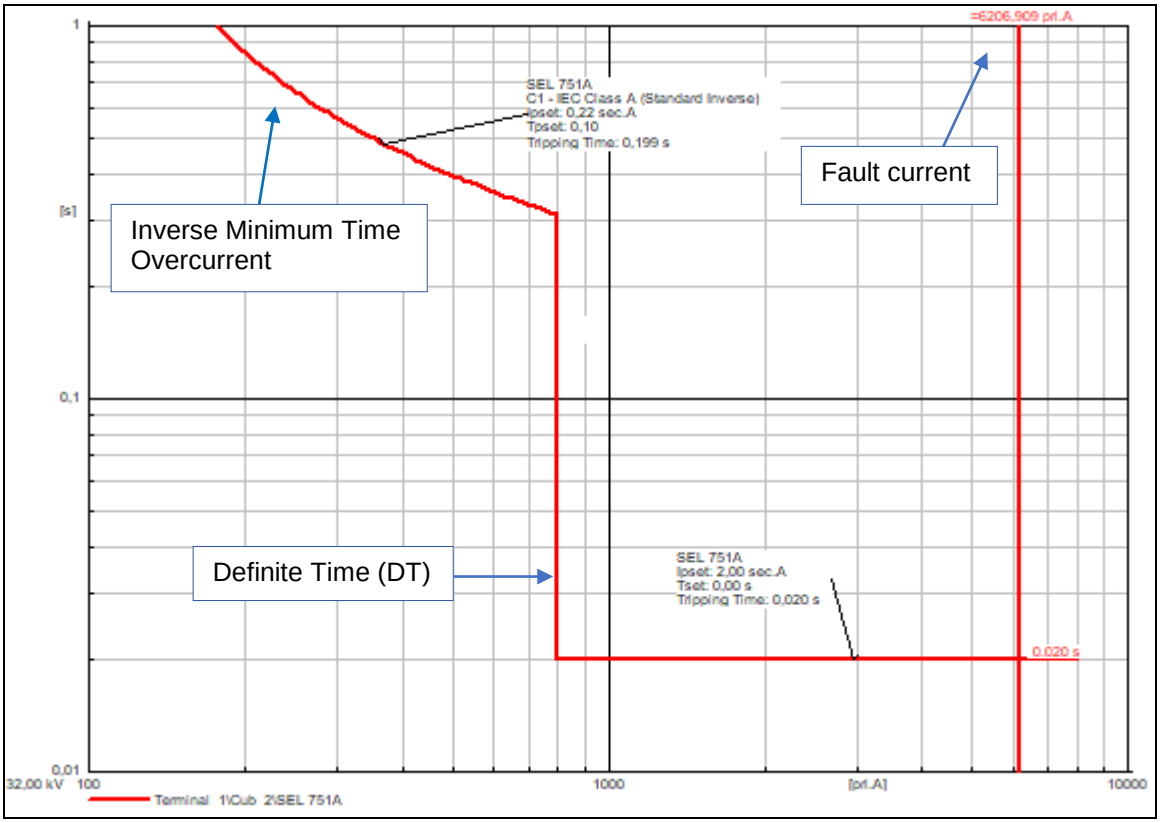


Figure 4.30: Overcurrent relay response for a three-phase fault at HV side of the transformer

From the tripping curve of the relay shown in Figure 4.30 above, it is noted that the fault triggers both of the relay elements (50P1 and 51P1). Definite time Element (50P1) clears the fault at 0.020 seconds, and 51P1 inverse time overcurrent element (51P1) will clear the fault at 0.199 seconds if supposedly the element 50P1 fails to clear.

4.6.2 Case study two: Double phase fault

This study aims to investigate the overcurrent relay response for a phase to phase fault on the HV (132kV) side of the transformer. Usually, the differential protection clears the fault, however, in this case, study the differential element is kept out of service to simulate a failure of the scheme.

The EMT simulation is run for a total time of 0.2 seconds. The fault is applied to the network at 0.1 seconds and clears at 0.15 seconds. The fault current and voltage signals obtained from the LL fault study case are shown in Figure 4.31.

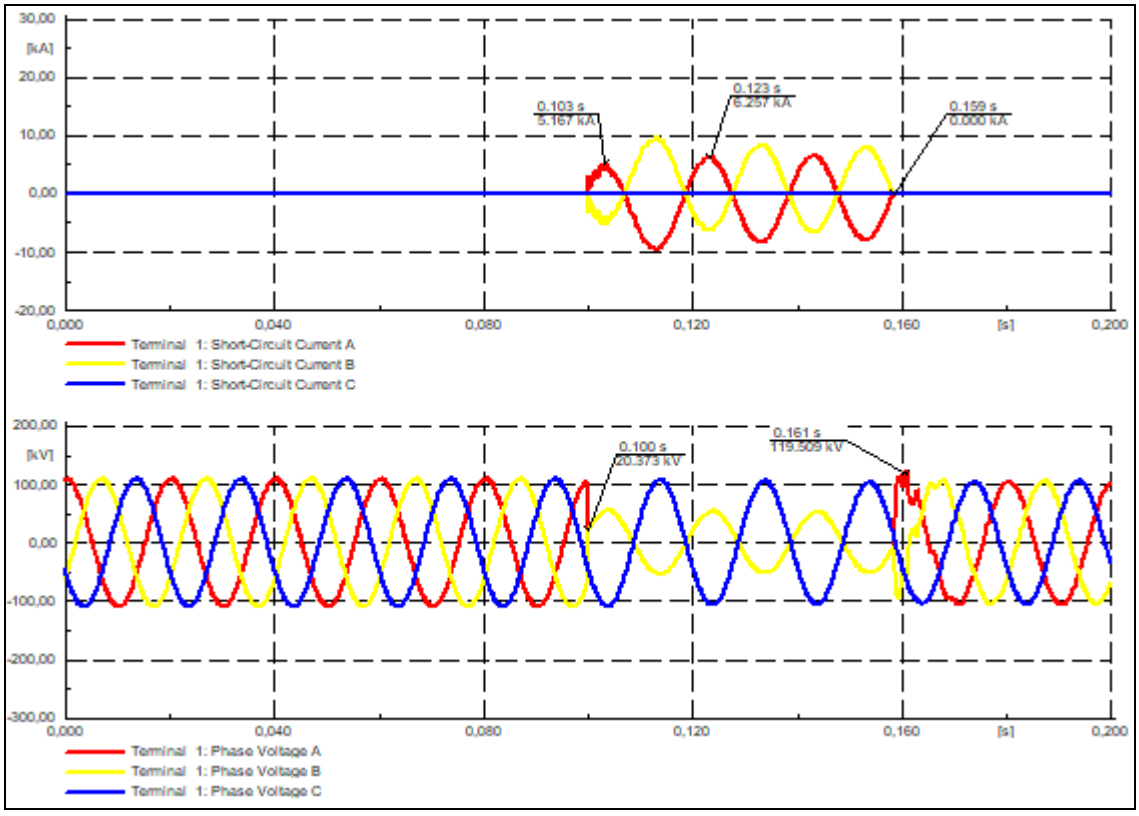


Figure 4.31: Teminal_1 current and voltage signals for a double-phase fault at HV side of the transformer

Figure 4.31 reveals that the voltage in the two faulted phases is reduced to 20.373kV and the fault current magnitude of 6.257kA. Figure 4.31 also shows the fault current only being cleared from the system after 0.15 seconds.

Table 4.27 provides the tripping time of the overcurrent for a phase-to-phase fault. Definite-time and for the inverse time overcurrent elements operated at 0.020 seconds and 0.199 seconds respectively. It also shows the fault currents on both primary and secondary of the CT connected at the HV of the transformer, in this case, 5383.08A and 13.457sec.A respectively for phases B and C and primary and 0.38A and 0.001sec.A for phase A, this is because it is a B-C fault. The ground element did not trip, and its tripping time is 9999.999 seconds.

Table 4.27: SEL-751A overcurrent relay response for a phase-to-phase short-circuit

```
| SEL 751A                        Relay Type : SEL 751-1A                                                                                    |
|   Ct    : 132KV CT @ bus4       Location   : Busbar       : Bus_0004           /                 Ratio       : 400A/1A                   |
|                                              Branch       : Breaker/Switch(1)                    Connection  : Y                         |
|                                              Cubicle      : Cub_1(2)                                                                     |
|   CoreCt: Current Transformer   Location   : Busbar       : Terminal(1)        /                 Ratio       : 1600A/1A                  |
|                                              Branch       : Trf_0004_0009                        Connection  : Y                         |
|                                              Cubicle      : Cub_1                                                                        |
|   51P1    : 51P1                ( IEC: I>t   ANSI: 51   )          Current  [sec.A]       [pri.A]          Tripping Time              |
|     Current Setting :   0,220 sec.A     88,00 pri.A   0,220 p.u.      A :     0,001          0,38              0,199 s                  |
|     Time Dial       :   0,100     Time Shift :   1,000                B :    13,457       5382,84                                     |
|     Characteristic  :   C1 - IEC Class A (Standard Inverse)           C :    13,458       5383,08                                     |
|   50P1    : 50P1                ( IEC: I>>   ANSI: 50   )          Tripping Current       [pri.A]          Tripping Time              |
|     Pickup Current  :   2,000 sec.A    800,00 pri.A   2,000 p.u.      A :     0,001          0,38              0,020 s                  |
|     Time Setting    :   0,000 s                                       B :    13,457       5382,84                                     |
|     Total Time      :   0,020 s                                       C :    13,458       5383,08                                     |
|   51G1    : 51G1                ( IEC: IE>t  ANSI: 51N  )          Tripping Current       [pri.A]          Tripping Time              |
|     Current Setting :   0,100 sec.A    160,00 pri.A   0,100 p.u.             0,000          0,00              9999,999 s               |
|     Time Dial       :   0,100     Time Shift  :   1,000                                                                                  |
|     Characteristic  :   C1 - IEC Class A (Standard Inverse)                                                                            |
|   50G1    : 50G1                ( IEC: IE>>  ANSI: 50N  )          Tripping Current       [pri.A]          Tripping Time              |
|     Pickup Current  :   0,300 sec.A    480,00 pri.A   0,300 p.u.             0,000          0,00              9999,999 s               |
|     Time Setting    :   0,000 s                                                                                                        |
|     Total Time      :   0,020 s                                                                                                        |
|   Logic     : Logic                                                                    yout            :     0,020 s                   |
|     Breaker           Cubicle      Branch                 Busbar              / Substation        Fault Clearing Time                |
|      Breaker/Switch(1) Cub_2        Breaker/Switch(1)      Terminal(1)         /                             0,020 s                  |
|   Closing Logiclosing Logic          Tripping Block:                          Tripping        :  9999,999 s                          |
|     Breaker           Cubicle      Branch                 Busbar              / Substation        Fault Clearing Time                |
|      Breaker/Switch(1) Cub_2        Breaker/Switch(1)      Terminal(1)         /                             0,020 s                  |
```

The relay tripping curve is shown in Figure 4.32, and a summary of the relay tripping times and the settings applied is given in Table 4.28.

Table 4.28: SEL-751A tripping times for a double phase fault at terminal_1

SEL 751A Overcurrent Relay							
51P1				50P1			
Overcurrent element setting	**Threshold value**	**Measured value**	**Tripping time**	**Overcurrent element setting**	**Threshold value**	**Measured value**	**Tripping time**
Pickup	0.22 sec. A	13.4577 sec A	0.199s	Pickup	2.0 sec A	13.457 sec A	0.020s
TMS	0.10			TMS	0.00		
Curve	C1			Curve	C1		

From the Figure 4.32, it can be observed that the phase to phase fault on the HV side of the transformer produced a fault current magnitude of 5383.07A and is cleared by the Definite Time (DT) element at 0.020 seconds. It is also noted that the

inverse time overcurrent element 51P1 clears the fault at 0.199 seconds, should the DT element fail to clear it.

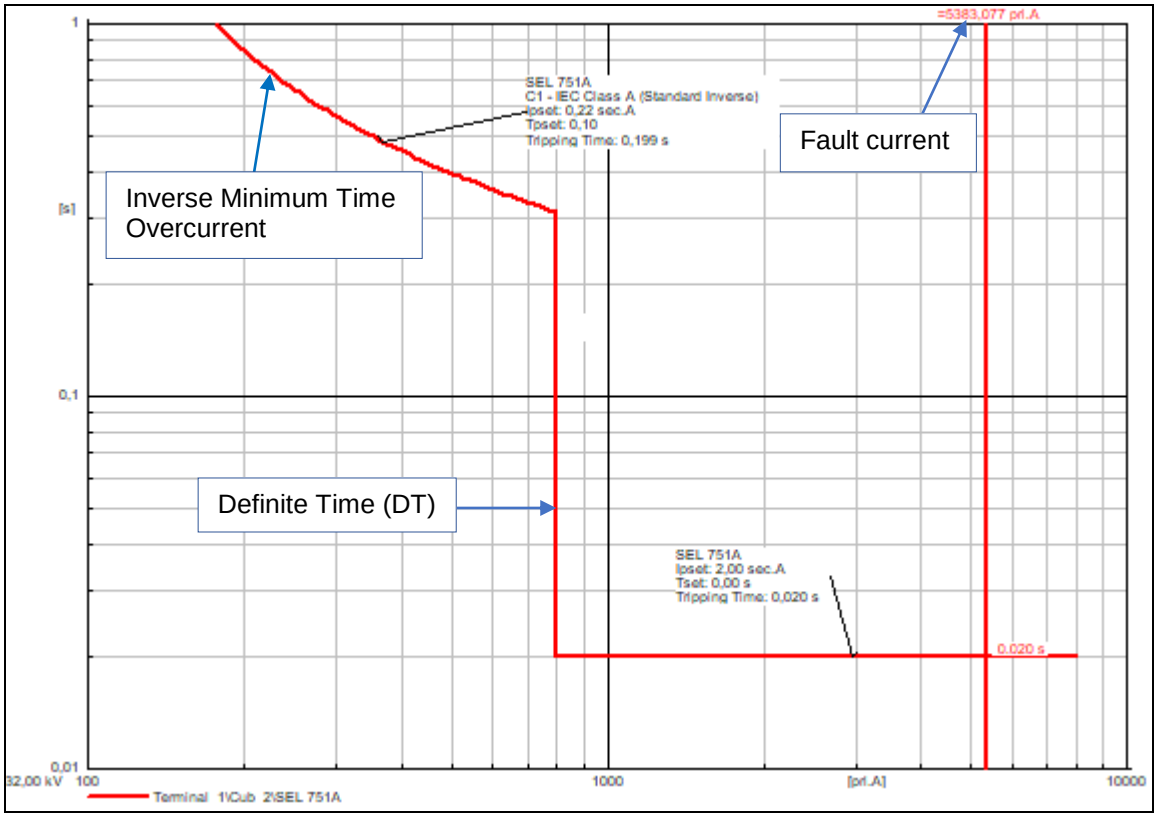


Figure 4.32: Overcurrent relay response for double phase fault at HV of the transformer

4.6.3 Case study three: Single-phase to ground fault

The aim of this case study is to investigate the SEL-751A overcurrent relay response for a single phase to ground fault on the HV side of the transformer. The electromagnetic transient simulation is conducted for a total time of 0.2 seconds. The fault is introduced in the system at 0.1 seconds and cleared at 0.15 seconds. The resulting fault current and voltage signals are shown in Figure 4.33.
Figure 4.33 depicts the voltage in the faulted phase red phase is zero and the current magnitude of 13.66kA on the faulted phase.

Table 4.29 provides the tripping time of the overcurrent for a single-phase to ground fault. Definite-time and for the inverse time overcurrent elements operated at 0.020 seconds and 0.199 seconds respectively. It also shows the fault currents on both primary and secondary of the CT connected at the HV of the transformer and they are in this case 4712.92A and 2.946sec.A respectively for phase A.

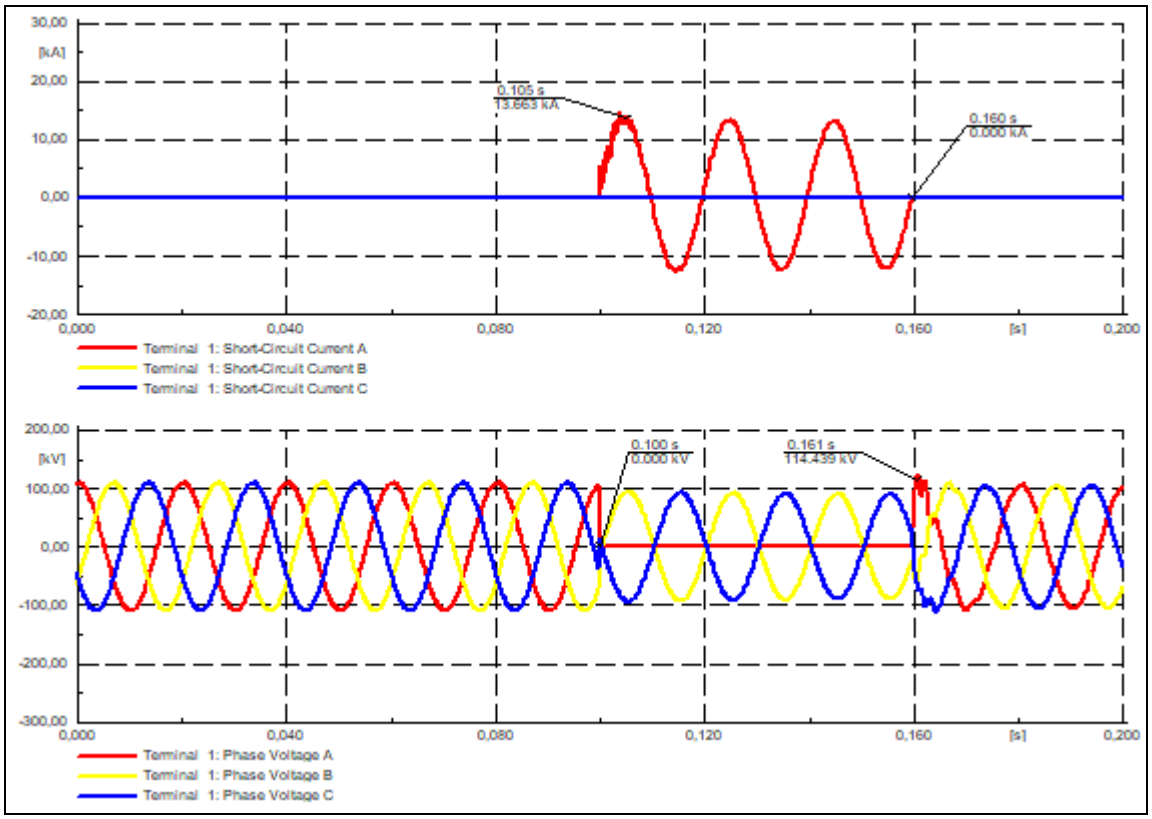


Figure 4.33: Terminal_1 current and voltage signals for a single-phase to ground fault

Table 4.29: SEL-751A protection results for a single-phase-to-ground short-circuit

```
| SEL 751A                        Relay Type : SEL 751-1A                                                                  |
|   Ct    : 132KV CT @ bus4       Location   : Busbar       : Bus_0004          /              Ratio       : 400A/1A      |
|                                              Branch       : Breaker/Switch(1)                Connection  : Y            |
|                                              Cubicle      : Cub_1(2)                                                    |
|   CoreCt: Current Transformer   Location   : Busbar       : Terminal_1        /              Ratio       : 1600A/1A     |
|                                              Branch       : Trf_0004_0009                    Connection  : Y            |
|                                              Cubicle      : Cub_1                                                       |
|   51G1    : 51G1                ( IEC: IE>t  ANSI: 51N  )         Tripping Current       [pri.A]          Tripping Time  |
|     Current Setting :   0,100 sec.A    160,00 pri.A   0,100 p.u.              2,946       4712,92             0,200 s    |
|     Time Dial       :   0,100     Time Shift  :   1,000                                                                  |
|     Characteristic  :   C1 - IEC Class A (Standard Inverse)                                                            |
|   50G1    : 50G1                ( IEC: IE>>  ANSI: 50N  )         Tripping Current       [pri.A]          Tripping Time  |
|     Pickup Current  :   0,300 sec.A    480,00 pri.A   0,300 p.u.              2,946       4712,92             0,020 s    |
|     Time Setting    :   0,000 s                                                                                        |
|     Total Time      :   0,020 s                                                                                        |
|   Logic     : Logic                                                                  yout            :     0,020 s      |
|     Breaker           Cubicle      Branch                 Busbar              / Substation       Fault Clearing Time    |
|      Breaker/Switch(1) Cub_2        Breaker/Switch(1)      Terminal_1          /                        0,020 s      |
|   Closing Logiclosing Logic          Tripping Block:                                 Tripping        :  9999,999 s      |
|     Breaker           Cubicle      Branch                 Busbar              / Substation       Fault Clearing Time    |
|      Breaker/Switch(1) Cub_2        Breaker/Switch(1)      Terminal_1          /                        0,020 s      |
```

Table 4.30: SEL-751A tripping times for a single-phase to ground fault at terminal_1

SEL 751A Overcurrent Relay							
51G1				50G1			
Overcurrent element setting	Threshold value	Measured value	Tripping time	Overcurrent element setting	Threshold value	Measured value	Tripping time
Pickup	0.10 sec. A	2.946 sec A	0.200s	Pickup	0.3 sec A	2.946 sec A	0.020s
TMS	0.10			TMS	0.00		

Curve	C1			Curve	C1		

The IDMT tripping curve is shown in Figure 4.34. A time overcurrent curve of the SEL-751A relay is used to analyse the performance of the overcurrent relay. Inverse time overcurrent and Definite Time (DT) curves are used to analyse the overcurrent relay response for the single-phase to ground fault.

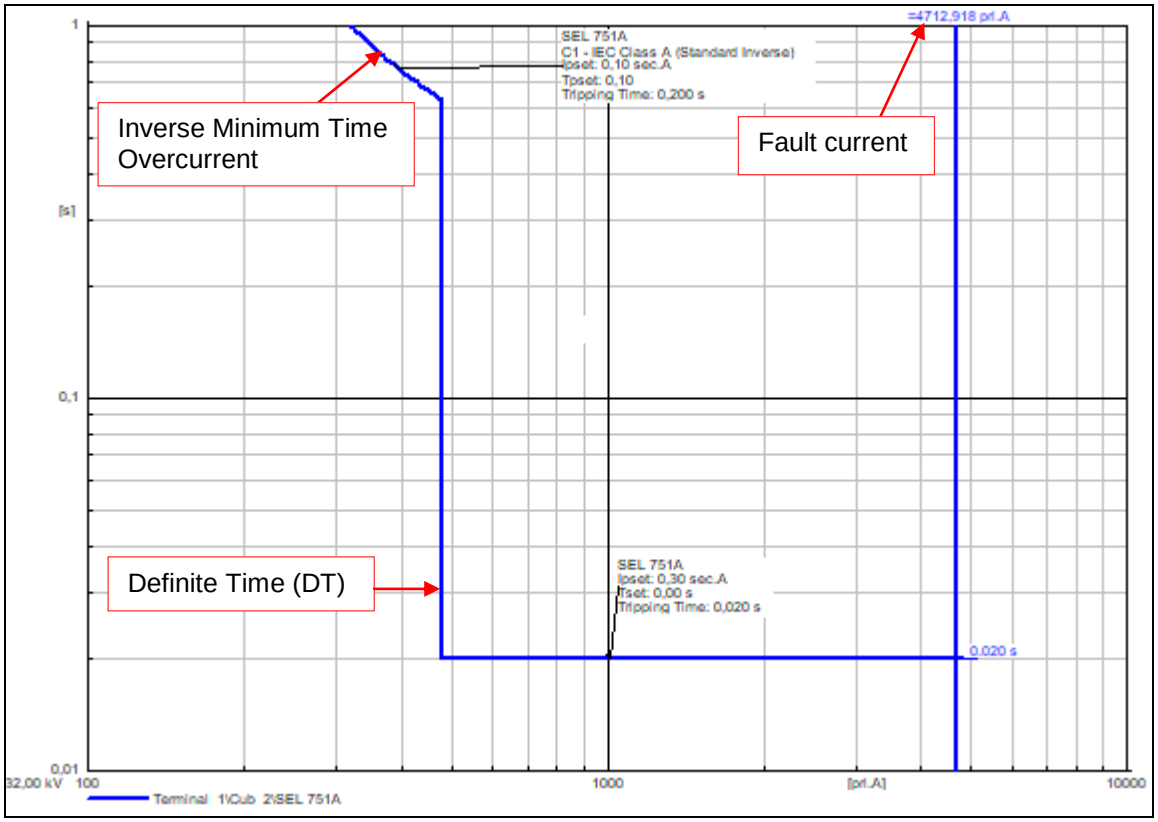


Figure 4.34: Overcurrent relay response for a single-phase to ground fault at HV side of the transformer

The overcurrent relay in this case study (LG) is similar to the behaviour observed in the case of study one for a three-phase short circuit. The fault current of the single-phase to ground fault is significantly higher than the three-phase short circuit results provided in Case study one.

4.6.4 Case study four: Double-phase to ground fault

This case study aims to investigate the overcurrent relay response for a double-phase to ground fault on the HV side of the transformer. The phases involved in the double-phase fault are the Red and Yellow phases.

An electromagnetic transient simulation study is conducted for a total simulation time of 0.2 seconds for double-phase to ground fault. The fault is introduced into the

system at 0.1 seconds and cleared at 0.15 seconds. The resulting fault currents and voltage signals are shown in Figure 4.35.

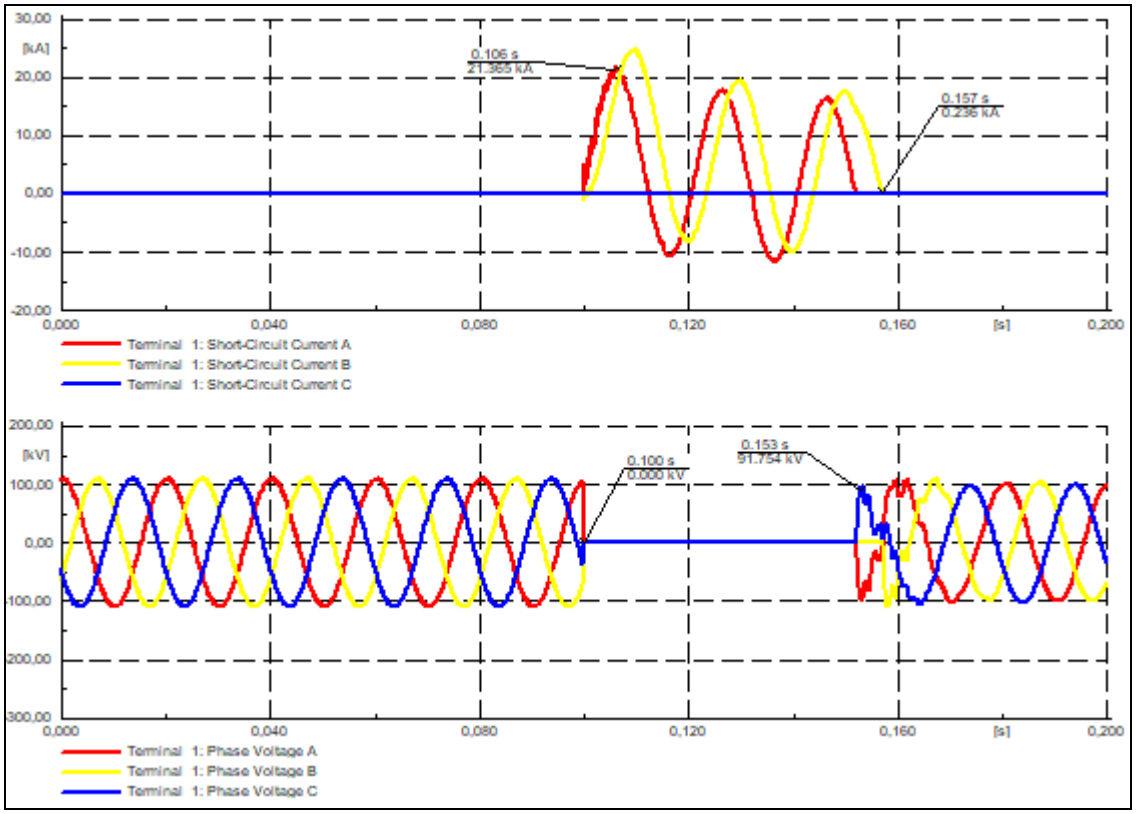


Figure 4.35: Terminal_1 current and voltage signals for a double-phase to ground fault

Figure 4.35 depicts the voltage in the faulted phases is zero during the transient period. The voltage arises again in the sub-transient period and attenuated.

Table 4.31: SEL-751A protection results for a double-phase-to-ground short-circuit

SEL 751A		Relay Type : SEL 751-1A					
Ct : 132KV CT @ bus4		Location : Busbar	: Bus_0004	/		Ratio	: 400A/1A
		Branch	: Breaker/Switch(1)			Connection	: Y
		Cubicle	: Cub_1(2)				
CoreCt: Current Transformer		Location : Busbar	: Terminal_1	/		Ratio	: 1600A/1A
		Branch	: Trf_0004_0009			Connection	: Y
		Cubicle	: Cub_1				
51G1 : 51G1		(IEC: IE>t ANSI: 51N)		Tripping Current	[pri.A]		Tripping Time
Current Setting :	0,100 sec.A	160,00 pri.A	0,100 p.u.	5,883	9412,97		0,199 s
Time Dial :	0,100	Time Shift :	1,000				
Characteristic :	C1 - IEC Class A (Standard Inverse)						
50G1 : 50G1		(IEC: IE>> ANSI: 50N)		Tripping Current	[pri.A]		Tripping Time
Pickup Current :	0,300 sec.A	480,00 pri.A	0,300 p.u.	5,883	9412,97		0,020 s
Time Setting :	0,000 s						
Total Time :	0,020 s						
Logic : Logic					yout	:	0,020 s
Breaker	Cubicle	Branch	Busbar	/ Substation		Fault Clearing Time	
Breaker/Switch(1)	Cub_2	Breaker/Switch(1)	Terminal_1	/			0,020 s
Closing Logic	closing Logic	Tripping Block:			Tripping	:	9999,999 s
Breaker	Cubicle	Branch	Busbar	/ Substation		Fault Clearing Time	
Breaker/Switch(1)	Cub_2	Breaker/Switch(1)	Terminal_1	/			0,020 s

Table 4.31 provides the tripping time of the overcurrent for a single-phase to ground fault. Definite-time and for the inverse time overcurrent elements operated at 0.020 seconds and 0.199 seconds respectively. It also shows the fault currents on both

primary and secondary of the CT connected at the HV of the transformer and they are in this case 9412.97A and 5.883sec.A respectively for double phase A and B.

Table 4.32: 751A tripping times for a double-phase to ground fault at bus 4

SEL 751A Overcurrent Relay							
51G1				50G1			
Overcurrent element setting	**Threshold value**	**Measured value**	**Tripping time**	**Overcurrent element setting**	**Threshold value**	**Measured value**	**Tripping time**
Pickup	0.10 sec. A	5.883 sec A	0.199s	Pickup	0.3 sec A	5.883 sec A	0.020s
TMS	0.10			TMS	0.00		
Curve	C1			Curve	C1		

The time-overcurrent characteristic of the relay is shown in Figure 4.36.

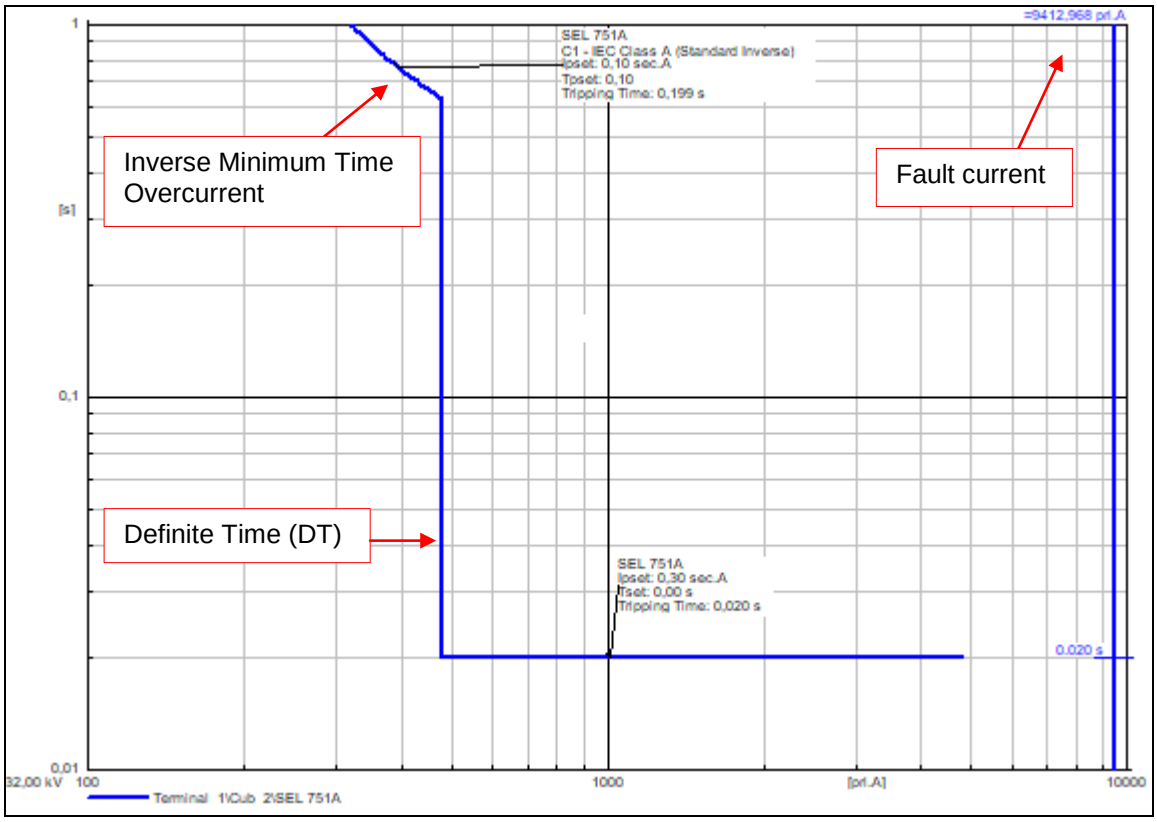


Figure 4.36: Overcurrent relay response for a double-phase to ground fault at HV side of the transformer

Figure 4.36 shows the definite time (50G1) element clears the fault at 0.02 seconds. Suppose, if 50G1 element fails to clear the fault, the inverse element 51G1 clears the fault at 0.199 seconds.

4.6.5 Case study five: Transformer Magnetizing Inrush Current

Transformer Magnetizing Inrush Current (TMIC) is a phenomenon that arises from energisation or any transient condition in the transformer circuit. During TMIC a significant amount of inrush currents flow into the transformer without a corresponding current leaving. The differential relay, overcurrent relay and distance protection relay identify this inrush current as a fault. The inrush current has second and fifth harmonic currents, which makes it easy for an intelligent electronic device to detect it. Most transformer differential protection IEDs have the capability to detect inrush currents by measuring the level of harmonics flowing into the transformer. The overcurrent relay backup protection for the transformer (SEL-751A) on the other hand, does not have this capability and may operate during inrush conditions.

This case study aims to investigate the overcurrent relay behaviour during the inrush condition. It should, however, be noted that the standard transformer model in DIgSILENT Power Factory simulation environment does not have the property of inrush currents during energisation. As a result, the transformer magnetizing inrush current estimation peaks must be calculated by the user and the data defined into DIgSILENT simulation environment manually. Thereafter a TMIC phenomenon can be simulated by triggering a switch event.

The key insight is that the residual flux in the transformer core directly dictates the magnitude of the inrush current. Further, we know the inrush current is a transient phenomenon subject to decay in an exponential manner.
The peak inrush current is calculated using Equation (4.7) to (4.10) as given below (Kulkani S.V. and Khaparde S.A., 2004). The system reactance is calculated using Equation (4.7):

$$X_s = \frac{\mu_0 N^2 A_w}{h_w} \times 2 \times \pi \times f \tag{4.7}$$

Where:

μ_0 – permeability of free space

f – system frequency in Hz

N – number of turns on the excited winding

X_s – System supply reactance in Ω

A_w – Area inside the mean turn of excited winding m^2

h_w – height of energised winding in m

Table 4.33 below provides the parameters of a 100MVA, 132/33kV transformer according to reference (Kulkani S.V. and Khaparde S.A., 2004).

Table 4.33: Design parameters of the power transformer

Name	Parameter	Value
Apparent power	S	100MVA
The active area of the core	A_{fe}	302927mm2
The area covered by the windings in plan with the above	A_w	1.025m2
System resistance	R%	2.39%
System reactance	X%	21%
Height of energized winding	H_w	1.77m
Number of turns on the primary winding	N_1	230
Number of turns on the secondary winding	N_2	920
Saturation flux density	B_s	2.03T
Peak value of the designed steady state flux density in the core	B_{mp}	1.7T
Correctional factor for saturation angle	K1	0.9
correctional factor for the peak value	K2	1.15

The phase angle of the voltage is calculated using Equation (4.8):

$$\theta = K_1 cos^{-1}\left(\frac{B_s - B_{mp} - B_r}{B_{mp}}\right) \quad (4.8)$$

Where:

B_s – saturation flux density (2.03T)

B_{mp} – peak value of the designed steady state flux density in the core (1.7T)

B_r – Residual flux density (0.8 x Bmp)

K_1 – correctional factor for saturation angle (0.9)

The peak inrush current for the first cycle can then be calculated using Equation (4.9):

$$i_o = \frac{h_w H}{N_1} = \frac{(2B_{mp} + B_r - B_{sat})A_{fe}h_w}{m\mu_o A_w N_1}$$

or

$$i_{omax} = \frac{k_2 V\sqrt{2}}{X_s}(1 - cos\theta) \quad (4.9)$$

Where:

V – RMS voltage applied at energisation

K_2 – correctional factor for the peak value (1.15)

The residual flux at the end of the first cycle is calculated using Equation (4.10):

$$B_{r(new)} = B_{r(old)} - B_{mp} \times \frac{K_3 R}{X_s}[2(sin\theta - \theta cos\theta)] \quad (4.10)$$

Where:

R – sum of transformer winding resistance and system resistance

K_3 – correctional factor for the decay of inrush (2.26)

The first peak estimation of the inrush current is 3.1kA. The rated current is 440A. The peak values for the first 5 cycles have been calculated according to equations 4.7-4.10 and the results as given Table 4.34.

Table 4.34: TMIC peak values with their corresponding flux

Cycle	Current peak (kA)	Flux peak (p.u)
1	3.1434	0.599
2	3.151	0.602
3	3.1587	0.605
4	3.1663	0.608
5	3.1739	0.611

With peak TMIC values, the EMT simulation is conducted whereby the transformer is de-energised at 0.005 seconds and energised at 0.1 seconds. The TMIC results are shown in Figures 4.38, 4.39 and 4.40. With the calculated estimation values of the inrush peak currents and their corresponding flux defined in the DIgSILENT software, the breaker is closed at 100ms.

The calculated TMIC values are then transferred into DIgSILENT PowerFactory as shown in Figure 4.37.

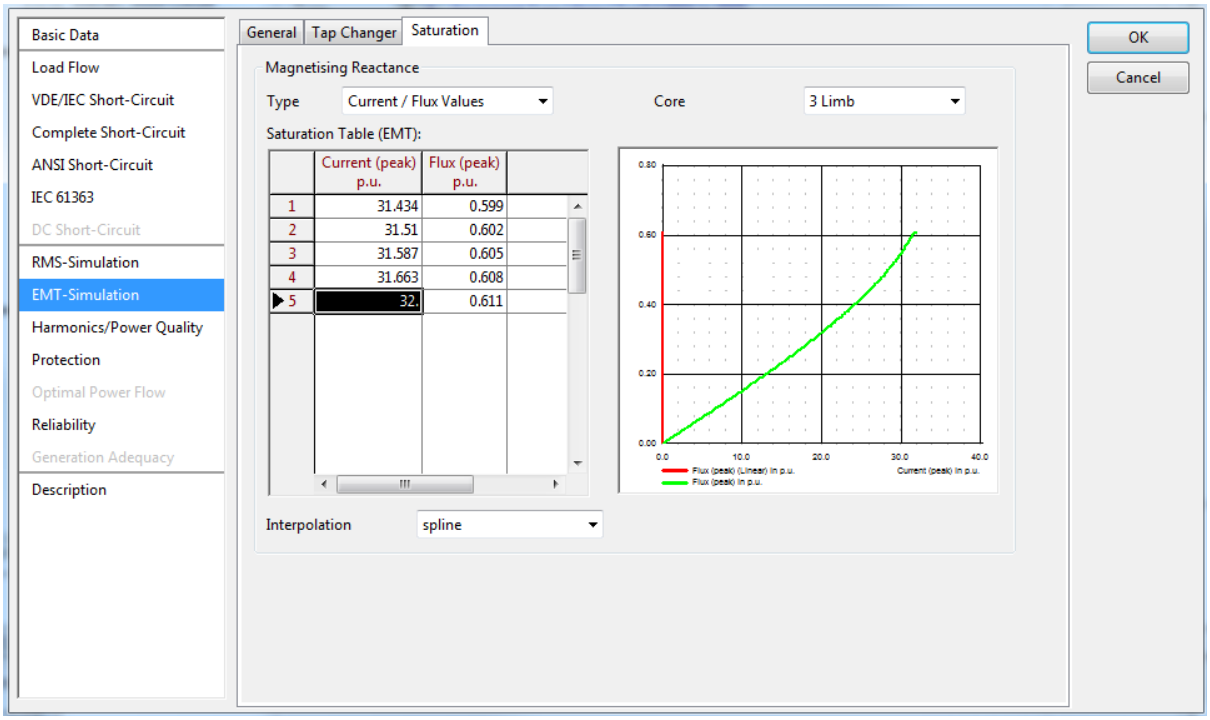


Figure 4.37: TMIC peak values in the DIgSILENT environment

From Figure 4.38, the transformer is assumed to be energised at the instant when the voltage is at zero value. It is also assumed that the residual flux in the same direction as that of the initial flux change, thus giving a maximum possible value of inrush current after the core saturation. The DIgSILENT simulated inrush current peaks for the first 5 cycles correspond to the hands-on calculated inrush current peaks estimation values using Equations (4.7) to (4.9) and given in Table 4.34.

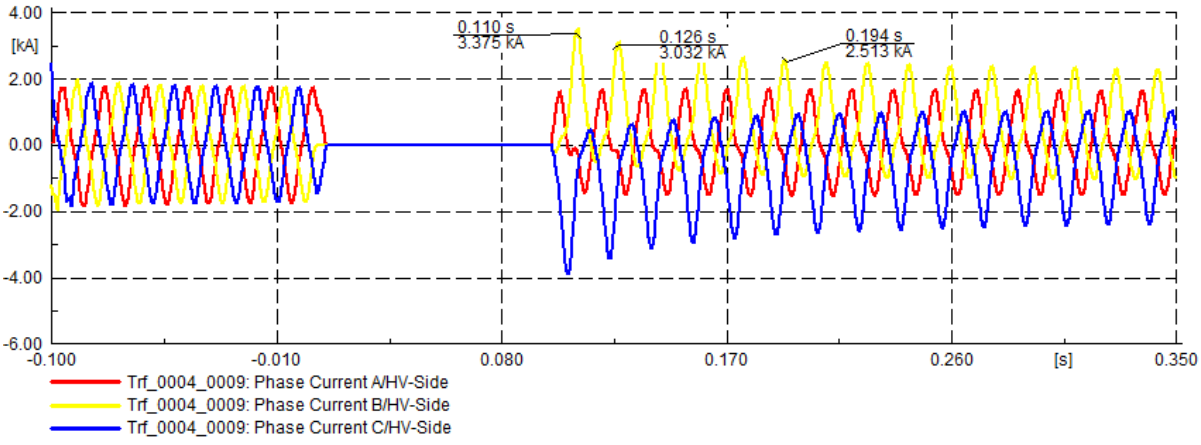


Figure 4.38: Transformer inrush currents signals

It can be observed that SEL-751A overcurrent relay tripped at 127.958ms as shown in Figure 4.40 after the second switching event and the current reaches completely zero at 132ms as shown in 4.39. Clearly, it is observed that SEL-751A used as a back-up for the power transformer protection which considers the inrush current as a

fault and it is opening the breaker and disconnects the power transformer from the system.

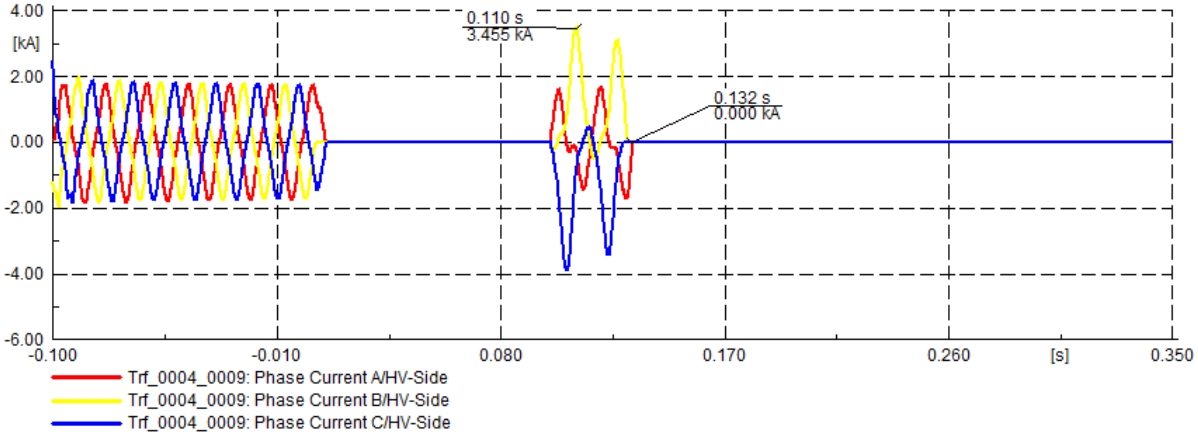


Figure 4.39: SEL-751A overcurrent relay tripping during transformer magnetizing inrush current

```
(t=-100:000 ms) Initial conditions calculated.
(t=005:000 ms) -------------------------------------------------------------
(t=005:000 ms) 'Grid\Breaker/Switch.ElmCoup':
(t=005:000 ms) Circuit-Breaker Action: 'Open' - 'All phases'.
(t=005:000 ms) -------------------------------------------------------------
(t=005:000 ms) 'Grid\Breaker/Switch(1).ElmCoup':
(t=005:000 ms) Circuit-Breaker Action: 'Open' - 'All phases'.
(t=005:645 ms) Element ' Gen_0001' is local reference in separated area of ' Bus_0001'
(t=005:645 ms) Grid split into 2 isolated areas
(t=005:645 ms) Element ' Gen_0001' is reference in 60.0 Hz-system
(t=005:823 ms) Element ' Gen_0001' is local reference in separated area of ' Bus_0001'
(t=005:823 ms) Grid split into 2 isolated areas
(t=005:823 ms) Element ' Gen_0001' is reference in 60.0 Hz-system
(t=009:826 ms) Element ' Gen_0001' is local reference in separated area of ' Bus_0001'
(t=009:826 ms) Grid split into 2 isolated areas
(t=009:826 ms) Element ' Gen_0001' is reference in 60.0 Hz-system
(t=009:875 ms) Element ' Gen_0001' is local reference in separated area of ' Bus_0001'
(t=009:875 ms) Grid split into 2 isolated areas
(t=009:875 ms) Element ' Gen_0001' is reference in 60.0 Hz-system
(t=010:116 ms) Element ' Gen_0001' is local reference in separated area of ' Bus_0001'
(t=010:116 ms) Grid split into 2 isolated areas
(t=010:116 ms) Element ' Gen_0001' is reference in 60.0 Hz-system
(t=100:000 ms) -------------------------------------------------------------
(t=100:000 ms) 'Grid\Breaker/Switch.ElmCoup':
(t=100:000 ms) Circuit-Breaker Action: 'Close' - 'All phases'.
(t=100:000 ms) -------------------------------------------------------------
(t=100:000 ms) 'Grid\Breaker/Switch(1).ElmCoup':
(t=100:000 ms) Circuit-Breaker Action: 'Close' - 'All phases'.
(t=100:000 ms) Element ' Gen_0001' is local reference in separated area of ' Bus_0001'
(t=100:000 ms) Element ' Gen_0001' is reference in 60.0 Hz-system
(t=127:958 ms) -------------------------------------------------------------
(t=127:958 ms) 'Grid\Terminal(1)\Cub_2\SEL 751A.ElmRelay':
(t=127:958 ms) Relay is tripping. 'Open' signal is sent to the connected breaker(s).
(t=127:958 ms) -------------------------------------------------------------
(t=127:958 ms) 'Grid\Breaker/Switch(1).ElmCoup':
(t=127:958 ms) Circuit-Breaker Action: 'Open' - 'All phases'.
(t=129:314 ms) Element ' Gen_0001' is local reference in separated area of ' Bus_0001'
(t=129:314 ms) Element ' Gen_0001' is reference in 60.0 Hz-system
(t=131:121 ms) Element ' Gen_0001' is local reference in separated area of ' Bus_0001'
(t=131:121 ms) Element ' Gen_0001' is reference in 60.0 Hz-system
(t=133:228 ms) Element ' Gen_0001' is local reference in separated area of ' Bus_0001'
(t=133:228 ms) Element ' Gen_0001' is reference in 60.0 Hz-system
```

1st Switch event-Transformer de-energized

2nd Switch event-Transformer energized to simulate TMIC

SEL-751A tripping due to TMIC

Figure 4.40: Transformer inrush current report in the DIgSILENT environment

Figure 4.40 shows the report of the switching events that causes the magnetizing inrush current conditions in the DIgSILENT environment. The inrush current shows that first switching event (transformer de-energisation) occurs at 5ms which open the three poles of the circuit breaker. The second switching event (transformer energisation) occurs at 100ms which closes the circuit breaker and at the same time the SEL-751A overcurrent relay sends a trip signal to open the breakers due to inrush current produced on transformer energisation.

Therefore, it is necessary to send a blocking signal to the overcurrent relay in order to prevent it from tripping during the inrush condition on the power transformer. This is not feasible in the DIgSILENT environment because the SEL-751A relay model in the DIgSILENT has limited functions. So, the hardware-in-the-loop simulation needs to be conducted to implement the blocking scheme for the power transformer. The test bench test is implemented at CSAEMS laboratory for inrush blocking scheme, and it is described in chapter five.

4.7 Conclusion

This chapter has provided a transformer protection scheme implementation in a DIgSILENT simulation environment. The IEEE 14-Bus system is used to simulate the transformer differential protection scheme using DIgSILENT software package. Load flow was simulated, and the results were analysed. Performance of the transformer differential scheme is studied for both external and internal fault conditions.

From the simulation result, it is evident that an overcurrent relay will mal-operate due to transformer magnetizing inrush currents. It is also clear from the simulation results that the differential protection relay (SEL-487E) has not tripped due to TMIC. The proposed solution is to implement a test bench for the reverse harmonic blocking scheme. The proposed scheme can utilise blocking signals derived from the SEL-487E relay to inhibit the SEL-751A overcurrent relay from mal-operating due to TMIC. A lab-scale implementation of this scheme is discussed in the next chapter. A lab-scale test bench is developed to simulate transformer external and internal events. The performance of transformer differential and overcurrent schemes are studied in the next chapter.

CHAPTER FIVE
IMPLEMENTATION OF THE LAB SCALE TEST BENCH TO TEST DIFFERENTIAL AND OVERCURRENT PROTECTION SCHEMES FOR POWER TRANSFORMER

5.1 Introduction

The most critical components in a power transmission and distribution system are the transformers, the generators and the busbars. Usually, differential relays are applied as their main protection against short-circuit faults within the protected area (G Rockefeller, 2007). The current differential principle is based on Kirchhoff's law, i.e. the sum of the currents flowing into a conducting network is zero. During a fault in the protected zone, a current will flow from one phase to another phase or ground. In this case, the sum of the measured currents in at least one phase is not zero. Therefore, the relay can detect the fault and issue a trip signal to the circuit breakers to clear the fault.

This chapter provides the lab-scale test bench setup to test the differential and overcurrent protection schemes for the power transformer. The differential SEL-487E relay configuration setting which includes trip time characteristic and harmonic restraint is described in detail. The overcurrent relay SEL-751A configuration settings which includes both the definite-time (50) and inverse minimum time (51) overcurrent elements are used as a backup protection for the power transformer. The test injection Omicron CMC 356 is used to provide the necessary currents and voltages to test the differential and overcurrent functions of the power transformer. The test universe software of the Omicron device used to provide the pre-set differential and overcurrent test modules templates which are used to test the hardwired and differential and overcurrent protection functions of the SEL-487E and SEL-751A IEDs respectively in the lab-scale environment.

The lab-scale test bench set up simulation results of the differential and overcurrent protection schemes is compared with DigSilent simulation results.

5.2 Differential and overcurrent protection setting on numerical relays

This section provides the lab-scale test bench setup for the differential (SEL-487E) and overcurrent (SEL-751A) protection elements and is tested using the Omicron test injection device. It also provides the differential protection setting of SEL-487E transformer protection numerical relays (SEL-487E Instruction manual, 2012) and

OMICRON test injection device (Omicron manual). The differential protection test bench setup is shown in Figure 5.1. The test bench setup has transformer protection intelligent electronic device (SEL-487E), Overcurrent IED (SEL-751A), OMICRON test injection device (CMC 356) and a personal computer loaded with the relay configuration tools (AcSELerator Quickset and Test universe software). The equipment in the lab-scale test bench setup is connected using static IP network and Ruggedcom Ethernet Switch as shown in Figure 5.1.

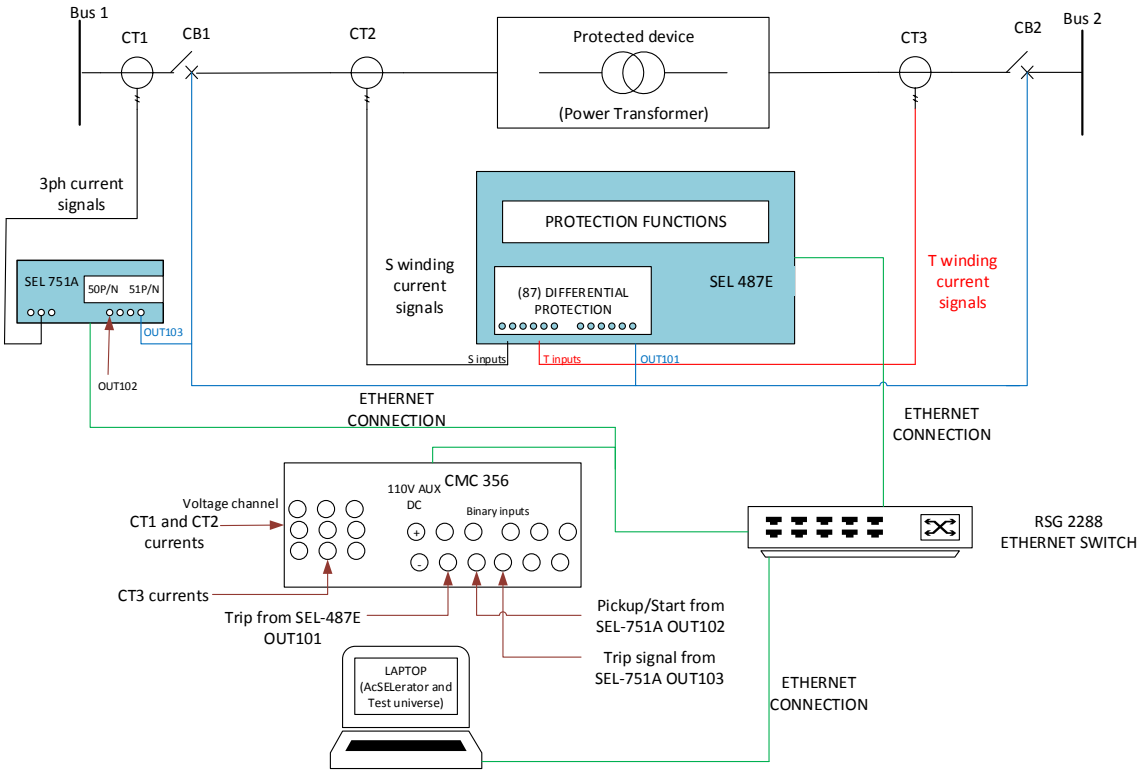


Figure 5.1: Transformer differential and overcurrent protection scheme test bench setup

The test bench setup provides the lab scale illustration of how the physical power transformer is protected using SEL-487E and SEL-751A as shown in Figure 5.1. The current signals (CT2 and CT3) on both (primary and secondary) sides of the power transformer are injected into the S and T windings current channels of the SEL-487E using the OMICRON test injection device. The CT1 current signals are injected into the SEL-751A current channels. Each end of the power transformer is connected to the switching device, circuit breakers (CB1 and CB2) respectively. The pickup and trip signal of the circuit breakers are represented using the binary signal connected to the output port (OUT101) of the SEL-487E and (OUT102 and OUT103) of the SEL-751A, which are mapped to the binary input 1 and 2 of the test injection device as shown in Figure 5.1. For internal events, the SEL-487E and SEL-751A IEDs send a

pickup and trip signals to the binary contact of the test injection device as shown in Figure 5.1.

5.2.1 Communication setting of the SEL-487E IED

AcSELerator Quickset is windows-based program supplied by Schweitzer Engineering Laboratories (SEL) to interact with SEL relays through a communications link. The program is used to create relay settings, upload them and retrieve them from any SEL relay connected to a computer via Ethernet or serial connection. AcSELerator Quickset is also used for the analysis of substation events logged by the relay, meter logs etc. through the Human Machine Interface (HMI).

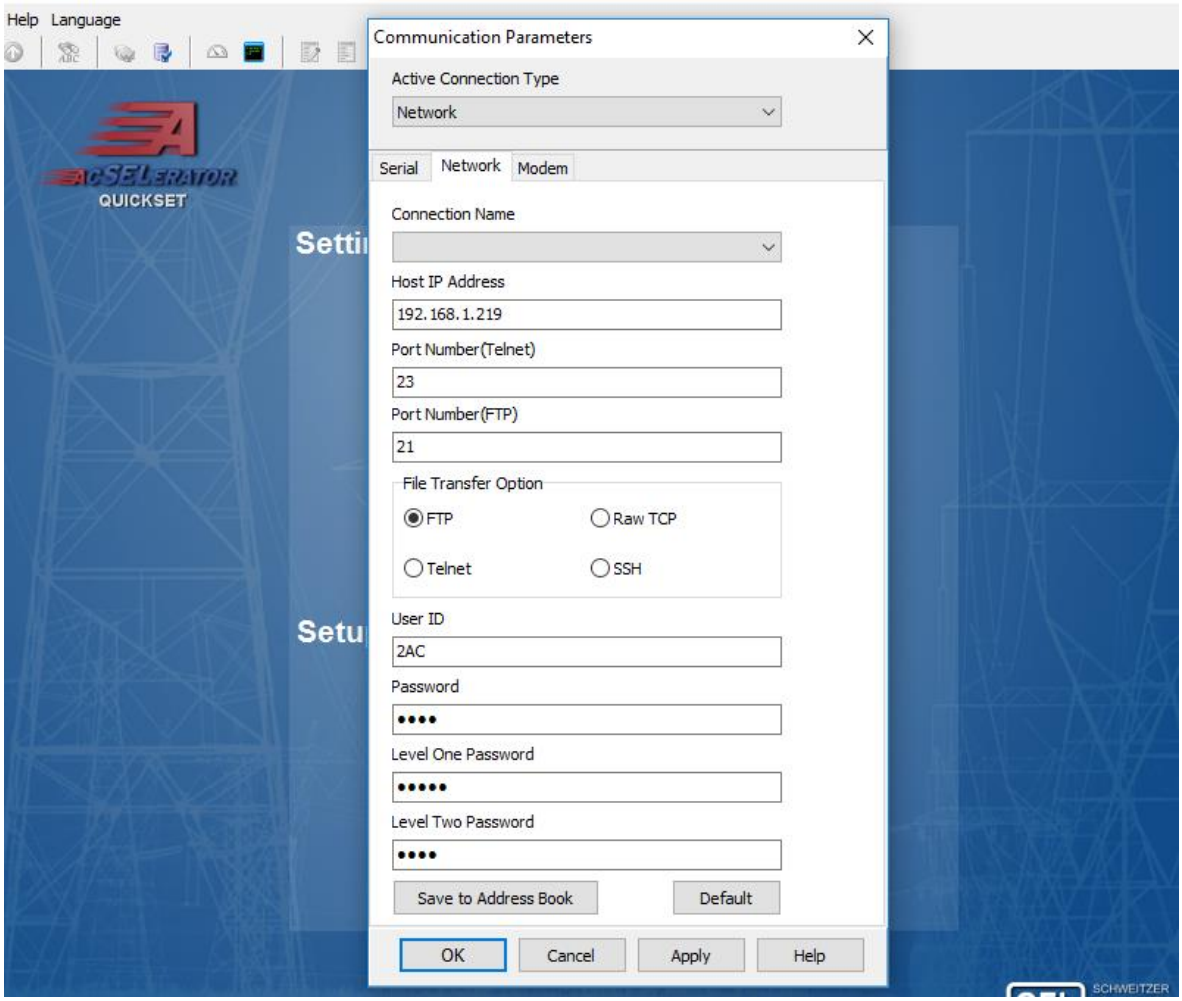


Figure 5.2: SEL-487E communication parameter setting on AcSELerator Quickset

The computer communication port must be configured correctly to establish the communication with the SEL-487E numerical relay as shown in Figure 5.2.

The IP address domain used to configure the computer's communications port should correspond to the IP address domain of the IED. The communication setting

for SEL-487E IED is given in Figure 5.2. Once a communications link has been successfully established, the user can read, edit and write settings on SEL-487E relay.

5.2.2 Transformer differential protection (SEL-487E IED) configuration setting using the AcSELerator Quickset software

This section describes the transformer and differential protection configuration settings using AcSELerator Quickset software. Table 5.1 provides the power transformer and differential protection parameters which includes the instrument transformer settings, differential characteristic settings and the harmonic restraint settings as given in Table 5.1

Table 5..1: Input data of the power transformer and differential protection settings

Parameter name	Parameter Value	Description
Frequency	50Hz	Nominal system frequency
Transformer data	100MVA	Rated power
	132kV	Rated voltage on the primary side of the transformer (it is used for the calculation of the transformation ratio of the transformer)
	33 kV	Rated voltage on the secondary side of the transformer (it is used for the calculation of the transformation ratio of the transformer)
	Yyn0	Vector group
CT data	400 A / 1A	CT ratio on the primary side of the transformer
	1600 A / 1A	CT ratio on the secondary side of the transformer
Differential characteristic settings	0.5 I_{ref}	Idiff>, pick-up value of the first stage differential element (I_{ref} is a reference current which can be obtained from the relay manual. In this case it is the rated current of the transformer)
	8 I_{ref}	Idiff>>, Second stage of the differential element (there is no stabilization above this value)
	0.35	Slope 1 of the differential characteristic
	0.75	Slope 2 of the differential characteristic
	4.0 I_{ref}	Bias current where the first slope ends, and the second slope begins.
Harmonic restraint settings	15 %	2nd harmonic restraint value (relative to the fundamental frequency differential current)
	35 %	4th and 5th harmonic restraint value (relative to the fundamental frequency differential current)

The general global settings of the main protection power transformer relay are shown in Figure 5.3 which includes station identifier as Station A, relay identifier as SEL-487E, nominal system frequency set to 50Hz and the system phase rotation as ABC with $120°$ phase shift.

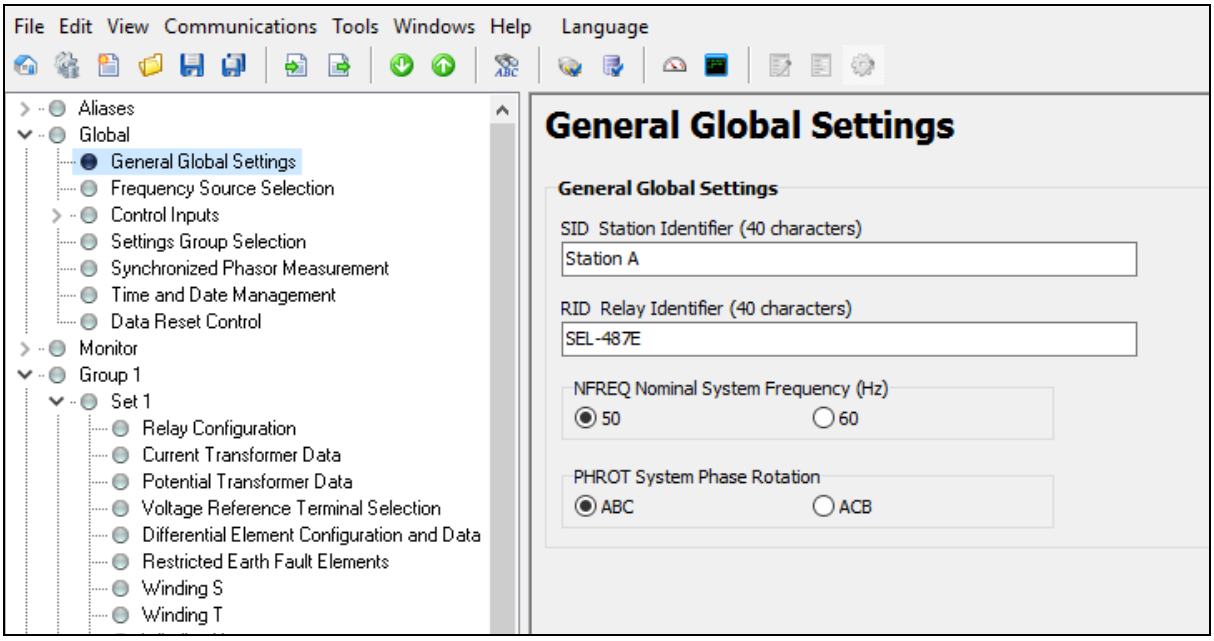


Figure 5.3: General global setting of SEL-487E IED

Table 5.2 provides CT ratio settings of the phase and neutral elements. As shown in Figure 5.4 CT ratio on S winding side (CTRS) is connected at S winding channel of the relay and is set to 400. CT ratio on T winding side (CTRT) is connected at the T winding channel of the relay and is set to 1600, and both CTs are connected in star.

Table 5.2: Current transformers ratio for S and T windings on SEL- 487E IED

Abbreviation (Relay Word Bit)	Description of the relay word bits	Value
CTRS	Current Transformer ratio for S winding	400
CTCONS	Current Transformer connection for S winding	Y
CTRT	Current Transformer ratio for T winding	1600
CTCONT	Current Transformer connection for T winding	Y

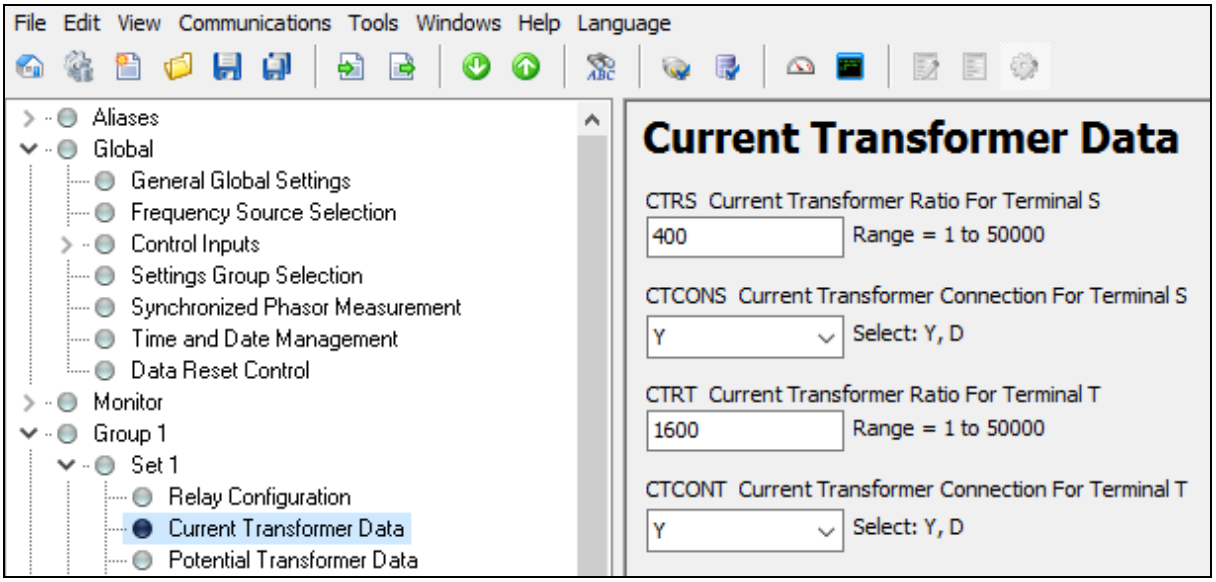


Figure 5.4: Current transformer setting on SEL-487E IED

The transformer differential element configuration setting is given in Table 5.3. Phase differential element pickup (O87P) is set to 0.5 p.u, slope 1 and slope 2 are set to 35% and 75% respectively as shown in Figure 5.5. Negative sequence protection pickup (87QP) is set to 0.3 p.u.

Table 5.3: Power transformer differential protection setting on SEL-487E IED

Abbreviation (Relay Word Bit)	Description of the relay word bits	Value
E87TS	Include S winding in the differential element for the following conditions	1
E87TT	Include T winding in the differential element for the following conditions	1
ICOM	Internal CT connection matrix compensation enable	Yes
TSCTC	Terminal S CT connection compensation	12
TTCTC	Terminal T CT connection compensation	12
MVA	Transformer maximum MVA rating (MVA)	100
VTERMS	Terminal S nominal line-to-line voltage (kV)	132
VTERMT	Terminal T nominal line-to-line voltage (kV)	33
O87P	Differential element operating current pickup (p.u.)	0.5
SLP1	Slope 1 setting (%)	35
SLP2	Slope 2 setting (%)	75
U87P	Unrestrained element current pickup (p.u.)	8
DIOPR	Incremental operate current pickup (p.u.)	1.20
DIRTR	Incremental restraint current pickup (p.u.)	1.20
E87HB	Enable Harmonic Blocking differential element	Yes

E87HR	Enable Harmonic Restraint differential element	Yes
PCT2	Second-Harmonic percentage (%)	15
PCT4	Fourth-Harmonic percentage (%)	35
PCT5	Fifth-Harmonic percentage (%)	35
87QP	Negative sequence differential element operating current (p.u.)	0.30
SLPQ1	Negative sequence differential slope (%)	25
87QD	Negative sequence differential element delay (cycles)	10

Figure 5.5 shows the configuration setting of SEL-487E IED

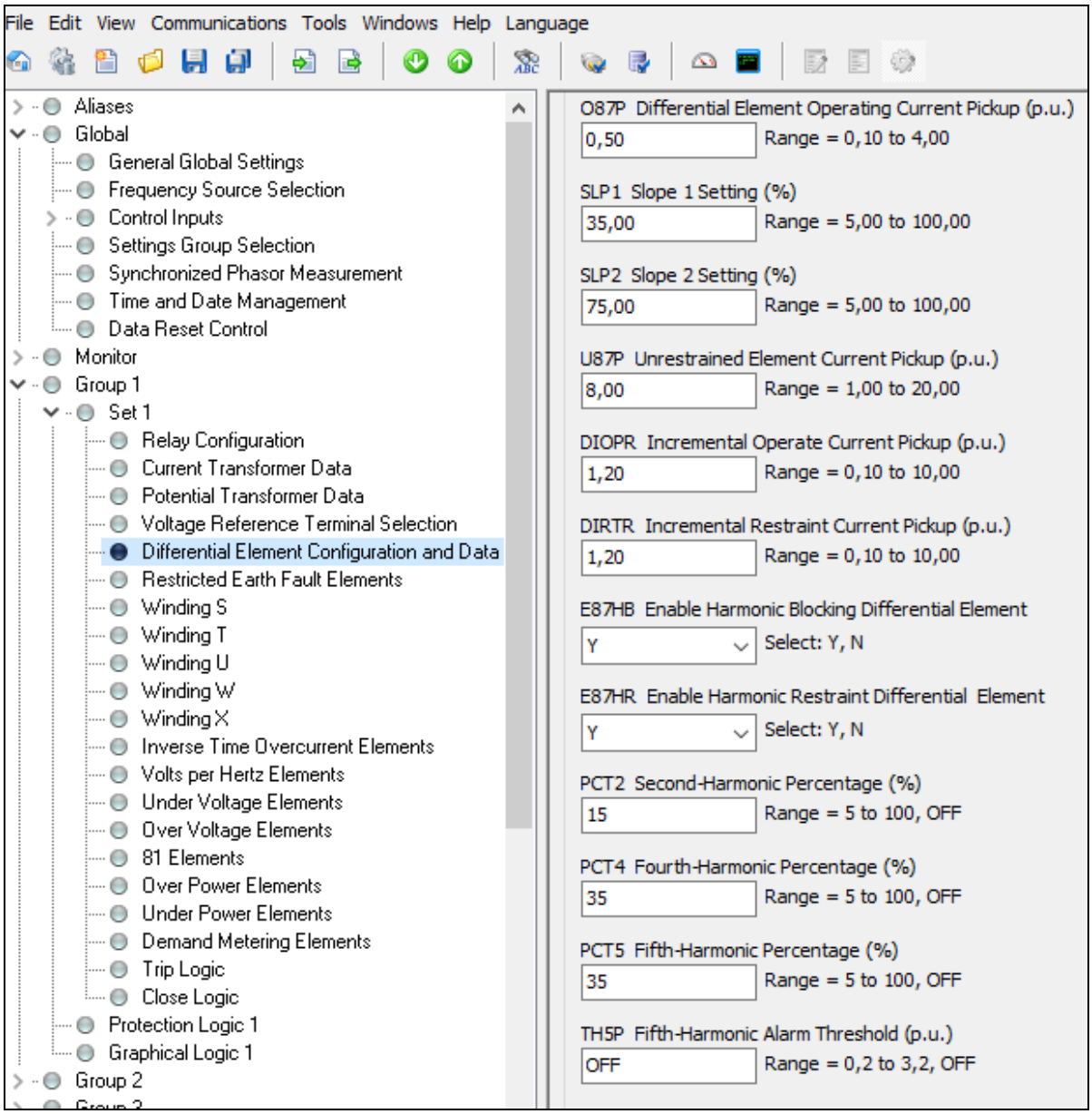


Figure 5.5: Differential element configuration setting in AcSELerator Quickset

Table 5.4 provides the Relay Word Bit used to implement the transformer differential protection scheme.

Table 5.4: Relay Word Bits of the transformer differential protection relay (SEL-487E IED)

Abbreviation Relay word bits	Description of the relay word bits
87ABK2 OR 87ABK4	2nd and 4th harmonic blocking asserted zone A
87ABK5	5th harmonic blocking asserted zone A
87AHB	Harmonic blocking differential element picked up A
87AHR	Harmonic restraint differential element picked up A
87BBK2 OR 87BK4	2nd and 4th harmonic blocking asserted zone B
87BBK5	5th harmonic blocking asserted zone B
87BHB	Harmonic blocking differential element picked up B
87BHR	Harmonic restraint differential element picked up B
87CBK2 OR 87CBK4	2nd and 4th harmonic blocking asserted zone C
87CBK5	5th harmonic blocking asserted zone C
87CHB	Harmonic blocking differential element picked up C
87CHR	Harmonic restraint differential element picked up C
87Q	Negative-Sequence differential element asserted (inter-turn fault detected)
87QB	Block negative and zero-sequence directional elements
87R	Restrained differential element operated
87RA	Restrained differential element operated phase A
87RB	Restrained differential element operated phase B
87RC	Restrained differential element operated phase C
87U	Unrestrained element operation
87UA	Unrestrained element asserted zone A
87UB	Unrestrained element asserted zone B
87UC	Unrestrained element asserted zone C
87XBK2	Harmonic cross-blocking picked up
CON	Fault outside of transformer differential zone
CONA	External fault detected zone A
CONB	External fault detected zone B
CONC	External fault detected zone C
E87TS	Terminal S currents included in differential zone
E87TT	Terminal T currents included in differential zone
ER	Event report triggered
FAULT	Fault detected
IFLTA	Fault inside transformer differential zone A

IFLTB	Fault inside transformer differential zone B
IFLTC	Fault inside transformer differential zone C
OUT101-OUT108	Output 101-108 asserted
PSV01-PSV08	Protection SELogic Variable 01-08 asserted
TRIP	Transformer or Terminal Trip signal asserted
TRIPS	Terminal S trip output asserted
TRIPT	Terminal T trip output asserted
TRPXFMR	Transformer trip output asserted
TRS	Terminal S trip equation asserted
TRT	Terminal T trip equation asserted
TRXFMR	Transformer trip equation asserted

Figure 5.6 describes the relay trip logic used in this research project. The Transformer Trip timer starts when SELogic control equation TRXFMR asserts for one processing interval, and this assertion is caused by Relay Word Bit 87U and 87R (SEL-487E Instruction manual, 2012). The assertion of this equation immediately asserts output TRPXFMR. Output TRPXFMR remains asserted for the Minimum Trip Duration timer (TDURD) setting regardless of the status of TRXFMR input.

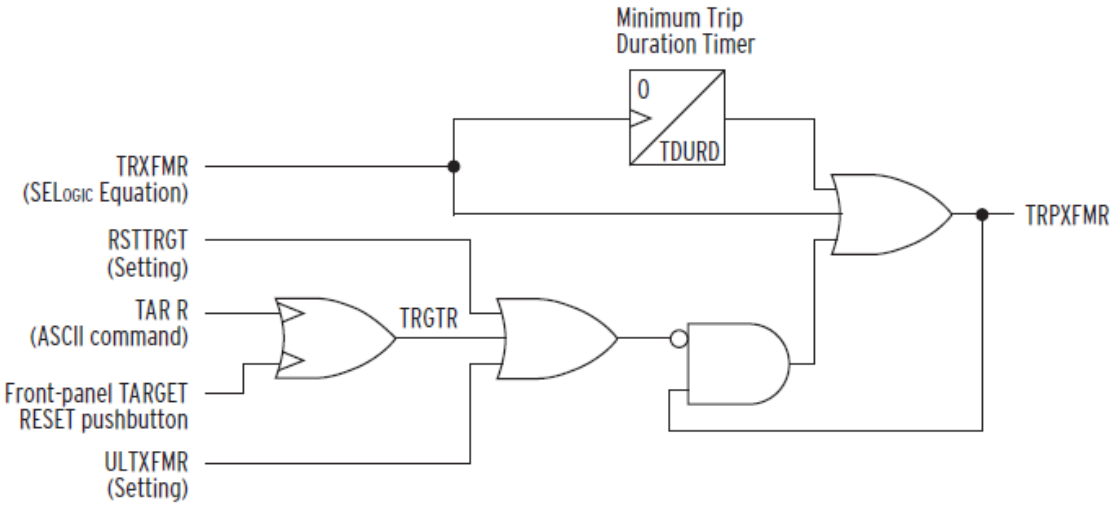


Figure 5.6: Transformer trip logic (SEL-487E Instruction manual, 2012)

SELogic control equation ER is programmed to trigger high-resolution raw data oscillography and standard event reports for conditions other than TRIP conditions, in this case, Harmonic Blocking elements (87AHB, 87BHB and 8787CHB). When ER asserts, the SEL-487E begins recording data if the relay is not already capturing data initiated by another trigger. Internal faults (IFLTA, IFLTB and IFLTC) and external fault (CON) are the conditions for asserting FAULT bit. However, the relay should

only trip for internal faults, and Relay Word bit CON changes the operating mode of the relay to high-security mode, primarily to avoid mis-operation resulting from CT saturation for external faults.

Table 5.5: SEL-487E Trip logic conditions for the differential protection of power transformer

Abbreviation	Description of the relay word bits	Relay word bit
TRXFMR	Trip conditions for transformer terminals	87U OR 87R
ULTXFMR	Unlatch trip conditions for transformer terminals	TRGTR
TRS	Trip condition for terminal S	0
ULTRS	Unlatch trip conditions for terminal S	TRGTR
TRT	Trip condition for terminal T	0
ULTRT	Unlatch trip conditions for terminal T	TRGTR
TDURD	Minimum trip duration (cycles)	5.000
ER	Conditions for triggering event reports	87AHB OR 87BHB OR 87CHB
FAULT	Conditions for asserting FAULT bit	IFLTA OR IFLTB OR IFLTC OR CON

5.2.3 OMICRON test universe configuration setting for power transformer differential protection scheme

Test Universe Omicron's software provides a variety of function-oriented test modules that can be used to test protective devices. For single tests, a single test module can be run standalone; however, if a series of tests need to be conducted together, the necessary test modules can be grouped together into an OMICRON control centre documents. The first step in configuring an OMICRON control centre test document is to define the test object parameters. The test object being the protective device being tested. A hardware configuration thereafter follows and lastly the test modules to be incorporated in the OMICRON test document. This section provides the Test Universe engineering configuration setting for differential protection scheme.

5.2.3.1 Test object

The settings of the SEL-487E relay to be tested must be defined in the test object. In order to do engineering configuration Test Object has to be opened by double-clicking the Test Object in the OCC file as shown in Figure 5.7.

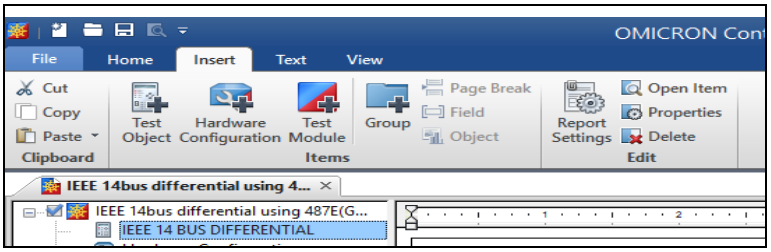


Figure 5.7: Defining test object of SEL-487E IED in the Test Universe environment

General relay settings which include relay type, relay ID, substation details are defined in the RIO function Device. The CT data is not defined in the RIO function. It is defined in the RIO function Differential.

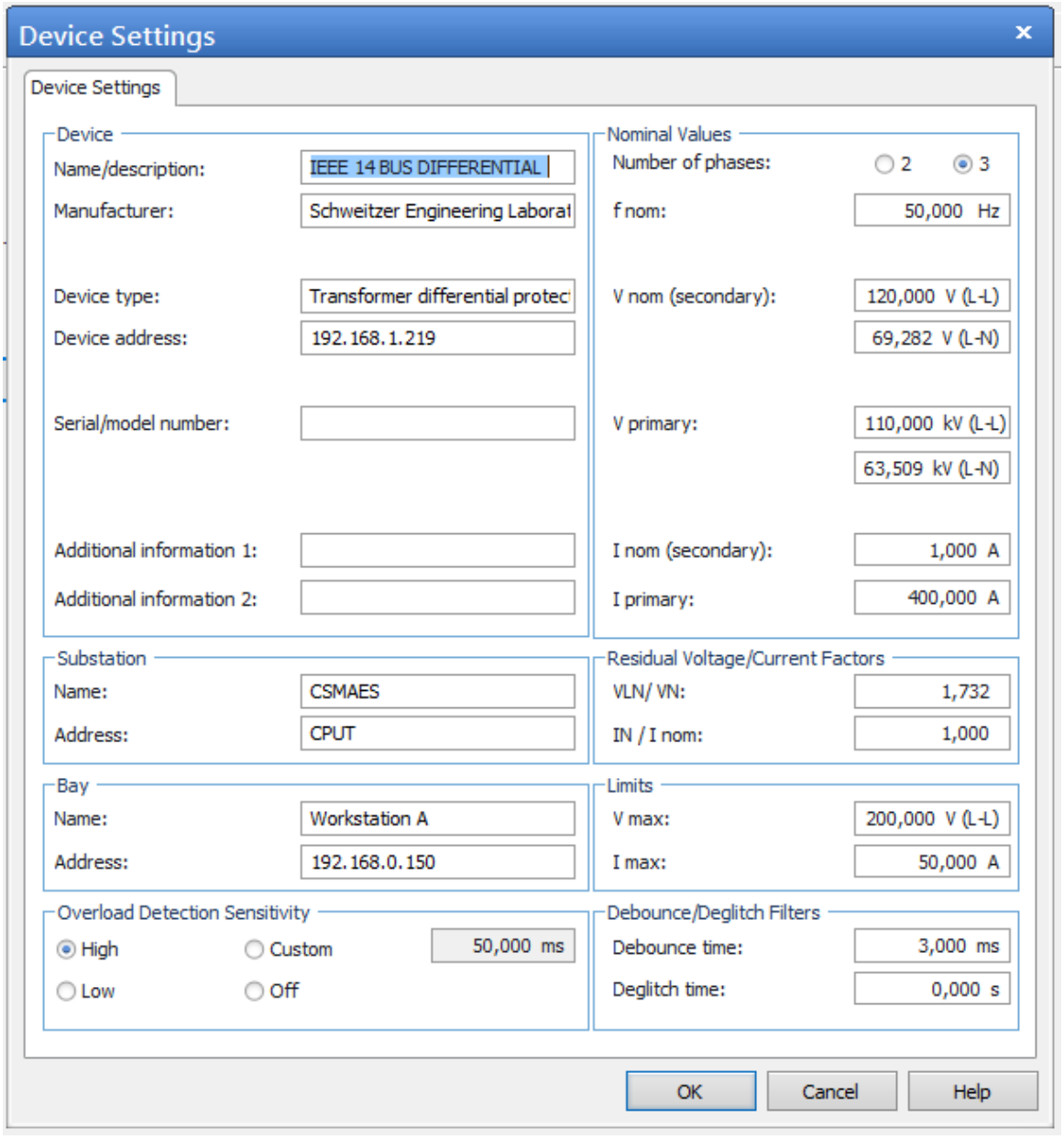


Figure 5.8: SEL-487E device settings in Test Universe software

The device setting given in Figure 5.8 provides the detailed information of the protection device and system nominal frequency, primary and secondary voltage and currents, residual factors and debounce time.

5.2.3.2 Advanced differential configuration setting

More specific data concerning the transformer differential protection relay can be defined in the RIO (Relay Interface by Omicron) Differential function. The advanced differential configuration setting section provides the transformer data, CT data, general relay settings, operating characteristic and harmonic restraint definition.

i. Protected object configuration setting

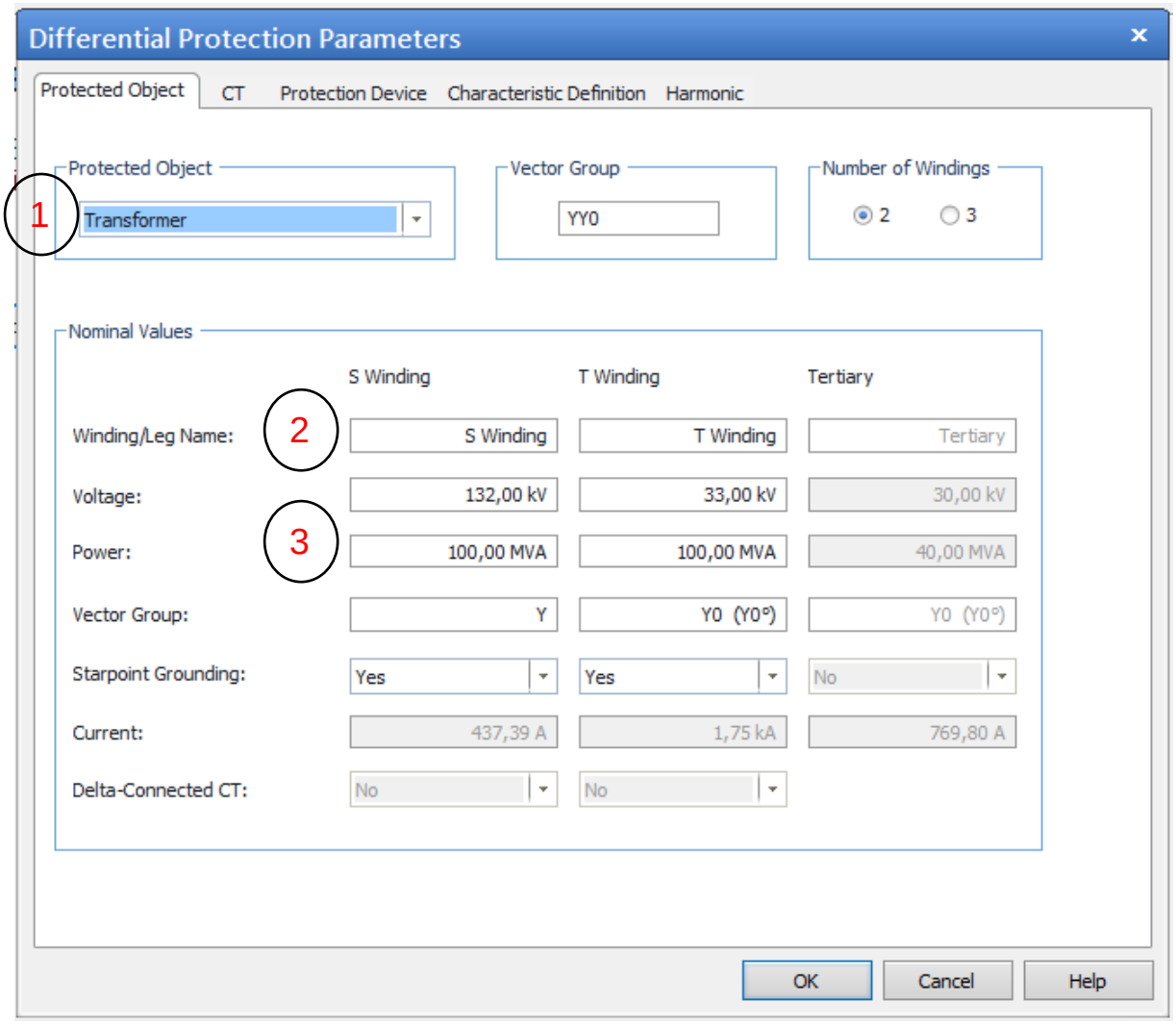


Figure 5.9: Protected Object (SEL-487E IED) configuration setting

The differential protection setting of the protected object (SEL-487E transformer protection IED) is shown in Figure 5.9. The encircled numbers are used to describe the protected object parameter settings as given below.

1) The protected object is selected as a transformer

2) The windings of the transformer are entered in the winding/leg name

3) The transformer data are defined for each winding which includes the nominal voltage and the nominal power and the vector group of the transformer. For each Y winding the star-point grounding can be defined. This setting has an influence on the zero-sequence currents during single-phase faults.

ii. Current Transformer data for the transformer differential protection scheme

The data of the current transformer for the differential protection scheme is shown in Figure 5.10.

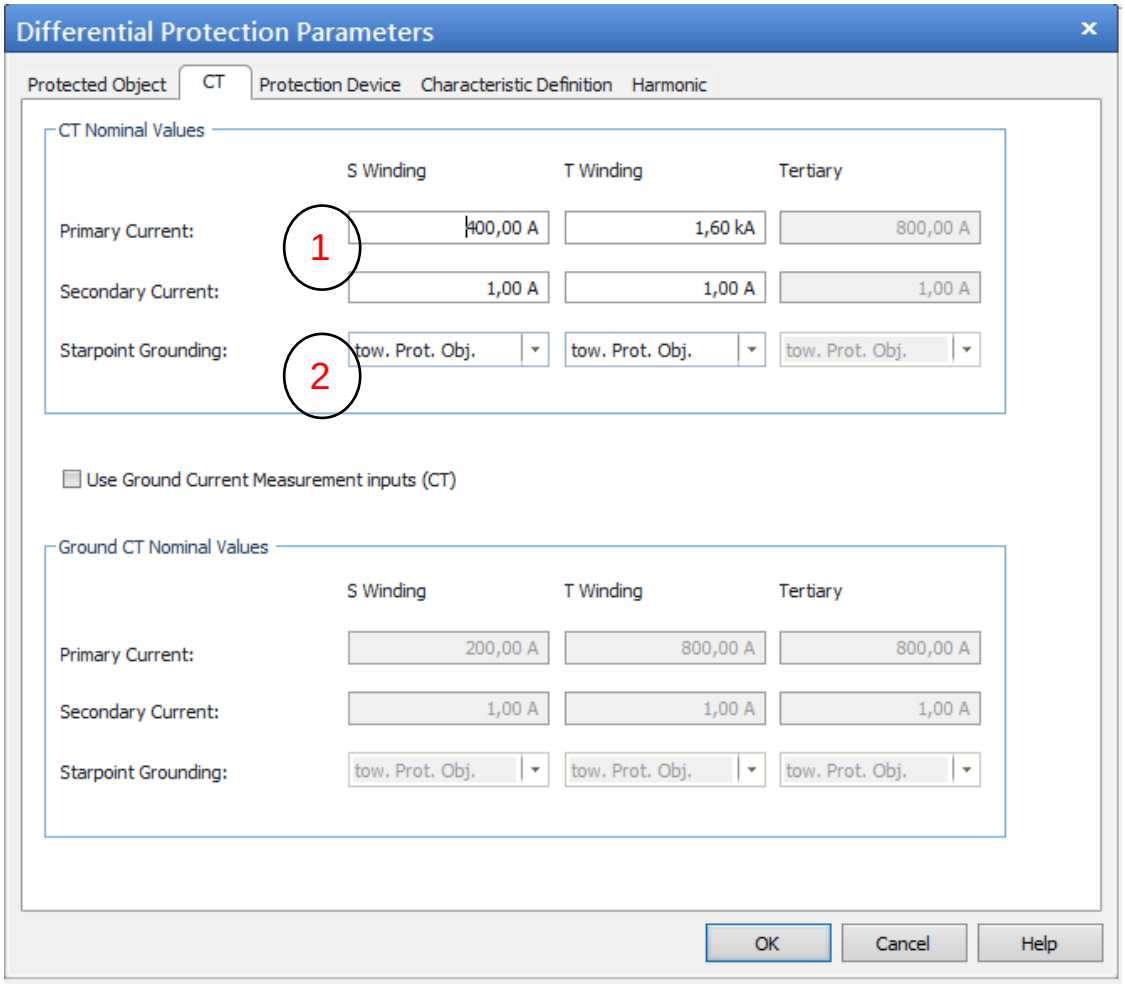


Figure 5.10: Current Transformer configuration settings in Test Universe

1. The nominal currents of the CTs on S and T windings are provided

2. The CT star-point grounding is connected according to the wiring of the CTs is selected

iii. Protection device settings

The settings of the protection device are shown in Figure 5.11, which provides the differential current and time settings for stage 1 and stage 2 of the differential element along with the basis current setting. The encircled numbers in Figure 5.11 provides the detailed engineering configuration setting of the protection device as follow (OMICRON Instruction manual, 2015):

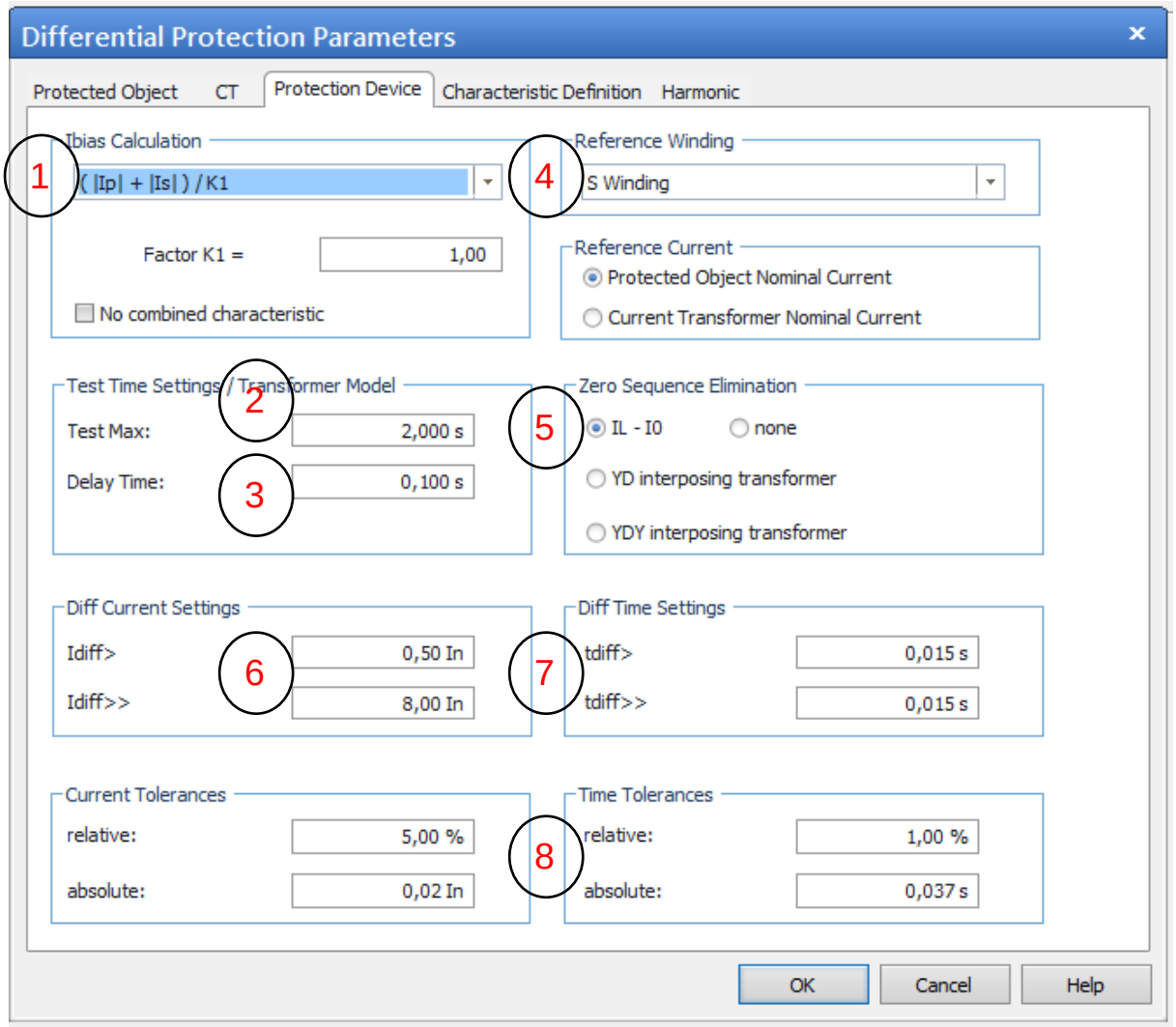


Figure 5.11: Protection device configuration settings in Test Universe

1. The calculation method of the bias current is selected. This method depends on the relay type. No combined characteristic needs to be selected if the relay uses only the phase with the highest current magnitude for the differential and bias current calculation. For SEL 487E relay calculates these currents in all three phases simultaneously.

2. Test Max (2s) is the test shot time if the relay does not trip. It should be set higher than the expected relay trip time but shorter than possible trip times of

additional protection functions (for example, overcurrent protection). Since a differential relay typically trips instantaneously so test time can be set quite low as 2 seconds to speed up the test.

3. The Delay Time (0.1s) defines the pause between two test shots, and during this time no currents will be generated. Therefore, this time may be increased to prevent overheating of electromechanical relays.

4. As all differential current settings are defined relative to the nominal current and must be defined. The nominal current is calculated according to the winding reference selection.

5. The Zero Sequence Elimination has an influence on the currents during phase-to-ground faults. Therefore, IL - I0 has been selected since SEL-487E relay uses zero sequence elimination.

6. The setting Idiff> (0.5In) defines the pick-up of the differential protection function. If the differential current does not exceed threshold value, the relay will not trip. Idiff>> (8In) defines the high differential current element. If the differential current exceeds this value, the relay will always trip.

7. The time settings tdiff> (0.015s) and tdiff>> (0.015s) define the trip times of the differential elements.

8. The current and time tolerances are obtained from the SEL 487E instruction manual.

iv. Differential characteristics definition

The line segments of the differential characteristic are set by defining their corner points. The necessary steps to define an operating differential characteristic are shown in Figure 5.12:

Step 1: Equations for the line segments including fixed lines are set up. Unknown parameters are replaced by variables like a, b, c:

(I): $I_{diff} = 2.I_{bias}$ Fixed line from (0/0) to IRS0

(II): $I_{diff} = 0.35.I_{bias}$+ a Segment 1 from IRS0 to IRS1

(III): $I_{diff} = 0.75.I_{bias}$+ b Segment 2 from IRS1 and IRS2

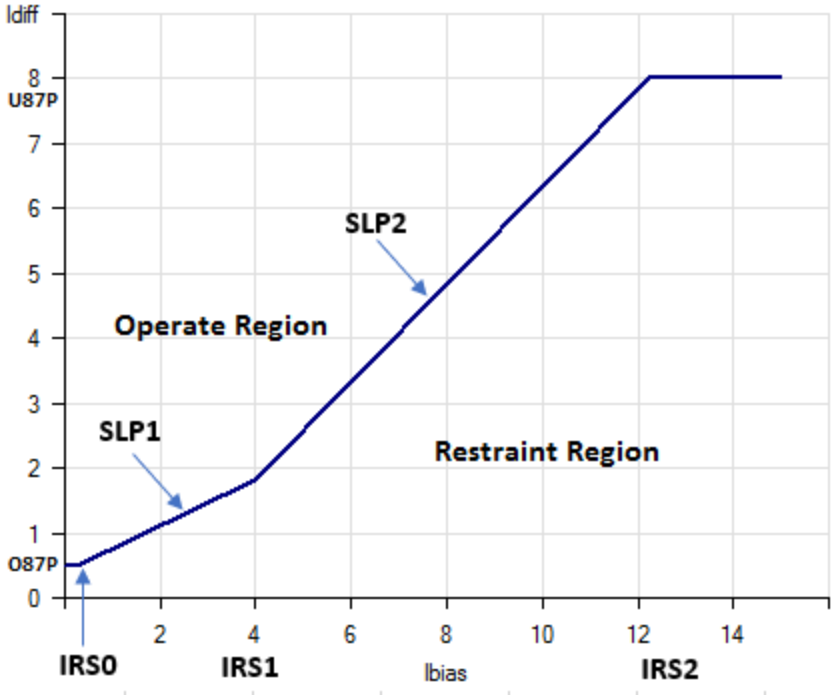


Figure 5.12: SEL-487E differential operating characteristic with corner points

Step 2: The corner points of the differential characteristic and the unknown parameters are calculated:

- IRS0: I_{diff}> is used in Equation (I) to get I_{bias} of IRS0 where Idiff = 0.5In

  0.5 = $2.I_{bias}$

  I_{bias} = 0.25

IRS0 = (I_{bias} / I_{diff}) = (0.25 / 0.5)

- a: To use IRS0 in Equation (II) to get the variable a.

  0.5 = 0.35x0.25 + a

  a = 0.5 – 0.0875

  a = 0.4125

- IRS1: I_{diff} of this point needs to be found

  I_{diff} = 0.35x4 + 0.4125= 1.8125

  IRS1 = (4 / 1.8125)

- b: We use IRS1 in Equation (III) to get variable b

  1.8125 = 0.75x4 + b

b = -1.1875

- IRS2: we use I_{diff}>> in Equation (III) to get I_{bias} of IRS2

  8 = $0.75.I_{bias}$ – 1.1875

  9.1875 = $0.75.I_{bias}$

  I_{bias} = 12.25

  IRS2 = (12.25 / 8)

Step 3: The above calculated points are the start and end points of the line segments IRS0, IRS1 and IRS2 respectively as shown in Figure 5.12.

Figure 5.13 provides the differential slope characteristic settings in the test universe software environment.

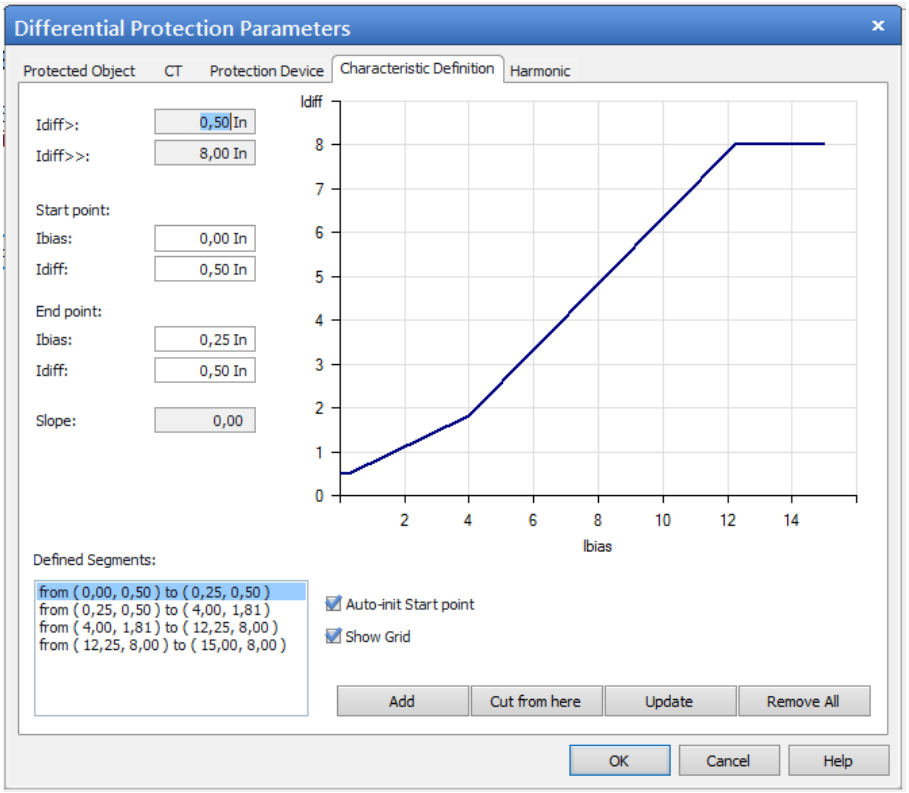


Figure 5.13: Differential slope characteristic setting in test universe software

v. Harmonic setting

The numbers from 1 to 4 circled in Figures 5.14 and 5.15 describe the harmonic tolerances, harmonic characteristics and line segments. The detailed descriptions of the encircled numbers are given below:

1. The number of the harmonic that blocks the differential protection has been selected, in this case, is the second and fifth harmonic at 15% and 35% respectively of the differential currents.

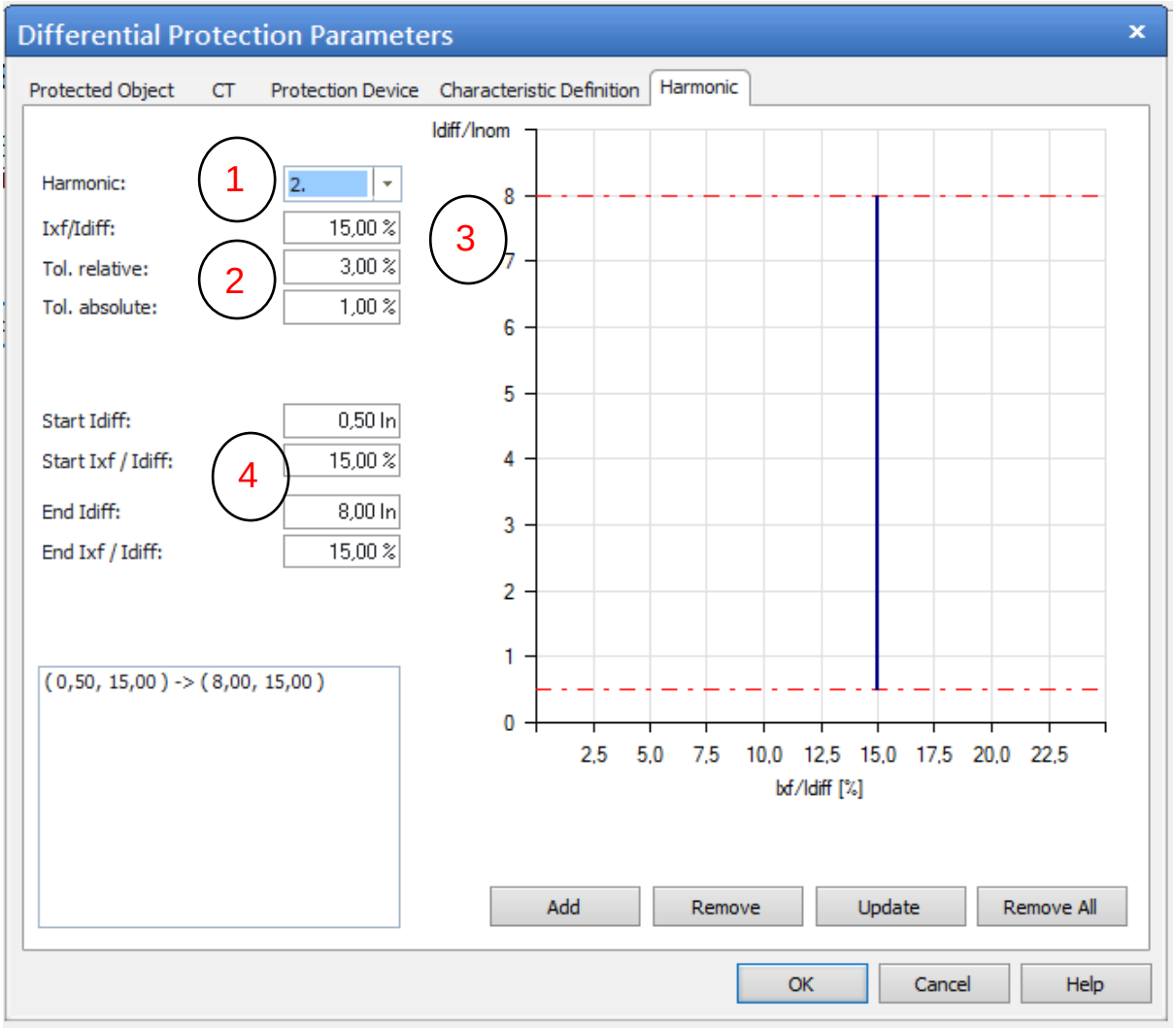


Figure 5.14: Second harmonic setting in Test Universe

2. The relative and absolute tolerances are entered as 3% and 1% respectively as specified in the SEL-487E instruction manual

3. The harmonic blocking threshold set to eight times the nominal current (8.00In). The above steps 1 to 3 is repeated to perform the fifth harmonic configuration setting.

4. The second and fifth harmonic characteristics can be created by defining line segments with start and end points as shown in Figures 5.14 and 5.15 respectively.

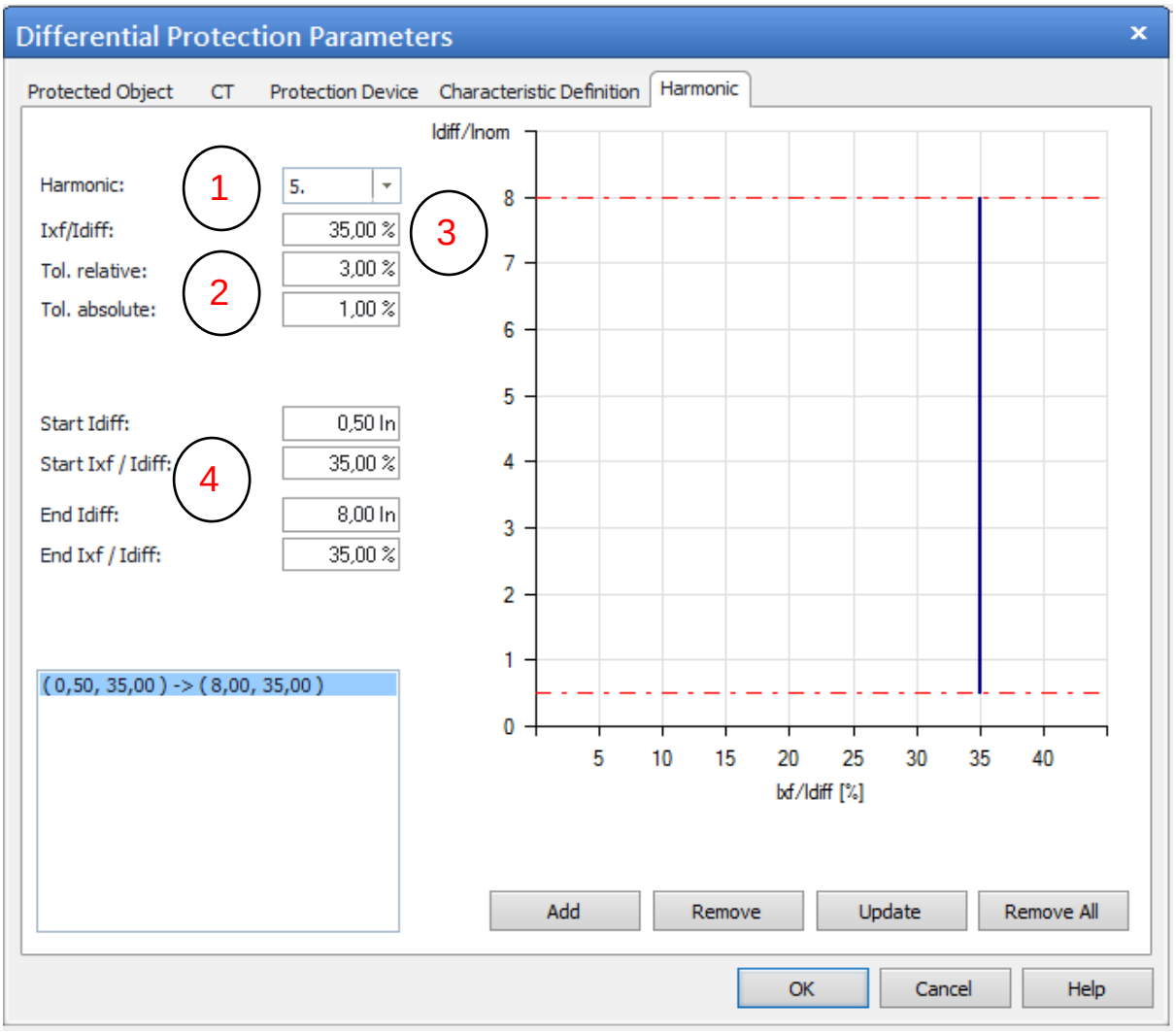


Figure 5.15: Fifth harmonic setting in test universe software

5.2.3.3 Global hardware configuration setting to test the transformer differential protection scheme

The global hardware configuration specifies the general input/output configuration of the CMC test set. It is valid for all subsequent test modules and, therefore, it has to defined according to the relay's connections.

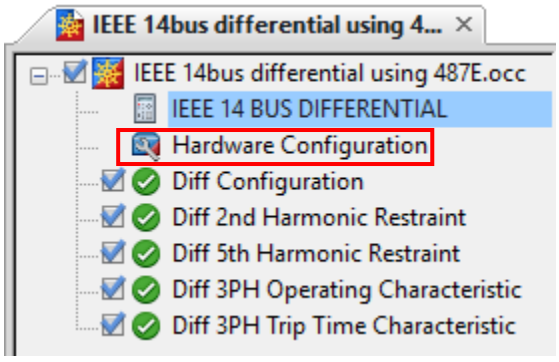


Figure 5.16: Hardware configuration setting for transformer differential protection scheme

It can be defined by double-clicking the hardware configuration entry in the OCC as shown in Figure 5.16.

Figure 5.17 shows the output configuration of the current differential protection scheme.

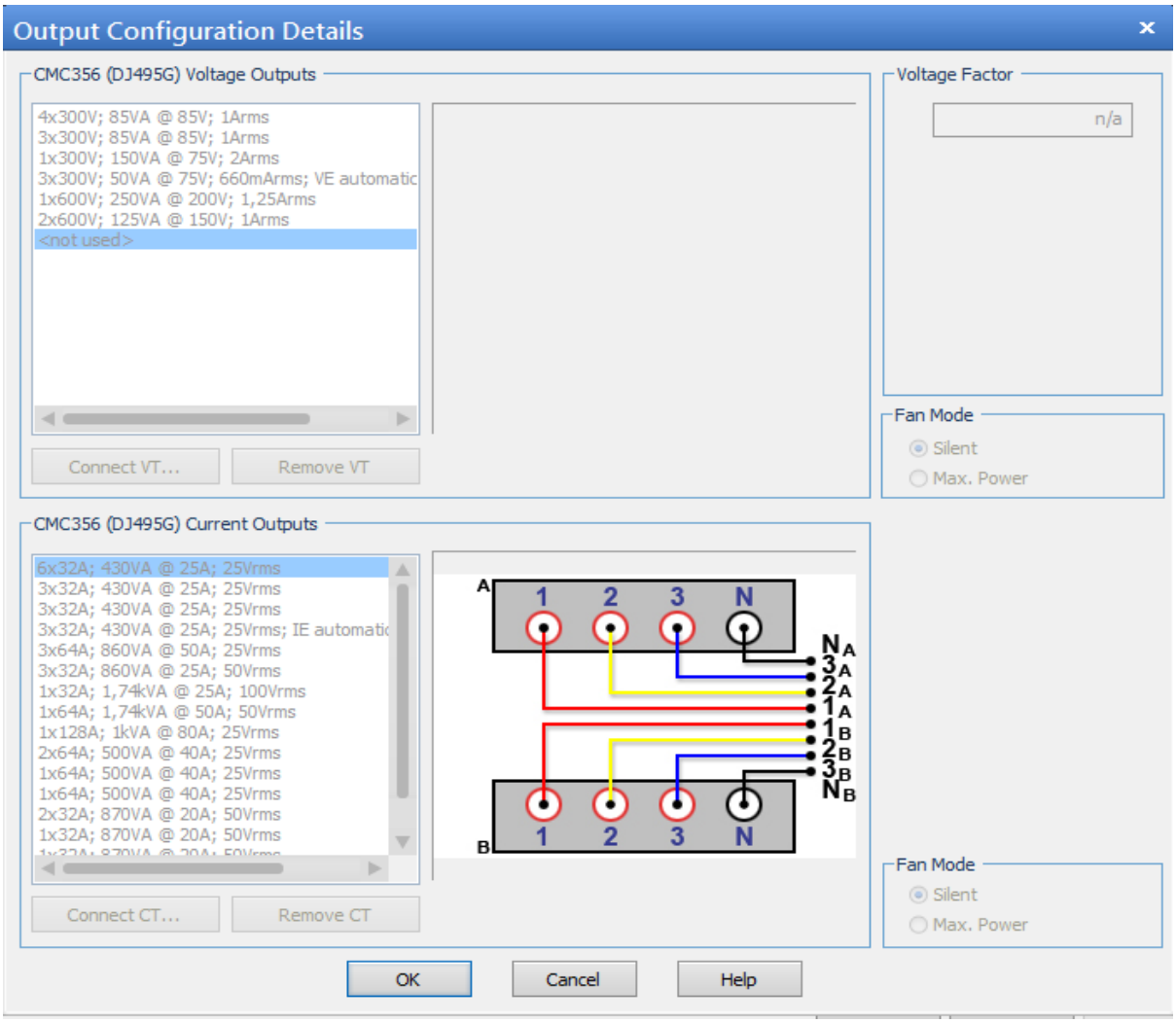


Figure 5.17: Current differential output configuration setting

The analogue outputs, binary inputs and outputs can be activated individually in the local hardware configuration of the specific test module. The binary outputs, analogue inputs, DC analogue inputs and time source, are not used in this test module. Analogue Outputs and Binary/Analog Inputs are shown in Figures 5.18 and 5.19 respectively. The transformer current differential scheme needs two set of current inputs which are provided by the current channel A and current channel B of the Omicron test. The trip signal is the output of the transformer current differential relay which is mapped to the binary input 1 of the CMC test set as shown in Figure 5.19

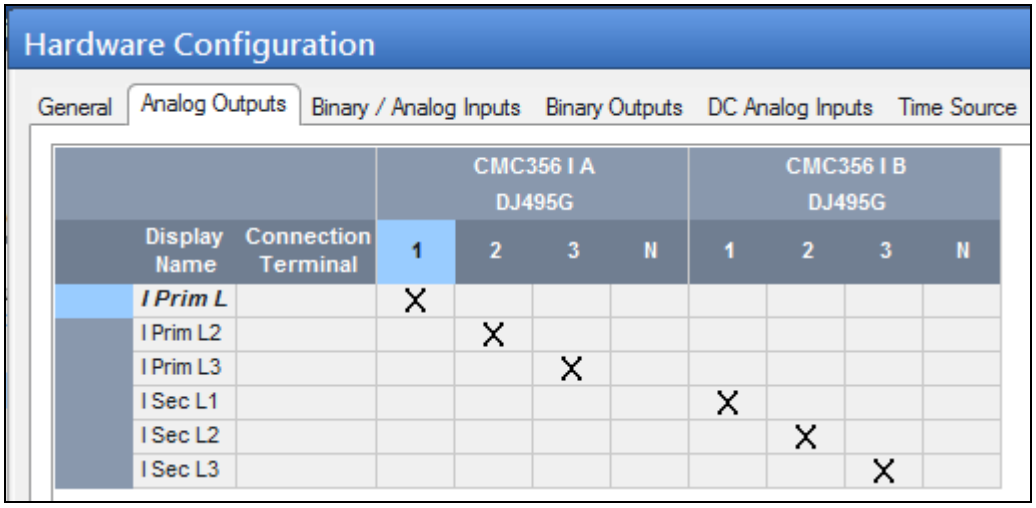


Figure 5.18: Two sets of the differential relay current signals mapped to the analogue outputs of the CMC test set

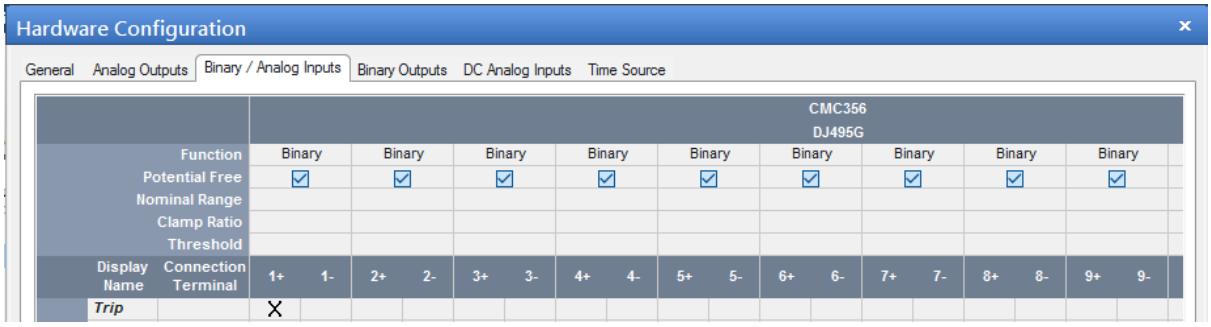


Figure 5.19: Trip signal of the differential relay mapped to a binary input of the CMC test set

5.2.4 Transformer current differential protection testing

Advance Differential test modules are used to test the three-phase current differential protection functions. These test modules are (OMICRON Instruction Manual, 2015):

- The Differential Configuration module: for testing the differential protection which consists of the wiring and the relay parameters such as transformer data, CT data and zero sequence elimination.
- The Differential Operating Characteristic module: for testing the operating characteristic of the differential protection.
- The Differential Trip Time Characteristic module: for testing the trip times of the differential protection.
- The Differential Harmonic Restraint module: for testing the blocking of the differential trip due to current harmonics

5.2.4.1 Differential Configuration Test module

Differential protection relays are usually set to be very sensitive. Therefore, even small differential currents can lead to a trip. If the wiring is incorrect or if parameters such as the nominal voltages, the zero-sequence elimination, the CT ratios or the CT star-point directions are not set correctly, currents flowing through the protected zone may lead to an unwanted operation (OMICRON Instruction Manual, 2015).

The differential configuration test module simulates external faults in which, the fault current flows through the protected zone. During the external faults, the differential relay must not trip, and it confirms that the wiring and the relay setting are correct.

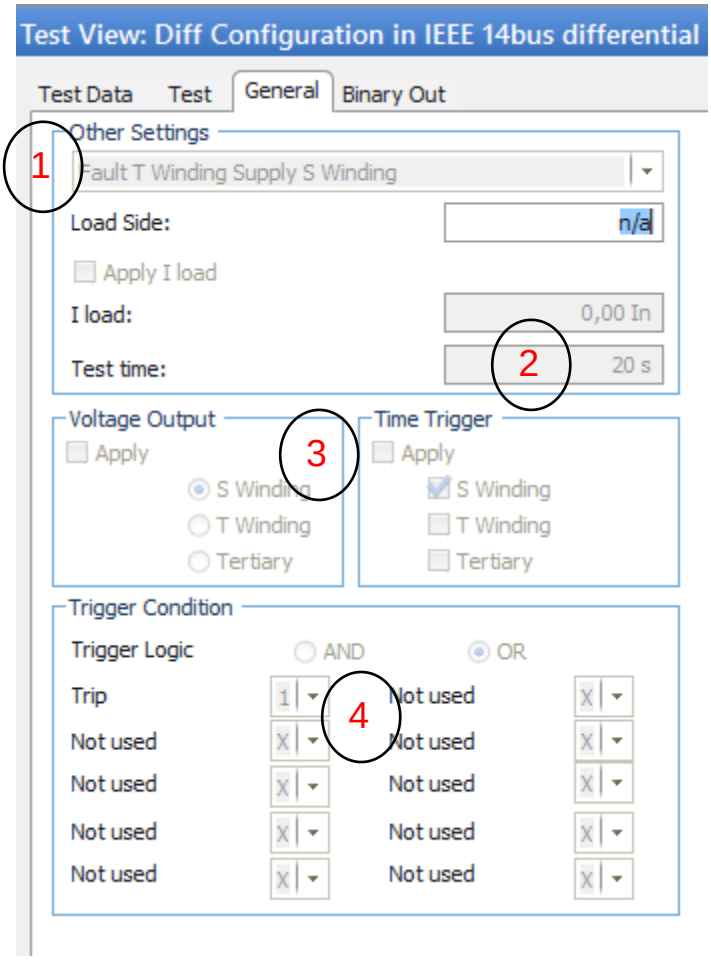


Figure 5.20: General differential configuration setting in Test Universe

General settings of the differential configuration test module are defined as shown in Figure 5.20. The numbers circled from 1 to 4 describe the differential configuration setting as follow:

1. This defines on which side of the transformer the fault and the source should be located, in this case, the fault on the T winding side and source on S winding side of the transformer

2. The test time of 20s should be set long enough to allow the measured currents from the relay to be read.

3. The voltage output and time trigger settings are defined if the CMC should generate voltages and whether the test should be time synchronised via GPS or IRIG-B. In this case, neither of these settings are necessary.

4. The trigger Logic has to be defined according to the relay configuration, in this case, the binary input 1 is mapped to the trip logic of the SEL-487E output port 101.

It is also important to note that if the relay uses multiple trip contacts, they should be linked with OR gate trigger logic as shown in Figure 5.20. This way the test can be assessed as failed if any of the trip contacts are triggered.

The Test Data settings are given in Figure 5.21; the following settings are defined as follows:

1. The test current 1A is defined, and it is relative to the nominal current on the fault side.
2. The new test point appears in the test point list
3. The fault type is defined. It is also important to note that only one fault type can be set per test module. More test modules can be added to the OCC file if multiple fault types are to be tested. In this case, three-phase fault (L1-L2-L3) is selected in the configuration setting.
4. The current outputs of the CMC are shown in the single line view for the protected test object.

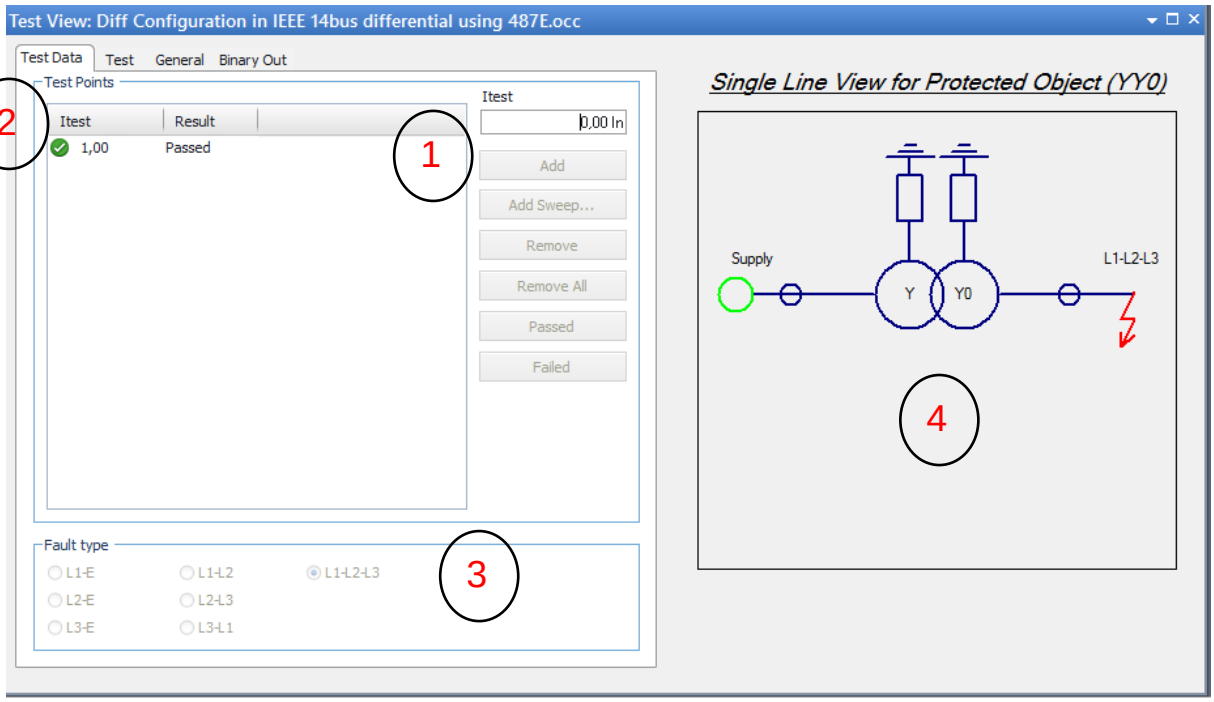


Figure 5.21*:* Test data parameters

5.2.4.2 Operating characteristic test

The operating characteristic of the differential relay is defined in this test. Tests points of the differential relay operating characteristic is shown in Figure 5.22.

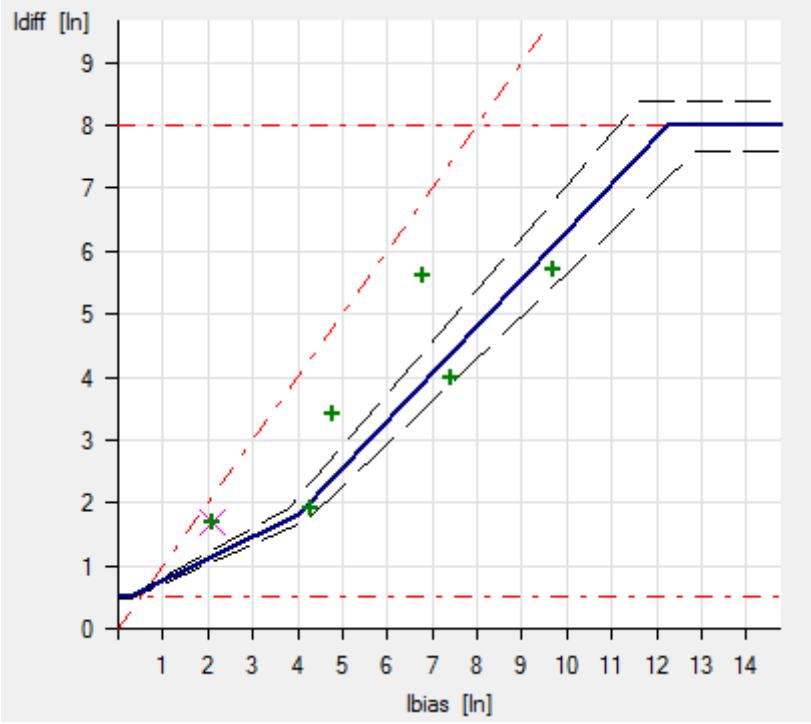


Figure 5.22: Differential relay operating characteristics curve

The currents corresponding to the test points depicted in Figure 5.22 are given in Table 5.6, and the simulation results of the test set are given in Table 5.7

Table 5.6: Currents injected into the differential relay (SEL-487E)

Shot	1	2	3	4	5	6
Idiff	1.70 In	1.90 In	3.40 In	5.60 In	4.00 In	5.70 In
Ibias	2.10 In	4.30 In	4.80 In	6.80 In	7.40 In	9.70 In
IL1 (S)	2.078 A -180.00°	3.390 A -180.00°	4.483 A -180.00°	6.779 A -180.00°	6.233 A -180.00°	8.420 A -180.00°
IL2 (S)	2.078 A 60.00°	3.390 A -60.00°	4.483 A -60.00°	6.779 A -60.00°	6.233 A -60.00°	8.420 A -60.00°
IL3 (S)	2.078 A -60.00°	3.390 A -60.00°	4.483 A -60.00°	6.779 A -60.00°	6.233 A -60.00°	8.420 A -60.00°
IL1 (T)	0.219 A 0.000°	1.312 A 0.000°	0.765 A 0.000°	0.656 A 0.000°	1.859 A 0.000°	2.187 A 0.000°
IL2 (T)	0.219 A -120.00°	1.312 A -120.00°	0.765 A -120.00°	0.656 A -120.00°	1.859 A -120.00°	2.187 A -120.00°
IL3 (T)	0.219 A 120.00°	1.312 A 120.00°	0.765 A 120.00°	0.656 A 120.00°	1.859 A 120.00°	2.187 A 120.00°

Table 5.7: Differential relay operating test results

Idiff	Ibias	Nominal Trip Time	Actual Trip Time	Assessment
1.90 In	4.30 In	N/T	N/T	Passed
4.00 In	7.40 In	N/T	N/T	Passed
5.70 In	9.70 In	N/T	N/T	Passed
1.70 In	9.20 In	0.0140 s	0.0464 s	Passed
3.40 In	4.80 In	0.0140 s	0.0475 s	Passed
5.60 In	6.80 In	0.0140 s	0.0480 s	Passed

NOTE: N/T means the differential relay did not trip.

The test shots placed above the operating characteristic, the relay tripped. Test shots placed below the restraining characteristic of the relay did not trip.

5.2.4.3 Second Harmonic Blocking test module

During transformer energisation the magnetic core saturates. This saturation causes high power losses which lead to high currents being drawn into the transformer without a corresponding current leaving the transformer. The relay can interpret

these high currents as differential currents and produce a trip signal. The harmonic blocking case study aims to test the differential relay ability to identify inrush currents and restraint itself from tripping. Operational philosophy of the harmonic blocking scheme is such that, if the percentage of the second and fifth harmonic current exceeds the setting value, the relay can block/restrain itself from tripping as shown in Figure 5.23.

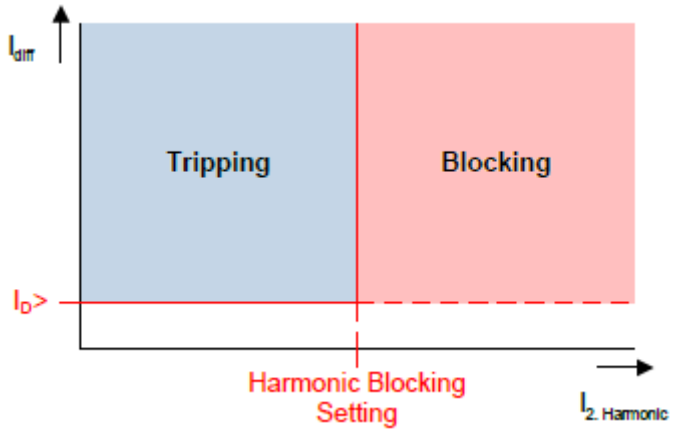


Figure 5.23: Harmonic blocking/tripping characteristic curve

There is a high harmonic content in the inrush currents; however, the fault currents have less harmonic contents that is less than 15%. Therefore, the way to test the inrush current condition is by generating differential currents with harmonic content above 15%.

The SEL-487E is configured to block all the differential currents with a harmonic percentage of 15% or more. The results obtained from the harmonic blocking test are given in Table 5.8.

Table 5.8: Second harmonic blocking test results

Idiff	Ixf/Idiff	Angle	Trip	Assessment
1.10 I/In	14.90%	-120.0°	No	Passed
2.70 I/In	14.90%	-120.0°	No	Passed
4.20 I/In	14.90%	-120.0°	No	Passed
5.80 I/In	15.00%	-120.0°	No	Passed
7.30 I/In	15.00%	-120.0°	No	Passed

The results revealed that the relay was able to restrain itself from tripping when differential currents in the range of 14.9% - 15% of injected harmonic currents. The differential relay has a tolerance band of ±1%, and for that reason, it could restrain

itself from tripping even when the percentage of harmonic currents is 14.9%. The second harmonic restraint for 15% differential current is shown in Figure 5.24.

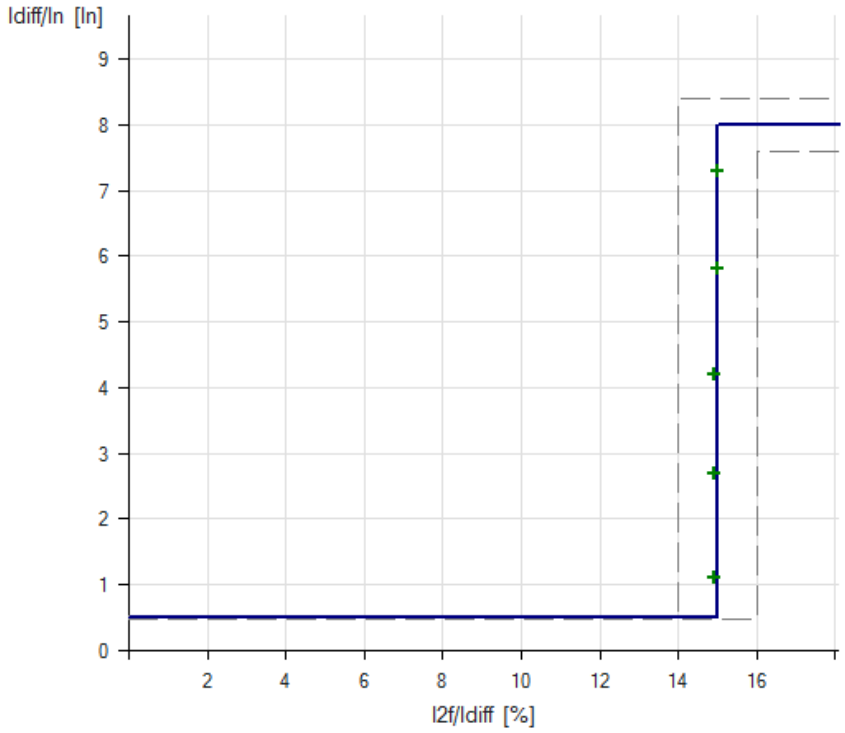


Figure 5.24: Second harmonic restraint characteristic curve

5.2.4.4 Differential Trip times test module

The trip times test confirms the operating time of the differential protection function. Therefore, test shots with different test points (Figure 5.25) are applied to the differential relay and the corresponding trip times of the SEL-487E relay are measured as shown in Figure 5.25.

The test points with several differential currents are applied as shown in Figure 5.25. It shows the differential current on the x-axis and the corresponding trip time on the y-axis. The differential trip time test results are given in Table 5.9.

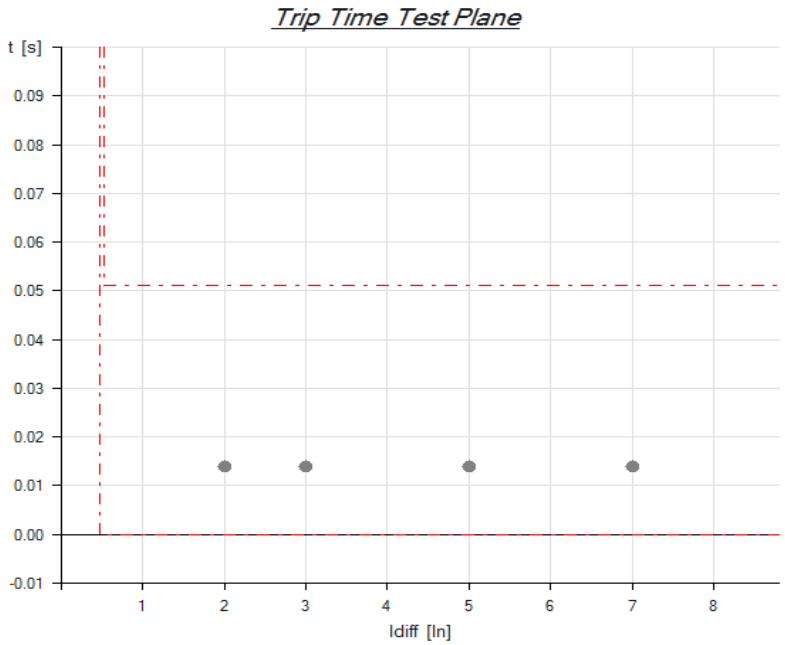


Figure 5.25: Differential relay trip time test points

Table 5.9: Differential relay trip time results

Idiff	Nominal Trip Time	Measured Trip Time	Assessment
2.00 In	0.0140 s	0.0455 s	Passed
3.00 In	0.0140 s	0.0461 s	Passed
5.00 In	0.0140 s	0.0462 s	Passed
7.00 In	0.0140 s	0.0470 s	Passed

From the differential relay trip time test results, it is observed that the measured trip time is slower than the nominal trip time of the SEL-487E relay by approximately 30 milliseconds and it is acceptable because they are within the debounce tolerance limits.

5.3 SEL-751A overcurrent relay configuration setting for backup protection of the power transformer

The SEL-751A relay used as a backup protection for the power transformer as shown in Figure 5.1. It does not have the inrush current blocking function, whenever the power transformer energises, the inrush currents operate the overcurrent function on the upstream of the network. Therefore, this research work developed an IEC 61850 GOOSE standard-based message inrush current blocking scheme in chapter six to avoid the maloperation of the overcurrent function due to the transformer magnetizing inrush current conditions. Therefore, it is necessary to provide the

engineering configuration setting of the overcurrent relay before proceeding to that in order to understand the transformer inrush blocking scheme.

This section of the chapter provides the configuration setting of the SEL-751A numerical relay in the AcSELerator Quickset and Omicron respectively. The test bed is implemented to test the overcurrent protection function, and the simulation results are provided.

5.3.1 Communication setting of the SEL-751A IED

Communication configuration setting of the SEL-751A numerical relay is shown in Figure 5.26. The computer communication port must be configured to the IP address domain of the IED's IP address.

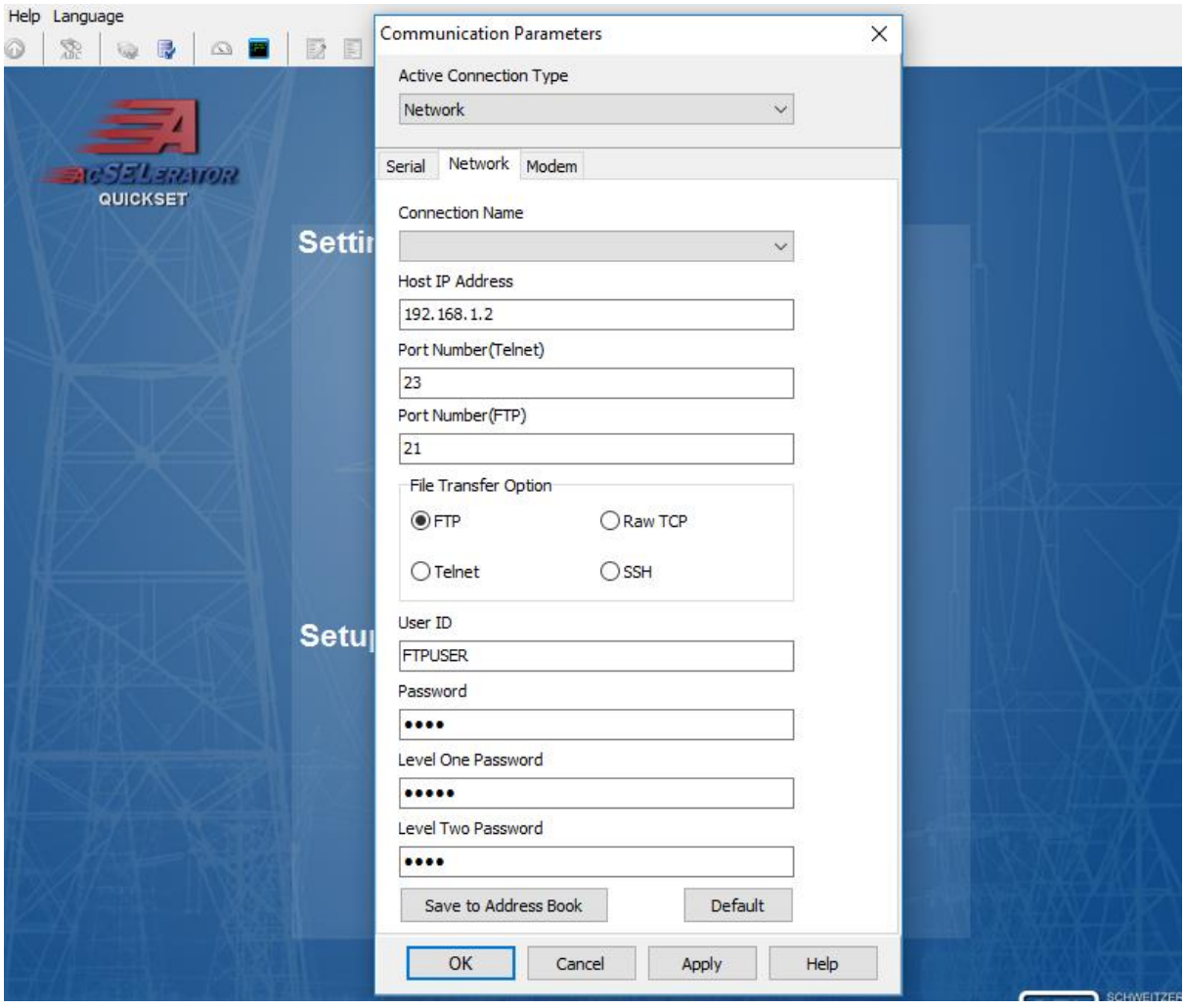


Figure 5.26: SEL-751A communication parameter configuration setting on AcSELerator Quickset

Not matching the IP address and port number will result in the communication link not being established. The default password is 'OTTER'. Once a communications link

has been successfully established, the user can read, edit and write settings onto the relay.

5.3.2 SEL-751A Overcurrent protection configuration setting using AcSELerator Quickset software

The general global setting of the overcurrent protection relay is shown in Figure 5.27 which includes system phase rotation as ABC; a nominal system rated frequency set to 50Hz, date format and Fault condition (SELogic).

Table 5.10 provides CT ratio settings of the phase and neutral elements. CTR and CTN are connected at the high voltage side of the power transformer and is set to 400A. According to CT ratio configuration settings, the relay measures the current signals and report the primary quantities. It calculates the phase and neutral CT ratios by taking the ratio of primary/secondary, which is set to 1A.

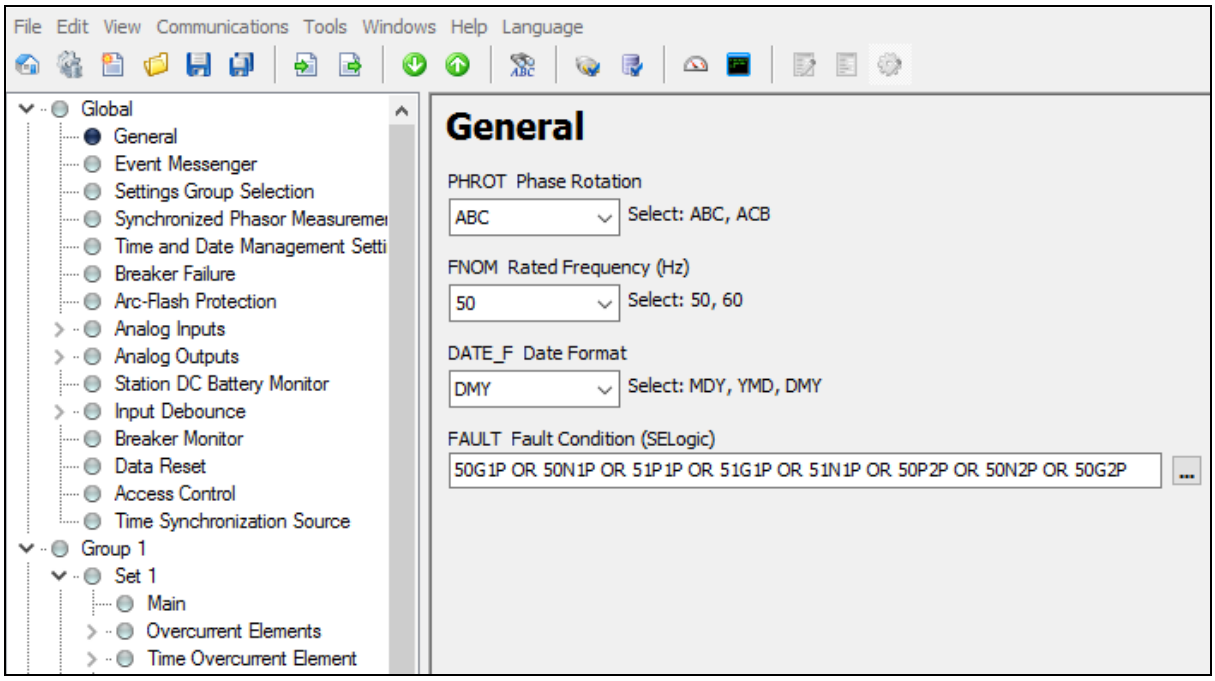


Figure 5.27: SEL-751A general global setting

Table 5.10: Current transformer configuration setting of the SEL-751A

Abbreviation	Description	Value
CTR	Phase (IA, IB, IC) CT ratio	400
CTN	Neutral (IN) CT ratio	400

The overcurrent elements (50 and 51) pickup and time delay settings, TOC curve selection, maximum phase time overcurrent torque control and trip time are configured according to the defined parameters as given in Table 5.11.

Table 5.11: SEL-751A Overcurrent elements configuration setting

Abbreviation (Relay Word Bit)	Description of the relay word bits	Value
50P2P	Maximum phase overcurrent trip pickup (Amps sec)	1.5
50P2D	Maximum phase overcurrent trip delay (seconds)	0.01
50P2TC	Maximum phase overcurrent torque control (SELogic)	1
50N2P	Neutral overcurrent trip pickup (Amps sec)	0.3
50N2D	Neutral overcurrent trip delay (seconds)	0.05
50N2TC	Neutral overcurrent torque control (SELogic)	1
51P1P	Time overcurrent trip pickup (Amps sec)	0.25
51P1C	TOC curve selection	C1
51P1RS	EM reset delay	N
51P1CT	Constant time adder (seconds)	0.00
51P1MR	Minimum response time (seconds)	0.00
51P1TC	Maximum phase time overcurrent torque control (SELogic)	1
51N1P	Neutral time overcurrent trip pickup (Amps sec)	0.30
51N1C	Neutral TOC curve selection	C1
51N1RS	EM reset delay	N
51N1CT	Constant time adder (seconds)	0.00
51N1MR	Minimum response time (seconds)	0.00
51N1TC	Neutral time overcurrent torque control (SELogic)	1

The SEL-751A tripping logic is designed to control the switching action of the circuit breakers. The relay logic allows the conditions that cause a trip and unlatch the trip and mapped to the output contact of the relay.

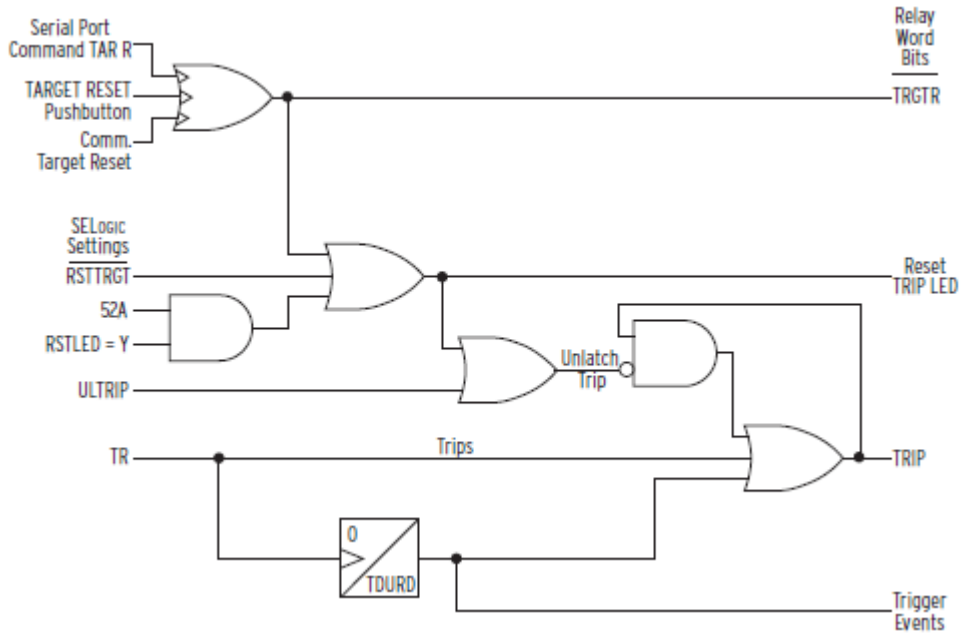


Figure 5.28: Trip logic (SEL-751A Instruction manual, 2012)

Figure 5.28 provides the SEL-751A trip logic. Following a fault, the trip signal is maintained until any of the following conditions are true:

- Minimum trip duration time (TDURD) passes
- The TR SELogic control equation result de-asserts to logical 0.

And one of the following occurs:

- Unlatch Trip SELogic control equation setting ULTRIP asserts to logical 1.
- Target Reset SELogic control equation setting RSTTRGT asserts to logical 1.
- Target Reset Relay Word TRGTR asserts. The TRGTR is asserted when the front-panel (TARGET RESET) pushbutton is pressed.

Table 5.12 provides SEL-751A trip logic conditions to provide the backup protection of the transformer.

Table 5.12: SEL-751A Trip logic conditions

Abbreviation (Relay Word Bit)	Description of the relay word bits	Value
TDURD	Minimum trip time (seconds)	0.5
CFD	Close failure time delay (seconds)	1
TR	Trip (SELogic)	50P2T OR 50N2T OR 51P1T OR 51N1T
REMTRIP	Remote trip (SELogic)	0
ULTRIP	Unlatch trip (SELogic)	NOT (51P1P OR 51G1P OR 51N1P OR 52A)
52A	Breaker status (SELogic)	0
CL	Close equation (SELogic)	SV03T AND LT02 OR CC
ULCL	Unlatch close (SELogic)	0

5.3.3 OMICRON test universe configuration setting to test the Overcurrent protection functions

The Overcurrent test module is used to perform the tests that are needed for the non-directional overcurrent protection function. In this case, the non-directional overcurrent protection elements are used as a backup protection for the power transformer. The definition of the Test Object settings and the Hardware configuration for non-directional overcurrent elements configuration setting are described in this section:

General relay settings such as relay type, relay ID, substation details are provided in the RIO function device as shown in Figure 5.29.

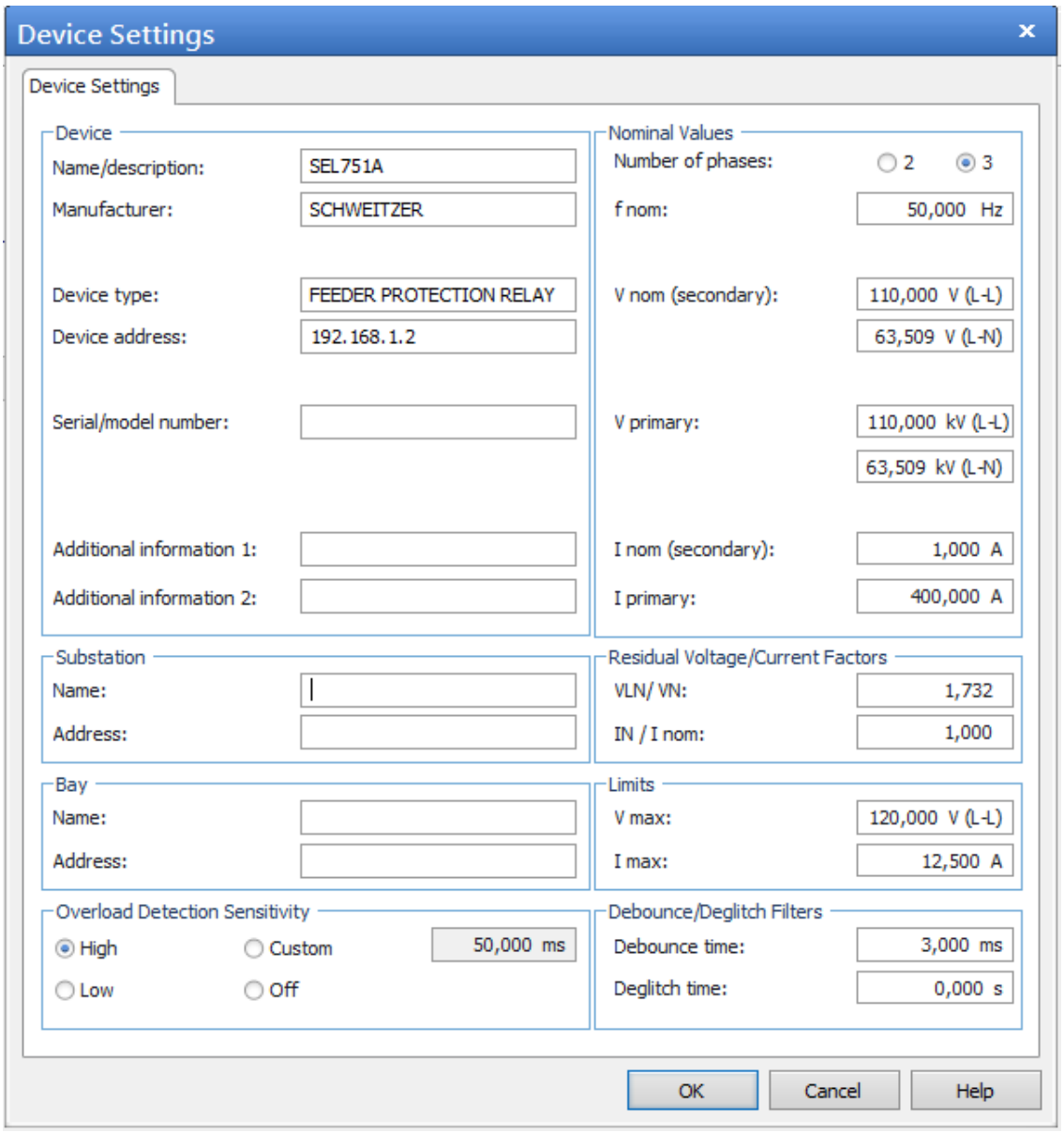


Figure 5.29: SEL-751A device settings in Test Universe

5.3.3.1 Overcurrent test module

This section provides the overcurrent relay configuration setting and its characteristics curve selection.

I. Overcurrent relay configuration setting

This subsection provides the Non-directional and Directional behaviour of the overcurrent function as well as the relay tolerances as shown in Figure 5.30.

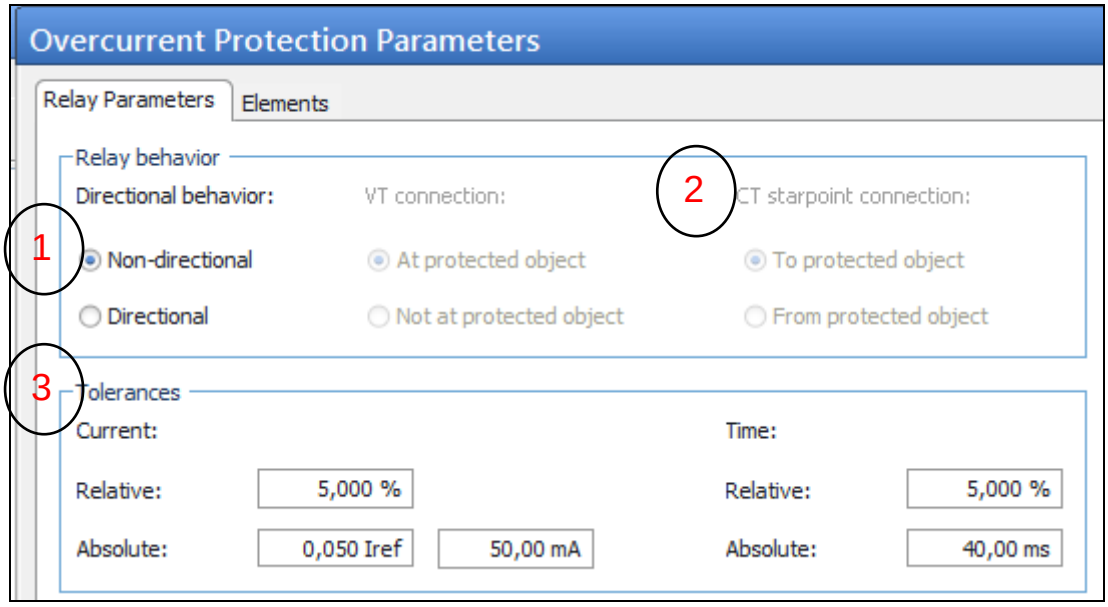


Figure 5.30: SEL-751A relay parameters

The numbers encircled from 1 to 3 in Figure 5.30 above provide the configuration setting of the non-directional overcurrent relay, CT and VT connection types, current and time tolerances respectively. The detailed description of the overcurrent protection configuration setting is given below:

1. The non-directional overcurrent relay used for the backup protection of the power transformer.

2. The CT star-point connection has to be set according to the connection of the secondary windings of the CT. In this case, the CT star point connection is towards the protected object.

3. The current and the time tolerances are set to 5% according to the SEL-751A relay instruction manual.

II. Phase/Residual overcurrent Elements characteristic curve selection

Operating time of the overcurrent relay defined by IEC 60255 and IEEE C37.112. Operating time defined by IEC 60255 and IEEE C37.112 is given in Equation 5.1 as follows:

$$t(s) = \frac{A * Td + K1}{M^P - Q} + B * Td + K2 \quad (5.1)$$

Where:

t is the relay operating time in seconds

Td is the Time dial or time multiplier setting

M is Ratio of I / Ipick-up where I is the test current, and Ipick-up the pick-up current setting.

B is a constant

A is the Slope constant

P is the Slope constant

Table 5.13 provides the A, B, P, Q, K1 and K2 constant values for the inverse time overcurrent curves defined by IEC 60255 international standards.

Table 5.13: Inverse-time overcurrent relay constants

Characteristic curve	A	B	P	Q	K1	K2
IEC Normal Inverse	0.14	0.0	0.02	1.0	0.0	0.0
IEC Very Inverse	13.5	0.0	1.0	1.0	0.0	0.0
IEC Extremely Inverse	80.0	0.0	2.0	1.0	0.0	0.0

III. Overcurrent protection elements configuration setting

The characteristic of the IEEE/IEC inverse-time overcurrent stages is defined in this section. The numbers encircled 1 to 5 in Figure 5.31 is described as follows:

1. Overcurrent element type is selected using this option either phase or ground as shown in Figure 5.31.

2. The elements which define the tripping characteristic are shown in this table for the selected element type. The stage name of the elements is selected according to the name used in the relay. In this case, element 1 is set to IEC normal inverse (phase) and element 2 is set to IEC definite time characteristic curve.

3. The overcurrent characteristic curve type is selected using this option. It provides the time constants for both IEEE/IEC inverse time overcurrent characteristic curves.

4. Pickup current and the time delay settings of the overcurrent elements are defined. In this case, the pickup current is 0.25Iref and time delay is 0.1s.

5. The tolerance limits of both overcurrent elements and time delay settings are defined.

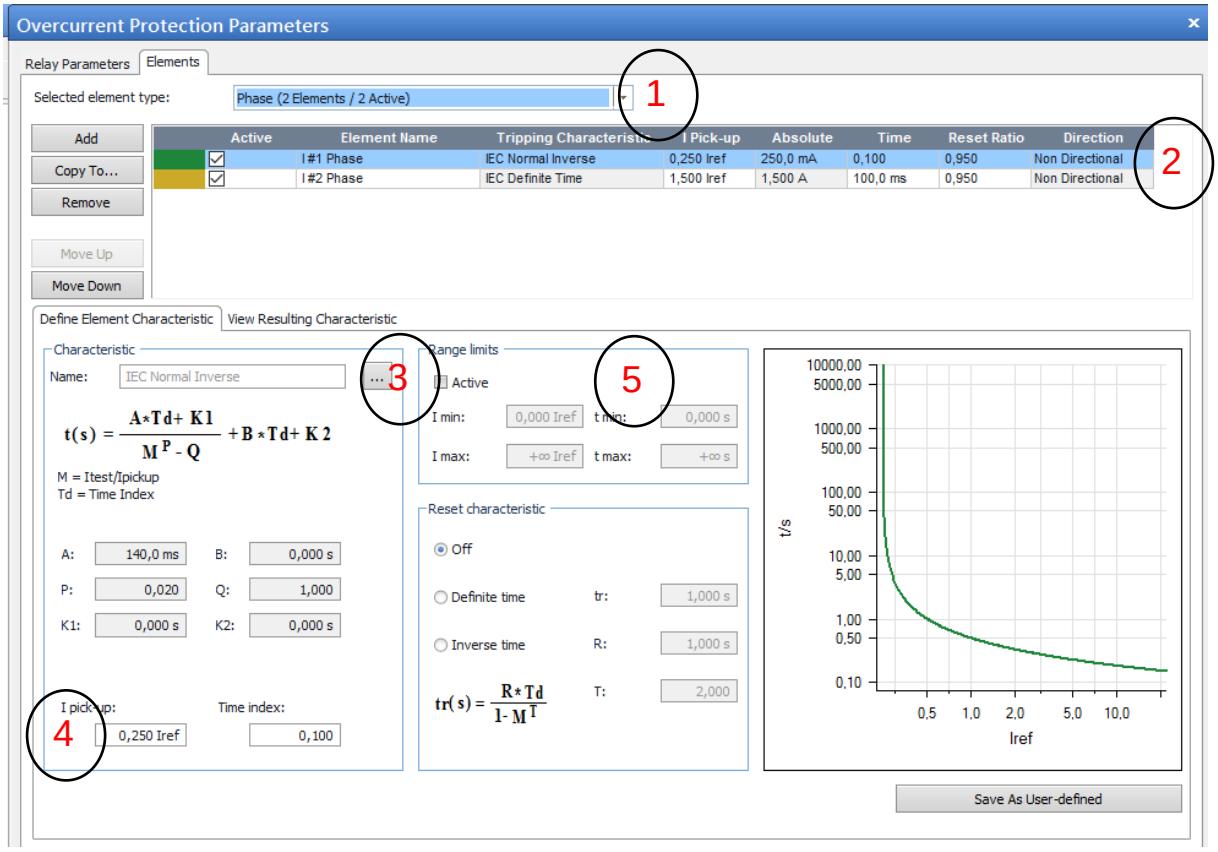


Figure 5.31: Overcurrent element configuration setting

Tables 5.14 and 5.15 provide the configuration setting of the IEC Normal Inverse and Definite Time overcurrent characteristics of a phase and residual elements respectively.

Table 5.14: Phase overcurrent element configuration setting

Active	Name	Tripping characteristic	I Pick-up	Time	Reset ratio	Direction
Yes	I #1 Phase	IEC Normal Inverse	0.25 Iref	0.10	0.95	Non-Directional
Yes	I #2 Phase	IEC Definite Time	1.5 Iref	0.01	0.95	Non-Directional

Table 5.15: Residual overcurrent element configuration setting

Active	Name	Tripping characteristic	I Pick-up	Time	Reset ratio	Direction
Yes	I #1 Phase	IEC Normal Inverse	0.25 Iref	0.10	0.95	Non-Directional
Yes	I #2 Phase	IEC Definite Time	0.3 Iref	0.05	0.95	Non-Directional

Figures 5.32 and 5.33 show the phase and residual overcurrent characteristics curves respectively. The phase overcurrent element is set between the range of 0.25Iref and 6.0Iref for inverse time overcurrent characteristics and any current above 6.0Iref is set for the definite time overcurrent.

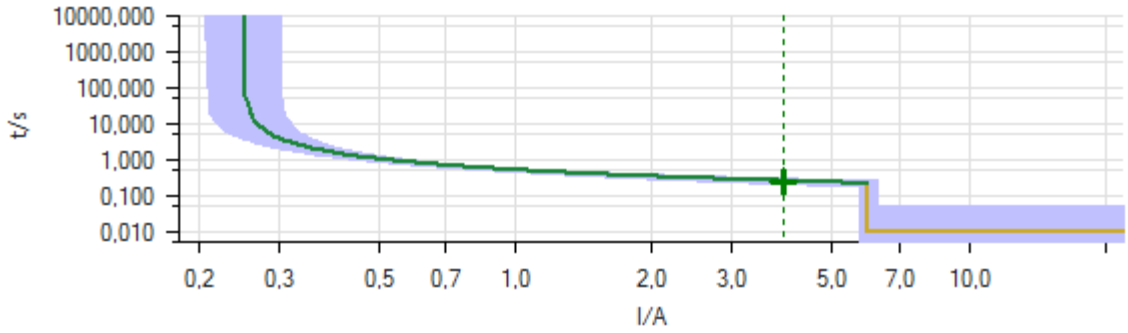


Figure 5.32: Phase overcurrent characteristic curve in Test Universe

The ground/residual overcurrent element is set between the range of 0.10Iref and 2.0Iref for inverse time overcurrent characteristics curve any current above 2.0Iref is set for the definite time overcurrent.

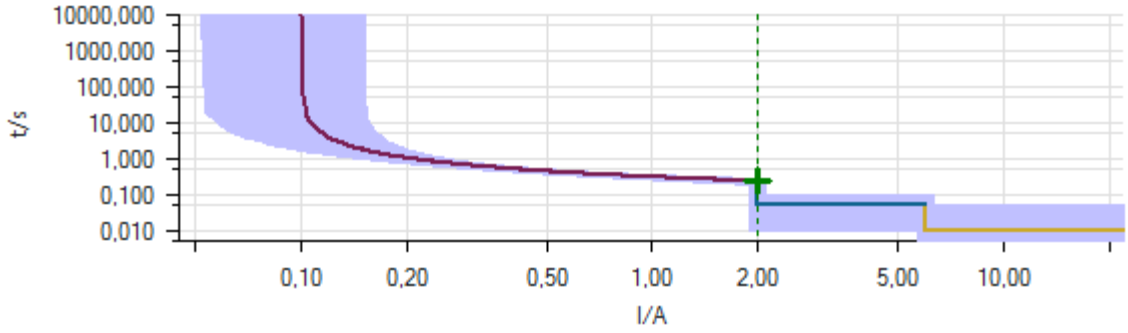


Figure 5.33: Residual overcurrent characteristic curve

5.3.3.2 Hardware configuration setting of the SEL-751A overcurrent elements in Test Universe

The global hardware configuration has been defined according to the relay connection.

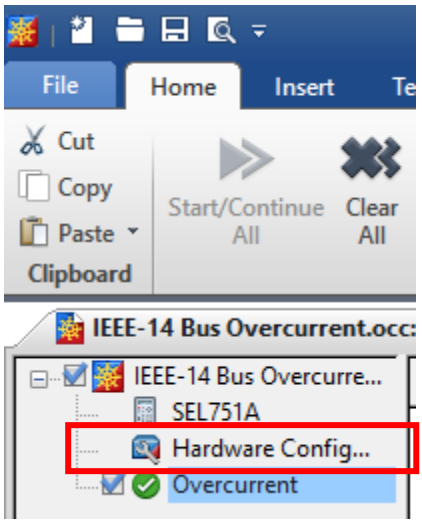


Figure 5.34: Hardware configuration of the overcurrent test module

The hardware configuration of the overcurrent test module is shown in Figure 5.34. In this case, overcurrent elements of the SEL-751A relay are used as a backup protection for power transformer IED (SEL-487E). Therefore, the three-phase current signals of the SEL-751A is mapped to the channel A of the Omicron CMC 256plus test injection device as shown in Figure 5.35.

The output configuration of the current channel A is set to a 1 A nominal secondary current as shown in Figure 5.35.

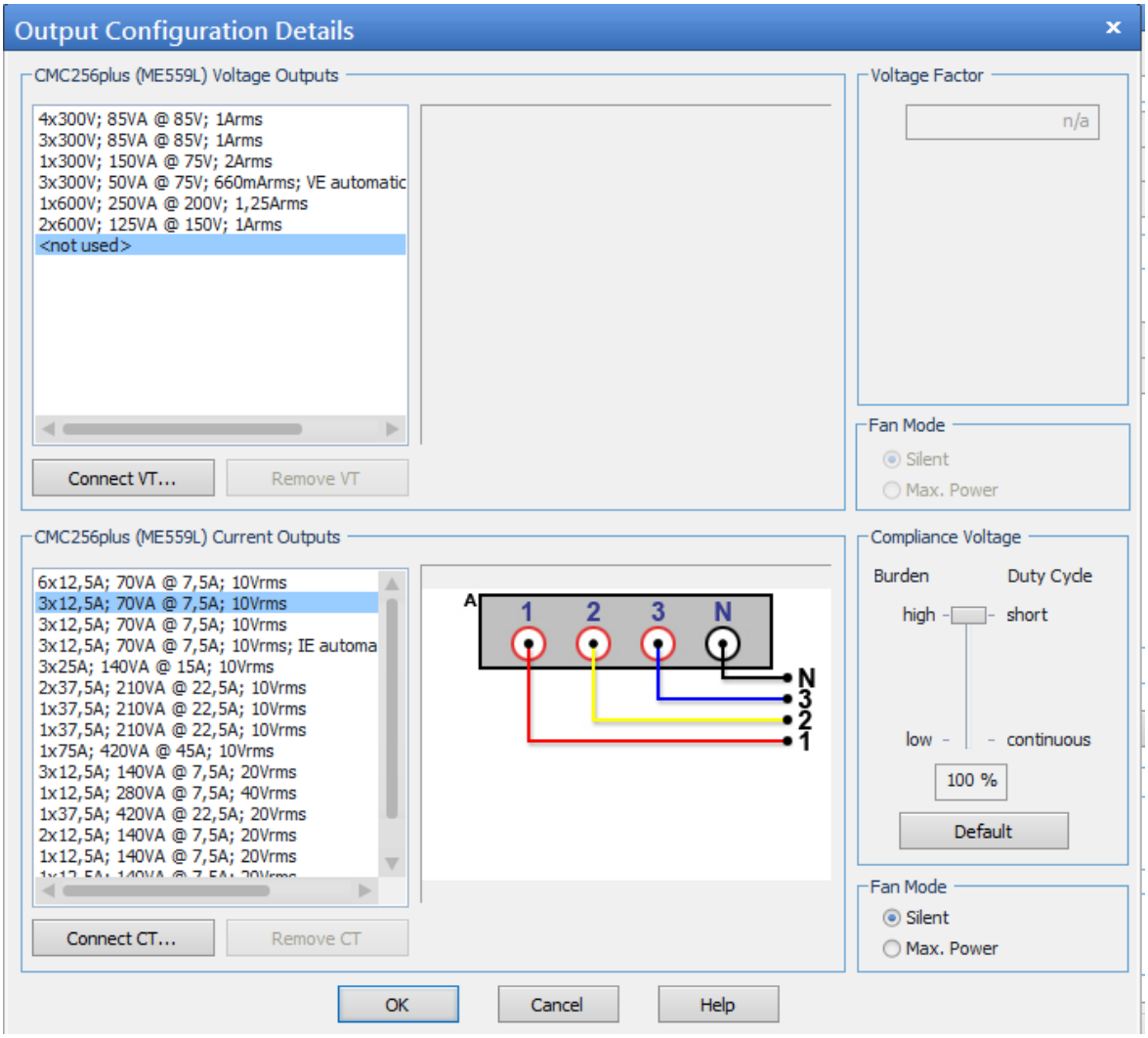


Figure 5.35: Current channel A output configuration settings of the CMC 256 device

a) Analogue output configuration setting of the SEL-751A IED

The analogue outputs, binary inputs and binary outputs are activated individually in the local hardware configuration of the specific test module. Figure 5.36 shows the analogue outputs configuration, in this case, the three-phase currents of the SEL-

751A overcurrent relay is configured to the analogue outputs 1 to 3 of the CMC 256 test set.

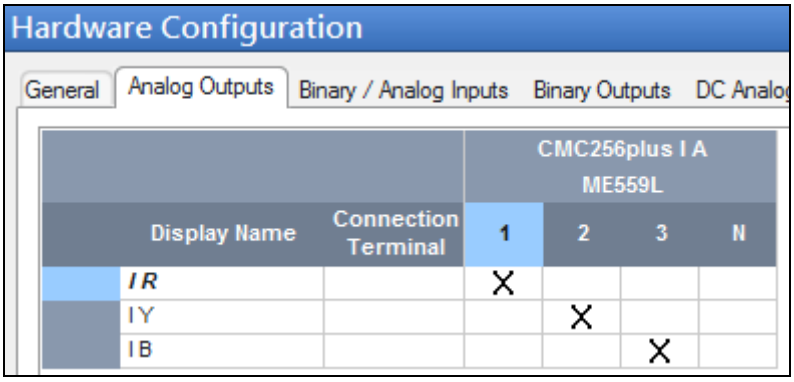


Figure 5.36: Analog output configuration setting of the SEL-751A overcurrent test module

b) Binary input configuration setting on the CMC 256 test set for the SEL-751A overcurrent elements

The start command is mapped to the pickup current of the overcurrent element, and it is connected to Binary Input (BI1). The trip command is connected to Binary Input (BI2). The binary outputs, the analogue inputs etc. are not configured in this case. Figure 5.37 shows the mapping of Start and Trip signals in the CMC 256 test injection device.

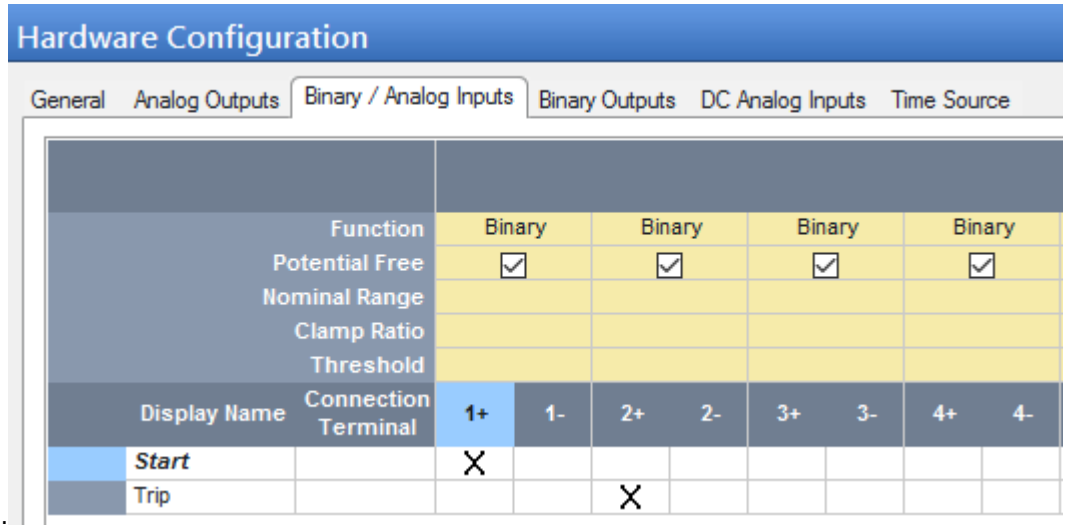


Figure 5.37: Binary inputs (start and trip signals) configuration setting of the SEL-751A

5.4 Comparison of the DIgSILENT Power Factory Overcurrent simulation test results with test bench results using SEL-751A IED

In this section the DIgSILENT overcurrent simulation results are compared with the test bench results for the considered three scenarios, they are (i) three-phase event, (ii) line-to-line event and (iii) line-to-ground event. The simulation results of the above

scenarios are presented in this section. In order to make the comparison between the DIgSILENT simulations results and the test bench results, fault currents from DIgSILENT need to be converted according to current coil limits of SEL-751A overcurrent relay. Table 5.16 provides the conversion factor used to transfer the DIgSILENT simulation currents to hardware SEL-751A overcurrent relay.

Table 5.16: Conversion factor used to transfer DIgSILENT simulation currents according to current coil limits of SEL-751A

Fault type	DIgSILENT simulation results (primary currents)	DIgSILENT simulation results (secondary currents)	Secondary current injected into the SEL-751A using CMC 256	Primary current injected into the SEL-751A using CMC 256
Three-phase fault	6209.909A	$I_{test} = CT_r \times I_{fault} = \frac{1}{400} \times 6209.909$ = 15.52	$I_{test} = I_{sec} \times I_{ref} = 15.52 \times 0.25$ = 3.88A	$I_{test} = CT_r \times I_{sec} = 400 \times 3.88$ = 1552A
Line-line fault	5383.07A	$I_{test} = CT_r \times I_{fault} = \frac{1}{400} \times 5383.07$ = 13.45	$I_{test} = I_{sec} \times I_{ref} = 13.45 \times 0.25$ = 3.36A	$I_{test} = CT_r \times I_{sec} = 400 \times 3.36$ = 1344A
Line-ground fault	7944.797A	$I_{test} = CT_r \times I_{fault} = \frac{1}{400} \times 7944.797$ = 19.86	$I_{test} = I_{sec} \times I_{ref} = 19.86 \times 0.1$ = 1.98A	$I_{test} = CT_r \times I_{sec} = 400 \times 1.98$ = 792A

5.4.1 Three-phase short-circuit scenario

Three-phase short-circuit simulation study in DIgSILENT Power Factory environment generated a fault current of 6209.909A. To simulate a scenario for 6209.909 fault current magnitude is generated using the CMC 256 device in the implemented overcurrent lab-scale test bench setup, the CT ratio of 400/1A is adopted. The CT ratio must always be selected high enough, so that the magnitude of the currents that are injected into the relay can be limited, to ensure that the currents injected into the IED do not damage the relay coils. The maximum time that a certain current can be injected into the device without damage is calculated using Equation 5.2 (SEL-751A Instruction manual, 2012).

$$T_{max} = \frac{10000}{\left(\frac{I_{test}}{I_{nom}}\right)^2} \quad (5.2)$$

Where:

I_{test} - test current being injected into the relay

I_{nom} – rated input current of the relay (1 or 5A), in this case, 1A CT is used.

The magnitude of the current that we need to inject into the IED for this study case is calculated using Equation 5.3 below.

$$I_{test} = CT_r \times I_{fault} \tag{5.3}$$

Where:

CT_r is the CT ratio of the SEL-751A relay;

I_{fault} is the three-phase short-circuit in Amperes.

$$I_{test} = \frac{1}{400} \times 6209.909$$

$$I_{test} = 15.52\ A$$

Since this current is above the nominal rating of the IED, we need to calculate how long it can safely be applied without causing damage to the IED using Equation 5.4.

$$T_{max} = \frac{10000}{\left(\frac{15.52}{1}\right)^2} \tag{5.4}$$

$$T_{max} = 41.516\ seconds$$

The three-phase short-circuit simulation results obtained from the Test Universe and AcSELerator Quickset are shown in Figures 5.38 and 5.39 respectively.

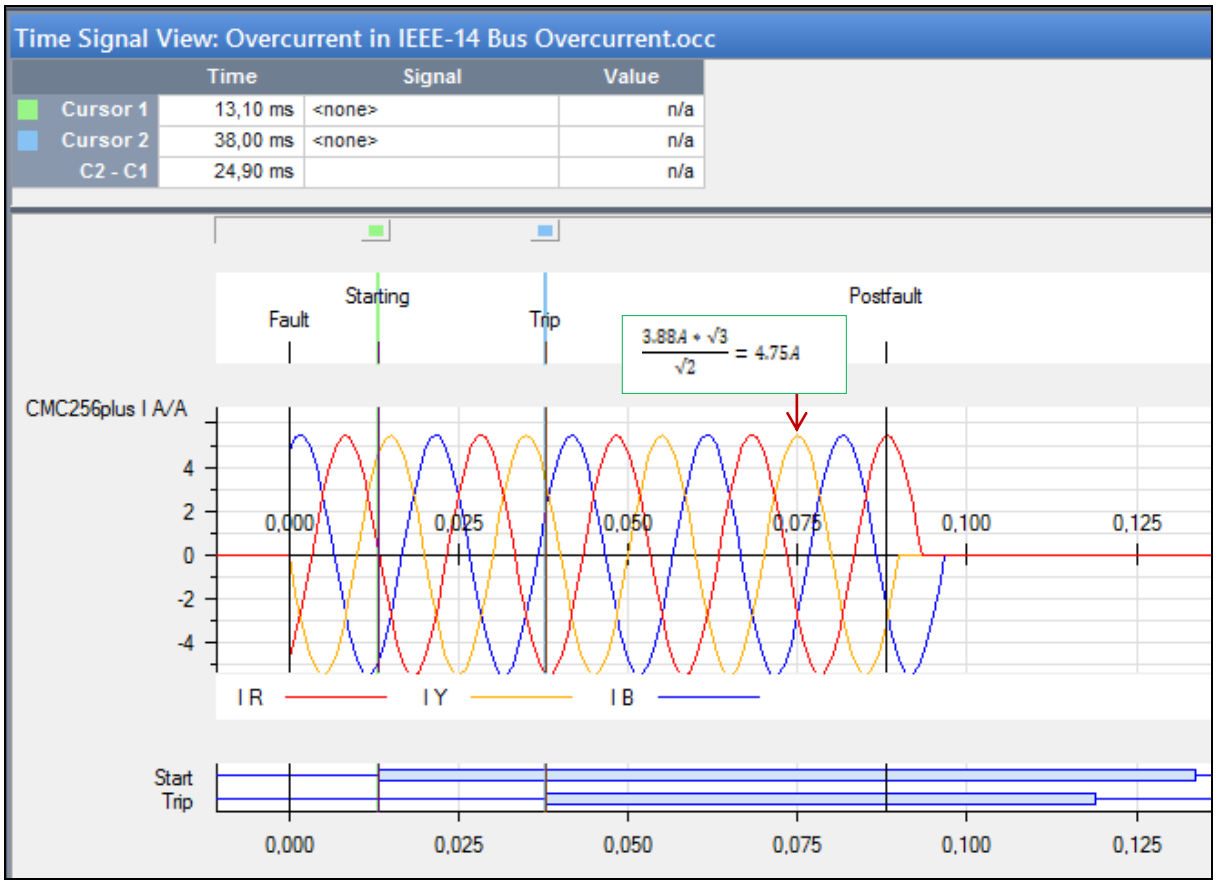


Figure 5.38: Three-phase short-circuit simulation results in Test Universe

The phase and ground overcurrent protection elements configuration setting are given in Tables 5.14 and 5.15 respectively. It is noted that CT ratio is 400/1 Amps and the phase element 1 set to IEC normal inverse curve with the pickup current of 0.25Iref and the Time dial of 0.1 seconds.

With the factor to (6209.9A/400A) = 15.52, then the CT secondary current to be injected to the relay equals to (15.52 X 0.25A) = 3.88A. Therefore, the Omicron simulation results for L1-L2-L3 fault loop provide 3,88 A secondary current which is equal to (3.88 X 400) = 1552Amps primary current.

The results of the SEL-751A IED is analysed with AcSELerator Analytic tool which provides 1552Amps for L1-L2-L3 fault loop, and it is the same as the test universe simulation result. 50P2P instantaneous element picks up the fault after 0.013 seconds and 50P2T element issues the trip signal at 0.038 seconds after the pickup as shown in Figure 5.39.

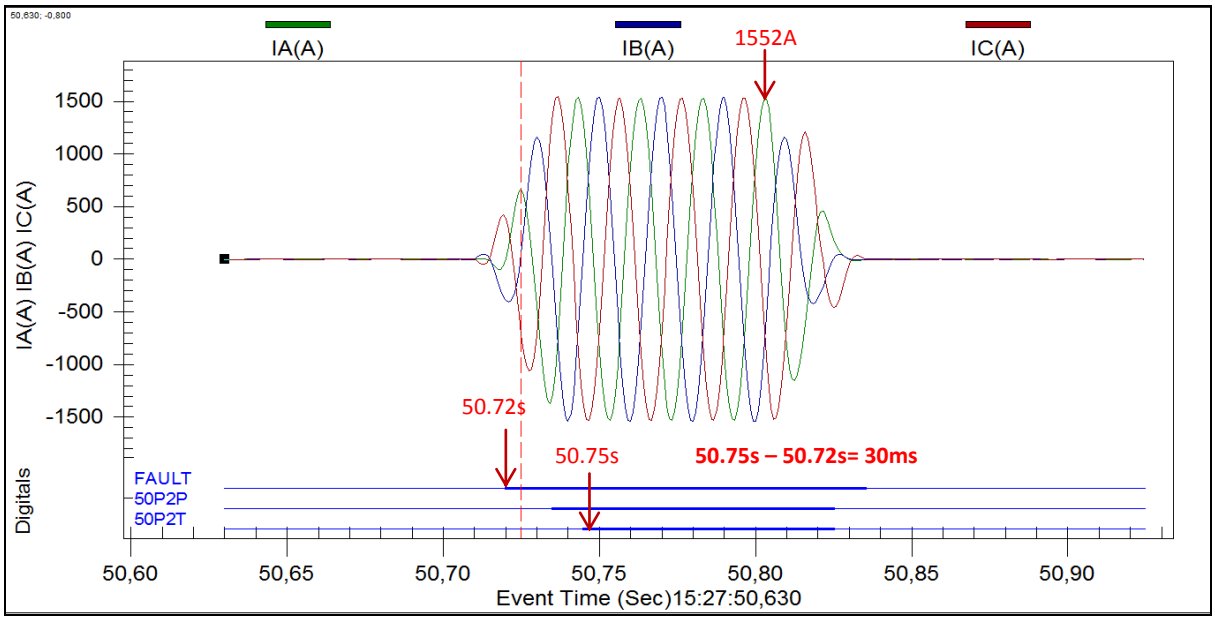


Figure 5.39: Three-phase fault signals and its digital signals (relay word bits) of the SEL-751A overcurrent relay

5.4.2 Line-to-line short circuit scenario

This study case is assessing the real-world tripping time of the SEL 751A for a double phase fault scenario with a current magnitude of 5383.07A. The current that needs to be injected into the IED was calculated to be 3.362A using Equation 5.2, and the simulation results of the test LL fault scenario is shown in Figures 5.40 and 5.41 respectively from the Test Universe and SEL analytic tool.

The Omicron test report provides L1-L2 fault loop scenario generated a 3,362 A secondary current which is equal to (3.362 X 400) = 1344.8Amps primary current. The AcSELerator Analytic tool results provide 1344.8Amps for L1-L2 fault loop

scenario which the same as the test universe result. 50P2P instantaneous element picks up the fault after 0.014 seconds and 50P2T element issues the trip at 0.0439 seconds after the pickup as shown in Figure 5.41.

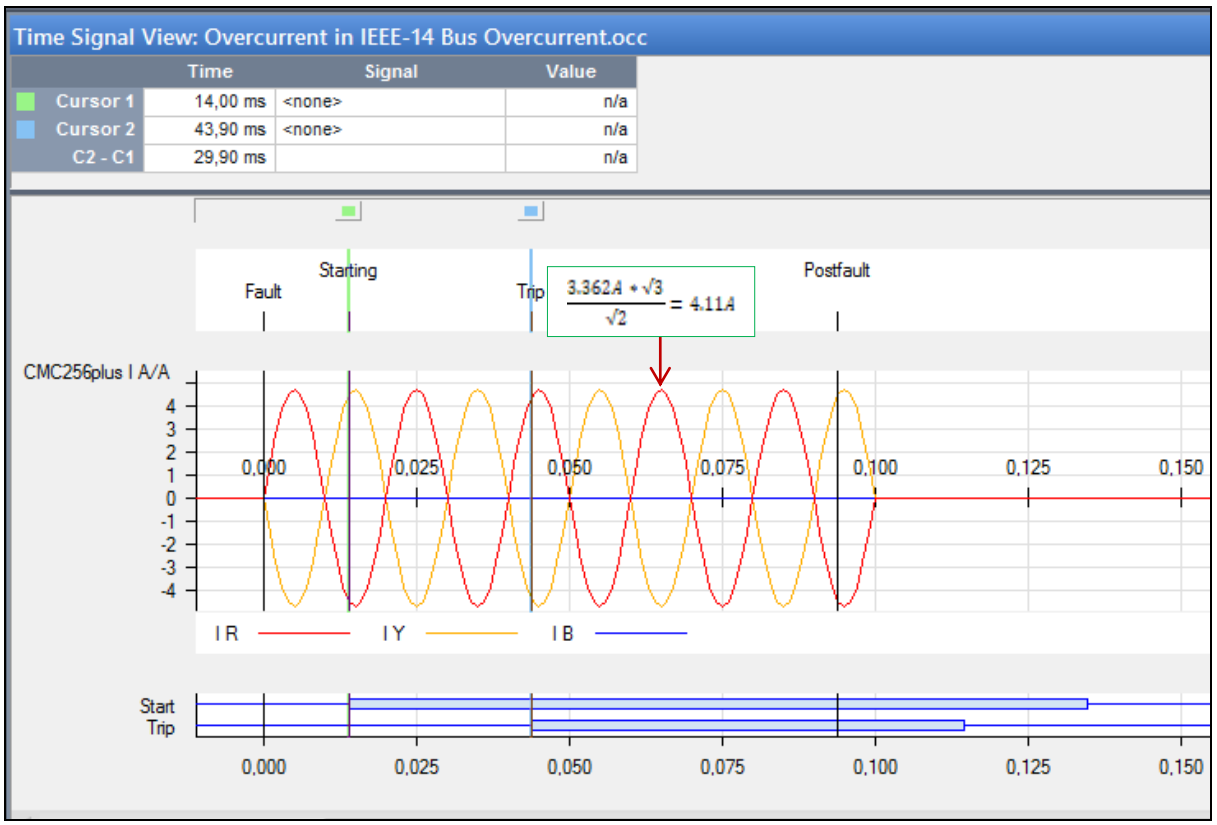


Figure 5.40: Phase-to-phase short-circuit simulation results in Test Universe

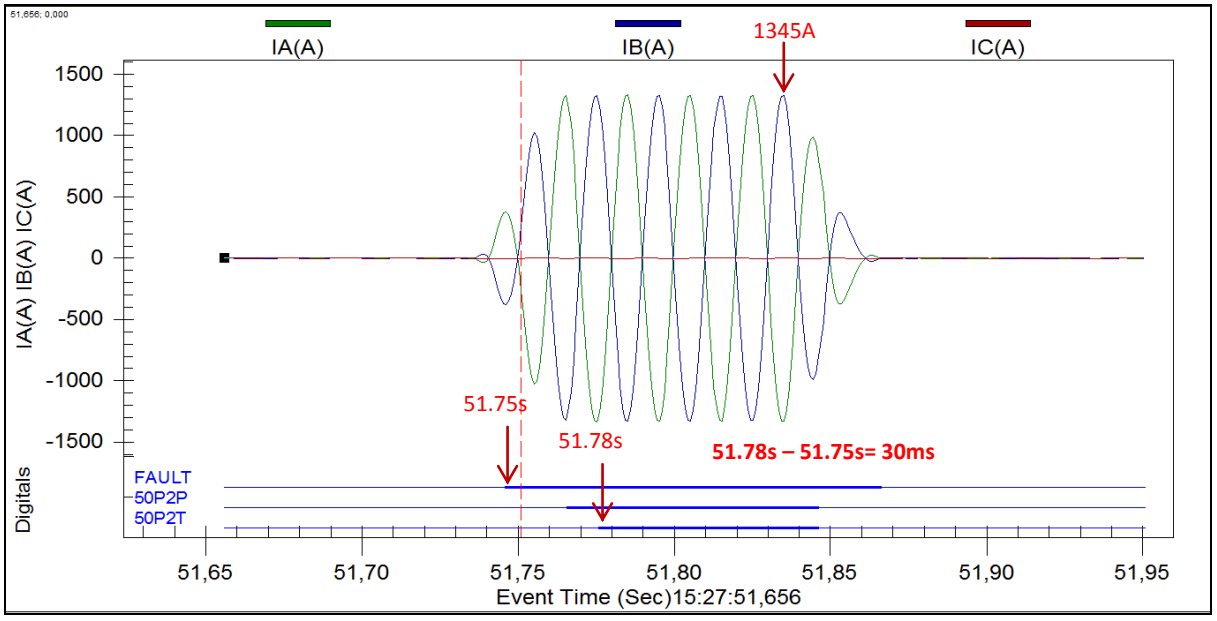


Figure 5.41: Phase-to-phase fault signals and its digital signals (relay word bits) of the SEL-751A overcurrent relay

5.4.3 Single-phase to ground fault scenario

The single phase to ground fault DIgSILENT simulation results provide a fault current of 7944.797A and a tripping time of 20ms. This translates to a current of 19.86A using Equation 5.2 that needs to be injected into the SEL-751A IED. The Test Universe and SEL analytic tool simulation results are shown in Figures 5.42 and 5.43 respectively.

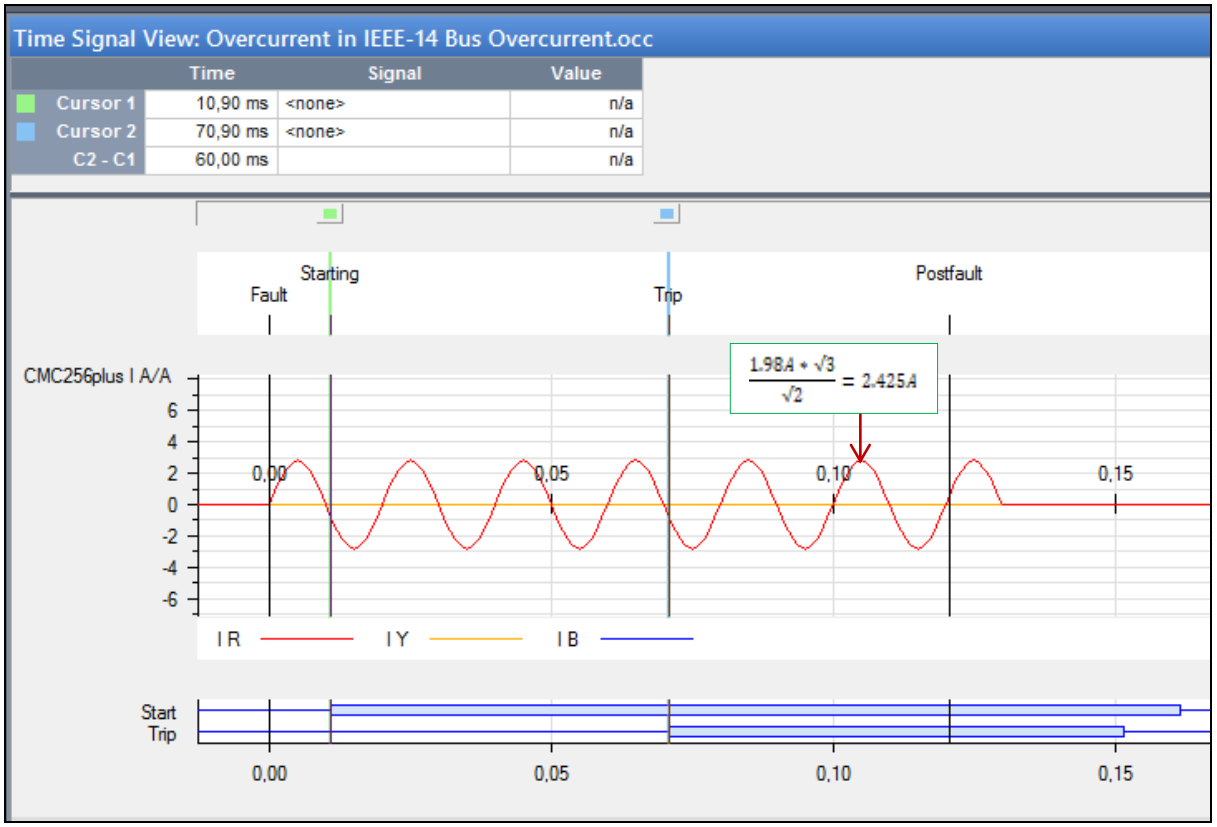


Figure 5.42: Single-phase short-circuit simulation results in Test Universe

The phase and ground overcurrent protection configuration settings are given in Tables 5.14 and 5.15 respectively. It is noted that CT ratio is 400/1 Amps and the phase element 1 set to IEC normal inverse curve with the pickup current of 0.1 Iref and the Time dial of 0.1 seconds. With the factor of (7944.797A/400A) = 19.86A is the current to be injected to the relay which equals to (19.86 X 0.1A) = 1.98A secondary Amps.

Therefore, Omicron simulation results for L1-E fault loop provide 1.98 A secondary current which is equal to (1.98 X 400) = 792Amps primary current. The results of the SEL-751A IED is analysed using the AcSELerator Analytic tool which provides 792Amps for L1-E fault loop, and it is same as the test universe simulation result given in Figure 5.42. 50P2P instantaneous element picks up the fault after 0.010

seconds and 50P2T element issues the trip 0.070 seconds after the pickup as shown in Figure 5.43.

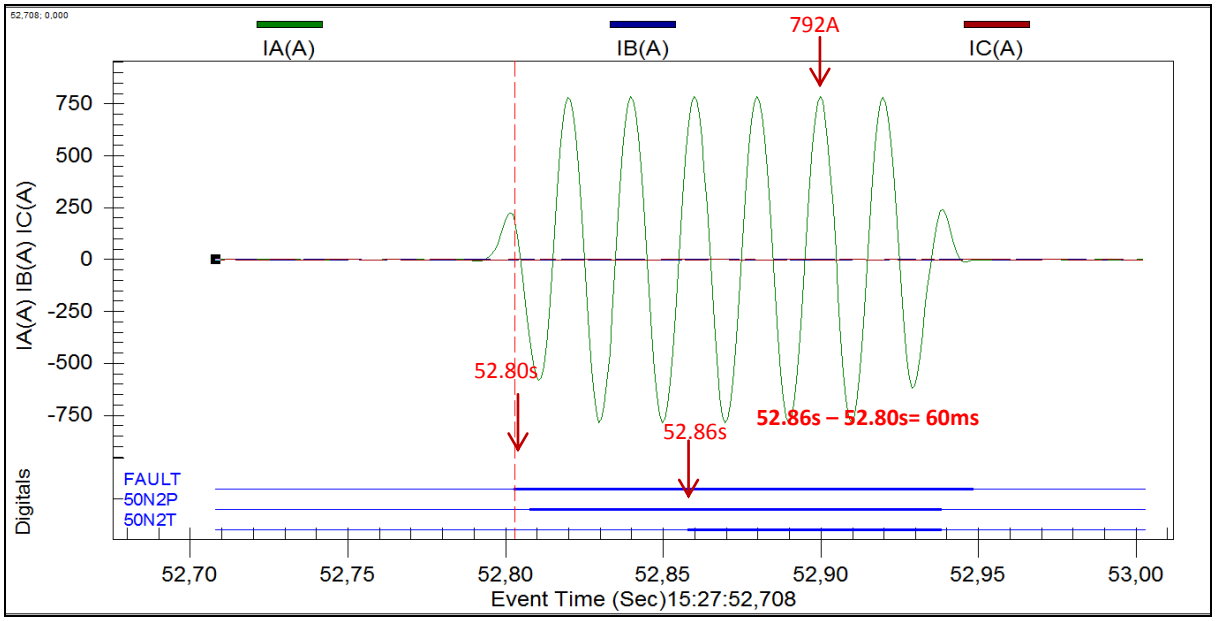


Figure 5.43: Single-phase fault current and its digital signals (relay word bits) of the SEL-751A overcurrent relay

Table 5.16 provides the summary of the comparison of the DIgSILENT overcurrent simulation results with SEL-751A test bench results according to their fault current magnitudes and trip times.

Table 5.17: Comparison of the DIgSILENT overcurrent simulation results with SEL-751A test bench results

Type of Events	Fault current magnitude in Amps		Trip time in seconds	
	DIgSILENT simulation results	SEL-751A Test bench results	DIgSILENT simulation results	SEL-751A Test bench results
Three-phase event (L1-L2-L3)	6209.90	1552	0.020	0.038
Line-to-line (L1-L2)	5383.07	1344.80	0.020	0.044
Line-to-ground (L1-G)	7944.79	792	0.020	0.070

It can be seen from the results that the tripping times from the test bench are slightly higher than the DIgSILENT simulation. The reason for this is that the DIgSILENT results are calculated from a soft relay that has no moving contacts and no signals being transmitted through hardwire. With the lab scale test, the SEL-751A relay has moving contacts that have a time delay to them. Added to that, one must factor in the time delay caused by the time it takes the feedback signal to travel through the hardwire, and the time taken by the Omicron test set to process that signal and asses

the test. In summary, the maximum time delay of 50ms has occurred between the DIgSILENT and the overcurrent test bench simulation results.

5.5 Conclusion

This chapter provided the configuration setting of the transformer differential protection function and its backup overcurrent protection.

The detailed description of the test object settings as well as the hardware configuration settings for both differential and Overcurrent test modules are provided. The test bench setup is implemented (Figure 5.1) to test the SEL-487E current differential function and SE-751A overcurrent functions of the protective relaying systems.

SEL-487E sensed the unbalance flow of currents for three types of different events (LLL, LL, and LG) internal to the protection zone. The performance of the differential relay was tested successfully for the following scenarios:

- Differential configuration
- Differential operating characteristic
- Differential trip time characteristic
- Differential harmonic restraint

On the other hand, the backup overcurrent transformer protection SEL-751A performance was also successfully tested for LLL, LL and LG events. Furthermore, SEL-751A trip times performance was tested and compared with DIgSILENT simulation results.

Chapter six discusses the implementation of the Hardwired and IEC 61850 GOOSE message based reverse harmonic blocking scheme for the power transformer in order to prevent overcurrent elements from tripping during magnetizing inrush current conditions.

CHAPTER SIX

IMPLEMENTATION OF THE HARDWIRED AND IEC 61850 STANDARD-BASED GOOSE MESSAGE FOR REVERSE HARMONIC BLOCKING SCHEME

6.1 Introduction

During transformer energisation or recovery from a system fault, a substantial amount of inrush currents flows into the transformer without a corresponding current leaving. The differential relay has the capability to detect an inrush condition and

restrain itself from tripping. However, the overcurrent relay employed as backup protection does not have inrush current feature.

In order to restrain the SEL 751A overcurrent relay from tripping during inrush conditions, a reverse blocking scheme based on harmonic currents is employed. The scheme uses the Harmonic Blocking element (87HB) of the SEL 487E IED to send a blocking signal to the SEL 751A IED at upstream of the network to inhibit it from tripping during inrush conditions as shown in Figure 6.1.

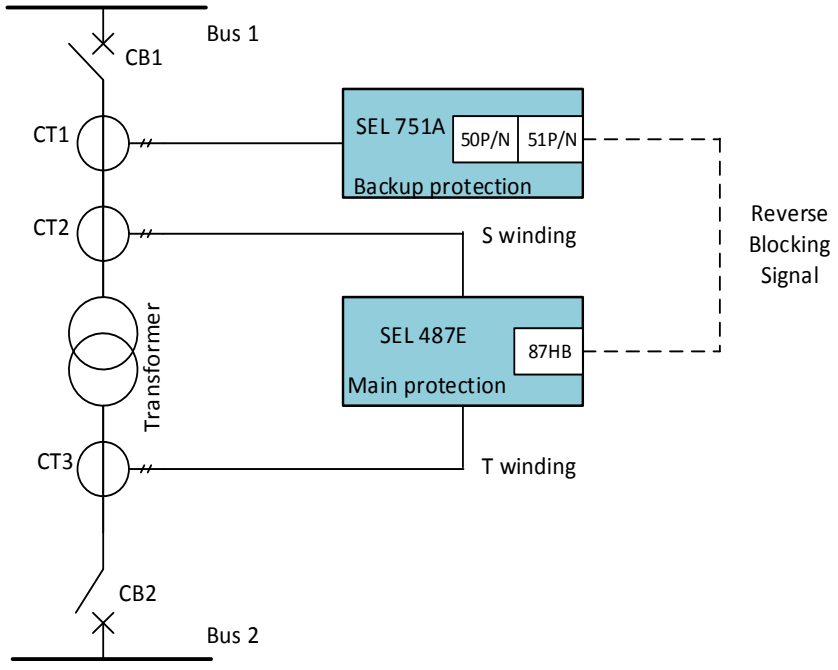


Figure 6.1: Reverse Harmonic Blocking scheme for power transformer protection

SEL-751A: Overcurrent relay

SEL-487E: Current Differential relay

CB: Circuit Breaker

CT: Current Transformer

As soon as currents are fed into the IEDs by the CTs (CT1, CT2 and CT3) as shown in Figure 6.1, the SEL 487E and SEL 751A perform Discrete Fourier Transform (DFT) signal processing and calculate internal protection function to determine which element is asserted and de-asserted. During Transformer Magnetizing Inrush Current (TMIC), if the calculated second harmonic values of the primary currents exceed the pickup or setting value, the Harmonic Blocking element (87HB) of the SEL 487E asserts and restrain the SEL 487E from tripping. While asserted, the 87HB element transmits a blocking signal to the SEL 751A to restrain from tripping due to TMIC condition as shown in Figure 6.1.

This chapter provides the test bench implementation for the reverse harmonic blocking scheme using hardwired DC signals and IEC 61850 standard-based GOOSE message. The developed algorithm for the reverse harmonic blocking scheme is presented. Two case studies are studied, one for the malfunction of the SEL-751A IED due to TMIC and another one to prevent the tripping of the SEL-751A IED due to TMIC using the reverse harmonic blocking scheme.

6.2 Test bench set-up of the reverse harmonic blocking scheme

To verify and investigate the performance of the reverse harmonic blocking scheme, a test bench is developed and is shown in Figure 6.2 and 6.3 respectively. The test bench consists of the following equipment: SEL 487E IED, SEL 751A IED, Omicron CMC 356 Test set, RUGGEDCOM RSG 2288 Ethernet switch and the personal computer with AcSELerator Quickset application to perform engineering configuration for the numerical relay and AcSELerator Architect IEC 61850 engineering configuration software tool as shown in Figure 6.2.

In Figure 6.2, the OMICRON test set is used to inject the inrush currents from channel A and B of the CMC 356 into the protection IEDs (SEL-487E and SEL-751A). The S winding of the SEL 487E is connected in series with the SEL 751A via current channel A of the CMC test set. This is because the S winding of SEL-487E and the SEL 751A backup overcurrent relay both monitor the primary winding of the power transformer. The CMC 356 device is used to provide the 110DC voltage which is used to interlock the two IEDs (SEL-487E and SEL-751A) as shown in Figure 6.2. The T winding secondary side of the power transformer is connected to current channel B of the CMC 356 test set. The IEDs (SEL-487E and SEL-751A), CMC 35

and a laptop with engineering configuration tools are connected in the network using the Ethernet protocol for substation communication.

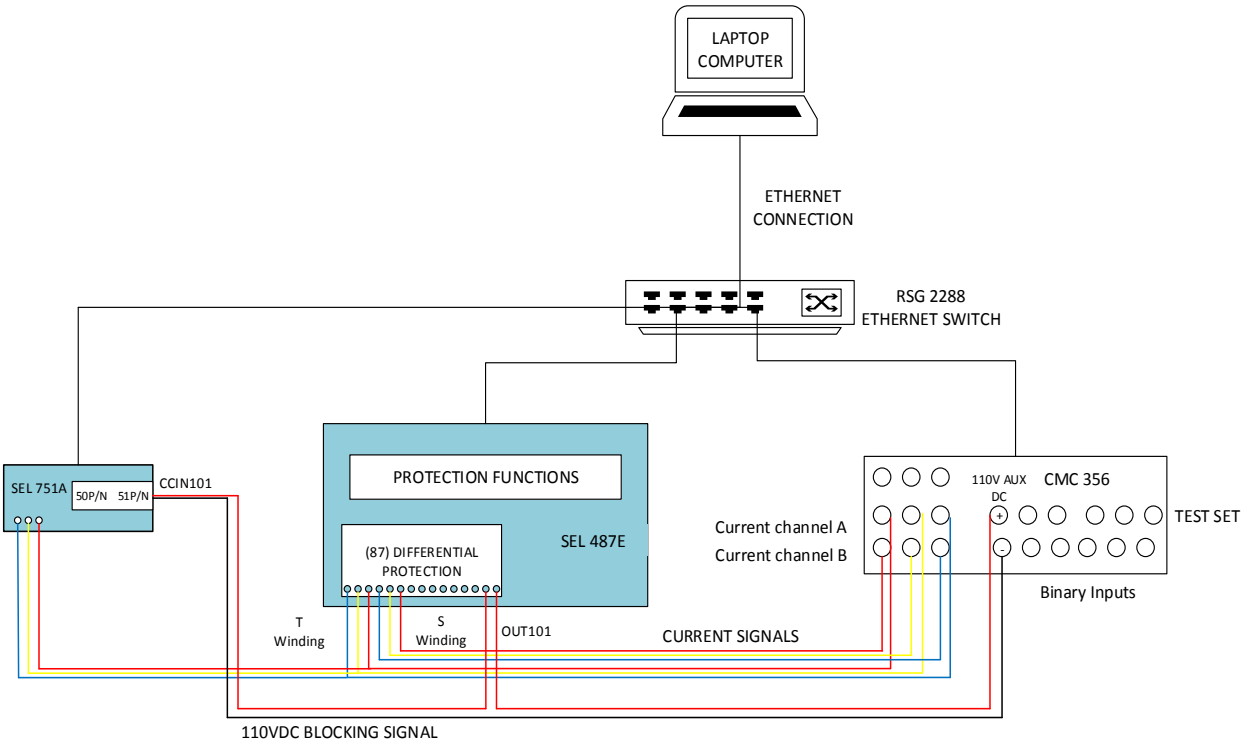


Figure 6.2: Implementation of the Reverse Harmonic Blocking scheme

The reverse harmonic blocking scheme is implemented using both hardwired and IEC 61850 standard-based GOOSE message. To achieve the reverse harmonic blocking scheme, the SEL-487E and SEL-751A need to be configured using the given SELogic control Equations (6.1 to 6.8) to produce a blocking signal whenever the harmonic blocking element picks up an inrush condition on any one of the three phases.

To avoid relay mis-operation during inrush conditions the filtered differential element uses harmonics to either block or restrain the differential element. The SEL-487E relay blocks all the phases when the harmonic magnitude of any one of the three phases excesses the harmonic setting (SEL-487E Instruction manual, 2012). Even numbered harmonics (second and fourth) provide security during transformer energisation, while fifth-harmonic provides security for overexcitation conditions. Harmonic blocking and harmonic restraint provide a good balance between speed and security. The harmonic blocking element includes common (cross) second and fourth harmonic blocking and independent fifth harmonic blocking for improved security.

To verify the performance of the reverse harmonic blocking scheme, the scheme is implemented as depicted in Figure 6.3 below.

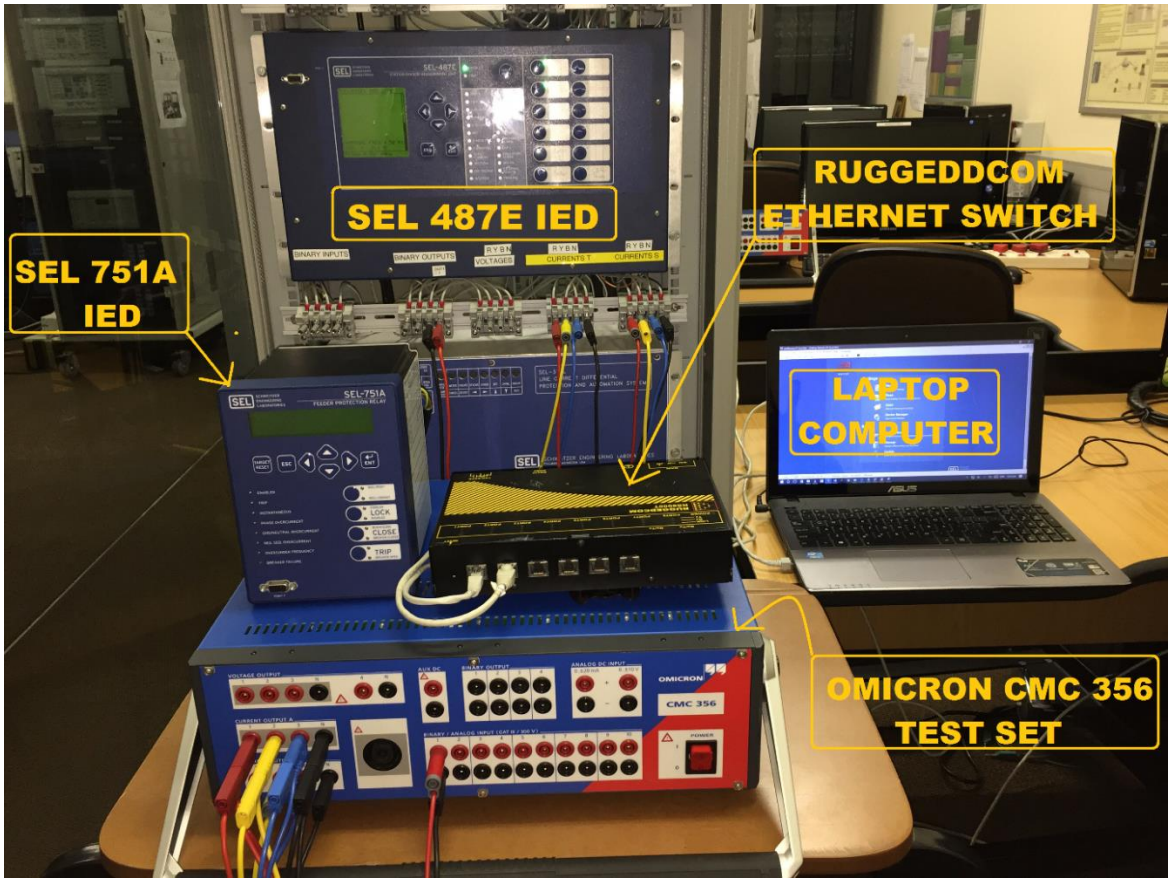


Figure 6.3: Test bench setup for the Reverse Harmonic Blocking scheme at CPUT CSAEMS lab

The developed SELogic equations to provide the reverse harmonic blocking scheme is discussed in the next section.

6.3 Developed SELogic control equations for the reverse harmonic blocking scheme

This section describes the developed SELogic control equations of the reverse harmonic blocking scheme.

6.3.1 Developed SELogic Control Equations in SEL-487E IED for either harmonic blocking or restraint due to inrush conditions

In order for the SEL 487E to generate a reverse harmonic blocking signal, the following SELogic control equations (6.1 to 6.3) were created in AcSELerator Quickset:

$$PLT32S = 87AHB\ OR\ 87AHR\ OR\ 87BHB\ OR\ 87BHR\ OR\ 87CHB\ OR\ 87CHR\ OR\ 87XBK2 \quad (6.1)$$

$$PLT32R = TRGTR \quad (6.2)$$

$$PSV01 = PLT32 \quad (6.3)$$

The graphical logic representation of this free-form SELogic control equations (6.1 to 6.3) is shown in Figure 6.4.

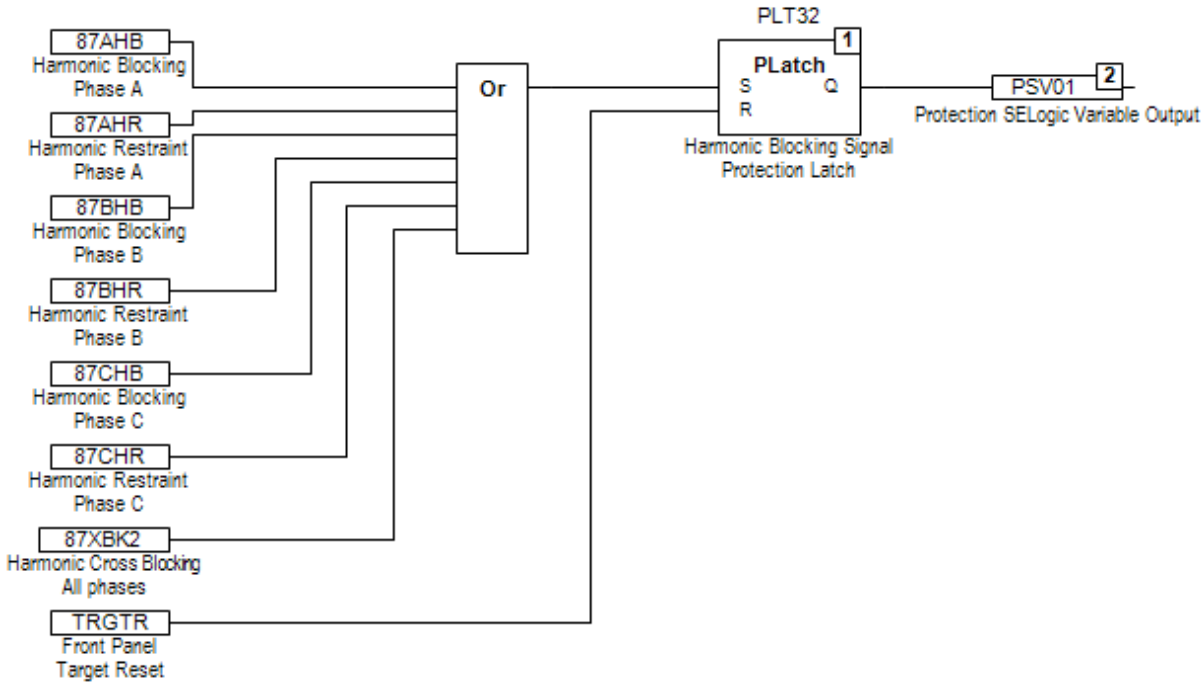


Figure 6.4: Developed SELogic control equations in SEL-487E for harmonic blocking/restraint differential

From the Figure 6.4, it is discernible that any asserted phase harmonic restraint or blocking elements (87HB or 87HR) will set the protection latch PLT32, which asserts the protection SELogic variable PSV01. The protection latch PLT32 is used to latch in the harmonic signal because either harmonic blocking or restraint elements (87HB or 87HR) do not assert continuously. The status value of the protection SELogic variable PVS01 is transmitted as the reverse blocking signal as shown in Figure 6.4.

Table 6.1 provides the description of the relay word bits used to create the reverse harmonic blocking scheme given in Figure 6.4.

Table 6.1: Relay Word Bits used for the reverse harmonic blocking scheme

Abbreviation (Relay Word Bits)	Description of the relay word bits
87AHR	Harmonic restraint differential element picked up A
87AHB	Harmonic blocking differential element picked up A
87BHR	Harmonic restraint differential element picked up B

87BHB	Harmonic blocking differential element picked up B
87CHR	Harmonic restraint differential element picked up C
87CHB	Harmonic blocking differential element picked up C
87XBKR	Harmonic Cross blocking picked up
TRGTR	Target reset
PSV01	Protection SELogic Variable 01 asserted
51P1TC	Phase-Inverse Time overcurrent torque control stage 1
51N1TC	Neutral-Inverse Time overcurrent torque control stage 1
50P2TC	Phase-Definite Time overcurrent torque control stage 2
50N2TC	Neutral-Definite Time overcurrent torque control stage 2
IN101	Input port 101 asserted
VB001	Virtual Bit 1 asserted

6.3.2 Implementing the developed SELogic control equations to prevent the tripping of the SEL-751A IED during TMIC using hardwired and IEC 61850 GOOSE message based reverse harmonic blocking scheme

In order to restrain the SEL 751A overcurrent IED from tripping during transformer inrush condition upon receipt of the blocking signal from SEL-487E, the following SELogic control equations are created in AcSELerator Quickset:

$$51P1TC = NOT\ (IN101\ OR\ VB001) \quad (6.4)$$

$$51N1TC = NOT\ (IN101\ OR\ VB001) \quad (6.5)$$

$$50P2TC = NOT\ (IN101\ OR\ VB001) \quad (6.6)$$

$$50N1TC = NOT\ (IN101\ OR\ VB001) \quad (6.7)$$

$$OUT102 = NOT\ (IN101\ OR\ VB001)\ AND\ (51P1T\ OR\ 51N1T\ OR\ 50P2T\ OR\ 50N2T \quad (6.8)$$

The torque control elements 51P1TC, 51N1TC, 50P2TC and 50N2TC, are used to interlock the 51P, 51N, 50P and 50N elements and avert them from asserting during inrush conditions as shown in Figure 6.5. Under normal conditions (no TMIC) the control input IN101 and the virtual bit VB001 carry a logical value of 0. Applying this logical state to a NOT gate produces a high logical state, which guarantees that the torque-controlled elements 51P, 51N, 50P, and 50N can still assert if a fault occurs on the system. Output 102 is also interlocked to the reverse blocking signal to ensure that no other element of the SEL-751A IED can energise this output and pass a trip signal onto the circuit breaker during inrush conditions.

The graphical logic representation of these free-form SELogic control equations is shown in Figure 6.5.

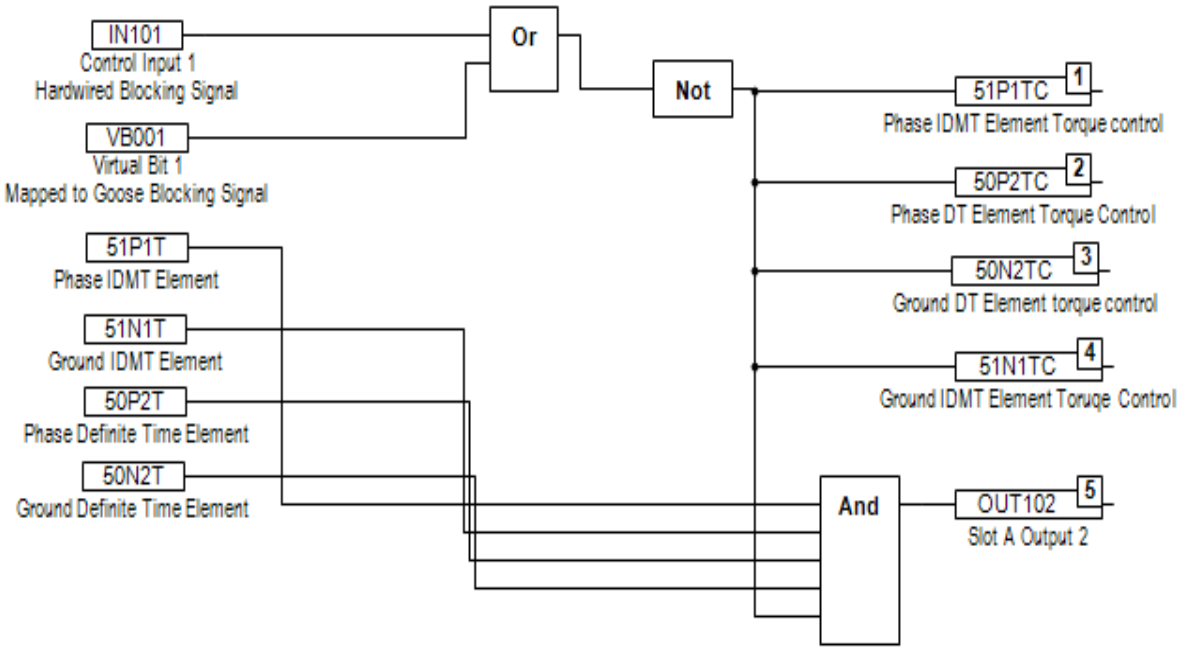


Figure 6.5: Developed SELogic control equations in SEL-751A for the implementation of the Reverse Harmonic Blocking scheme

Next section discusses the reverse harmonic blocking scheme algorithm for the transformer.

6.4 Algorithm to implement the reverse harmonic blocking scheme using hardwired and IEC 61850 standard-based GOOSE message

SEL-751A IED does not have an inbuilt function for harmonic blocking so whenever the power transformer energises, the TMIC asserts 50 & 51 elements of the backup protection IED SEL-751A as shown in Figures 6.1 and 6.2. To block the 50 & 51 elements from tripping during TMIC condition, reverse harmonic blocking scheme algorithm is implemented using hardwired, and IEC 61850 standard-based GOOSE message and is described in detail in this section.

Steps to implement the reverse harmonic blocking scheme algorithm using IEC 61850 standard-based GOOSE message are as follows:

1. SEL-487E power transformer IED performs a Discrete Fourier Transform (DFT) signal processing using input current signals from the current transformers CT2 and CT3 connected to S and T windings respectively as shown in Figure 6.1.

2. Calculate the internal protection function on SEL-487E using DFT signals from step 1.

3. For internal faults on the power transformer, the corresponding relay word bit 87T is asserted. SEL-487E performs the second-harmonic ratio calculation in the differential currents, for internal faults obviously the 2nd harmonic will be less than the threshold setting value. Relay sends a trip signal to the circuit breakers CB1 and CB2 across the power transformer as shown in Figure 6.1.

4. During TMIC conditions, SEL-487E performs the second-harmonic ratio calculation again. If the 2nd harmonic primary current exceeds its pickup setting, then the harmonic blocking elements (87HB and 87HR) are asserted and restrain the relay from tripping.

5. After successful completion of step 4, SEL-487E transfers a magnetizing inrush blocking (87HB) signal as protection SELogic variable (PSV01) to SEL-751A IED using hardwired and IEC 61850 standard-based GOOSE message.

6. SEL-751A overcurrent IED performs a Discrete Fourier Transform (DFT) signal and processing using the input currents from the current transformer CT1 connected at the primary side of the power transformer. SEL-751A is used as a backup protection for the power transformer SEL-487E IED as shown in Figure 6.1.

7. SEL-751A IED checks whether phase definite-time overcurrent (50) or phase time-overcurrent (51) elements are asserted for internal events.

8. For internal faults described in step 7 on the protection zone of the power transformer, the corresponding relay word bits 50T or 51T is asserted and the circuit breaker CB1 connected at the primary of the power transformer clears the faults as shown in Figure 6.1.

9. However, during TMIC condition SEL-751A receives the magnetizing inrush blocking signals transferred by SEL-487E from step 5 in order to de-assert the relay word bits 50 and 51 from tripping.

10. The transfer of magnetizing inrush blocking signal is implemented using hardwired DC signals which are mapped to the input (IN101) as shown in Figure 6.2 and IEC 61850 standard-based GOOSE message which is mapped to virtual bit (VB001) as shown in Equation (6.8) and the diagram shown in Figure 6.18. Output 102 is interlocked to the reverse blocking signal

to ensure that either 50 or 51 elements of the SEL-751A IED cannot energise the output (OUT102).

11. Finally, the protection speed, reliability and performance of the reverse harmonic blocking scheme is analysed using hardwired and IEC 61850 standard-based GOOSE message.

A flowchart for the reverse harmonic blocking scheme algorithm is depicted in Figure 6.6 below.

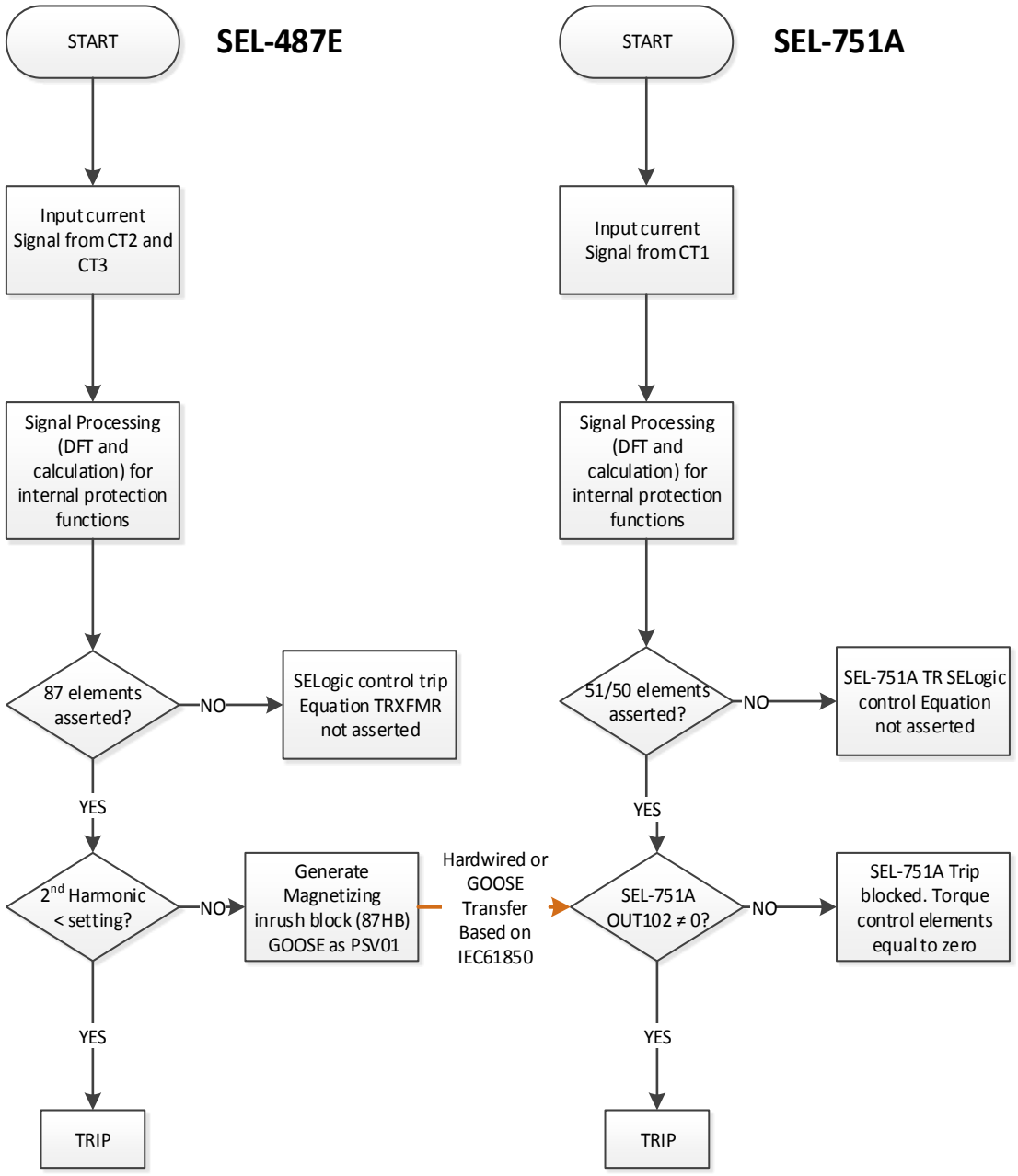


Figure 6.6: Flowchart for the reverse harmonic blocking scheme

Two case studies are considered, one with the scheme implemented using traditional hardwiring and other with IEC 61850 standard-based GOOSE message replacing the traditional hardwiring. The results of each case study are presented and discussed in the next sections of this chapter.

6.5 Analyse of the hardwired simulation test results of the reverse harmonic blocking scheme

The following two case studies are investigated, they are:

1. Case study one – Investigation of the malfunction of the SEL-751A IED due to TMIC
2. Case study two – Application of the reverse harmonic blocking scheme to prevent malfunctioning of the SEL-751A due to TMIC

6.5.1 Case study one: Investigation of the malfunction of the SEL-751A IED due to TMIC

This case study aims to investigate the performance of the SEL 751A overcurrent relay installed on the upstream of the network during transformer magnetisation inrush current conditions. The SEL-751A IED is tested without the implementation of the developed reverse harmonic blocking scheme.

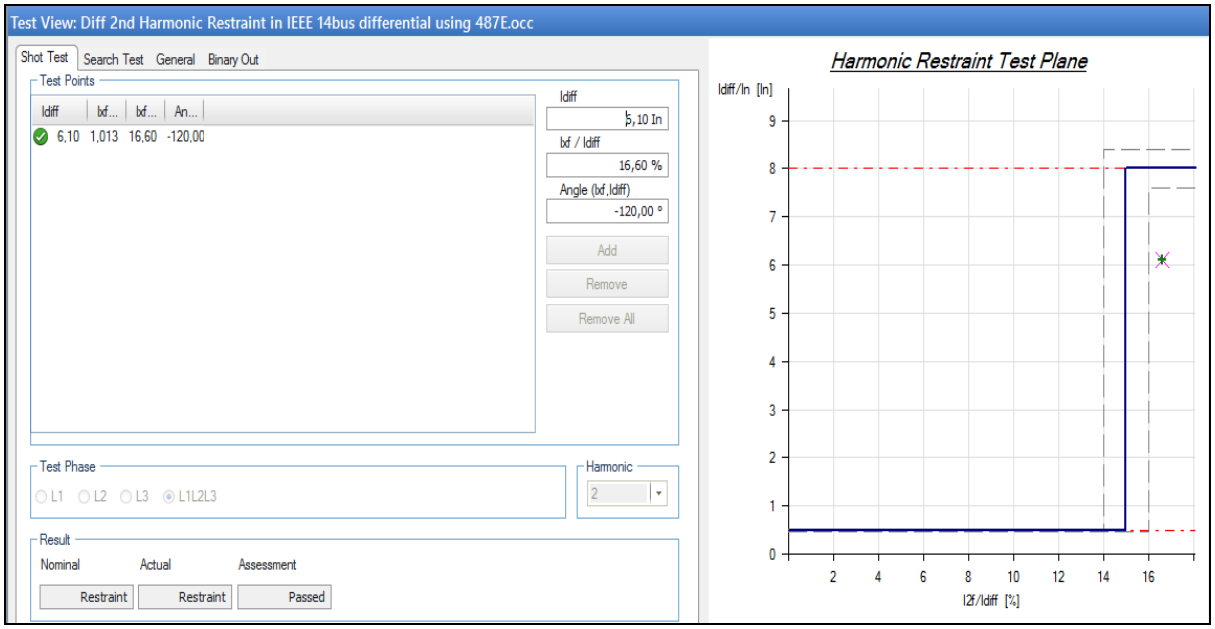


Figure 6.7: Second harmonic test results from in Omicron test universe

There is a high harmonic content in the inrush currents; however, the fault currents have less harmonic contents that are less than 15%. Therefore, the way to test the inrush current condition is by generating differential currents with harmonic content above 15%. The omicron CMC 356 test set is used to inject currents with a 2nd

harmonic level percentage of 16.60% into the IEDs (SEL-487E and SEL-751A) as shown in Figure 6.7.

The pickup differential current is set to 0.5 A and CT ratio set to 400A at the primary side of the power transformer, the test factor selected is 6.10 times the nominal current (6.10 X 400A) = 2440A.
Therefore, the Omicron second harmonic simulation currents for L1-L2-L3 to be injected to the IEDs is (2440A X 0.5) = 1220A.

The results obtained from the hardwired simulation test are presented in Figure 6.8a and 6.8b respectively. Figure 6.8a shows that 16.60% of the 2nd harmonic currents injected in both IEDs (SEL-487E and SEL-751A), in which SEL-751A IED picks up this injected 2nd harmonic current as a fault by asserting inverse time-overcurrent (51P1P) and FAULT elements at 5.95 seconds.

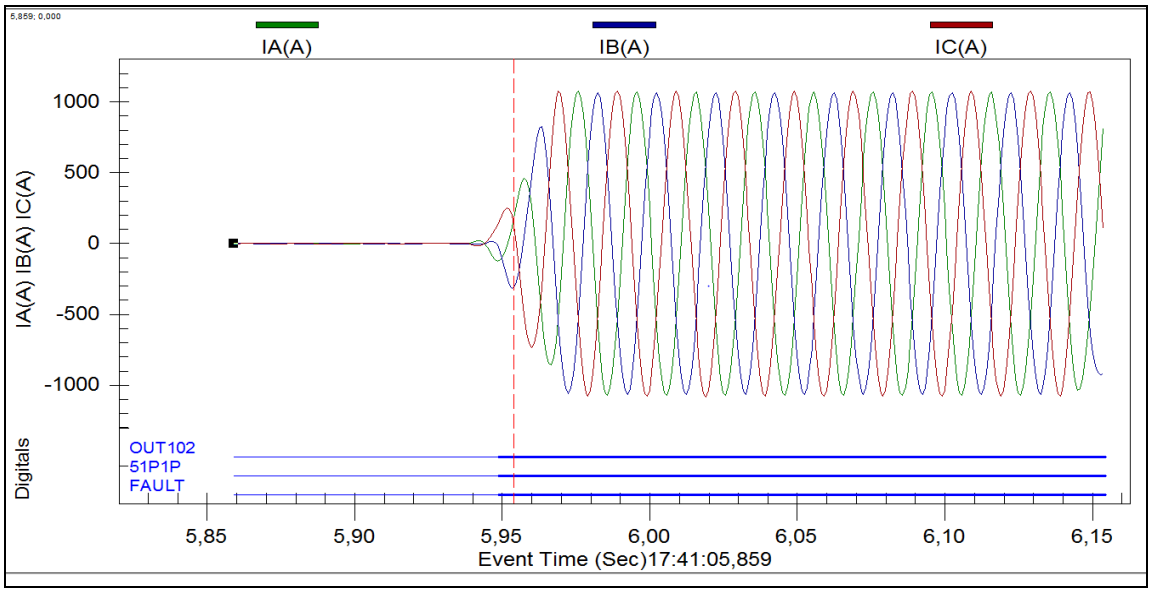


Figure 6.8a: SEL-751A current signals during transformer inrush current condition

In Figure 6.8b, shows that the inverse definite minimum time element 51P1 of SEL 751A overcurrent relay asserted for the 2nd harmonic inrush current which produces a trip signal (51P1T) at 0.36s (6.31s – 5.95s = 0.36s). It is also evident from the Figure 6.8b that no blocking signal sent to SEL-751A IED from SEL-487E in order to restrain the TRIP and 51P1T elements due to TMIC conditions.

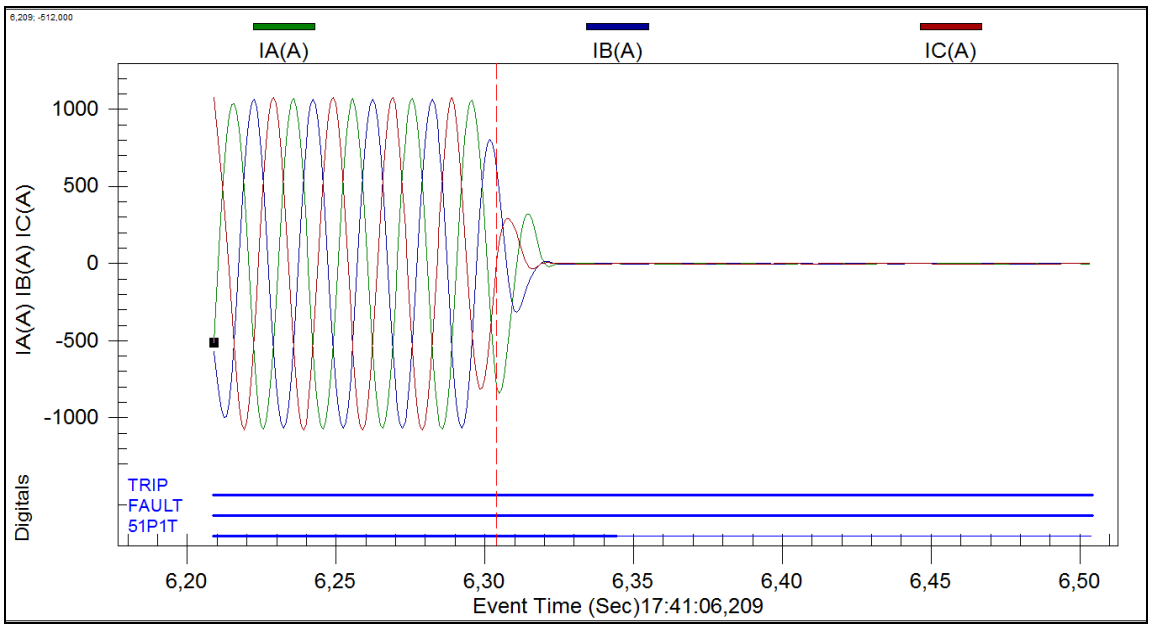


Figure 6.8b: SEL-751A trip signal during transformer inrush current condition

6.5.2 Case study two: Application of the reverse hardwired harmonic blocking scheme to prevent malfunctioning of the SEL-751A due to TMIC

The aim of this study case is to investigate the reverse harmonic blocking scheme during transformer inrush conditions. This scheme uses a 110V DC signal looped between SEL 751A and SEL 487E IEDs as shown in Figure 6.9. The 110V DC signal is wired in series with the normally open output contact OUT102 of the SEL 487E as shown in Figure 6.9. The normally open output 102 of the SEL 487E is mapped to the protection SELogic variable PSV01 and transition to a closed position and pass the blocking signal to the control input CCIN101 of the SEL 751A when PSV01 asserts.

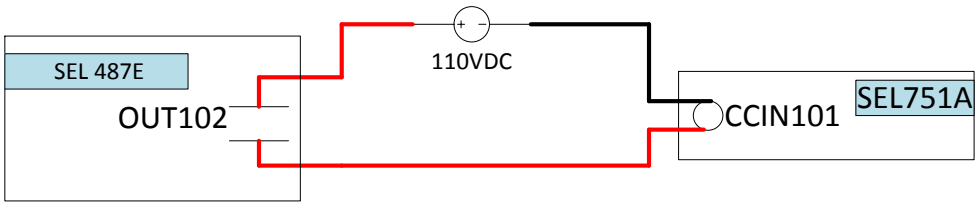


Figure 6.9: Reverse harmonic blocking signal wiring diagram

As shown in Figure 6.9, the relay is tested with the developed reverse harmonic blocking scheme. The omicron CMC 356 test set is used to inject differential currents with 16.60% of 2nd harmonic content into the IEDs. The results obtained from the hardwired test simulation is given in Figure 6.10a and Figure 6.10b respectively.

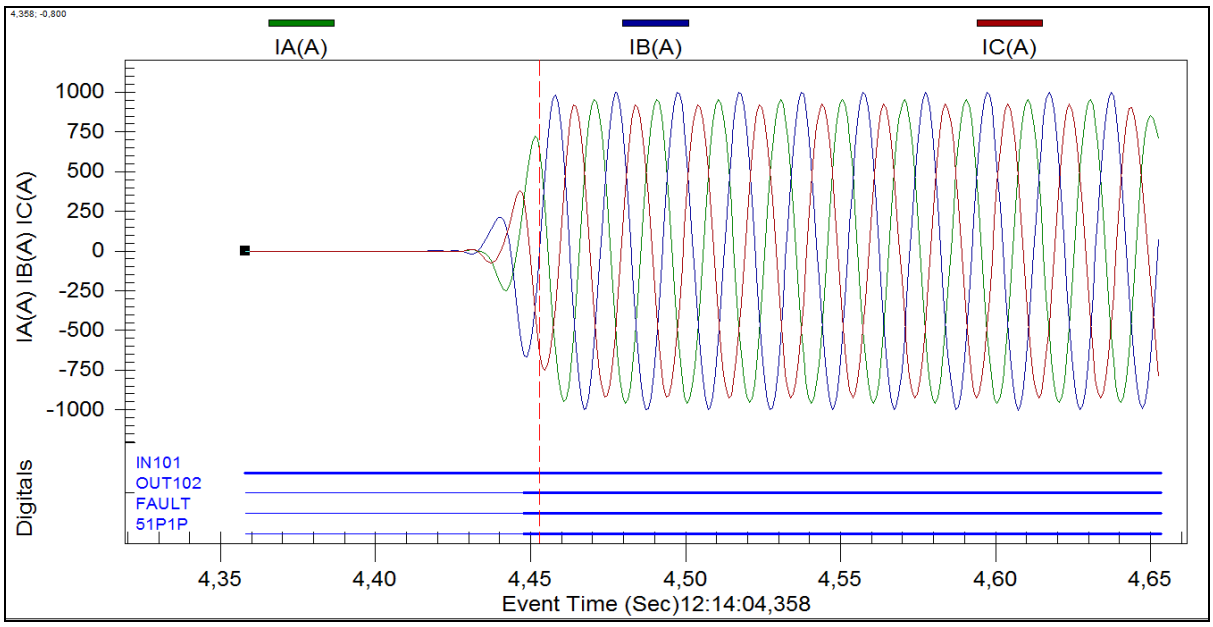


Figure 6.10a: SEL-751A recorded signals during inrush current conditions

Figure 6.10a shows that 16.60% of the 2nd harmonic currents injected in both IEDs (SEL-487E and SEL-751A), in which SEL-751A IED picks up this injected 2nd harmonic current as a fault by asserting inverse time-overcurrent (51P1P) and FAULT elements at approximately 4.45 seconds.

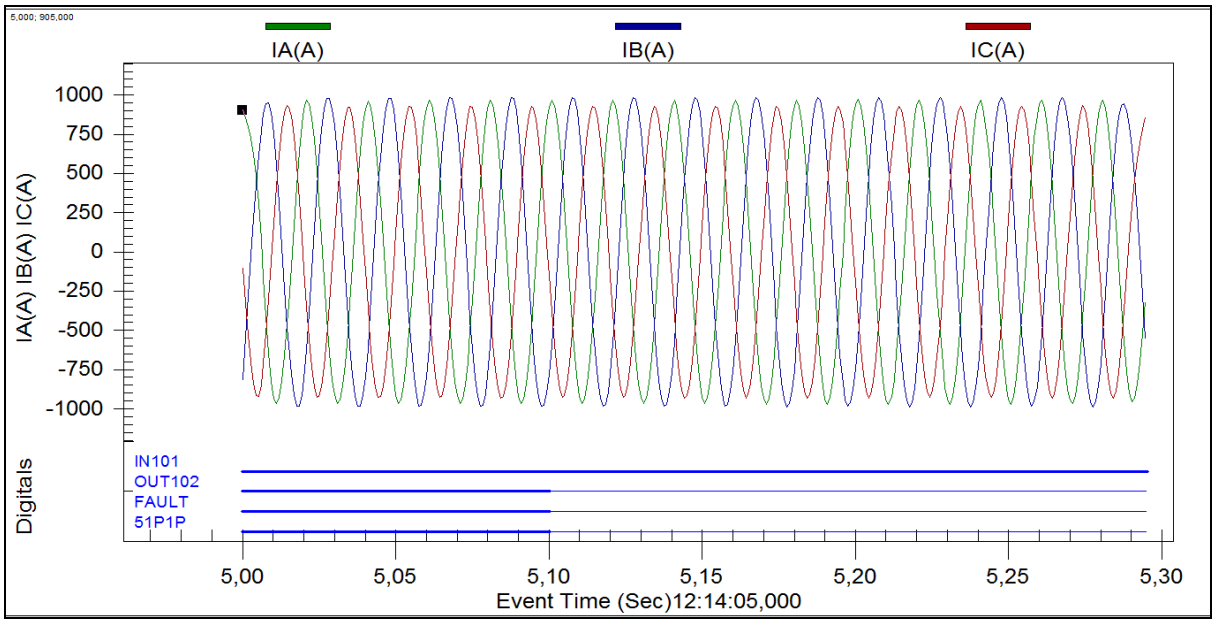


Figure 6.10b: SEL-751A overcurrent relay response during transformer inrush current conditions

Figure 6.10b shows that the pickup elements 51P1P and FAULTS are de-asserted at 5.10 seconds, and the SEL-751A relay does not produce any trip signal. This is because the overcurrent elements are being blocked from asserting by the reverse

blocking signal being received through control input IN101. The results of this test also indicate that the malfunctioning caused by transformer magnetisation inrush currents can be prevented by implementing the reverse harmonic blocking scheme.

6.6 IEC 61850 standard for the substation communication

This section provides the introduction to the IEC 61850 standard, IEC 61850 architecture for substation communication, a structure of the manufacturing message specification, IEC 61850 data models and logical nodes and IEC 61850 standard-based GOOSE message.

6.6.1 Introduction to the IEC 61850 standard for substation communication

In the early 1990s, the Institute of Electrical and Electronics Engineers (IEEE) and the Electric Power Research Institute (EPRI) began work on the definition of a Utility Communications Architecture (UCA). The main focus was centred around the inter-control centre and substation-to-control centre communications, through years of extensive research Inter-Control Centre Communications Protocol (ICCP) was introduced. The ICCP later adopted by the IEC as 60870-6 TASE 2 became the standard protocol for real-time data exchange between different databases (SEL-487E instruction manual, 2012). With UCA in place, the IEEE and EPRI began work on UCA 2.0, which later was turned into IEC 61850 through combined efforts of IEC technical committee 57. The IEC 61850 standard describes client-server and peer-to-peer communications, substation design and configuration, project standards and testing.

The motive behind IEC61850 is interoperability between devices from like or dissimilar vendors through a standard communications link. The standard provides a platform for different devices within a substation to share information relating to protection functions, monitoring, and control of the substation. IEC 61850 furthermore makes it possible to digitalise the whole substation without the need for communication gateways, allowing for added redundancy while reducing commissioning costs and maintenance time (SEL-487E Instruction manual, 2012).

6.6.2 IEC 61850 architecture for substation communication

The station and process bus consist of communication network switches linked with optical or electrical signals to form active communication elements. The switches used on the station or process bus have to support the definition of virtual private local area networks (VPLANs), priority tagging and time synchronisation.

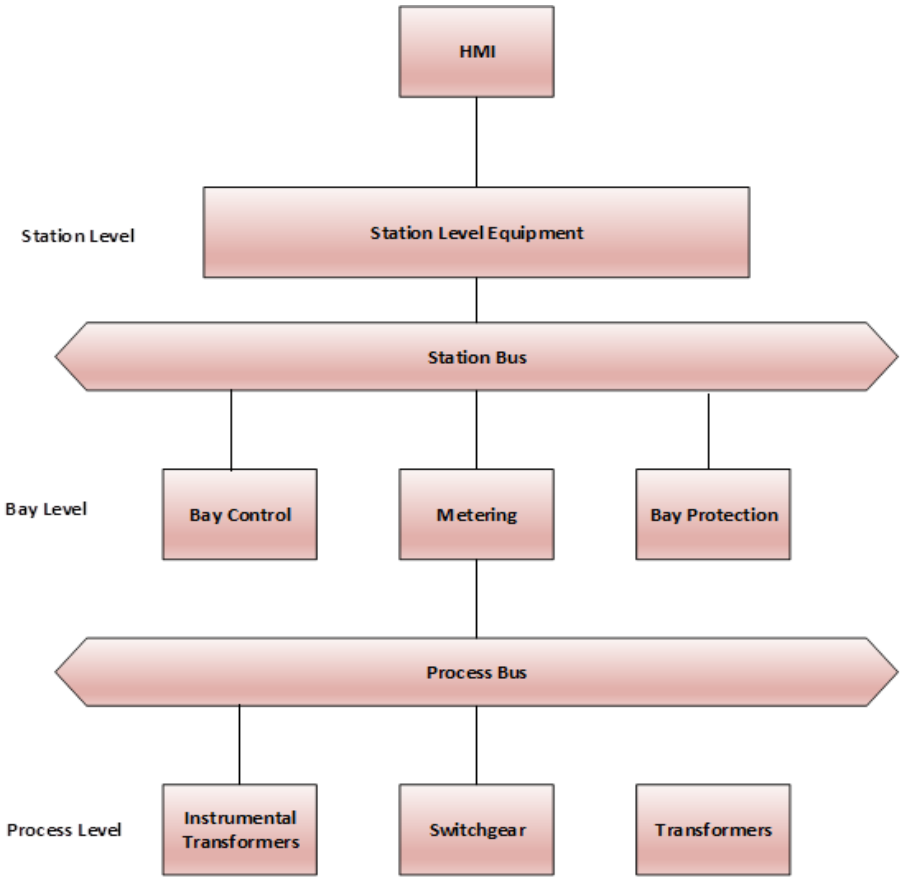


Figure 6.11: IEC 61850 architecture for substation communication

Intelligent electronic devices are then linked to each other via switches direct the flow of traffic on the LAN. The basic idea in IEC 61850 is to have an architecture with 3 levels as depicted in Figure 6.11 above.

The station bus defined in part 8 of the IEC 61850 is intended for communications between station and Bay level. Similarly, the process bus defined in IEC 61850-9 is intended for the communication between bay and process level.

6.6.3 Manufacturing Message Specification (MMS) in IEC 61850 standard

MMS developed as a network independent data exchange protocol in the 1980s and provides services for the application-layer transfer of real-time data within a substation LAN (SEL-487E instruction manual, 2012). Technically IEC 61850 can be mapped to any protocol, but it can become very complicated to map objects and services to a protocol that only provides access to simple data points through registers or index numbers. MMS on the other hand, however, supports complex named objects and flexible services that make the mapping to IEC 61850 in a straightforward manner. It is for this reason that IEC chose to keep Manufacturing messaging specification in the IEC 61850 standard (SEL-487E instruction manual,

2012). MMS is an international standard (ISO 9506) dealing with the messaging system for transferring real-time process data and supervisory control information between networked devices and/or computer applications as shown in Figure 6.12.

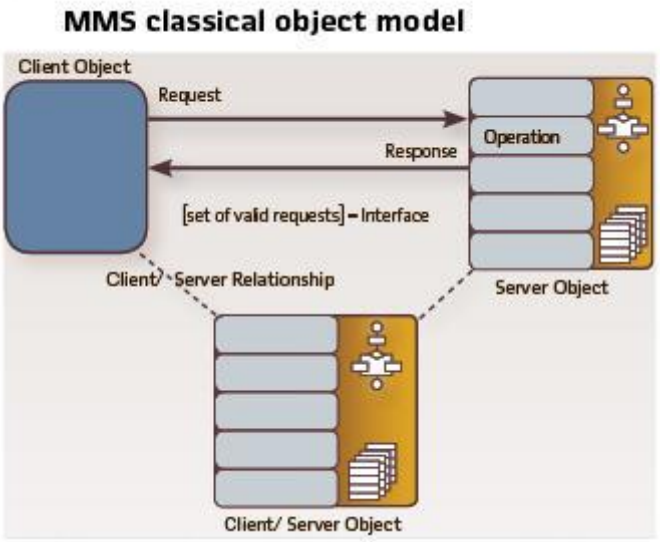


Figure 6.12: MMS object model (Walter Schossig and Thomas Schossig, 2016)

6.6.4 IEC 61850 data models and logical nodes

To achieve interoperability, all data in the data model need a strong definition with regards to syntax and semantics of the data which is mainly provided by the names assigned to logical nodes and the data they contain (International Standard, 2003). To ensure that all device vendors conform to a common way of defining data models, the IEC 61850 standard was adopted, and it dictates how data models are defined. The IEC 61850 standard relies strongly on Abstract Communications Service Interface (ASCI) for the definition of substation control, monitoring and protection services and responses to these services. In terms of power system networks, abstract modelling provides a platform for different Intelligent electronic devices to behave identically and also for the creation of data items according to the Common Data Class (CDC) specification in section 7-3 of the IEC 61850 standard which describes the type and structure of each element within a logical node. Each CDC has a unique attribute, and each CDC attribute belongs to a set of functional constraints that group the attributes into specific categories namely substituted value (SV), description (DC) and status (ST) (SEL-487E instruction manual, 2012).

IEC 61850 being a superset of UCA2 means that it contains most of the UCA2.0 specifications such as GOMSEF (Generic Object Models for Substation and Feeder Equipment) plus added functionality. GOMSEF was used in UCA 2.0 to broadcast

data from different intelligent electronic devices in the power system network as a series of models or bricks. GOMSEF was however integrated into 61850 with a few modifications to the terminology, one of which involved renaming the data objects from bricks to logical nodes.

Each logical node houses a group of data associated with a specific function. This data may be of protection, controls, or simply measurements type. For example, logical node IN1GGIO14 contains data regarding the status and behaviour of inputs 1N101 to 1N107. Figure 6.13 below depicts an example of an XCBR logical node.

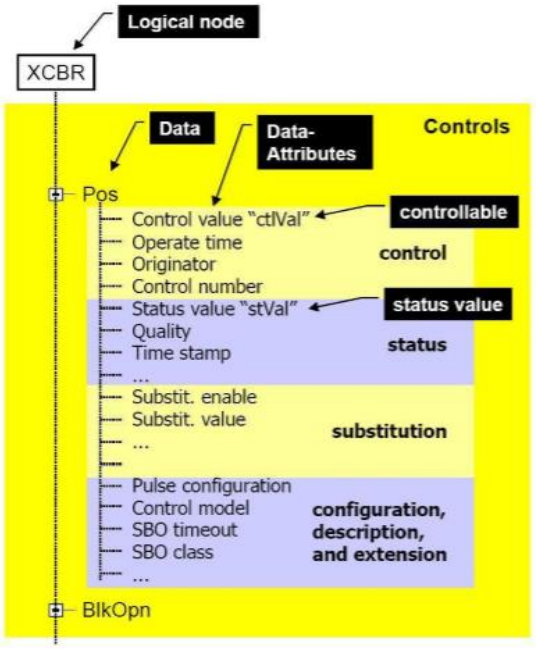


Figure 6.13: IEC 61850 circuit breaker (XCCBR) logical node (Apostolov A., 2016)

In Figure 6.13, a circuit breaker is modelled as logical node XCBR with an array of data such as Pos which contains information about the circuit breaker position, BlkOpn which contains circuit breaker opening instructions, OpCnt containing the breaker operations count data etc.

Logical nodes can be grouped into logical devices and logical devices into physical devices as depicted by the IEC 61850 hierarchy in Figure 6.14. In summary, each physical device can contain many logical devices which in turn contain many logical nodes.

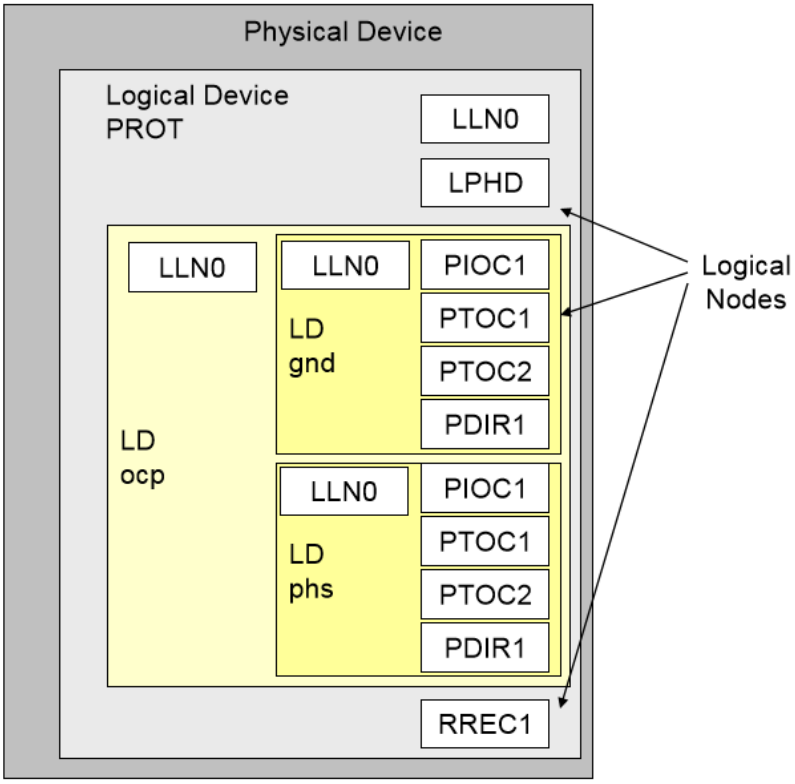


Figure 6.14: IEC 61850 hierarchy (Apostolov A., 2016)

IEC 61850 devices have the capability of self-description, which means that the user does not need to refer to the specification for the logical nodes, measurements and other components in order to request data from another IEC 61850 compliant device (SEL-487E instruction manual, 2012). An IEC 61850 can simply query another IEC 61850 device and receive a description of all logical devices, logical nodes and available data. In IEC 61850, data is presented with descriptors in a composite notation made up of components as shown in Figure 6.15.

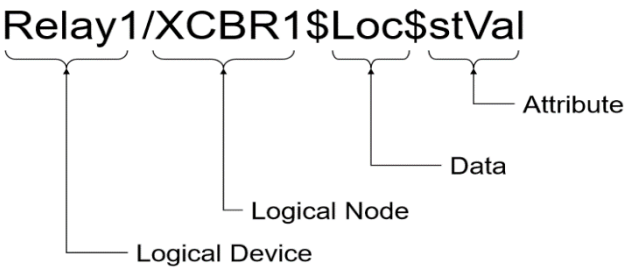


Figure 6.15: IEC 61850 data descriptor

Figure 6.15 shows that the name of the device is Relay 1 and the next part shows the logical node. The first letter ‘X’ represents the group of the node which according to IEC 61850-7-4 is switchgear. The logical node XBR has a reference number ‘1'

which refers to circuit breaker 1. Similarly, XBR2 would indicate circuit breaker 2. The data object Loc indicates local control mode of the circuit and the value is contained in stVal (Adamiak M. et al., 2009).

Table 6.2 from the IEC 61850-7-4 shows the logical node groupings according to group designators.

Table 6.2: IEC 61850 logical node groups

Group indicator	Logical node groups
A	Automatic control
C	Supervisory control
G	Generic function references
I	Interfacing and archiving
L	System logical nodes
M	Metering and measurement
P	Protection functions
R	Protection related functions
S	Sensors and monitoring
T	Instrument transformers
X	Switchgear
Y	Power transformer and related functions
Z	Further (power system) equipment

6.6.5 IEC 61850 standard-based GOOSE messages

The Generic Object-Oriented Substation Event (GOOSE) is used for high-speed control messaging (SEL-487E instruction manual, 2012). GOOSE is messaging to be employed in substation automation and control, it has to perform the functions of hardwiring using a LAN connection. The GOOSE sender publishes the GOOSE message as a multicast message onto the LAN, meaning that it is not addressed to a specific IED; thus, any intelligent electronic device on the network can subscribe to it (Cossio M.L.T et al., 2012). The subscriber (GOOSE receiver) does not confirm receipt of the message, nor does the publisher requests for confirmation. It is for this reason that the GOOSE is published several times continuously to increase the likelihood of other devices on the network receiving it.

Each GOOSE publisher on the IEC 61850 network attaches an Ethernet multicast group address and a text identification string or goose control block as commonly

known onto every outgoing message (SEL-487E instruction manual, 2012). For a protection scheme to function properly the intelligent electronic devices on the network have to update their contact status and analogue values every few milliseconds (Cossio M.L.T et al., 2012). This, therefore, means that every publisher (GOOSE sender) needs to repeat the latest updated goose message numerous times. The publisher will continue publishing the multicast message onto the network but with a long-time interval. Should a status change occur in the data within a certain dead band, a GOOSE update is sent out instantaneously. Figure 6.16 depicts the transmission of GOOSE messages.

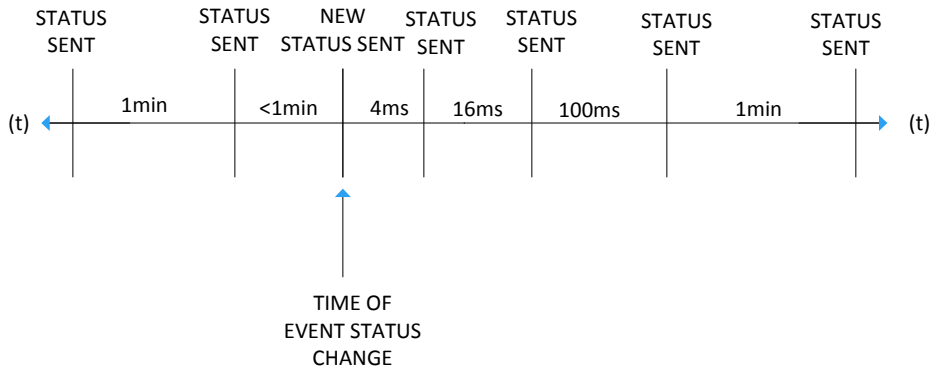


Figure 6.16: GOOSE message publication intervals

6.6.6 Substation Configuration Language and its file types

Substation Configuration Language (SCL) is an Extensive Markup Language (XML) based system used to support the exchange of database configuration data between different configuration tools, which may come from different vendors (SEL-487E instruction manual, 2012). Different types of SCL files exist, namely:

i. **IED Capability Description file (. ICD):** The ICD file describes the capabilities of an intelligent electronic device. It also contains information about the logical nodes and GOOSE support of the IED.
ii. **System Specification Description file (. SSD):** The SSD describes the substation single line diagram and the logical nodes required for the application
iii. **Substation Configuration Description file (. SCD):** The SCD file contains information about all the intelligent electronic devices in the substation, communications configuration data, and a substation description.

iv. **Configured IED Description file (. CID):** This file contains information including the address of a single configured intelligent electronic device within the project. At the end of the project, there may be a number of CID files available depending on the number of IEDs in the network.

The process of configuring an IEC 61850 network is depicted in Figure 6.17.

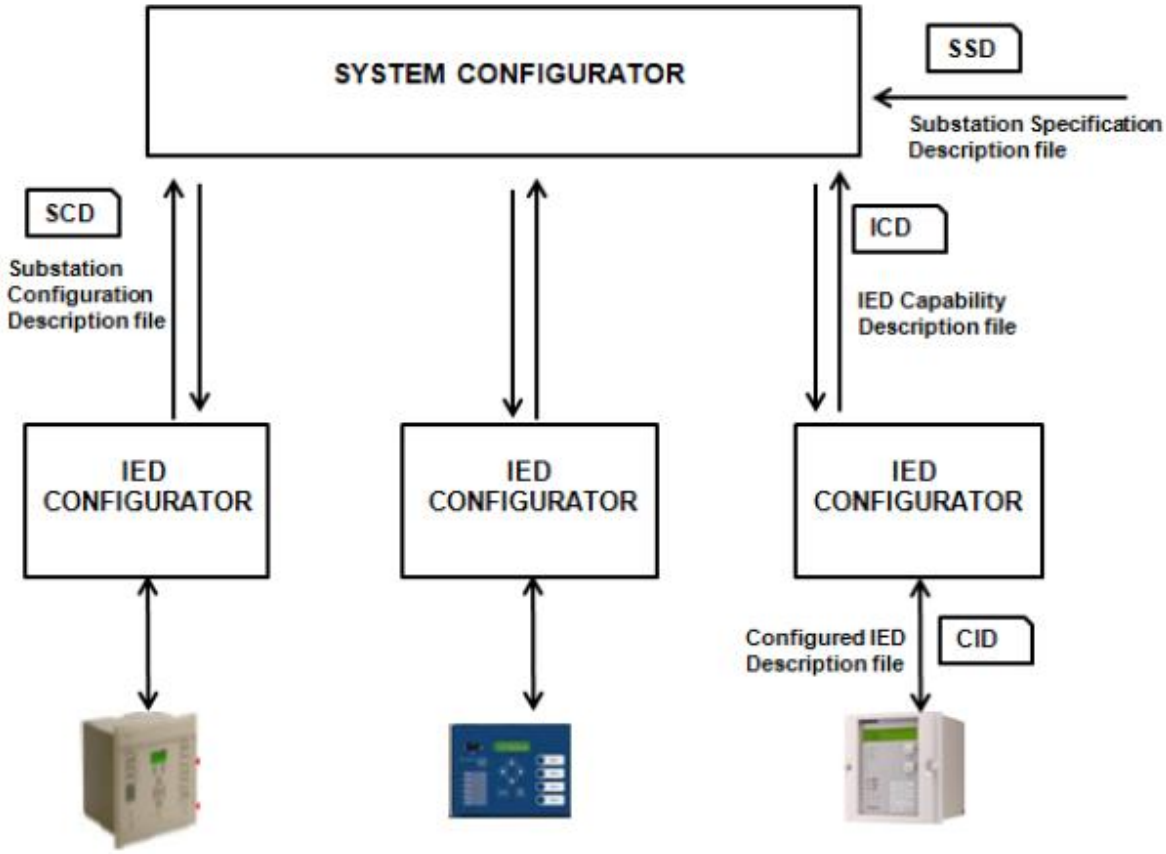


Figure 6.17: IEC 61850 configurator

The process begins with the extraction of the system and IED data from the SSD and ICD files. The system configurator will then create an SCD file, which consists of the functions and information transmission for each IED. The IED configurator then collects the SCD file and generates the CID file that incorporates the format suitable for the IED. The generated CID file is transmitted into the individual IED via a communication link.

6.7 Implementation of the reverse harmonic blocking scheme using IEC 61850 standard-based GOOSE message

Reverse harmonic blocking scheme test bench implementation the to prevent the operation of the SEL-751A overcurrent elements (51P1 & 50P1) during the transformer magnetizing inrush current conditions is given in Figure 6.18.

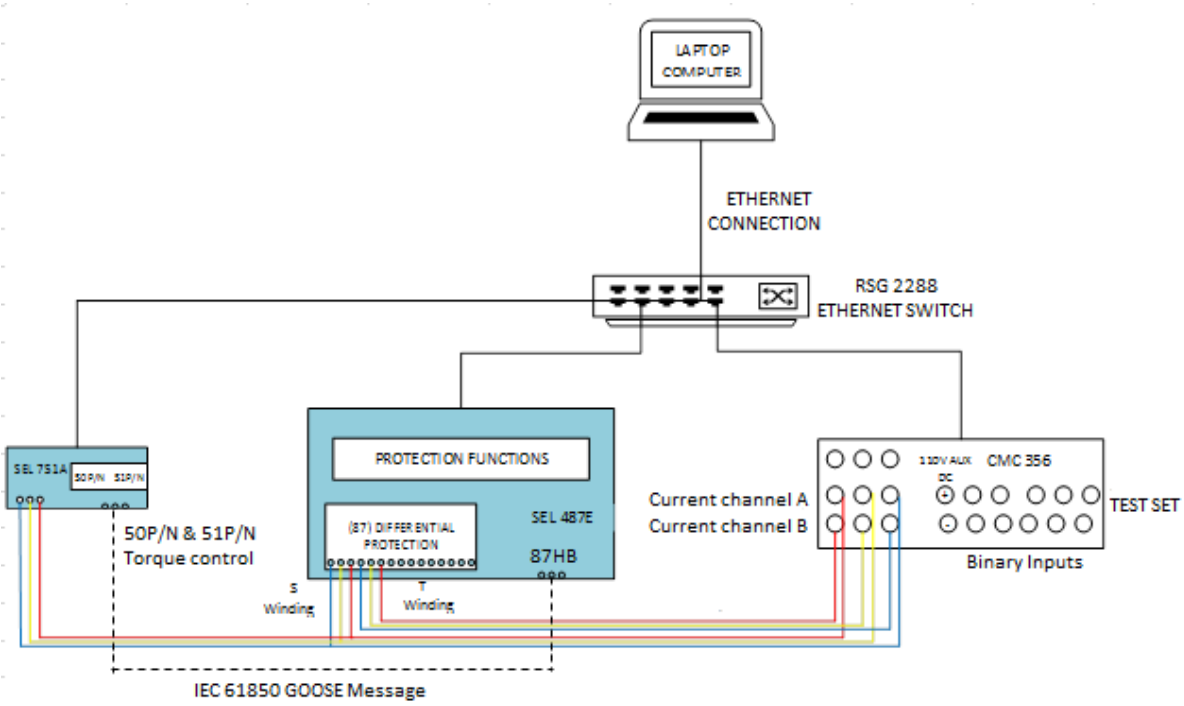


Figure 6.18: Implementation of the reverse harmonic blocking scheme using IEC 61850 standard-based GOOSE message

The Reverse harmonic blocking scheme based on IEC 61850 GOOSE is implemented as shown in Figure 6.18 above. In Figure 6.18, the omicron CMC356 test set is used to inject the inrush currents into the SEL 487E and SEL 751A IEDs. The S winding of the SEL 487E is connected in series with the SEL 751A current inputs. This is because the S winding and the SEL 751A backup overcurrent relay both monitor the primary winding of the protected transformer. The RUGGEDCOM Ethernet switch links the two protective IEDs with the personal computer and the CMC 356 test via a virtual local area network VLAN. The reverse harmonic blocking (87HB) signal is transmitted through Ethernet as a GOOSE message to block the torque control overcurrent elements as shown in Figure 6.18.

6.7.1 IEC 61850 GOOSE configuration to implement reverse harmonic blocking scheme

AcSELerator architect is a configuration tool for SEL devices for IEC 61850 GOOSE communication. AcSELerator Architect can be used to create and edit datasets, Generic Object-Oriented Substation Event GOOSE messages, configured IED description files and Substation Configuration Language files SCL. The main sections of the AcSELerator Architect configuration tool are shown in Figure 6.19.

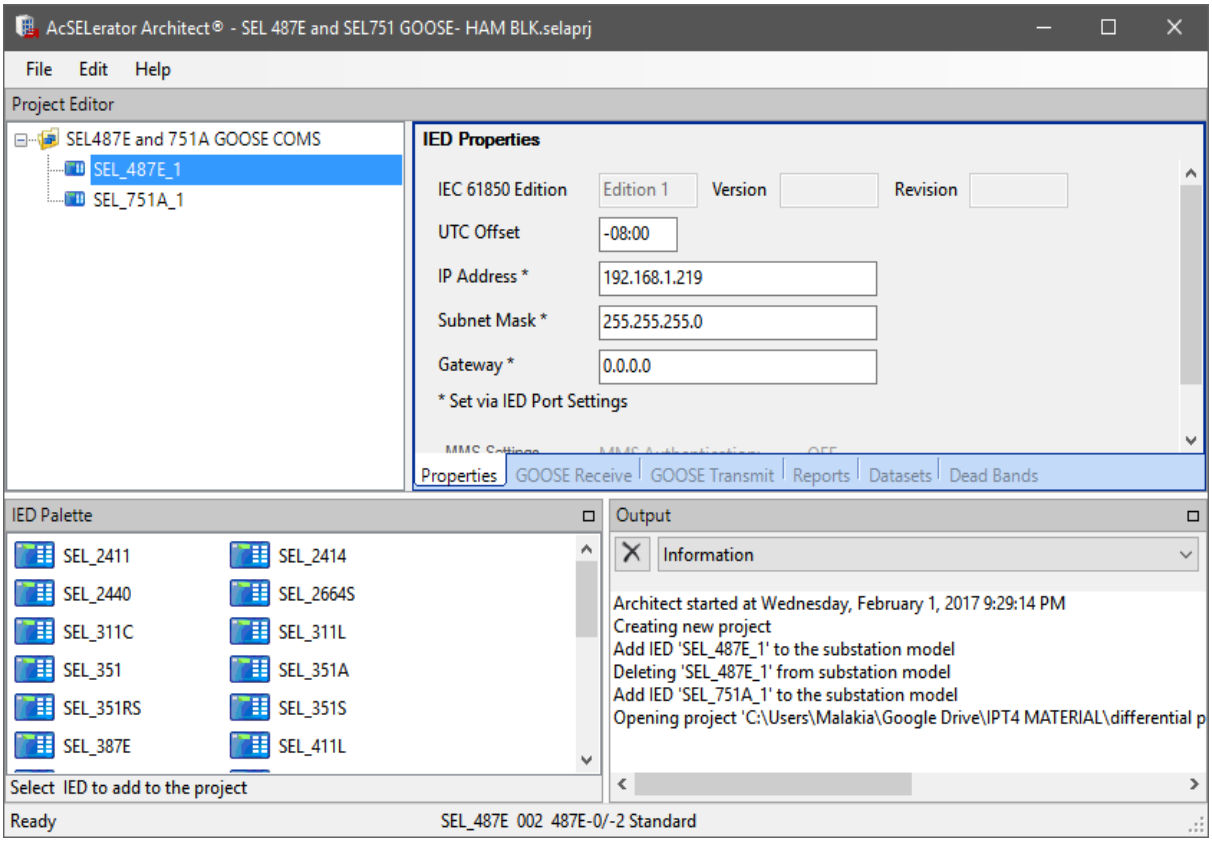


Figure 6.19: AcSELerator Architect IEC 61850 configuration tool

As shown in Figure 6.19, the main sections of the configuration tool are the project editor, IED Palette, and IED configurations tab. The IED Palette consists of a list of all SEL devices that are IEC 61850 compliant. To start a new project, a device is selected from the IED palette and dragged into the project editor. When a device has been successfully added to the project editor, the IED configuration window pops up. The IED configuration windows comprise of the IED properties, GOOSE receive configuration, GOOSE transmit configuration, Reports and Dead bands configuration tabs as shown in Figure 6.19.

To implement the harmonic blocking scheme, the SEL487E is configured to transmit a GOOSE message with the reverse harmonic blocking signal (87HB), and the SEL 751A is configured to subscribe to the GOOSE message. The steps involved in the IEC 61850 engineering configuration are described below:

Step 1: A new dataset for the SEL 487E is defined, under the Dataset configuration tab. There are 14 predefined datasets available that the user can choose from, however, for this application, a new dataset is created and assigned the name ‘SEL487E_87_BLOCK'. The name is chosen, such that it helps the user to easily identify the GOOSE message from the list of many

other data sets has been published. After the dataset has been created, a functional constraint that encompasses the required logical nodes needs to be assigned to it. For the harmonic blocking signal (87HB) to successfully restraint the SEL751A from malfunctioning during inrush conditions, the data attributes of the protection SELogic variable PSV01 needs to be published to the SEL 751A. The dataset ‘Ind001’ encompasses the data attributes of the SELogic variable PSV01 and is housed in the logical node ‘IN1GGIO14’, which falls under the Annunciation logical device ANN. The configured dataset is shown in Figure 6.20.

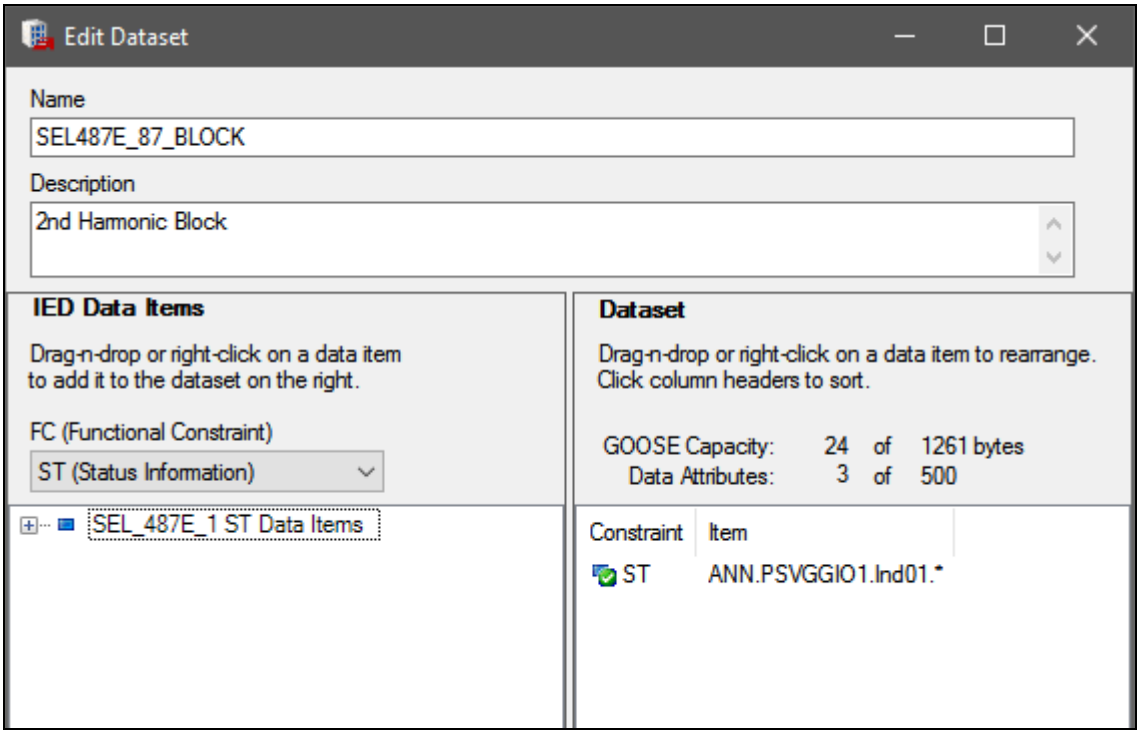


Figure 6.20: Configured dataset for SEL-487E

Step 2: SEL 487E IED able to transmit the required data, the datasets created in the previous step need to be mapped to a GOOSE control block as shown in Figure 6.21. A new GOOSE control block can be created under the GOOSE transmit tab, or the existing predefined one can be used. For this application, a new GOOSE control block was created and assigned the name ‘SEL487E_87_BLK'.

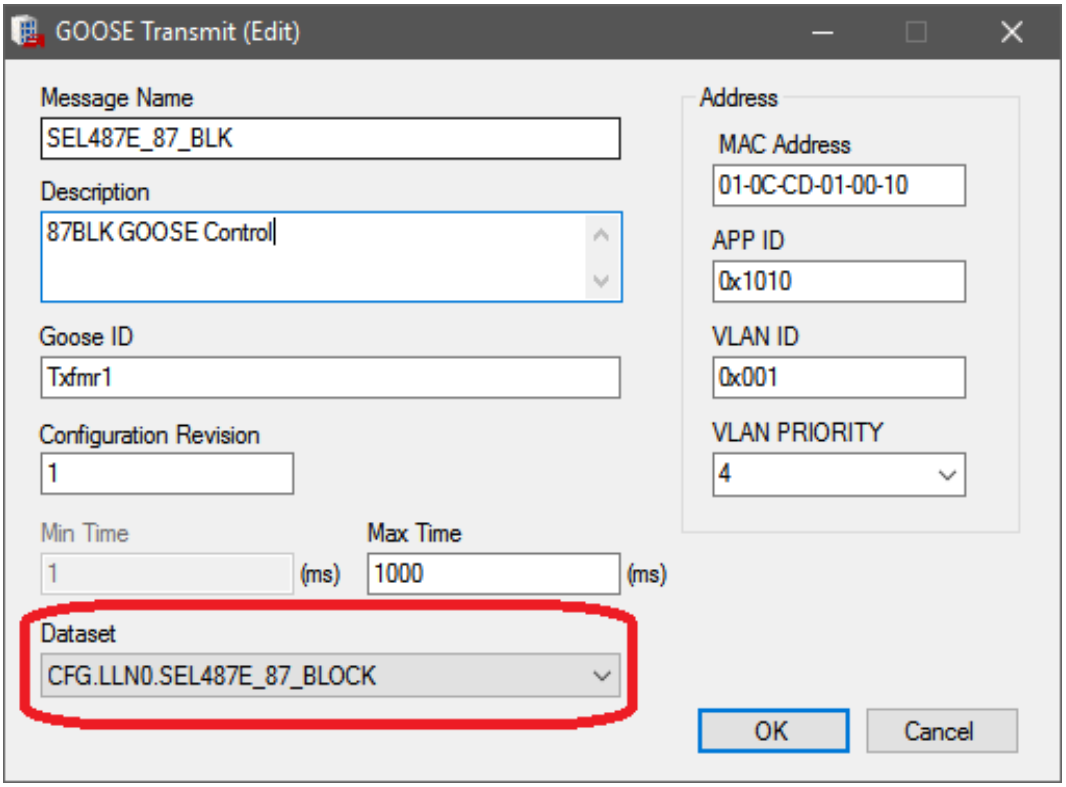


Figure 6.21: SEL487E harmonic blocking GOOSE control block

As shown in the Figure 6.21, a dataset should be mapped to the GOOSE control block. This is done by clicking on the drop-down arrow under ‘dataset’ (encircled red on the Figure 6.21). The user should define the application identifier APP ID according to IEC 61850-8-1 or left to the default value. The time interval between the publication of GOOSE messages after the exponential decay and there is no change in the GOOSE data set can be adjusted by entering the preferred value in the ‘Max Time' column.

Step 3: The SEL 751A is configured to subscribe to the GOOSE message being published by the SEL 487E. This is done by defining on the SEL 751A IED in the project editor and defining on the GOOSE receive tab. The GOOSE message being published by the SEL 487E IED will be listed under the GOOSE receive tab as shown in Figure 6.22.

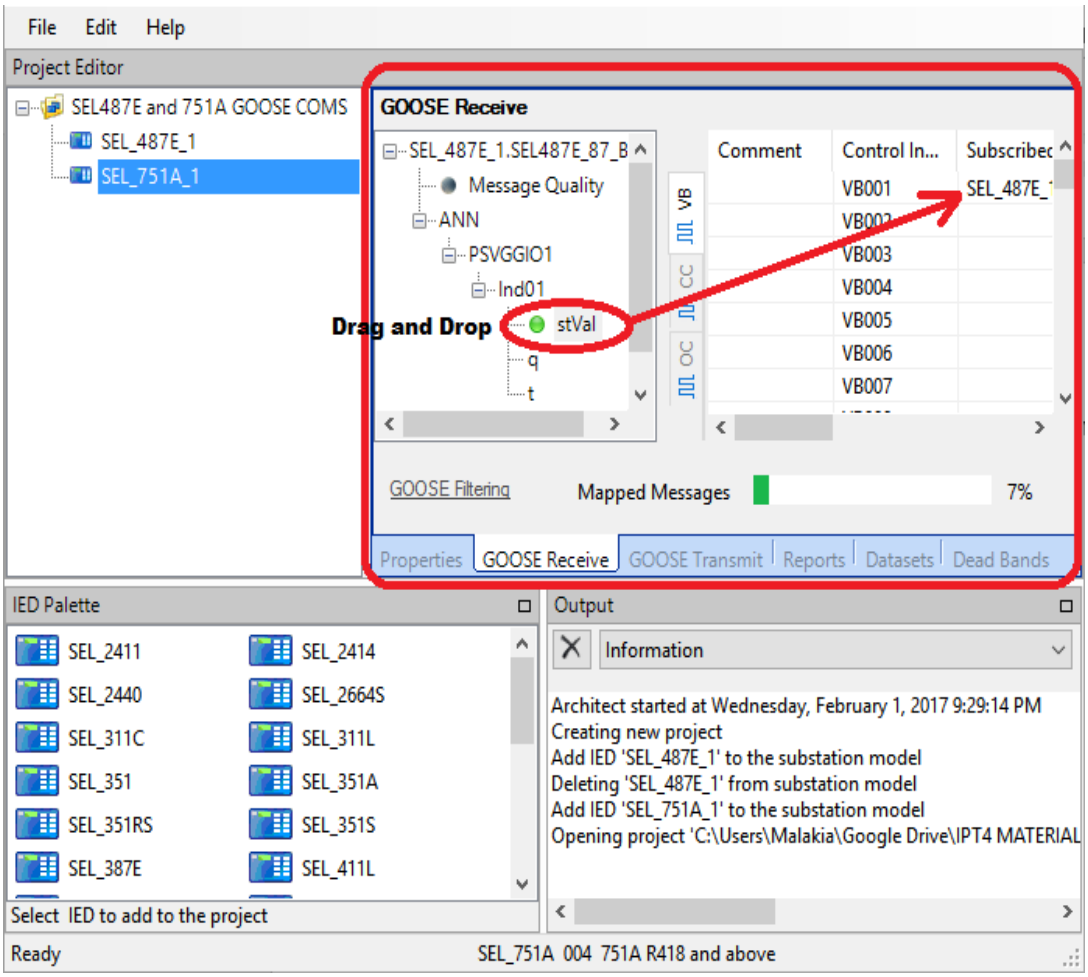


Figure 6.22: SEL 751A GOOSE message mapping for reverse harmonic blocking

The received GOOSE message needs to be mapped to a certain function of the SEL751A IED. This is done by double-clicking on the GOOSE message to decode it down to logical node level and drag and drop the status value onto a specific function. For this application, the received GOOSE message is mapped to virtual bit VB001 of the SEL 751A IED as shown in Figure 6.22.

Step 4: The configured IED descriptive CID files can be uploaded onto the IEDs by right-clicking on a specific IED in the project editor and clicking on send 'CID'. An access control window will pop up prompting the user to provide the log in details before continuing to upload the CID file onto the IED as shown in Figure 6.23 for the SEL 751A and Figure 6.24 for the SEL 487E IEDs respectively. Table 6.3 provides the access control credentials for SEL-751A and SEL-487E IEDs respectively.

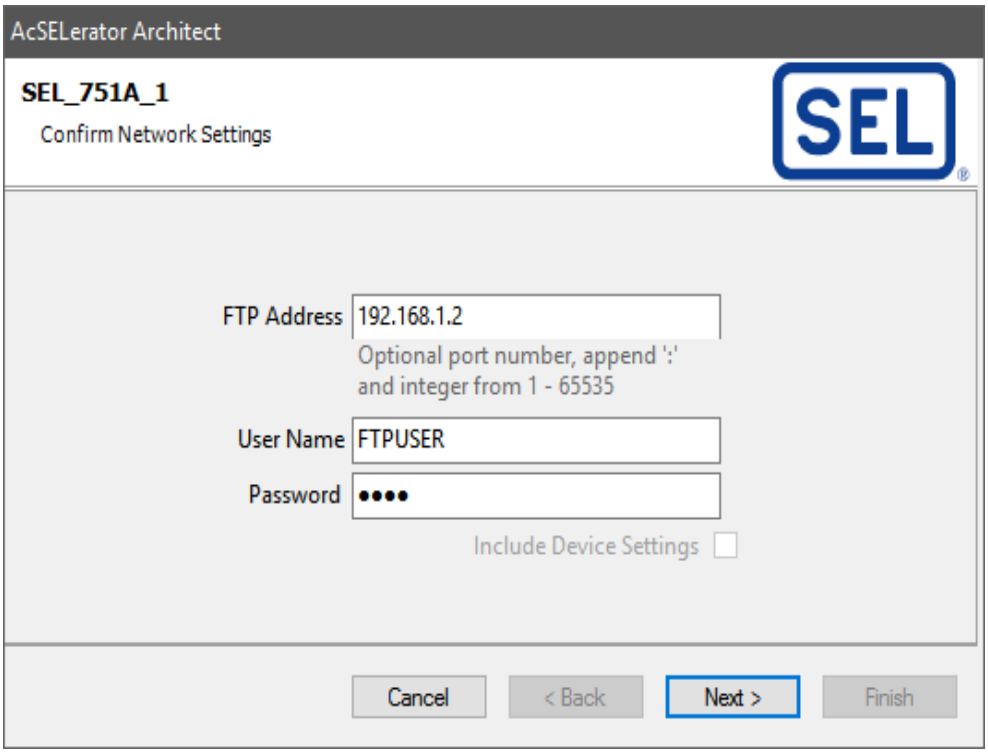


Figure 6.23: SEL 751A Access control window

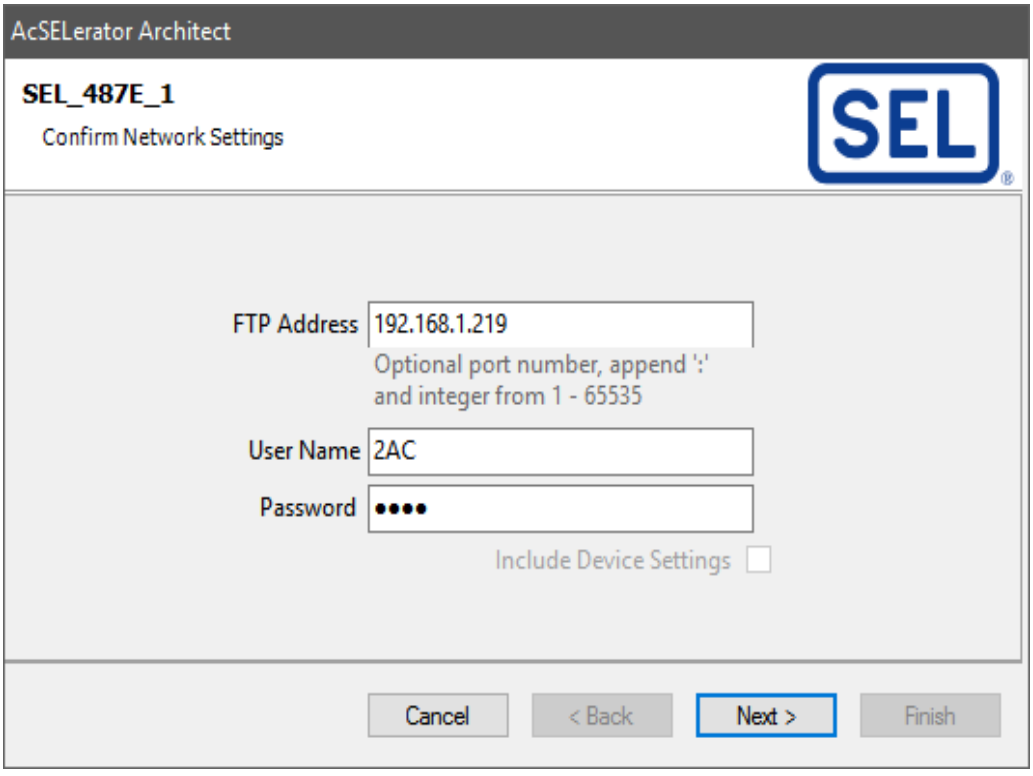


Figure 6.24: SEL 487E Access control window

The access details for the SEL 751A and SEL 487E IEDs are given in Table 6.3.

Table 6.3: SEL-487E and SEL-751A IEDs access credentials

SEL 751A		SEL 487E	
Username	Password	Username	Password
FTPUSER	TAIL	2AC	TAIL

6.7.2 Analysis of simulation results of the reverse harmonic blocking scheme using IEC 61850 standard-based GOOSE message

As shown in Figure 6.25, the relay is tested using the developed reverse harmonic blocking scheme. An inrush current with 16.60% of the harmonic level is injected into the IEDs. The analogue and digital signals recorded during the simulation are shown in Figure 6.25a and 6.25b respectively.

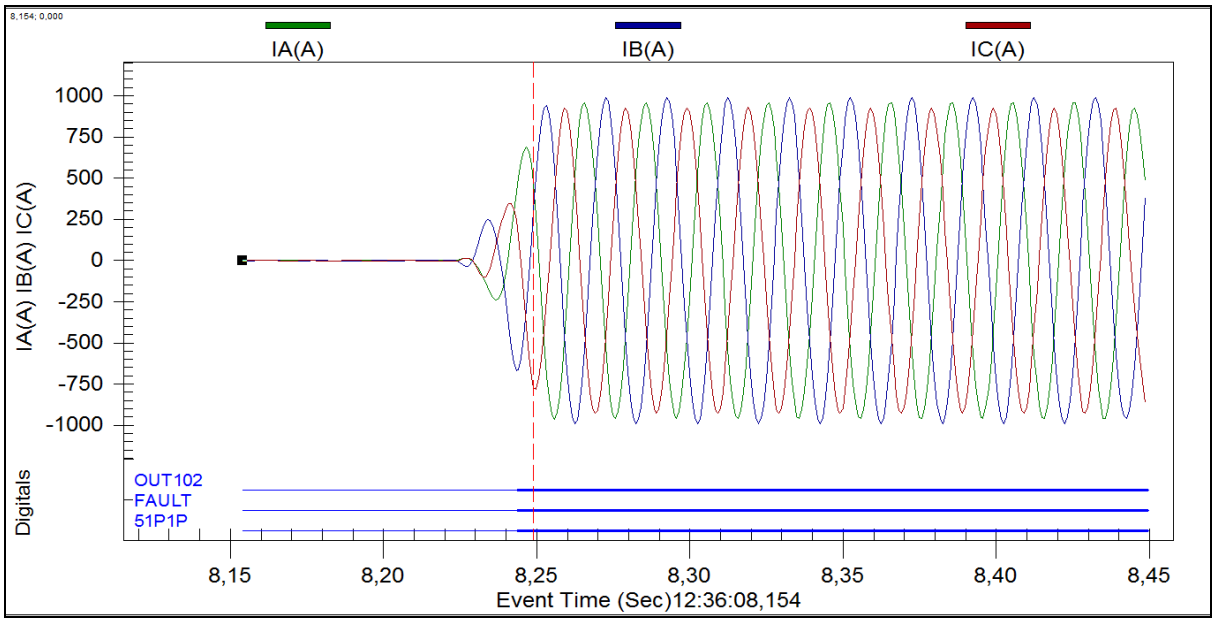


Figure 6.25a: Inrush current condition monitored from SEL-751A

From Figure 6.25a, it is observed that with a 16.60% 2nd harmonic currents are injected in both IEDs (SEL-487E and SEL-751A), this picks up as fault by asserting 51P1P and FAULT elements.

In Figure 6.25b, the digital signals 51P1P represents the phase Inverse Definite Minimum Time (IDMT) element. 51P1P element asserts when the fault on the system and 51P1T should assert when the element issues a trip signal. VB001 is the virtual SELogic protection variable that is mapped to the incoming GOOSE message from SEL-487E.

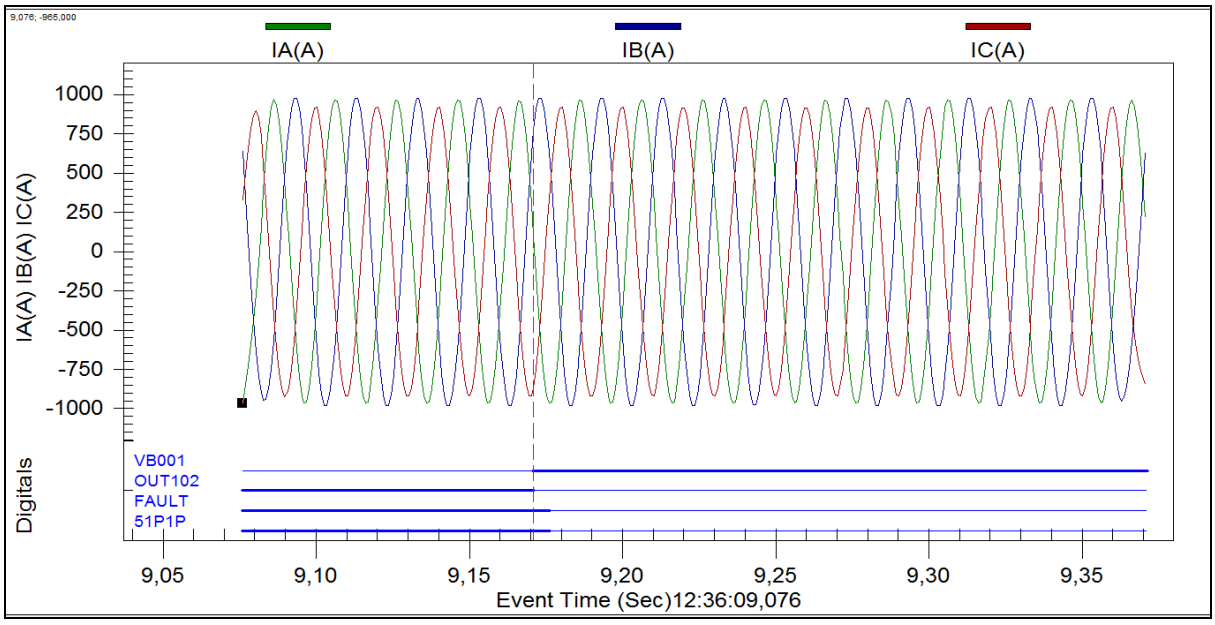


Figure 6.25b: Reverse harmonic blocking signal recorded by SEL-751A

It is evident that upon receipt of the GOOSE message, the 51P1P element dropped out, preventing the relay from issuing a trip signal during TMIC condition. The signals recorded by the SEL-487E during the fault are shown in Figure 6.26.

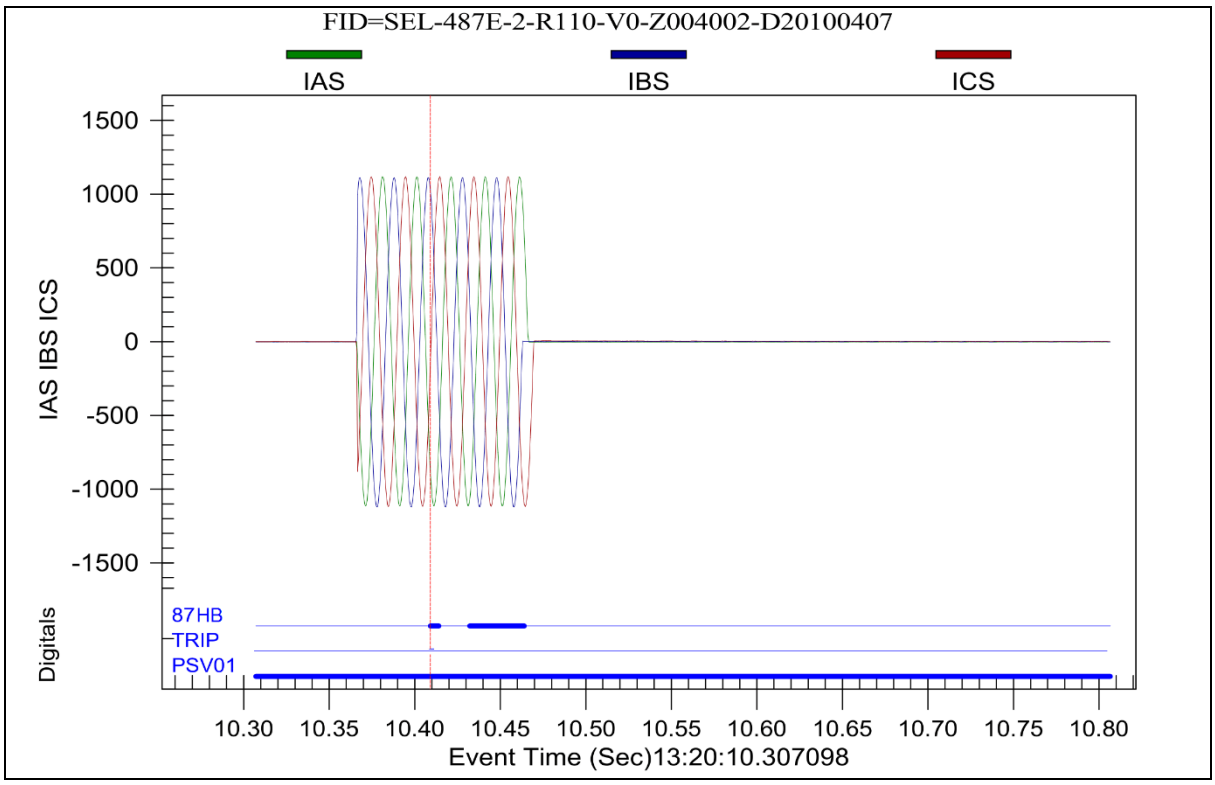


Figure 6.26: Inrush current condition recorded by SEL-487E

In Figure 6.26, harmonic blocking element (87HB) digital signal and the protection SELogic variable (PSV01) configured to transmit a harmonic blocking GOOSE message signal during an inrush condition. Although the harmonic blocking element 87HB asserts and de-asserts, the state of the protection SELogic variable PSV01 remains stable. This because the signal is sealed in the SELogic protection latch PLT 32 Equation (6.1) to (6.3) as soon as the harmonic blocking element asserts for the first time. The results of the IEC 61850 GOOSE message-based simulation prove that the reverse harmonic blocking scheme can be employed to prevent the tripping of the SEL-751A relay malfunction due to the transformer magnetisation inrush current condition as shown in Figure 6.26.

6.8 Conclusion

The IEC 61850 GOOSE message based, and hardwired laboratory study was conducted in the CSAEMS lab, and various faults pertaining to power transformers were simulated using the omicron test injection device, and relay performance was monitored. The implementation of the lab-scale test bench setup transformer protection is shown in Figure 6.2.

This chapter presents the practical implementation of the IEC 61850 standard based protection scheme. The scheme applies IEC 61850 GOOSE messaging to send a reverse harmonic blocking scheme from the SEL 487E differential IED to the SEL-751A overcurrent IED during the transformer magnetizing inrush current condition.

In addition to that, this chapter presents the developed algorithm for the reverse harmonic blocking scheme. The test bench setup is implemented for both hardwired DC signals and IEC 61850 GOOSE message signals for reverse harmonic blocking for transformer differential elements. Two case studies are simulated in order to analyse the performance of the transformer protection speed, security and reliability of the developed reverse harmonic blocking scheme.

Next chapter provides the Hardware-in-the-loop test implementation and simulation analysis of the developed reverse harmonic blocking scheme using the Real-Time Digital Simulator (RTDS) and numerical IEDs.

CHAPTER SEVEN
IMPLEMENTATION OF THE HARDWARE-IN-THE-LOOP TESTING OF THE REVERSE HARMONIC BLOCKING SCHEME FOR TRANSFORMER PROTECTION

7.1 Introduction

This chapter is analysing the reverse harmonic blocking scheme using IEC 61850 GOOSE message with data obtained in real-time using Real-Time Digital Simulator (RTDS). The hardware-in-the-loop tests were implemented for IEEE 14-Bus system network designed and modelled in RSCAD environment. The hardware-in-the-loop was implemented using RTDS, SEL-487E and overcurrent software relay model.

Two case studies were conducted, case study one analyses the transformer inrush current condition and case study two analyses the transformer inrush current condition using IEC 61850 GOOSE blocking signal sent from transformer differential IED to the overcurrent software IED.

An external physical IED SEL-487E is connected in a closed-loop configuration with the Real-Time Digital Simulator (RTDS). SEL-487E IED is configured to send a reverse blocking signal to the RTDS and an internal software overcurrent relay model is configured to receive the IEC 61850 standard-based GOOSE blocking signal to avoid the malfunction caused during the transformer magnetizing inrush conditions (TMIC).

This chapter provides the modelling and simulation of the IEEE 14-Bus system in RSCAD software. Real-time external and internal faults simulations on power transformer were carried out using RTDS connected in a closed-loop with an external IED (SEL-487E) and RSCAD software overcurrent relay model. Finally, results obtained from RSCAD runtime environment and event records simulation results are analysed. Next section provides the overview of the RSCAD simulation software, which is designed to interface with the RTDS simulator hardware to perform real-time digital simulations.

7.2 RSCAD simulation software

RSCAD software suite of RTDS employs an advanced and straightforward way to use graphical user interface. The software is comprised of several modules, which enable the user to design, simulate and analyse the simulation output of the real-time

digital simulator. The users can model the power system using the components present in the power and control system library and simulate it using the Real-Time Digital Simulator. The file manager window in the RSCAD has ‘Draft', ‘Runtime', ‘Multiplot', ‘Cable', ‘T-Line, ‘Help', ‘Convert' and ‘Manuals' menus. The power system modelling is done through the ‘Draft' option in RSCAD, where the requisite components can be modelled using a drag and drop interface provided. The transmission lines present in the power system test case (IEEE 14-bus system) have been modelled using the ‘TLine' option. Once the RSCAD simulation model is compiled without any errors, the simulation results can be observed through the ‘Runtime' option. The RSCAD software is an excellent graphical user interface through which the parameters of the power system components can be defined in detail. The RSCAD software suite of RTDS enables the user to prioritize the components so that the processor usage is adequately distributed without overloading a particular processor (RTDS Instruction manual, 2009).

7.3 Real-Time Digital Simulator (RTDS)

RTDS simulator is a tool to model and simulate the real-time simulations of power and control systems (Ouellette D.C. et al., 2004). The dynamic behaviour of a power system is studied using RTDS in real-time simulation. The real-time simulation is of paramount importance when the behaviour of a power system is to be studied under transient conditions and dynamically changing conditions. There is a need to simulate different fault conditions on a power system in order to observe the reliability of the protection system being used. By simulating the fault conditions in real time improves the accuracy of observations, as the simulations would be closer to the real-world scenarios. This helps in enhancing the protection strategy and also the protective system models (McLaren P.G. et al., 1992).

The RTDS uses a custom parallel processing hardware architecture, which takes place in units called racks. The RTDS consists of various cards including Triple Processor Cards (3PC), Giga Processor Cards (GPC), and Twelve Channel Analogue Output Card (GTAO), etc. The 3PC card can be used to model the power system test case. The analogue device called the ADSP21062 (SHARC) digital signal processors (DSP) is present in each 3PC card of the RTDS hardware (RTDS Instruction manual, 2009). The 3PC cards provide the analogue channel outputs, which can be used to connect external equipment and conduct the hardware-in-the-loop (HIL) testing.

Each of the Triple Processor Card (3PC) cards contain three SHARC digital signal processors ADSP21062, 24 analogue output channels that can provide an output of ±10 Volts peak, two 16-bit digital input channels of 5 Volts, and two 16-bit digital output channels of 5 Volts (RTDS Instruction manual, 2009). The Giga Processor Card (GPC) is another component of the RTDS with powerful computational capacity. The RTDS hardware is shown in Figure 7.1.

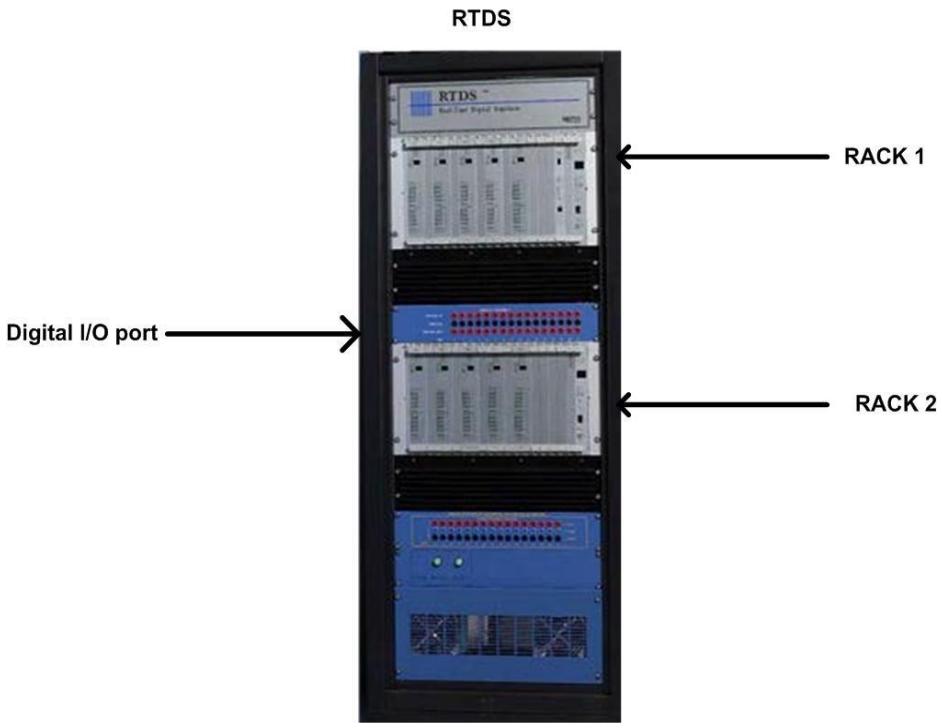


Figure 7.1: Real-Time Digital Simulator

As seen in Figure 7.1, the racks are placed on the front panel of the RTDS hardware. The digital input/output port on the front panel allows the feedback signals from the relay hardware to be connected to the RTDS hardware.

The RTDS can be used for the following applications:

- High-speed simulations
- Closed-loop testing of protection equipment, e.g. relays
- Closed-loop testing of control equipment e.g. exciters, voltage regulators, FACTS devices, power system stabilisers, etc.
- Hardware-in-the-loop applications

The RTDS modules available at Centre for Substation Automation and Energy Management Systems (CSAEMS) at Cape Peninsula University of Technology has the following processor cards:

- 4 Gigabit Transceiver Workstation Interface (GTWIF) card
- 3 Gigabit Processor Card (GPC) card
- 5 Gigabit Transceiver Network Interface Card (GTNET) cards supporting communication protocols such as PMU, GSE, SV and DNP3.
- 2 Gigabit Transceiver Analogue Output Card (GTAO)
- Gigabit Transceiver Front Panel Interface (GTFPI) card
- 1 Gigabit Transceiver Analogue Input (GTAI) card
- 6 PB5 Processor card which is a previous generation of processing hardware for the RTDS simulator
- 1 Gigabit Transceiver Network Interface Card GTNETx2 which is the latest generation for communication protocol x2 (GSE and SKT)
- 2 GYSYNC card which is used to synchronise the RTDS simulation time step to an external synchronize time reference GPS clock and to devices under test
- Digital I/O panel
- HV Patch Panel

Next section provides the overview of the hardware-in-the-loop testing of the protective relaying system.

7.4 Hardware-In-The-Loop (HIL) testing using Real-Time Digital Simulator (RTDS)

The Real-Time Digital Simulator (RTDS) is a useful tool for modelling and simulation of power and control systems (RTDS Instruction manual, 2009).

The real-time simulations play a crucial role in the power system to observe the power system behaviour in response to transient conditions and other rapid and sudden changes in the power system. The modelling and simulation in real time help in improving the quality of the protection system and to maintain the stability and continuity of the power system operation. The real-time simulations have been studied in this project for the hardware in the loop testing and software in the loop testing of the reverse harmonic blocking scheme. The real-time simulation is the tool being used to test the protective relay and observe its reliability and efficiency during the transient conditions on the power system. Real-time open loop and closed loop testing (Forsyth P. et al., 2004) are the ultimate testing techniques for any protective device. The real-time closed loop testing is capable of the following:

1. Interacting with one or more protective devices.
2. Interfacing the power system and the protective devices to find the exact interaction.
3. Increasing the efficiency of the real-time simulation.

One of the most important techniques, which falls under the closed loop and open loop testing, is the Hardware-In-The-loop (HIL) testing technique used to analyse the nonlinear and dynamic behaviour of the physical device and helps in building and validating a model to control the physical devices. The HIL simulation is being used in the development and testing of complex real-time systems. The main idea behind the HIL simulation is to provide a useful platform to develop the test-bed to test the protective relay in a real-time simulation environment. The HIL simulation must include electrical emulation of sensors and actuators for the communication interface between a protective relay and the simulator. Control algorithm enables the flow of signals through the sensors and the actuators in the protective system. In an HIL simulation, the virtual power system is connected to the actual physical devices.

7.5 IEEE 14 Bus system

The IEEE 14-Bus the transmission system is published by the IEEE Power Engineering Society. The network was designed and modelled in RSCAD using the data given in Tables 4.1 to 4.5.

The IEEE 14-Bus system consists of 14 buses (nodes), 5 generators, 11 loads, 16 lines, 5 transformers and one shunt. Figure 7.2 shows the single line diagram of the IEEE 14 bus system in the RSCAD software environment.

Figure 7.2 below shows a portion of the IEEE 14-Bus system designed in RSCAD software environment. CB1 and CB2 define the transformer protection zone, in other words, any fault event within the zone of protection is an internal fault and the fault event outside the protection zone is an external fault. Therefore, for internal events the differential protection relay SEL-487E is expected to send a trip feedback which will open the circuit breakers (CB1 and CB2) in RSCAD runtime. The full IEEE 14-Bus system can be found in Appendix A.3.1.

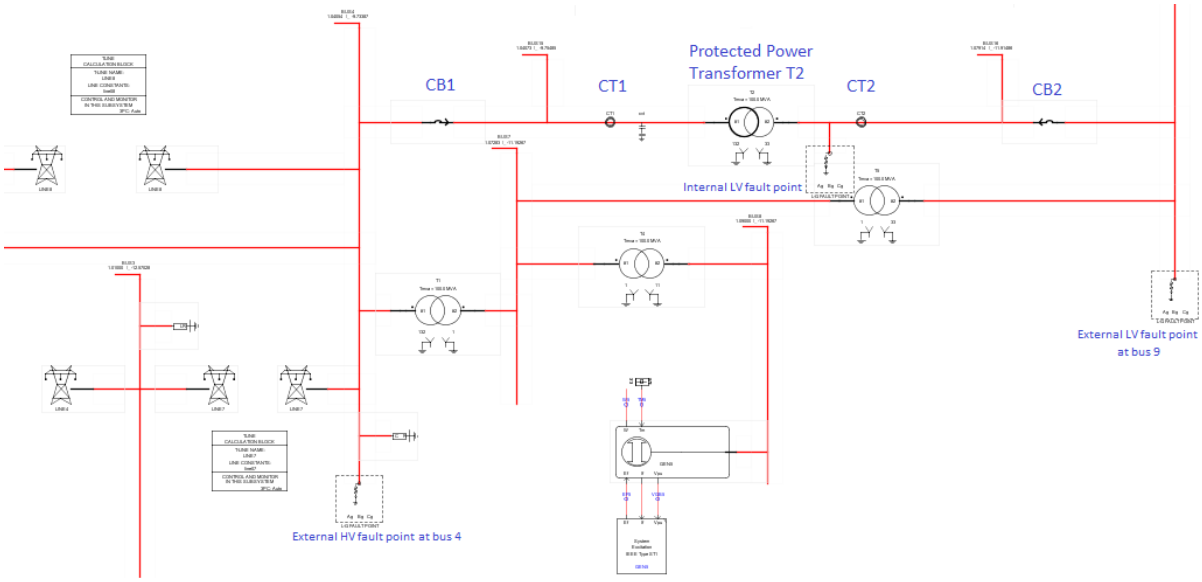


Figure 7.2: IEEE 14-bus system in RSCAD

7.6 Hardware in the loop testbed implementation for a transformer reverse harmonic blocking scheme

Hardware in the loop testing technology is one of the techniques used to understand the nonlinear and dynamic behaviour of the physical device and helps in building and validating a model to control the physical devices. In a HIL simulation, the virtual power system is connected to the actual physical devices (Tang J. et al., 2006).

The digital to analogue converter (DAC) with its current signals are shown in Figure 7.3. The digital to analogue converter component present in the RSCAD is used to send the currents measured by the CTs to the protective relay equipment as shown in Figure 7.3. The currents measured by the CT1 are named as IBUR1A, IBUR1B and IBUR1C, whereas the currents measured by the CT2 are named as IBUR2A, IBUR2B and IBUR2C, respectively.

The GTAO component, as it is called in the RSCAD library, sends the input signals to GTAO high precision analogue output board. The GTAO board is a 12-channel component of the RTDS hardware. The GTAO takes in REAL input signals. The component converts the input signals and scales them to 16-bit and writes them to the GTAO card via the optical port of the RTDS hardware. The GTAO gives an output in the range of ±10 V. The GTAO card interfaced between the RTDS rack, and Omicron amplifiers are shown in Figure 7.4.

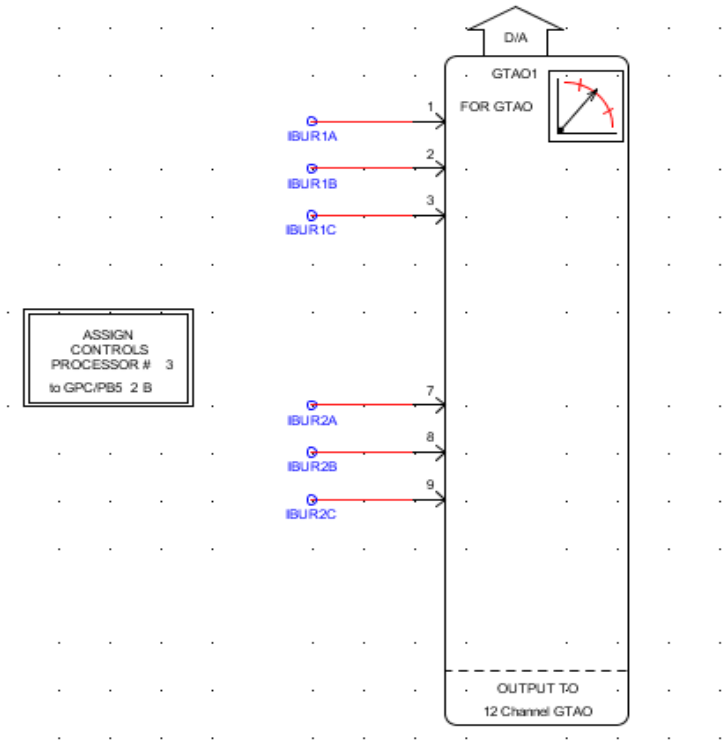


Figure 7.3: DAC Component in RSCAD

The hardware interface block is designed in RSCAD, which allows the connection between the SEL-487E Transformer differential relay and the RTDS GTAO interface card as shown in Figure 7.4. The current signals (CT1 and CT2) simulated in RTDS are sent to the SEL-487E hardware relay as shown in Figure 7.4. The feedback connection from the SEL-487E hardware relay to the Digital, I/O port of the front panel of the RTDS, is defined to send the trip and/or GOOSE signals as shown in Figure 7.4. The current signals of the S and T windings of the SEL-487E hardware relay are continuously monitored and updated. The digital current signals from the RTDS GTAO card are amplified and fed to the SEL-487E hardware relay. The Omicron amplifiers amplify the CT1 and CT2 current signals to the S and T windings of the SEL-487E which emulate a real-time simulation environment (Kezunovic M et al., 1996).

The SEL-487E Transformer differential relay is defined to issue trip signals for internal events on the protected zone of the power transformer. AcSELerator Quickset engineering configuration software is used to configure the SEL-487E relay. The zone definition is based on the position of the device to be protected and its circuit breakers connection.

The S and T windings current signals from RTDS simulation are sent continuously to the SEL-487E transformer differential relay through the GTAO and CMS156 Omicron amplifier as shown in Figure 7.4.

The S and T winding current signals from the RTDS are connected through the back panel to the SEL-487E relay hardware. The SEL-487E relay monitors the current signals and based on its protection logic and issues a trip signal when there is a fault condition at the power system transformer T2 as shown in Figure 7.2. This trip signal from the SEL-487E relay is sent to the digital input port on the front panel of the RTDS hardware as shown in Figure 7.4.

The trip signal is sent from the SEL-487E relay hardware through the cables connected to the front panel (digital input port) of the RTDS, thus completing the hardware in the loop physically. The hardware-in-the-loop test arrangement of the SEL-487E Transformer differential relay and the RTDS is shown in Figure 7.4.

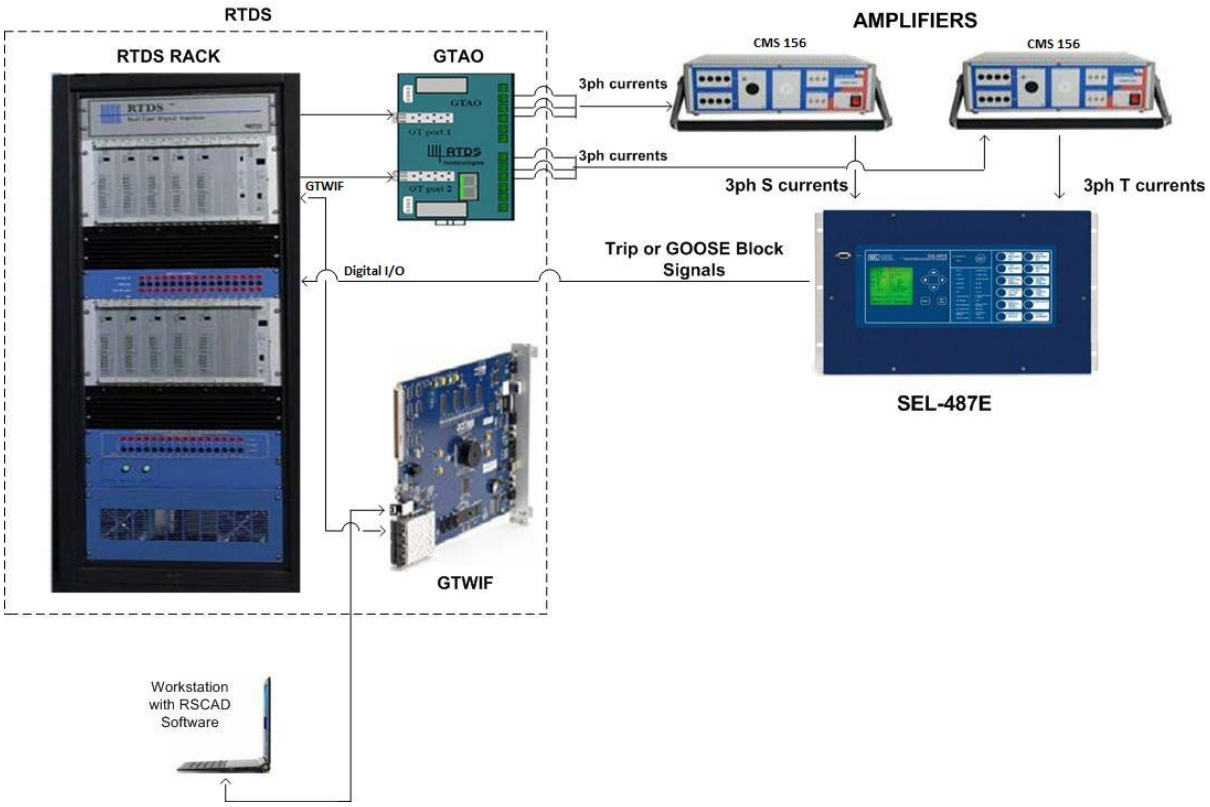


Figure 7.4: RTDS Hardware-in-the-loop testbed setup for the reverse harmonic blocking scheme

The following abbreviations are given below help to understand the HIL testbed setup shown in Figure 7.4

- CMS156: Voltage and current amplifier for low-level analogue signals provided by RTDS
- GTWIF: Gigabit Transceiver Workstation Interface card
- GTAO: Gigabit Transceiver Analogue Output card
- SEL-487E: SEL power transformer Intelligent Electronic Device (IED)
- 3ph S currents: three-phase currents inputs to S channel of the SEL-487E IED
- 3ph T currents: three-phase currents inputs to T channel of the SEL-487E IED
- GOOSE block signal: IEC 61850 standard-based Generic Object-Oriented Substation Event message to Digital I/O port of the RTDS

The simulation outputs from the RSCAD Runtime environment of the RTDS are exported via GTWIF card. Two Omicron amplifiers are connected to the GTAO card in order to convert ±10V analogue current signals to the S and T windings currents channels of the SEL-487E relay as shown in Figure 7.4. These analogue current signals are made available to the Current Transformers (CTs) modules of the SEL-487E relay.

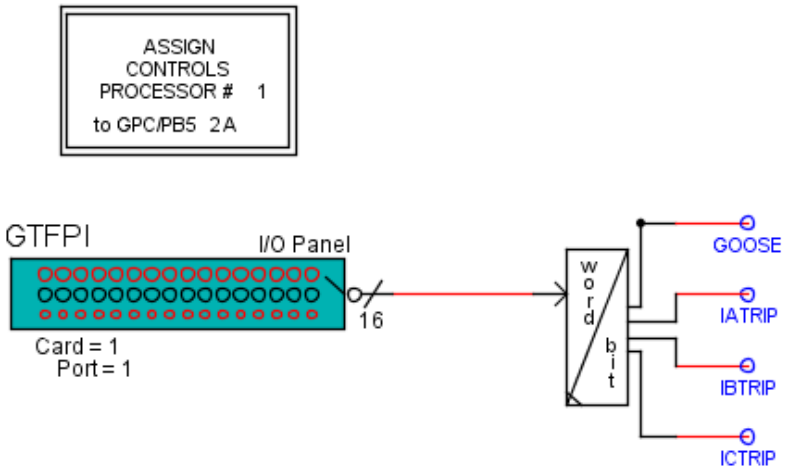


Figure 7.5: GTFPI Component and its word to bit conversion for the trip and GOOSE signals

The digital input port of the GTFPI card, word to bit convert block and the output trip and GOOSE signals are shown in Figure 7.5 in the RSCAD simulation environment. Eventually, the outputs from the SEL-487E either trip or GOOSE block 16-bit data is read through the digital input port of the RTDS. Only the 3PC processors A and B access the digital input port. The digital input port reads the 16-bit data and returns

an INTEGER. In order to further process this INTEGER word, there is a word to bit conversion block, which converts the INTEGER word to multiple logical signals namely, IATRIP, IBTRIP, ICTRIP, and GOOSE, which are the trip signals of phases A, B and C, respectively and IEC 61850 GOOSE message signal sent from SEL-487E to the network.

7.6.1 Fault Control Logic

Controls components in the RSCAD library are used to create the fault control logic that controls the type, duration, point on the wave, and location of the fault. The fault can be controlled in the RTDS runtime environment and is used to analyse the relay operation during the fault at high voltage side faults, low voltage side faults, and internal faults.

The fault control logic is shown in Figure 7.6 is designed to incept a single line to ground, double line to ground and triple line to ground. The fault types are external and internal faults at the power transformer T2, which is protected by the relay hardware SEL-487E.

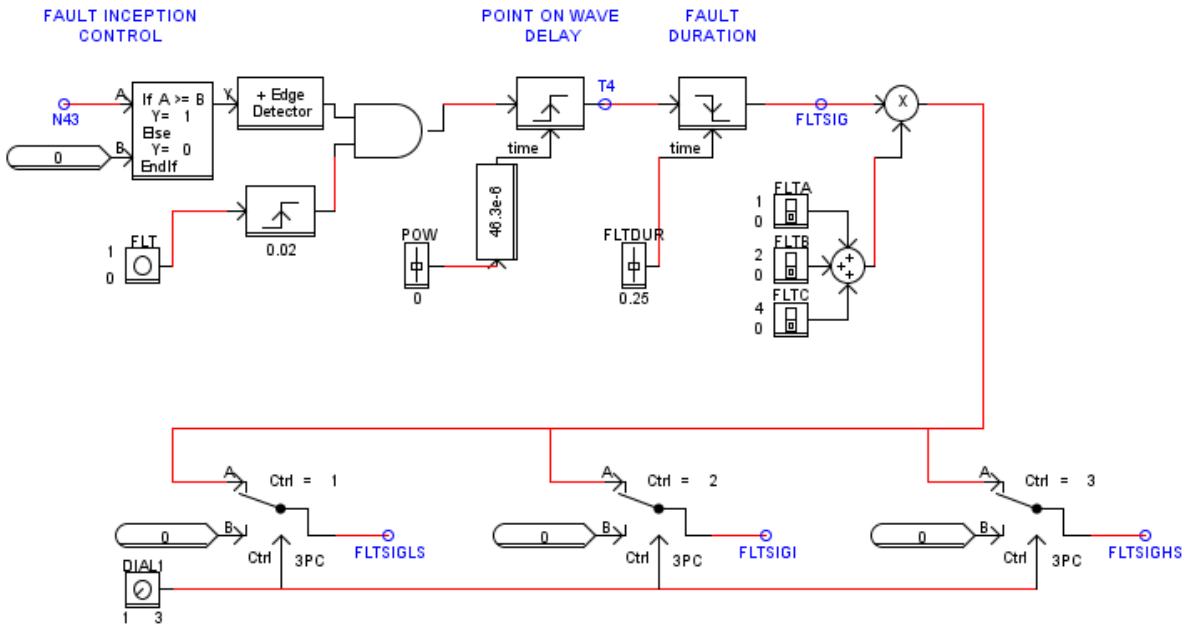


Figure 7.6: Fault control logic

Table 7.1: Description of the control components used to build the fault control logic

Abbreviation (control components)	Description of the control component used in the fault control logic
N43	Voltage reference node at bus 4
FLT	Fault control

FLTA	Fault on phase A
FLTB	Fault on phase B
FLTC	Fault on phase C
POW	Point on the wave
FLTDUR	Fault duration
FLTSIG	Fault signal
FLTSIGLS	External fault signal on the low voltage side of the power transformer
FLTSIGHS	External fault signal on the high voltage side of the power transformer

The inception of the faults at the protected transformer is based upon the node voltages at the transformer. The fault inception logic is a critical part of the hardware in the loop testing because it enables the inception of the fault, which is eventually detected by the hardware relay. The fault inception logic considers the node voltage at the protected power transformer namely N43 as the reference point for the point on wave delay. An If-Then-Else logic gate with a positive edge detector determines when N43 voltage has crossed the x-axis and is on the positive side. As soon as the FLT button is pressed, the raising edge detector sends out a signal carrying the value '1' which initiates the fault sequence. A pulse is then produced by the AND gate that combines the zero-crossing detector and the fault button. The pulse drives the point on wave logic, which is comprised of a slider, a gain block, and a pulse duration timer set to detect a rising edge. When the pulse rises to logic one, the output of the duration timer is set to logic one which is equal to the time it takes to rotate the number of degrees from the zero-crossing detection, set by the POW slider control. The point on the wave and the duration of the fault can be varied using the POW and FLTDUR sliders, respectively. Fault switches for the phase-to-phase and phase-to-ground fault types are combined to create the necessary integer value. The three switches FLTA, FLTB and FLTC are used to select the phase on which the fault is to be incepted. The final signal out of the logic i.e. FLTSIG is multiplied by the fault type integer value and is sent to the fault inception block present at the protected transformer in the power system test case.

The dial component DIAL1 is used change from FLTSIGLS, FLTSIGI and FLTSIGHS which represent external fault at LV side, internal fault and external fault at HV side of the power transformer respectively.

7.6.2 Circuit Breaker control logic

To demonstrate transformer inrush phenomena the breakers placed on the primary and the secondary of the transformer needed to be open and closed as shown in Figure 7.7. Opening the breakers will de-energise the transformer leaving a residual flux in the core of the transformer. Subsequently energising the transformer by closing the primary breaker will produce inrush currents. The severity of inrush currents depends on the point on the voltage waveform at the breaker terminal and the residual flux. The situation that generates the highest magnitude inrush currents is when the breaker is closed at the instant the voltage passes through zero causing the flux to increase in the same direction as the offset. The offset is due to the residual flux. (RTDS Instruction manual, 2009)

The purpose of this logic circuit given in Figure 7.7 is to provide a circuit breaker OPEN and CLOSE pushbuttons that can operate the circuit breakers in RSCAD runtime. The circuit breakers are also supervised by the status of the lockout relay (86T). If the 86T is operated, the circuit breakers will open if previously closed and cannot be closed until the 86T is reset. The differential relay trip outputs for each phase set the 87T and provide a logic signal called 86T for monitoring purposes.

The controller logic used to operate the circuit breakers is shown in Figure 7.7.

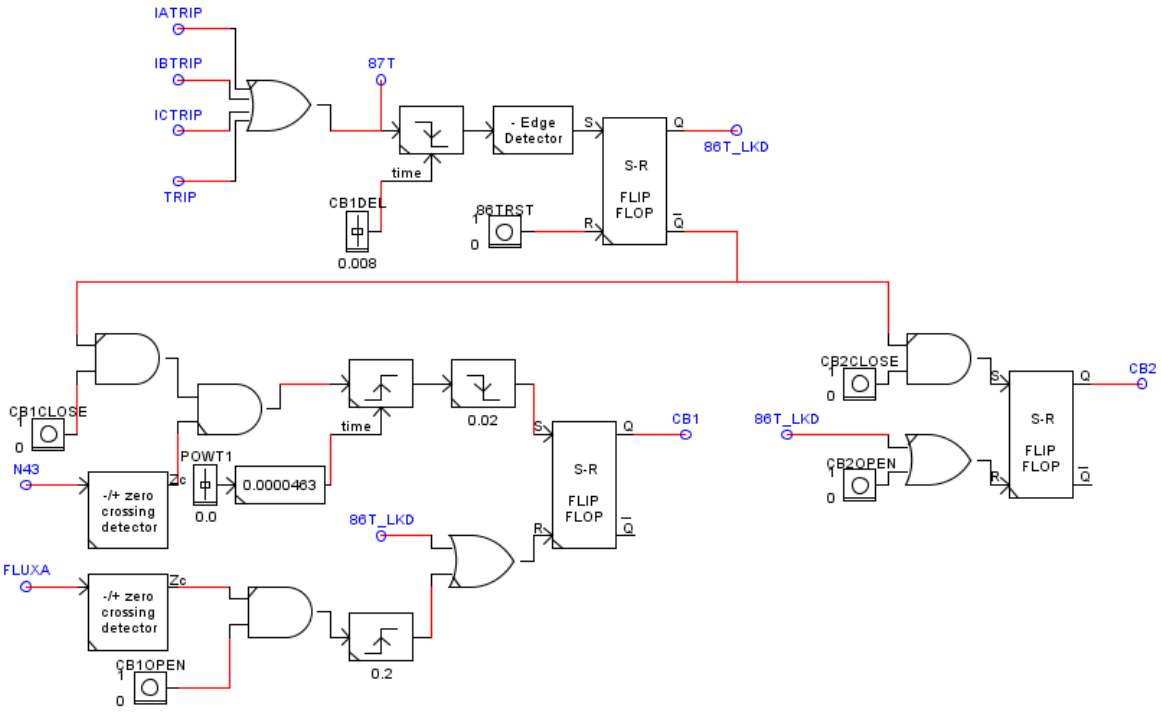


Figure 7.7: Circuit breaker control logic

Table 7.2: Description of the control components used to build the circuit breaker logic

Abbreviation	Description of the control component used in CB control logic
CB1CLOSE	Circuit breaker 1 close
CB2CLOSE	Circuit breaker 2 close
CB1OPEN	Circuit breaker 1 open
CB2OPEN	Circuit breaker 2 open
FLUXA	Residual flux phase A
POWT1	Point on wave
86T_LKD	Status of the lockout relay
CB1	Circuit breaker 1 at the primary side of the power transformer
CB2	Circuit breaker 2 at the secondary side of the power transformer
87T	Transformer differential trip
CB1DEL	Circuit breaker 1
86TRST	Lockout relay reset
TRIP_A	Trip phase A
TRIP_B	Trip phase B
TRIP_C	Trip phase C
TRIP	RSCAD overcurrent software relay trip

Two pushbuttons are included for each breaker, one to open and another one to close the breakers as shown in Figure 7.7. Trip signals (IATRIP, IBTRIP and ICTRIP) and TRIP from external differential relay SEL-487E and overcurrent software relay respectively are used to open both circuit breakers (CB1 and CB2). Therefore, when a trip signal is issued either from SEL-487E or RSCAD software overcurrent relay 87T differential trip signal is produced. The output duration timer is set to logic one for the specified time using slider CB1DEL; this output is connected to the negative edge detector component. The S-R flip-flop has two inputs such as negative edge detector and lockout relay reset (86RST) components as shown in Figure 7.7. The S-R flip-flop initiates the lockout relay 86T_LKD or opens both circuits breakers (CB1 and CB2).

The breakers will open when the flux has passed through zero in the positive direction, and the open pushbuttons are pressed in RunTime. The point on wave energisation is controlled using the slider POWT1. This was included to ensure that the residual flux results in a positive offset. Similarly, the primary breaker will close when the node voltage N43 has passed through zero in the positive direction, and

CB1CLOSE is set to 1 by pressing in RunTime. The point on wave value is entered in degrees; this value is converted to time using the gain block (0.000463).

7.6.3 Overcurrent relay modelling in RSCAD software suite of RTDS

To test the reverse harmonic blocking scheme in the hardware-in-the-loop with RTDS, the RSCAD software overcurrent relay is used as a back-up protection for the three-phase power transformer which is a replacement of SEL-751A IED used in chapter six, because CSAEMS at CPUT has only two amplifiers at the moment that is the reason the RSCAD software overcurrent relay is used in this chapter to test HIL simulation.

Overcurrent relays can operate with or without intentional delay and operate for any given direction of the current. The various inverse−time characteristic curves provide one of the most basic forms of protection used to protect power system components (RTDS Instruction manual, 2009). The magnitude of a sinusoidal waveform is used to create the operating force required to operate a protective relay. A method other than just measuring the current magnitude must be used to determine the direction of current flow thereby providing directional sensitivity. The inverse time overcurrent relay parameters are used to calculate the expected operate and reset times for the IEC and IEEE inverse time overcurrent curve algorithms. Different operational time delays can be achieved by varying certain parameters of the relay design given in Table 7.3.

Table 7.3: IEC and IEEE inverse time overcurrent relay parameter settings

Inverse-time overcurrent characteristic curves	A	B	P	TR
IEC Standard Inverse	0.14	0.0	0.02	4.85
IEC Very Inverse	13.5	0.0	1.0	21.6
IEC Extremely Inverse	80.0	0.0	2.0	29.1
IEEE Moderately Inverse	0.0103	0.0228	0.02	0.97
IEEE Very Inverse	3.922	0.0982	2.0	4.32
IEEE Extremely Inverse	5.64	0.0243	2.0	5.82

The variables given in Table 7.3 is used to calculate trip and reset time for the overcurrent relays using are used in Equations 7.1 and 7.2 respectively.

$$tp = TMS\left[B + \frac{A}{\left(\frac{I}{I_p}\right)^p - 1}\right] \quad (7.1)$$

$$tr = \frac{TR}{\left(\frac{I}{I_p}\right)^2 - 1} \quad (7.2)$$

Where:

tp is the pickup time of the overcurrent relay;

TMS is the time multiplier setting;

A, B, P and TR are the constants of the IEC and IEEE inverse time overcurrent relay;

I is the measured RMS current;

I_p is the pickup current

tr is the reset time

The next section provides the logic used to create the IEEE/IEC inverse time overcurrent relay curves.

The dial component is created in the RSCAD software environment as shown in Figure 7.8 to change the values of the variables A, B, P, and TR using Table 7.3.

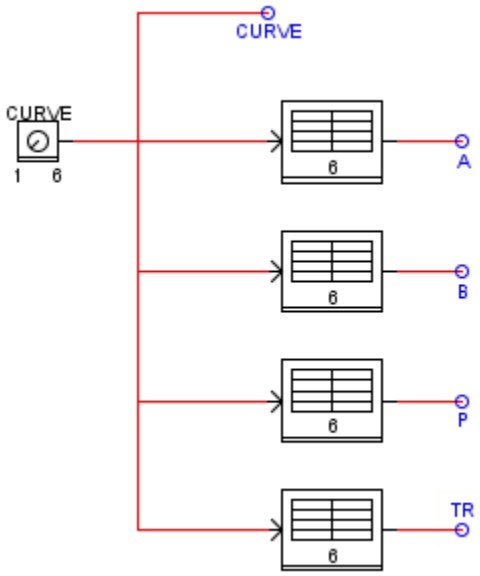


Figure 7.8: IEC and IEEE inverse time overcurrent curve setting parameter logic

Figure 7.8 above provides the IEC and IEEE inverse time overcurrent curve setting parameters logic, a dial component curve containing six types of characteristic curves as shown in Table 7.3. It allows the user to change the values of variables A, B, P and TR according to the type of the curve chosen then the overcurrent relay will calculate the trip and reset times using Equations 7.1 and 7.2 respectively.

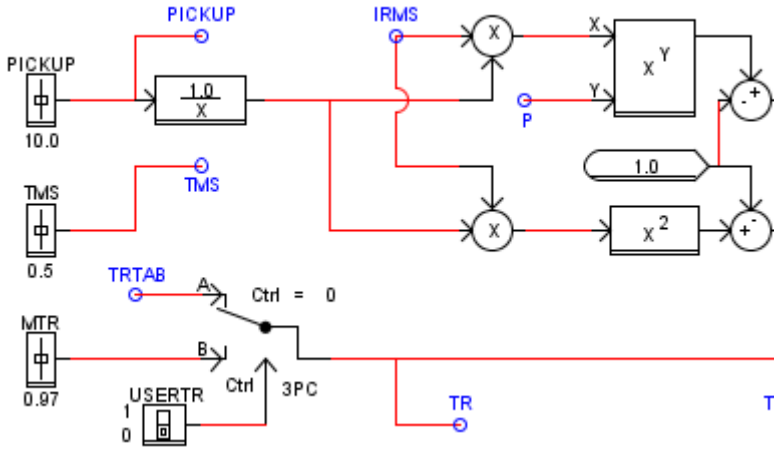


Figure 7.9: Part 1: operate and reset times

Figure 7.9 above provides the trip and reset time setting, the PICKUP slider is used to set the pickup current value from 0.1A to 50A. The TMS slider is used for time multiplier settings; it can be set from the value of 0.01 up to 10. And finally, a slider named MTR is used for resetting, and it can be set from 0.1 up to 100.

Table 7.4: Description of the parameters used to create the operate and reset times of the RSCAD software overcurrent relay

Abbreviation of the control components	Description of the parameters used to create the overcurrent relay model in RSCAD
A, B, P and TR	The constants of the IEEE and IEC inverse time overcurrent relay
PICKUP	Overcurrent relay pickup current
TMS	Time Multiplier Setting
MTR	Reset setting
USERTR	User reset pushbutton
IRMS	Measured RMS current
TIx	Expected operate time before sampling
TI	Expected operate time
S/H	Sample and hold signal processing
TIR	Expected reset time
SMPL	Converted sample values

KSUM	Operate time integer value
KTRSUM	Reset time integer value

These sliders values are then used to compute the expected operate and reset times. An additional logic gate and switch (USERTR) is used to define reset time constant. From Figure 7.9 above, the inverse of the pickup current setting is multiplied by the measured RMS current and raised to the power of P, and then subtracted from the result. It is also important to note that the value of P depends on the type the curve selected. This is the computation of the denominator part of Equation 7.1. The inverse of the pickup current setting is multiplied by the measured RMS current and then squared, with one subtracted from the result, and this is the computation of the denominator part of Equation 7.2.

The output value divides the constant "A" from Figure 7.9, then added to the constant “B”, and then multiplied by the time multiplier “TMS”. This completes Equation 7.1.

The reset time output from Figure 7.10 is computed by dividing the reset time constant by the value from part 1 and then multiplied by the time multiplier “TMS”. This completes Equation 7.2, and we now have the expected reset time. The remaining section of Figure 7.10 is used to sample and hold the expected operate and reset times.

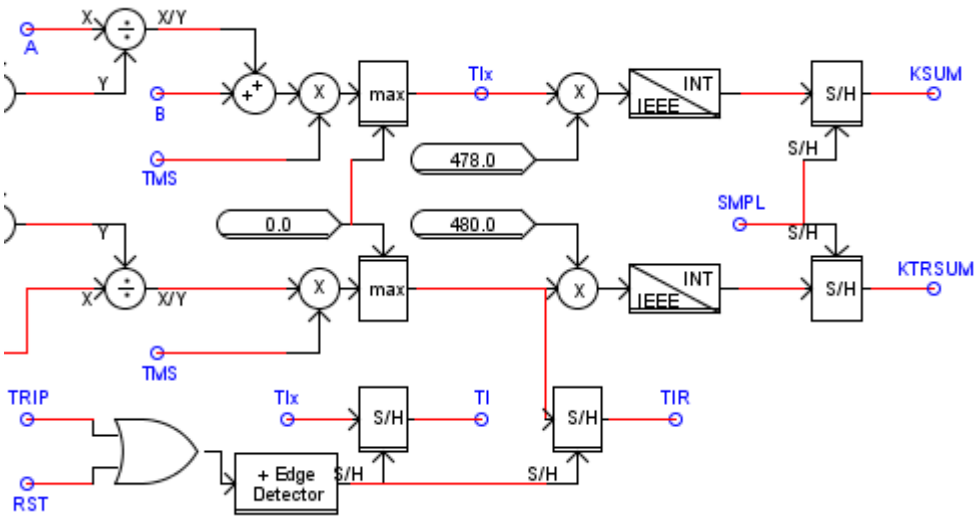


Figure 7.10: Part 2: operate and reset times

The computed times are first limited to values above zero, and then sample and these values are held whenever a "trip" or "reset" condition occurs. Therefore, the

monitoring of the expected operate "TI" and reset "TIR" times are allowed and compared to the actual operate and reset times.

The expected trip and reset times are multiplied by the sample rate, this value is converted to an integer, and then this value is sampled and held whenever the measured analogue data is above the pickup value. The two integer values "KSUM" and "KTRSUM" are used for determining when the operate and reset conditions occur. The expected operating time is adjusted by using a value other than the exact sample rate to define the actual operate times closer to the expected operating times.

7.6.3.1 Trip and reset logic of the RSCAD software overcurrent relay model

This section provides trip and reset elements logic design for the RSCAD software overcurrent relay.

When the measured RMS current is above the minimum pickup level and the analogue signal is sampled one time−step pulse is produced. This pulse is then used to drive two counters that increment to a maximum determined by the integer value for operate plus one and the other to a maximum determined by the integer value for reset. When the counter has exceeded this value, and the measured current is still above pickup, and positive torque exists, the relay trip signals produced. If a trip condition is issued from the relay, TRIP1 signal is energised before a setting called “MINTDUR” (minimum trip duration) is used to produce a trip signal with a minimum pulse width as shown in Figure 7.11.

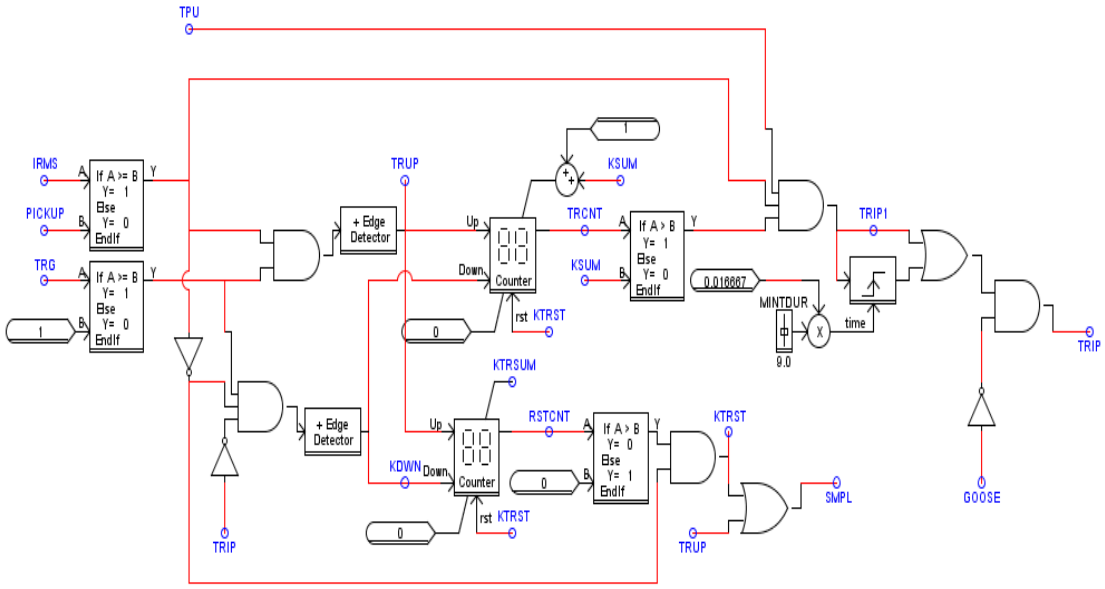


Figure 7.11: Trip and reset logic of the overcurrent function

Table 7.5: Description of the control components used to create the trip and reset logic

Abbreviation	Description of the control components used in trip and reset logic
IRMS	Measured RMS current
PICKUP	Pickup current value
TRG	Torque trigger
TPU	Torque control element
TRUP	Up-counter input
TRIP	Trip output
TRCNT	Trip counter output
TRIP1	Initial trip signal before GOOSE
RSTCNT	Reset counter output
KTRST	Counters reset signal
SMPL	Overcurrent software relay reset output
GOOSE	Generic object-oriented substation event
KSUM	Expected trip time
KTRSUM	Expected reset time
MINTDUR	Minimum trip duration

When the measured current is below the minimum pickup level, and the analogue signal is sampled and there is no trip condition, a one time−step pulse is produced. This pulse is used to reduce the count value of the two counters. When the reset counter has reached zero, the output (RSTCNT) of the counter will be zero. If the value of the measured current is below the minimum pickup setting the signal "KTRST" will go high and reset both counters as shown in Figure 7.11.

From Figure 7.11 above, it can be seen that the overcurrent software relay receives GOOSE signal from external SEL-487E relay when there is inrush current condition in the system. Only initial trip signal before GOOSE (TRIP1) signal is issued and the TRIP signal is blocked by the GOOSE signal.

7.7 HIL Simulation results for the reverse harmonic blocking scheme

The hardware-in-the-loop tests were implemented, and the power transformer reverse harmonic blocking scheme is studied. Faults are placed on bus 9 and bus 4 as an external fault on high and low voltage sides of the power transformer respectively and on bus 15 and bus 16 as internal fault as shown in Figure 7.12. It is important to note that in RSCAD software it is not feasible to connect the circuit breaker between the busbar and the two-winding transformer. Therefore, internal nodes (bus 15 and 16) are created to connect the high and low voltage sides of the

transformer with the circuit breakers in order for it to be protected as shown in Figure 7.12.

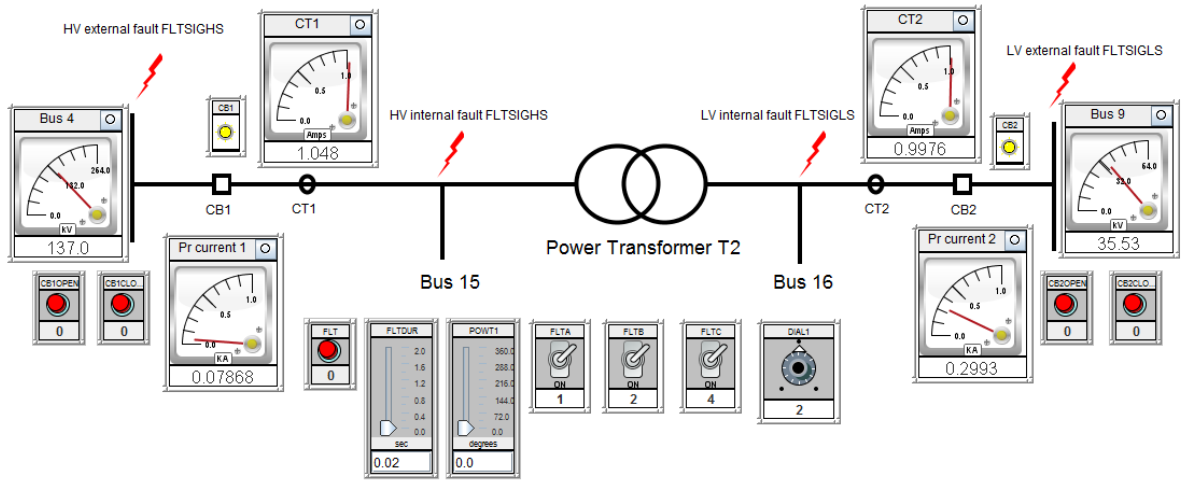


Figure 7.12: Power transformer protection in RSCAD RunTime

Three-phase power transformer T2 as shown in the above Figure 7.12 is protected using SEL-487E transformer differential relay. Various internal and external fault conditions are incepted at Bus 4 and Bus 9 using the designed fault inception block as shown in Figure 7.6. As soon as the relay detects the internal fault, the relay sends a trip signal to both breakers CB1 and CB2 to open and isolate the power transformer until the fault is cleared. Four pushbuttons (CB1OPEN, CB1CLOSE, CB2OPEN and CB2CLOSE) are used to open and close circuit breakers (CB1 and CB2) manually as shown in Figure 7.12. Pushbutton FLT is used to introduce the fault in the system and switches FLTA, FLTB, and FLTC are used to select the type of the fault. The dial component DIAL1 is used to change from position 1 to 2 and 3 which represent HV external (FLTSIGHS), LV external (FLTSIGLS) and internal (FLTSIGI) faults respectively. Two LEDs (CB1 and CB2) are used to indicate the status of the circuit breakers, if the lights are yellow it indicates that the circuit breakers are closed, in the case the breakers are open the lights turn to dark grey colour.

The hardware-in-the-loop test implemented on the SEL-487E power transformer differential relay does not include reclosing of the breakers. The breakers are to be closed manually after the fault is cleared. Therefore, the HIL test results of the IEEE 14-Bus power system model, the trip signals for various fault conditions are analysed. The relay will open both breakers as soon as an internal fault is detected.

The hardware interface between the power system and the relay hardware has been described in this Chapter in section 7.6.

The hardware-in-the-loop testing involves simulating the power system test case (IEEE 14-Bus system) in the RSCAD software environment and interfacing the RTDS to the actual SEL-487E power transformer differential relay. The voltages and currents drawn by the power transformer (T2) on HV and LV sides are as shown in the Figure 7.13 and Figure 7.14 respectively, are sent to the SEL-487E relay hardware through this interface.

The internal faults are incepted inside the protected zone through the fault inception block. The relay issues a trip signal as soon as it detects a fault inside the protected zone. The CT ratio used for CT1 is 400 turns and for CT2 is 1600 turns. The HIL test results of the IEEE 14-Bus power system tests case are presented for the normal conditions (when there is no fault) and when there is an internal and external fault on the protected zone.

Figures 7.13 and 7.14 below show the current and voltage during the normal operating condition of the three-phase power transformer (T2).

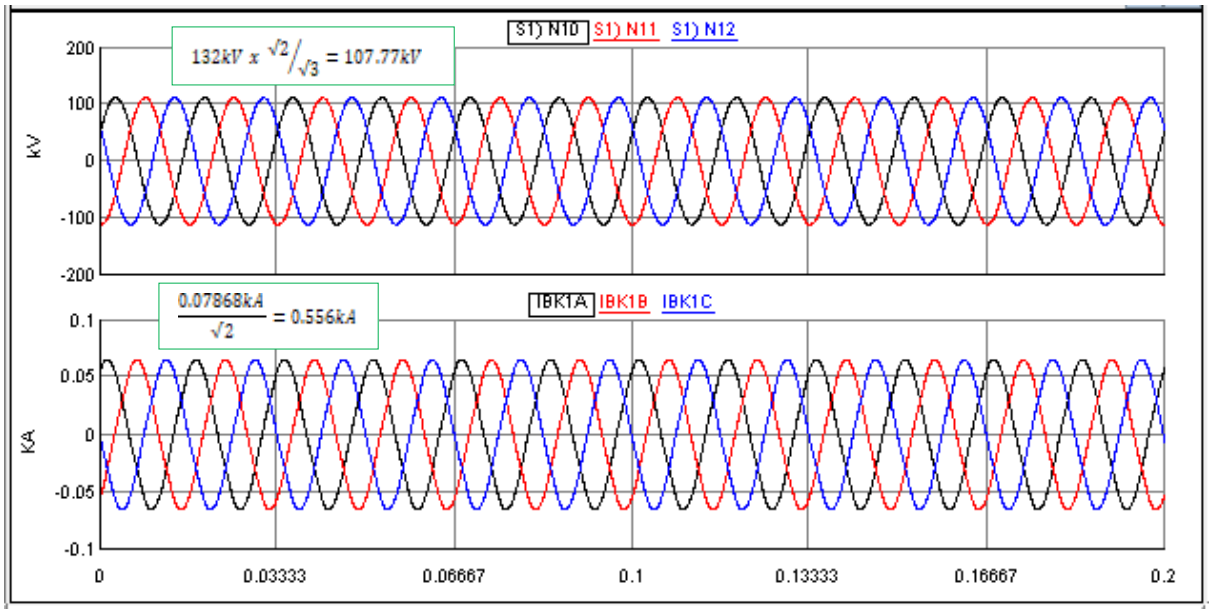


Figure 7.13: Voltage and current signals on the HV side of the power transformer during normal conditions

Figure 7.13 shows the RMS values of voltage and current signals on the primary side of the power transformer flowing through the breaker CB1. N10, N11 and N12 represent each phase voltage connected on bus 4 and IBK1A, IBK1B and IBK1C represent each phase current flowing on the primary side of the transformer.

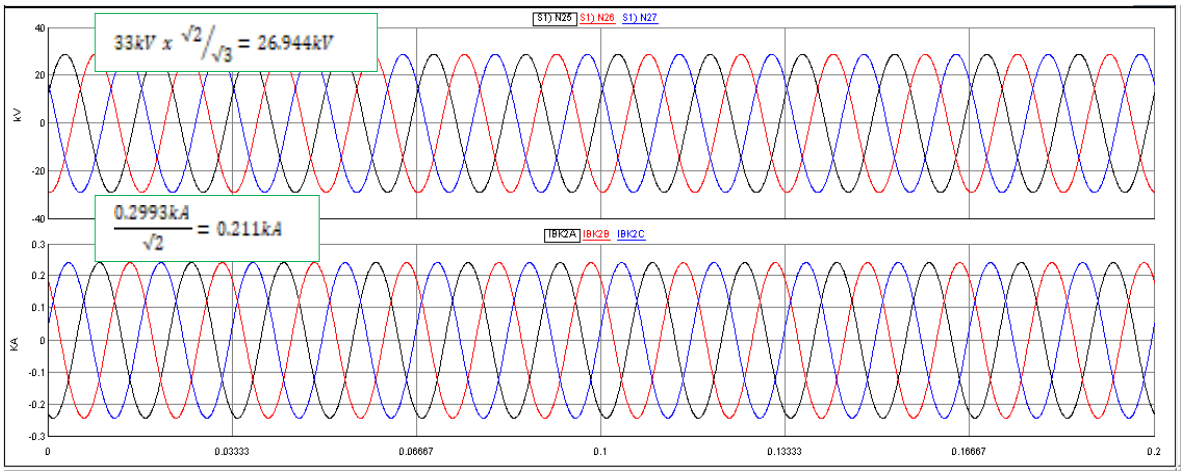


Figure 7.14: Voltage and current signals on the LV side of the power transformer during normal conditions

Figure 7.14 shows the RMS values of voltage and current signals on the secondary side of the power transformer. N25, N26 and N27 represent each phase voltage connected on bus 9 and IBK2A, IBK2B and IBK2C represent each phase current flowing on the secondary side of the transformer.

It is proved that voltage current signals from Figures 7.13 and 7.14 maintain the steady-state values during transformer normal operating conditions.

7.7.1 Simulation results of the transformer differential protection scheme for external fault conditions

The developed transformer differential protection scheme needs to be tested using HIL simulation at CSAEMS at CPUT. For external faults, the differential relay is not expected to trip.

A high magnitude through fault (external fault fed by the transformer) shakes and heats a transformer winding, and the longer the through fault lasts, the greater the risk of it evolving into an internal transformer fault; hence, fast clearing for external faults is part of the transformer protection scheme (ALSTOM Grid, 2011).

The Figures 7.15 and 7.16 show the current, voltage, and trip signals for a single line to ground fault on phase A at Bus 9 of the considered IEEE 14-Bus power system.

Figure 7.15 above shows the voltage and current signals on the HV side of the transformer during a single-phase-to-ground external fault at bus 9 which produced a current magnitude of 600A and the voltage on phase A was reduced to 50kV.

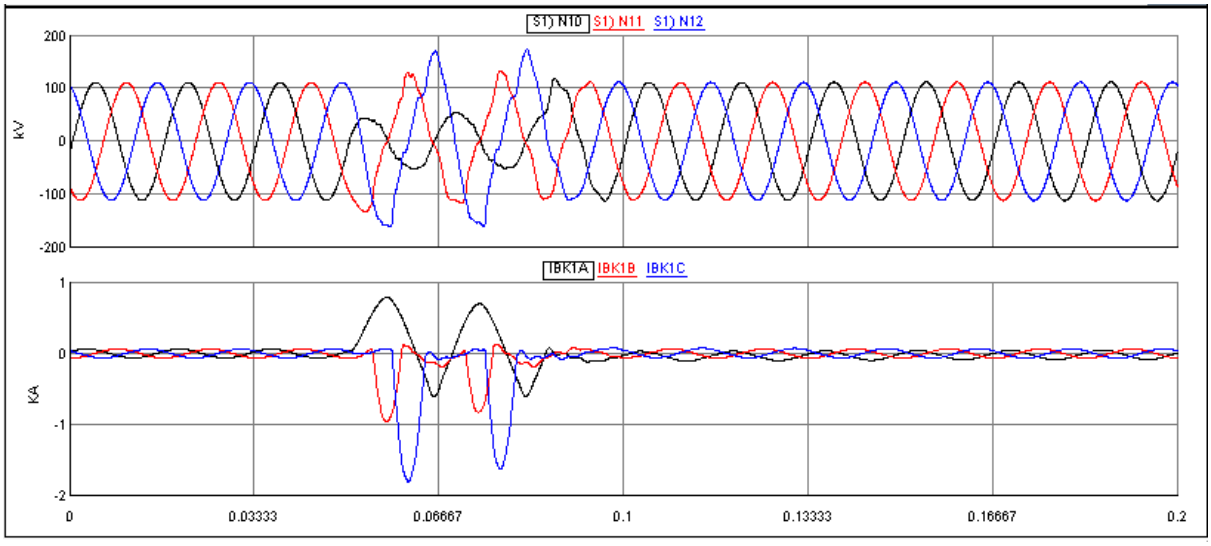


Figure 7.15: Voltage and current signals on the HV side of the transformer for an external LG fault in phase A

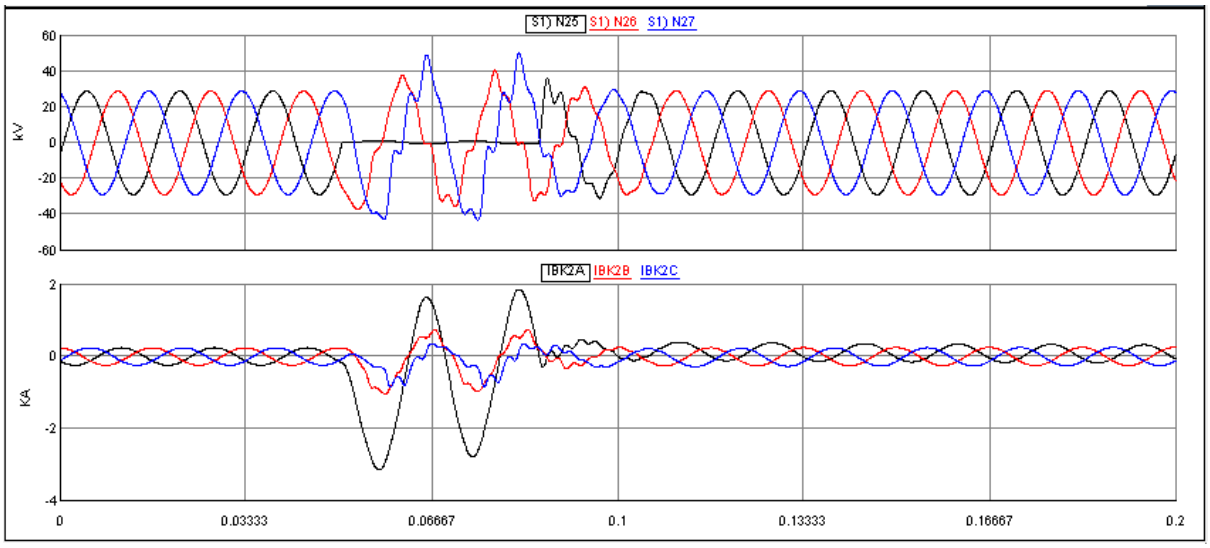


Figure 7.16: Voltage and current signals on the LV side of the transformer for an external LG fault in phase A

Figure 7.16 shows the peak fault current magnitude of almost 2kA obtained from an external single-phase-to-ground fault at bus 9 connected on the secondary side of the power transformer and the corresponding voltage signal was reduced to 0kV on phase A.

An LG short-circuit in phase A was applied at Bus 9. The level of the fault current is high enough, and it depends upon the voltage which has been short-circuited and impedance of the circuit up to the fault point. The simulation results show that the SEL-487E relay is not tripping for the external LG fault.

Figure 7.17 shows SER (Sequential Event Report) from SEL-487E for an external LG fault introduced in phase A on the secondary side of the 3ph power transformer. It is observed that the currents read by the relay are half the amount sent from the HIL simulation this is because of the GTAO's digital to analogue output scaling, and it is the case for all HIL simulation results presented in this chapter.

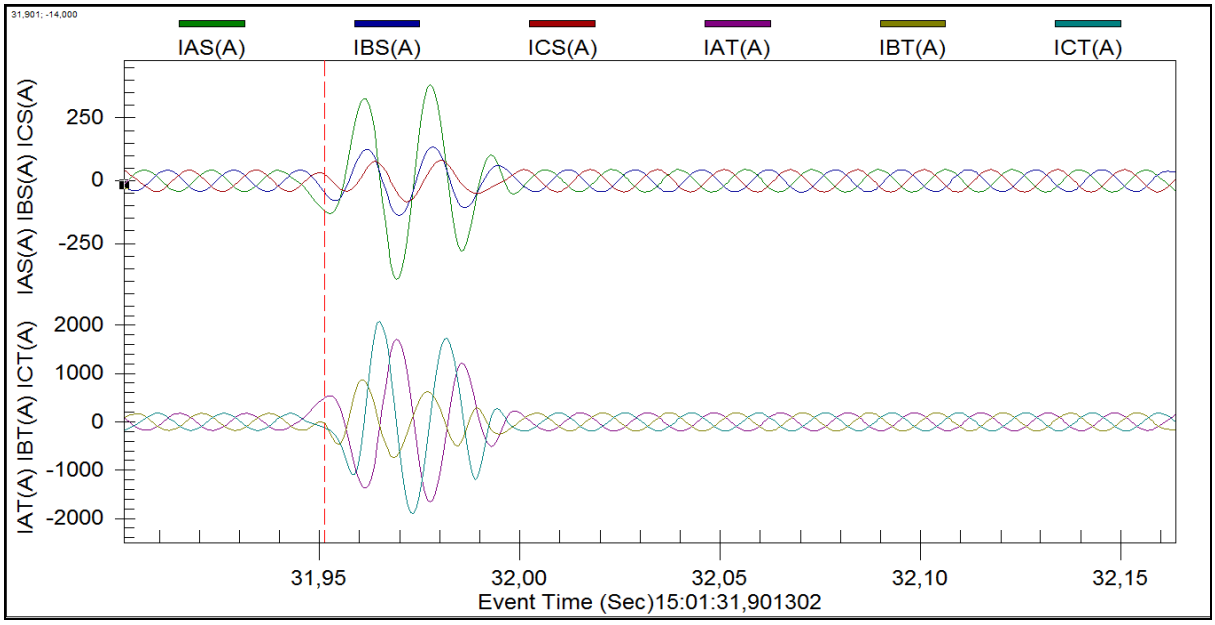


Figure 7.17: S and T windings current signals from the SEL-487E for an external LG fault on LV side of the power transformer (T2)

Figures 7.18 and 7.19 show the current, voltage and trip signals for a double line to ground fault on phases A and B at Bus 9 on considered the IEEE 14-Bus power system.

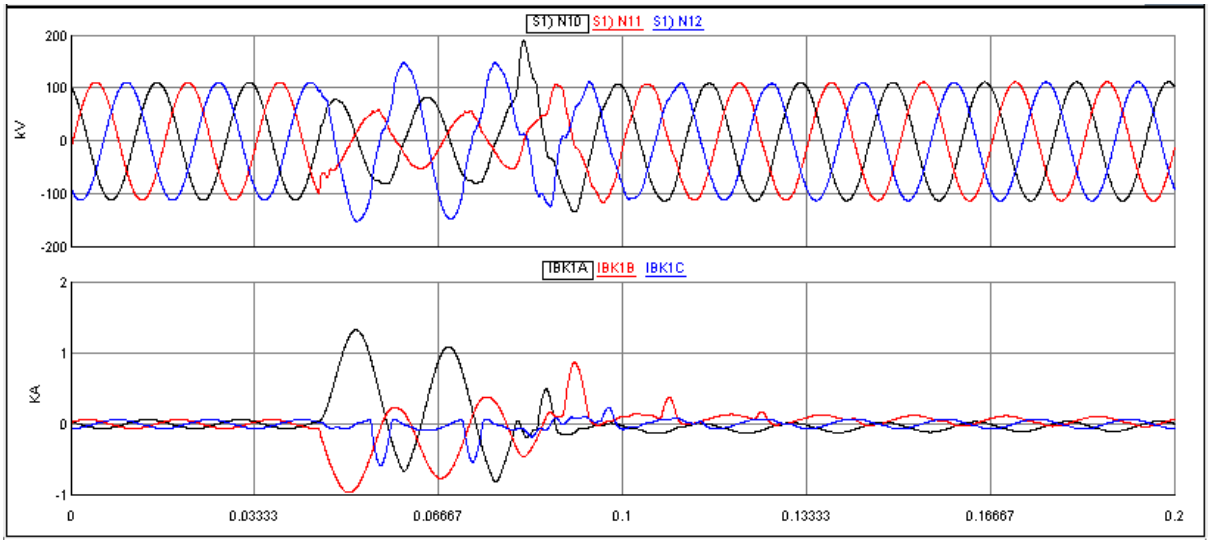


Figure 7.18: Voltage and current signals for an external LLG fault on HV side of the transformer

Figure 7.18 above shows the voltage and current signals on the HV side of the transformer during an external two-phase-to-ground fault at bus 9 which produced a current magnitude of 1kA and the voltage on phases A and B was reduced to 60kV.

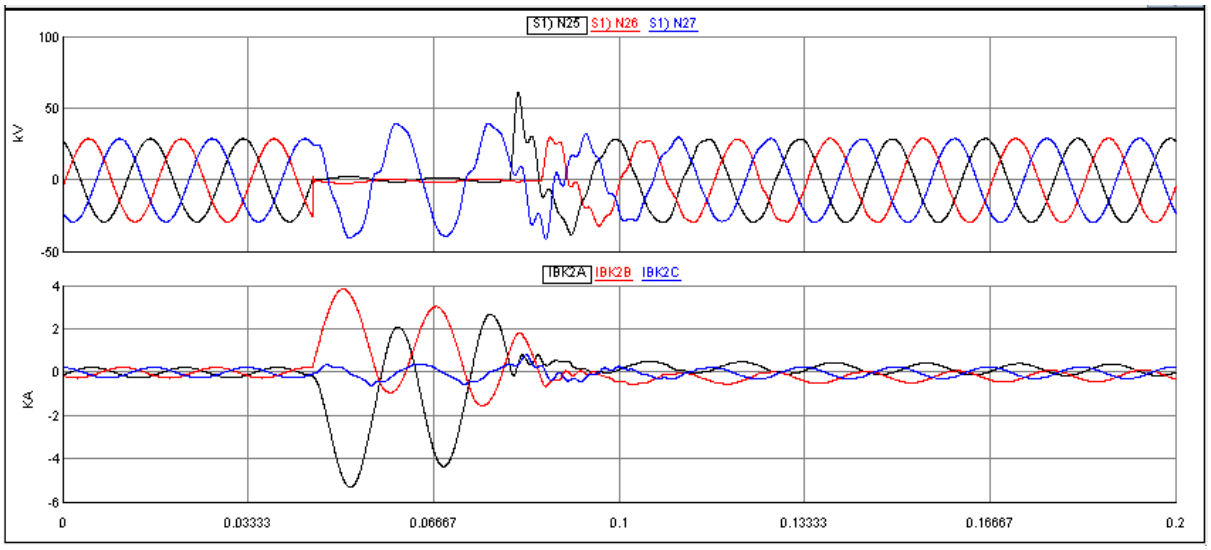


Figure 7.19: Voltage and current signals for an external LLG fault on LV side of the transformer

Figure 7.19 shows the peak fault current magnitude of approximately 4kA for an external two-phase-to-ground fault at bus 9 connected on the secondary side of the power transformer, and the voltage signal was reduced to 0kV on phases A and B respectively. Figure 7.20 shows SER report from SEL-487E for an external LLG fault on LV side of the 3ph power transformer.

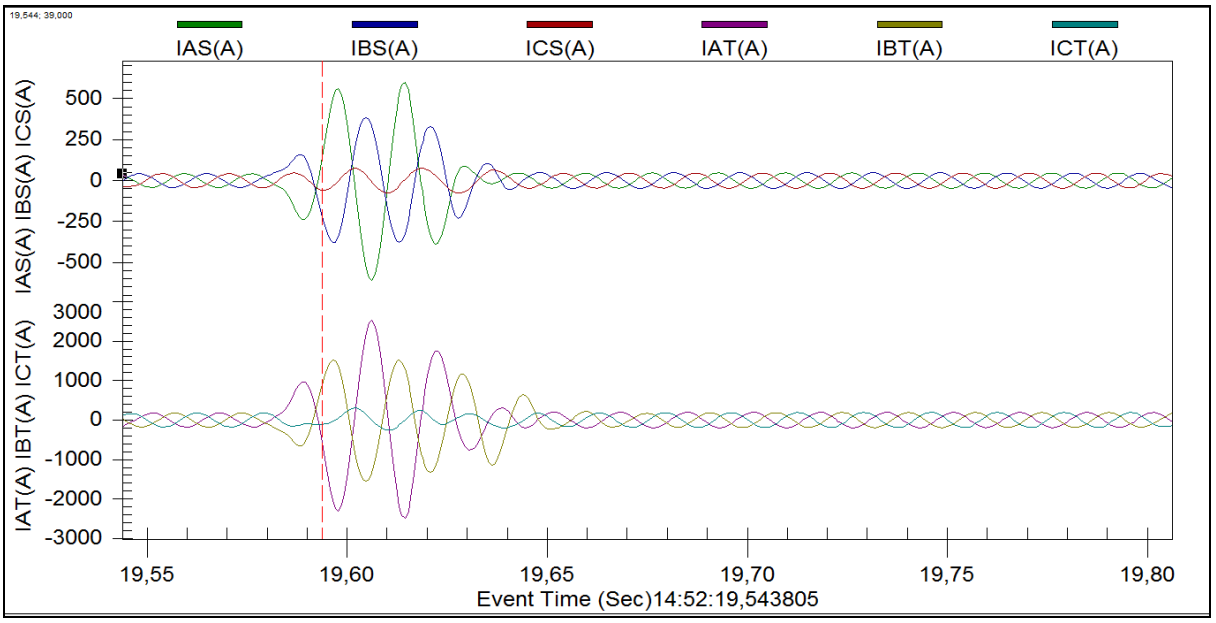


Figure 7.20: S and T windings current signals from SEL-487E for an external LLG fault on LV side of the power transformer (T2)

It can be observed that SEL-487E measures the S and T windings currents signals on the primary and secondary of the transformer respectively. The relay monitors the increase of the currents on S and T windings terminals due to an external fault but does not trip.

Figures 7.21 and 7.22 show the current, voltage and trip signals for a triple line to ground fault at Bus 9 of the considered IEEE 14-Bus power system.

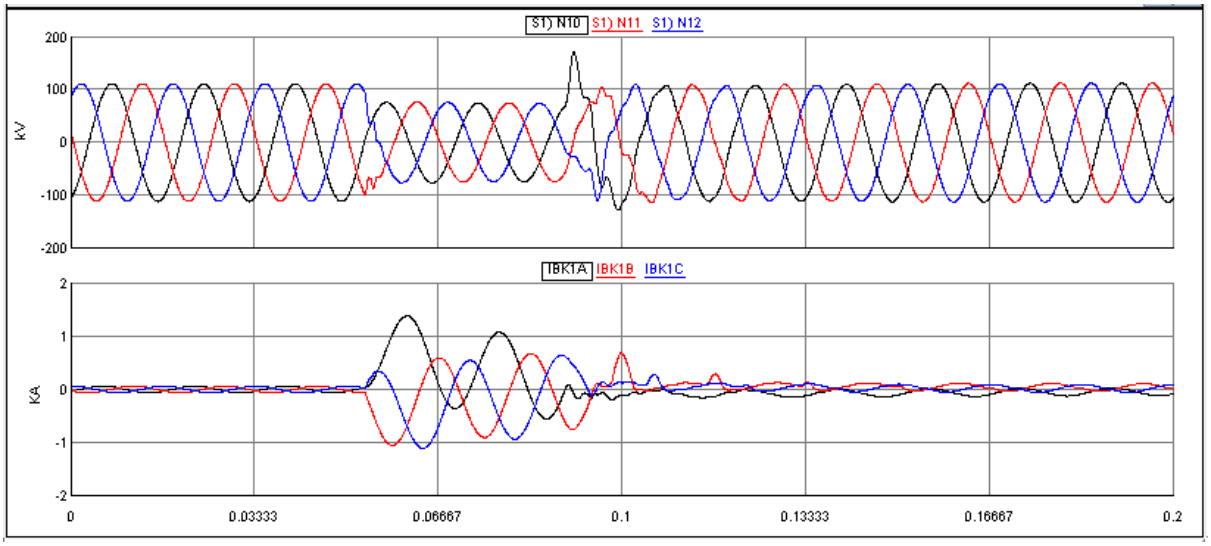


Figure 7.21: Voltage and current signals for an external LLLG fault on HV side of the transformer

Figure 7.21 above shows the voltage and current signals on the HV side of the transformer during an external three-phase-to-ground fault at bus 9 which produced a current magnitude of 1kA and the voltage on phases A, B and C was reduced to 60kV.

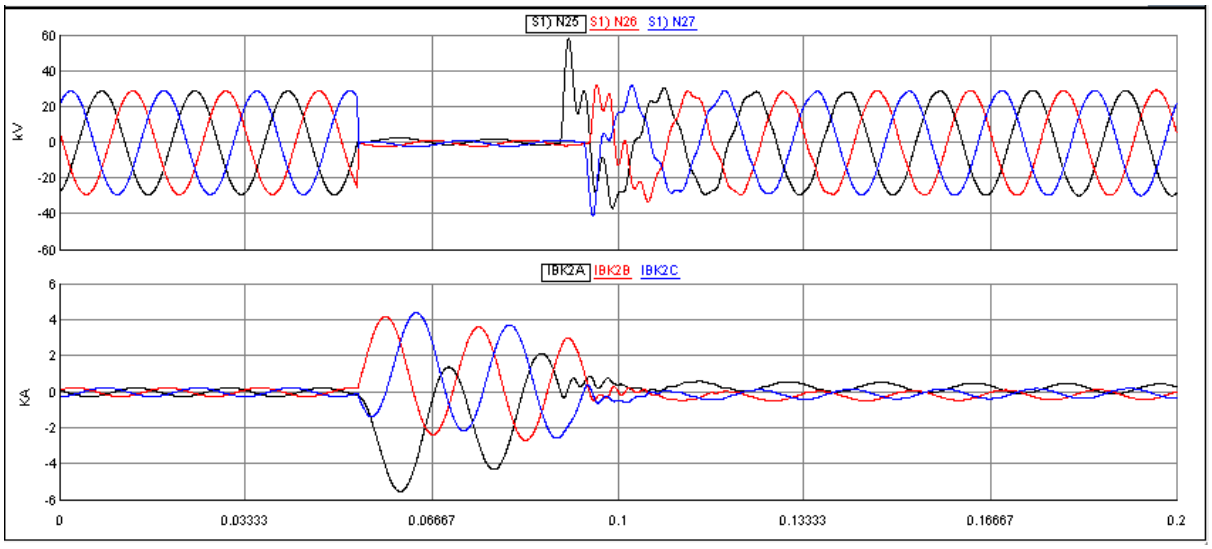


Figure 7.22: Voltage and current signals for an external LLLG fault on LV side of the transformer

Figure 7.22 shows the peak fault current magnitude of approximately 4kA simulated for an external three-phase-to-ground fault at bus 9 on the secondary side of the power transformer, and the voltage signal is reduced to 0kV on phases A, B and C respectively.

Figure 7.23 shows the SER report from SEL-487E for an external LLLG fault introduced in phases A, B and C at LV side of the 3ph power transformer. SEL-487E monitors half of the current signals simulated in RSCAD software environment, i.e. 500A and 2kA on S and T windings respectively, and the relay does not send trip for this external fault condition.

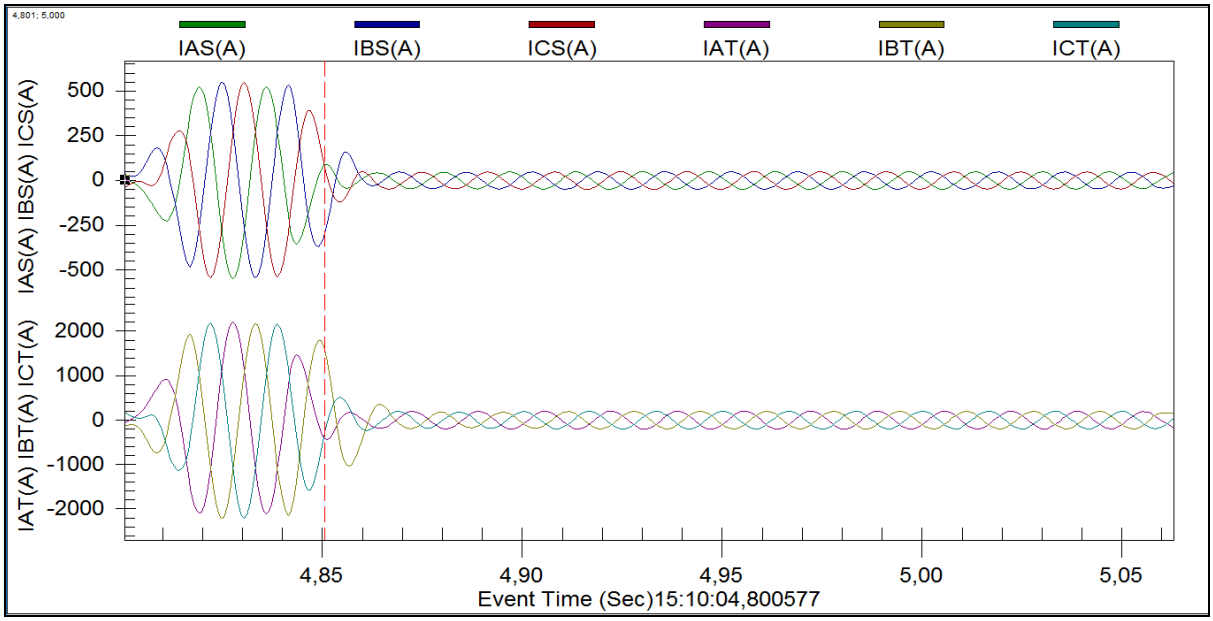


Figure 7.23: S and T windings currents signals from SEL-487E for an external LLLG fault on LV side of the power transformer (T2)

7.7.2 Simulation results of the transformer differential protection scheme for Internal fault conditions

Transformer Differential protection schemes are mainly used to protect against phase-to-phase fault and phase to earth faults. Usually, the operating coil carries no current as the current is balanced on both the side of the power transformers. When the internal fault occurs in balanced transformer windings is disturbed, and the operating coils of the differential relay carry current corresponding to the difference of the current among the two windings of the transformers and the differential relay trips the main circuit breakers on both sides of the power transformers.

7.7.2.1 Trip logic for transformer unit faults

This section provides the trip logic for transformer unit faults. The trip output of the A-phase differential element asserts relay word bit 87RA. The assertion of 87RA asserts

Relay Word bit 87R. Relay Word bit 87R is the OR combination of the outputs from the A-, B-, and C-phase differential elements (SEL-487E instruction manual, 2012). This means once a trip output is issued even from a single-phase-to-ground fault, all the phases of circuit breakers on both sides will open.

In Figure 7.24, the Transformer Trip timer starts when SELOGIC control equation TRXFMR asserts for one processing interval. The assertion of this equation immediately asserts output TRPXFMR. Output TRPXFMR remains asserted for the Minimum Trip Duration timer (TDURD) setting regardless of the status of input TRXFMR. When output TRPXFMR asserts, the logic seals TRPXFMR in through the AND gate under the following conditions (SEL-487E instruction manual, 2012):

- SELOGIC control equation RSTTRGT is de-asserted (global setting)
- The target reset (TRGTR) input is de-asserted
- The unlatch input (ULTXFMR) is de-asserted
- The ECTTERM setting includes the terminal name

Relay Word Bit TRGTR asserts when either the front panel TARGET/RESET pushbutton is pressed, or the ASCII TAR R command is issued.

Once latched, TRPXFMR remains asserted until any (or all) of the following happens (SEL-487E manual, 2012):

- SELOGIC control equation RSTTRGT asserts
- The target reset (TRGTR) input asserts
- The unlatch input (ULTXFMR) asserts

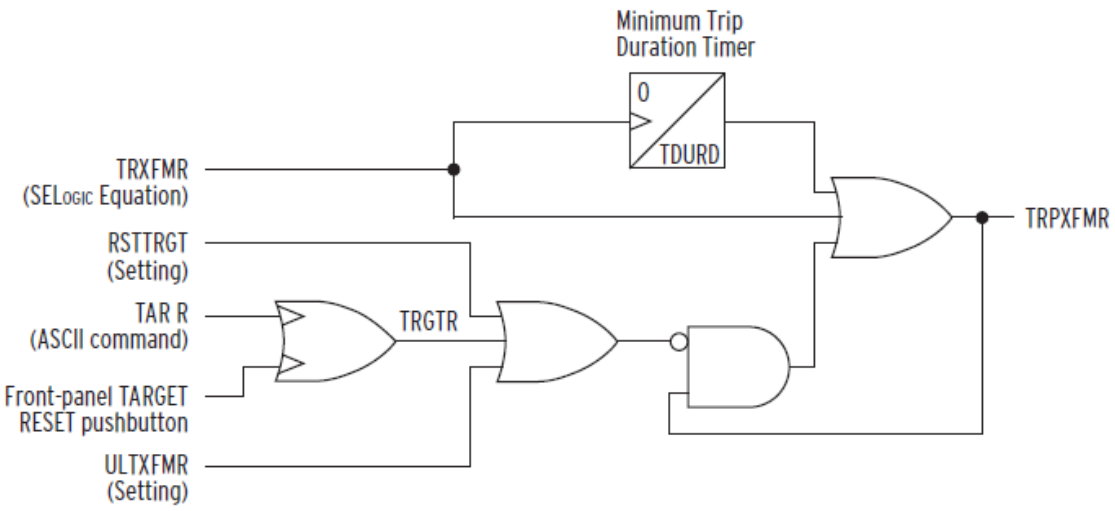


Figure 7.24: Transformer trip Logic for unit faults

Where

TRXFMR is Transformer trip equation asserted

TRPXFMR is Transformer trip output asserted

TDURD is the Minimum trip duration

RSTTRGT is the Reset front panel targets

TRGTR is the Target reset

TAR R is Command used to reset any latched relay targets resulting from a tripping event

ULTXFMR is the Unlatch transformer trip

The Figures 7.25 and 7.26 show the current, voltage and trip signals for an internal single line to ground fault on phase A on the low voltage side of transformer T2 of the considered IEEE 14-Bus power system.

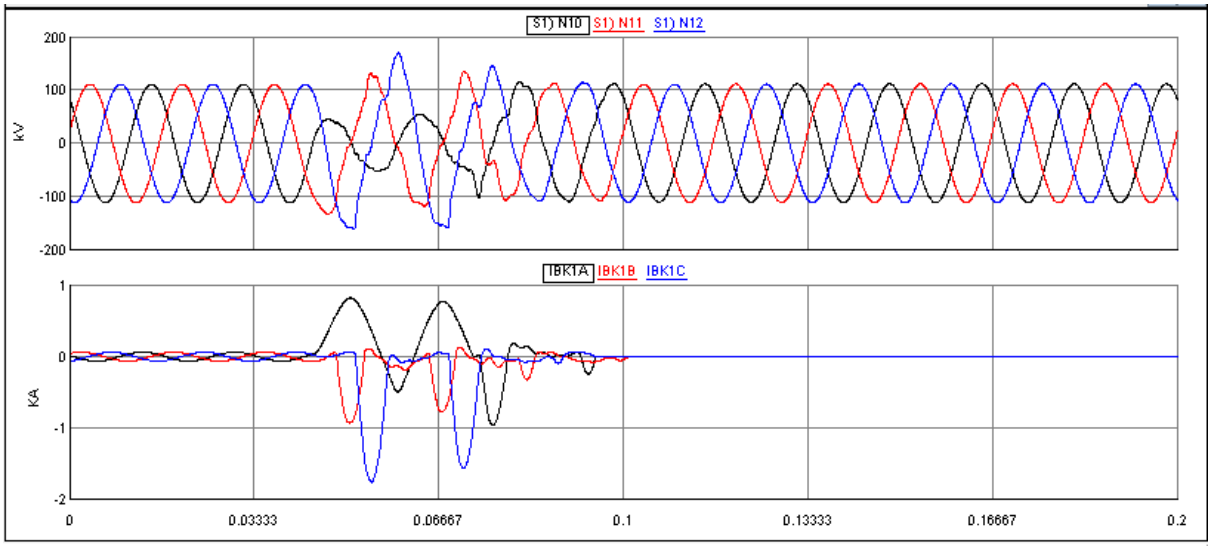


Figure 7.25: Voltage and current signals for an internal LG fault on HV side of the transformer

As shown in Figure 7.25 above, the internal LG fault resulted in a current magnitude of 1kA and 50kV in the faulted phase.

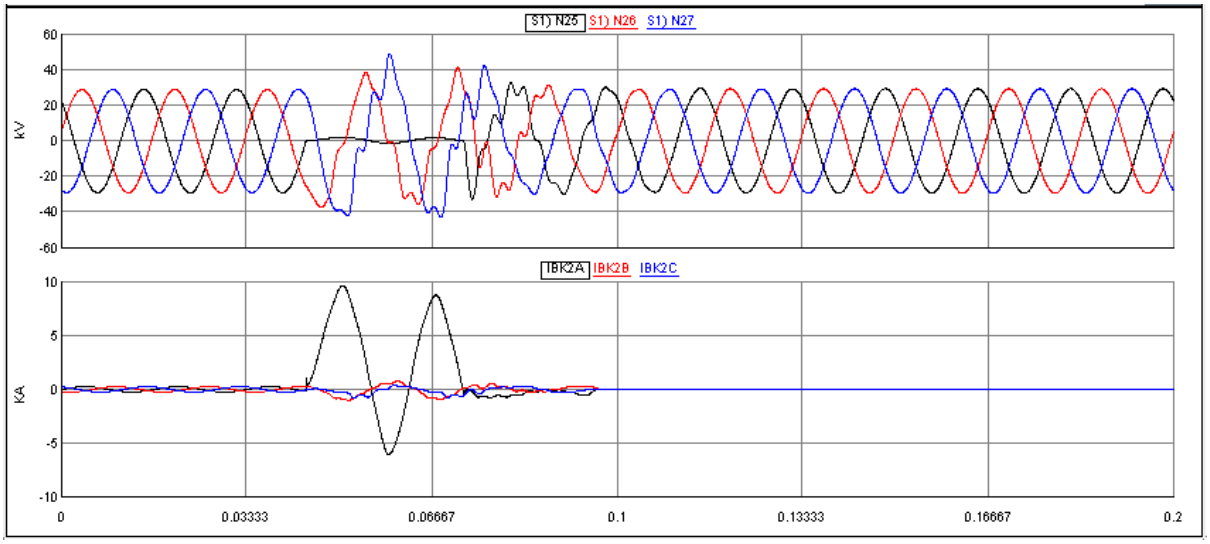


Figure 7.26: Voltage and current signals for an internal LG fault on LV side of the transformer

From Figure 7.26 above, the peak fault current magnitude for internal single-phase-to-ground is approximately 5kA and the voltage is 0kV in the faulted phase. It is observed that the trip signal sent by the SEL-487E open the breakers.

In Figure 7.27, the trip signal IATRIP shifts from binary “0” to “1” as soon as the fault signal FLTSIGI (internal fault) is introduced and the circuit breaker CB1 shifts from binary “1” to “0” approximately after 12ms. This trip signal logic is the same for other types of internal faults.

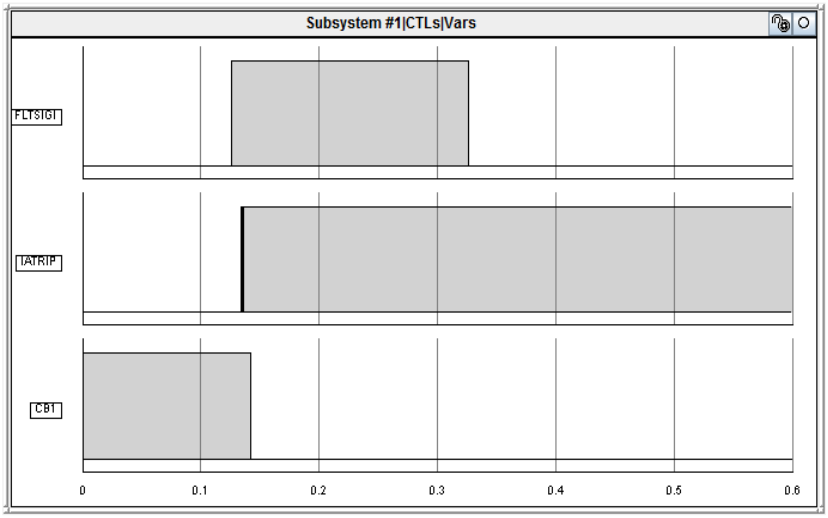


Figure 7.27: Digital trip and circuit breaker signal for an internal LLLG fault

Figure 7.28 below shows that SEL-487E SER report for an internal LG fault on LV side of the 3ph power transformer.

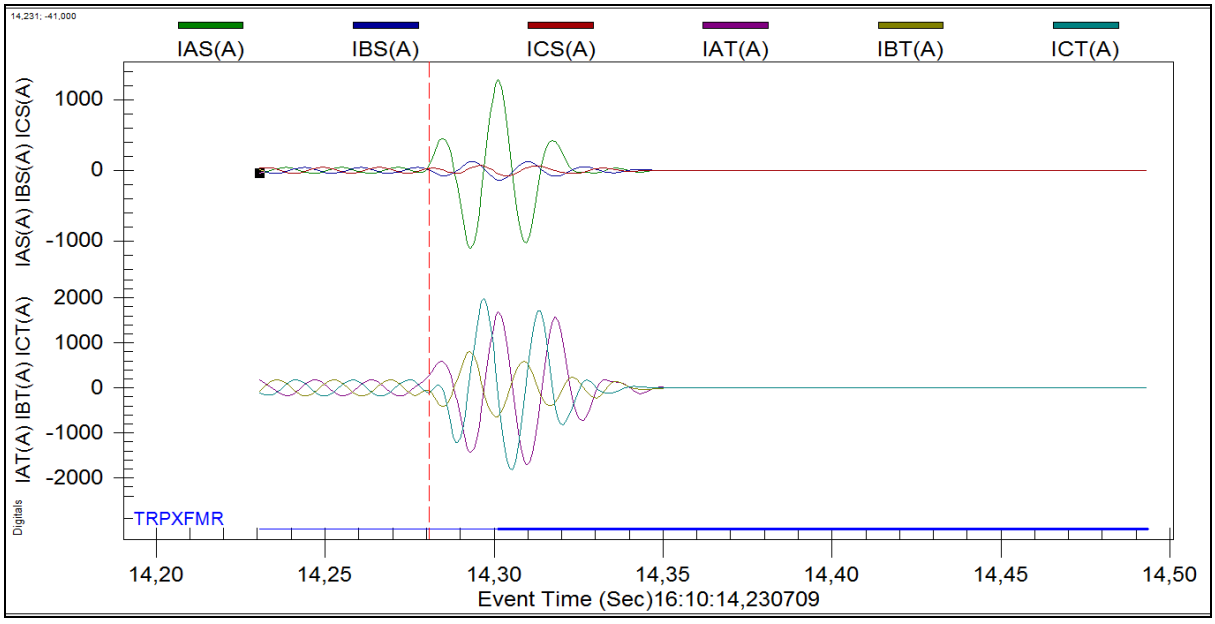


Figure 7.28: S and T winding current signals from SEL-487E for an internal LG fault on LV side of the transformer (T2)

It can be observed that TRPXFMR (Trip Transformer) element is asserted as soon as the fault is simulated with a small delay allowing the breakers to open.

The Figures 7.29 and 7.30 show the current, voltage and trip signals for an internal double line to ground fault on the low voltage side of transformer T2 of the considered IEEE 14-Bus power system.

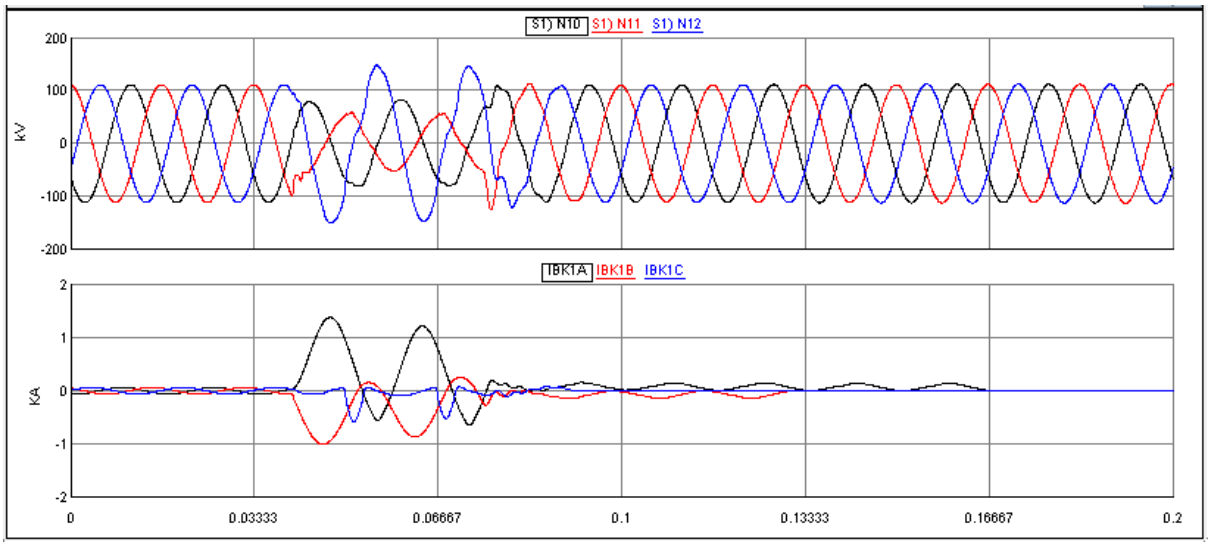


Figure 7.29: Voltage and current signals for an internal LLG fault on HV side of the transformer

As depicted in Figure 7.29 above, the LLG fault resulted in a current magnitude of 1.5kA and the 60kV voltage in the faulted phases A and B. It is observed that the current signals reach zero amperes after the trip signal feedback issued by the SEL-487E.

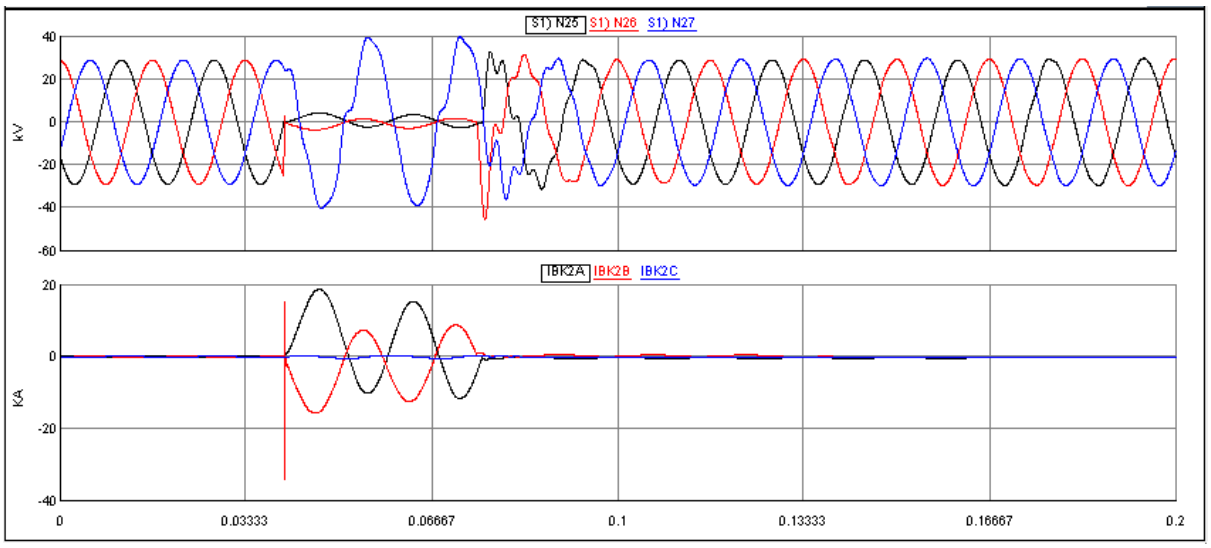


Figure 7.30: Voltage and current signals after an internal LLG fault on LV side of the transformer

From Figure 7.30 above, the peak current fault magnitude for an internal single-phase-to-ground is approximately 20kA and 0kV voltage in the faulted phases A and B. It is observed that the SEL-487E relay trip signal open the breakers.

Figure 7.31 shows SER report from SEL-487E for an internal LLG fault on the LV side of the 3ph power transformer. It can be seen that TRPXFMR (Transformer Trip Output) element is asserted as soon as the internal transformer fault was applied with a small delay allowing the circuit breakers to open.

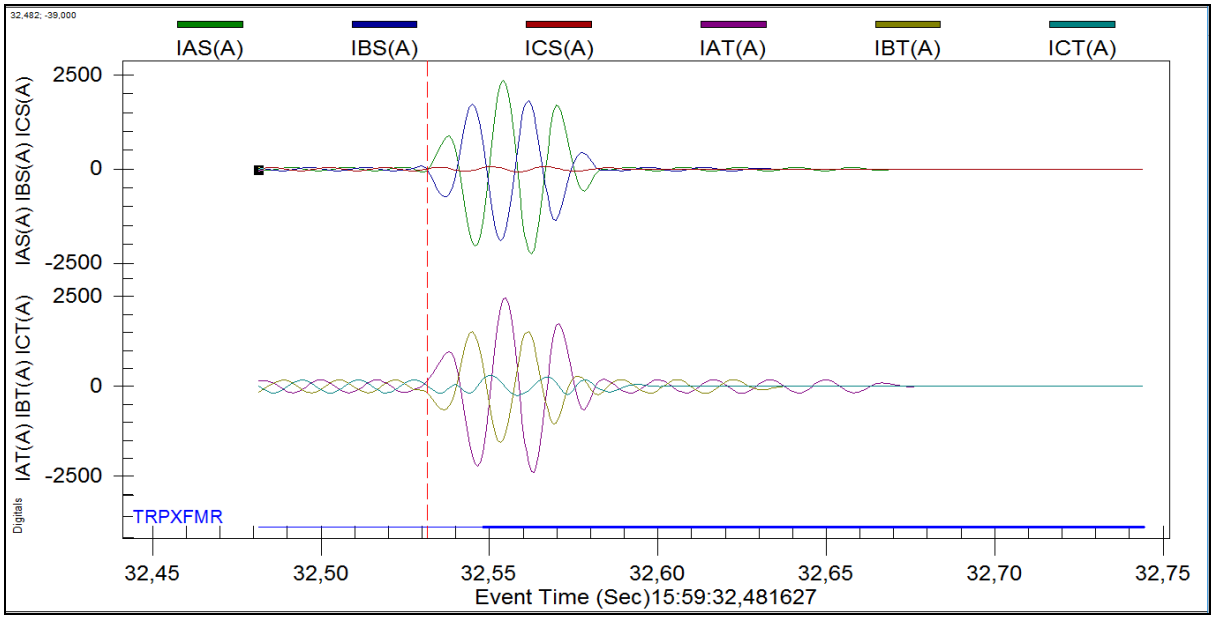


Figure 7.31: S and T winding current signals from SEL-487E for an internal LLG fault on LV side of the transformer (T2)

The Figures 7.32 and 7.33 show the current, voltage and trip signals for an internal triple line to ground fault on the low voltage side of transformer T2 of the considered IEEE 14-Bus power system.

The internal three-phase fault at the LV side of the power transformer produced a current magnitude of 1kA and voltage reduced to 60kV as shown in Figure 7.32. It is observed that SEL-487E relay issues a trip signal and the current signals reach zero.

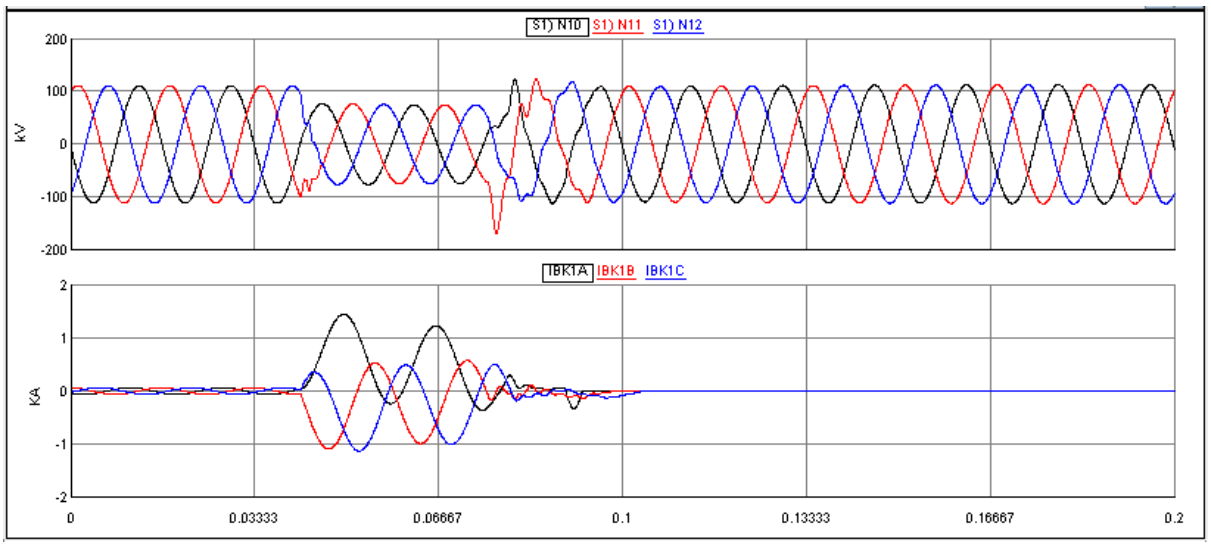


Figure 7.32: Voltage and current signals for an internal LLLG fault on HV side of the transformer

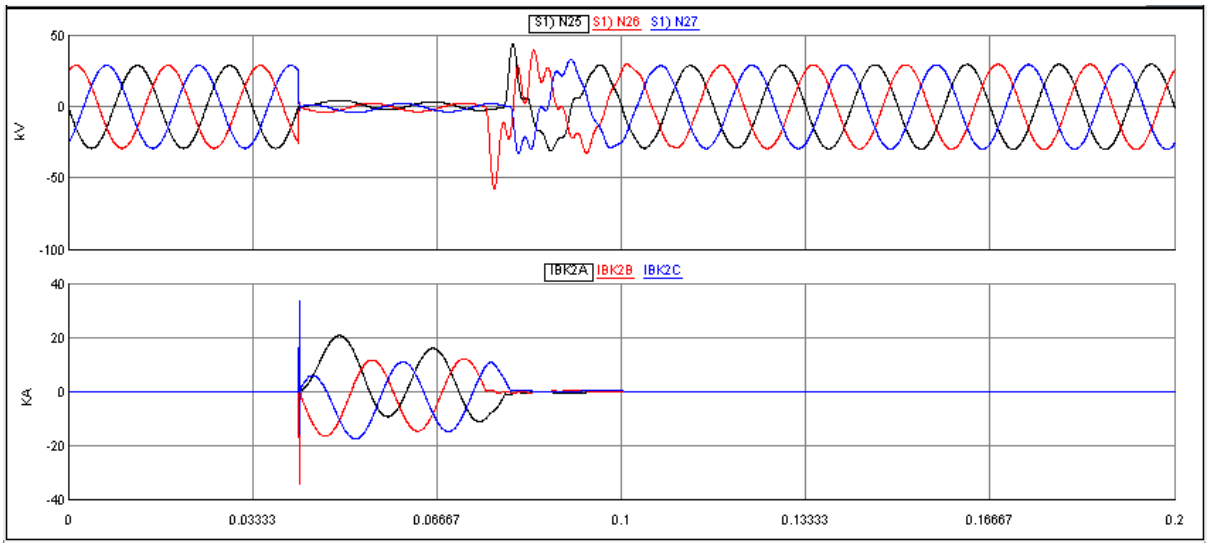


Figure 7.33: Voltage and current signals after an internal fault LLLG on LV side of the transformer

From Figure 7.33 above, the peak fault magnitude for an internal three-phase-to-ground is 20kA, and the 0kV voltage in the faulted phases A, B and C. It is observed that the SEL-487E relay trip signal open the breakers.

Figure 7.34 shows SER report from SEL-487E after an internal LLLG fault was introduced in phase A, B and B on LV side of the 3ph power transformer. It can be observed that TRPXFMR (Transformer Trip Output) element is asserted as soon as the internal transformer fault was applied with a small-time delay allowing breakers to open.

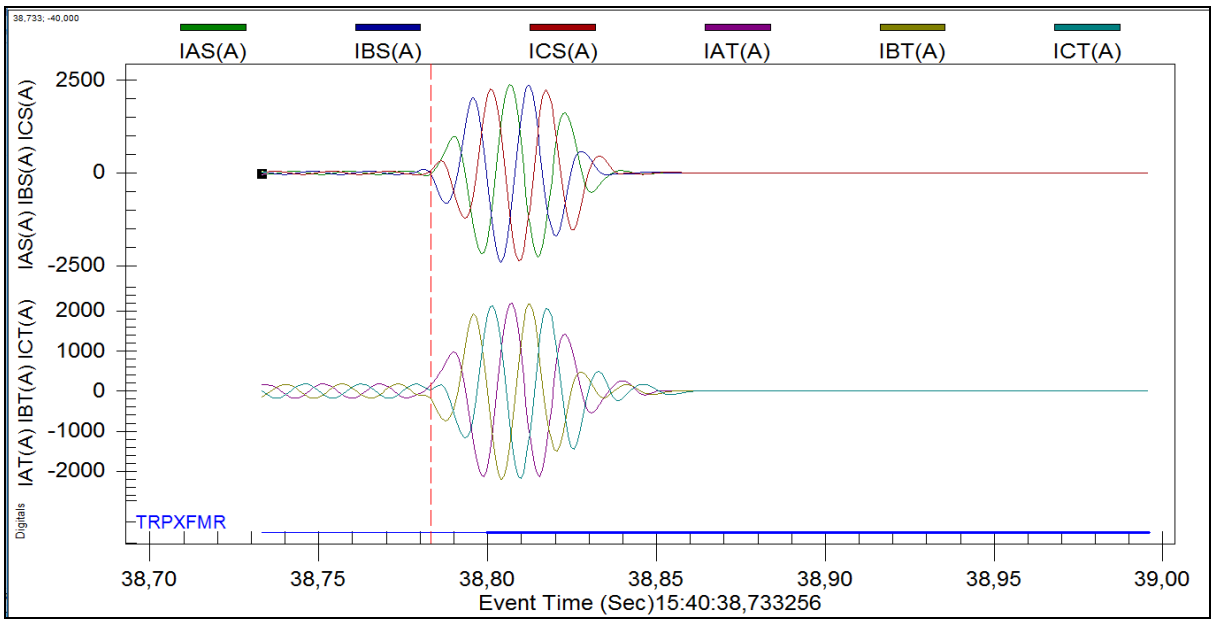


Figure 7.34: S and T winding current signals from SEL-487E for an internal LLLG fault on LV side of the transformer

7.8 Case study one: Simulation results analysis for the transformer inrush current condition

The current required by the magnetic circuit of a power transformer during a step change in the voltage terminals can be quite large. The magnetic nature of a transformer requires an excitation current to be drawn from the power source to create the necessary magnetic flux. The magnetic flux lags the system voltage and can be retained by a transformer de-energisation because of the hysteresis loop of the steel core (John H. Brunke and Klaus J. Frohlich, 2001). This retention or residual flux may have an adverse effect on the inrush current when a voltage is re−applied to the transformer.

7.8.1 Analysing the transformer inrush current condition during steady state operating condition

If energisation occurs at a voltage zero−crossing the flux required should be at or near the maximum negative value. Assuming the transformer residual flux is at zero, then the flux starts to increase and continues to increase until 2 times the normal flux. This increase in flux would have been larger had the residual flux been at a positive value and would have been smaller had the residual flux been at a negative value (John H. Brunke and Klaus J. Frohlich, 2001). The rated flux and flux knee point value can be calculated using Equations 7.3 and 7.4 respectively.

$$\Phi_{rated} = \frac{V_{pk}}{2\pi f} \tag{7.3}$$

$$\Phi_{knee} = K * \Phi_{rated} \quad (7.4)$$

Where

Φ_{rated} is the rated flux of the transformer;

V_{pk} is the primary peak voltage;

f is the system frequency;

Φ_{knee} is the transformer flux knee point;

K is a constant

Figure 7.35 shows the transformer flux requirement when the circuit breaker (CB1) is closed at a zero crossing for A phase. The calculated flux is 0.3501kWb using Equation 7.3, and the peak flux of the transformer core is shown in Figure 7.35.

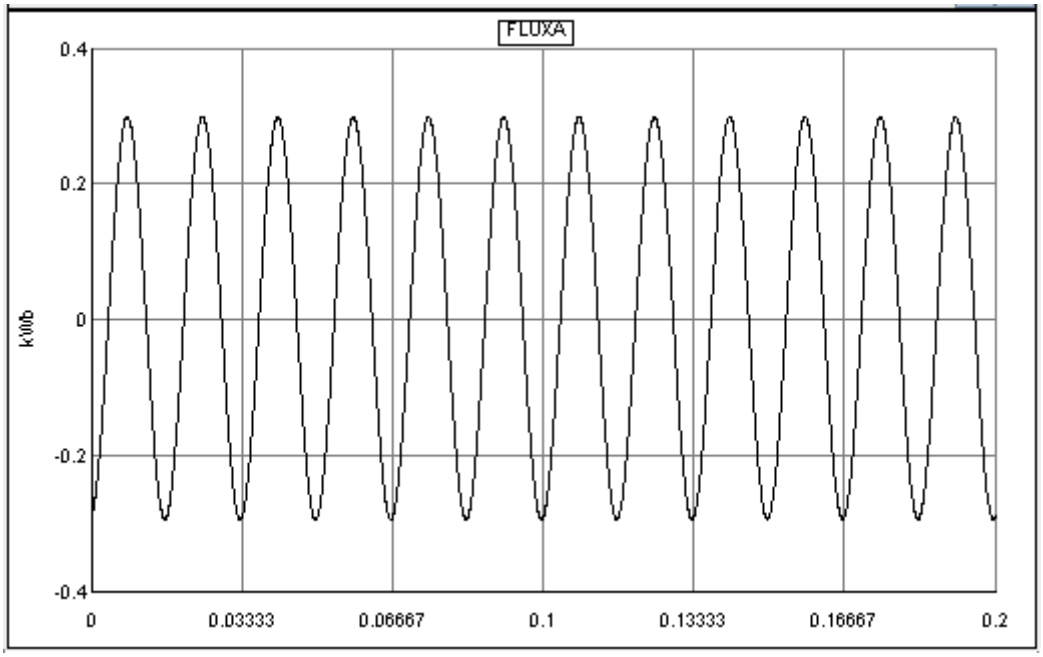


Figure 7.35: Transformer T2 peak flux in the steady-state condition

The greater than normal flux requirements during energisation causes a large exciting current to be drawn from the system. Transformers are designed for efficiency and typically operate at the knee point of a saturation curve. The transformer will saturate very quickly, and the maximum inrush current may be 8 − 30 times the normal full load current. The inrush current can eventually decay to normal excitation levels over time (Blakburn J. L, 1998). The decay time varies with respect to the residual flux, size of the transformer, system L/R ratio, and transformer iron type.

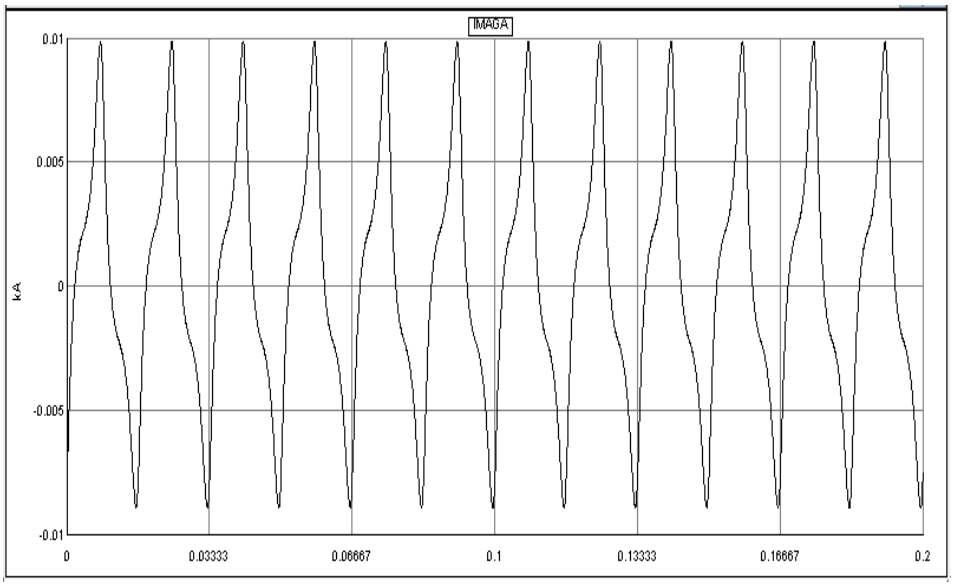


Figure 7.36: Transformer (T2) Magnetizing current in steady state condition

The magnetizing inrush current required by the magnetic circuit of a power transformer can contain a large second harmonic component. This second harmonic content has been used as the signature to determine a magnetizing inrush condition. This signature recognition is an important part of a transformer differential relay, as the relay should only operate for valid fault conditions. The harmonic content of power transformer magnetizing inrush current can range from 7% to 15% or more. Generally, the newer transformers which have a more efficient design and steel core will have the lesser harmonic content (Blakburn J.L, 1998). B-H loop of the power transformer is shown in Figure 7.37 below.

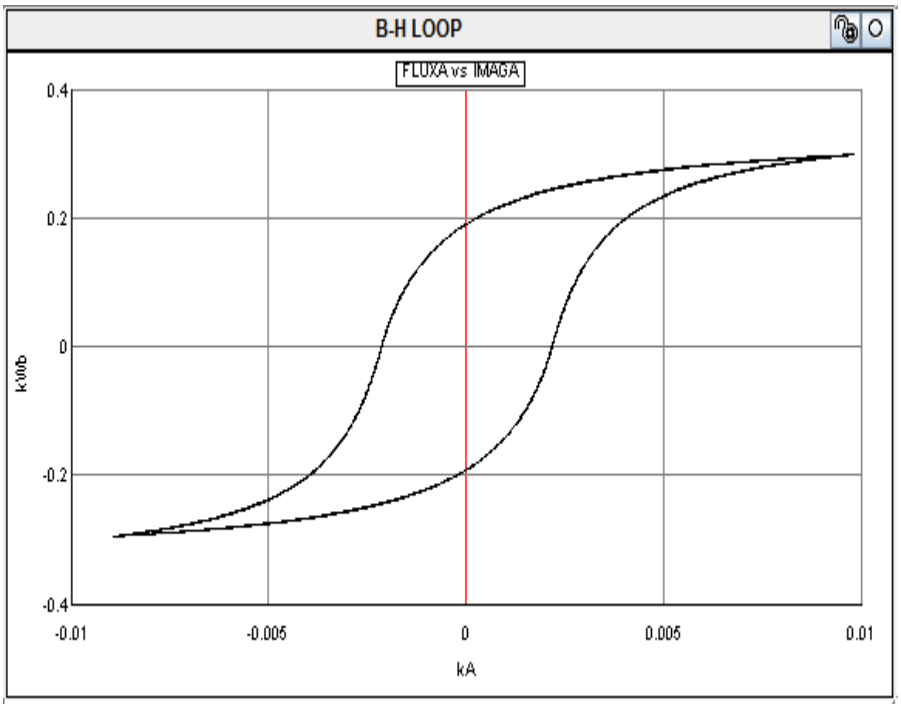


Figure 7.37: B-H LOOP of the transformer (T2) in steady-state condition

7.8.2 De-energisation of the power transformer

A power transformer can be subjected to many conditions that may cause a magnetizing inrush condition to occur. These conditions are commonly referred to as initial, recovery, and sympathetic inrush.

To de-energise the transformer, the breakers are open by pressing the CB1OPEN and CB2OPEN pushbuttons in RUNTIME as shown in Figure 7.12 in section 7.7. The residual flux can now be measured from FLUXA plot. The residual flux is 0.19kWb, which is 63.33% of the rated flux and is in the range. Typically, the residual flux is 20-70% of the rated flux.

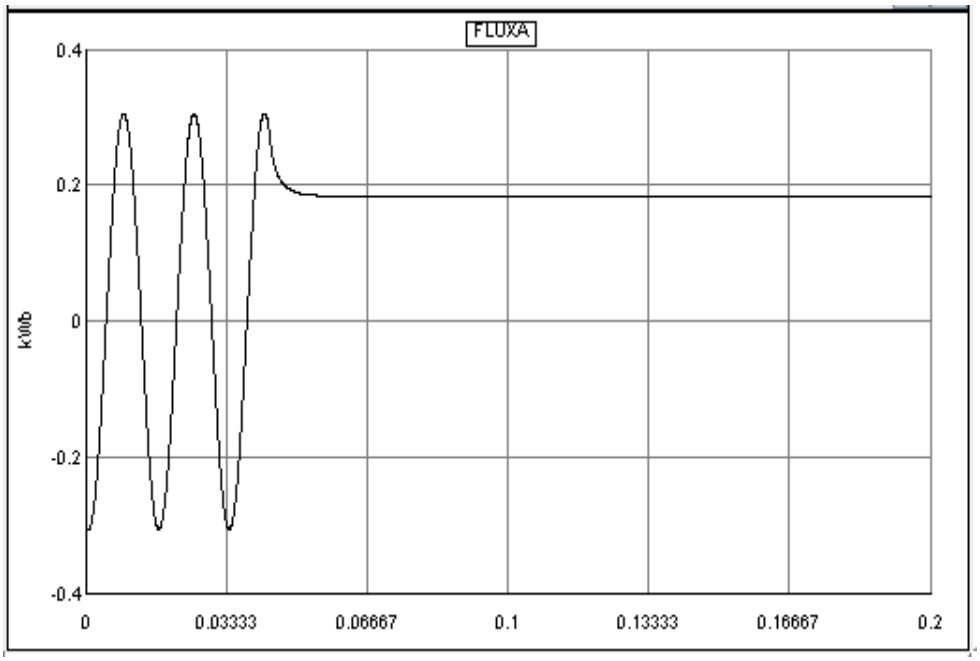


Figure 7.38: Transformer residual flux when the circuit breakers are open

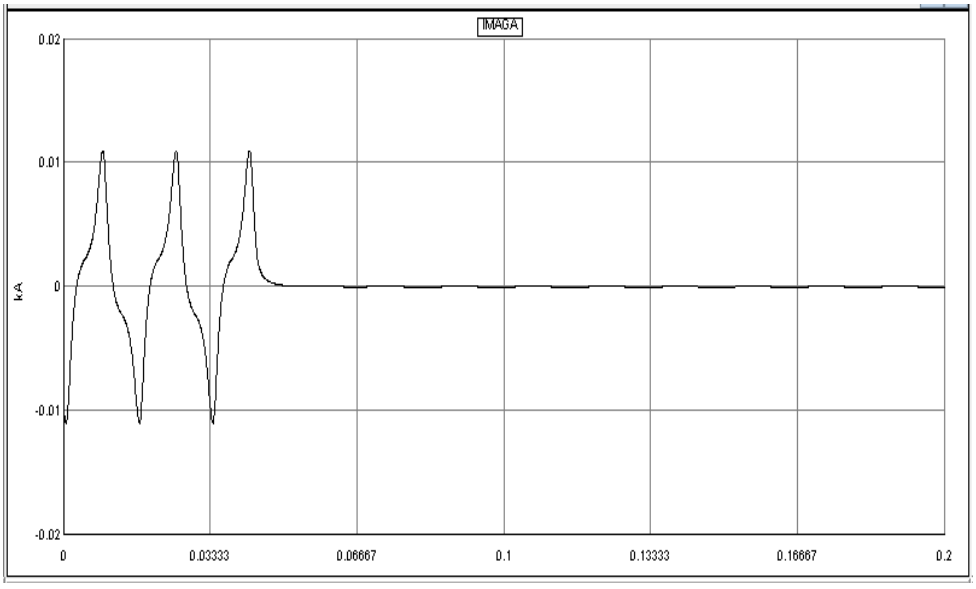


Figure 7.39: Magnetizing current of the Transformer during de-energisation

It is observed from Figure 7.39 the transformer magnetizing current ranges from 10A to zero due to circuit breakers switching event.

7.8.3 Energisation of the power transformer

To re-energise the transformer, the breakers are closed by pressing CB1CLOSE and CB2CLOSE pushbuttons in RUNTIME. With the POWT slider set to 0, the transformer is energised by closing the breakers as shown in Figure 7.12 in section 7.7. The magnetizing inrush current currents reach a magnitude of 0.62kA. Referring to the B-H loop, it can be seen that, the transformer has saturated.

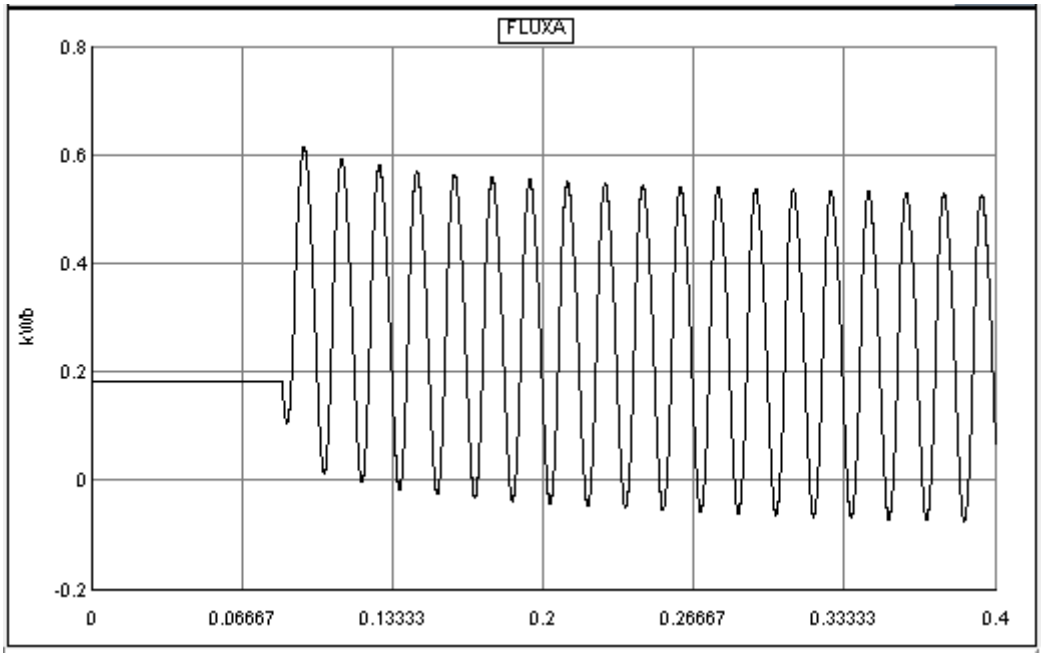


Figure 7.40: Transformer flux during energization

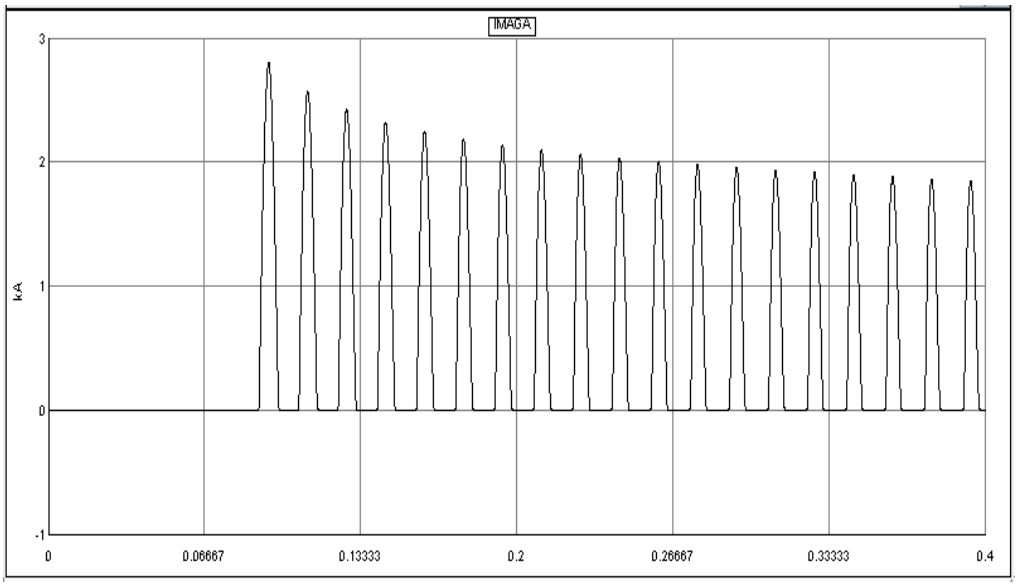


Figure 7.41: Transformer magnetizing Inrush current during energisation

The simulation results of the transformer provide the knee point flux and air core inductance can be determined using the B-H curve. The flux knee point can be found by defining a line asymptotic to the non-linear segment of the saturation curve. The intersection of the current in the x-axis with the flux knee point in y-axis as shown in Figure 7.42.

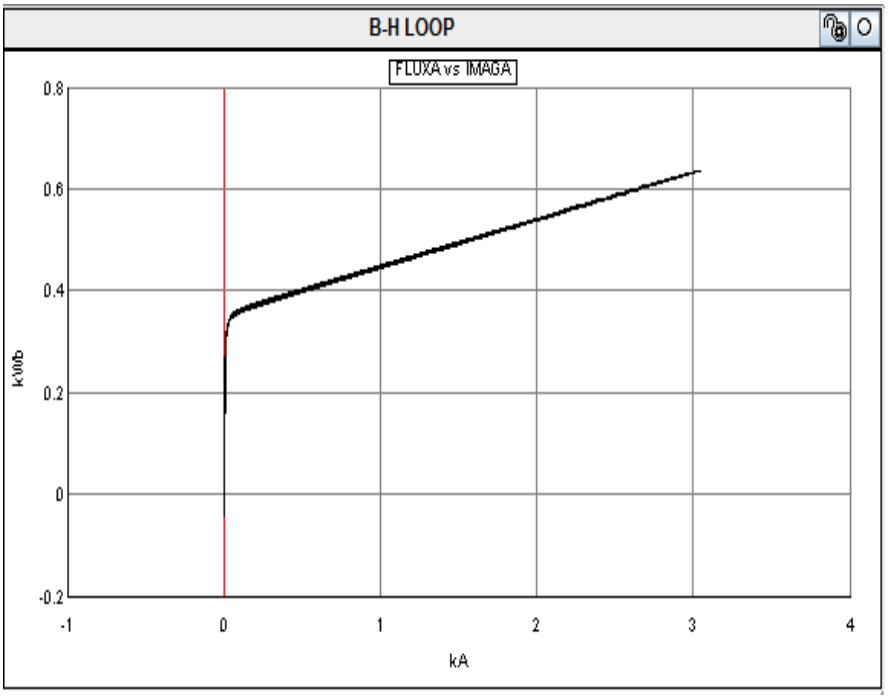


Figure 7.42: Transformer Flux Knee Point

From Figure 7.43, it is observed that the RSCAD software overcurrent relay model issues a trip signal after the breakers are closed.

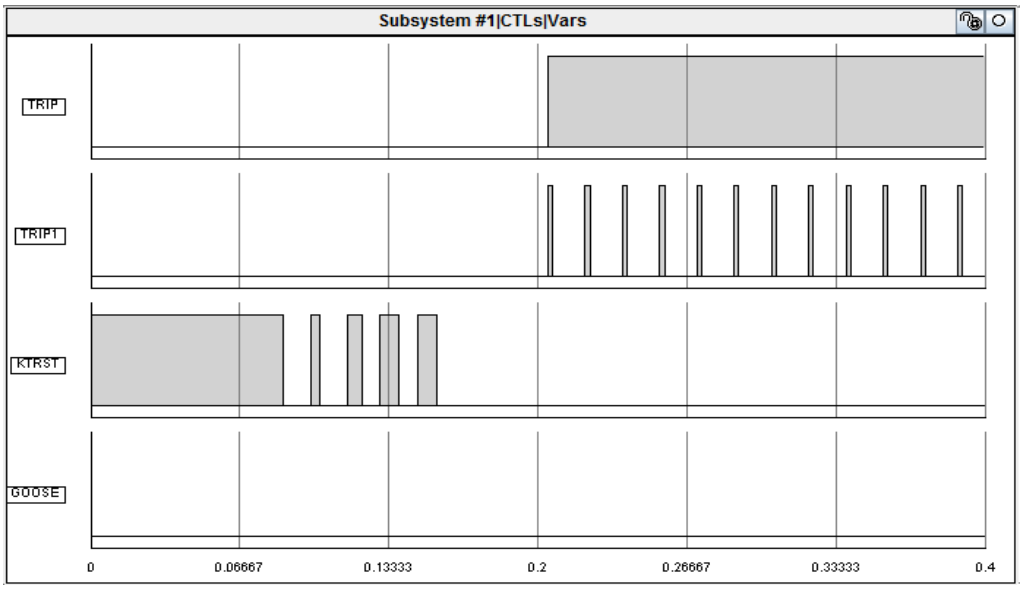


Figure 7.43: Trip signals from RSCAD software overcurrent relay during inrush conditions

Because the magnetizing inrush currents resemble the fault currents. Subsequently, the measured RMS current is above the minimum pickup level when the breaker closes. Even though the magnetizing inrush current is not a fault, it can be confirmed that the backup overcurrent relay is mal-operating during inrush conditions as shown in Figure 7.43.

7.9 Case study two: IEC 61850 GOOSE message based reverse harmonic blocking scheme for the transformer magnetizing inrush current

Case study two analyses the result of the developed reverse harmonic blocking scheme. The backup overcurrent relay and SEL-487E are connected via the IEC 61850 based communication network.

SEL-487E transformer current differential relay carries the inrush current blocking signal. That signal is used to block the tripping of the overcurrent relay using IEC 61850 GOOSE message. The backup overcurrent is defined to receive the GOOSE message signal and take appropriate action.

Figure 7.44 shows the inrush current signals on the primary side of the three-phase power transformer simulated in RSCAD environment. This signal is sent to the physical transformer differential relay SEL-487E via RTDS and CMS156 amplifiers which amplify the simulated analogue signals into appropriate scale factors as shown in Figure 7.4.

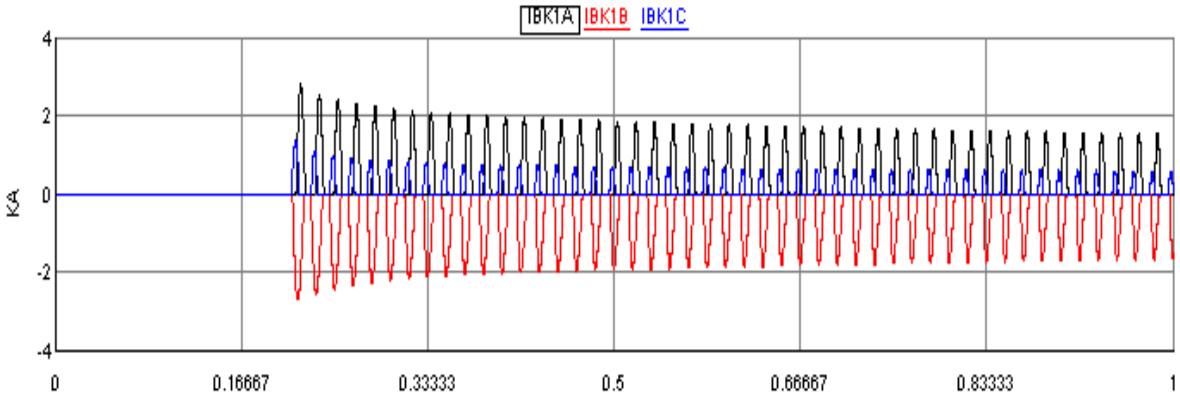


Figure 7.44: Inrush Conditions in RSCAD

Figure 7.45 shows the inrush current signals on the primary of the three-phase power transformer measured in SEL-487E IED. It is observed that the harmonic blocking elements 87AHB, 87BHB and 87CHB are asserting and de-asserting as shown in Figure 7.45. For this reason, a protection latch PLT32 was used to latch in the harmonic blocking signals as explained in the IEC 61850 GOOSE configuration setting in chapter six. The status value of the protection SELogic variable PVS01 is

transmitted as an IEC 61850 GOOSE reverse blocking signal as shown in Figure 4.45.

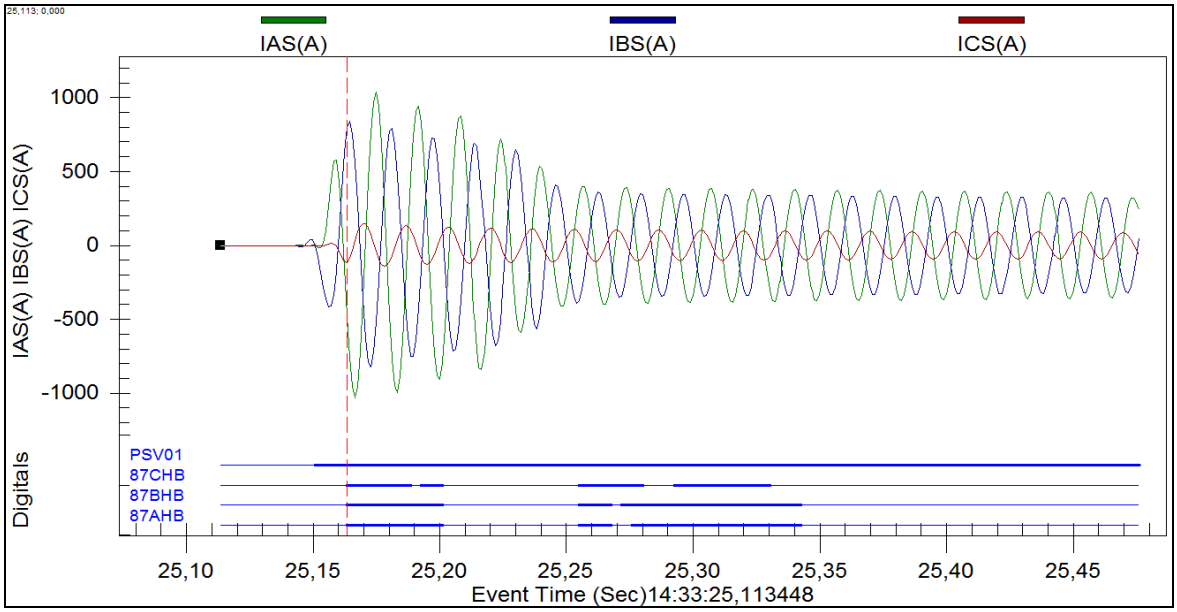


Figure 7.45: Measured inrush current signals in S winding of the SEL-487E

From Figure 7.46, it is observed that as soon as the transformer breaker is closed the IEC 61850 GOOSE blocking signal is published from SEL-487E and RSCAD software overcurrent relay receives this GOOSE blocking signal. While the counter reset signal (KTRST) changes from high to low input signal because of the inrush current signal. The initial trip signal before GOOSE (TRIP1) is monitored, and the trip signal (TRIP) is blocked during transformer magnetizing current as shown in Figure 7.46

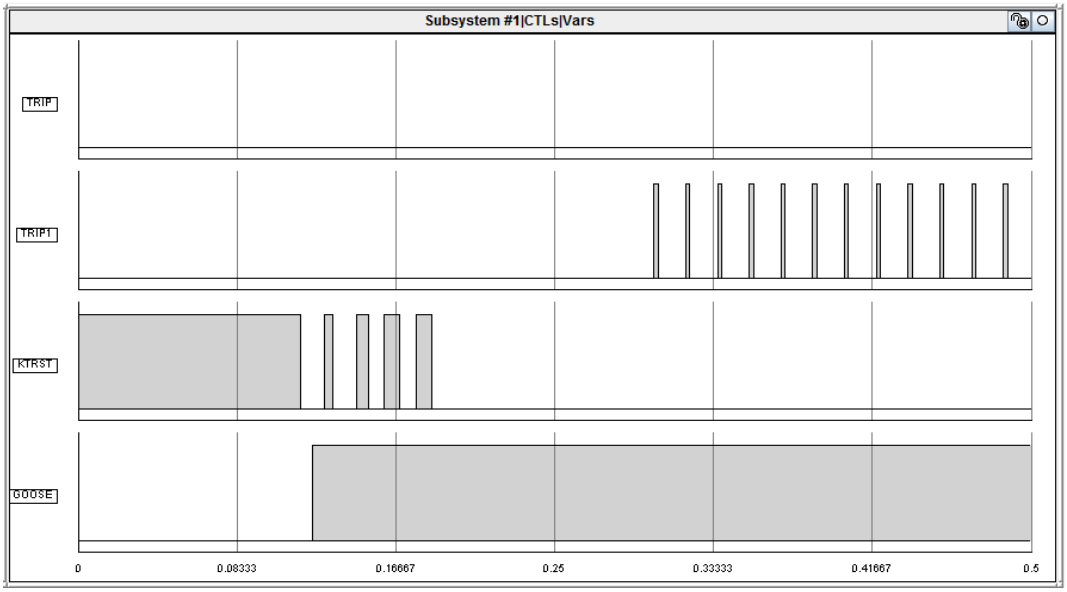


Figure 7.46: Blocking of the overcurrent relay trip signal using reverse harmonic scheme during transformer magnetizing inrush condition

7.10 Conclusion

This chapter presented HIL implementation and simulation results of the developed reverse harmonic blocking method which prevented the malfunction of the backup overcurrent relay of the power transformer during transformer magnetizing inrush current condition. The HIL implementation testbed setup is done using RTDS and IEC 61850 GOOSE data sharing between the IEDs. This chapter discussed the hardware-in-the-loop implementation and simulation results of the reverse harmonic blocking scheme for various internal, external events and inrush current conditions.

When the transformer generated inrush current, SEL-487E IED sends out harmonic blocking signals using IEC 61850 GOOSE signal to the backup overcurrent relay. The backup overcurrent relay restrains itself from malfunctioning because of the transformer inrush current by using the received IEC 61850 GOOSE blocking signal.

The next chapter presents the deliverables of the thesis and how and where the developed method can be applied. Also, recommendations for future work and publications associated with the thesis are given therein.

CHAPTER EIGHT
CONCLUSION

8.1 Introduction

This research project aimed to develop and implement a feasible and reliable IEC 61850 standard-based protection scheme for power transformers employing fundamental and harmonic currents. The IEEE 14-bus transmission system is considered as a use case study, and the investigation of the transformer current differential and backup overcurrent schemes were analysed.

Simulations of external, internal and inrush current conditions were conducted. Short circuit analysis was performed in DIgSILENT and RSCAD simulation environments.

The lab scale testing and implementation of the transformer protection scheme was performed. The development and implementation of a reliable power transformer protection scheme using harmonic blocking based on IEC 61850 GOOSE application to overcome the tripping of the backup overcurrent relays during magnetizing inrush current conditions were done. AcSELerator Quickset software was used to read, modify/create and write protection settings onto the SEL IEDs. AcSELerator Architect was used to configuring IEC 61850 GOOSE communication between IEDs and test Universe software which is a hardware interface was used to configure and control the Omicron CMC 356 test inject device. Hardware-in-the-loop implementation of the IEC 61850 standard-based harmonic blocking scheme was performed using RTDS, SEL 487E, SEL 751A protective IEDs and OMICRON test injection device.

The developed IEC 61850 GOOSE message based harmonic blocking scheme for the power transformer was implemented and tested in a hardware-in-the-loop simulation using external IEDs SEL 487E and RSCAD software overcurrent relay interfaced with Real-Time Digital Simulator (RTDS). The modelling and hardware-in-the-loop simulations were performed using RSCAD software. COMTRADE files for fault events within the RSCAD runtime environment and from the external IEDs were used to analyse the simulation results of the transformer protection scheme for internal, external and inrush current conditions.

This Chapter summarises the results obtained, the key findings and the thesis deliverables. The deliverables of the thesis are presented in section 8.2. Section 8.3 describes the possible academic, research and industry applications of the thesis deliverables. The future research work in the field of protection of distribution

transformers with integrated renewable energy sources is proposed in section 8.4. Section 8.5 gives reference of the paper sent for publication.

8.2 Deliverables

During inrush current conditions, the transformer backup overcurrent protection relay often operates due to a high level of transformer magnetizing inrush currents. Therefore, this project sends the IEC61850 GOOSE-based blocking signals from the differential SEL-487E IED to the backup overcurrent SEL-751A IED to prevent the tripping of the transformer operation during inrush conditions. The deliverables of the thesis are as follows:

8.2.1 Literature review

The literature review analysed the various techniques used for transformer protection. The algorithms for transformer protection schemes in terms of speed, stability, security and dependability have been reviewed. It also presented principles of power transformers, common transformer failures and the phenomenon of magnetization inrush and CT saturation.

Review investigation of the IEC 61850 which is a new communication standard that allows the development of a new range of protection and control applications that result in significant benefits compared to the conventional hardwired solutions. Hardware-in-the-loop simulation for the protective relaying system was reviewed using RTDS and relays. It was noted from the literature review that the application of protective (IED's) that comply with the IEC 61850 standard has proven to be the solution to a reliable protection of the power transformer.

8.2.2 Theory on power transformer protection schemes

This thesis provided the theory of different transformer protection schemes such as differential, negative-sequence differential and overcurrent. The mechanical protection of transformer covered the application of gas-accumulation and sudden-pressure relays to provide sensitive detection of internal faults to the transformer tank. Monitoring the transformer for thermal overload and excessive through-fault currents using pressure and thermal relays.

8.2.3 DIgSILENT implementation of the differential and overcurrent protection schemes for transformer

The performance of the transformer protection scheme was studied through the external and internal faults and inrush current simulations. The IEEE 14-Bus transmission system was considered as a case study. The transformer differential

protection scheme was implemented and simulated in the DIgSILENT environment, and load flow results were analysed. The performance of the transformer current differential scheme was studied for both external and internal events.

From the simulation results, it is evident that an overcurrent relay was going to mal-operate due to Transformer Magnetizing Inrush Currents (TMIC). It is also clear from the simulation results that the current differential relay (SEL-487E) did not trip due to TMIC. Therefore, it was necessary to develop a reverse harmonic blocking scheme using IEC 61850 GOOSE application.

8.2.4 Implementation of the differential and overcurrent protection schemes for power transformer using numerical relays

The engineering configuration setting of the transformer differential and its backup overcurrent protection functions were done using AcSELerator Quickset tool. The differential relay (SEL-487E) configuration settings was successfully tested for four different scenarios such as Differential configuration, Differential operating characteristic, Differential trip time characteristic and Differential harmonic restraint. The results of the above scenarios were analysed.

The performance of the transformer backup overcurrent relay (SE-751A) was tested for three different events such as LLL, LL and LG conditions. Finally, the numerical relay simulation results are compared with DIgSILENT ones.

8.2.5 Implementation of harmonic blocking scheme

In order to restrain the SEL 751A backup overcurrent relay from tripping during inrush current conditions, a reverse harmonic blocking scheme based on harmonic restraint currents was developed, implemented and tested in the lab scale environment. The scheme used the harmonic blocking element (87HB) of the transformer differential relay SEL-487E to send a blocking signal to the backup overcurrent relay SEL-751A to inhibit it from tripping during inrush current conditions.

The lab-scale transformer protection test bench setup was implemented at the CSAEMS lab within CPUT. Various faults pertaining to power transformers were simulated using the OMICRON test injection device. Transformer differential and backup overcurrent relays performance were monitored. The lab scale implementation of the IEC 61850 standard-based transformer protection scheme was presented. The scheme applied IEC 61850 GOOSE messaging signal to send a reverse harmonic blocking scheme from SEL 487E differential IED to the SEL 751A overcurrent IED during inrush current conditions.

8.2.6 Implementation of the hardware-in-the-loop simulation for harmonic blocking scheme

The performance of the transformer protection was analysed for external and internal faults, and inrush current conditions using the developed IEC 61850 GOOSE message based reverse harmonic blocking scheme.

IEEE 14-Bus system network was designed and modelled in RSCAD software environment. The hardware-in-the-loop test was implemented using RTDS, SEL-487E and the RSCAD software overcurrent relay in the closed loop simulation environment.

Two case studies were conducted in order to analyse the developed reverse harmonic blocking scheme. The first case study was simulated without the reverse harmonic scheme. In this case, backup overcurrent IED malfunctioned during inrush current condition. In the second case study, the developed reverse harmonic blocking signal sent from the differential relay SEL-487E to the backup RSCAD software overcurrent relay which inhibited from tripping during inrush current conditions.

8.3 Academic/Research and Industrial Application

The developed DIgSILENT and RSCAD models simulation results for power transformers can help both undergraduate and post-graduate students to understand the behaviour of a power transformer during normal operation and the faults conditions.

The thesis provides a standard benchmark for both academic and industry applications through the implementation of the transformer current differential protection scheme in DIgSILENT and RSCAD environments. It provides a lab scale test bench setup for implementation of the differential and overcurrent protection schemes for power transformers using numerical relays and hardware-in-the-loop simulation test.

Therefore, it is recommended to use the developed IEC 61850 standard-based reverse harmonic blocking method provides fast and reliable backup protection, which can be used by the power utilities to avoid mal-operation of the backup overcurrent relay of the power transformer during inrush current conditions.

8.4 Future work

This research project focused only on the transformer protection of the transmission system. It will be interesting for future work to investigate protection of small-sized distribution, pole mounted transformers and unit generator-transformer protection

schemes. Investigating the sympathetic inrush current conditions will be interesting. Their effects on the transformer due to renewable energy integration based on IEC 61850 standard could also be considered as future research scope.

This future research will consider power transformer protection using negative sequence currents to detect minor internal turn-to-turn faults in power transformers. The existing transformer models in DIgSILENT and RSCAD simulation environments do not support the internal turn-to-turn fault scenarios. Therefore, RSCAD's CBuilder software module provides a mechanism for RTDS users to develop their own component models. Using this facility, the users can design their own transformer model and to investigate the internal turn-to-turn fault conditions in power transformers.

8.5 Publication

1. B. Elenga Baningobera, S. Krishnamurthy and R. Tzoneva, 2018. IEC 61850 standard-based reverse harmonic blocking scheme for power transformers. Submitted to the International Journal of Electrical Power and Energy Systems, Elsevier, pp 1-10.
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APPENDICES

APPENDIX A: IEEE 14-BUS SYSTEM DATA

A.1 Introduction

The 14 Bus System consists of 14 buses (nodes), 5 generators, 11 loads, 16 lines, 5 transformers and one shunt capacitor bank. 3 of these 5 transformers are used to represent one single 3-winding transformer. Figure A1 shows the single line diagram of the IEEE 14-Bus system and it is a simplified model of the transmission system in the Midwest United States.

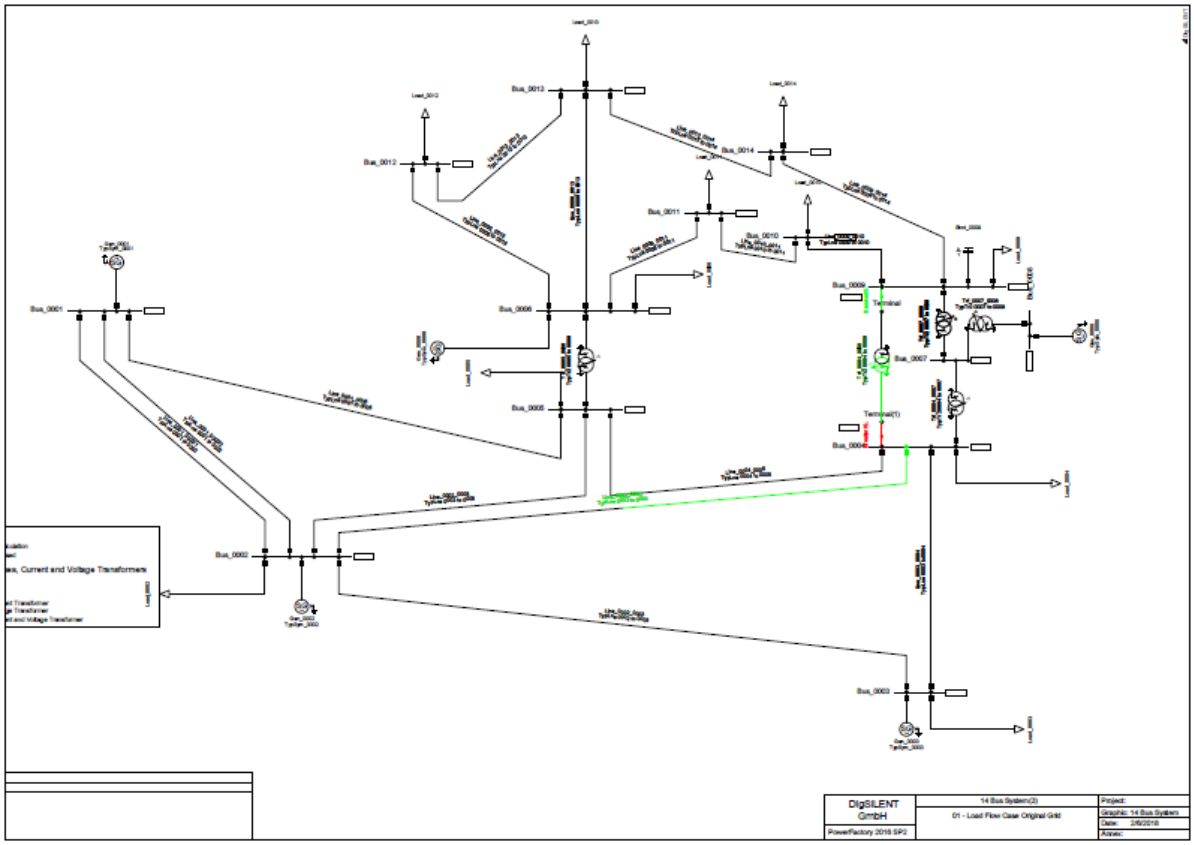

Figure A.1: Single line diagram of the IEEE 14 Bus system

A.2 IEEE 14 bus system

The typical nominal voltages of the IEEE 14 bus system are given as follows:

- Bus 1 - Bus 5: 132kV
- Bus 6, Bus 9 - Bus 14: 33kV
- Bus 7: 1kV
- Bus 8: 11kV

The nominal frequency of the 14 Bus System is 50 Hz. The network parameters are given in per unit values based on 100MVA. Loads and generation are given in MW and Mvars respectively.

Table A.1: Bus data of the IEEE 14 Bus system

Bus data							
Bus no.	**V(pu)**	**V_{rated} (kV)**	**δ (deg)**	**P_G (MW)**	**Q_G (MVar)**	**P_L (MW)**	**Q_L (MVar)**
1	1.06	132	0	232.9	-16.8	-	-
2	1.04	132	-5	40	43.1	21.7	12.7
3	1.01	132	-12.7	-	23.9	94.2	19
4	1.02	132	-10.4	-	-	47.8	-3.9
5	1.02	132	-8.8	-	-	7.6	1.6
6	1.07	33	-13.9	-	10.1	11.2	7.5
7	1.06	1	-13.6	-	-	-	-
8	1.09	11	-13.6	-	18.8	-	-
9	1.05	33	-15.3	-	-21.0	29.5	16.6
10	1.05	33	-15.3	-	-	9	5.8
11	1.05	33	-15.3	-	-	3.5	1.8
12	1.06	33	-14.6	-	-	6.1	1.6
13	1.06	33	-14.6	-	-	13.5	5.8
14	1.02	33	-17.1	-	-	14.9	5

The following subsections describe the network data used for symmetrical load flow calculation.

A.2.1 Generator data

Generator “Gen 0001” is the slack bus generator, therefore the load flow computation provides voltage magnitude and its angle as 1.060 p.u. and 0.0 degrees respectively. The other generators are configured to control the active power injection and voltage magnitudes at the connected buses. Therefore, the active power dispatch and controlled voltage magnitudes at the generator terminals are given in Table A.2 and A.3 respectively.

Table A.2: Generator dispatch of the IEEE 14 Bus system

Generator Name	Bus no	P in MW	Q in Mvar
Gen_0001	Bus_0001	-	-
Gen_0002	Bus_0002	40.0	-

Gen_0003	Bus_0003	0.0	-
Gen_0006	Bus_0006	0.0	-
Gen_0008	Bus_0008	0.0	-

The machines at buses 3, 6 and 8 are synchronous condenser.

Table A.3: Generator controller settings of the IEEE 14 Bus system

Generator and condenser				
Generator	**Bus Type**	**Voltage in p.u.**	**Minimum capability in MVA**	**Maximum capability in MVA**
Gen_0001	Slack	1.060	-	-
Gen_0002	PV	1.045	-40.0	50.0
Gen_0003	PV	1.010	0.0	40.0
Gen_0006	PV	1.070	-6.0	24.0
Gen_0008	PV	1.090	-6.0	24.0

A.2.2 Transformer data

Transformer data are given in Table A.4 in per unit (p.u.) and with base power Sb = 100MVA. The rated power of each transformer is assumed as Sr = 100MVA.

Transformer data of the IEEE 14-Bus system are given in Table A.4. In addition to that, tap changers are modelled to control the system voltage and its data is given in Table A.4.

Table A.4: Transformer data for the IEEE 14 Bus system

Transformers data							
Transformer name	**From Bus**	**To Bus**	**HV in kV**	**LV in kV**	**R in p.u.**	**X in p.u.**	**Transformer turns ratio**
Trf_0004_0007	4	7	132.0	1.0	0.0	0.20912	0.978
Trf_0004_0009	4	9	132.0	33.0	0.0	0.55618	0.969
Trf_0005_0006	5	6	132.0	33.0	0.0	0.25202	0.932
Trf_0007_0008	7	8	11.0	1.0	0.0	0.17615	0.000
Trf_0007_0009	7	9	33.0	1.0	0.0	0.11001	0.000

A.2.3 Transmission lines

The transmission line data are given in ohm units with base power Sb = 100MVA as given in Table A.5. There is no line length given for the IEEE 14-Bus system,

therefore the length of each line in the PowerFactory simulation has been assumed to 1km. Line data of the IEEE 14-bus system are given in Table A.5. The rated current of each line is not known and therefore it is assumed to be 1kA.

The line between bus 1 and bus 2 is a double circuit and therefore it has been modelled as two parallel lines in the PowerFactory simulation environment.

Table A.5: Line data of the IEEE 14 Bus system

Line Name	Impedance in polar form $Z\angle\delta$		Impedance in rectangular form $Z = R + jX$	
	Z1(Ω)	δ	R1(Ω)	X1(Ω)
L1-2-01	21.69739	71.86478	6.753542	20.61956
L1-2-02	21.69739	71.86478	6.753542	20.61956
L1-5	39.98651	76.38279	9.414187	38.8625
L2-5	31.88047	71.8651	9.922968	30.29685
L2-4	32.34747	71.75926	10.12509	30.722
L2-3	35.45266	76.64742	8.187537	34.49428
L3-4	32.00595	68.60462	11.67582	29.80027
L4-5	7.697139	72.40999	2.326104	7.337246
L6-12	3.090643	64.33693	1.33849	2.785771
L6-13	1.591062	63.07893	0.7203735	1.41864
L6-11	2.400311	64.4743	1.034332	2.166021
L12-13	3.244373	42.1376	2.405819	2.176693
L13-14	295.567	63.84204	130.2999	265.2957
L10.-11	2.274501	66.86842	0.8935243	2.091643
L9-10	0.9832489	69.37118	0.3464109	0.9202054
L9-14	3.253584	64.82103	1.384228	2.944439

A.2.4 Loads

Loads are not voltage-dependent, they are constant active and reactive power demand. It is important to note that this is achieved by disabling the load option “Consider Voltage Dependency of Loads” in the PowerFactory load flow computation setting. Load data (active power P and reactive power Q) are given in Table A.6.

Table A.6: Load demand for the IEEE 14 Bus system

Load demand			
Load name	**Bus no**	**P in MW**	**Q in Mvar**
Load_0002	Bus_0002	21.7	12.7
Load_0003	Bus_0003	94.2	19.0
Load_0004	Bus_0004	47.8	-3.9

Load_0005	Bus_0005	7.6	1.6
Load_0006	Bus_0006	11.2	7.5
Load_0009	Bus_0009	29.5	16.6
Load_0010	Bus_0010	9.0	5.8
Load_0011	Bus_0011	3.5	1.8
Load_0012	Bus_0012	6.1	1.6
Load_0013	Bus_0013	13.5	5.8
Load_0014	Bus_0014	14.9	5.0

A.2.5 Shunt capacitor data

Shunt capacitor data are given in per unit (p.u.). The 14 Bus System has one capacitor at bus 9, which has a susceptance (B) of 0.19p.u. with base power Sb = 100MVA. Shunt capacitor bank in PowerFactory uses either susceptance (B) in µS or rated reactive power (Q) in Mvar.

A.3 IEEE 14 Bus system in RSCAD software environment

A.3.1 Single line diagram of the IEEE 14 Bus system in RSCAD software environment

The network was designed and modelled in RSCAD using the IEEE 14-bus system data. The IEEE 14-Bus system consists of 14 buses (nodes), 5 generators, 11 loads, 16 lines, 5 transformers and one shunt. Figure A.2 shows the single line diagram of the IEEE 14 bus system in the RSCAD software environment.

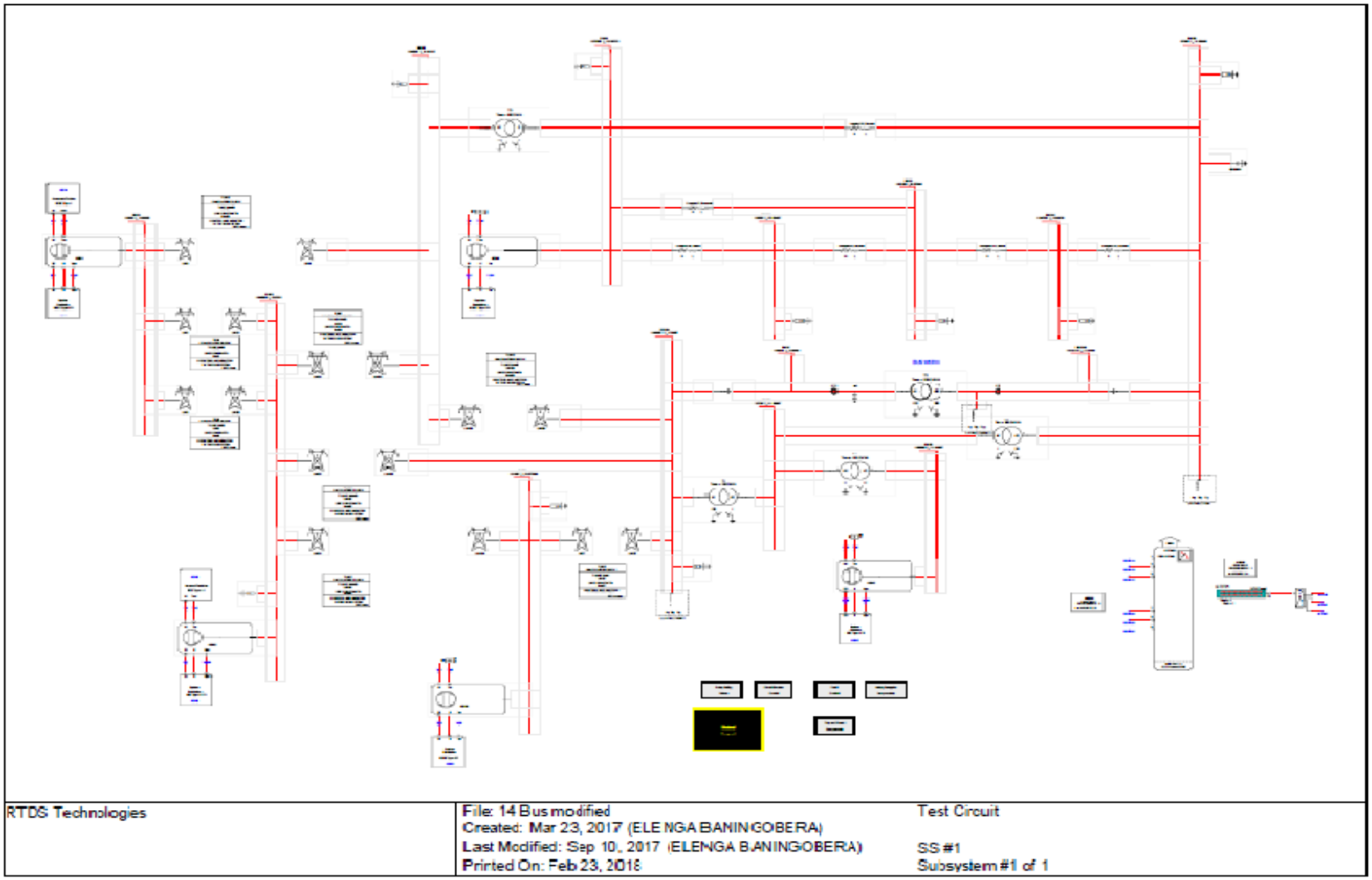

Figure A.2: Single line diagram of the IEEE 14 Bus system in RSCAD software environment

A.3.2 RSCAD map file for the IEEE 14 Bus system

This section provides RSCAD map file for the IEEE 14-bus system. It provides the map file information about the generators, transmission lines and control components (sliders, dial, pushbutton, switches etc.) and RPC-GPC cards and processors.

The RSCAD map file information for loads and shunt capacitors are not provided, because they were converted from dynamic to resistive and inductive components which means there is no processor attached to them. Transmission line model is not required for lines 9 to 16 are modelled as RL coupled branch which does not require processor to compute the line power flows.

The map file is a user readable file which provides information on processor allocation (ie: cross reference listing for component/processor match−up), input/output channel allocation, analogue output channel scaling and system initial conditions. The map file is particularly useful and important when physical connections are to be made between the RTDS and external equipment.
The compiler software essentially converts the graphical representation of a power system entered by the user from the RSCAD/Draft module into machine level code which is directly executed when the case is run. The .MAP file, generated by the RTDS compiler, provides the user with information as to which processors have been allocated to which part of the user's circuit. The map file contains the minimum time−step with which the power system model could be simulated in real−time.
This section provides the RSCAD map file information of subsystem 1 on RPC-GPC card 1, processor A.

```
>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>
   VSC component ordering
>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>

>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>

    RISC CONTROLS COMPONENTS (proc 0) --> RPC-GPC Card #1
    Processor A numberOfModels = 1

    Subsystem 1, Network Solution processor 1 Statistics:
    Number of nodes: 42
    Number of passed G values: 3
    Number of switched G overlays: 0
    Number of columns dynamically decomposed: 36

    component type=risc_net model=netsolCB name=1:1 DMStart =
    2DE8 DM Size=3520


    RISC CONTROLS COMPONENTS (proc 1) --> RPC-GPC Card #1
    Processor B Number Of Models = 10
```

A.3.2.1 RSCAD map file information of the generators

This section provides RSCAD map file information from generators 1 to 5 respectively.

A.3.2.1.1 RISC-based MAC_V3 Machine model named: GEN1 in subsystem: #1

This section provides RSCAD map file information for generator 1 (GEN1).

```
RPC-GPC Synchronous Machine model "GEN1"
Initial Mechanical Torque required: 0.519879 PU
Initial Field Voltage required:     1.381223 NORM

D axis circuit parameters
-------------------------
Stator Leakage Reactance:  Xs1= 0.100000 pu
Stator Resistance:  Rs1= 0.010000 pu
Field-Damper Mutual Leakage Reactance: X230= 0.000000 pu
Unsaturated magnetizing reactance: Xmd0= 1.900000 pu
Damper Leakage Reactance:  X3d= 0.161628 pu
Damper Resistance:  R3d= 0.015857 pu
Field Leakage Reactance:  X2d= 0.304262 pu
Field resistance:  R2d= 0.008292 pu

Q axis circuit parameters
-------------------------
Stator Leakage Reactance:  Xs1= 0.100000 pu
Stator Resistance:  Rs1= 0.010000 pu
Magnetizing Reactance:  Xmq= 1.900000 pu
2nd Damper Leakage Reactance:  X3q= 0.161628 pu
2nd Damper Resistance:  R3q= 0.015857 pu
1st damper Leakage Reactance:  X2q= 0.304262 pu
1st Damper resistance:  R2q= 0.008292 pu

component type=RISC_CMODEL model=MACV31_CB name=GEN1
DMStart = 4ED4 DMSize=3720
```

A.3.2.1.2 RISC-based MAC_V3 Machine model named: GEN2 in subsystem: #1

This section provides RSCAD map file information for generator 2 (GEN2).

```
RPC-GPC Synchronous Machine model "GEN2"
Initial Mechanical Torque required: 0.403802 PU
Initial Field Voltage required:     1.550199 NORM

D axis circuit parameters
-------------------------
Stator Leakage Reactance:  Xs1= 0.100000 pu
Stator Resistance:  Rs1= 0.001000 pu
Field-Damper Mutual Leakage Reactance: X230= 0.000000 pu
Unsaturated magnetizing reactance: Xmd0= 1.900000 pu
Damper Leakage Reactance:  X3d= 0.161628 pu
Damper Resistance:  R3d= 0.015857 pu
Field Leakage Reactance:  X2d= 0.304262 pu
Field resistance:  R2d= 0.008292 pu
```

```
Q axis circuit parameters
-------------------------
Stator Leakage Reactance:  Xs1= 0.100000 pu
Stator Resistance:  Rs1= 0.001000 pu
Magnetizing Reactance:  Xmq= 1.900000 pu
2nd Damper Leakage Reactance:  X3q= 0.161628 pu
2nd Damper Resistance:  R3q= 0.015857 pu
1st damper Leakage Reactance:  X2q= 0.304262 pu
1st Damper resistance:  R2q= 0.008292 pu

component type=RISC_CMODEL model=MACV31_CB name=GEN2
DMStart = 5D5C DMSize=3720
```

A.3.2.1.3 RISC-based MAC_V3 Machine model named: GEN3 in subsystem: #1

This section provides RSCAD map file information for generator 3 (GEN3).

```
RPC-GPC Synchronous Machine model "GEN3"
Initial Mechanical Torque required: 0.003415 PU
Initial Field Voltage required:     1.440516 NORM

D axis circuit parameters
-------------------------
Stator Leakage Reactance:  Xs1= 0.100000 pu
Stator Resistance:  Rs1= 0.001000 pu
Field-Damper Mutual Leakage Reactance: X230= 0.000000 pu
Unsaturated magnetizing reactance: Xmd0= 1.900000 pu
Damper Leakage Reactance:  X3d= 0.161628 pu
Damper Resistance:  R3d= 0.015857 pu
Field Leakage Reactance:  X2d= 0.304262 pu
Field resistance:  R2d= 0.008292 pu

Q axis circuit parameters
-------------------------
Stator Leakage Reactance:  Xs1= 0.100000 pu
Stator Resistance:  Rs1= 0.001000 pu
Magnetizing Reactance:  Xmq= 1.900000 pu
2nd Damper Leakage Reactance:  X3q= 0.161628 pu
2nd Damper Resistance:  R3q= 0.015857 pu
1st damper Leakage Reactance:  X2q= 0.304262 pu
1st Damper resistance:  R2q= 0.008292 pu

component type=RISC_CMODEL model=MACV31_CB name=GEN3
DMStart = 3AAC DMSize=3720
```

A.3.2.1.4 RISC-based MAC_V3 Machine model named: GEN4 in subsystem: #1

This section provides RSCAD map file information for generator 4 (GEN4).

```
RPC-GPC Synchronous Machine model "GEN4"
Initial Mechanical Torque required: 0.003893 PU
Initial Field Voltage required:     1.942955 NORM

D axis circuit parameters
-------------------------
Stator Leakage Reactance:  Xs1= 0.100000 pu
Stator Resistance:  Rs1= 0.001000 pu
```

```
Field-Damper Mutual Leakage Reactance: X230= 0.000000 pu
Unsaturated magnetizing reactance: Xmd0= 1.900000 pu
Damper Leakage Reactance:  X3d= 0.161628 pu
Damper Resistance:  R3d= 0.015857 pu
Field Leakage Reactance:  X2d= 0.304262 pu
Field resistance:  R2d= 0.008292 pu

Q axis circuit parameters
-------------------------
Stator Leakage Reactance:  Xs1= 0.100000 pu
Stator Resistance:  Rs1= 0.001000 pu
Magnetizing Reactance:  Xmq= 1.900000 pu
2nd Damper Leakage Reactance:  X3q= 0.161628 pu
2nd Damper Resistance:  R3q= 0.015857 pu
1st damper Leakage Reactance:  X2q= 0.304262 pu
1st Damper resistance:  R2q= 0.008292 pu

component type=RISC_CMODEL model=MACV31_CB name=GEN4
DMStart = 4934 DMSize=3720
```

A.3.2.1.5 RISC-based MAC_V3 Machine model named: GEN5 in subsystem: #1

This section provides RSCAD map file information for generator 5 (GEN5).

```
RPC-GPC Synchronous Machine model "GEN5"
Initial Mechanical Torque required: 0.003970 PU
Initial Field Voltage required:     1.607561 NORM

D axis circuit parameters
-------------------------
Stator Leakage Reactance:  Xs1= 0.100000 pu
Stator Resistance:  Rs1= 0.001000 pu
Field-Damper Mutual Leakage Reactance: X230= 0.000000 pu
Unsaturated magnetizing reactance: Xmd0= 1.900000 pu
Damper Leakage Reactance:  X3d= 0.161628 pu
Damper Resistance:  R3d= 0.015857 pu
Field Leakage Reactance:  X2d= 0.304262 pu
Field resistance:  R2d= 0.008292 pu

Q axis circuit parameters
-------------------------
Stator Leakage Reactance:  Xs1= 0.100000 pu
Stator Resistance:  Rs1= 0.001000 pu
Magnetizing Reactance:  Xmq= 1.900000 pu
2nd Damper Leakage Reactance:  X3q= 0.161628 pu
2nd Damper Resistance:  R3q= 0.015857 pu
1st damper Leakage Reactance:  X2q= 0.304262 pu
1st Damper resistance:  R2q= 0.008292 pu

component type=RISC_CMODEL model=MACV31_CB name=GEN5
DMStart = 3ED6 DMSize=3720
```

A.3.2.2 RSCAD map file information of the transmission lines

This section provides RSCAD map file information of the transmission lines.

```
T-Line "LINE1" parameters at 50.00 Hz
```

```
Travel time(usecs) mode0 = 146.20227 mode1 = 148.26431
mode2 = 148.26431
CIRCUIT #1
POSITIVE SEQUENCE
Line Impedance = 6.75 + j20.62 ohms
               = 21.70 /_71.86 degree
Shunt Capacitive Reactance = 6600.19 ohms
ZERO SEQUENCE
Line Impedance = 13.51 + j40.10 ohms
               = 42.31 /_71.38 degree
Shunt Capacitive Reactance = 13200.00 ohms

T-Line "LINE2" parameters at 50.00 Hz (Pi-Section Model)
Travel time(usecs) mode0 = 5.00294 mode1 = 148.26431
mode2 = 148.26431
CIRCUIT #1
POSITIVE SEQUENCE
Line Impedance = 6.75 + j20.62 ohms
               = 21.70 /_71.86 degree
Shunt Capacitive Reactance = 6600.19 ohms
ZERO SEQUENCE
Line Impedance = 0.36 + j1.23 ohms
               = 1.28 /_73.58 degree
Shunt Capacitive Reactance = 345139.96 ohms

T-Line "LINE3" parameters at 50.00 Hz (Pi-Section Model)
Travel time(usecs) mode0 = 5.00294 mode1 = 277.92817
mode2 = 277.92817
CIRCUIT #1
POSITIVE SEQUENCE
Line Impedance = 9.41 + j38.86 ohms
               = 39.99 /_76.38 degree
Shunt Capacitive Reactance = 3540.10 ohms
ZERO SEQUENCE
Line Impedance = 0.36 + j1.23 ohms
               = 1.28 /_73.58 degree
Shunt Capacitive Reactance = 345139.96 ohms

T-Line "LINE4" parameters at 50.00 Hz (Pi-Section Model)
Travel time(usecs) mode0 = 5.00294 mode1 = 246.32723
mode2 = 246.32723
CIRCUIT #1
POSITIVE SEQUENCE
Line Impedance = 8.19 + j34.49 ohms
               = 35.45 /_76.65 degree
Shunt Capacitive Reactance = 4000.12 ohms
ZERO SEQUENCE
Line Impedance = 0.36 + j1.23 ohms
               = 1.28 /_73.58 degree
Shunt Capacitive Reactance = 345139.96 ohms

T-Line "LINE5" parameters at 50.00 Hz (Pi-Section Model)
Travel time(usecs) mode0 = 5.00294 mode1 = 215.37767
mode2 = 215.37767
CIRCUIT #1
POSITIVE SEQUENCE
Line Impedance = 10.12 + j30.72 ohms
               = 32.35 /_71.76 degree
```

```
Shunt Capacitive Reactance = 4660.14 ohms
ZERO SEQUENCE
Line Impedance = 0.36 + j1.23 ohms
               = 1.28 /_73.58 degree
Shunt Capacitive Reactance = 345139.96 ohms

T-Line "LINE6" parameters at 50.00 Hz (Pi-Section Model)
Travel time(usecs) mode0 = 5.00294 mode1 = 206.48220
mode2 = 206.48220
CIRCUIT #1
POSITIVE SEQUENCE
Line Impedance = 9.92 + j30.30 ohms
               = 31.88 /_71.87 degree
Shunt Capacitive Reactance = 5000.15 ohms
ZERO SEQUENCE
Line Impedance = 0.36 + j1.23 ohms
               = 1.28 /_73.58 degree
Shunt Capacitive Reactance = 345139.96 ohms

T-Line "LINE7" parameters at 50.00 Hz (Pi-Section Model)
Travel time(usecs) mode0 = 5.00294 mode1 = 204.78304
mode2 = 204.78304
CIRCUIT #1
POSITIVE SEQUENCE
Line Impedance = 11.68 + j29.80 ohms
               = 32.01 /_68.60 degree
Shunt Capacitive Reactance = 5000.15 ohms
ZERO SEQUENCE
Line Impedance = 0.36 + j1.23 ohms
               = 1.28 /_73.58 degree
Shunt Capacitive Reactance = 345139.96 ohms

T-Line "LINE8" parameters at 50.00 Hz (Pi-Section Model)
Travel time(usecs) mode0 = 5.00294 mode1 = 61.61209 mode2
= 61.61209
CIRCUIT #1
POSITIVE SEQUENCE
Line Impedance = 2.33 + j7.34 ohms
               = 7.70 /_72.41 degree
Shunt Capacitive Reactance = 13600.40 ohms
ZERO SEQUENCE
Line Impedance = 0.36 + j1.23 ohms
               = 1.28 /_73.58 degree
Shunt Capacitive Reactance = 345139.96 ohms
```

NOTE: lines 9 to 16 are modelled as RL coupled branch lines which do not require RTDS processor to solve the transmission line power flow computation.

A.3.2.3 RISC CONTROLS COMPONENTS information on RPC-GPC Cards and Processors

This section provides RSCAD map file information for the control components mapped to the RPC-GPC cards 2 and 3 and its processors A and B respectively.

A.3.2.3.1 RISC CONTROLS COMPONENTS (proc 2) --> RPC-GPC Card #2 Processor A number Of Models = 50 (part 1)

This section provides RSCAD map file information for the control components such as dial, slider, pushbuttons, switches etc. which are used to create the overcurrent protection scheme in RSCAD software suite of RTDS.

```
component type=RISC_CMODEL model=dial_i DMStart = 2E96
DMSize=16
component type=RISC_CMODEL model=slider_f DMStart = 2EA6
DMSize=12
component type=RISC_CMODEL model=slider_f DMStart = 2EB2
DMSize=12
component type=RISC_CMODEL model=slider_f DMStart = 2EBE
DMSize=12
component type=RISC_CMODEL model=switch_i DMStart = 2ECA
DMSize=12
component type=RISC_CMODEL model=RCONST DMStart = 2ED6
DMSize=4
component type=RISC_CMODEL model=RCONST DMStart = 2EDA
DMSize=4
component type=RISC_CMODEL model=RCONST DMStart = 2EDE
DMSize=4
component type=RISC_CMODEL model=RCONST DMStart = 2EE2
DMSize=4
component type=RISC_CMODEL model=RCONST DMStart = 2EE6
DMSize=4
component type=RISC_CMODEL model=RCONST DMStart = 2EEA
DMSize=4
component type=RISC_CMODEL model=switch_i DMStart = 2EEE
DMSize=12
component type=RISC_CMODEL model=switch_i DMStart = 2EFA
DMSize=12
component type=RISC_CMODEL model=RCONST DMStart = 2F06
DMSize=4
component type=RISC_CMODEL model=RCONST DMStart = 2F0A
DMSize=4
component type=RISC_CMODEL model=slider_f DMStart = 2F0E
DMSize=12
component type=RISC_CMODEL model=RCONST DMStart = 2F1A
DMSize=4
component type=RISC_CMODEL model=RCONST DMStart = 2F1E
DMSize=4
component type=RISC_CMODEL model=pushb_i DMStart = 2F22
DMSize=8
component type=RISC_CMODEL model=slider_f DMStart = 2F2A
DMSize=12
component type=RISC_CMODEL model=slider_f DMStart = 2F36
DMSize=12
component type=RISC_CMODEL model=pushb_i DMStart = 2F42
DMSize=8
component type=RISC_CMODEL model=pushb_i DMStart = 2F4A
DMSize=8
component type=RISC_CMODEL model=pushb_i DMStart = 2F52
DMSize=8
```

```
component type=RISC_CMODEL model=pushb_i DMStart = 2F5A
DMSize=8
component type=RISC_CMODEL model=RCONST DMStart = 2F62
DMSize=4
component type=RISC_CMODEL model=switch_i DMStart = 2F66
DMSize=12
component type=RISC_CMODEL model=switch_i DMStart = 2F72
DMSize=12
component type=RISC_CMODEL model=switch_i DMStart = 2F7E
DMSize=12
component type=RISC_CMODEL model=slider_f DMStart = 2F8A
DMSize=12
component type=RISC_CMODEL model=slider_f DMStart = 2F96
DMSize=12
component type=RISC_CMODEL model=pushb_i DMStart = 2FA2
DMSize=8
component type=RISC_CMODEL model=dial_i DMStart = 2FAA
DMSize=16
component type=RISC_CMODEL model=ICONST DMStart = 2FBA
DMSize=4
component type=RISC_CMODEL model=ICONST DMStart = 2FBE
DMSize=4
component type=RISC_CMODEL model=ICONST DMStart = 2FC2
DMSize=4
component type=RISC_CMODEL model=pushb_i DMStart = 2FC6
DMSize=8
component type=RISC_CMODEL model=ICONST DMStart = 2FCE
DMSize=4
component type=RISC_CMODEL model=ICONST DMStart = 2FD2
DMSize=4
component type=RISC_CMODEL model=ICONST DMStart = 2FD6
DMSize=4
component type=RISC_CMODEL model=ICONST DMStart = 2FDA
DMSize=4
component type=RISC_CMODEL model=slider_f DMStart = 2FDE
DMSize=12
component type=RISC_CMODEL model=RCONST DMStart = 2FEA
DMSize=4
component type=RISC_CMODEL model=ICONST DMStart = 2FEE
DMSize=4
component type=RISC_CMODEL model=RCONST DMStart = 2FF2
DMSize=4
component type=RISC_CMODEL model=RCONST DMStart = 2FF6
DMSize=4
component type=RISC_CMODEL model=RCONST DMStart = 2FFA
DMSize=4
component type=RISC_CMODEL model=RCONST DMStart = 2FFE
DMSize=4
component type=RISC_CMODEL model=newGTFPI DMStart = 3002
DMSize=24
```

A.3.2.3.2 RISC CONTROLS COMPONENTS (proc 2) --> RPC-GPC Card #2 Processor A number Of Models = 50 (part 2)

```
component type=RISC_CMODEL model=word2bit_ DMStart = 301A
DMSize=50
component type=RISC_CMODEL model=Sampler_C DMStart = 304C
DMSize=42
```

```
component type=RISC_CMODEL model=Sampler_C DMStart = 3076
DMSize=42
component type=RISC_CMODEL model=Sampler_C DMStart = 30A0
DMSize=42
component type=RISC_CMODEL model=Sampler_C DMStart = 30CA
DMSize=42
component type=RISC_CMODEL model=compareX01 DMStart =
30F4 DMSize=20
component type=RISC_CMODEL model=mul_B DMStart = 3108
DMSize=6
component type=RISC_CMODEL model=monoX01 DMStart = 310E
DMSize=16
component type=RISC_CMODEL model=gain_cb DMStart = 311E
DMSize=4
component type=RISC_CMODEL model=sum3_A DMStart = 3122
DMSize=12
component type=RISC_CMODEL model=compareX03 DMStart =
312E DMSize=22
component type=RISC_CMODEL model=edgedet_cb DMStart =
3144 DMSize=6
component type=RISC_CMODEL model=zcdet_A DMStart = 314A
DMSize=14
component type=RISC_CMODEL model=zcdet_A DMStart = 3158
DMSize=14
component type=RISC_CMODEL model=gain_cb DMStart = 3166
DMSize=4
component type=RISC_CMODEL model=zcdet_A DMStart = 316A
DMSize=14
component type=RISC_CMODEL model=compareX04 DMStart =
3178 DMSize=22
component type=RISC_CMODEL model=inv_cb DMStart = 318E
DMSize=16
component type=RISC_CMODEL model=table_cb DMStart = 319E
DMSize=294
component type=RISC_CMODEL model=table_cb DMStart = 32C4
DMSize=294
component type=RISC_CMODEL model=table_cb DMStart = 33EA
DMSize=294
component type=RISC_CMODEL model=table_cb DMStart = 3510
DMSize=294
component type=RISC_CMODEL model=SYNBUFRC DMStart = 3636
DMSize=276
component type=RISC_CMODEL model=mul_B DMStart = 374A
DMSize=6
component type=RISC_CMODEL model=XPOWNC DMStart = 3750
DMSize=212
component type=RISC_CMODEL model=XPOWNC DMStart = 3824
DMSize=212
component type=RISC_CMODEL model=sum3_B DMStart = 38F8
DMSize=16
component type=RISC_CMODEL model=sum3_B DMStart = 3908
DMSize=16
component type=RISC_CMODEL model=sum3_B DMStart = 3918
DMSize=16
component type=RISC_CMODEL model=sum3_B DMStart = 3928
DMSize=16
component type=RISC_CMODEL model=SYNBUFRC DMStart = 3938
DMSize=276
```

```
component type=RISC_CMODEL model=mul_B DMStart = 3A4C
DMSize=6
component type=RISC_CMODEL model=XPOWNC DMStart = 3A52
DMSize=212
component type=RISC_CMODEL model=XPOWNC DMStart = 3B26
DMSize=212
component type=RISC_CMODEL model=sum3_B DMStart = 3BFA
DMSize=16
component type=RISC_CMODEL model=logicX01 DMStart = 3C0A
DMSize=12
component type=RISC_CMODEL model=logicX01 DMStart = 3C16
DMSize=12
component type=RISC_CMODEL model=mul_B DMStart = 3C22
DMSize=6
component type=RISC_CMODEL model=mul_B DMStart = 3C28
DMSize=6
component type=RISC_CMODEL model=mul_B DMStart = 3C2E
DMSize=6
component type=RISC_CMODEL model=mul_B DMStart = 3C34
DMSize=6
component type=RISC_CMODEL model=sh_B DMStart = 3C3A
DMSize=12
component type=RISC_CMODEL model=sigsw_cb DMStart = 3C46
DMSize=10
component type=RISC_CMODEL model=mul_B DMStart = 3C50
DMSize=6
component type=RISC_CMODEL model=sum3_B DMStart = 3C56
DMSize=16
component type=RISC_CMODEL model=mul_B DMStart = 3C66
DMSize=6
component type=RISC_CMODEL model=sum3_B DMStart = 3C6C
DMSize=16
component type=RISC_CMODEL model=monoX01 DMStart = 3C7C
DMSize=16
component type=RISC_CMODEL model=monoX01 DMStart = 3C8C
DMSize=16
component type=RISC_CMODEL model=sum3_B DMStart = 3C9C
DMSize=16
```

A.3.2.3.3 RISC CONTROLS COMPONENTS (proc 2) --> RPC-GPC Card #2 Processor A number Of Models = 50 (part 3)

```
component type=RISC_CMODEL model=sum3_B DMStart = 3CAC
DMSize=16
component type=RISC_CMODEL model=mul_B DMStart = 3CBC
DMSize=6
component type=RISC_CMODEL model=sqrt_cb DMStart = 3CC2
DMSize=10
component type=RISC_CMODEL model=mul_B DMStart = 3CCC
DMSize=6
component type=RISC_CMODEL model=edgedet_cb DMStart =
3CD2 DMSize=6
component type=RISC_CMODEL model=monoX02 DMStart = 3CD8
DMSize=16
component type=RISC_CMODEL model=mul_B DMStart = 3CE8
DMSize=6
component type=RISC_CMODEL model=gain_cb DMStart = 3CEE
DMSize=4
```

```
component type=RISC_CMODEL model=sqrt_cb DMStart = 3CF2
DMSize=10
component type=RISC_CMODEL model=compareX03 DMStart =
3CFC DMSize=22
component type=RISC_CMODEL model=not_cb DMStart = 3D12
DMSize=4
component type=RISC_CMODEL model=logicX01 DMStart = 3D16
DMSize=12
component type=RISC_CMODEL model=mul_A DMStart = 3D22
DMSize=6
component type=RISC_CMODEL model=mul_B DMStart = 3D28
DMSize=6
component type=RISC_CMODEL model=sum3_B DMStart = 3D2E
DMSize=16
component type=RISC_CMODEL model=mul_B DMStart = 3D3E
DMSize=6
component type=RISC_CMODEL model=XPOWNC DMStart = 3D44
DMSize=212
component type=RISC_CMODEL model=mul_B DMStart = 3E18
DMSize=6
component type=RISC_CMODEL model=gain_cb DMStart = 3E1E
DMSize=4
component type=RISC_CMODEL model=edgedet_cb DMStart =
3E22 DMSize=6
component type=RISC_CMODEL model=sigsw_cb DMStart = 3E28
DMSize=10
component type=RISC_CMODEL model=sigsw_cb DMStart = 3E32
DMSize=10
component type=RISC_CMODEL model=sigsw_cb DMStart = 3E3C
DMSize=10
component type=RISC_CMODEL model=mul_B DMStart = 3E46
DMSize=6
component type=RISC_CMODEL model=xdivy_cb DMStart = 3E4C
DMSize=10
component type=RISC_CMODEL model=sum3_B DMStart = 3E56
DMSize=16
component type=RISC_CMODEL model=xpowy DMStart = 3E66
DMSize=200
component type=RISC_CMODEL model=ARCTRIG DMStart = 3F2E
DMSize=190
component type=RISC_CMODEL model=mul_B DMStart = 3FEC
DMSize=6
component type=RISC_CMODEL model=xdivy_cb DMStart = 3FF2
DMSize=10
component type=RISC_CMODEL model=mul_B DMStart = 3FFC
DMSize=6
component type=RISC_CMODEL model=sum3_B DMStart = 4002
DMSize=16
component type=RISC_CMODEL model=sum3_B DMStart = 4012
DMSize=16
component type=RISC_CMODEL model=sine_cb DMStart = 4022
DMSize=162
component type=RISC_CMODEL model=gain_cb DMStart = 40C4
DMSize=4
component type=RISC_CMODEL model=sigsw_cb DMStart = 40C8
DMSize=10
component type=RISC_CMODEL model=sigsw_cb DMStart = 40D2
DMSize=10
```

```
component type=RISC_CMODEL model=xdivy_cb DMStart = 40DC
DMSize=10
component type=RISC_CMODEL model=minmax_cb DMStart = 40E6
DMSize=8
component type=RISC_CMODEL model=sum3_B DMStart = 40EE
DMSize=16
component type=RISC_CMODEL model=compareX03 DMStart =
40FE DMSize=22
component type=RISC_CMODEL model=mul_B DMStart = 4114
DMSize=6
component type=RISC_CMODEL model=mul_B DMStart = 411A
DMSize=6
component type=RISC_CMODEL model=ieee2int_ DMStart = 4120
DMSize=4
component type=RISC_CMODEL model=minmax_cb DMStart = 4124
DMSize=8
component type=RISC_CMODEL model=mul_B DMStart = 412C
DMSize=6
component type=RISC_CMODEL model=ieee2int_ DMStart = 4132
DMSize=4
component type=RISC_CMODEL model=IEEEG1x DMStart = 4136
DMSize=244
component type=RISC_CMODEL model=ST1x DMStart = 422A
DMSize=166
component type=RISC_CMODEL model=IEEEG1x DMStart = 42D0
DMSize=244
```

A.3.2.3.4 RISC CONTROLS COMPONENTS (proc 2) --> RPC-GPC Card #2 Processor A number Of Models = 40 (part 4)

```
component type=RISC_CMODEL model=ST1x DMStart = 43C4
DMSize=166
component type=RISC_CMODEL model=ST1x DMStart = 446A
DMSize=166
component type=RISC_CMODEL model=ST1x DMStart = 4510
DMSize=166
component type=RISC_CMODEL model=ST1x DMStart = 45B6
DMSize=166
component type=RISC_CMODEL model=logicX02 DMStart = 465C
DMSize=12
component type=RISC_CMODEL model=monoX02 DMStart = 4668
DMSize=16
component type=RISC_CMODEL model=edgedet_cb DMStart =
4678 DMSize=6
component type=RISC_CMODEL model=srff_A DMStart = 467E
DMSize=8
component type=RISC_CMODEL model=logicX01 DMStart = 4686
DMSize=12
component type=RISC_CMODEL model=logicX02 DMStart = 4692
DMSize=12
component type=RISC_CMODEL model=logicX01 DMStart = 469E
DMSize=12
component type=RISC_CMODEL model=srff_A DMStart = 46AA
DMSize=8
component type=RISC_CMODEL model=logicX02 DMStart = 46B2
DMSize=12
component type=RISC_CMODEL model=logicX01 DMStart = 46BE
DMSize=12
```

```
component type=RISC_CMODEL model=monoX01 DMStart = 46CA
DMSize=16
component type=RISC_CMODEL model=monoX02 DMStart = 46DA
DMSize=16
component type=RISC_CMODEL model=srff_A DMStart = 46EA
DMSize=8
component type=RISC_CMODEL model=logicX01 DMStart = 46F2
DMSize=12
component type=RISC_CMODEL model=edgedet_cb DMStart =
46FE DMSize=6
component type=RISC_CMODEL model=UPDOWNC DMStart = 4704
DMSize=18
component type=RISC_CMODEL model=compareX01 DMStart =
4716 DMSize=20
component type=RISC_CMODEL model=logicX01 DMStart = 472A
DMSize=12
component type=RISC_CMODEL model=edgedet_cb DMStart =
4736 DMSize=6
component type=RISC_CMODEL model=logicX02 DMStart = 473C
DMSize=12
component type=RISC_CMODEL model=sh_A DMStart = 4748
DMSize=12
component type=RISC_CMODEL model=sh_A DMStart = 4754
DMSize=12
component type=RISC_CMODEL model=sum3_A DMStart = 4760
DMSize=12
component type=RISC_CMODEL model=UPDOWNC DMStart = 476C
DMSize=18
component type=RISC_CMODEL model=compareX01 DMStart =
477E DMSize=20
component type=RISC_CMODEL model=logicX01 DMStart = 4792
DMSize=12
component type=RISC_CMODEL model=monoX01 DMStart = 479E
DMSize=16
component type=RISC_CMODEL model=logicX02 DMStart = 47AE
DMSize=12
component type=RISC_CMODEL model=not_cb DMStart = 47BA
DMSize=4
component type=RISC_CMODEL model=edgedet_cb DMStart =
47BE DMSize=6
component type=RISC_CMODEL model=edgedet_cb DMStart =
47C4 DMSize=6
component type=RISC_CMODEL model=logicX02 DMStart = 47CA
DMSize=12
component type=RISC_CMODEL model=edgedet_cb DMStart =
47D6 DMSize=6
component type=RISC_CMODEL model=TIMERC DMStart = 47DC
DMSize=26
component type=RISC_CMODEL model=TIMERC DMStart = 47F6
DMSize=26
component type=RISC_CMODEL model=sh_B DMStart = 4810
DMSize=12
component type=RISC_CMODEL model=sh_B DMStart = 481C
DMSize=12
```

A.3.2.3.5 RISC CONTROLS COMPONENTS (proc 3) --> RPC-GPC Card #2 Processor B Number Of Models = 1

This section provides RSCAD map file information of the control components included in the RPC-GPC card 2, processor B.

```
component type=RISC_CMODEL model=newGTAO DMStart = 2C18
DMSize=320
```

A.3.2.3.6 RISC CONTROLS COMPONENTS (proc 4) --> RPC-GPC Card #3 Processor A number Of Models = 10

This section provides RSCAD map file information of the control components included in the RPC-GPC card 3, processor B.

```
component type=RISC_CMODEL model=trf3p2wL name=T1 DMStart
= 2CB4 DMSize=900
component type=RISC_CMODEL model=trf3p2wL name=T4 DMStart
= 3038 DMSize=900
component type=RISC_CMODEL model=RLcoupled name=Line10
DMStart = 33BC DMSize=216
component type=RISC_CMODEL model=RLcoupled name=Line11
DMStart = 3494 DMSize=216
component type=RISC_CMODEL model=RLcoupled name=Line12
DMStart = 356C DMSize=216
component type=RISC_CMODEL model=tln_mdl_03 name=LINE7
DMStart = 3644 DMSize=1104
component type=RISC_CMODEL model=slider_f DMStart = 3A94
DMSize=12
component type=RISC_CMODEL model=slider_f DMStart = 3AA0
DMSize=12
```

A.3.2.3.7 RISC CONTROLS COMPONENTS (proc 5) --> RPC-GPC Card #3 Processor B Number Of Models = 10

This section provides RSCAD map file information of the control components included in the RPC-GPC card 3, processor B.

```
component type=RISC_CMODEL model=trf3p2wI name=T2 DMStart
= 2D4A DMSize=1248
component type=RISC_CMODEL model=trf3p2wL name=T5 DMStart
= 322A DMSize=900
component type=RISC_CMODEL model=CTpsys name=CT1 DMStart
= 35AE DMSize=520
component type=RISC_CMODEL model=CTpsys name=CT2 DMStart
= 37B6 DMSize=520
component type=RISC_CMODEL model=CVTpsys name=cvt DMStart
= 39BE DMSize=644
component type=RISC_CMODEL model=RLcoupled name=Line15
DMStart = 3C42 DMSize=216
component type=RISC_CMODEL model=RLcoupled name=Line16
DMStart = 3D1A DMSize=216
```

```
component type=RISC_CMODEL model=RLcoupled name=Line13
DMStart = 3DF2 DMSize=216
component type=RISC_CMODEL model=slider_f DMStart = 3ECA
DMSize=12
component type=RISC_CMODEL model=trf3p2wL name=T3 DMStart
= 2C98 DMSize=900
component type=RISC_CMODEL model=tln_mdl_02 name=LINE1
DMStart = 301C DMSize=1240
component type=RISC_CMODEL model=tln_mdl_03 name=LINE2
DMStart = 34F4 DMSize=1104
component type=RISC_CMODEL model=tln_mdl_03 name=LINE3
DMStart = 3944 DMSize=1104
component type=RISC_CMODEL model=tln_mdl_03 name=LINE6
DMStart = 3D94 DMSize=1104
component type=RISC_CMODEL model=tln_mdl_03 name=LINE5
DMStart = 41E4 DMSize=1104
component type=RISC_CMODEL model=tln_mdl_03 name=LINE4
DMStart = 4634 DMSize=1104
component  type=RISC_CMODEL  model=tln_mdl_03  name=LINE8
DMStart = 4A84 DMSize=1104
```

APPENDIX B: SEL-487E and SEL-751A IEDs engineering configuration settings

This section provides the engineering configuration settings for transformer differential relay function (SEL-487E) and overcurrent relay (SEL-751A).

B.1 SEL-487E transformer differential relay configuration settings from Quickset AcSELerator software

This section provides the SEL-487E transformer differential relay configuration settings which include the device information, communication port (port F and port 5), Global, Group 1, protection 1, output ports and report.

B.1.1 SEL-487E device information

This section provides the SEL-487E device information which includes FID and part number.

Device Information	
Part Number	0487E2X64811A0B3H623XXX
FID	SEL-487E-2-R110-V0-Z004002-D20100407
BFID	SLBT-4XX-R205-V0-Z001002-D20100128

B.1.2 Port F configuration setting of SEL-487E IED

This section provides the front panel port F configuration setting of SEL-487E which includes the protocol, data speed selection, parity bits and conditions to enable fast message, read data access for meters and targets.

Port F			
Setting	**Description**	**Range**	**Value**
PROTO	Protocol	Select: SEL, MBA, MBB, RTD, PMU	SEL
SPEED	Data Speed (bps)	Select: 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600	57600
DATABIT	Data Bits	Select: 7, 8	8
PARITY	Parity	Select: Odd, Even, None	N
STOPBIT	Stop Bits	Select: 1, 2	1
RTSCTS	Enable Hardware Handshaking	Select: Y, N	N
TIMEOUT	Port Time-Out (minutes)	Range = 1 to 60, OFF	5
AUTO	Send Auto-Messages to Port	Select: Y, N	Y

Port F			
Setting	**Description**	**Range**	**Value**
FASTOP	Enable Fast Operate Messages	Select: Y, N	N
TERTIM1	Initial Delay -Disconnect Sequence (seconds)	Range = 0 to 600	1
TERSTRN	Termination String -Disconnect Sequence (9 char max)	Range = ASCII string with a maximum length of 9.	\005
TERTIM2	Final Delay -Disconnect Sequence (seconds)	Range = 0 to 600	0
FMRENAB	Enable Fast Message Read Data Access	Select: Y, N	Y
FMRLCL	Enable Local Region for Fast Message Access	Select: Y, N	N
FMRMTR	Enable Meter Region for Fast Message Access	Select: Y, N	Y
FMRDMND	Enable Demand Region for Fast Message Access	Select: Y, N	Y
FMRTAR	Enable Target Region for Fast Message Access	Select: Y, N	Y
FMRHIS	Enable History Region for Fast Message Access	Select: Y, N	N
FMRBRKR	Enable Breaker Region for Fast Message Access	Select: Y, N	N
FMRSTAT	Enable Status Region for Fast Message Access	Select: Y, N	N
FMRANA	Enable Analog Region for Fast Message Access	Select: Y, N	Y
FMRSER	Enable State Region for Fast Message Access	Select: Y, N	N
FMRD1	Enable D1 Region for Fast Message Access	Select: Y, N	N

B.1.3 Port 5 configuration setting of SEL-487E IED

This section provides the Ethernet port 5 configuration setting of SEL-487E IED which includes IP address, subnetwork, router, telnet port and fast message read data access.

Port 5			
Setting	**Description**	**Range**	**Value**
MAXACC	Maximum Access Level	Select: 1, B, P, A, O, 2, C	C
TIMEOUT	Port Time-out (minutes)	Range = 1 to 60, OFF	5
AUTO	Send Auto Messages to Port	Select: Y, N	Y
FASTOP	Enable Fast Operate Messages	Select: Y, N	Y
TERTIM1	Initial Delay for Disconnect Sequence (seconds)	Range = 0 to 600	1
TERSTRN	Termination String for Disconnect Sequence	Range = ASCII string with a maximum length of 9.	\005
TERTIM2	Final Delay for Disconnect Sequence (seconds)	Range = 0 to 600	0
IPADDR	IP Address (www[h].xxx[h].yyy[h].zzz[h])	Range = ASCII string with a maximum length of 20.	192.168.1.219
SUBNETM	Subnet Mask (www[h].xxx[h].yyy[h].zzz[h])	Range = ASCII string with a maximum length of 20.	255.255.255.0
DEFRTR	Default Router (www[h].xxx[h].yyy[h].zzz[h])	Range = ASCII string with a maximum length of 20.	192.168.1.1
ETCPKA	Enable TCP Keep-Alive	Select: Y, N	Y
KAIDLE	TCP Keep-Alive Idle (seconds)	Range = 1 to 20	10
KAINTV	TCP Keep-Alive Interval (seconds)	Range = 1 to 20	1
KACNT	TCP Keep-Alive Count	Range = 1 to 20	6

Port 5			
Setting	**Description**	**Range**	**Value**
NETPORT	Primary Network Port (A=Port A, B=Port B, D=Disabled)	Select: A, B, D	A
FAILOVR	Enable Fail Over Mode	Select: Y, N	Y
FTIME	Network Port Fail Over Time (milliseconds)	Range = 5 to 65535	5
NETASPD	Network Speed, Port A (A=Auto, 10=10Mbs, 100=100Mbs)	Select: A, 10, 100	A
NETBSPD	Network Speed, Port B (A=Auto, 10=10Mbs, 100=100Mbs)	Select: A, 10, 100	A
T1CBAN	Telnet Connect Banner for Host	Range = ASCII string with a maximum length of 254.	trek-sas-s04-ied1 HOST TERMINAL SERVER:
T1INIT	Allow Telnet Sessions to be Initiated by Host	Select: Y, N	Y
T1RECV	Allow Telnet Sessions to be Received by Host	Select: Y, N	Y
T1PNUM	Telnet Port Number for Host (1-19,22-101,103-65534)	Range = 1 to 65534	23
T2CBAN	Telnet Connect Banner for Card	Range = ASCII string with a maximum length of 254.	trek-sas-s04-ied1 CARD TERMINAL SERVER:
T2RECV	Allow Telnet Sessions to be Received by Card	Select: Y, N	Y
T2PNUM	Telnet Port Number for Card (1-19,22-101,103-65534)	Range = 1 to 65534	1024
TIDLE	Telnet Idle Time-Out (minutes)	Range = 0 to 255	5
FTPSERV	Enable FTP Server	Select: Y, N	Y
FTPCBAN	FTP Connect Banner	Range = ASCII string with a maximum length of 254.	trek-sas-s04-ied1 FTP SERVER:
FTPIDLE	FTP Idle Time-Out (minutes)	Range = 5 to 255	5
FTPANMS	Enable Anonymous FTP Login	Select: Y, N	N
FTPAUSR	Associate Anonymous User Access Rights with User	Select: QUI, ACC, BAC, PAC, AAC, OAC, 2AC or Blank	2AC
FMRENAB	Enable Fast Message Read Data Access	Select: Y, N	Y
FMRLCL	Enable Local Region for Fast Message Access	Select: Y, N	N
FMRMTR	Enable Meter Region for Fast Message Access	Select: Y, N	Y
FMRDMND	Enable Demand Region for Fast Message Access	Select: Y, N	Y
FMRTAR	Enable Target Region for Fast Message Access	Select: Y, N	Y
FMRHIS	Enable History Region for Fast Message Access	Select: Y, N	N
FMRBRKR	Enable Breaker Region for Fast Message Access	Select: Y, N	N
FMRSTAT	Enable Status Region for Fast Message Access	Select: Y, N	N

Port 5			
Setting	**Description**	**Range**	**Value**
FMRANA	Enable Analog Region for Fast Message Access	Select: Y, N	Y
FMRSER	Enable State Region for Fast Message Access	Select: Y, N	N
FMRD1	Enable D1 Region for Fast Message Access	Select: Y, N	N
E61850	Enable IEC 61850 Protocol	Select: Y, N	Y
EGSE	Enable IEC 61850 GSE	Select: Y, N	Y
EPMIP	Enable Synchrophasors over Ethernet	Select: Y, N	Y
PMOTS1	PMU Output 1 Transport Scheme	Select: OFF, TCP, UDP_S, UDP_T, UDP_U	OFF
PMOTS2	PMU Output 2 Transport Scheme	Select: OFF, TCP, UDP_S, UDP_T, UDP_U	OFF

B.1.4 Global configuration setting of SEL-487E IED

This section provides the global configuration setting of SEL-487E which includes the conditions to enable the group settings (SS1 to SS5).

Global			
Setting	**Description**	**Range**	**Value**
SID	Station Identifier (40 characters)	Range = ASCII string with a maximum length of 40.	Station A
RID	Relay Identifier (40 characters)	Range = ASCII string with a maximum length of 40.	SEL-487E
NFREQ	Nominal System Frequency (Hz)	Select: 50, 60	50
PHROT	System Phase Rotation	Select: ABC, ACB	ABC
FRQST	Select the Primary Frequency Source Voltage Terminal	Select: OFF, V, Z	OFF
EICIS	Enable Independent Control Input Settings	Select: Y, N	N
IN1XXD	Debounce Time For Mainboard Contact Inputs (ms)	Range = 0,0 to 30,0	3,0
IN2XXD	Debounce Time For Interface Board # 1 Contact Inputs (ms)	Range = 0,0 to 30,0	2,0
SS1	Condition(s) to Enable Setting Group 1	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	PB3 AND NOT SG1
SS2	Condition(s) to Enable Setting Group 2	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	PB3 AND SG1
SS3	Condition(s) to Enable Setting Group 3	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NA
SS4	Condition(s) to Enable Setting Group 4	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NA
SS5	Condition(s) to Enable Setting Group 5	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NA
SS6	Condition(s) to Enable Setting Group 6	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NA
TGR	Group Change Delay (cyc)	Range = 1 to 54000	180
EPMU	Enable Synchronized Phasor	Select: Y, N	Y

Global			
Setting	**Description**	**Range**	**Value**
	Measurements		
MFRMT	Message Format	Select: C37.118, FM	C37.118
MRATE	Messages per Second	Select: 1, 2, 5, 10, 25, 50	10
PMAPP	Type of PMU Application	Select: F, N	N
PHCOMP	Frequency Based Phasor Compensation	Select: Y, N	Y
PMSTN	Station Name (16 characters)	Range = ASCII string with a maximum length of 16.	STATION A
PMID	PMU Hardware Identifier	Range = 1 to 65534	1
PHVOLT	Include Voltage Terminal	Select: V, Z, "V, Z"	V, Z
PHDATAV	Phasor Data Set, Voltages	Select: V1, PH, ALL, NA	ALL
PMFRQST	PMU Primary Frequency Source Terminal	Select: V, Z	V
PMFRQA	PMU Frequency Application	Select: F, S	S
VVCOMP	Voltage Phase Angle Compensation For Voltage Terminal V (deg)	Range = -179,99 to 180,00	0,00
VZCOMP	Voltage Phase Angle Compensation For Voltage Terminal Z (deg)	Range = -179,99 to 180,00	0,00
PHCURR	Include the following Current Terminals in Synchrophasor Packet	Combo of S,T,U,W,X,Y	S, T, U, W, X, Y
PHDATAI	Phasor Data Set, Currents	Select: I1, PH, ALL, NA	ALL
ISCOMP	Current Angle compensation For Current Terminal S (deg)	Range = -179,99 to 180,00	0,00
ITCOMP	Current Angle compensation For Current Terminal T (deg)	Range = -179,99 to 180,00	0,00
IUCOMP	Current Angle compensation For Current Terminal U (deg)	Range = -179,99 to 180,00	0,00
IWCOMP	Current Angle compensation For Current Terminal W (deg)	Range = -179,99 to 180,00	0,00
IXCOMP	Current Angle compensation For Current Terminal X (deg)	Range = -179,99 to 180,00	0,00
IYCOMP	Current Angle compensation For Current Terminal Y (deg)	Range = -179,99 to 180,00	0,00
PHNR	Phasor Numerical Representation	Select: I, F	F
PHFMT	Phasor Format	Select: R, P	P
FNR	Frequency Numerical Representation	Select: I, F	F
NUMANA	Number of Analog Quantities	Select: 0-16	16
NUMDSW	Number of 16-bit Digital Status Words	Select: 0-4	4
TREA1	Trigger Reason Bit 1	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NA
TREA2	Trigger Reason Bit 2	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NA
TREA3	Trigger Reason Bit 3	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NA
TREA4	Trigger Reason Bit 4	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NA
PMTRIG	Trigger	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NA
EPMDR	Enable PMU Data Recording	Select: Y, N	N
MRTCDLY	Maximum RTC Synchrophasor Packet	Range = 20 to 1000	500

Global			
Setting	**Description**	**Range**	**Value**
	Delay (ms)		
RTCRATE	Remote Messages per Second	Select: 1, 2, 5, 10, 25, 50	2
DATE_F	Date Format	Select: MDY, YMD, DMY	MDY
RST_DEM	Condition(s) for Resetting of Demand Metering Data	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NA
RST_PDM	Condition(s) for Resetting of Peak Demand Metering Data	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NA
RST_ENE	Condition(s) for Resetting of Energy Metering Data	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NA
RSTTRGT	Condition(s) for Resetting of Target LEDs	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NA
RSTDNPE	Condition(s) for Resetting of DNP Fault Summary Data	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	TRGTR

B.1.5 Group 1 configuration setting of SEL-487E IED

This section provides the group 1 configuration setting of SEL-487E which includes enables differential, harmonic, slope setting and time overcurrent protection functions.

Group 1			
Setting	**Description**	**Range**	**Value**
ECTTERM	Enable the Following Current Terminals	OFF or combo of S,T,U,W,X	S, T
EPTTERM	Enable the Following Voltage Terminals	OFF or combo of V,Z	OFF
E87	Include the Following Terminals in the Differential Element	OFF or combo of S,T	S, T
E50	Enable Definite Time Overcurrent Elements for the Following Terminals	OFF or combo of S,T	OFF
E46	Enable Current Unbalance Elements for the Following Terminals	OFF or combo of S,T	OFF
EBFL	Enable Breaker Failure Protection for the Following Terminals	OFF or combo of S,T	OFF
EREF	Enable the Following Number of Restricted Earth Fault Elements	Select: N, 1-3	N
E51	Enable the Following Number of Inverse Time Overcurrent Elements	Select: N, 1-10	N
EDEM	Select the Number of Demand Metering Elements Required	Select: N, 1-10	N
CTRS	Current Transformer Ratio For Terminal S	Range = 1 to 50000	400
CTCONS	Current Transformer Connection For Terminal S	Select: Y, D	Y
CTRT	Current Transformer Ratio For Terminal T	Range = 1 to 50000	1600
CTCONT	Current Transformer Connection For Terminal T	Select: Y, D	Y
E87TS	Include Terminal S in the Differential Element for the Following Conditions	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	1

Group 1			
Setting	**Description**	**Range**	**Value**
E87TT	Include Terminal T in the Differential Element for the Following Conditions	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	1
ICOM	Internal CT Connection Matrix Compensation Enabled	Select: Y, N	Y
TSCTC	Terminal S CT Connection Compensation	Range = 0 to 12	12
TTCTC	Terminal T CT Connection Compensation	Range = 0 to 12	12
MVA	Enter Transformer Maximum MVA Rating (MVA)	Range = 1 to 5000, OFF	100
VTERMS	Terminal S Nominal Line-to-Line Voltage (kV)	Range = 1,00 to 1000,00	132,00
VTERMT	Terminal T Nominal Line-to-Line Voltage (kV)	Range = 1,00 to 1000,00	33,00
TAPS	Terminal S Current Tap (Amps)	Range = 0,10 to 35,00	1,09
TAPT	Terminal T Current Tap (Amps)	Range = 0,10 to 35,00	1,09
TAPU	Terminal U Current Tap (Amps)	Range = 0,10 to 35,00	1,00
TAPW	Terminal W Current Tap (Amps)	Range = 0,10 to 35,00	1,00
TAPX	Terminal X Current Tap (Amps)	Range = 0,10 to 35,00	1,00
O87P	Differential Element Operating Current Pickup (p.u.)	Range = 0,10 to 4,00	0,50
SLP1	Slope 1 Setting (%)	Range = 5,00 to 100,00	35,00
SLP2	Slope 2 Setting (%)	Range = 5,00 to 100,00	75,00
U87P	Unrestrained Element Current Pickup (p.u.)	Range = 1,00 to 20,00	8,00
DIOPR	Incremental Operate Current Pickup (p.u.)	Range = 0,10 to 10,00	1,20
DIRTR	Incremental Restraint Current Pickup (p.u.)	Range = 0,10 to 10,00	1,20
E87HB	Enable Harmonic Blocking Differential Element	Select: Y, N	Y
E87HR	Enable Harmonic Restraint Differential Element	Select: Y, N	Y
PCT2	Second-Harmonic Percentage (%)	Range = 5 to 100, OFF	15
PCT4	Fourth-Harmonic Percentage (%)	Range = 5 to 100, OFF	35
PCT5	Fifth-Harmonic Percentage (%)	Range = 5 to 100, OFF	35
TH5P	Fifth-Harmonic Alarm Threshold (p.u.)	Range = 0,2 to 3,2, OFF	OFF
87QP	Negative Sequence Differential Element Operating Current Pickup (p.u.)	Range = 0,05 to 1,00	0,30
SLPQ1	Negative Sequence Differential Slope (%)	Range = 5 to 100	25
87QD	Negative Sequence Differential Element Delay	Range = 2,000 to	10,000

Group 1			
Setting	**Description**	**Range**	**Value**
	(Cycles)	9999,000	
TRXFMR	Trip Condition(s) for Transformer Terminals	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	87U OR REFF1 OR 87R
ULTXFMR	Unlatch Trip Condition(s) for Transformer Terminals	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	TRGTR
TRS	Trip Condition(s) for Terminal S	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	0
ULTRS	Unlatch Trip Condition(s) for Terminal S	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	TRGTR
TRT	Trip Condition(s) for Terminal T	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	0
ULTRT	Unlatch Trip Condition(s) for Terminal T	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	TRGTR
TDURD	Minimum Trip Duration (Cycles)	Range = 2,000 to 8000,000	5,000
ER	Condition(s) for Triggering Event Reports	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	50SQ1 OR 50TQ1 OR 87AHB OR 87BHB OR 87CHB
FAULT	Condition(s) for Asserting FAULT Bit	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	50SQ1 OR 50TQ1 OR 87AHB OR 87BHB OR 87CHB
CLS	Close Condition(s) for Terminal S	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	LB10
ULCLS	Unlatch Close Condition(s) for Terminal S	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	52CLS
CLT	Close Condition(s) for Terminal T	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	LB10
ULCLT	Unlatch Close Condition(s) for Terminal T	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	52CLT
CFD	Close Failure Delay (Cycles)	Range = 2,00 to 99999,00, OFF	4,00

B.1.6 Protection 1 configuration setting of SEL-487E IED

This section provides the protection 1 logic settings of SEL-487E.

Protection 1			
Setting	**Description**	**Range**	**Value**
PROTSEL1	Protection SELogic Row 001	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	PLT32S := 87CHB OR 87CHR OR 87AHB OR 87AHR OR 87BHB OR 87BHR OR 87XBK2
PROTSEL2	Protection SELogic Row 002	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	PLT32R := TRGTR
PROTSEL3	Protection SELogic Row 003	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	PSV01 := PLT32

B.1.7 Automation 1 configuration setting of SEL-487E IED

This section enables the automatic monitoring of the SEL-487E parameters such as real, reactive and apparent powers and power factor meters.

Automation 1			
Setting	**Description**	**Range**	**Value**
AUTO_1	Free Form Logic Row 001	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	AMV001 := 3PWFC # MV MW
AUTO_2	Free Form Logic Row 002	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	AMV002 := 3QWFC # MV MVAR
AUTO_3	Free Form Logic Row 003	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	AMV003 := 3SWFC # MV MVA
AUTO_4	Free Form Logic Row 004	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	AMV004 := 3DPFW # MV POWER FACTOR

B.1.8 Output configuration setting of SEL-487E IED

This section maps the relay word bits 87R, 87U and PSV01 to the output ports of SEL-487E.

Output			
Setting	**Description**	**Range**	**Value**
OUT101	Main Board Output OUT101	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	87R OR REFF1 OR 87U OR PSV01
OUT102	Main Board Output OUT102	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	PSV01
OUT103	Main Board Output OUT103	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	PCT02Q
OUT104	Main Board Output OUT104	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	PCT04Q
OUT108	Main Board Output OUT108	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NOT (SALARM OR HALARM)

B.1.9 Report configuration setting of SEL-487E IED

This section provides the Sequential Event Report (SER) configuration setting of SEL-487E to analyse the event reports.

Report			
Setting	**Description**	**Range**	**Value**
ESERDEL	Automatic Removal of Chattering SER Points	Select: Y, N	N
SITM1	SER Points and Aliases, Point 1	DeviceWord Element, AliasName, AssertedText, DeAssertedText	52CLS, 52CLS, Asserted, Deasserted, N
SRATE	Sample Rate of Event Report (kHz)	Select: 1, 2, 4, 8	1
LER	Length of Event Report (seconds)	Range = 0,25 to 5,00	1,00
PRE	Length of Pre-Fault (seconds)	Range = 0,05 to 0,95	0,05
ERAQ	ERAQ	Valid range = Word Elements	
ERDG	ERDG	Valid range = Word Elements	TRPXFMR, TRIPS, TRIPT, TRIPU, TRIPW, TRIPX, 87RA, 87RB, 87RC, 87Q, 87AHB, 87BHB, 87CHB, #, REFF1, REFF2, REFF3, REFR1, REFR2, REFR3, #, VPOLV, VPOLZ, LOPV, LOPZ, #, SF32P, SR32P, SF32Q, SR32Q, SF32G, SR32G, #, TF32P, TR32P, TF32Q, TR32Q, TF32G, TR32G, #, UF32P, UR32P, UF32Q, UR32Q, UF32G, UR32G, #, WF32P, WR32P, WF32Q, WR32Q, WF32G, WR32G, #, XF32P, XR32P, XF32Q, XR32Q, XF32G, XR32G, #, FBFS, FBFT, FBFU, FBFW, FBFX, #, IN101, IN102, IN103, IN104, IN105, IN106, IN107, #, OUT101, OUT102, OUT103, OUT104, OUT105, OUT106, OUT107, OUT108, #, RMB1A, RMB2A, RMB3A, RMB4A, RMB5A, RMB6A, RMB7A, RMB8A, #, TMB1A, TMB2A, TMB3A, TMB4A, TMB5A, TMB6A, TMB7A, TMB8A, #, ROKA, RBADA, CBADA, LBOKA, ANOKA, DOKA, #, PSV01, PSV02, PSV03, PSV04, PSV05, PSV06, PSV07, PSV08, #, PLT01, PLT02, PLT03, PLT04, PLT05, PLT06, PLT07, PLT08, #, PCT01Q, PCT02Q, PCT03Q, PCT04Q, PCT05Q, PCT06Q, PCT07Q, PCT08Q, #, CCS, CCT, CCU, CCW, CCX, OCS, OCT, OCU, OCW, OCX

B.2 SEL-751A transformer overcurrent relay configuration settings from Quickset AcSELerator software

This section provides the engineering configuration setting of SEL-751A overcurrent relay which includes the device information, communication ports (F and 1), Global, Group 1 protections functions, logic 1, output ports and report.

B.2.1 SEL-751A device information

This section provides the SEL-751A device information which includes the part number and FID.

Device Information	
Part Number	751A11A0X0X0X810230
FID	SEL-751A-R419-V0-Z011003-D20131025
BFID	BOOTLDR-R500-V0-Z000000-D20090925

B.2.2 Port F configuration setting of SEL-751A IED

This section provides the front panel (port F) communication configuration setting of SEL-751A IED which includes the protocol selection, data speed and parity bits.

Port F			
Setting	**Description**	**Range**	**Value**
PROTO	Protocol	Select: SEL, MOD, EVMSG, PMU	SEL
SPEED	Data Speed	Select: 300, 1200, 2400, 4800, 9600, 19200, 38400	9600
BITS	Data Bits	Select: 7, 8	8
PARITY	Parity	Select: O, E, N	N
STOP	Stop Bits	Select: 1, 2	1
RTSCTS	Hardware Handshaking	Select: Y, N	N
T_OUT	Port Time-Out	Range = 0 to 30	5
AUTO	Send Auto Messages to Port	Select: Y, N	N

B.2.3 Port 1 configuration setting of SEL-751A IED

This section provides the Ethernet port 1 communication settings of SEL-751A IED which includes the IP address, subnet mask, router, conditions to enable IEC 61850 protocol and GOOSE.

Port 1			
Setting	**Description**	**Range**	**Value**
IPADDR	Device IP Address	Range = ASCII string with a maximum length	192.168.1.2

Port 1			
Setting	**Description**	**Range**	**Value**
	[zzz.yyy.xxx.www]	of 15.	
SUBNETM	Subnet Mask	Range = ASCII string with a maximum length of 15.	255.255.255.0
DEFRTR	Default Router Gateway (15 characters)	Range = ASCII string with a maximum length of 15.	192.168.1.1
ETCPKA	Enable TCP Keep-Alive	Select: Y, N	Y
KAIDLE	TCP Keep-Alive Idle Range	Range = 1 to 20	10
KAINTV	TCP Keep-Alive Interval Range	Range = 1 to 20	1
KACNT	TCP Keep-Alive Count Range	Range = 1 to 20	6
TPORT	Telnet Port	Range = 1025 to 65534, 23	23
TIDLE	Telnet Port Time-Out	Range = 1 to 30	15
FTPUSER	File Transfer User Name	Range = ASCII string with a maximum length of 20.	FTPUSER
E61850	Enable IEC 61850 Protocol	Select: Y, N	Y
EGSE	Enable IEC 61850 GOOSE	Select: Y, N	Y
FASTOP	Fast Operate	Select: Y, N	N
NETASPD	Network Speed Port A	Select: AUTO, 10, 100	AUTO
EMOD	Enable Modbus Sessions	Select: 0-2	0
EDNP	Enable DNP Sessions	Select: 0-3	0
ESNTP	Enable SNTP Client	Select: OFF, UNICAST, MANYCAST, BROADCAST	OFF

B.2.4 Front panel configuration setting of SEL-751A IED

This section provides the trip and close logics of the overcurrent relay word bits mapped to the front panel LEDs and pushbuttons of SEL-751A.

Front Panel			
Setting	**Description**	**Range**	**Value**
EDP	Display Points Enable	Range = 1 to 32, N	4
ELB	Local Bits Enable	Range = 1 to 32, N	N
FP_TO	Front-Panel Timeout	Range = 1 to 30, OFF	15
FP_CONT	Front-Panel Contrast	Range = 1 to 8	3
FP_AUTO	Front-Panel Auto messages	Select: OVERRIDE, ROTATING	OVERRIDE
RSTLED	Reset Trip-Latched LEDs On Close	Select: Y, N	Y
T01LEDL	Trip Latch T_LED	Select: Y, N	Y
T01_LED		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	ORED50T

Front Panel			
Setting	**Description**	**Range**	**Value**
T02LEDL	Trip Latch T_LED	Select: Y, N	Y
T02_LED		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	51AT OR 51BT OR 51CT OR 51P1T OR 51P2T
T03LEDL	Trip Latch T_LED	Select: Y, N	Y
T03_LED		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	51N1T OR 51G1T OR 51N2T OR 51G2T
T04LEDL	Trip Latch T_LED	Select: Y, N	Y
T04_LED		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	51QT
T05LEDL	Trip Latch T_LED	Select: Y, N	Y
T05_LED		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	81D1T OR 81D2T OR 81D3T OR 81D4T
T06LEDL	Trip Latch T_LED	Select: Y, N	N
T06_LED		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	(BFT OR T06_LED) AND NOT TRGTR
PB1A_LED		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	79RS
PB2A_LED		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NOT LT02 OR SV02 AND NOT SV02T AND SV05T
PB3A_LED		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NOT LT02 AND NOT 52A
PB4A_LED		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	0
PB1B_LED		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	79LO
PB2B_LED		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	LT02 OR SV02 AND NOT SV02T AND SV05T
PB3B_LED		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	52A OR SV03 AND NOT SV03T AND SV05T
PB4B_LED		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NOT 52A OR SV04 AND NOT SV04T AND SV05T

B.2.5 Global configuration setting of SEL-751A IED

This section provides the configuration setting of SEL-751A overcurrent protection function which includes conditions to enable the group settings (SS1 to SS3)

Global			
Setting	**Description**	**Range**	**Value**
PHROT	Phase Rotation	Select: ABC, ACB	ABC
FNOM	Rated Frequency	Select: 50, 60	50
DATE_F	Date Format	Select: MDY, YMD, DMY	DMY
FAULT	Fault Condition	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	50G1P OR 50N1P OR 51P1P OR 51QP OR 50Q1P OR TRIP OR 51AP OR 51BP OR

Global			
Setting	**Description**	**Range**	**Value**
			51CP
EMP	Messenger Points Enable	Range = 1 to 32, N	N
TGR	Group Change Delay	Range = 0 to 400	3
SS1	Select Settings Group1	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	1
SS2	Select Settings Group2	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	0
SS3	Select Settings Group3	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	0
EPMU	Enable Synchronized Phasor Measurement	Select: Y, N	N
IRIGC	IRIG-B Control Bits Definition	Select: NONE, C37.118	NONE
UTC_OFF	Offset From UTC	Range = -24,00 to 24,00	0,00
DST_BEGM	Month To Begin DST	Range = 1 to 12, OFF	OFF
52ABF	52A Interlock in BF Logic	Select: Y, N	N
BFD	Breaker Failure Delay	Range = 0,00 to 2,00	0,50
BFI	Breaker Failure Initiate	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	R_TRIG TRIP
IN101D	IN101 Debounce	Range = 0 to 65000, AC	10
IN102D	IN102 Debounce	Range = 0 to 65000, AC	10
EBMON	Enable Breaker Monitor	Select: Y, N	Y
BKMON	Control Breaker Monitor	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	TRIP
COSP1	Close/Open Operations Set Point 1 -max	Range = 0 to 65000	10000
KASP1	kA(pri) Interrupted Set Point 1 -min	Range = 0,00 to 999,00	1,20
COSP2	Close/Open Operations Set Point 2 -mid	Range = 0 to 65000	150
KASP2	kA(pri) Interrupted Set Point 2 -mid	Range = 0,00 to 999,00	8,00
COSP3	Close/Open Operations Set Point 3 -min	Range = 0 to 65000	12
KASP3	kA(pri) Interrupted Set Point 3 -max	Range = 0,00 to 999,00	20,00
RSTTRGT	Reset Targets	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	0
RSTENRGY	Reset Energy	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	0
RSTMXMN	Reset Max/Min	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	0
DSABLSET	Disable Settings	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	0
BLKMBSET	Block Modbus Settings Edit	Select: NONE, R_S, ALL	NONE

B.2.6 Group 1 configuration setting of SEL-751A IED

This section provides the group 1 configuration setting of SEL-751A IED which enables the phase and neutral: definite and time overcurrent protection functions, CT ratios, trip logics and breaker status.

Group 1			
Setting	**Description**	**Range**	**Value**
RID	Relay Identifier	Range = ASCII string with a maximum length of 16.	SEL-751A
TID	Terminal Identifier	Range = ASCII string with a maximum length of 16.	FEEDER RELAY
CTR	Phase (IA,IB,IC) CT Ratio	Range = 1 to 5000	400
CTRN	Neutral (IN) CT Ratio	Range = 1 to 5000	400
50P1P	Maximum Phase Overcurrent Trip Pickup	Range = 0,10 to 20,00, OFF	OFF
50P2P	Maximum Phase Overcurrent Trip Pickup	Range = 0,10 to 20,00, OFF	2,00
50P2D	Maximum Phase Overcurrent Trip Delay	Range = 0,00 to 5,00	0,01
50P2TC	Maximum Phase Overcurrent Torque Control	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	1
50P3P	Maximum Phase Overcurrent Trip Pickup	Range = 0,10 to 20,00, OFF	OFF
50P4P	Maximum Phase Overcurrent Trip Pickup	Range = 0,10 to 20,00, OFF	OFF
50N1P	Neutral Overcurrent Trip Pickup	Range = 0,10 to 20,00, OFF	OFF
50N2P	Neutral Overcurrent Trip Pickup	Range = 0,10 to 20,00, OFF	0,30
50N2D	Neutral Overcurrent Trip Delay	Range = 0,00 to 5,00	0,05
50N2TC	Neutral Overcurrent Torque Control	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	1
51P1P	Time Overcurrent Trip Pickup	Range = 0,10 to 3,20, OFF	0,25
51P1C	TOC Curve Selection	Select: U1, U2, U3, U4, U5, C1, C2, C3, C4, C5	C1
51P1TD	TOC Time Dial	Range = 0,05 to 1,00	0,10
51P1RS	EM Reset Delay	Select: Y, N	N
51P1CT	Constant Time Adder	Range = 0,00 to 1,00	0,00
51P1MR	Minimum Response Time	Range = 0,00 to 1,00	0,00
51P1TC	Maximum Phase Time Overcurrent Torque Control	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NOT VB001
51P2P	Time Overcurrent Trip Pickup	Range = 0,10 to 3,20, OFF	OFF
51QP	Time Overcurrent Trip Pickup	Range = 0,10 to 3,20, OFF	OFF
51N1P	Time Overcurrent Trip Pickup	Range = 0,10 to 3,20, OFF	0,10
51N1C	TOC Curve Selection	Select: U1, U2, U3, U4, U5, C1, C2, C3, C4, C5	C1
51N1TD	TOC Time Dial	Range = 0,05 to 1,00	0,10
51N1RS	EM Reset Delay	Select: Y, N	N
51N1CT	Constant Time Adder	Range = 0,00 to 1,00	0,00
51N1MR	Minimum Response Time	Range = 0,00 to 1,00	0,00

Group 1			
Setting	**Description**	**Range**	**Value**
51N1TC	Neutral Time Overcurrent Torque Control	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	1
TDURD	Minimum Trip Time	Range = 0,0 to 400,0	0,5
CFD	Close Failure Time Delay	Range = 0,0 to 400,0, OFF	1,0
TR	Trip	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	(NOT VB001 OR IN101) AND (51AP OR 51BP OR 51CP OR 51P1T)
REMTRIP	Remote Trip	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	0
ULTRIP	Unlatch Trip	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NOT (51P1P OR 51G1P OR 51N1P OR 52A)
52A	Breaker Status	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	0
CL	Close Equation	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	SV03T AND LT02 OR CC
ULCL	Unlatch Close	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	0
E79	Enable Recloser	Select: OFF, 1-4	OFF

B.2.7 Logic 1 configuration setting of SEL-751A IED

This section provides the overcurrent relay word bits, trip and close logics mapped to the output ports of SEL-751A IED.

Logic 1			
Setting	**Description**	**Range**	**Value**
ELAT	SELogic Latches	Range = 1 to 32, N	4
ESV	SELogic Variables/Timers	Range = 1 to 32, N	5
ESC	SELogic Counters	Range = 1 to 32, N	N
EMV	SELogic Math Variables	Range = 1 to 32, N	N
SET01		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NA
RST01		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NA
SET02		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	R_TRIG SV02T AND NOT LT02
RST02		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	R_TRIG SV02T AND LT02
SET03		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	PB03_PUL AND LT02 AND NOT 52A
RST03		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	(PB03_PUL OR PB04_PUL OR SV03T) AND LT03
SET04		Valid range = The legal operators: AND OR	PB04_PUL AND 52A

Logic 1			
Setting	**Description**	**Range**	**Value**
		NOT R_TRIG F_TRIG	
RST04		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	(PB03_PUL OR PB04_PUL OR SV04T) AND LT04
SV01PU	SV_ Timer Pickup	Range = 0,00 to 3000,00	0,00
SV01DO	SV_ Timer Dropout	Range = 0,00 to 3000,00	0,00
SV01	SV_ Input	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	WDGTRIP OR BRGTRIP OR OTHTRIP OR AMBTRIP OR (27P1T OR 27P2T) AND NOT LOP
OUT101FS	OUT101 Fail-Safe	Select: Y, N	Y
OUT101		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	HALARM OR SALARM OR AFALARM
OUT102FS	OUT102 Fail-Safe	Select: Y, N	N
OUT102		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NOT (IN101 OR VB001) AND (51P1P OR 51N1P OR 51P2P OR 50P2P OR 50N2P)
OUT103FS	OUT103 Fail-Safe	Select: Y, N	N
OUT103		Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	NOT (IN101 OR VB001) AND (51P1T OR 51N1T OR 51P2T OR 50P2T OR 50N2T OR 50P1T OR 50G1T OR 50N1T)

B.2.8 Report configuration setting of SEL-751A IED

This section provides the overcurrent relay word bits mapped to the Sequential Event Report (SER) of SEL-751A IED.

Report			
Setting	**Description**	**Range**	**Value**
ER	Event Report Trigger	Valid range = The legal operators: AND OR NOT R_TRIG F_TRIG	R_TRIG 51P1P OR R_TRIG 51G1P OR R_TRIG 50P1P OR R_TRIG 50G1P OR R_TRIG 51N1P OR R_TRIG CF OR R_TRIG 50P1T OR R_TRIG 50N1T OR R_TRIG 50G1T OR R_TRIG 51P1T OR R_TRIG 51N1T OR R_TRIG 51G1T OR R_TRIG OUT101 OR R_TRIG IN101 OR VB001
LER	Length of Event Report	Select: 15, 64	15
PRE	Prefault Length	Range = 1 to 10	5
ESERDEL	Auto-Removal Enable	Select: Y, N	N
SER1	(24 Relay Word bits)	Range = Maximum of 24 Digital	IN101 IN102 51P1T 51G1T

Report			
Setting	**Description**	**Range**	**Value**
		Elements	50P1P 50N1T 51N1T PB01 PB02 PB03 PB04 OUT103 VB001
SER2	(24 Relay Word bits)	Range = Maximum of 24 Digital Elements	CLOSE 52A CC
SER3	(24 Relay Word bits)	Range = Maximum of 24 Digital Elements	81D1T 81D2T
SER4	(24 Relay Word bits)	Range = Maximum of 24 Digital Elements	SALARM
EALIAS	Enable ALIAS Settings	Range = 1 to 20, N	4
ALIAS1		Range = 2 Elements	PB01 FP_AUX1 PICKUP DROPOUT
ALIAS2		Range = 2 Elements	PB02 FP_LOCK PICKUP DROPOUT
ALIAS3		Range = 2 Elements	PB03 FP_CLOSE PICKUP DROPOUT
ALIAS4		Range = 2 Elements	PB04 FP_TRIP PICKUP DROPOUT
LDLIST	Load Profile List (17 Analog Quantities)	Range = Maximum of 17 Analog Elements	NA
LDAR	Load Profile Acquisition Rate	Select: 5, 10, 15, 30, 60	15