The design of a high efficiency Class-F power amplifier using GaN technology

by

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03/09/2020

Signed **Date**

Abstract

Power amplifiers are used in the final amplification stage of all wireless electronic communication systems to transmit information-bearing signals for a diverse range of applications. Power amplifiers are fundamentally power converters that convert direct current power to radio frequency power. The fraction of direct current power that is not converted to radio frequency power is dissipated as heat within the power amplifier. This phenomenon is described by the power conversion efficiency, and power added efficiency.

A CubeSat is a very small satellite, which must conform to specific standardised criteria that allocate constraints on factors such as the size, shape, and weight of the CubeSat and its components. CubeSats are battery operated and have limited available direct current power. This constraint warrants extensive investigation to minimize the direct current power consumption. One of the methods to achieve this minimising of direct current power consumption on the CubeSat is by maximizing the efficiency of one of the components, which is the power amplifier, that wastes much of this precious resource.

To achieve maximum power efficiency a review into power amplifier classes and their respective operations were performed. A power amplifier operated in Class-F mode is a suitable candidate to achieve high power efficiency and thus further investigation and analysis was conducted into this power amplifier class and mode of operation.

The design of a Class-F power amplifier is presented in this thesis. The power amplifier uses the GaN HEMT CGH40010F active device from Cree/Wolfspeed. A special output network, connected to the drain of the active device, was designed to achieve high efficiency. This Class-F power amplifier achieved a power efficiency, power added efficiency, and output power of 82.16 %, 72.4 %, and 40.06 dBm respectively, at a frequency of 2.1 GHz.

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Glossary

ACPR	-	Adjacent Channel Power Ratio
ADS	-	Advanced Design System
BJT	-	Bipolar Junction Transistor
CPUT	-	Cape Peninsula University of Technology
dB	-	Decibel
DC	-	Direct Current
EDA	-	Electronic Design Automation
ESR	-	Equivalent Series Resistance
EVM	-	Error Vector Magnitude
F'SATI	-	French South African Institute of Technology
GaAs	-	Gallium Arsenide
GaN	-	Gallium Nitride
Ge	-	Germanium
HEMT	-	High Electron Mobility Transistor
IMD	-	Intermodulation Distortion
InP	-	Indium Phosphide
IP_{1dB}	-	Input Power at 1 dB compression point
IP_{IMD}	-	Input Power of Intermodulation Distortion
IRL	-	Input Return Loss
LDMOS	-	Laterally Diffused Metal Oxide Semiconductor
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
OP_{1dB}	-	Output Power at 1 dB compression point
OP_{IMD}	-	Output Power of Intermodulation Distortion Product
ORL	-	Output Return Loss
PA	-	Power Amplifier

PAE	-	Power Added Efficiency
PCB	-	Printed Circuited Board
P_{DC}	-	DC Supply Power
P_{DD}	-	DC Supply Power to PA
PE	-	Power Efficiency
P_{RFin}	-	RF Input Power
P_{RFout}	-	RF Output Power
RF	-	Radio Frequency
Si	-	Silicon
SiC	-	Silicon Carbide
VHF	-	Very High Frequency

Chapter 1

Introduction

1.1 Motivation

A CubeSat is a tiny satellite, which must conform to specific standardised criteria that allocate constraints on factors such as the size, shape, and weight of the CubeSat. These standards are necessary to reduce the cost of mass-manufacturing components which also allows the use of standard off-the-shelf components (Chin *et al.*, 2017:4).

There are various sizes of standard CubeSat units, for example, 1U, 2U, and 3U sizes. The standard size of a 1U CubeSat is 10cm × 10cm × 11cm and that of a 3U CubeSat is 10cm × 10cm × 34cm (Chin *et al.*, 2017:4).

A CubeSat makes use of small solar panels to generate energy and batteries to store this energy. The limited size of the solar panels on the CubeSat places severe constraints on the power available from the batteries and hence the direct current (DC) power consumption of systems onboard the satellite.

The transmitter, within the communication system, requires a power amplifier (PA) which is located in the final stage of the transmitter, to amplify the information bearing signal to a suitable level for transmission. This amplification stage requires a significant amount of power to achieve the required signal power level. Fundamentally a PA is a DC to radio frequency (RF) power converter and this conversion causes a significant loss of DC power which is dissipated within the amplifier. Since the available DC power within a CubeSat is very limited, an obvious system requirement is to use this available DC power as efficiently as possible.

The Cape Peninsula University of Technology (CPUT) satellite program, in association with F'SATI (French South African Institute of Technology), successfully developed and launched the first African CubeSat, a 1U size CubeSat named ZACUBE-1, in November 2013. In December 2018, this satellite program launched another 3U CubeSat named ZACUBE-2.

The PA integrated into the 2W S-Band transmitter (STX) on ZACUBE-2 has a power conversion efficiency (*PE*) of 25%. That is, the PA has a DC to RF output power conversion ratio of 1:4. The remaining 75% of the DC power consumed is dissipated within the amplifier module as heat. The pass-over time of ZACUBE-2 is five minutes and occurs twice every twenty-four hours, where it must communicate with the ground station on earth. During this time a significant amount of data must be transmitted down to earth and places sudden power demands on the battery system within the CubeSat. It is thus crucial to minimise any power wastage, hence conserving this limited DC power resource.

The main aim of this research is to produce a highly efficient RF PA suitable for use in future CubeSats and which will optimise the DC to RF power conversion, and in doing so minimise the DC power consumption in the active device, control the harmonic content of the output signal, and maximise the amplification of the applied signal.

1.2 Objectives

The specific objectives of this project are:

Primary:

- To design, build, measure, and characterise the performance of a highly efficient class-F PA.

Secondary:

- To investigate and analyse RF PAs in general.
- To compare the performance parameters of the constructed PA circuit to similar class PAs.

1.3 Research Methodology

- Research the performance of the current PA on ZACUBE-2.
- Execute research to find possible solutions to maximise the efficiency of PAs.
- Research RF active device technologies that are suitable for satellite applications.
- Determine if the design techniques are attainable and feasible.
- Use Keysight's Advanced Design System (ADS) extensively in the design process.
- Use appropriate RF design techniques for the construction of the PA.
- Measure the performance parameters of the PA.
- Compare the measured performance parameters, the simulated parameters with the design specifications.

1.4 Delineation

In modern digital communications, the complexity of the modulated signal has been raised significantly to increase the rate of information transfer, that is, to increase the data rate thereof. Hence, modern digital information-bearing signals convey the data by simultaneously varying the amplitude, frequency, and/or phase of the carrier signal. This requires a PA, the operation of which must be highly linear to prevent distortion of the modulated signal. However, the efficiency of a PA is maximised when the active device is driven into saturation, that is, the amplifier is operated in its non-linear region.

The requirements for achieving maximum efficiency and optimum linearity in a PA are conflicting and thus a compromise is necessary to achieve maximum efficiency while still maintaining sufficient linearity. Typically, a modern PA will be driven at a certain back-off input power level thus maintaining sufficient linearity and acceptable efficiency. This will ensure minimal distortion of modern digitally modulated signals which must be amplified by a PA which minimises DC power wastage.

Based on the type and the relatively limited amount of data to be transferred from the CubeSat to the ground station, at this stage the plans for the modulation schemes in future CubeSats developed

in the CPUT satellite program are to use linear modulation techniques such as QPSK and 8-PSK. Hence, in this research, maximising the linearity of a PA is not the main design goal but rather is focused on maximising the efficiency of a PA which is achieved by driving the amplifier into saturation.

Chapter 2

History of the Transistor

2.1 Introduction

The invention of the triode valve by De Forest in 1906 resulted in an evolutionary step towards our modern way of living. The triode is a device where an electron stream is controlled in a vacuum by a voltage potential which is applied across a grid. This discovery laid the foundation for the variety of electron tubes (commonly known as vacuum tubes) and eventually to the transistor which is the most fundamental component in modern electronic systems (Guy *et al.*, 1958:131).

The electron tube ranges in a variety of sizes and was used as a fundamental component in oscillators, detectors, amplifiers, modulators, and rectifiers in applications that range from computers, radars, radios, automation systems, transmitters, and receivers, to list a few. The operation of electron tubes includes the injection of free electrons into an evacuated envelope. The free electrons are attracted to more positively charged electrodes in the tube and are then controlled by voltage potentials across a grid interposed between the free electrons and their destination (Guy *et al.*, 1958:131).

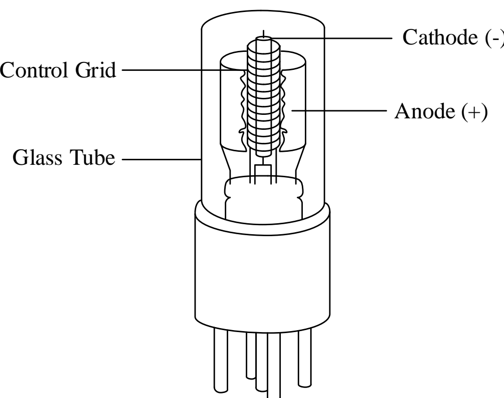


Figure 1: Vacuum Tube (Anthony, 2014)

The development of the transistor in 1947 at Bell Laboratories, replaced the electron tube in almost every application in the years to come due to its size, manufacturing cost, and efficient operation.

The transistor operates by controlling the electrical conduction properties of a material categorised as a semiconductor.

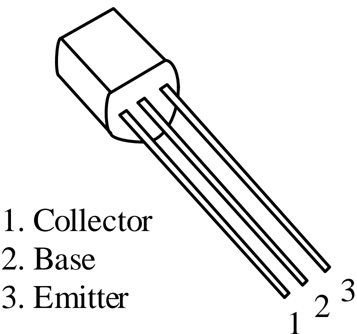


Figure 2: BJT Transistor

2.2 Materials

Metals such as gold, silver, copper, and iron are labelled as outstanding conductors of electricity due to their number of free electrons. Materials like glass, rubber, and plastics are labelled as insulators due to their lack of free available electrons. Materials, the conduction properties of which fall between these two categories, are called semiconductors and have relatively few free electrons. The properties of semiconductors which are exploited are their amount of free charged carriers. The amount of these charged carriers is proportional to the ambient temperature or the amount of impurities present and are controlled to obtain a component which will conduct current in one direction and limit the conduction of current in the opposite direction (Guy *et al.*, 1958:131).

When the conduction of current in a material is mainly by means of an electron then it is termed N-type (N: negative carrier) material, and when the conduction of current is mainly by means of holes then it is termed P-type (P: positive carrier) material (Guy *et al.*, 1958:161-162). Different methods can be employed to join N-type and P-type materials and result in a junction being formed between them, as depicted in Figure 3.

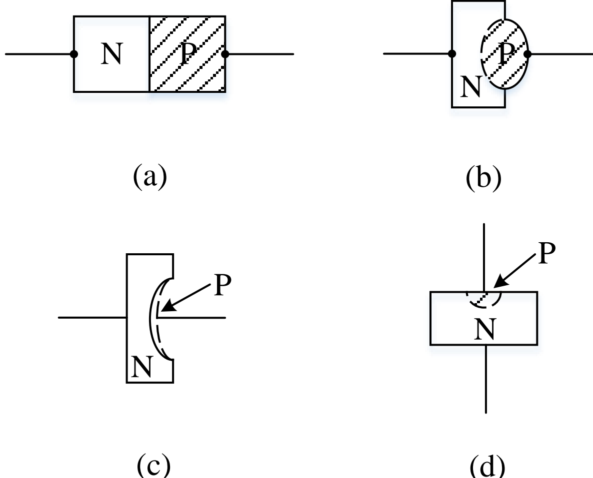


Figure 3: Different junction formations: (a) grown (b) diffused (c) plated (d) point contact (Guy *et al.*, 1958:163)

2.3 Semiconductor Diode

The development and fusion of N- and P-Type material gave birth to the semiconductor diode. Referring to Figure 4 (a), the P-N junction has no applied potential across its terminals resulting in the N-region which contains an excess of free electrons and the P-region containing an excess of holes. Typically these excess free electrons and holes are referred to as the majority carriers (Guy *et al.*, 1958:163).

Referring to Figure 4 (b), when a potential is applied across the diode as illustrated, the holes and electrons are forced to move to the junction by the electric field. Electrons will move across the junction to fill the holes and new holes are created by the positive electromotive force (emf) which then moves to the junction to support the loss of holes. The negative terminal which is connected to the N-type material provides electrons, and this process causes current to flow as long as the conditions are maintained and are commonly known as the forward bias state (Guy *et al.*, 1958:163).

With regards to Figure 4 (c), when a potential is applied across the diode and the N-region is positively charged the majority carriers of each region will move away from the junction and to their respective terminals. The junction is then lacking charge and is representing a high resistance and is thus restricting the flow of current. This particular state is known as a reverse bias state. A small leakage current could occur due to the conduction properties of the particular material and

should be insignificant enough to be considered negligible with regards to the desired operating current (Guy *et al.*, 1958:163).

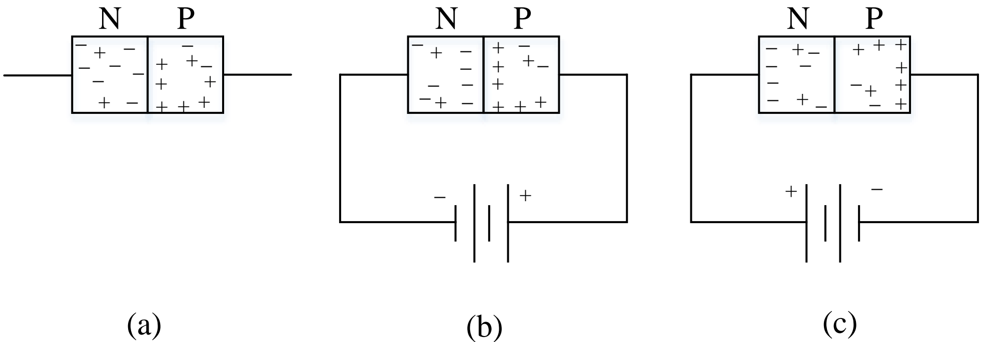


Figure 4: Semiconductor diode in (a) neutral, (b) forward bias and (c) reverse bias state (Guy *et al.*, 1958:164)

The current-voltage (I-V) characteristic curve of a silicon diode is shown in Figure 5.

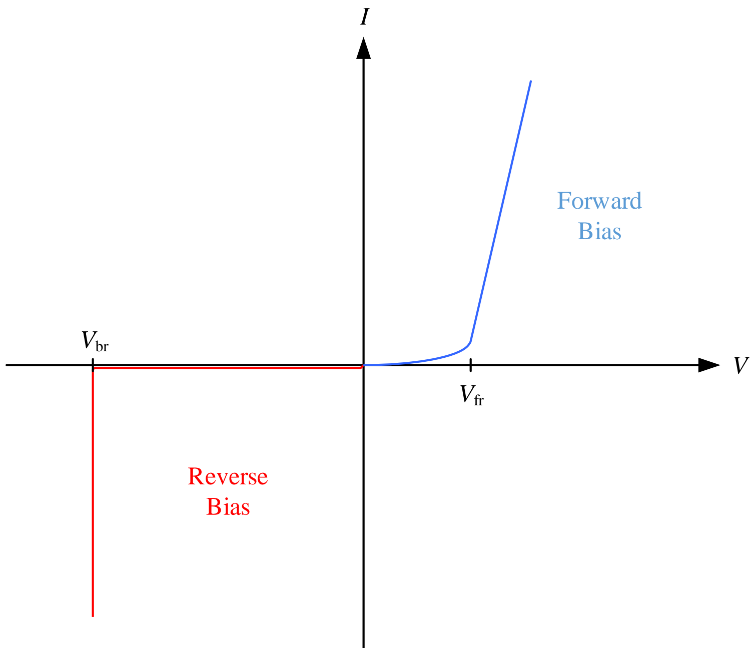


Figure 5: Ideal I-V characteristic curves of a diode (Floyd, 2012: 38)

At some negative value of voltage, referred to as the breakdown voltage (V_{br}), the diode will conduct a large amount of current as there is little resistance present.

2.4 Transistor

Joining two semiconductor diodes together results in a semiconductor triode which is commonly known as a transistor (Guy *et al.*, 1958:165).

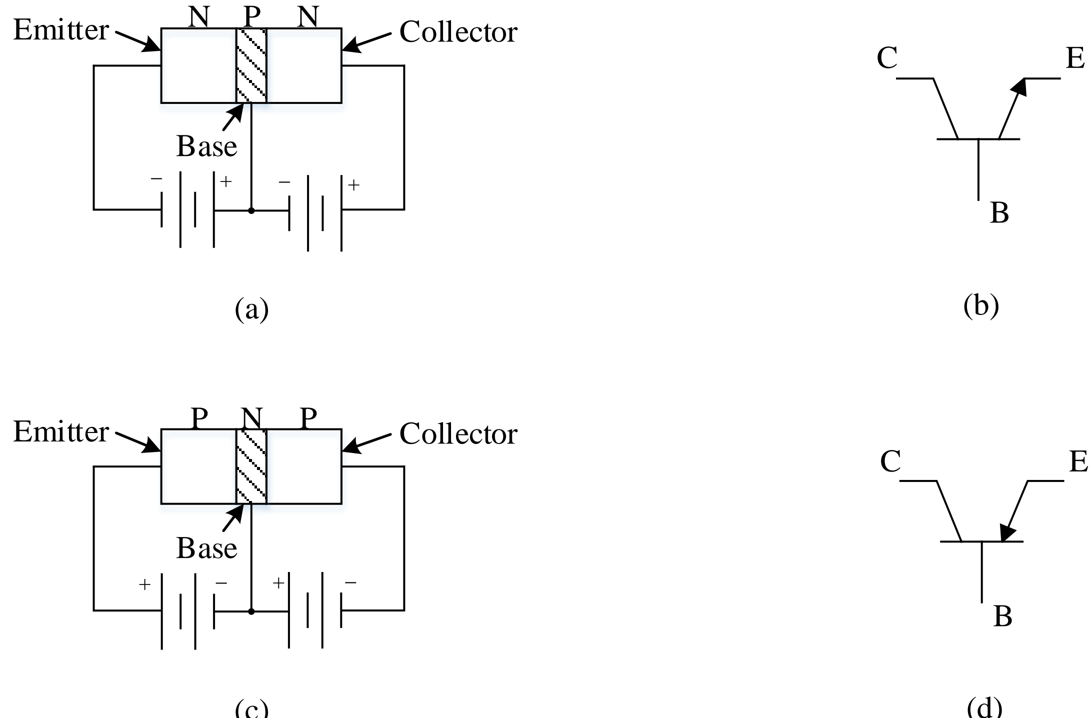


Figure 6: The Transistor: (a) NPN, (b) Bipolar Junction Transistor (BJT) NPN Symbol, (c) PNP, (d) Bipolar Junction Transistor (BJT) PNP Symbol, (Guy *et al.*, 1958:165)

Forward biasing the left-hand side PN junction of the transistor in Figure 6 (a) will initiate a low resistance path and electrons can easily flow into the P-region of the base. This will allow the N-region to emit electrons and is labelled the *emitter*. The PN junction on the right-hand side of the transistor in Figure 6 (a) is reversed-biased and will lure most of the electrons, injected into the base, towards the P-region on the right. The collection of electrons on the right-hand side P-region is labelled as the *collector*. If the base-emitter junction potential is modulated by a signal e_s , then the flow of electrons through this junction will vary according to the applied signal (Guy *et al.*, 1958:165-167).

2.5 RF Device Technology

Initially, the most utilised semiconductor technology for RF PAs was Silicon (Si) since it was the most affordable. Gallium Arsenide (GaAs), although more expensive, became favoured for its use in microwave applications due to improved performance (Cripps, 2006:14).

The production of modern commercial active devices predominantly incorporates the use of silicon (Si), gallium arsenide (GaAs), and associated semiconductor materials. A tremendous amount of research has since been conducted to develop high power density devices that use silicon carbide (SiC) and gallium nitride (GaN), commonly referred to as wide-bandgap materials (Colantonio, Giannini & Limiti, 2009:29).

Device performance is predominantly affected by the substrate properties as presented in Table 1. The energy needed to migrate an electron from valence- to conduction-band is referred to as the energy bandgap and according to Colantonio, Giannini & Limiti, (2009:30), this energy bandgap affects the power capabilities of the device and the maximum temperature permitted.

Property	Si	Ge	GaAs	GaN	4H-SiC	InP
Electron mobility $\left(cm^2{\cdot}V^{-1}{\cdot}s^{-1}\right)$	1500	3900	8500	1000	900	5400
Hole mobility $\left(cm^2{\cdot}V^{-1}{\cdot}s^{-1}\right)$	450	1900	400	350	120	200
Bandgap (eV)	1.12	0.66	1.42	3.2	3.23	1.35
Avalanche Field 10^5 V/cm	3.8	2.3	4.2	50	35	5.0
Saturated Drift velocity $\left(10^7\ cm/s\right)$	0.7	0.6	2.0	1.8	0.8	2.0
Saturation field $\left(10^3\ V/cm\right)$	8		3	15	25	25
Thermal Conductivity at $25°C\ (W/cm{\cdot}°C)$	1.4	0.6	0.45	1.7	4.9	0.68
Dielectric constant	11.9		12.9	14	10	8
Substrate resistance $(\Omega\ cm)$			>1000	>1000	1-20	>1000

Transistors			MESFET			MESFET
			HEMT	MESFET	MESFET	HEMT
			HBT	HEMT	HEMT	HBT
			P-HEMT			P-HEMT

Table 1: Properties of Semiconductors (Colantonio, Giannini & Limiti, 2009:30)

Devices, such as GaN and SiC, which exhibit wide bandgaps, operate at higher temperatures which allow for the manufacture of physically smaller devices with higher power density properties. These devices also allow, before the occurrence of breakdown, the sustainability of a larger internal electric field (Colantonio, Giannini & Limiti, 2009:30).

2.6 Conclusion

The invention of the triode valve by De Forest paved the way for the evolutionary step towards the discovery of the semiconductor diode and eventually the semiconductor triode which is commonly known as a transistor.

The transistor became the most fundamental component in modern electronic systems and has been improved continuously as research conducted in the field provided newly enhanced capabilities.

The development of high power density devices that use silicon carbide (SiC) and gallium nitride (GaN), commonly referred to as wide-bandgap materials, has paved the way to yet another evolutionary step in modern electronics.

Chapter 3

Theory of Power Amplifiers

3.1 The RF Power Amplifier

The key function of a PA, which operates in the RF band, is to increase the amplitude of the output signal to an appropriate level at the required frequency of operation. The ability of the PA to transform DC energy into RF energy is defined, for a particular PA, by the power efficiency (*PE*) and the power added efficiency (*PAE*) (Colantonio, Giannini & Limiti, 2009:5).

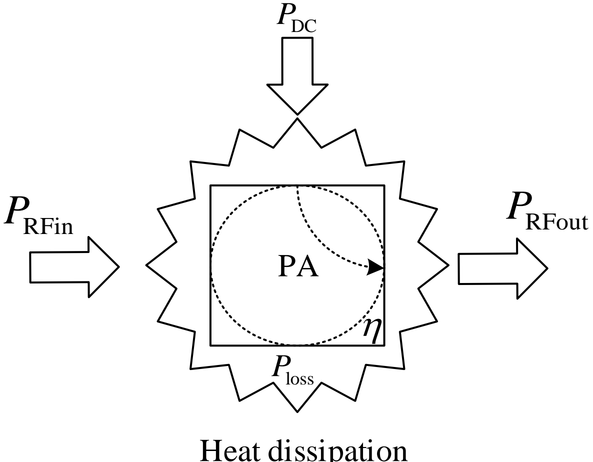


Figure 7: Power Conversion and Loss in a PA (Adapted from Colantonio, Giannini & Limiti, 2009:4)

The portion of DC power (P_{DC}) not transformed into RF output power (P_{RFout}) is thermally dissipated in the active device, resulting in a reduction in RF output power and is illustrated in Figure 7 (Prodanov & Banu, 2007:352).

The design of PAs generally involves a trade-off between numerous conflicting requirements which typically include efficiency vs linearity or increased RF output power level vs minimal distortion (Colantonio, Giannini & Limiti, 2009:1).

The fundamental block diagram of an RF PA consists of an active device (FET or BJT), output network, input network, RF chokes, and coupling capacitors. The active device operation can be either that of a switch or a dependant current source (Kazimierczuk, 2008:1).

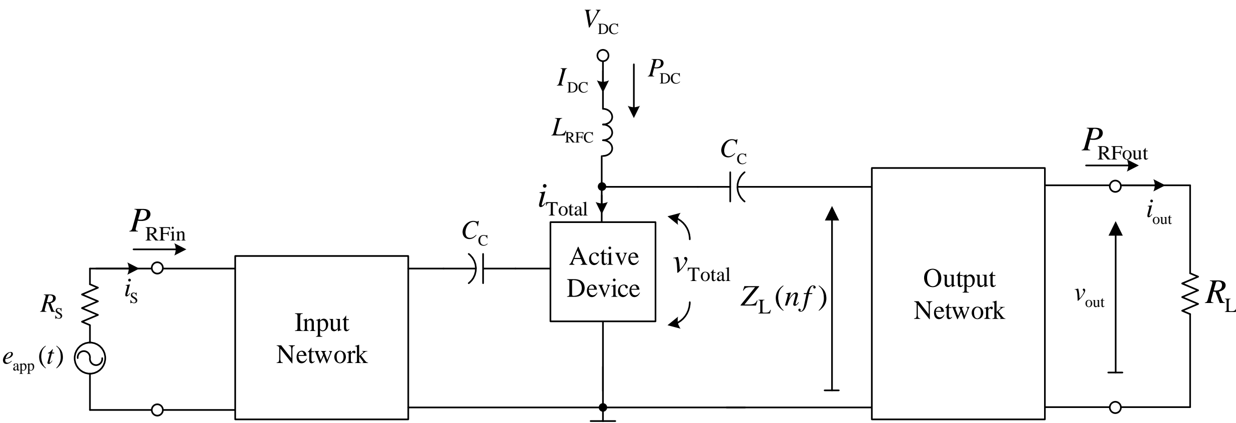


Figure 8: RF PA Block Diagram (Adapted from Kazimierczuk, 2008:2)

3.2 Performance Parameters of a PA

3.2.1 RF Output Power P_{RFout}

The power delivered to the load of the PA, denoted P_{RFout} , is the power developed in this load at the fundamental frequency of operation (Colantonio, Giannini and Limiti, 2009:2) and is expressed as:

$$P_{RFout}(f_0) = \frac{1}{2}\mathrm{Re}\{V_{out}I_{out}^{*}\} \tag{3.1}$$

Expressing the output power level in logarithmic units and referencing it to 1 mW results in:

$$P_{RFout}(\mathrm{dBm}) = 10\log\left(\frac{P_{RFout}}{10^{-3}}\right) = 30 + 10\log\left(P_{RFout}\,\mathrm{mW}\right) \qquad \mathrm{dBm} \tag{3.2}$$

3.2.2 RF Input Power P_{RFin}

The RF input power refers to the power level developed across the input port of the PA at the fundamental frequency (Colantonio, Giannini and Limiti, 2009:2) and is expressed as:

$$P_{\mathrm{RFin}}(f_0) = \frac{1}{2}\mathrm{Re}\{V_{\mathrm{in}} I_{\mathrm{in}}^{*}\} \qquad \mathrm{W} \tag{3.3}$$

Expressing the input power level in logarithmic units and referencing it to 1 mW results in:

$$P_{\mathrm{RFin}}(\mathrm{dBm}) = 10\log\left(\frac{P_{\mathrm{RFin}}}{10^{-3}}\right) = 30 + 10\log\left(P_{\mathrm{RFin}}\ \mathrm{mW}\right) \tag{3.4}$$

3.2.3 Linear Power Gain G_L of PA

The power gain is a comparison of RF output power to RF input power (Colantonio, Giannini and Limiti, 2009:2), as given by:

$$G(f_0) = \frac{P_{\mathrm{RFout}}(f_0)}{P_{\mathrm{RFin}}(f_0)} \tag{3.5}$$

For low-level input signals as shown in Figure 9, the PA behaves in a linear manner and the linear gain is defined as:

$$G_{\mathrm{L}}(f_0) = \lim_{P_{\mathrm{RFin}} \to 0}\left[G(f_0)\right] \tag{3.6}$$

3.2.4 Non-Linear Power Gain of PA

Referring to Figure 9, as the level of the input signal to the active device is increased, the power level of the output signal will increase linearly up to the output 1 dB compression point (OP_{1dB}). As the level of the input signal is increased above the input 1 dB compression point (IP_{1dB}), the

active device goes into compression. That is, the increase in the power level of the output signal reduces when the power level of the input signal is increased to an extent such that the non-linear properties of the active device restrict the voltage and current waveforms of the output signal. The non-linear characteristics in this region of operation restrict the output current and voltage swings and limit the output power to its saturated quantity (Colantonio, Giannini and Limiti, 2009), expressed as:

$$P_{\text{sat}}(f_0) = \lim_{P_{\text{in}} \to \infty} \left[P_{\text{in}}\left(f_0\right) \right] \qquad \text{W} \tag{3.7}$$

According to Colantonio, Giannini, and Limiti (2009:2) as the power gain approaches zero the power gain in dB is expressed by:

$$G_{\text{dB}} = (10)\log_{10}\left(G\right) = P_{\text{RFout,dBm}} - P_{\text{RFin,dBm}} \tag{3.8}$$

3.2.5 PA Linearity

PAs are classified as non-linear amplifiers since they are operated within their non-linear region to reduce the power dissipation within the active device. The operation of PAs in their non-linear region leads to an unfavourable replication of the input signal at the output port. That is, the output signal is severely distorted and contains multiple harmonics of the fundamental component of the input signal (Colantonio, Giannini & Limiti, 2009:1).

PA linearity parameters include:

- 1 dB Compression Point: $IP_{1\text{dB}}$ and $OP_{1\text{dB}}$
- Minimal Detectable Signal Level (IP_{MDS} and OP_{MDS})
- Intermodulation Distortion Products (*IMD*)
- Dynamic Range (*DR*)
- Third Order Intercept Point: IIP_3 and OIP_3
- Error Vector Magnitude (EVM)
- Adjacent Channel Power Ratio (ACPR)

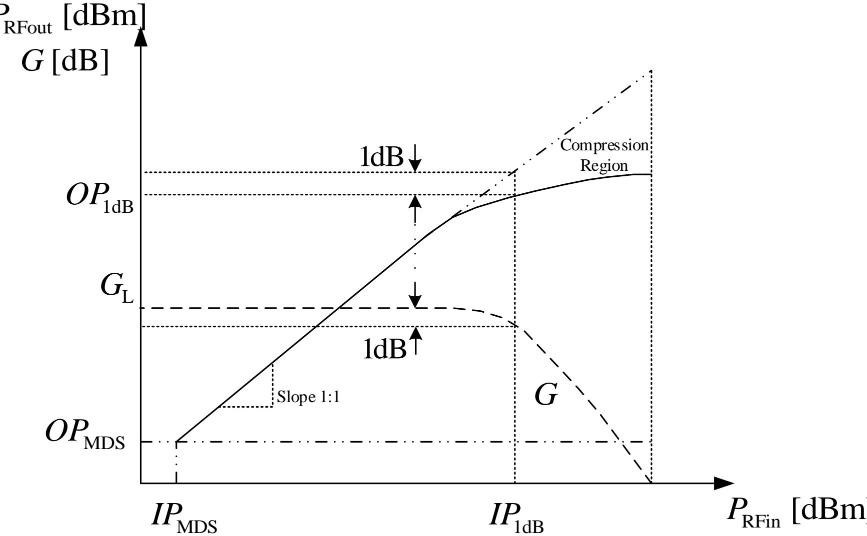


Figure 9: P_{RFout} vs P_{RFin} (Adapted from Colantonio, Giannini & Limiti, 2009:4)

3.2.5.1 The 1 dB Compression Point

Ideally, as the amplitude of the input signal is increased so will the amplitude of the output signal in a linear fashion. However, a further increase in input signal power will cause the amplifier to saturate and operate in its region of compression (Whaits & MacPherson, 2004:6-2)

The OP_{1dB} power level, specified in dBm, is a parameter used to quantify the linearity and the maximum output power which an amplifier can provide while still being considered to operate within its linear region (Louw, 2015:19).

The IP_{1dB} and OP_{1dB} power levels are determined by:

$$IP_{\mathrm{1dB}} = OP_{\mathrm{1dB}} + 1\mathrm{dB} - G_{\mathrm{L}} \qquad \mathrm{dBm} \tag{3.9}$$

$$OP_{\mathrm{1dB}} = (G_{\mathrm{L}} - 1\mathrm{dB}) + IP_{\mathrm{1dB}} \qquad \mathrm{dBm} \tag{3.10}$$

The greater the *DR* the greater the linearity of the amplifier and the greater the maximum output power level obtainable.

3.2.5.2 Minimal Detectable Signal Level

An amplifier is deemed to have a linear region of operation where an increase in input signal level will result in a proportional increase in output signal level. This region of operation is referred to as the region of linear gain (Whaits & MacPherson, 2004:6-1)

Noise is an inevitable phenomenon in electronic circuitry and the minimum level of the input signal which an amplifier can operate on is limited to and determined by the level of the noise floor. This minimum input signal level is known as the IP_{MDS}. This IP_{MDS} level corresponds to an output power level known as the OP_{MDS} (Whaits & MacPherson, 2004:6-3).
These quantities can be determined as follows:

$$IP_{\text{MDS}} = -174 + 10\log(B) + 10\log(F) + x \qquad \text{dB} \tag{3.11}$$

$$OP_{\text{MDS}} = -174 + 10\log(B) + 10\log(F) + x + 10\log(G_{\text{L}}) \qquad \text{dB} \tag{3.12}$$

where,

the minimum level of the input signal is x dB above the thermal noise floor

$K.T_{\text{o}}.B = -174$ dBm.Hz^{-1}

K = Boltzmann’s constant

T_{o} = Standard room temperature in Kelvin

B = System Bandwidth in Hertz

F = Noise factor

3.2.5.3 Intermodulation Distortion Products

Typically, the input signal to an amplifier comprises several components at different frequencies. The amplifier does not only amplify this complex input signal but also generates other unwanted signal components due to its non-linear behaviour. The unwanted signals generated are harmonics and also intermodulation distortion (*IMD*) products (Krauss, Bostian & Raab, 1980:361-362).

Intermodulation distortion products consist of sums and differences of the signal components of the input signal, as shown in Figure 10. The lower the level of the third-order components the greater the level of OIP_3 and the more linear the amplifier is deemed to be.

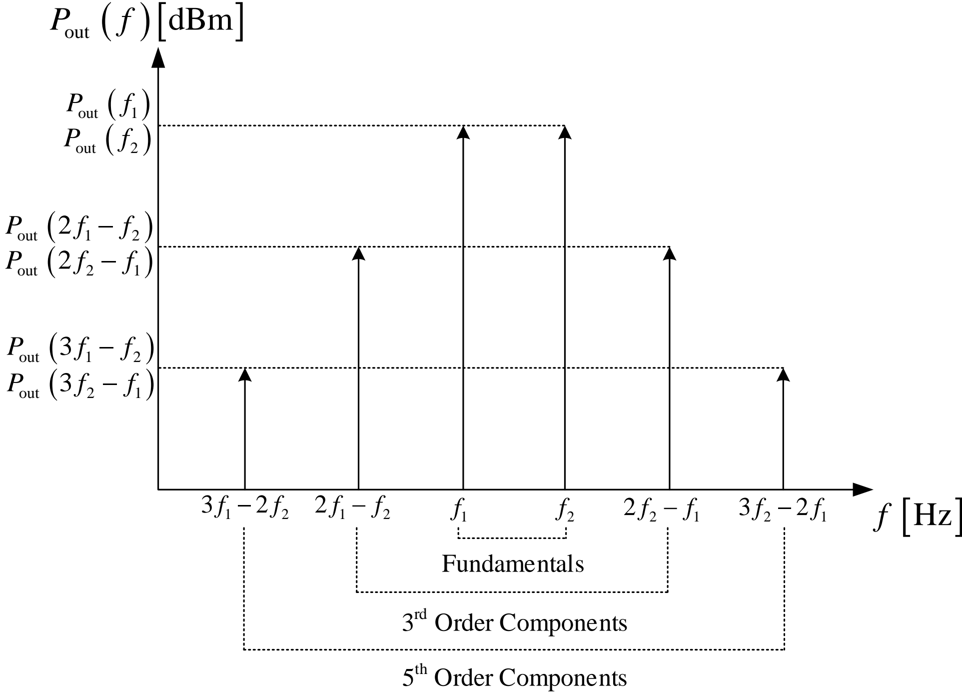


Figure 10: Two-Tone *IMD* Products (Whaits & MacPherson, 2004:6-5)

3.2.5.4 Third-Order Intercept (*TOI*) Point

According to Whaits & MacPherson, (2004:6-5) the OIP_3 level can be defined as the theoretical output power level at which the third-order and fundamental components intersect. At this point, the theoretical output power level of the fundamental component is equal to the theoretical output

power level of the third-order component of the output signal. The greater the value of OIP_3 the more linear the amplifier is deemed to be. The *TOI* point is given by:

Referenced to the output port of the DUT:

$$OIP_3 = P_{\text{out}}\left[\text{dBm}\right] + \frac{\Delta}{2} \qquad \text{dBm} \tag{3.13}$$

Referenced to the input port of the DUT:

$$IIP_3 = P_{\text{out}}\left[\text{dBm}\right] + \frac{\Delta}{2} - G_{\text{L}} \qquad \text{dBm} \tag{3.14}$$

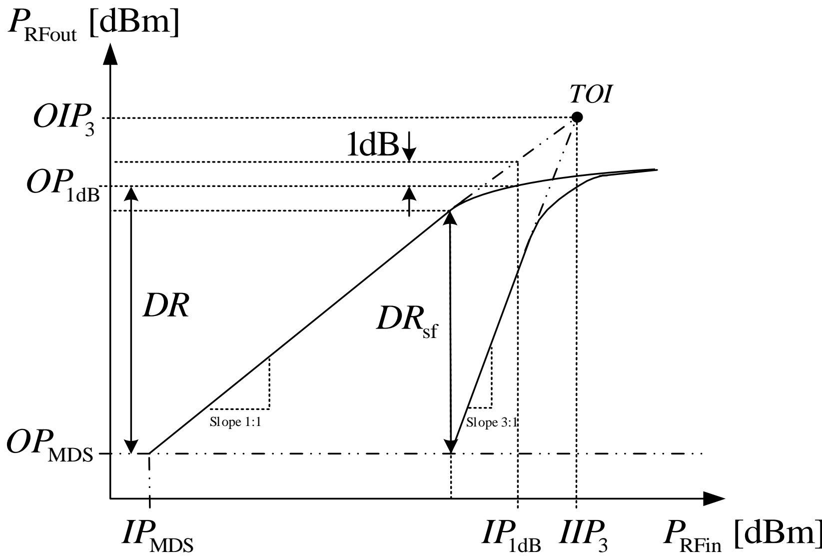


Figure 11: Third Order Intercept Point (Whaits & MacPherson, 2004:6-3; Colantonio, Giannini & Limiti, 2009:3)

3.2.5.5 Dynamic Range

The dynamic range of an amplifier is defined as the range of output signal power levels over which the amplifier is deemed to operate within its linear region (Whaits & MacPherson, 2004:6-2). This range is limited by the level of the noise floor and the $OP_{1\text{dB}}$ point of the amplifier.

$$DR = OP_{1\text{dB}} - OP_{\text{MDS}} \qquad \text{dB} \tag{3.15}$$

According to Whaits & MacPherson, (2004:6-6) The spurious-free dynamic range of an amplifier is the range of signal power levels over which the output signal will not contain any significant *IMD* products and is given by:

$$DR_{\mathrm{sf}} = \frac{2}{3}\left(OIP_3 - OP_{\mathrm{MDS}}\right) \qquad \mathrm{dB} \tag{3.16}$$

The greater the *DR* the greater the range of linear operation.

3.2.5.6 EVM

According to Colantonio, Giannini & Limiti, (2009:20), the EVM is used to further characterise a non-linear PA by assessing the generated distortion of the output signal. This distortion refers to the unwanted change in the amplitude, frequency, and phase of the output signal. The EVM is the Euclidian distance measurement between an ideal reference waveform (signalling point) and the distorted waveform (signalling point) and is illustrated in Figure 12. This measurement is used in profiling the linearity performance of a PA when driven by a modulated signal. The less the EVM the greater the linearity of the PA.

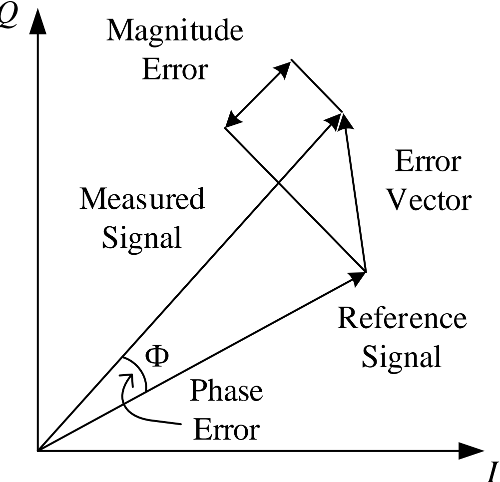


Figure 12: EVM and Associated Quantities (Adapted from Colantonio, Giannini & Limiti, 2009:20)

3.2.5.7 ACPR

Due to the non-linear behaviour of PAs, a certain amount of the power spectral density of the output signal is present in adjacent channels. The measurement of the ACPR is used to quantify the level of the output signal which exists in the adjacent channel, and further characterise the power spectral behaviour, that is the *BW* and hence the filtering characteristics of a PA when driven by a modulated signal (Colantonio, Giannini & Limiti, 2009:15-17; Mugisho, 2016:7). According to Colantonio, Giannini & Limiti, (2009:16) the ACPR is given by:

$$ACPR = \frac{P_{\text{in-band}}}{P_{\text{in the adjacent channel}}} \tag{3.17}$$

The greater the value of ACPR the less the interference of the output signal in the adjacent channel.

3.2.6 *PE*

Since a PA can be construed to be a DC to RF power converter as is illustrated in Figure 7, the DC power supply, according to Colantonio, Giannini & Limiti, (2009:4), is the product of the DC bias voltage and the average value of the bias current, and given by:

$$P_{\text{DC}} = V_{\text{bias}} \cdot \frac{1}{T} \cdot \int_0^T I_{\text{bias}}(t) \cdot dt \qquad \text{W} \tag{3.18}$$

The *PE* is the conversion ratio of DC power to usable RF output power and is also known as the drain efficiency (*DE*) in the case of FETs or collector efficiency (*CE*) in the case of BJTs. The power efficiency ratio is given:

$$\eta_{\text{PE}} = \frac{P_{\text{RFout}}}{P_{\text{DC}}} \tag{3.19}$$

The greater the value of η_{PE} the more efficient the amplifier is deemed to be.

3.2.7 *PAE*

The *PAE* of a PA, as stated by Kazimierczuk, (2008:6), is the comparison between $\left(P_{\mathrm{RFout}} - P_{\mathrm{RFin}}\right)$ and P_{DC}, which is given by:

$$\eta_{\mathrm{PAE}} = \frac{P_{\mathrm{RFout}} - P_{\mathrm{RFin}}}{P_{\mathrm{DC}}} \tag{3.20}$$

The greater the value of η_{PAE} the more efficient the amplifier is deemed to be.

3.3 PA Power Balance

To obtain 100% *PE*, it is required that all the DC power utilised by the active device be converted into RF output power. The two factors which limit the *PE* are the power dissipated in the active device and the power due to the harmonic content which is dissipated in the load. The power dissipated in the active device is a function of the drain- current and voltage waveforms (Colantonio, Giannini & Limiti, 2009:178) and expressed as:

$$P_{\mathrm{diss}} = \frac{1}{T}\int_0^T v_{\mathrm{DS}}(t)\, i_{\mathrm{DS}}(t)\, dt \qquad \mathrm{W} \tag{3.21}$$

The output power delivered by the active device comprises the following two entities: $P_{\mathrm{RFout}}\left(f_0\right)$ and $P_{\mathrm{RFout}}\left(nf_0\right)$. $P_{\mathrm{RFout}}\left(f_0\right)$ is the power delivered to the load of the active device at the fundamental frequency and $P_{\mathrm{RFout}}\left(nf_0\right)$ is the powered delivered to the load of the active device at multiples of the fundamental frequency, where $\{n \in \mathbb{Z}, n > 1\}$ (Colantonio, Giannini & Limiti, 2009:178).

The Fourier series expansions of the drain voltage and current waveforms are given by:

$$i_{\mathrm{DS}}\left(t\right)=I_0+\sum_{n=1}^{\infty}I_n\cdot\cos(n\omega t+\xi_n) \tag{3.22}$$

$$v_{\mathrm{DS}}\left(t\right)=V_{\mathrm{DD}}+\sum_{n=1}^{\infty}V_n\cdot\cos(n\omega t+\psi_n) \tag{3.23}$$

where, $\omega=2\pi f$, ξ_n and ψ_n are the phases of the n$^{\mathrm{th}}$ harmonic current I_n and voltage V_n components respectively, (Colantonio, Giannini and Limiti, 2009).

The power dissipated in the active device is a function of the phase shift ϕ_{n} between V_n and I_n, and also a function of the magnitude of the harmonic components present. The quantities V_n and I_{n} are directly- and indirectly proportional to the load impedance of the active device $Z_{\mathrm{L}}(nf_0)$, in accordance with Ohm's law. The power due to the harmonic components, according to Colantonio, Giannini & Limiti, (2009:179) to $P_{\mathrm{RFout}}\left(nf_0\right)$ is given by:

$$P_{\mathrm{RFout}}\left(nf_0\right)=\frac{1}{2}V_nI_n\cos\left(\phi_n\right)=\frac{1}{2}Z_{\mathrm{L}}\left(nf\right)I_n^2\cos\left(\phi_n\right)=\frac{1}{2}Y_nV_n^2\cos\left(\phi_n\right) \qquad \mathrm{W} \tag{3.24}$$

The DC input power to the active device is expressed as the sum of the power dissipated in the active device, the power delivered to the load at the operating frequency, and the power delivered to the load at the frequencies of the harmonic components.

$$P_{\mathrm{DC}}=P_{\mathrm{RFout}}\left(f_0\right)+P_{\mathrm{diss}}+\sum_{n=2}^{\infty}P_{\mathrm{RFout}}\left(nf_0\right) \qquad \mathrm{W} \tag{3.25}$$

Therefore (3.19) can be expressed as:

$$\eta_{\mathrm{PE}}=\frac{P_{\mathrm{RFout}}\left(f_0\right)}{P_{\mathrm{RFout}}\left(f_0\right)+P_{\mathrm{diss}}+\sum_{n=2}^{\infty}P_{\mathrm{RFout}}\left(nf_0\right)} \tag{3.26}$$

Hence, it becomes clear that to obtain a PE of 100%, that is $P_{\mathrm{DC}} = P_{\mathrm{RFout}}(f_0)$, the second two terms in the denominator of equation (3.26) must be zero. That is,

$$P_{\mathrm{diss}} + \sum_{n=2}^{\infty} P_{\mathrm{RFout}}(nf_0) = 0 \qquad \mathrm{W} \tag{3.27}$$

Thus, to obtain the maximum PE of 100% the two conditions that must be simultaneously satisfied are:

$$P_{\mathrm{diss}} = \frac{1}{T}\int_0^T v_{\mathrm{DS}}(t)\, i_{\mathrm{DS}}(t)\, dt = 0 \qquad \mathrm{W} \tag{3.28}$$

and

$$P_{\mathrm{RFout}}(nf_0) = \frac{1}{2}V_n I_n \cos(\phi_n) = \frac{1}{2}Z_{\mathrm{L}}(nf_0) I_n^2 \cos(\phi_n) = \frac{1}{2}Y_n V_n^2 \cos(\phi_n) = 0 \qquad \mathrm{W} \tag{3.29}$$

where $n \neq 1$

Achieving the conditions as specified in equations 3.28 and 3.29, are theoretically possible but in practice, these conditions are the focus of much research.

3.4 Design Principles

The main objective in implementing an optimum design of a PA is to extract the maximum performance from the active device while operating it in a reliable and non-damaging manner (Whaits & MacPherson, 2004:12). Precautions must be implemented to ensure that the practical constraints placed on actual active devices do not cause damage or limit the performance thereof.

3.4.1 Load-Line Matching

The load-line matching technique is used to ensure that maximum power can be extracted from an active device by utilising the maximum permitted current and voltage swing for that particular active device. According to Whaits and MacPherson, (2004:6-12), this is achieved by implementing load-line theory to select an optimum load resistance which is given by:

$$R_{opt} = \frac{v_{DSmax}}{i_{DSmax}} \ \Omega \tag{3.30}$$

where, v_{DSmax} and i_{DSmax} equal the maximum selected drain voltage and current, assuming that R_{gen} >> R_{opt}, where R_{gen} is the impedance of the source generator.

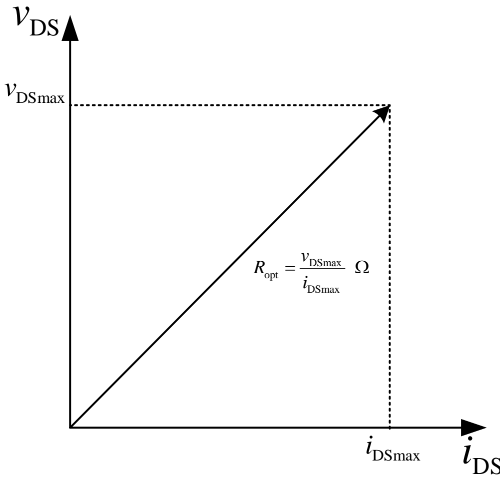


Figure 13: Load-Line Match (Whaits & MacPherson, 2004:13)

The load-line match is a real-world compromise implemented to extract maximum power from active devices and simultaneously keep the RF voltage swing within specified limits and the available DC supply. The load-line method is a useful and convenient way to strive for optimum load conditions, especially during the absence of modern computer-aided design (CAD) techniques. However, according to Colantonio, Giannini and Limiti, (2009:23) the load-line method results in the degradation of the output VSWR of the system.

3.4.2 Load-Pull

According to Cripps, (2006:20), there is a relationship between output power and output matching. A load-pull measurement is performed by using a form of calibrated tuning at the output port of an active device and then displaying the measured data on a Smith chart.

Load-pull data allows a designer to more accurately target a predefined impedance which can be of assistance to design appropriate matching networks. In essence, it allows the transformation of a non-linear problem to be solved in a linear fashion (Cripps, 2006:20).

There are numerous methods to implement load-pull techniques and it is eventually decided by the designer, customer, or based on design requirement (Simpson, 2014:1-6).

Fundamentally the load-pull technique implements a controlled varied impedance at the output port of an active device to obtain the optimal performance of this active device (Ghannouchi & Hashmi, 2011:1).

The conventional laboratory technique to design and build PAs is more reliable and accurate but is not ideal enough for mass production and is not time-efficient for market turnover (Ghannouchi & Hashmi, 2011:1).

CAD techniques have decreased the time for the design process and greatly simplified manufacturing procedures. The performance of the active device is governed by the precision of the active device model which is provided by the vendor (Ghannouchi & Hashmi, 2011:1).

The load-pull technique plays an essential part in high-performance PAs, high efficient harmonic tuned PAs and for the data generation for non-linear PAs (Ghannouchi & Hashmi, 2011:1).

A typical setup for a load-pull measurement is illustrated in Figure 14.

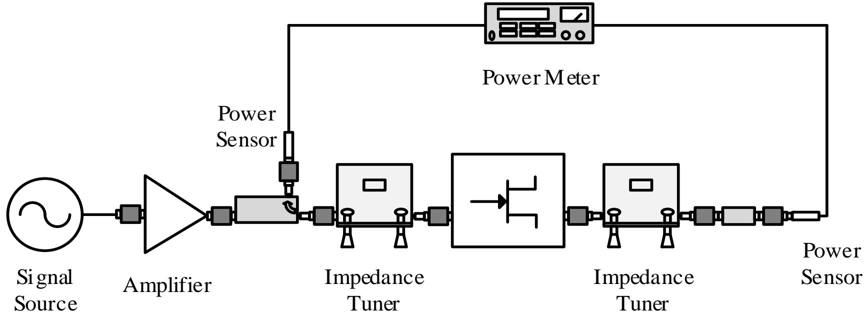


Figure 14: Classical Load-Pull Setup (Keysight, 2014:9)

3.5 Conclusion

Fundamentally a PA is a DC to RF power converter and the efficiency of this power conversion process is fundamental in the performance of a PA. Important characteristics of a PA are the RF output power, the power gain, the efficiency, and the linearity.

The output power is a function of the shape and phase of the drain voltage and current waveforms and must be closely controlled to ensure maximum output power and efficiency.

The most important linearity parameters of a PA are the 1 dB compression point, the third-order intercept point, the intermodulation distortion parameter, the dynamic range, the EVM, and ACPR.

The design of PAs is a trade-off between many conflicting requirements which typically include efficiency vs linearity or increased RF output power level vs minimal distortion and a balance between these conflicting requirements must be pursued to maximise the performance of the PA.

Chapter 4

Classes of Power Amplifiers

4.1 Introduction

PAs are traditionally categorised based on their classes of operation. The literature on these established classes initially seems relatively straightforward but can be complex to perceive due to ambiguities and vagueness which can also be delusive (Colantonio, Giannini & Limiti, 2009:24).

Examination of the circuit topology of an amplifier is not enough to accurately characterise the class of operation (Sokal, 1997:179). The operating class can be broken down into the following sub-categories: bias-point, matching-network topology, operating conditions and conduction angle (Colantonio, Giannini & Limiti, 2009:24).

According to Colantonio, Giannini & Limiti (2009:24), the term *biasing class* defines the quiescent bias point of the active device. The quiescent bias point determines the output current waveform conduction angle (CWCA), that is, the portion of the cyclic nature of the input signal over which the active device is conducting current. In this thesis, the term biasing class will also define the quiescent bias point of the active device.

The various operating classes of a PA will be explained with the aid of idealised devices to gain a more in-depth and illustrative understanding as to why they are categorised as such.

Operating Class	Current Conduction Angle (θ °)	Dependence on Drive Level	Biasing	
			FET	BJT
A	$\theta = 360°$	No	Midway between Device Pinch-off and Saturation regions	Midway Between Device Cut-off and Saturation regions
AB	$180° < \theta < 360°$	Yes	Above Pinch-off	Above Cut-off
B	$\theta = 180°$	No	Device Pinch-off	Device Cut-off
C	$\theta < 180°$	Yes	Below Pinch-off	Below Cut-off

Table 2: Classifications of PAs in terms of output conduction angle θ or biasing point (Adapted from Colantonio, Giannini & Limiti, 2009:24)

In Table 2, the input signal to the PA is sinusoidal and the amplifying device is used in current source mode with regards to a BJT and voltage-controlled mode with regards to a FET.

The *PE* of the bias-class amplifiers is presented in Table 3.

Biasing Class	Maximum Theoretical Efficiency	Reference
A	50%	(Mugisho, 2016:26)
AB	60-70%	(Berglund, Johansson and Lejon, 2006:93)
B	78.5%	(Prodanov & Banu, 2007:6)
C	Tends to 100%	(Prodanov & Banu, 2007:355)

Table 3: Bias-Class Power Efficiencies

4.2 Current Controlled Device

A BJT is termed a current controlled device due to the collector current (I_C) being controlled which is achieved by controlling the base-emitter voltage (V_{BE}). Referring to Figure 15 (a), as the base current (I_B) will vary according to Ohm's law. I_B causes a potential difference across the base-emitter junction. An increase in V_{BE} causes I_C to increase and a decrease in V_{BE} causes I_C to decrease. This increase and decrease in I_C is due to the variation in the size of the depletion region in the transistor, as shown in Figure 15 (b), being reduced when less base current flows or enlarged when more base current flows. Thus, I_C is proportional to the I_B and thereby making the BJT a current controlled device (Watkins, 2008:1).

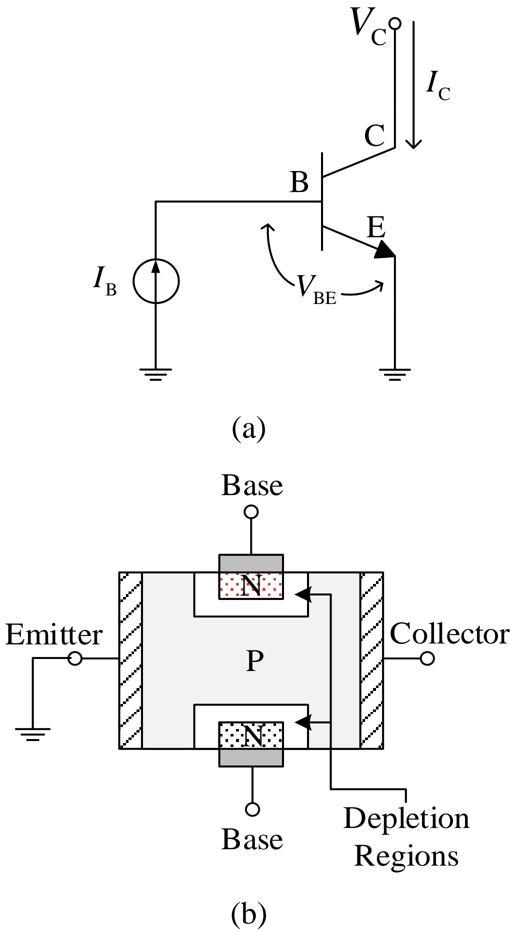


Figure 15: (a) Biased BJT (b) Band Diagram of NPN BJT depicting the Depletion Region (Freescale Semiconductor, 1993:1)

4.3 Voltage Controlled Device

A FET is termed a voltage-controlled device due to the gate-source voltage (V_{GS}) controlling the drain current. Referring to Figure 16 (a), the resistance between the drain and source terminals of the FET is controlled by V_{GS} which in turn controls the drain current I_D (Watkins, 2008:1).

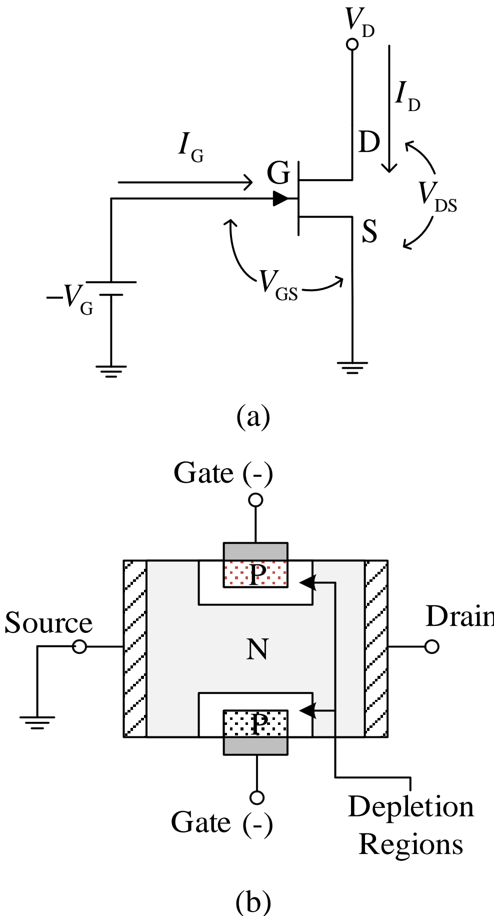


Figure 16: (a) Biased JFET (b) Internal Representation of a PNP JFET depicting the Depletion Regions (Freescale Semiconductor, 1993:1)

In Figure 16 (b), the depletion region encloses the P-type material of the gate terminals when the gate terminals are reversed biased. An increase in the reverse bias voltage will broaden the depletion regions until these two regions touch. This will create a nearly infinite resistance between the drain and source terminals thereby preventing current flow between drain and source (Freescale Semiconductor, 1993:1).

4.4 Operating Classes of PAs

Another important approach of classifying a PA is the operating conditions of the active device which are controlled by the load terminations of this active device. The operating classes of a PA can be divided into two broad categories, namely switching- and current-mode PAs (Colantonio, Giannini & Limiti, 2009:24).

Current-mode amplifiers are categorised based on the conditions of the load at harmonic frequencies of the fundamental, which determines the characteristics of the drain voltage and current waveforms, that is, wave-shaping, all to improve the level of the output power and the *PE* of the amplifier.

Switch-mode amplifiers are categorised based on their switching (conduction) time, their duty-cycle, or combinations of these. Figure 17 illustrates both the biasing and operational classes of PAs (Colantonio, Giannini & Limiti, 2009:24).

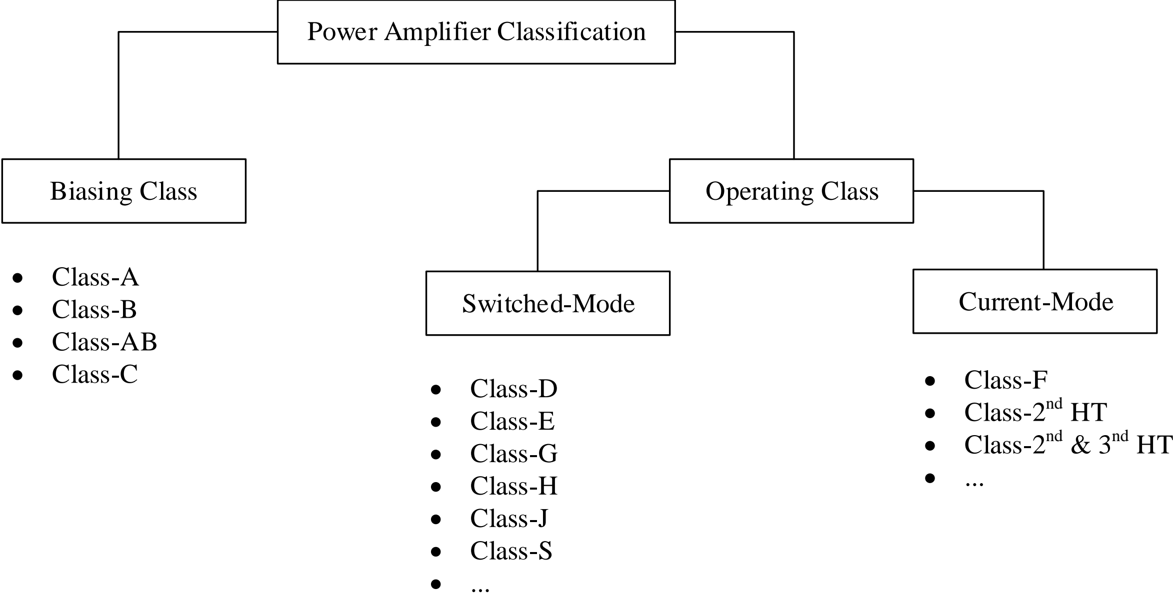


Figure 17: Graphical Summary of PA Classification Structure (Adapted from Colantonio, Giannini & Limiti, 2009:24)

4.5 I-V Characteristic Curves

The characteristic curves of current vs voltage (I-V curves) of an active device graphically define the behaviour of a device. The I-V characteristic curves are typically used to map the behaviour of transistors so that a better understanding can be obtained of the limitations of the device and so to extract the optimal operational conditions. These operational conditions include the efficiency and power gain or a combination of the two. Figure 18 and Figure 19 illustrate the I-V characteristic curves of a BJT and JFET transistor respectively.

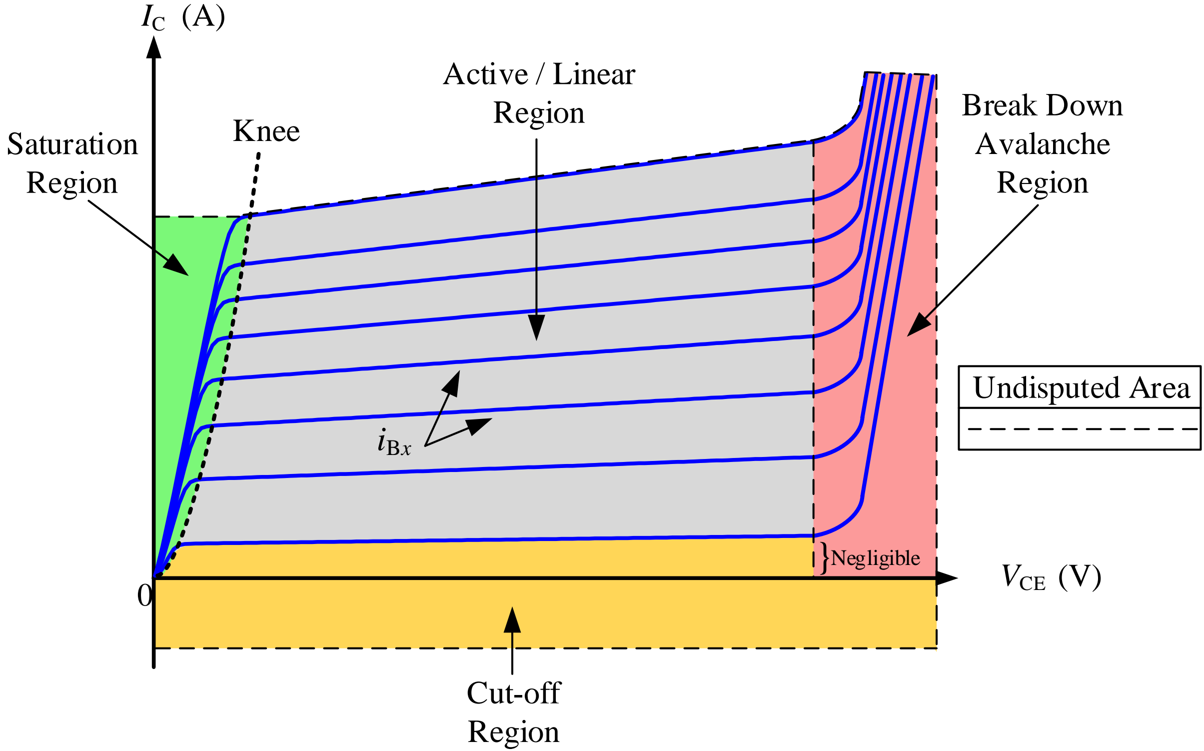


Figure 18: I-V Curves of a BJT (Adapted from Floyd, 2012:161)

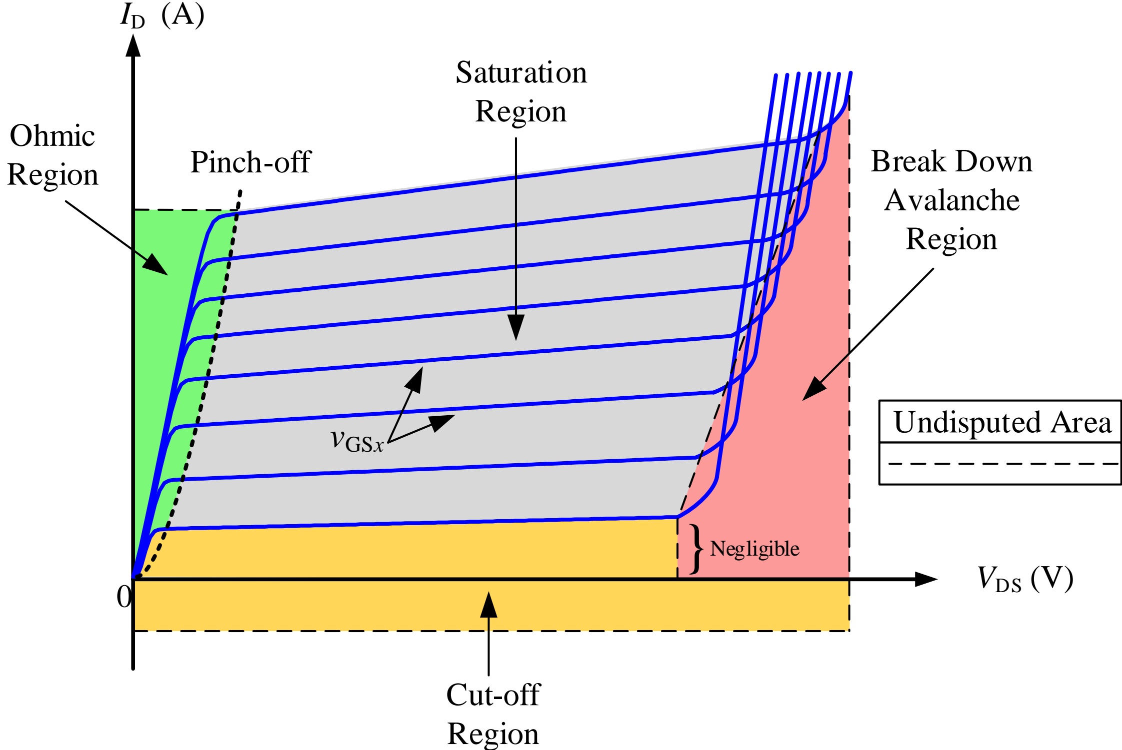


Figure 19: I-V Curves of a FET (Adapted from Colantonio, Giannini & Limiti, 2009:39; Floyd, 2012:388)

4.6 Biasing Classes

4.6.1 Class-A

The Class-A amplifier is considered as a linear amplifier due to its nature of producing an output signal which is an amplitude scaled replica of the input signal and is illustrated in Figure 20.

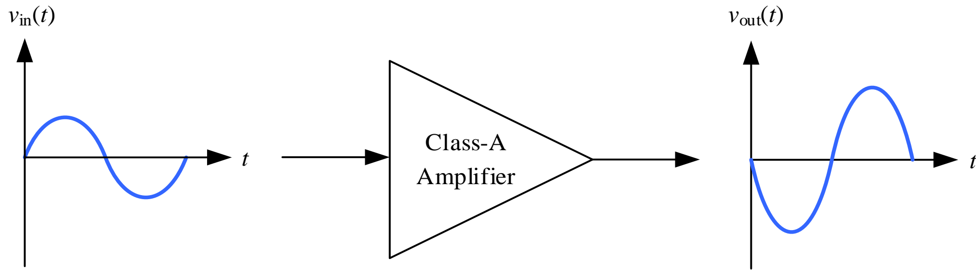


Figure 20: Input-Output Relationship of a Class-A Amplifier

The BJT is operated as a dependant current source and is defined as a device that conducts current continuously over a full period of the input signal. The level of the input signal is maintained low enough to prevent the transistor from being driven into cut-off.

A Class-A amplifier is defined by the specific quiescent bias conditions, often referred to as a *Q*-point, but more accurately it is the necessary and sufficient conditions which allow the amplification of the input signal to be linearly reproduced. The Class-A amplifier is biased midway between the device pinch-off and saturation region for FET amplifiers, and midway between the device cut-off and saturation region for BJTs, as shown in Figure 21.

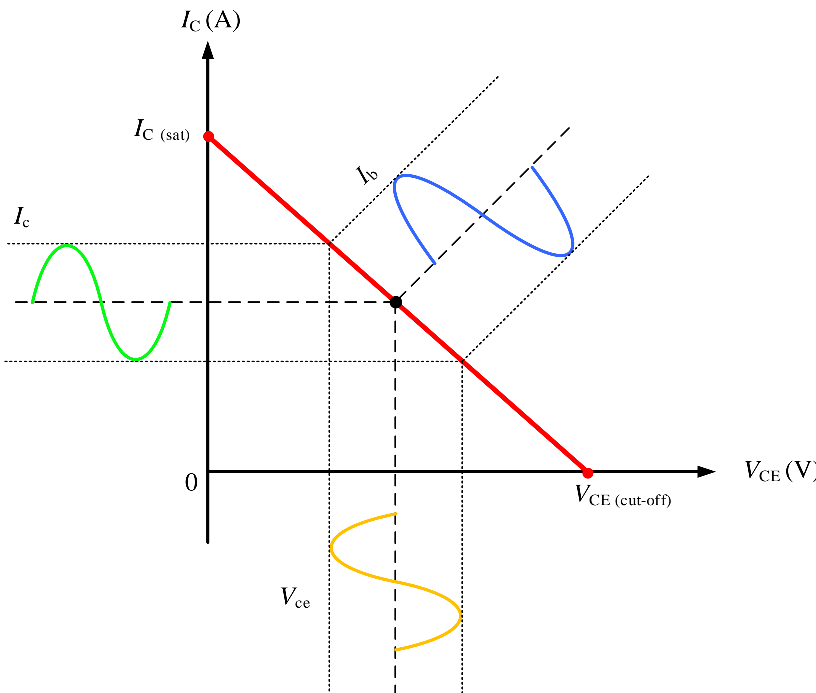


Figure 21: Biasing Conditions for a Class-A BJT Amplifier

The maximum theoretical *PE* which can be obtained from a Class-A PA is 50 %. This implies that half of the power drawn from the DC supply is dissipated in the active device (Mugisho, 2016:26). This phenomenon is due to the overlap in the time domain representations of the collector current and collector voltage or the drain voltage and drain current for BJTs and FETs respectively, as shown in Figure 22. This maximum overlap implies a greater dissipation of power, hence a lower *PE*.

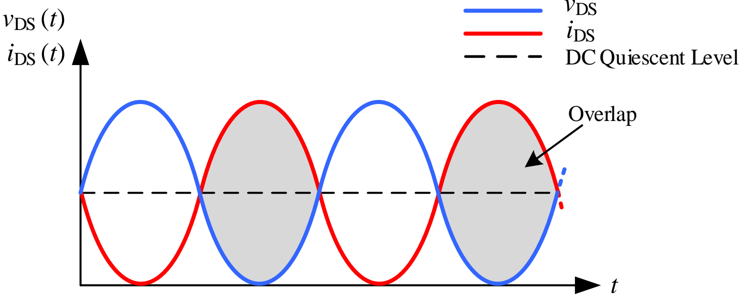


Figure 22: The Drain Voltage and Current Waveforms of a Class-A Amplifier (Adapted from Prodanov & Banu, 2007:355)

4.6.2 Class-B

The Class-B amplifier operates within its linear region for half of the period of the input signal and in cut-off for the second half cycle.

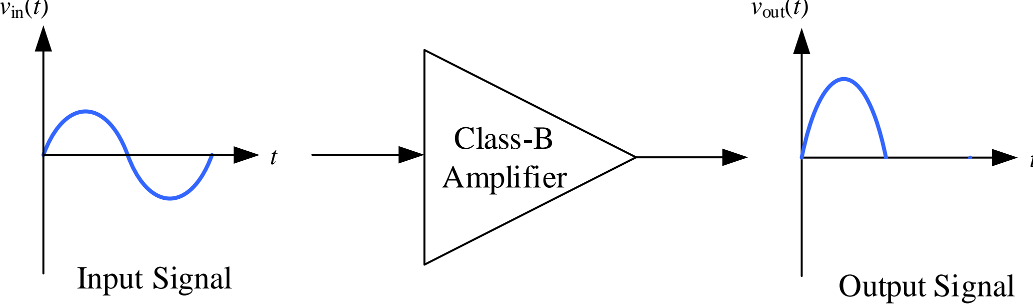


Figure 23: Input-Output Relationship of a Class-B Amplifier

The Class-B amplifier is biased at its cut-off point for both BJTs and FETs. These quiescent biasing conditions accommodate for a much larger input signal to be amplified.

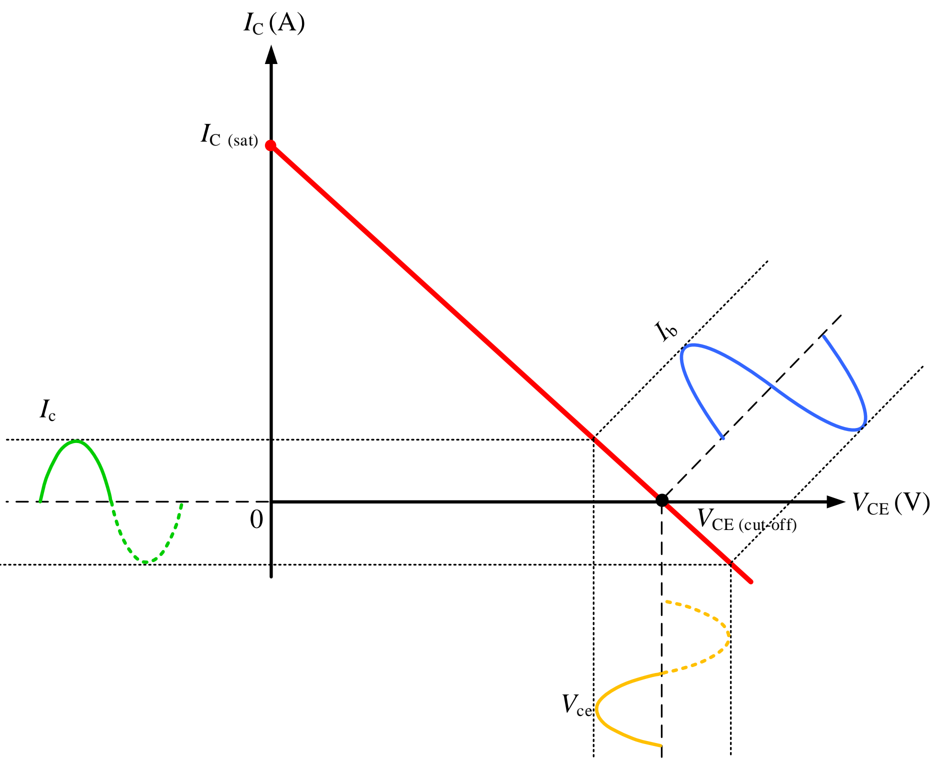


Figure 24: Biasing Conditions for a Class-B Amplifier

The Class-B amplifier is particularly useful when operated in a push-pull configuration with a complimentary pair of transistors being used. That is when two transistors with matched characteristics, one transistor is a npn and the other a pnp transistor, then a highly symmetrical output signal can be obtained. The one transistor is used to amplifier the positive half-cycle of the input signal and the other is used to amplify the negative half-cycle thereof (Kazimierczuk, 2008:95). This is illustrated in Figure 26, where transistors Q_1 and Q_2 are a complementary pair.

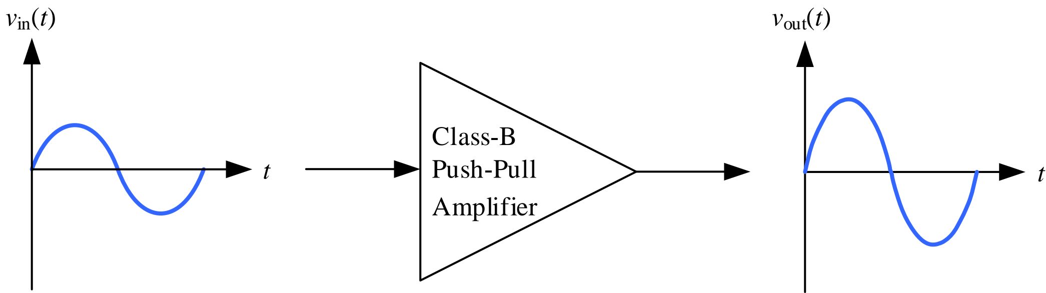


Figure 25: Input-Output Relationship of a Class-B Complementary Push-Pull Amplifier

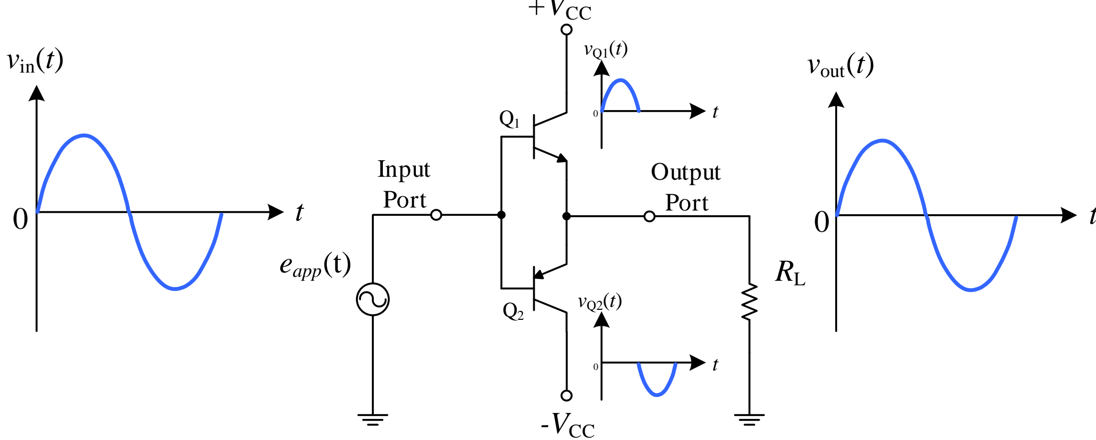


Figure 26: Classical Class-B Complimentary Push-Pull Amplifier (Floyd, 2012:348)

The maximum theoretical *PE* attainable from a Class-B PA is 78.5 % (Prodanov & Banu, 2007:6). As illustrated in Figure 27, the drain voltage and drain current overlap is less than that of the Class-A amplifier, resulting in less power being dissipated in the active device, hence a greater *PE*.

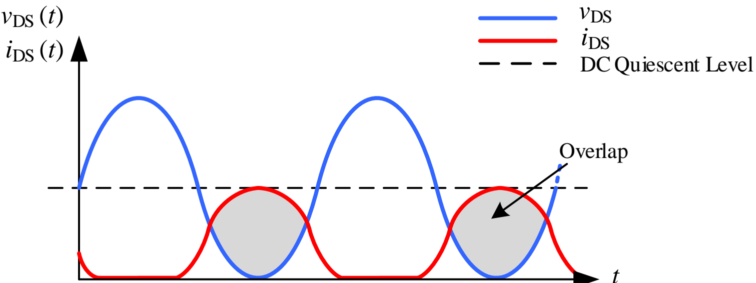


Figure 27: The Drain Voltage and Current Waveforms of a Class-B Amplifier (Adapted from Prodanov & Banu, 2007:355)

The complimentary Class-B push-pull amplifier has a major draw-back termed crossover distortion, and which causes an unwanted distorted output signal, as shown in Figure 28.

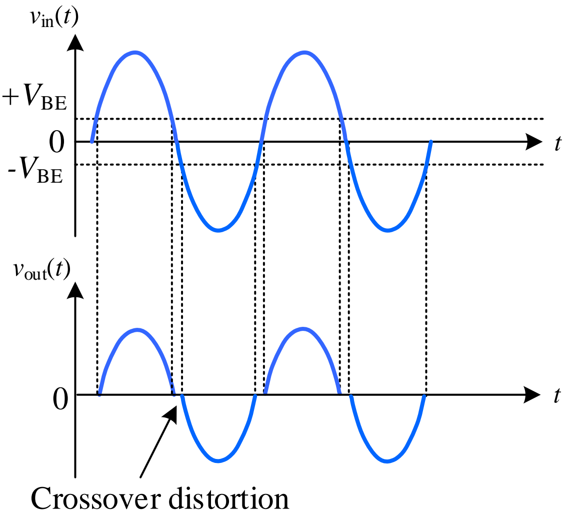


Figure 28: Illustration of Crossover Distortion

Figure 28 illustrates that crossover distortion occurs at the zero crossings of the output signal. This distortion is due to the reverse breakdown voltage of the base-emitter or the gate-source junction which needs to be reached before conduction occurs. This crossover distortion phenomenon led to the development of the classic Class-AB amplifier.

4.6.3 Class-AB

The bias conditions of a Class-AB amplifier are set to overcome the crossover distortion experienced in a Class-B push-pull amplifier. This is achieved by biasing the amplifier slightly into conduction, which will allow the reverse breakdown voltage of the respective junctions of the transistors to be overcome before applying the input signal. To implement the latter, the Class-AB amplifier is strategically biased well below saturation and slightly above cut-off for BJTs and well below pinch-off and slightly above cut-off for FETs, as shown in Figure 30. The Class-AB amplifier, as illustrated in Figure 29, can now be considered as a linear amplifier and is a compromise between linearity and *PE*.

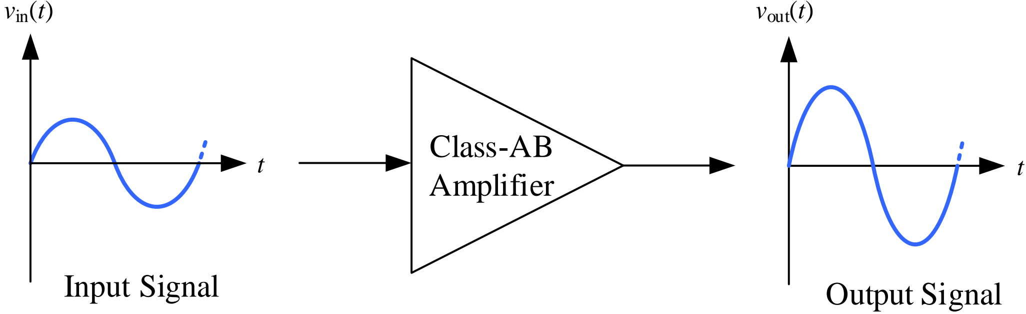


Figure 29: Input-Output Relationship of Class-AB Complementary Push-Pull Amplifier

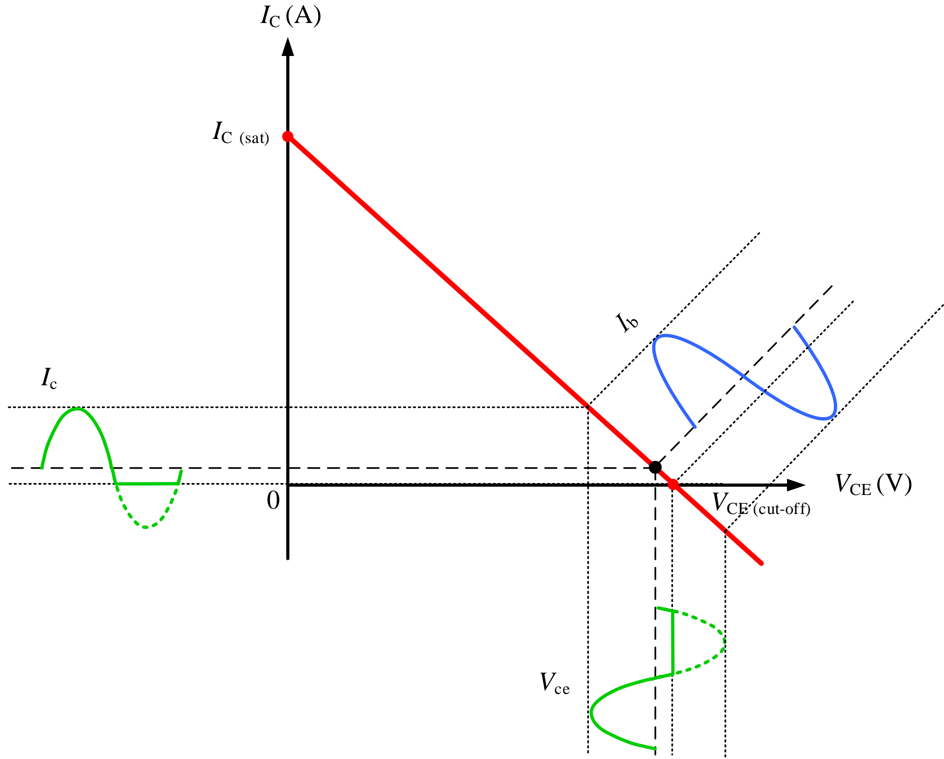


Figure 30: Biasing Conditions for a Class-AB Amplifier

The maximum *PE* attainable in a Class-AB amplifier is 60 % to 70 % (Berglund, Johansson & Lejon, 2006:93). The *PE* is a function of the overlap in the time domain representations of the voltage and current waveforms as illustrated in Figure 31. This *PE* is more than that of a Class-A amplifier but less than that of a Class-B amplifier.

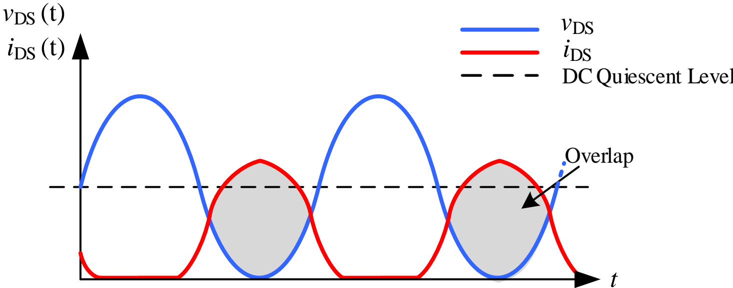


Figure 31: The Drain Voltage and Current Waveforms of a Class-AB Amplifier (Adapted from Prodanov & Banu, 2007:355)

4.6.4 Class-C

The Class-C amplifier is a non-linear amplifier, that is, the output signal is not an amplitude scaled replica of the input signal. The active device conducts current only when the base-emitter voltage, in the case of BJT's or gate-source voltage in the case of FET's, are exceeded by the level of the input signal, as shown in Figure 34 (a) and (b). The Class-C amplifier is biased below the cut-off region for FET and BJT amplifiers.

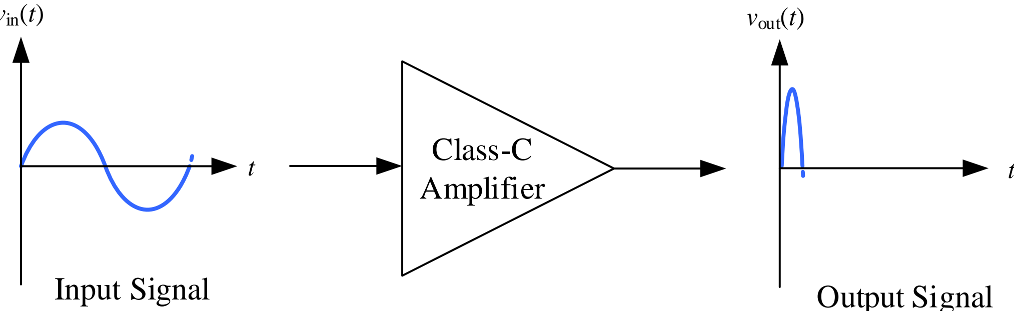


Figure 32: Systematic View of a Class-C Amplifier

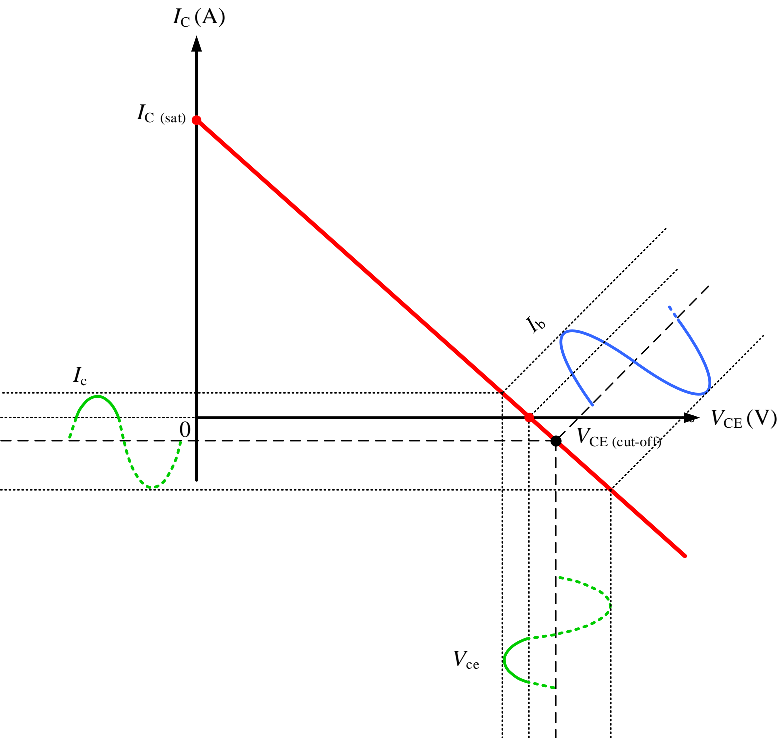


Figure 33: Biasing Conditions for a Class-C Amplifier

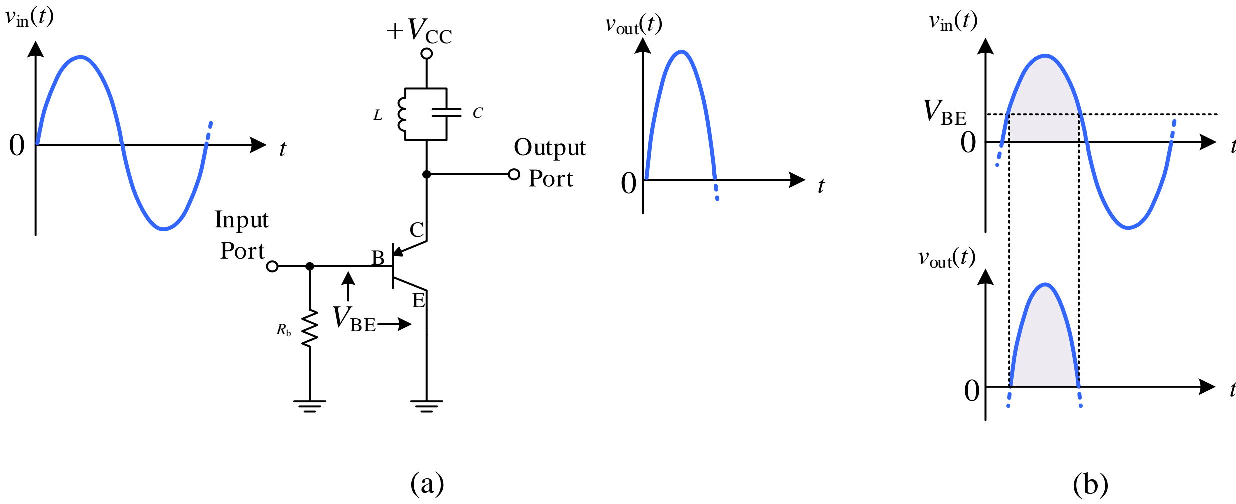


Figure 34: (a) Class-C Amplifier Illustrating Input and Output Relationships (b) Conduction Period Relative to Period of Input Signal

The Class-C amplifier has a theoretical *PE* tending to 100% (Prodanov & Banu, 2007:355). The drain voltage and current overlap for the Class-C amplifier, as shown in Figure 35, is considerably less than that of the Class-A, B and AB amplifiers. Hence, the power dissipated in the active device will be significantly less, thus maximising the *PE*.

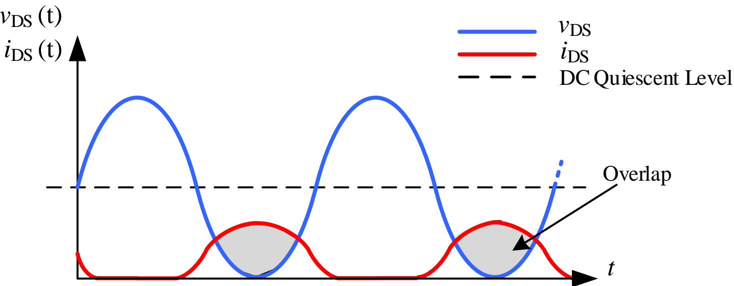


Figure 35: The Drain Voltage and Current Waveforms of a Class-C Amplifier (Adapted from Prodanov & Banu, 2007:355)

4.6.6 BJT Biasing Class Summary

Quiescent Biasing Points and Corresponding Collector-Emitter Voltage Waveforms for BJT Classes-A, AB, B and C

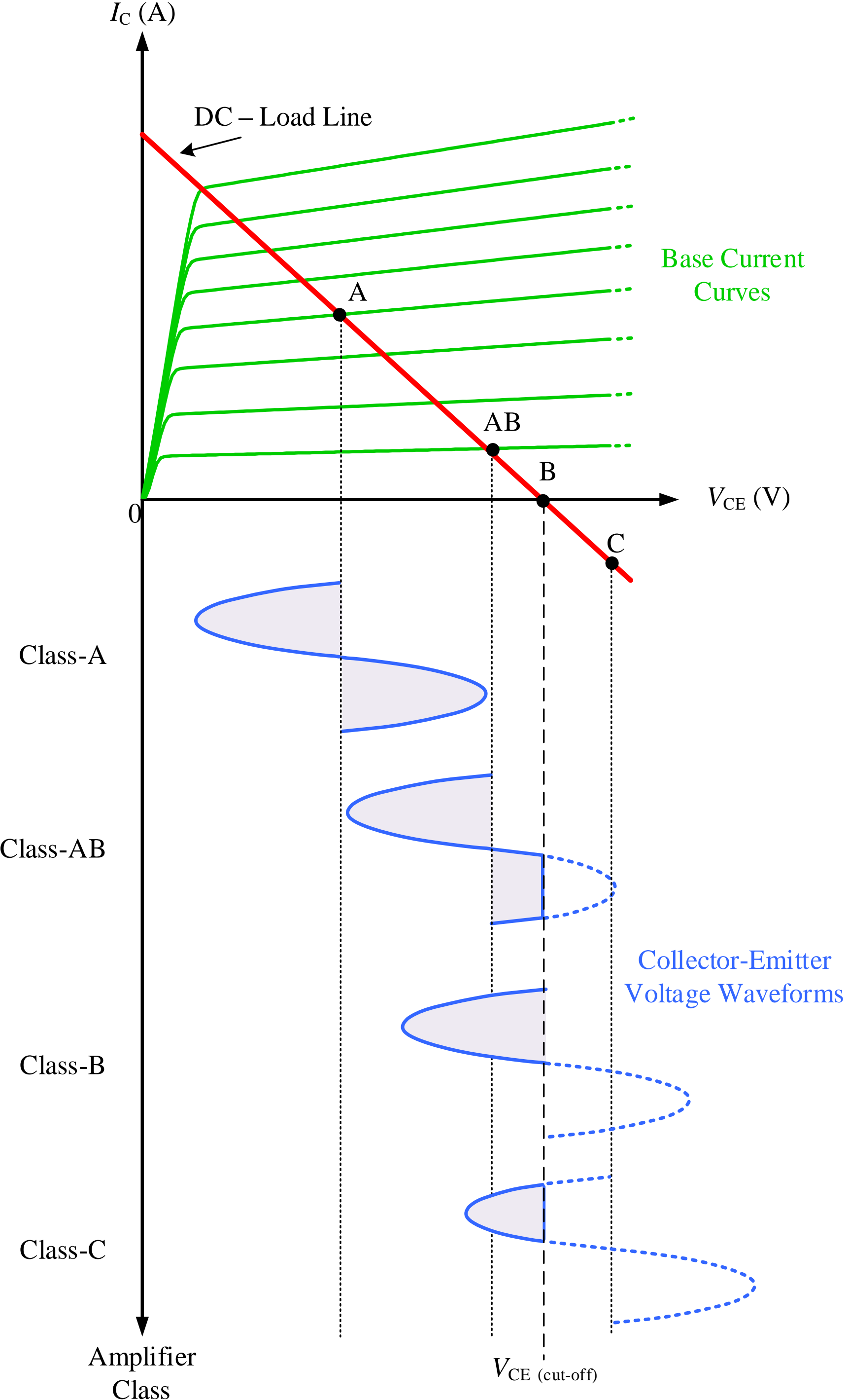


Figure 36: Quiescent Biasing Points and Corresponding Collector-Emitter Voltage Waveforms for BJT Classes-A, AB, B and C (Adapted from Guy *et al.*, 1958:215)

4.6.7 FET Biasing Class Summary

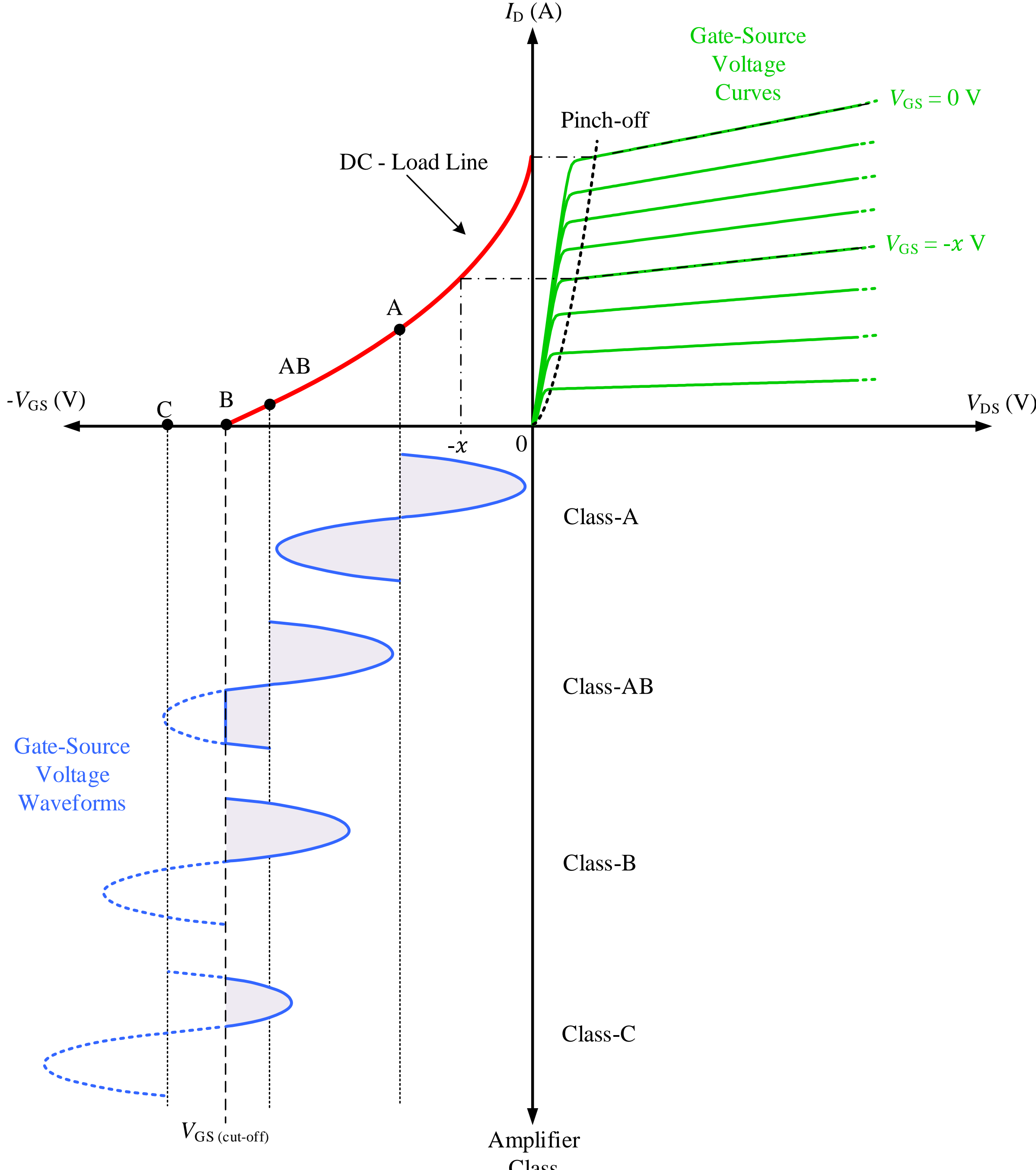


Figure 37: Quiescent Biasing Points and Corresponding Gate-Source Voltage Waveforms for JFET Classes-A, AB, B and C (Adapted from Guy *et al.*, 1958:215)

4.6.8 Biasing Class Summary

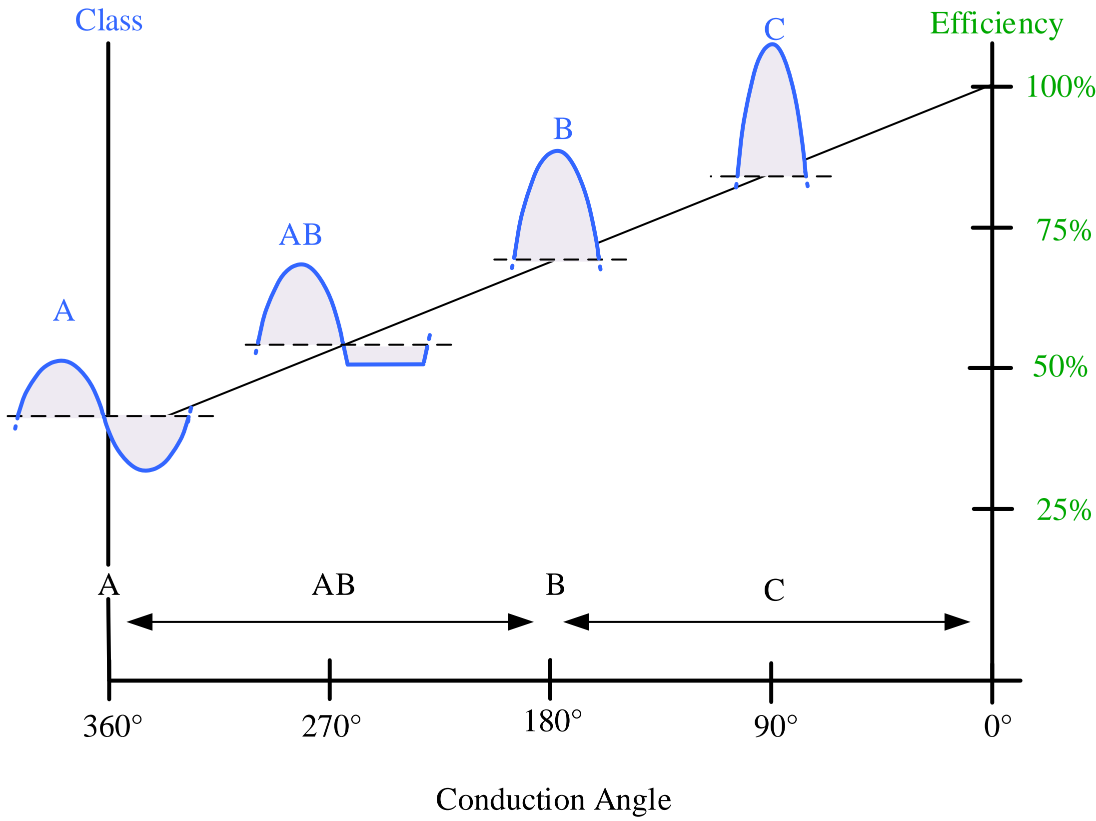


Figure 38: Amplifier Efficiency in terms of Conduction Angle

With regards to Figure 38, a Class-A PA is the least efficient biasing class of PAs but is the most linear, whereas a Class-B PA is less linear than a Class-A PA due to its conduction angle being half of that of the Class-A PA. This also means that a Class-B PA is more efficient than a Class-A PA. A Class-AB PA is a compromise between the efficiency of a Class-B PA and the linearity of a Class-A PA and minimises the crossover distortion present in Class-B operation. A Class-C amplifier produces the highest *PE* of the biasing-class amplifiers but at the cost of having the least linearity.

4.7 Operating Class Amplifiers

4.7.1 Switch-Mode Amplifiers

Amplifier efficiency can be maximised when the BJT or FET is operated as a switch. When the transistor is conducting, the impedance presented in the conduction path is low and acts as an ideal closed switch. Consequently, the active device has a low potential difference across its conduction terminals and a large current is flowing through it (Grebennikov & Sokal, 2007:55).

When the transistor is non-conducting, the impedance presented in the conduction path is very high and acts as an ideal open circuit. Consequently, the active device has a large potential difference across its terminals and no current flows through it (Grebennikov and Sokal, 2007:55). Switch-mode amplifiers incorporate a push-pull technique and can achieve a theoretical *PE* of 100% (Sommarek *et al.*, 2004:115).

4.7.1.1 Class-D

The Class-D PA can be sub-divided into two categories: the current-mode Class-D (CMCD) and the voltage-mode Class-D (VMCD). The CMCD PA is driven by a constant current source and incorporates a parallel resonant circuit in the output network, whereas the VMCD PA is driven by a constant voltage source and incorporates a series resonant circuit in the output network (Sommarek *et al.*, 2004:115; Berglund, Johansson & Lejon, 2006:93). Figure 39 and Figure 40 illustrate a VMCD and a CMCD PA respectively.

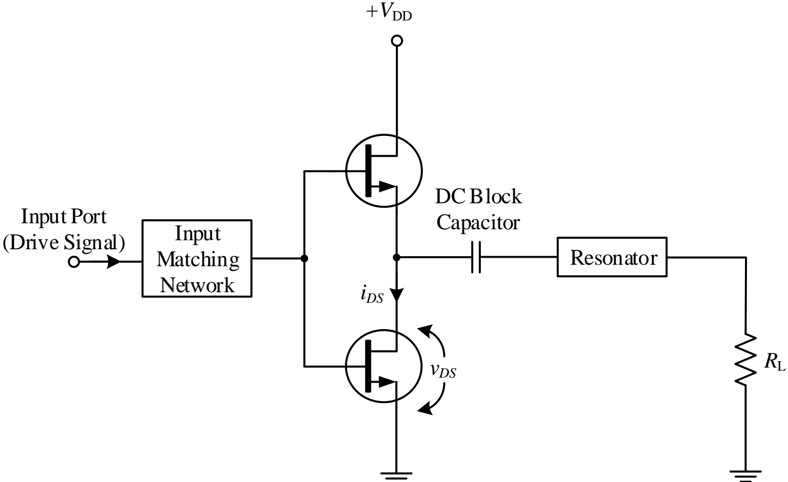


Figure 39: Circuit Topology of a VMCD PA (Adapted from Berglund, Johansson & Lejon, 2006:94)

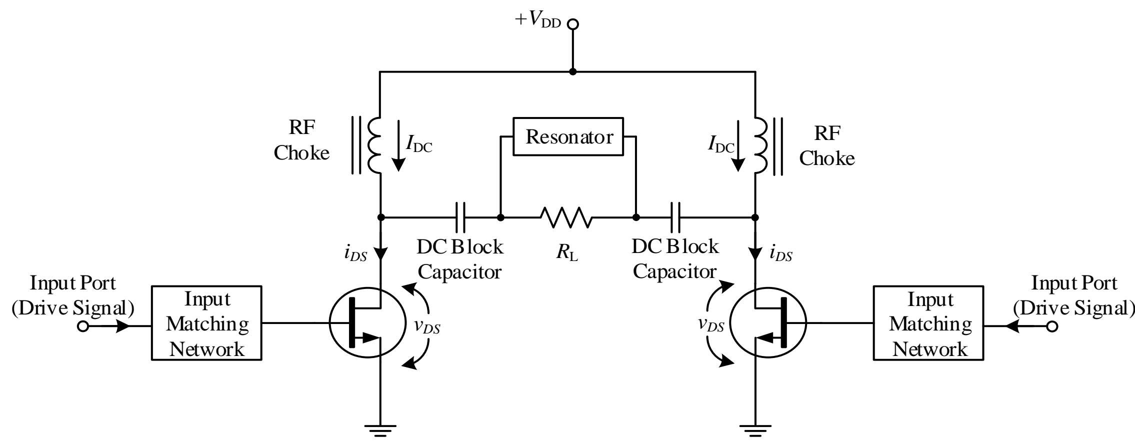


Figure 40: Circuit Topology of a CMCD PA (Adapted from Berglund, Johansson & Lejon, 2006:94)

Theoretically, it is possible for a Class-D amplifier to reach a *PE* of 100% because the drain voltage and current waveforms do not overlap as shown in Figure 41. This implies that zero power is dissipated in the active device, hence maximising the *PE.*

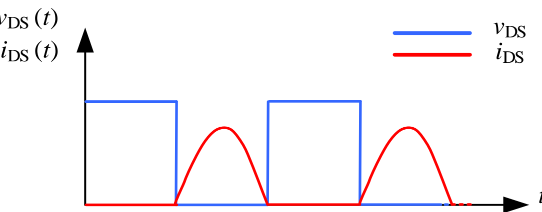


Figure 41: The Drain Voltage and Current Waveforms of a VM Class-D Amplifier (Adapted from Prodanov & Banu, 2007:60)

The major disadvantage of the VMCD PA is that the capacitance present between the drain and source as well as the speed at which the transistors switch severely limit the highest frequency at which the amplifier can operate and thereby degrade the *PE* at VHF and above (Berglund, Johansson & Lejon, 2006:93).

4.7.1.2 Class-E

The Class-E PA is a combination of a switching and a Class-AB PA (Berglund, Johansson & Lejon, 2006:93). The Class-E PA is categorised as an amplifier which switches on and off at a certain predefined frequency and the specifically shaped drain voltage and current waveforms do not overlap at any point in time. This trait of the Class-E PA facilitates a high *PE* since much less power is dissipated in the active device (Grebennikov, 2002:64). Wave-shaping is achieved by a series resonant circuit which is coupled between the drain and the load of the amplifier, as shown in Figure 42.

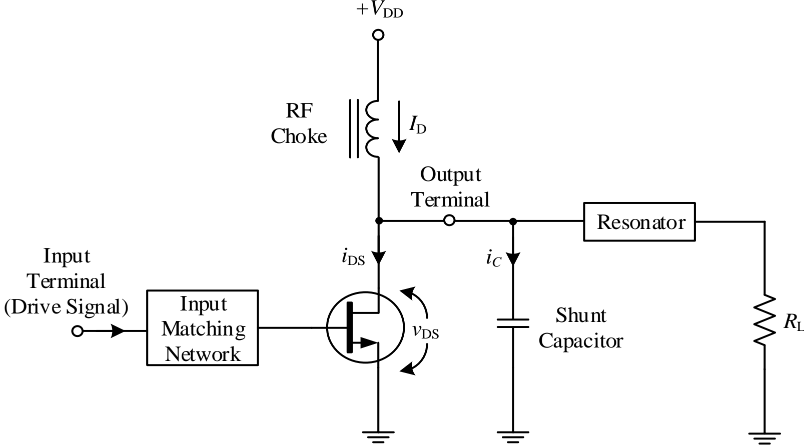


Figure 42: Circuit Topology of a CM Class-E PA (Adapted from Berglund, Johansson & Lejon, 2006:95)

The capacitor connected between the drain and ground, as depicted in Figure 42, has the important function of absorbing the parasitic capacitance present across the drain-source terminals of the transistor. The resonator is responsible for performing the wave-shaping function (Berglund, Johansson & Lejon, 2006:95). There is no overlap of v_{DS} and i_{DS} since $(v_{DS})(i_{DS}) = 0$ at all times as illustrated by the time-domain representations of the drain voltage and current waveforms in Figure 43.

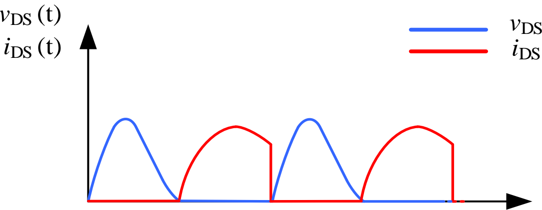


Figure 43: The Drain Voltage and Current Waveforms of a Class-E Amplifier (Adapted from Hashjani, 1997:56)

Ideally, when the active device switches into conduction, v_{DS} reduces to zero and i_{DS} increases. There is no overlap of v_{DS} and i_{DS} as illustrated in Figure 43. This absence of overlap implies no loss of power due to dissipation in the active device, hence a possible *PE* of 100% (Grebennikov, 2002:68-69).

An additional advantage of incorporating the drain-source capacitance at the output port is the minimising of the loss of power due to the shunt capacitor being charged and discharged, hence improving the *PE* (Hashjani, 1997:13).

In Class-E PAs v_{DS} (peak) can extend to $3V_{DC}$, thus the active device must be able to handle greater breakdown voltages (Kizilbey, Palamutcuogullari & Yarman, 2013:1).

This drain-source capacitance and the DC supply, V_{DD}, according to Mader *et al.*, (1998:1393) limit the maximum frequency of operation of a Class-E PA. This maximum frequency of operation is given by:

$$f_{max} = \frac{I_{DS}}{2\pi^2 C_s V_{DD}} \quad \text{Hz} \tag{4.1}$$

where, I_{DS} is the drain-source current

An increase in V_{DD} or the value of the drain-source capacitance, C_S, will result in a decrease of the maximum operating frequency.

4.7.2 Current Mode Amplifiers

The categorisation of current-mode amplifiers is based on the load terminations presented to the active device at harmonic frequencies. Also, these terminating load impedances perform the wave-shaping at the drain terminal which improves both output power and *PE*(Colantonio, Giannini & Limiti, 2009:24).

4.7.2.1 Class-F and Class-F^{-1}

The Class-F PA is a combination of a Class-B PA and a switching amplifier (Berglund, Johansson & Lejon, 2006: 94). The Class-F PA incorporates multiple resonators to purposely shape the voltage waveform to be rectangular and thereby manipulating the harmonic content thereof. By driving the transistor into saturation results in a half sinusoidal drain current waveform which also manipulates the harmonic content of the signal at the drain terminal (Jee *et al.*, 2012:89).

This is achieved by implementing an output network which presents the appropriate impedances at the fundamental frequency and multiples thereof to the drain terminal. This will ensure that the drain voltage waveform is a square-wave and will thus include the fundamental and all odd harmonic components. The half-sinusoid drain current waveform will include the fundamental component and all even harmonic components. (Cui *et al.*, 2018:2). These waveforms are shown in Figure 45.

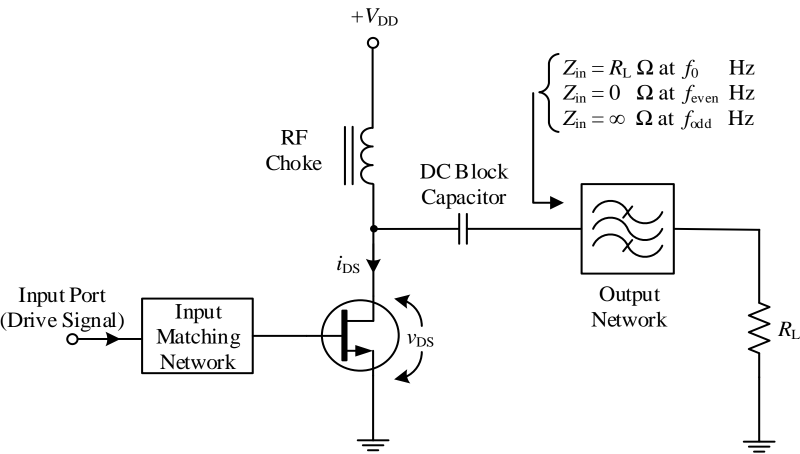


Figure 44: Basic Class-F PA topology (Adapted from Berglund *et al.*, 2006: 94)

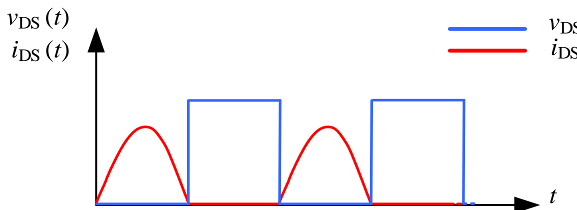


Figure 45: The Drain Voltage and Current Waveforms of an Ideal Class-F Amplifier (Adapted from Raab, 1997:2007)

In the Class-F^{-1} PA, the shapes of the drain waveforms are reversed with respect to those in a Class-F PA. That is, the drain current waveform is a square-wave whereas the drain voltage waveform is a half sine-wave. Thus, the drain current waveform will contain the fundamental component and all odd harmonics, and the drain voltage waveform will contain the fundamental component and all even harmonic components (Cui *et al.*, 2018:2). These waveforms are achieved by presenting the appropriate impedance to the drain terminal at the fundamental frequency and harmonics thereof.

Assuming an ideal scenario, that is, there is perfect wave-shaping by the output network which will ensure an infinite number of even and odd harmonic components are present at the drain terminal of the active device, then there will be no overlap between these voltage and current waveforms, hence a *PE* of 100% is achievable (Cui *et al.*, 2018:2).

4.8 Comparison of Different Classes of PAs

Amplifier Class	Frequency (GHz)	PAE (%)	Output Power (W)	Transistor Technology	Reference
A	2.142	25	33 dBm	GaAs HBT	ZACUBE-2
AB	3.4-3.7	59	38 dBm	GaN HEMT	(Alqadami *et al.*, 2017)
C	4	62	50.41W	GaN HEMT	(Yamasaki *et al.*, 2010)
D	1	60	41.14 W	LDMOS FET	(Lawrence. Long, 2003)
E	1.5-3.8	62	27 dBm	GaAs PHMET	(Lin and Chang, 2010)
F	2	80.1	40.7 dBm	GaN HEMT	(Hwang, *et al*., 2013:1-3)
F^{-1}	3.5	78	40.79 W	GaN HEMT	(Saad *et al.*, 2010)

Table 4: Comparison of PAs

4.9 Conclusion

Modern PAs mostly fall into the class of operational PAs, however, they are mostly still biased according to the biasing class of operation. Operational mode PAs are a combination of the bias class and the operational class. The quiescent point of the bias class and the load termination of operational mode jointly forms the operational class. For example, Class-F/F^{-1} are biased at Class-B cut-off, yet they are operational in Class-F/F^{-1} modes. Compared to three decades ago, operational class amplifiers were not as popular and traditional bias class PAs were used, such as Class-A, B, and C. As time has gone by an effort to improve efficiency in PAs has led to the design and implementation of Class-D, Class-E, and Class-F PAs.

Chapter 5

Class-F PA

5.1 Introduction

Numerous classes of PAs have been researched and subsequent design techniques developed to achieve a *PE* of 100%. The focus in this chapter is on the Class-F PA and will describe in detail the operation thereof. Additionally, a new output network topology, which conforms to Class-F PA criteria will be presented.

5.2 Description of a Class-F PA Including Waveform Shaping

The Class-F PA has uniquely shaped waveforms for the drain voltage and the drain current which allow the achievement of 100 % *PE*. Both of these waveforms are purposely shaped into a half sine-wave and a square-wave, respectively. The half sine-wave is due to the Class-B biasing condition and the square-wave is due to the rich harmonic content of the drain voltage and current waveforms. The Class-F PA schematic diagram is illustrated in Figure 46.

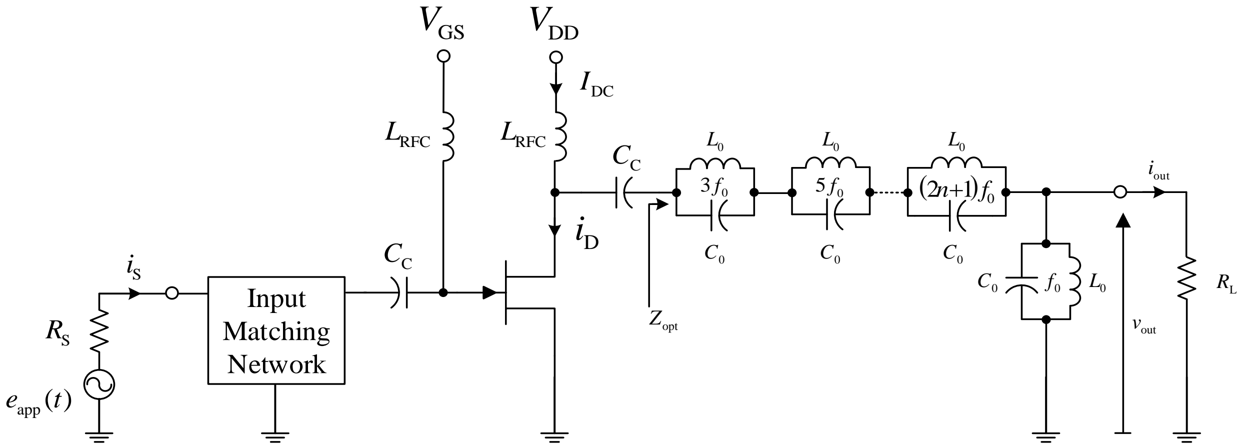


Figure 46: Schematic Diagram of Class-F PA (Adapted from Kazimierczuk, 2008:306)

Figure 47 illustrates the waveform shapes of the drain current and voltage for an ideal Class-F PA.

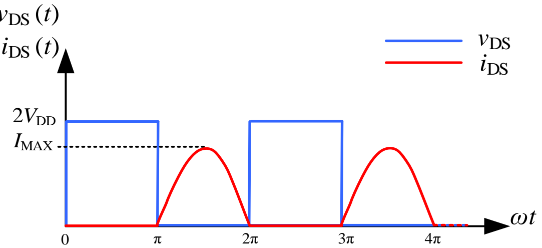


Figure 47: Ideal Waveforms of a Class-F PA

These ideal waveforms for $0 \le \omega t \le 2\pi$ are given by:

$$i_{DS}(\omega t) = \begin{cases} 0 & , \ 0 \le \omega t \le \pi \\ I_{MAX} \sin(\omega t) & , \ \pi \le \omega t \le 2\pi \end{cases} \qquad \text{A} \tag{5.1}$$

and

$$v_{DS}(\omega t) = \begin{cases} 2V_{DD} & , \ 0 \le \omega t \le \pi \\ 0 & , \ \pi \le \omega t \le 2\pi \end{cases} \qquad \text{V} \tag{5.2}$$

It is apparent from Figure 47 and from equations (5.1) and (5.2) that $v_{DS}(\omega t)$ and $i_{DS}(\omega t)$ do not overlap, which implies that the power dissipated in the active device is zero, and thus the first necessary condition for achieving a maximum *PE* of 100% in equation (3.26) is satisfied.

The Fourier expression for the drain current is given by:

$$i_{DS}(\omega t) = \sum_{n=0}^{\infty} I_n \cos(n\omega t) \qquad \text{A} \tag{5.3}$$

where the coefficients of the basis function cos($n\omega t$) are given (Colantonio, Giannini & Limiti, 2009:269), for all values of n, by:

$$I_n = \begin{cases} \dfrac{I_{\text{MAX}}}{\pi} & , \ n = 0 \\ \dfrac{I_{\text{MAX}}}{2} & , \ n = 1 \\ \dfrac{2I_{\text{MAX}}}{\pi} \dfrac{(-1)^{\frac{n}{2}+1}}{(-1+n^2)} & , \ n \text{ even} \\ 0 & , \ n \text{ odd} \end{cases} \quad \text{A} \tag{5.4}$$

The spectral components of the drain current are shown in Figure 48.

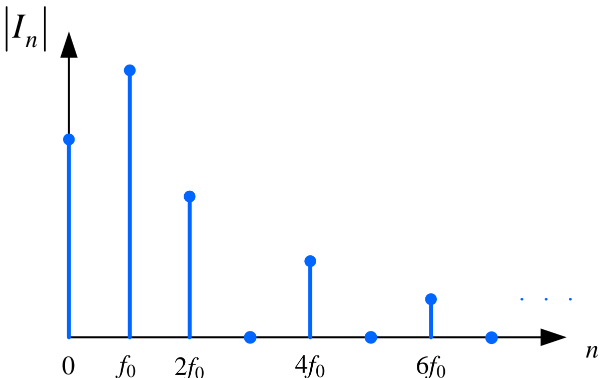


Figure 48: Spectral Content of $|I_n|$

The Fourier expression for the drain voltage is given by:

$$v_{\text{DS}}(\omega t) = \sum_{n=0}^{\infty} V_n \sin(n\omega t) \quad \text{V} \tag{5.5}$$

where the coefficients of the basis function sin($n\omega t$) are given, for all values of n, by:

$$V_n = \begin{cases} V_{\text{DD}} & , \ n = 0 \\ -\dfrac{4.V_{\text{DD}}}{\pi} & , \ n = 1 \\ 0 & , \ n \text{ even} \\ \dfrac{4.V_{\text{DD}}}{\pi} \dfrac{(-1)^{\frac{1+n}{2}}}{n} & , \ n \text{ odd} \end{cases} \qquad \text{V} \qquad (5.6)$$

The spectral components of the drain voltage are shown in Figure 49.

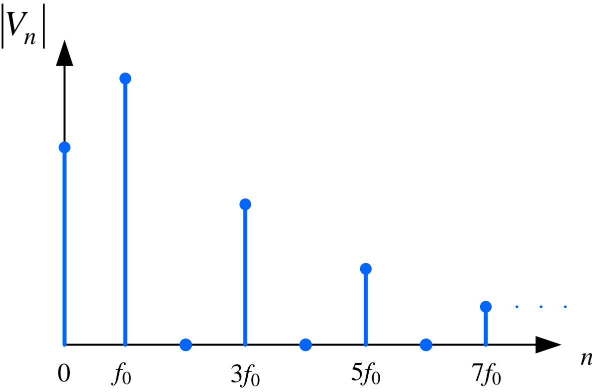


Figure 49: Spectral Content of $|V_n|$

Analysis of equations (5.4) and (5.6) reveal that the current waveform consists only of even harmonic components whereas the voltage waveform comprises only odd harmonics. However, both voltage and current waveforms have the same fundamental frequency. For maximum *PE* only the fundamental components of both current and voltage waveforms must be dissipated in the load, thus the second necessary condition for achieving a maximum *PE* of 100% in equation (3.26) is satisfied.

The magnitude of the drain current at the fundamental frequency is expressed as:

$$|I_1| = \frac{I_{\text{MAX}}}{2} \qquad \text{A} \qquad (5.7)$$

and the magnitude of the drain voltage at the fundamental frequency is expressed as:

$$\left|V_1\right| = \frac{4V_{\mathrm{DD}}}{\pi} \qquad \mathrm{V} \tag{5.8}$$

The output power at the fundamental frequency is expressed as:

$$P_{f_0} = \frac{1}{2}V_1 \cdot I_1 = \frac{1}{2} \cdot \frac{4V_{\mathrm{DD}}}{\pi} \cdot \frac{I_{\mathrm{MAX}}}{2} = \frac{V_{\mathrm{DD}} I_{\mathrm{MAX}}}{\pi} \qquad \mathrm{W} \tag{5.9}$$

The DC power of a Class-B biased device is given by (Colantonio, Giannini & Limiti, 2009:271):

$$P_{\mathrm{DD}} = V_{\mathrm{DD}} \cdot I_{\mathrm{DC}} = \frac{V_{\mathrm{DD}} I_{\mathrm{MAX}}}{\pi} \qquad \mathrm{W} \tag{5.10}$$

Consequently, the theoretical *PE* is expressed as:

$$PE = \frac{P_{f_0}}{P_{\mathrm{DC}}} \cdot 100\% = \frac{V_{\mathrm{DD}} I_{\mathrm{MAX}}}{\pi} \cdot \frac{\pi}{V_{\mathrm{DD}} I_{\mathrm{MAX}}} \cdot 100\% = 100\% \tag{5.11}$$

The impedance presented by the load network to the drain of the active device determines the magnitudes of the drain current and voltage, as well as the shape of these waveforms. This impedance, using Ohm's law, is given by:

$$Z_n = \begin{cases} \frac{8}{\pi} \cdot \frac{V_{\mathrm{DD}}}{I_{\mathrm{MAX}}} = R_{\mathrm{opt}} & , \; n = 1 \\ 0 & , \; n \text{ even} \\ \infty & , \; n \text{ odd} \end{cases} \qquad \Omega \tag{5.12}$$

To obtain a maximum *PE*, the output port (drain) of the active device must be terminated in an impedance value of $Z_1 = R_{\mathrm{opt}}\ \Omega$ for $n = 1$, $Z_n = 0\ \Omega$ for $n = \text{even}$ and $Z_n = \infty\ \Omega$ for $n = \text{odd}$, as shown in equation (5.12). These optimum impedance values will ensure that the waveforms are a square-wave drain voltage and half sine-wave drain current.

Colantonio, Giannini & Limiti, (2009:184) suggest that the control of the higher-order harmonic components is not justified, since a minimal improvement in *PE* is obtained at the cost of a significant increase in circuit complexity. In practice, only the amplitude of the harmonic components f_n where $n = 2, 3$ are reduced, that is, filtered out, resulting in a high *PE* being achieved, a philosophy which will be incorporated in the design of this class-F PA.

5.3 Limitations Effecting Maximum *PE*

The efficiency of a PA is typically limited by the effect of the parasitic components in an active device. Such components include the total output capacitance which predominantly consists of the drain-source capacitance (C_{DS}). Also, the bond wire and the lead inductance of the transistor package (L_{out}) significantly limit the achievement of a maximum *PE*. The parasitic components alter the relationship between the phase of the drain current and voltage waveforms and which must be eliminated to minimise the limitations imposed on the *PE* of the PA (Grebennikov, 2011:70-72).

If possible, C_{DS} of the transistor should be incorporated into the load network as one of the capacitive elements, thus minimising its influence on the *PE*. Moreover, at high harmonic frequencies, the impedance of C_{DS} will be lower, thereby shorting to ground the higher harmonic components, thus eliminating the necessity for the removal thereof.

If possible, the parasitic lead inductance of the bond wire should also be absorbed into the load network. That is, the value of this inductor can form part of the first series component in the load network. This can be achieved by selecting the first series component of the load network to be an inductive transmission line section.

5.4 Transmission Line Theory

To complement the detailed explanations of the functioning of the load network, a brief review of transmission line theory will now be presented.

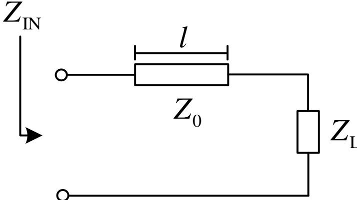


Figure 50: Loaded Transmission Line Section (Adapted from Pozar, 2012:57)

From transmission line theory the impedance transformation equation is expressed as:

$$Z(d) = \left[\frac{Z_L + Z_0 \tanh(\gamma d)}{Z_0 + Z_L \tanh(\gamma d)} \right] Z_0 \qquad \Omega \tag{5.13}$$

where, $\gamma =$ propagation constant of the transmission line
d = distance from Z_L to the input port of transmission line
Z_0 = characteristic impedance of transmission line
Z_L = load impedance of transmission line

When $d = l$ meters then equation (5.13) provides the impedance at the input port of the transmission line, that is Z_{IN}.

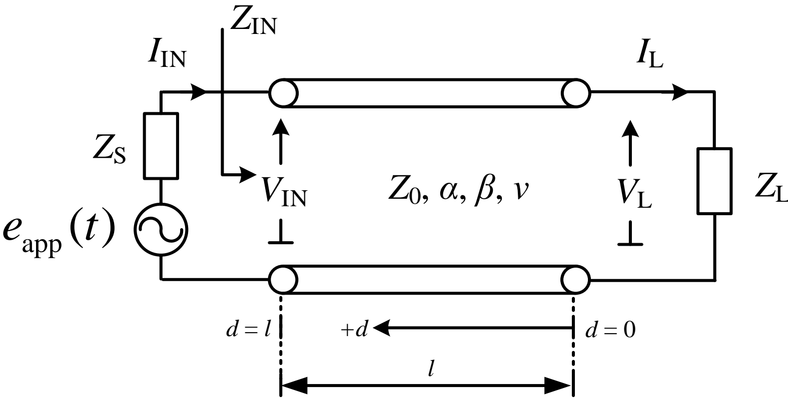


Figure 51: Transmission Line Parameters (Adapted from Pozar, 2012:57)

The propagation constant is given by:

$$\gamma = \alpha + j\beta \qquad \text{per unit length} \tag{5.14}$$

where, α : $\frac{\text{Nepers}}{m}$

β : $\frac{2\pi}{\lambda_g}$

l : the physical length in meters

βl : the electrical length in radians

If the transmission line is considered lossless, then $\alpha = 0$ Nepers, and equation (5.14) reduces to:

$$\gamma\big|_{\text{Lossless}} = j\beta \qquad , \frac{\text{Nepers}}{m} \tag{5.15}$$

Equation (5.13) then simplifies to (Pozar, 2012:59):

$$Z_{\text{IN}}(d) = \left[\frac{Z_{\text{L}} + jZ_0 \tan(\beta l)}{Z_0 + jZ_{\text{L}} \tan(\beta l)}\right] Z_0 \qquad \Omega \tag{5.16}$$

Since the transmission lines used in this load network are short enough to be considered lossless, equation (5.16) will be used extensively to explain the behaviour and functionality of the load network. This will be presented in the following section.

5.5 WHIP Network for a Class-F PA

An in-depth literature search revealed that numerous topologies for the load network have been developed for PAs to maximise the *PE*. This literature study also revealed that the load network utilised in these PAs perform four very important operational functions, namely that of:

- **W**ave-shaping
- **H**armonic suppression
- **I**mpedance transformation
- **P**arasitic component absorption

The load network proposed in the following section will hereinafter be referred to as a WHIP network, the name of which is based on these operational functions.

5.5.1 The Proposed WHIP Network

The proposed WHIP network topology, that will be implemented in this Class-F PA, is shown in Figure 52.

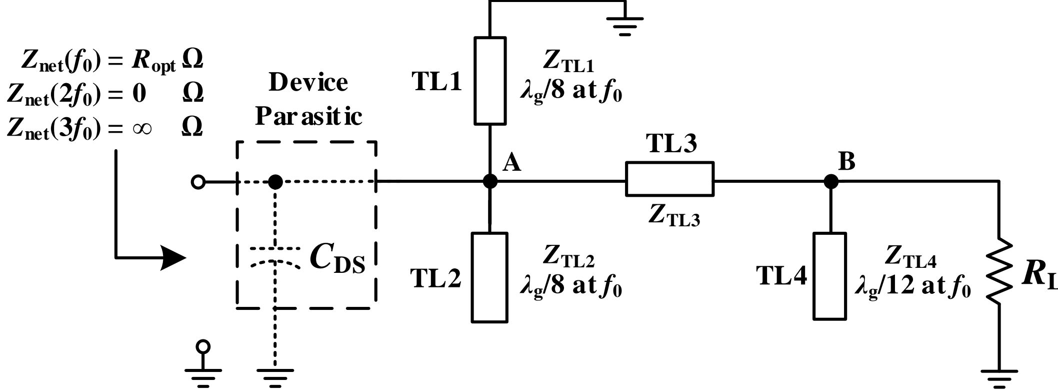


Figure 52: The Proposed WHIP Network

The WHIP network presented in Figure 52 is based on the network topology presented by (Grebennikov, 2000) where the $\frac{\lambda_g}{4}$ transmission line has been replaced by two $\frac{\lambda_g}{8}$ transmission line sections (TL1 and TL2), one with an open-circuit load and the other with a short circuit load.

This proposal is based on the research performed by Thian, Barakat & Fusco, (2015:661-662) who demonstrated that these open- and short-circuit $\frac{\lambda_g}{8}$ stubs will provide a much lower impedance value at their input ports to that of a short-circuit $\frac{\lambda_g}{4}$ stub. This lower impedance value significantly improves the harmonic filtering function of the WHIP network, hence suggesting the possibility of an improved *PE*. Since the physical length of a $\frac{\lambda_g}{8}$ stub is half that of a $\frac{\lambda_g}{4}$ stub, a lower impedance value will be presented at its input port and hence an improved short circuit termination. The actual impedance presented by the input port of a $\frac{\lambda_g}{8}$ stub section is half that of the $\frac{\lambda_g}{4}$ stub section and is mathematically verified in Appendix A.

The detailed functionality of the proposed WHIP network will now be presented:

Referring to Figure 52 and at the fundamental frequency (f_0), transmission lines TL1 and TL2 have physical lengths of $\frac{\lambda_g}{8}$ meter and their combined physical topology forms an open-circuit at node A. Hence, the WHIP network is transformed into the circuit topology illustrated in Figure 53.

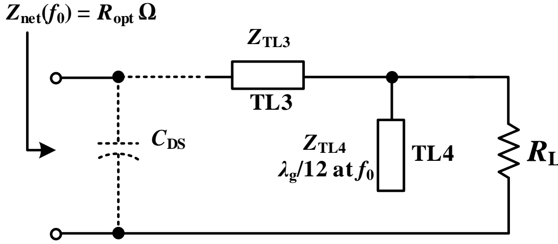


Figure 53: Equivalent WHIP Network at f_0

One of the functions of the WHIP network is to convert the load resistance, R_L, into the optimum value of resistance, R_{opt}, which will ensure maximum power is dissipated in the load. This impedance transformation is optimised by adjusting the characteristic impedance and the physical length of TL3, as well as the characteristic impedance of TL4 (Schmelzer & Long, 2006). The physical length of TL3 was determined from the equation for its electrical length given by (Grebennikov, 2000):773:

$$\theta_{TL3} = \frac{1}{3}\tan^{-1}\left(\frac{1}{3Z_0\omega_0 C_{DS}}\right) + \frac{\pi}{6} \quad \text{radians} \tag{5.17}$$

Referring to Figure 52, and at $2f_0$, the physical lengths of TL1 and TL2 will be $\frac{\lambda_g}{4}$ meters long and their combined physical topology presents an ideal short circuit at node A. The resulting equivalent circuit of the WHIP network at $2f_0$, is illustrated in Figure 54.

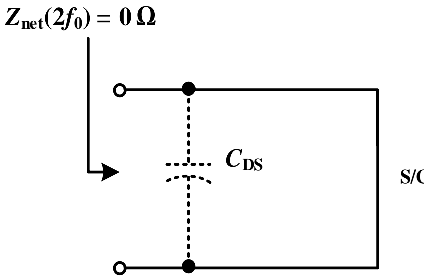


Figure 54: WHIP Network Equivalent Circuit at the Second Harmonic Frequency

Referring to Figure 52 at $3f_0$, transmission lines TL1 and TL2 have physical lengths of $\frac{3\lambda_g}{8}$ meters and their combined physical topology forms an open circuit at node A. The physical length of transmission line TL4 is $\frac{\lambda_g}{4}$ meters, and will transform the open-circuit load of TL4 to a short circuit at node B. The physical length of transmission line TL3 is selected such that it behaves as an inductive element and with the parasitic component C_{DS} forms a parallel circuit, resonant at $3f_0$, with the subsequent, very high impedance at its input port. The equivalent circuit at $3f_0$ is illustrated in Figure 55.

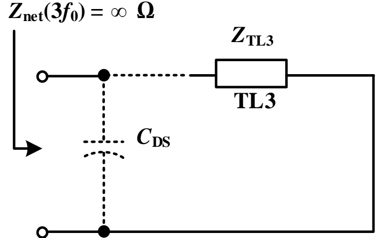


Figure 55: WHIP Network Equivalent Circuit at the Third Harmonic Frequency

At the fundamental frequency, TL3 can be lengthened by $\frac{\lambda_g}{6}$ meters (electrical length of 60°) to provide fundamental matching versatility. At $3f_0$ a multiple of $\frac{\lambda_g}{2}$ meters does not influence the harmonic termination as detailed in equation (5.17).

5.6 Conclusion

In this chapter, a mathematical analysis of the required performance of the WHIP network was presented and supported with appropriate time-domain representations of the drain-source waveforms of the active device.

The main parasitic component of the amplifying device which limits the attainment of a maximum *PE* was presented. It is imperative to incorporate the parasitic component into the functionality of the WHIP network to achieve a higher *PE*. The topology and functionality of a wave-shaping, harmonic suppression, impedance transformation and parasitic absorbing network were presented. It was clearly explained that by using various lengths of transmission line sections, that the optimal terminating impedances required for Class-F operation were achieved. The detailed theoretical analysis of the proposed WHIP network indicates that it will suffice in providing the optimal impedance terminations for Class-F operation.

Chapter 6

Design of a Class-F PA with a WHIP Network

6.1 Introduction

The detailed design of a Class-F PA incorporating the WHIP network as introduced in section 5.5 will now be presented. This section will include the selection of a suitable active device, the determination of the DC bias point using the load-line technique, the design of the WHIP network, the design of a matching network at the input port of the active device and finally perform a stability analysis of the complete PA using the STAN software tool provided by AMCAD Engineering. The electronic design automation (EDA) software used throughout this process is Keysight's Advanced Design System (ADS).

6.2 Transistor Technology and Device Selection

The transistor technology chosen for this PA was the Gallium-Nitride CGH40010F FET available from Cree. The CGH40010F FET is one of the most popular and widely used transistors in modern PA design. The device was selected because it has well-defined and mature linear and non-linear simulation models which allow for valid conceptual circuit design. Also, this device has delivered excellent performance results in numerous PA circuits and was readily available. The specifications of the active device are as detailed in the device datasheet in Appendix B.

Figure 56: The CGH40010F GaN Device by Cree

6.3 DC Operation Simulations

For a PA to conform to Class-F operational conditions it must be biased in the classical Class-B mode, which requires that the DC bias point should be selected at cut-off. Figure 57 and Figure 58 illustrate the respective IV plots and the equivalent DC circuit. The device was biased according to the recommended gate-source voltage, $V_{GS} = -2.680$ V, a drain current of $I_D = 0.248$ A, and a drain-source voltage of $V_{DS} = 28$V. The transconductance curve was determined to verify the value of transconductance at the selected bias conditions.

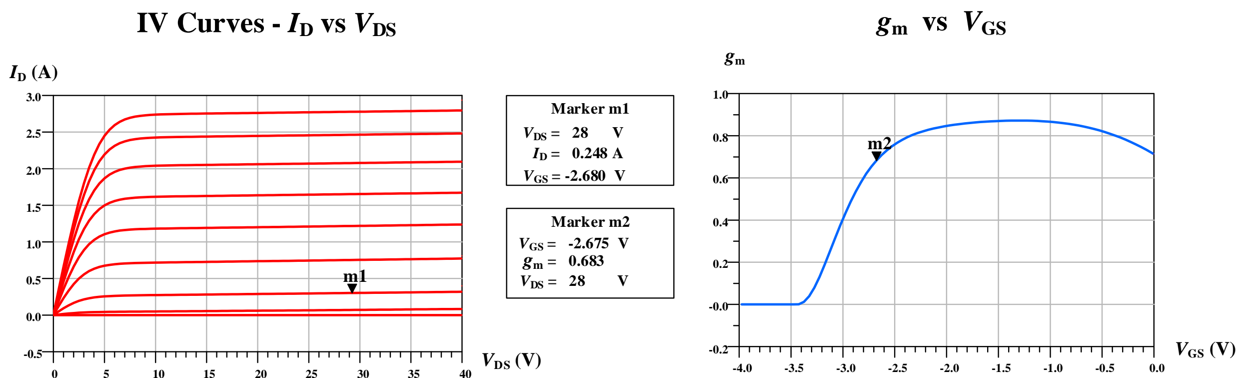


Figure 57: DC Operating Point and Transconductance curve (g_m)

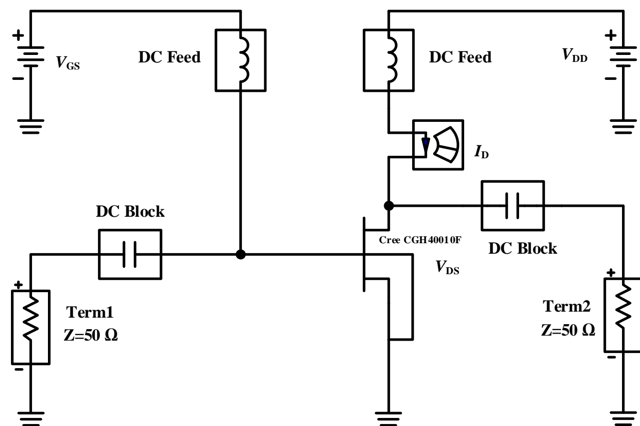


Figure 58: DC Bias Circuit

6.4 Design of WHIP Network

The WHIP network as proposed in section 5.5.1 was designed to operate at a frequency of 2.2 GHz. The parasitic component of the CGH40010F GaN active device was obtained from the datasheet as C_{DS} = 1.31pF. The Z_0 of transmission lines TL1 and TL2 were selected as 70 Ω to achieve a minimum impedance at their input ports at $2f_0$. The characteristic impedance for TL3 and TL4 was selected as 50 Ω. Equation (5.17) was used to calculate the electrical length of TL3, and the electrical lengths of TL1, TL2 and TL4 were calculated using:

$$EL(\theta_{TL}) = PL(\lambda_g) \times \frac{2\pi}{\lambda_g} \quad \text{radians} \tag{6.1}$$

where, EL= electrical length in radians

PL= physical length in terms of λ_g

Hence, $\theta_{TL1} = \theta_{TL2} = 45°$, $\theta_{TL3} = 66.245°$ and $\theta_{TL4} = 30°$.

The optimum resistance, R_{opt}, was calculated using the load-line technique and equation (5.12) to be 91.515 Ω. Variables Z_{TL3} and Z_{TL4} were adjusted (Schmelzer & Long, (2006)) to present a value of resistance as close to R_{opt} as possible. The equivalent network shown in Figure 53 was simulated in ADS with Z_{TL3} = 54.3 Ω and Z_{TL4} = 23 Ω and the input and output return losses, (*IRL* and *ORL*) are shown in Figure 59.

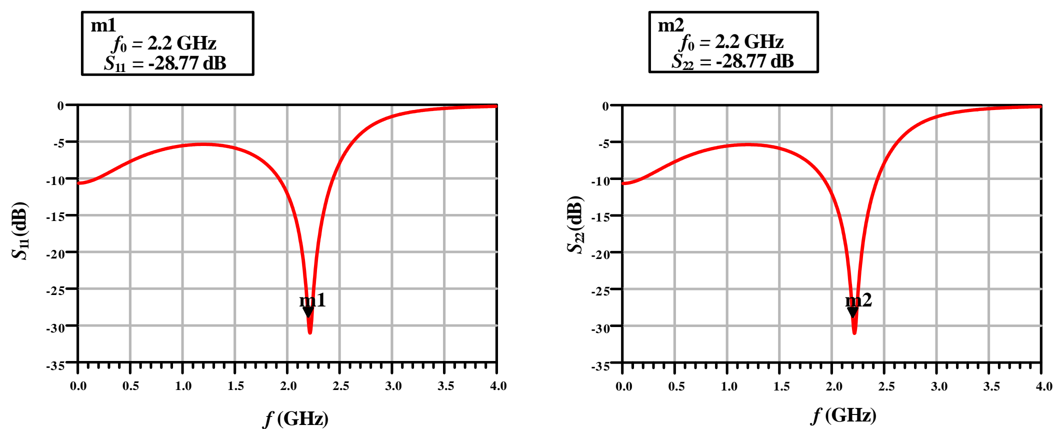


Figure 59: *IRL* and *ORL* of the Equivalent WHIP Network at f_0

The *IRL* (S_{11}(dB)) and *ORL* (S_{22}(dB)) of 28.767 dB each indicate correct impedance transformation at f_0.

The final WHIP network with the calculated electrical transmission line lengths is illustrated in Figure 60.

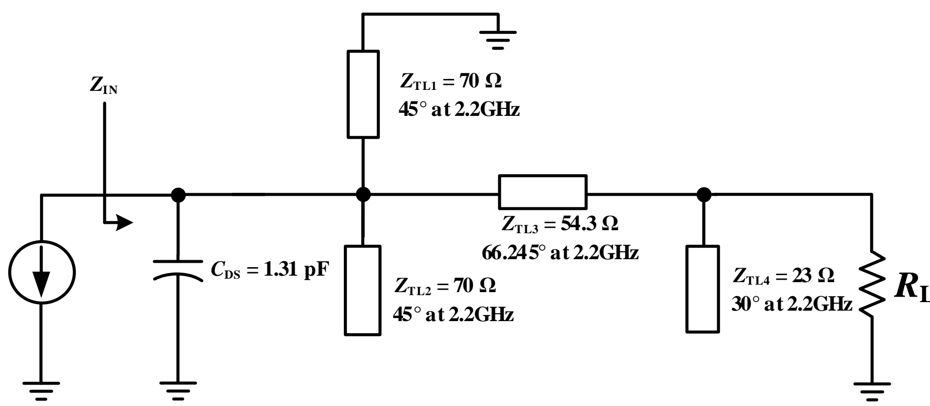


Figure 60: Final WHIP Network

The WHIP network in Figure 60 was simulated in ADS to verify harmonic suppression and impedance termination, the transfer function (S_{21} (dB)) of which is illustrated in Figure 63.

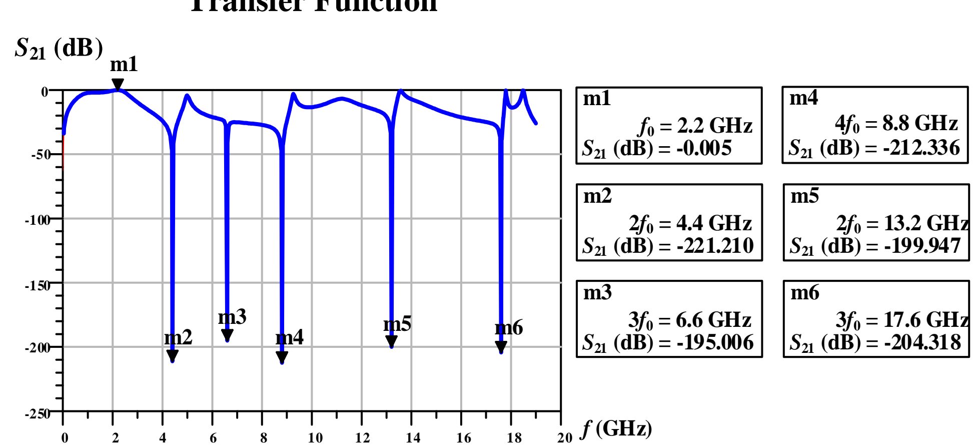


Figure 61: Transfer Function of WHIP Network

The marker m1 on the transfer function in Figure 61 indicates that at the fundamental frequency there is a minimal insertion loss of 0.005 dB. The first odd harmonic indicated by marker m3 is suppressed with an attenuation of 195 dB. The even harmonics represented by markers m2, m4, m5 and m6 are suppressed by 221.2 dB, 212.2 dB, 199.9 dB and 204.3 dB, respectively. These results indicate that the WHIP network is providing significant suppression of the harmonic components.

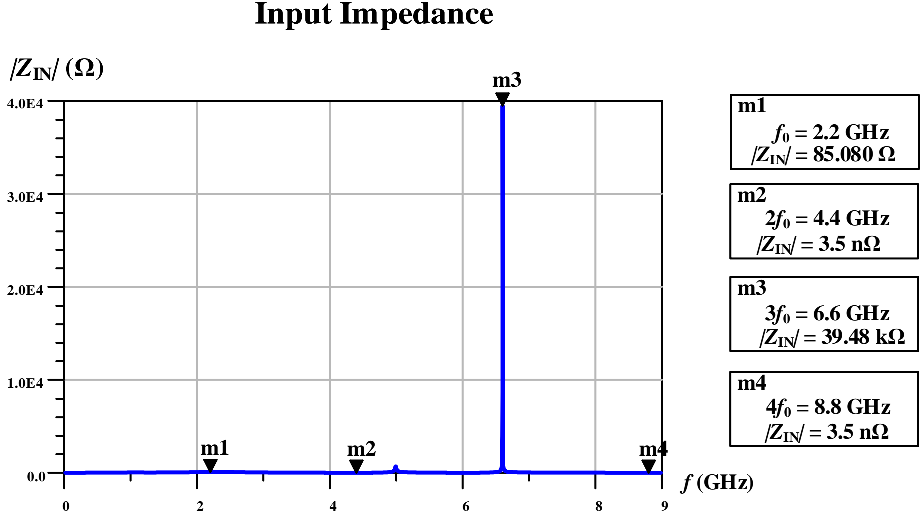


Figure 62: Impedance Presented by the WHIP Network

Considering Figure 62, the markers of the even harmonic components, that is markers m2 and m4, indicate that an extremely low impedance value of 3.5 nΩ, which can be considered as a short circuit, is presented at the input port of the WHIP network at these frequencies. Marker m3, which indicates the first odd harmonic frequency component, indicates that a relatively high impedance of 39.48 kΩ is presented at the input port of the WHIP network at this frequency. At the fundamental frequency, the WHIP Network is presenting an impedance of 85 Ω which is the closest compromised reached when tuning Z_{TL3}, θ_{TL3}, and Z_{TL4} (Schmelzer & Long, 2006:97) to obtain the desired optimum load resistance of 91.515 Ω. The results indicated in Figure 62 clearly show that the WHIP network satisfies the conditions in equation (5.12).

Considering Figure 63, at the fundamental frequency, that is marker m1, the magnitude of the input reflection coefficient is very close to zero indicating a maximum transfer coefficient of the WHIP network, and which coincides with marker m1 in Figure 61. Marker m2, which indicates the first

even harmonic component, shows a magnitude of the reflection coefficient of 1, indicating a minimum transfer coefficient of the WHIP network, and which coincides with marker m2 in Figure 61. Marker m3, which indicates the first odd harmonic component, shows a magnitude of reflection coefficient of 1, indicating a minimum transfer coefficient of the WHIP network, and which coincides with marker m3 in Figure 61.

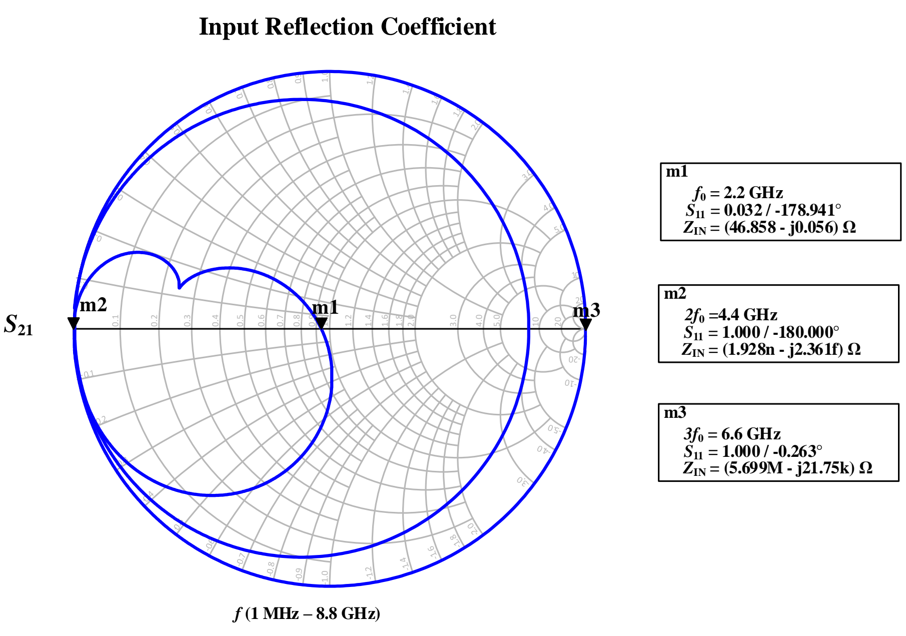


Figure 63: Harmonic Suppression and Termination

6.5 Design of Input Matching Network

For maximum power transfer, it is necessary to provide optimum matching on the input port of the active device. ADS was used to determine the gate-source impedance of the active device to enable a suitable matching network to be designed. Figure 64 depicts the simulated gate-source impedance of the active device, denoted Z_{IN}.

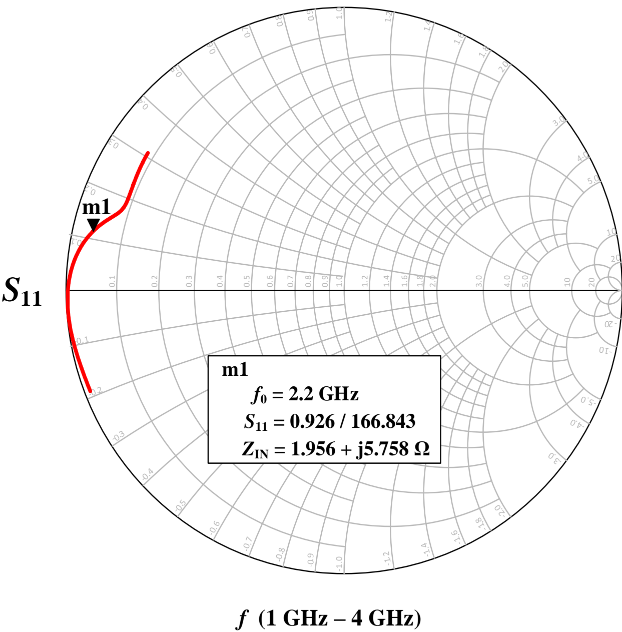


Figure 64: Simulated Gate-Source Impedance of Active Device Terminated in WHIP Network

A single stub microstrip matching network was designed to match the gate-source impedance of the active device to 50 Ω using a Smith chart. The transfer function (S_{21}(dB)) and the *IRL* (S_{11}(dB)) of the input matching network are illustrated in Figure 65. An *IRL* of just over 34 dB and a maximum forward transfer function were obtained at 2.2 GHz which indicates a reasonable degree of matching with minimal insertion loss.

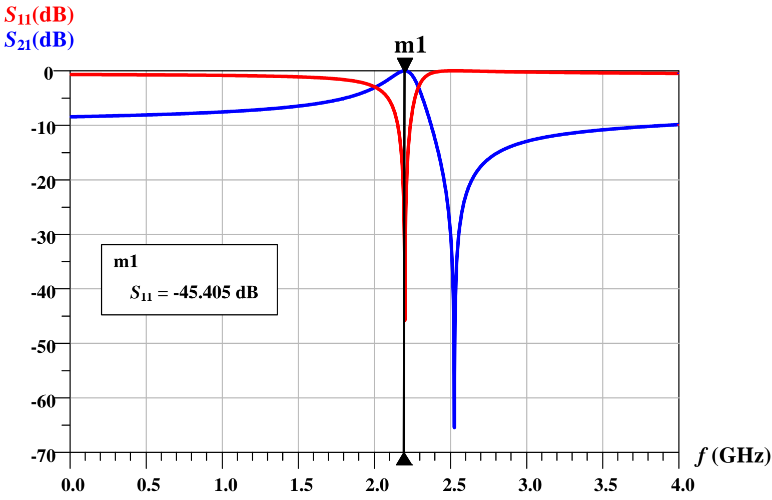


Figure 65: Performance of Input Matching Network

6.6 Simulated Performance of the Ideal PA Schematic

To validate the conceptual operation of the PA, harmonic balance simulations were performed in ADS on the circuit illustrated in Figure 66. The capacitors labelled C_c are utilised for RF coupling and DC blocking. The capacitors labelled C_{by} are utilised as bypass capacitors. The resistor R is implemented for stability of the PA (Grebennikov, 2011).

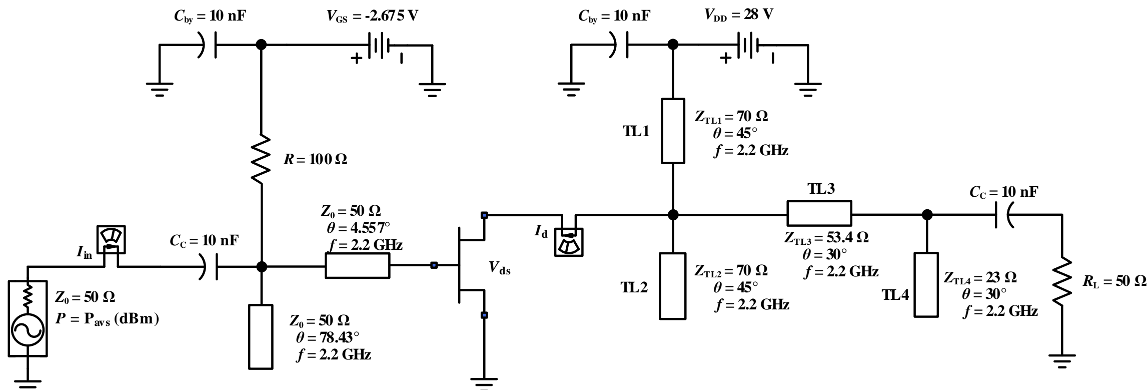


Figure 66: Initial Ideal Circuit of PA

Illustrations of $V_{DS}(t)$ and $I_{DS}(t)$ at an input power of 33dBm are shown in Figure 67.

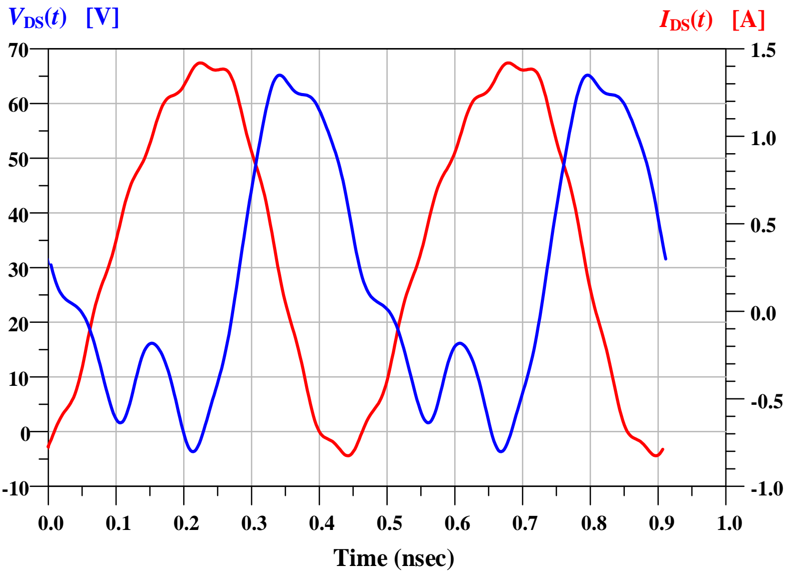


Figure 67: Simulated Drain Waveforms of Ideal PA Circuit

The simulated values for gain, P_{out}, PE and PAE are illustrated in Figure 68.

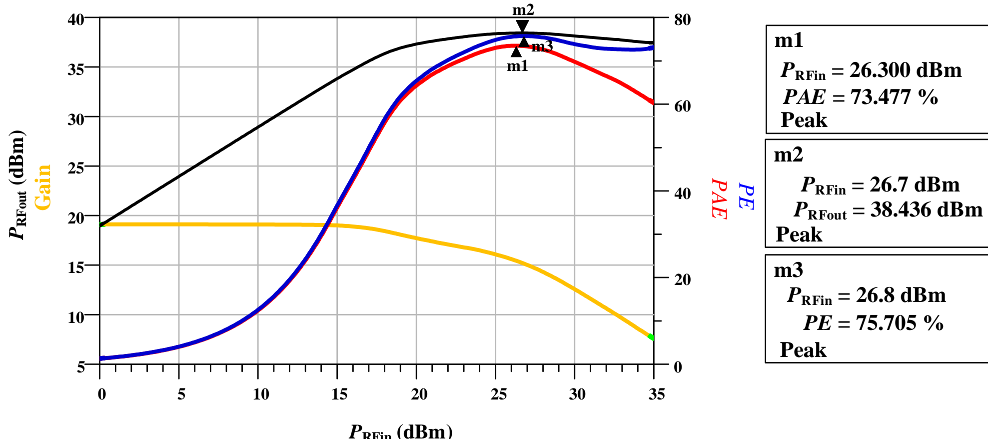


Figure 68: Simulated Values for Gain, P_{out}, PE and PAE

Initial simulations at f_0 resulted in a gain of approximately 15 dB, a maximum output power at of 38.435 dBm, a maximum PE of 75.705 % and a maximum PAE of 73.477 %. These initial simulated results validate the conceptual operation of this Class-F PA.

6.7 Stability

A two-port network might to oscillate in the presence of certain passive source and load terminations. It is important to incorporate a stability analysis in the design of a PA to ensure stable performance. The existence of feedback loops is predominantly the cause of unstable amplifiers and are formed due to the non-zero value of S_{12}. This non-zero value results in the creation of reflections and the higher gain from a PA results in higher power levels being reflected from the device load and can potentially cause the magnitude of S_{11} to exceed unity (Louw, 2015:22). A PA that does not oscillate regardless of the source and load terminations is said to be unconditionally stable. When an active device oscillates with certain terminations it is potentially unstable.

Stability performance of electronic devices is an extensive research area and is not covered in its entirety within the work of this thesis. An overview of stability performance will be presented related to linear and non-linear stability followed by appropriate simulations to validate the stability of this PA.

6.7.1 Stability Analysis of a Linear Network

Unconditional stability or potential instability of a linear two-port network is determined by the small signal S-parameters of the active device, and the terminations to this active device. Instability can be detected by determining the Rollet stability factor (K), the magnitude of the determinant of the S-parameters $|\Delta|$, and the Linville stability factor (μ). The satisfactory and necessary conditions for unconditional stability are:

$$K > 1 \quad \text{and} \quad |\Delta| < 1 \tag{6.2}$$

where,

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{6.3}$$

and,

$$|\Delta| = S_{11}S_{22} - S_{12}S_{21} \tag{6.4}$$

The Linville stability factor (μ) can be used as a standalone parameter for stability analysis of a linear network. The condition for unconditional stability is given by:

$$\mu = \frac{1-|S_{11}|^2}{|S_{22}-\Delta S_{11}^*|+|S_{12}S_{21}|} > 1 \qquad (6.5)$$

Stability analysis of a non-linear network by using equations (6.2) and (6.5) may result in unreliable parameters and as such cannot be used (Dellier, 2012:3).

6.7.2 Stability Analysis of a Non-linear Device

Techniques have been investigated and developed to analyse the stability of non-linear circuits such as PAs. AMCAD Engineering has developed a stability analysis (STAN) tool to analyse the stability of non-linear circuits and this STAN software was kindly made available for use in this work.

The STAN tool can detect oscillations such as parametric oscillations in PAs which could be related to the input drive signal. The STAN tool uses analysis of the frequency response of a PA to identify the pole/zero map and thereby the stability of the PA.

The setup for the analysis consists of determining a node within the PA circuit. According to (Dellier, 2012) any point can be selected as a node of analysis in a circuit which exhibits a simple and clear feedback structure.

Firstly, the frequency response of the PA must be obtained with regards to its large-signal regime. This is achieved by using ADS to perform a non-linear simulation.

Secondly, the frequency response needs to be identified to acquire the transfer function and its corresponding poles and zeros. This is achieved by using the STAN tool.

A multi-node analysis is then performed to analyse the stability of the PA and to determine the nature of any instability. The PA is stable if no poles are present on the right-hand side of the imaginary axis of the pole-zero plot.

The above-mentioned procedure is performed on this Class-F PA at an input power of 28.5 dBm where the frequency of the input signal is swept from 0 - 6 GHz. The corresponding pole-zero plot is shown in Figure 69 where the complex coordinates of the poles and zeros are plotted versus frequency.

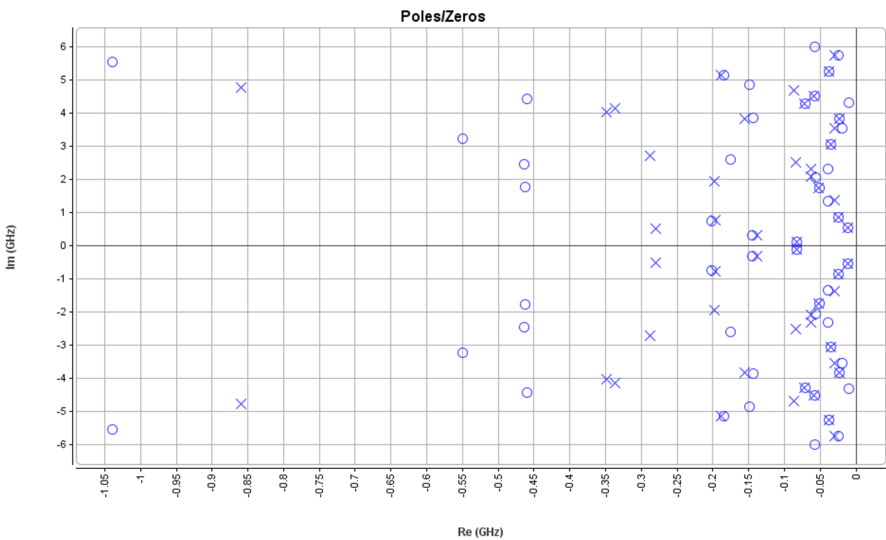


Figure 69: Complex Coordinates of the Pole-Zero Plot vs Frequency

Figure 69 shows the non-existence of poles on the right-hand side of the complex plane in the pole-zero map, hence the PA is considered stable under these simulated conditions.

The stability analysis of the PA is also checked for an input power level swept from 0 - 35 dBm. The corresponding complex coordinate plot of the poles and zeros is shown in Figure 70.

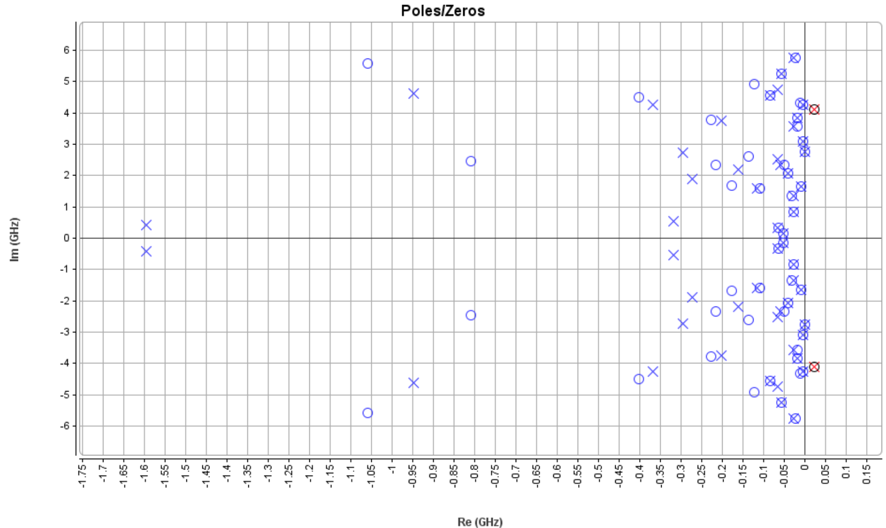


Figure 70: Complex Coordinates of the Pole-Zero Plot vs Frequency for a Swept Input Power

Figure 70 reveals the existence of two poles on the right-hand side of the complex plane at 4.1 GHz. The device can be made stable by increasing the value of the stabilising resistor connected to the gate of the active device (Dellier, 2012). This stabilising resistor was increased from 100 Ω to 110 Ω and another stability analysis conducted which resulted in the pole-zero plot shown in Figure 71.

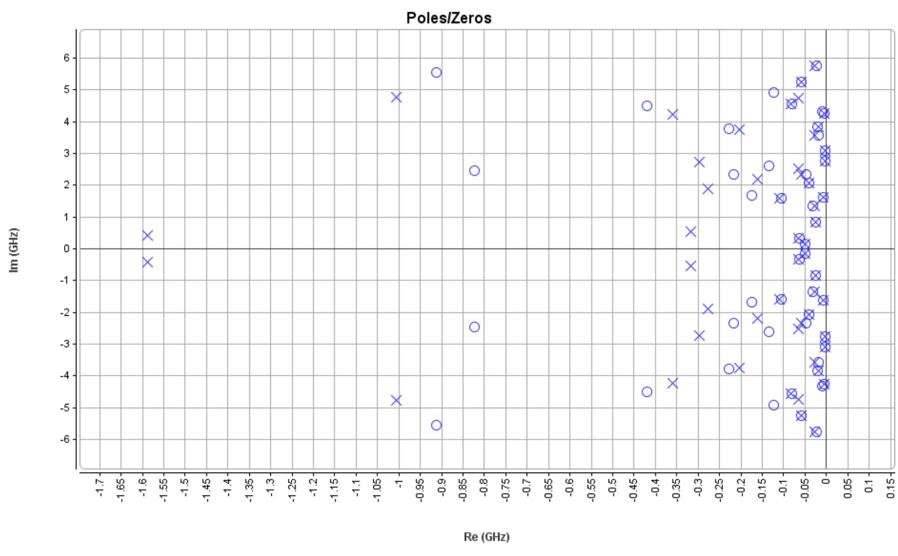


Figure 71: Pole-Zero Plot vs Frequency of PA with Increased Stability Resistor

Figure 71 reveals the non-existence of poles to the right-hand side of the complex plane, hence the PA is deemed stable from 0 - 6 GHz when the input power level is swept from 0 - 35 dBm.

6.8 PCB, Layout and Simulations

The simulations presented in section 6.6 were performed under ideal conditions and do not take into account the transmission line T- and cross-sections used to connect the actual transmission lines used in the PA. The actual physical dimensions of the transmission line sections in the PA were determined using the LineCalc tool provided in ADS. The physical layout incorporating these T- and cross-sections used to join the transmission line sections in the PA is shown in Figure 72.

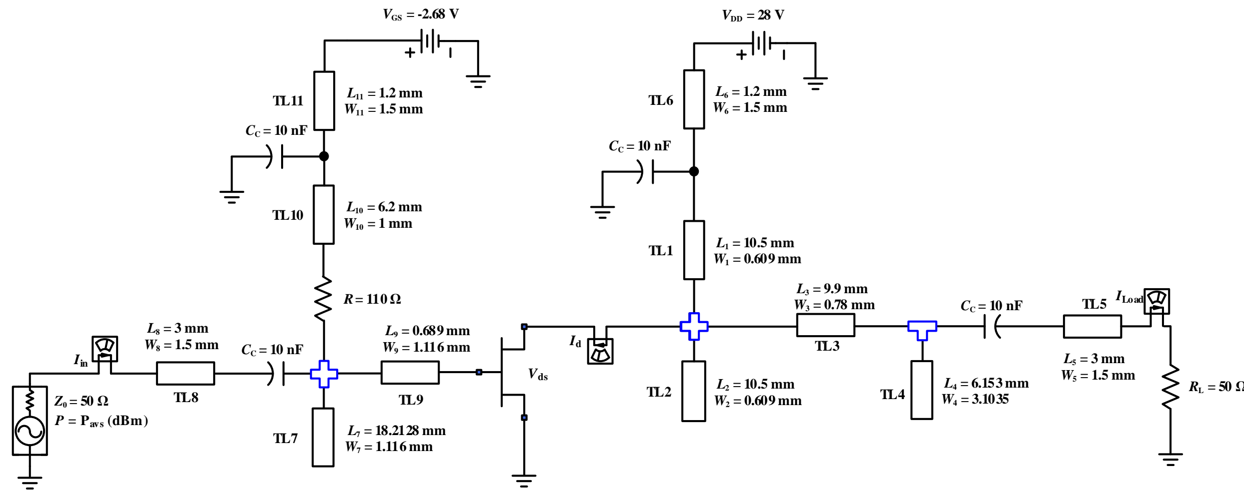


Figure 72: Final Schematic Diagram

The PCB for the PA was constructed using the layout tool provided in ADS and is shown in Figure 73. The substrate chosen for the PA was Rogers RO4003C with a thickness of 0.51 mm. The Momentum EM Simulator within ADS was used to characterise and generate an equivalent *S*-parameter model of the layout component and is shown in Figure 73.

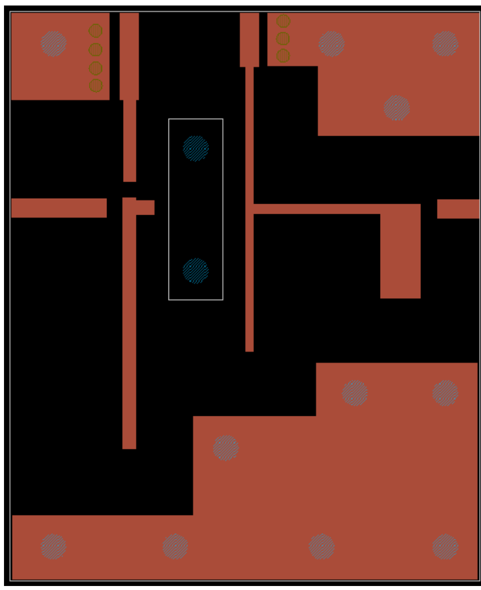


Figure 73: Layout Component of PCB

The *S*-parameter model of the PCB layout was used with the models of the actual circuit components which were obtained from the component vendors. An EM co-simulation was then performed in ADS, the results of which are shown in Figure 74.

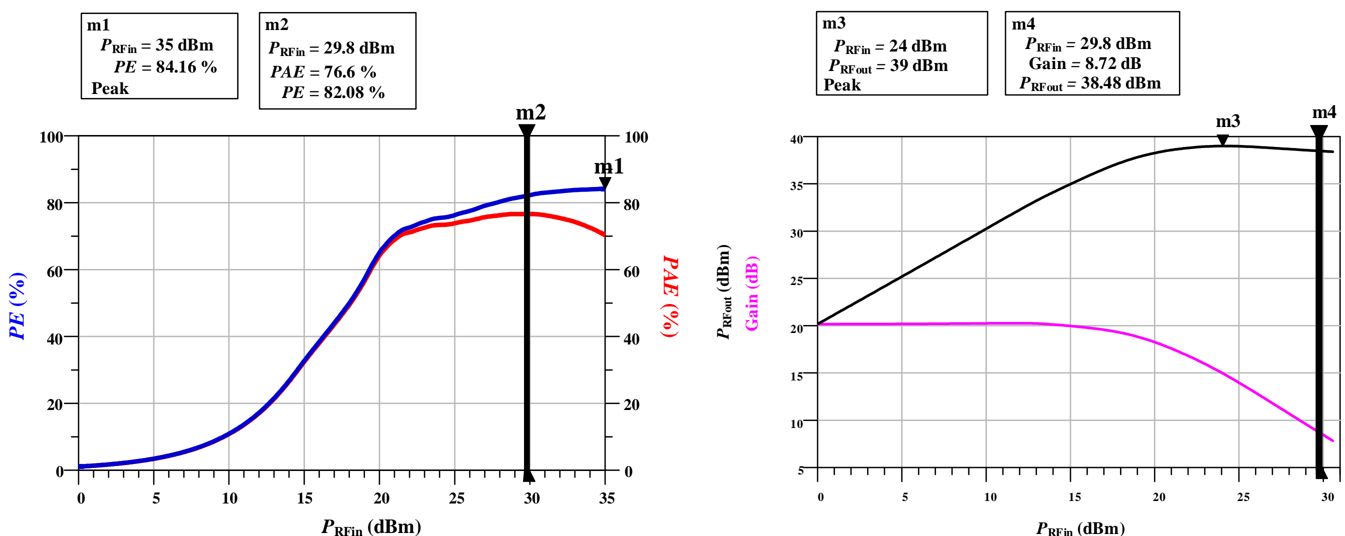


Figure 74: Momentum Simulated Results for *PE*, *PAE*, Gain and P_{RFout}

The following parameters were obtained: a peak PE of 84.162 % at P_{RFin} = 35 dBm, a peak PAE of 76.6 % at P_{RFin} = 29.8 dBm, as depicted by markers m1 and m2, respectively. A peak P_{RFout} of 39 dBm at P_{RFin} = 24 dBm as depicted by marker m3. The gain at an input power level corresponding to the peak PAE is 8.72 dB and is depicted by marker m4.

The compression characteristics of the PA were investigated, and the simulated parameters of the input and output compression points are shown in Figure 75.

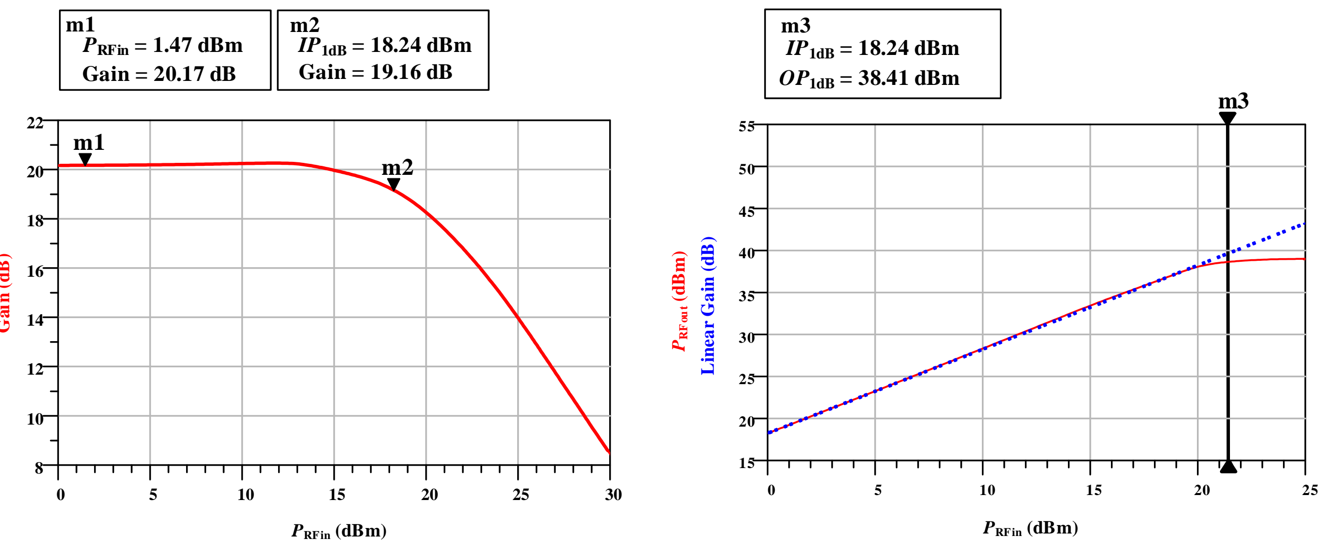


Figure 75: Simulated Results for $IP_{1\text{dB}}$ and $OP_{1\text{dB}}$

Figure 75 shows a simulated $IP_{1\text{dB}}$ of 18.24 dB and an $OP_{1\text{dB}}$ of 38.41 dBm. The corresponding gain at 1 dB compression is 19.16 dB. The highest PE is achieved when driving the PA into compression. Figure 76 shows that a PE and PAE of just above 50 % is achieved at the start of compression.

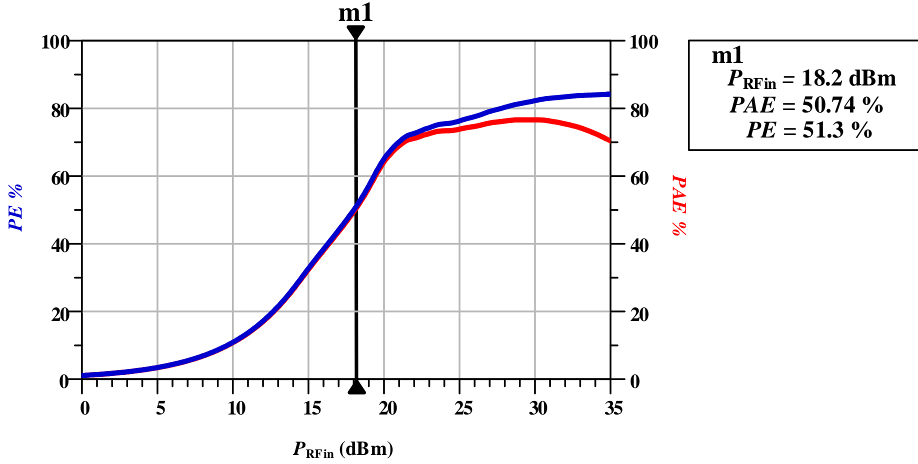


Figure 76: PE and PAE at IP_{1dB} Point

The performance of the PA was evaluated under conditions where the supply voltage was varied and the simulated results are shown in Figure 77. Such conditions were investigated to observe the behaviour of the PA and its ability to maintain functionality under reduced power supply conditions which typically may be experienced in a CubeSat as the battery power reduces over time.

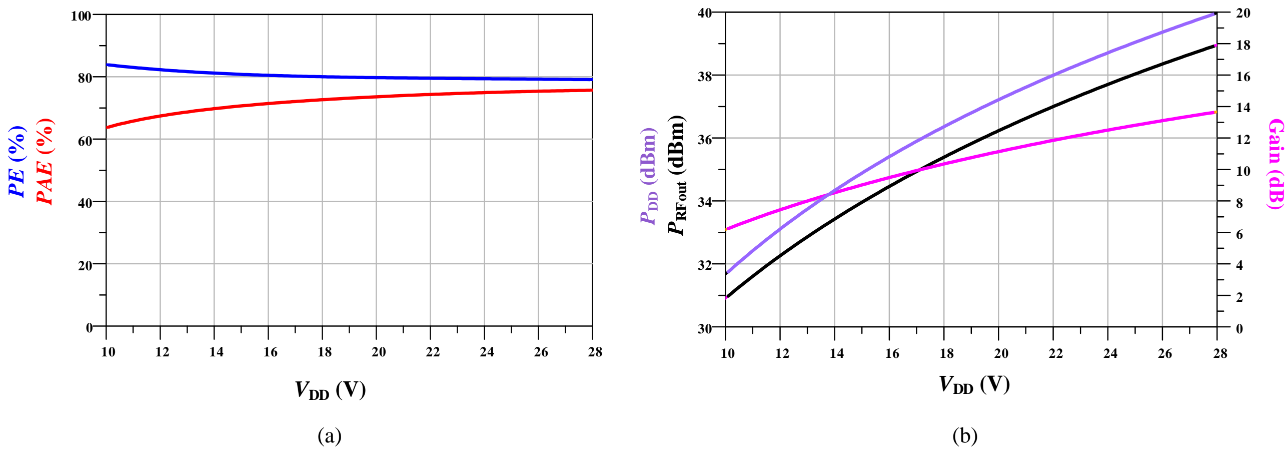


Figure 77: Simulated Performance with Varied V_{DD}

Figure 77 (a) shows that the PAE reduces from just above 75 % to just below 64 % as V_{DD} is decreased from 28 - 10 V, whereas the PE increased very slightly from 79 % to just below 84 %. The reason for this slight increase in PE, at lower values of V_{DD}, is that the DC power has decreased

slightly more than the RF output power hence the slight increase in *PE* at lower values of V_{DD}. Figure 77 (b) shows that as V_{DD} is reduced both the DC supply power (P_{DD} (dBm)) and the RF output power (P_{RFout} (dBm)) decrease. P_{DD} decreases from just below 40 dBm to just above 31 dBm, whereas P_{RFout} (dBm) decreases from just below 39 dBm to just below 31 dBm. The gain also decreased from just below 14 dB to just above 6 dB. The results in Figure 77 show that even when there is a significant reduction in DC supply voltage that both the *PE* and *PAE* remain above 64% which is still significantly better than the *PE* of 25 % in the existing PA as used in ZACUBE-2.

To evaluate the bandwidth of the PA, the variation in *PE*, *PAE* and P_{RFout} were simulated, at an input power level of 29.8 dBm, from 2 GHz to 2.3 GHz. The variation in these parameters is shown in Figure 78.

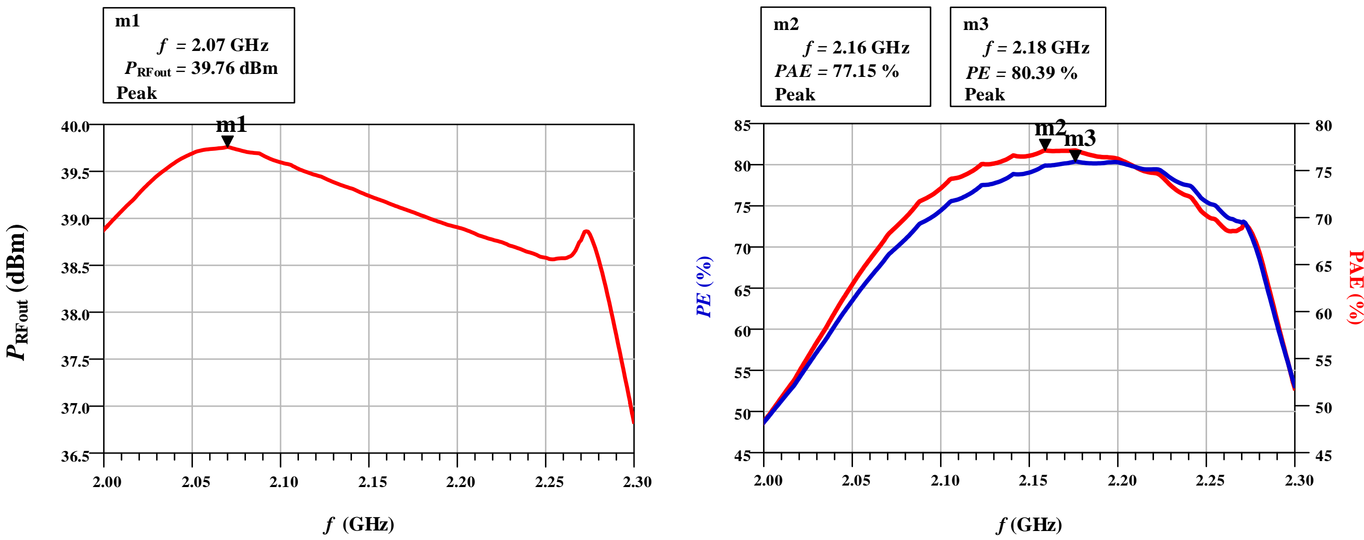


Figure 78: Variation in Simulated *PE*, *PAE* and P_{RFout} versus Frequency

Figure 78 shows that the PA maintains an output power level well above 36.5 dBm from 2 GHz to 2.3 GHz with a peak output power level of 39.76 dBm at 2.07 GHz. A peak *PAE* of 77.15 % is obtained at 2.16 GHz and a peak *PE* of 80.39 % at 2.18 GHz. A *PE* and *PAE* above 48 % are maintained from 2 - 2.3 GHz.

6.9 Conclusion

The simulated performance parameters of the WHIP network shown in Figure 61, Figure 62, and Figure 63 as well the waveforms for $V_{DS}(t)$ and $I_{DS}(t)$ shown in Figure 67 suggest that this very efficient PA is a Class-F PA. This is further confirmed by achieving a simulated *PE* of 82.08 % and a *PAE* of 76.6 % at 2.2 GHz.

Furthermore, this PA delivers a *PE* and a *PAE* of more than 48 %, and an output power level well above 36.5 dBm, from 2 GHz to 2.3 GHz.

Also, this PA delivers a *PE* above 79 %, a *PAE* above 63 %, and a P_{RFout} above 30 dBm when the supply voltage is varied from 28 down to 10 V.

The highest value of *PE* achieved was 84.16 % at a frequency of 2.2 GHz and an input power level of 35 dBm. The highest value of *PAE* achieved was 77.15 % at a frequency of 2.16 GHz and an input power level of 29.8 dBm. The maximum RF output power delivered to the load was 39.76 dBm at a frequency of 2.07 GHz at an input power level of 29.8 dBm.

The maximum gain achieved was just above 20 dB which dropped to 19.16 dB at P_{1dB}. The IP_{1dB} and OP_{1dB} points of the PA are 18.24 dB and 38.41 dB respectively, with a corresponding gain of 19.16 dB

The stability of the PA was evaluated using the specialised STAN tool, specifically designed to analyse the stability of non-linear circuits. This STAN tool evaluation revealed potentially instability of the PA at 4.1 GHz, which was then rendered stable from 0 - 6 GHz, with a swept input power level from 0 - 35 dBm, using an increased gate resistor value.

Chapter 7

The Constructed PA

7.1 Introduction

In this chapter, the construction of the Class-F PA is presented. The procedures followed during the measurement process are presented and explained and finally, the measured performance parameters are also presented. The constructed prototype PA is shown in Figure 79.

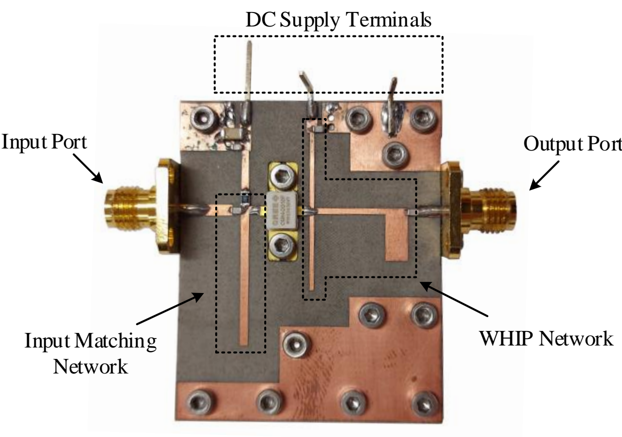


Figure 79: The Constructed Prototype PA

7.2 Measurements

To conduct accurate measurements of the constructed PA, specialised instruments are required, the setup of which is illustrated in Figure 80. The signal generator used for the measurements is an Agilent N9310 9 kHz - 3 GHz RF Signal Generator. The generated signal was applied to a Mini-Circuits ZVE-2W-272+ pre-amplifier with a gain of 20 dB to ensure a sufficient level of the input signal to drive the PA into compression. A Quest SM2023T isolator was used to isolate the Mini-Circuit pre-amplifier and the PA. The attenuation of the isolator was measured as 0.5 dB and is shown in Figure 81.

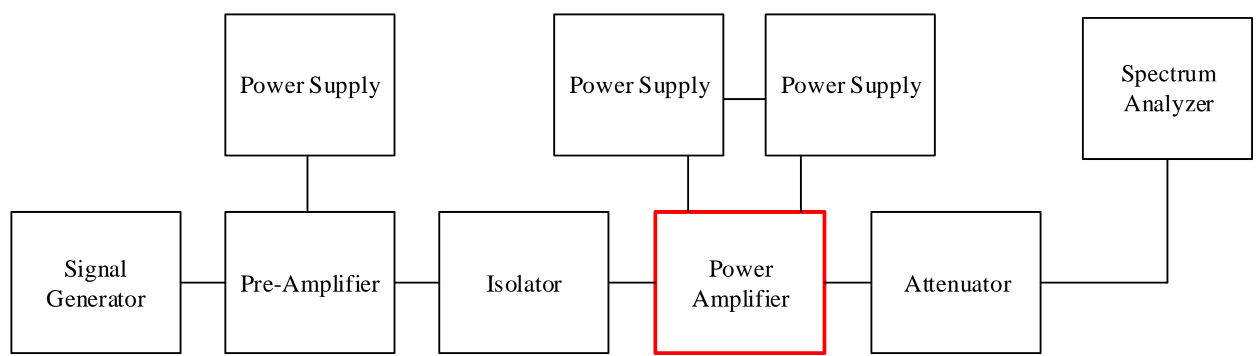


Figure 80: Instrument Setup for Measurements

The constructed PA is indicated by the red block in the measurement setup shown in Figure 80.

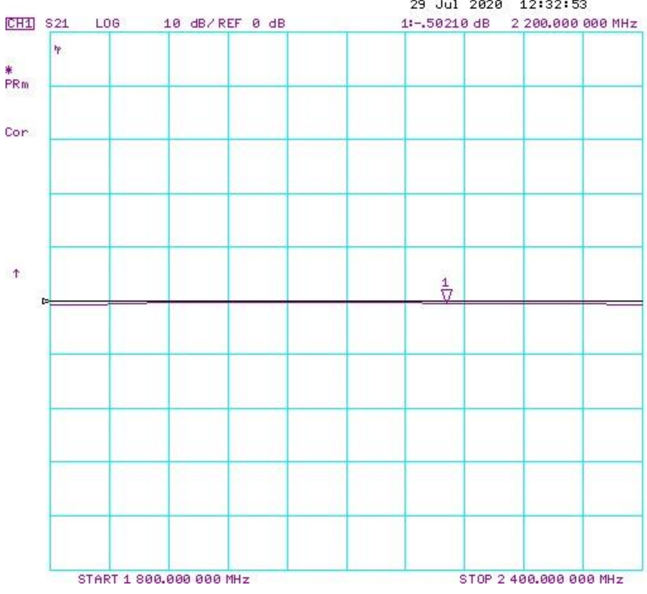


Figure 81: Measured Attenuation of the Isolator

A 40 dB attenuator was connected to the output port of the PA to limit the level of the signal at the input port of the spectrum analyser to prevent damage thereof. The measured attenuation of the attenuator was 40.969 dB and is shown in Figure 82. An Agilent E4404B spectrum analyser was used for spectral and power measurements.

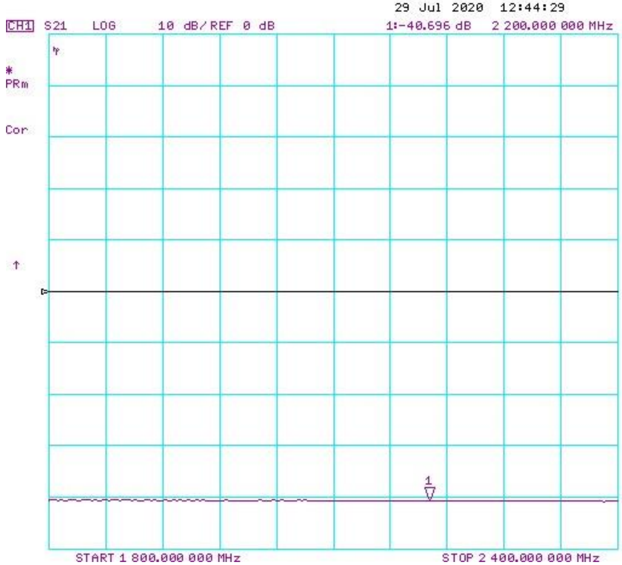


Figure 82: Measured Attenuation of the Attenuator

The performance of the pre-amplifier was measured, and the results are shown in Figure 83.

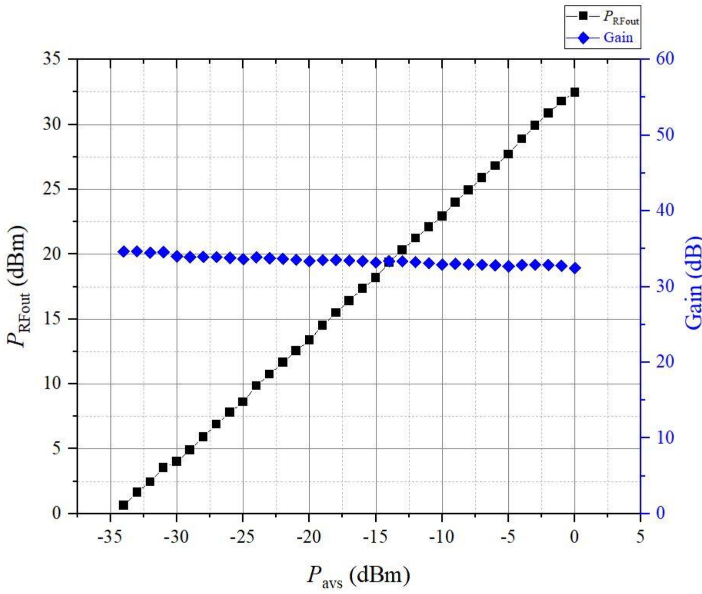


Figure 83: Gain and Output Power Measurements of the Pre-Amplifier

Figure 83 shows that the Mini-Circuits pre-amplifier, at 2.2 GHz, produces an average gain of 33 dB and a peak output power level of 33.5 dBm at an input level of 0 dBm.

The PA was biased at V_{DS} = 28 V and V_{GS} = −2.68 V as per the datasheet of the active device. The performance parameters of the constructed PA were then measured at 2.2 GHz by increasing the level of the applied signal in 1 dBm increments from -34 dBm to 0 dBm. At each increment, the DC input power to the constructed PA was calculated and then the *PE* and *PAE* were calculated using equations (3.19) and (3.20).

7.3 Performance Measurements

A frequency sweep revealed that maximum *PE* and *PAE* could be achieved at 2.1 GHz. The *PE* and *PAE* of the constructed PA were measured at this frequency, and the results are shown in Figure 84.

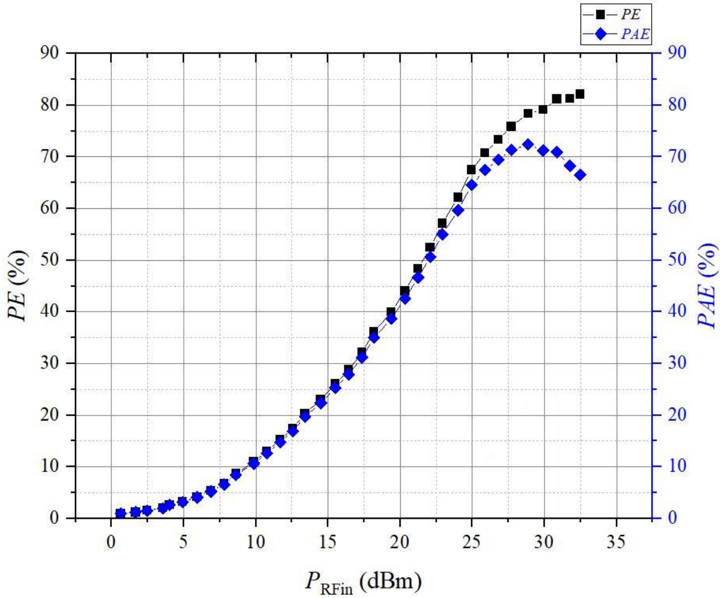


Figure 84: Measured *PE* and *PAE* at 2.1 GHz

A *PE* of 82.12 % was measured at P_{RFin} = 32.47 dBm and a *PAE* of 72.4 % at P_{RFin} = 28.87 dBm. P_{RFout} and gain were measured versus P_{RFin} and are shown in Figure 85.

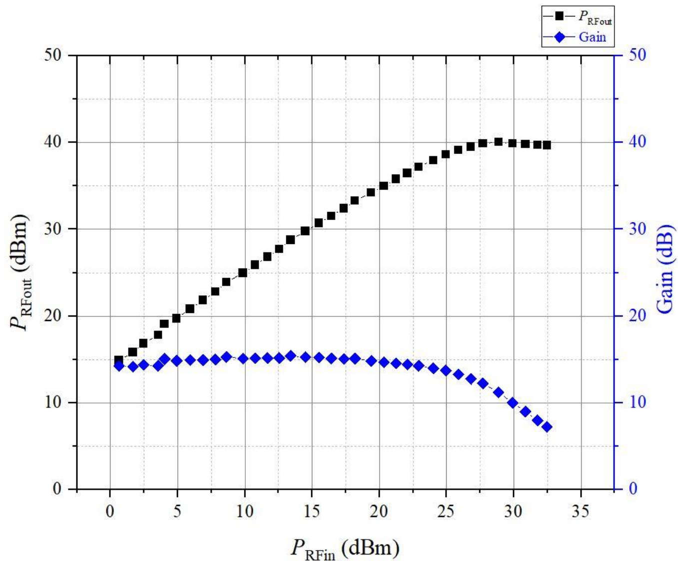


Figure 85: Measured P_{RFout} and Gain vs P_{RFin}

Compression in the PA starts approximately at P_{RFin} = 25 dBm with P_{RFout} = 37 dBm. The PA achieves a peak output power of 40.06 dBm.

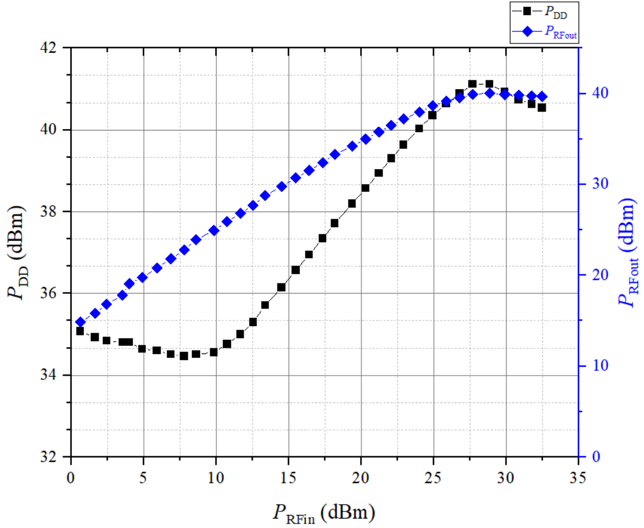


Figure 86: Measured P_{DD} and P_{RFout} vs P_{RFin}

The maximum P_{DD} of 41.12 dBm was supplied to the PA and a maximum P_{RFout} = 40.06 dBm was delivered to the load, both at P_{RFin} = 28.87 dBm. The variation in power delivered to the load was measured by varying the frequency of the applied signal from 1.9 GHz to 2.25 GHz, at P_{RFin} = 30.86 dBm. The measured parameters are shown in Figure 87.

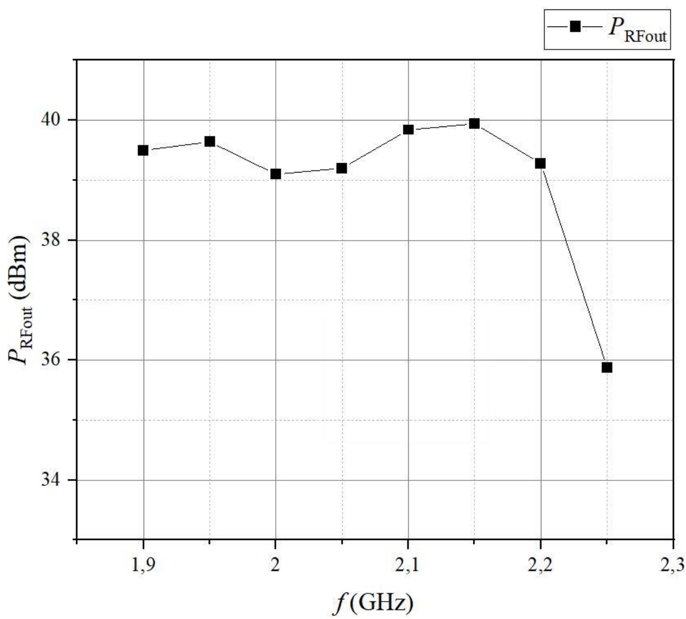


Figure 87: Measured Saturated P_{RFout} versus Frequency at P_{RFin} = 30.86 dBm

The level of P_{RFout} is greater than 39 dBm from 1.9 GHz to 2.2 GHz with a peak P_{RFout} of 39.94 dBm at 2.15 GHz, and a minimum P_{RFout} of 35.87 dBm measured at 2.25 GHz. The variation in *PE* and *PAE* versus frequency was measured by varying the frequency of the applied signal from 1.9 GHz to 2.25 GHz at a P_{RFin} of 30.86 dBm. The measured parameters are shown in Figure 88.

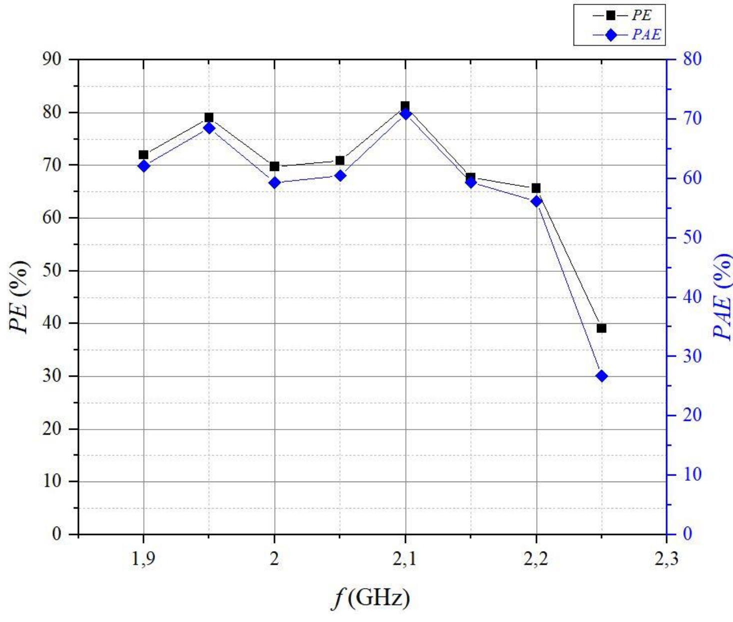


Figure 88: Measured Saturated *PE* and *PAE* vs Frequency at P_{RFin} = 30.86 dBm

At 2.1 GHz, the PA achieves a maximum *PE* of 81.18 % and a maximum *PAE* of 70.91 %. The *PE* varies from 72.02 % at 1.9 GHz to 65.63 % at 2.2 GHz and drops off to 39.1 % at 2.25 GHz. The *PAE* varies from 62.16 % at 1.9 GHz to 56.19 % at 2.2 GHz and drops off to 26.76 % at 2.25 GHz.

The variations in P_{RFout}, *PE*, and *PAE* of the PA were measured by varying V_{DD} from 10 - 28 V and are shown in Figure 89 and Figure 90. P_{RFin} was set at 30.86 dBm for these measurements.

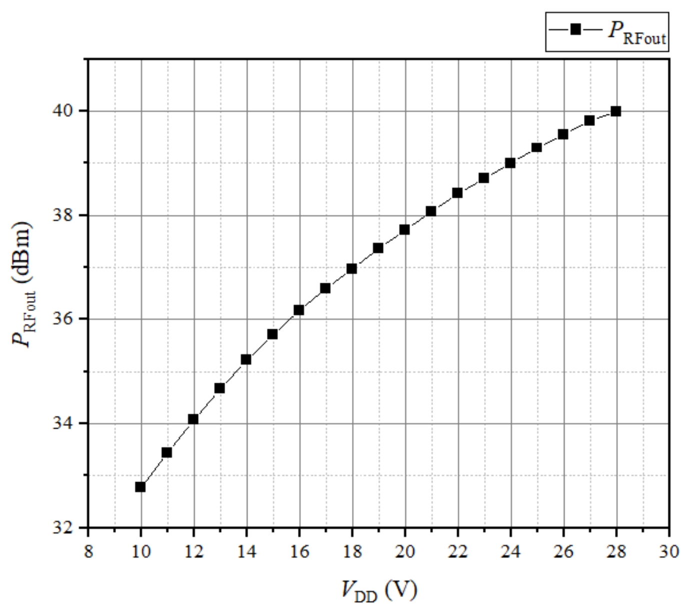


Figure 89: Measured P_{RFout} vs V_{DD} at P_{RFin} = 30.86 dBm

The PA achieves a maximum P_{RFout} just below 40 dBm at 28 V and a minimum P_{RFout} of just below 33 dBm at 10 V.

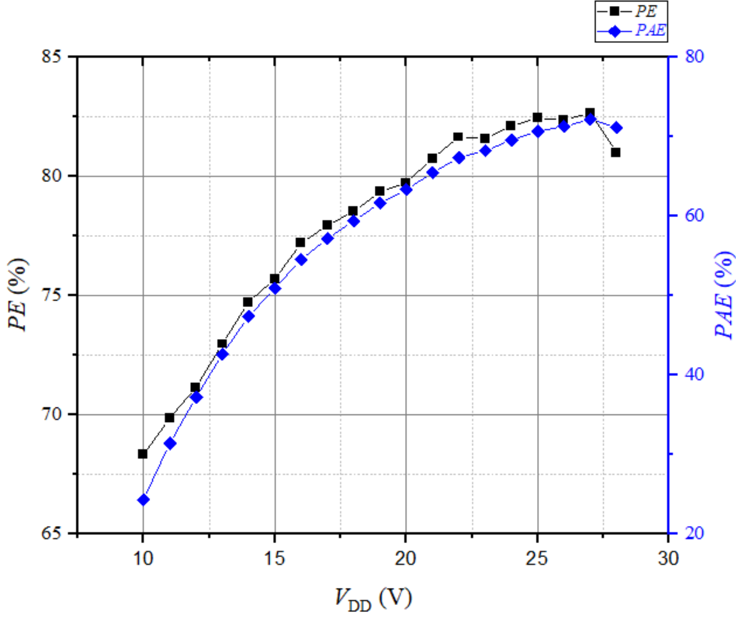


Figure 90: *PE* and *PAE* vs V_{DD} at P_{RFin} = 30.86 dBm

The PA achieves a maximum saturated *PE* and *PAE* of 82.63 % and 72.13 %, respectively at V_{DD} = 27 V. The *PE* varies from just above 68 % at V_{DD} = 10 V to just below 83 % at V_{DD} = 27 V. The *PAE* varies from just above 24 % at V_{DD} = 10 V to just above 72 % at V_{DD} = 27 V.

7.4 Comparisons

A comparison between the simulated and measured performance parameters are presented in Table 5.

Parameter	Simulated	P_{RFin} (dBm)	Measured	P_{RFin} (dBm)
PE (%)	84.16	35	82.12	32.47
PAE (%)	76.6	29.8	72.4	28.87
Output Power (dBm)	39	24	40.06	28.87

Table 5: Comparison between Simulated and Measured Parameters

The measured *PE* and *PAE* of the PA correlate very well with the simulated results and the output power level measured exceeds the simulated value.

A comparison of the performance parameters of this PA and other PAs are presented in Table 6.

Class	*f* (GHz)	*PE* (%)	*PAE* (%)	Output Power (dBm)	Technology	Reference
F	2	-	80.1	40.7	GaN HEMT	(Hwang *et al.*, 2013)
A	2.142	25	-	17	GaAs HBT	ZACUBE-2
F	0.5	76	-	43.01	LDMOS	(Grebennikov, 2000)
F	0.95	-	75	40	Gan HEMT	(Sharma *et al.*, 2016)
F	2.570	-	82	41.3	GaN HEMT	(Xiong *et al.*, 2014)
F	1.8	60	-	41.15	LDMOS	(Lépine, Ådahl and Zirath, 2005)
F	2.1	82.12	72.4	40.06	GaN HEMT	(Ryno Nienaber, 2020)

Table 6: Comparison Between the Constructed PA and existing PAs

7.5 Conclusions

A Class-F PA was designed, built, and tested. The performance parameters of this PA were measured, and the results indicate that the PA delivers a *PE* of 82.12 % and a *PAE* of 72.4 % at an operating frequency of 2.1 GHz. The maximum output power delivered to the load was 40.06 dBm, that is, an actual power of 10.14 Watts.

A *PE* of 82.12 % means that only 17.88 % of the DC input power is dissipated in the active device. The output power of 10.14 W approaches the maximum output power of 13 W, as specified in the datasheet by the manufacturer.

The simulated and measured performance parameters of this Class-F PA correlated extremely well with an average difference of 2.9 % between simulated and measured values.

When compared to the Class-F PA of Grebennikov, (2000), this PA performs extremely well with a higher *PE* but slightly less output power. However, when compared to the PAs which use GaN HEMT technology in Table 6, all the output powers are approximately 40 dBm. The *PAEs* were slightly higher than the constructed PA, but unfortunately, they did not publish the performance parameters of their *PE*s.

The current Class-A PA utilised in the F'SATI CubeSat, ZACUBE-2 has a *PE* of 25% and an output power of 17 dBm. The constructed PA would provide a significant saving in wasted power and an increased output power for the next generation of CubeSats planned by the F'SATI program.

The constructed PA did not show any signs of instability during the measurement procedure, thus the STAN stability analysis tool prediction was valid.

There was a slight shift in optimal operating frequency, possibly due to non-absorption of the parasitic series lead inductance of the active device.

7.6 Recommendations

The constructed PA had a relatively high efficiency at a slightly lower operating frequency than that simulated. This frequency shift may be avoided by utilising a wafer active device, rather than a packaged device because a Class-F WHIP network precludes the absorption of the series lead-inductance presented by the active device. It is thus recommended to evaluate the performance of a Class-F PA using a wafer active device.

The simulations for the transconductance of the active device indicated that the g_m obtained at the specific biasing conditions could be varied slightly. A slight decrease in V_{GS} would increase the transconductance and thereby possibly the gain, linearity, and output power of the PA. It is recommended that g_m be increased slightly, and the performance of the PA re-evaluated.

A highly linear pre-amplifier is required to supply a suitable input signal to drive the PA into compression. A suitable pre-amplifier candidate could be a Class-D push-pull amplifier. However, optimal performance is a trade-off between *PE* and linearity.

Lastly, it is recommended that a harmonic filter be implemented on the input port before the Class-F PA to minimise the harmonic content of the input signal, thereby potentially minimising IMD and better linearity of the PA.

Appendix A

The impedance presented by the input port of a short-circuited $\frac{\lambda_g}{4}$ stub compared to a combination of an open- and short circuit $\frac{\lambda_g}{8}$ stub connected in parallel.

From transmission line theory and as shown in section 5.4 the lossless impedance transformation equation is restated below:

$$Z(d) = \left[\frac{Z_L + jZ_0 \tan(\beta l)}{Z_0 + jZ_L \tan(\beta l)} \right] Z_0 \quad \Omega \qquad \text{restated (5.16)}$$

From equation (5.16), the impedance presented by the input port of a transmission line with an electrical length βl, and terminated in an open-circuit, is given by:

$$Z(d)\big|_{\text{O/C}} = -jZ_0 \cot(\beta l) \quad \Omega \tag{6.6}$$

Similarly, the impedance presented by the input port of a transmission line with an electrical length βl, and terminated in a short-circuit, is given by:

$$Z(d)\big|_{\text{S/C}} = -jZ_0 \cot(\beta l) \quad \Omega \tag{6.7}$$

The impedance presented by the input port of an open- and short-circuited transmission line of electrical length βl, and connected in parallel, is derived as follows:

$$
\begin{aligned}
Z_{\mathrm{p}}(d) &= Z(d)\big|_{\mathrm{O/C}} \quad \| \quad Z(d)\big|_{\mathrm{S/C}} \qquad \Omega \\
&= -jZ_0 \cot(\beta l) \,\|\, jZ_0 \tan(\beta l) \\
&= \frac{\left[-jZ_0 \cot(\beta l)\right]\left[jZ_0 \tan(\beta l)\right]}{\left[-jZ_0 \cot(\beta l) + jZ_0 \tan(\beta l)\right]} \\
&= \frac{Z_0^2}{\left[-jZ_0 \cot(\beta l) + jZ_0 \tan(\beta l)\right]} \\
&= \frac{Z_0^{2}}{-jZ_0\left[\cot(\beta l) - \tan(\beta l)\right]} \\
&= \frac{jZ_0}{\cot(\beta l) - \tan(\beta l)}
\end{aligned}
$$

$$
Z_{\mathrm{p}}(d) = \frac{jZ_0 \tan}{1 - \tan^2(\beta l)} \qquad \Omega
$$

which can be simplified by the double angle tangent identity resulting in:

$$
Z_{\mathrm{p}}(d) = \frac{1}{2} jZ_0 \tan(2\beta l) \qquad \Omega \tag{6.8}
$$

The impedance presented by the input port of a $\left.\frac{\lambda_{\mathrm{g}}}{4}\right|_{\mathrm{S/C}}$ stub is expressed by equation (6.7) and the impedance presented by the input port of an open- and short-circuited pair of transmission lines connected in parallel $Z_{\mathrm{p}}(d) = Z(d)\big|_{\mathrm{O/C}} \big\| Z(d)\big|_{\mathrm{S/C}}$ is expressed by equation (6.8).

This mathematical analysis reveals that the impedance presented by the input port of the combination of the open- and short circuit $\frac{\lambda_{\mathrm{g}}}{8}$ stubs is scaled by 0.5 and will thus present exactly half the impedance presented by the input port of the $\left.\frac{\lambda_{\mathrm{g}}}{4}\right|_{\mathrm{S/C}}$ stub.

This can be confirmed by simulating the impedance presented by the input port of the two networks at an operating frequency of 1GHz as shown in Figure 91.

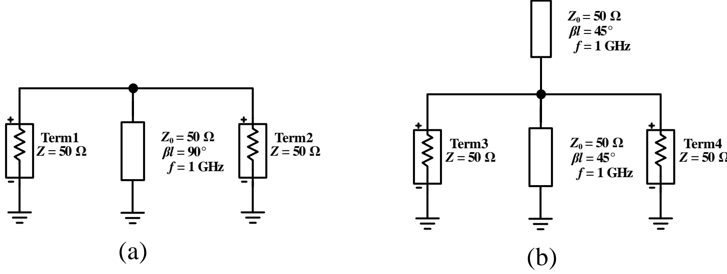


Figure 91: (a) $\left.\frac{\lambda_g}{4}\right|_{\mathrm{S/C}}$ stub and (b) $Z_p = \left.\frac{\lambda_g}{8}\right|_{\mathrm{S/C}} \Big\| \left.\frac{\lambda_g}{8}\right|_{\mathrm{O/C}}$ stub

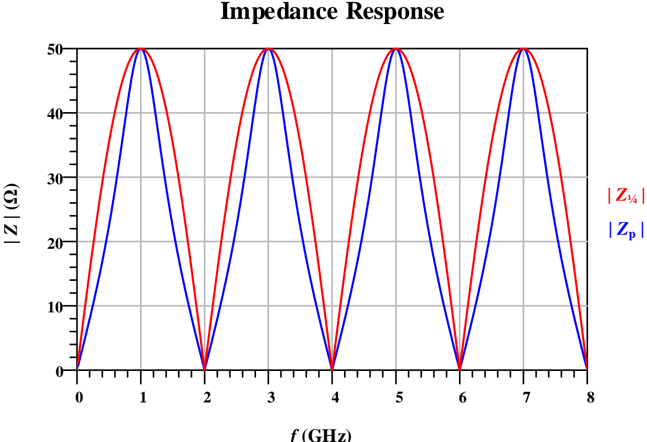


Figure 92: Magnitude of the Impedance Response

Figure 92 also reveals that the impedance response of the $\frac{\lambda_g}{8}$ transmission line combination is narrower than that of the short-circuited $\frac{\lambda_g}{4}$ transmission line, hence improved impedance loading characteristics.

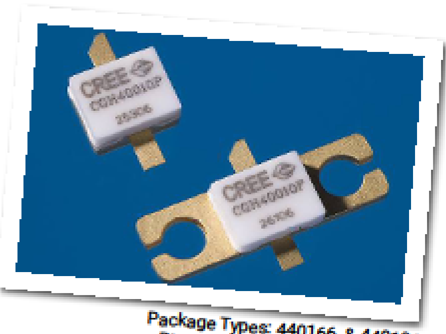
Appendix B

Cree CGH40010 GaN HEMT Datasheet

CGH40010

10 W, DC - 6 GHz, RF Power GaN HEMT

Cree's CGH40010 is an unmatched, gallium nitride (GaN) high electron mobility transistor (HEMT). The CGH40010, operating from a 28 volt rail, offers a general purpose, broadband solution to a variety of RF and microwave applications. GaN HEMTs offer high efficiency, high gain and wide bandwidth capabilities making the CGH40010 ideal for linear and compressed amplifier circuits. The transistor is available in both screw-down, flange and solder-down, pill packages.



Package Types: 440166, & 440196
PN's: CGH40010F & CGH40010P

FEATURES

- Up to 6 GHz Operation
- 16 dB Small Signal Gain at 2.0 GHz
- 14 dB Small Signal Gain at 4.0 GHz
- 13 W typical P_{SAT}
- 65 % Efficiency at P_{SAT}
- 28 V Operation

APPLICATIONS

- 2-Way Private Radio
- Broadband Amplifiers
- Cellular Infrastructure
- Test Instrumentation
- Class A, AB, Linear amplifiers suitable for OFDM, W-CDMA, EDGE, CDMA waveforms

Large Signal Models Available for ADS and MWO

Rev 4.0 – May 2015

Absolute Maximum Ratings (not simultaneous) at 25˚C Case Temperature

Parameter	Symbol	Rating	Units	Conditions
Drain-Source Voltage	V_{DSS}	84	Volts	25˚C
Gate-to-Source Voltage	V_{GS}	-10, +2	Volts	25˚C
Storage Temperature	T_{STG}	-65, +150	˚C	
Operating Junction Temperature	T_J	225	˚C	
Maximum Forward Gate Current	I_{GMAX}	4.0	mA	25˚C
Maximum Drain Current[1]	I_{DMAX}	1.5	A	25˚C
Soldering Temperature[2]	T_S	245	˚C	
Screw Torque	τ	60	in-oz	
Thermal Resistance, Junction to Case[3]	$R_{θJC}$	8.0	˚C/W	85˚C
Case Operating Temperature[3,4]	T_C	-40, +150	˚C	

Note:
[1] Current limit for long term, reliable operation
[2] Refer to the Application Note on soldering at www.cree.com/RF/Document-Library
[3] Measured for the CGH40010F at P_{DISS} = 14 W.
[4] See also, the Power Dissipation De-rating Curve on Page 6.

Electrical Characteristics (T_C = 25˚C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics[1]						
Gate Threshold Voltage	$V_{GS(th)}$	-3.8	-3.0	-2.3	V_{DC}	V_{DS} = 10 V, I_D = 3.6 mA
Gate Quiescent Voltage	$V_{GS(Q)}$	–	-2.7	–	V_{DC}	V_{DS} = 28 V, I_D = 200 mA
Saturated Drain Current	I_{DS}	2.9	3.5	–	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
Drain-Source Breakdown Voltage	V_{BR}	120	–	–	V_{DC}	V_{GS} = -8 V, I_D = 3.6 mA
RF Characteristics[2] (T_C = 25˚C, F_0 = 3.7 GHz unless otherwise noted)						
Small Signal Gain	G_{SS}	12.5	14.5	–	dB	V_{DD} = 28 V, I_{DQ} = 200 mA
Power Output[3]	P_{SAT}	10	12.5	–	W	V_{DD} = 28 V, I_{DQ} = 200 mA
Drain Efficiency[4]	η	55	65	–	%	V_{DD} = 28 V, I_{DQ} = 200 mA, P_{SAT}
Output Mismatch Stress	VSWR	–	–	10 : 1	Ψ	No damage at all phase angles, V_{DD} = 28 V, I_{DQ} = 200 mA, P_{OUT} = 10 W CW
Dynamic Characteristics						
Input Capacitance	C_{GS}	–	4.5	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Output Capacitance	C_{DS}	–	1.3	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Feedback Capacitance	C_{GD}	–	0.2	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz

Notes:
[1] Measured on wafer prior to packaging.
[2] Measured in CGH40010-AMP.
[3] P_{SAT} is defined as I_G = 0.36 mA.
[4] Drain Efficiency = P_{OUT} / P_{DC}

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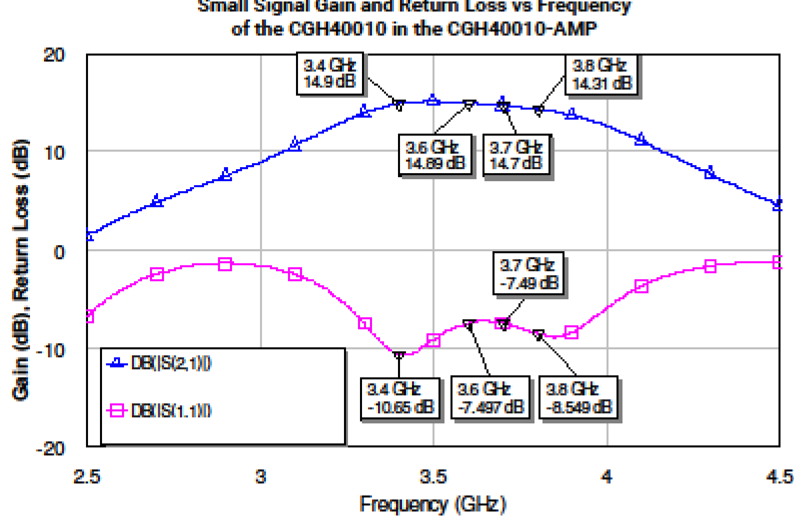
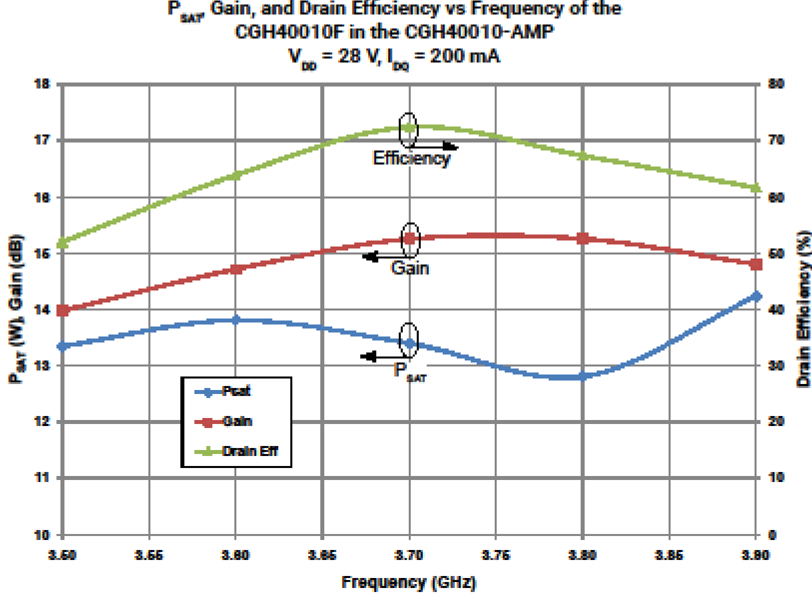
Typical Performance





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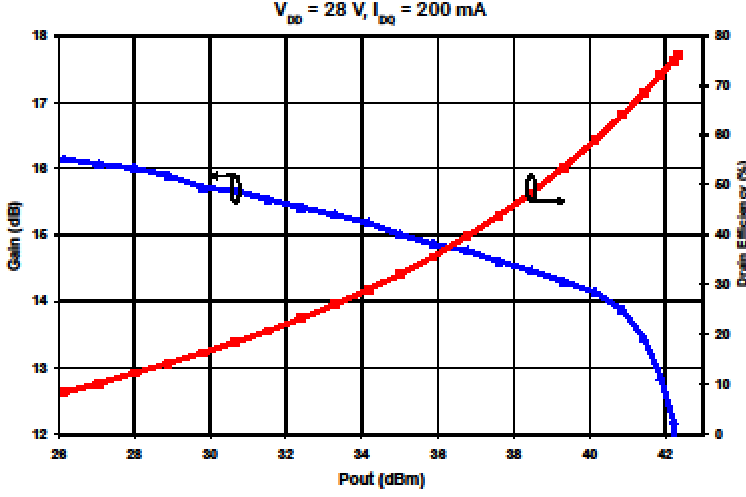
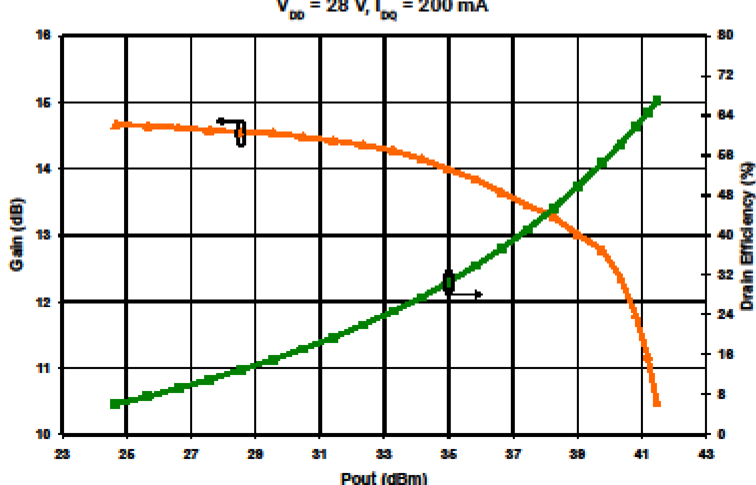
Typical Performance





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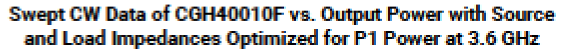
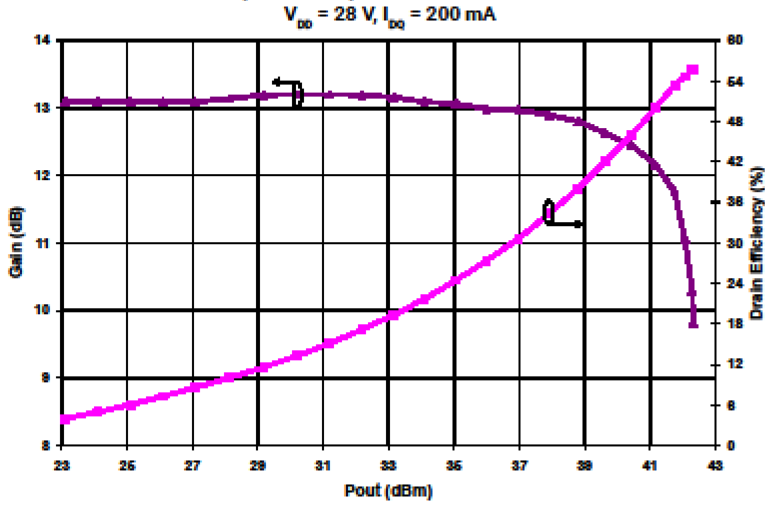
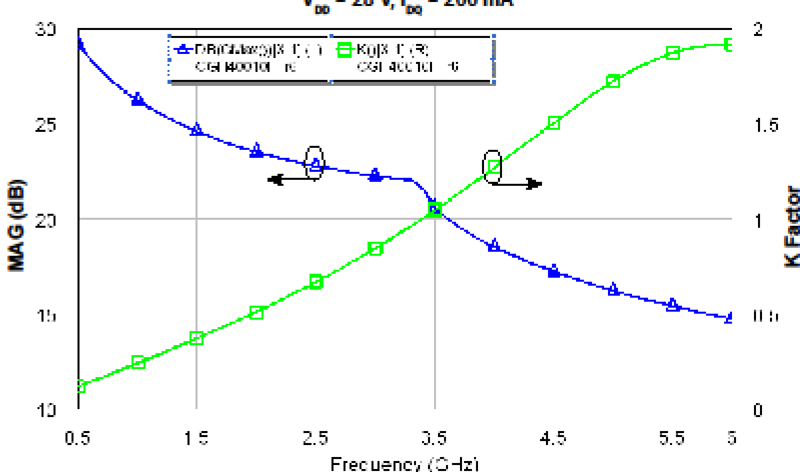
Typical Performance



Swept CW Data of CGH40010F vs. Output Power with Source and Load Impedances Optimized for P1 Power at 3.6 GHz
V_{DD} = 28 V, I_{DQ} = 200 mA



Simulated Maximum Available Gain and K Factor of the CGH40010F
V_{DD} = 28 V, I_{DQ} = 200 mA



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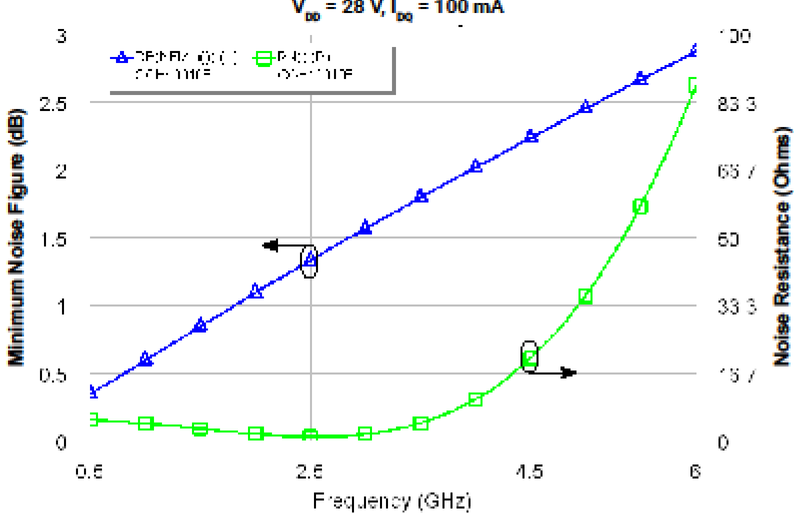
Typical Noise Performance

Simulated Minimum Noise Figure and Noise Resistance vs Frequency of the CGH40010F
V_{DD} = 28 V, I_{DQ} = 100 mA



Electrostatic Discharge (ESD) Classifications

Parameter	Symbol	Class	Test Methodology
Human Body Model	HBM	1A > 250 V	JEDEC JESD22 A114-D
Charge Device Model	CDM	1 < 200 V	JEDEC JESD22 C101-C

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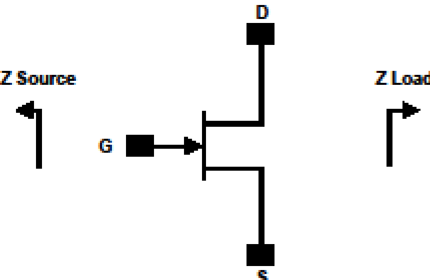
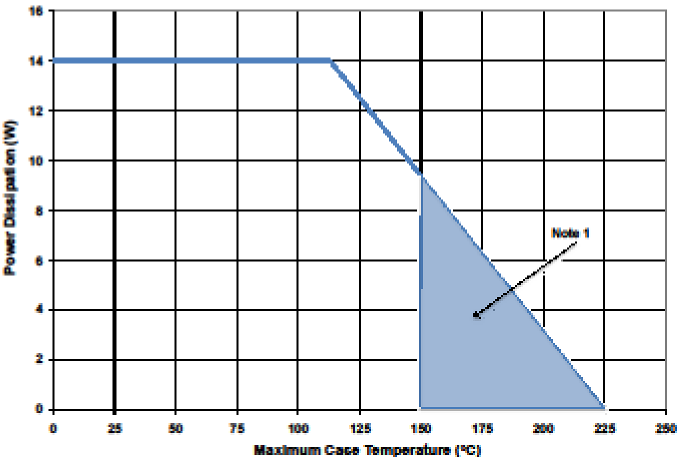
Source and Load Impedances



Frequency (MHz)	Z Source	Z Load
500	20.2 + j16.18	51.7 + j15.2
1000	8.38 + j9.46	41.4 + j28.5
1500	7.37 + j0	28.15 + j29
2500	3.19 - j4.76	19 + j9.2
3500	3.18 - j13.3	14.6 + j7.46

Note 1. V_{DD} = 28V, I_{DQ} = 200mA in the 440166 package.
Note 2. Optimized for power, gain, P_{SAT} and PAE.
Note 3. When using this device at low frequency, series resistors should be used to maintain amplifier stability.

CGH40010 Power Dissipation De-rating Curve



Note 1. Area exceeds Maximum Case Operating Temperature (See Page 2).

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CGH40010-AMP Demonstration Amplifier Circuit Bill of Materials

Designator	Description	Qty
R1,R2	RES,1/16W,0603,1%,0 OHMS	1
R3	RES,1/16W,0603,1%,47 OHMS	1
R4	RES,1/16W,0603,1%,100 OHMS	1
C6	CAP, 470PF, 5%,100V, 0603	1
C17	CAP, 33 UF, 20%, G CASE	1
C16	CAP, 1.0UF, 100V, 10%, X7R, 1210	1
C8	CAP 10UF 16V TANTALUM	1
C14	CAP, 100.0pF, +/-5%, 0603	1
C1	CAP, 0.5pF, +/-0.05pF, 0603	1
C2	CAP, 0.7pF, +/-0.1pF, 0603	1
C10,C11	CAP, 1.0pF, +/-0.1pF, 0603	2
C4,C12	CAP, 10.0pF,+/-5%, 0603	2
C5,C13	CAP, 39pF, +/-5%, 0603	2
C7,C15	CAP,33000PF, 0805,100V, X7R	2
J3,J4	CONN SMA STR PANEL JACK RECP	1
J2	HEADER RT>PLZ.1CEN LK 2 POS	1
J1	HEADER RT>PLZ .1CEN LK 5POS	1
-	PCB, RO4350B, Er = 3.48, h = 20 mil	1
Q1	CGH40010F or CGH40010P	1

CGH40010-AMP Demonstration Amplifier Circuit

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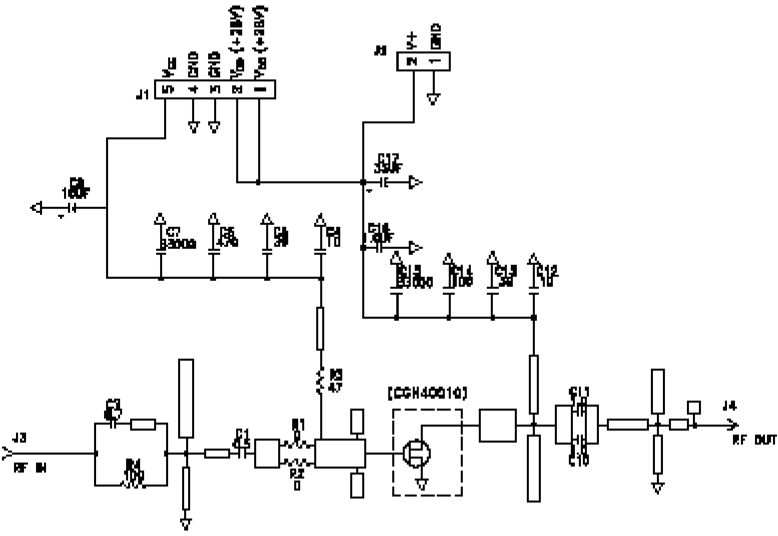
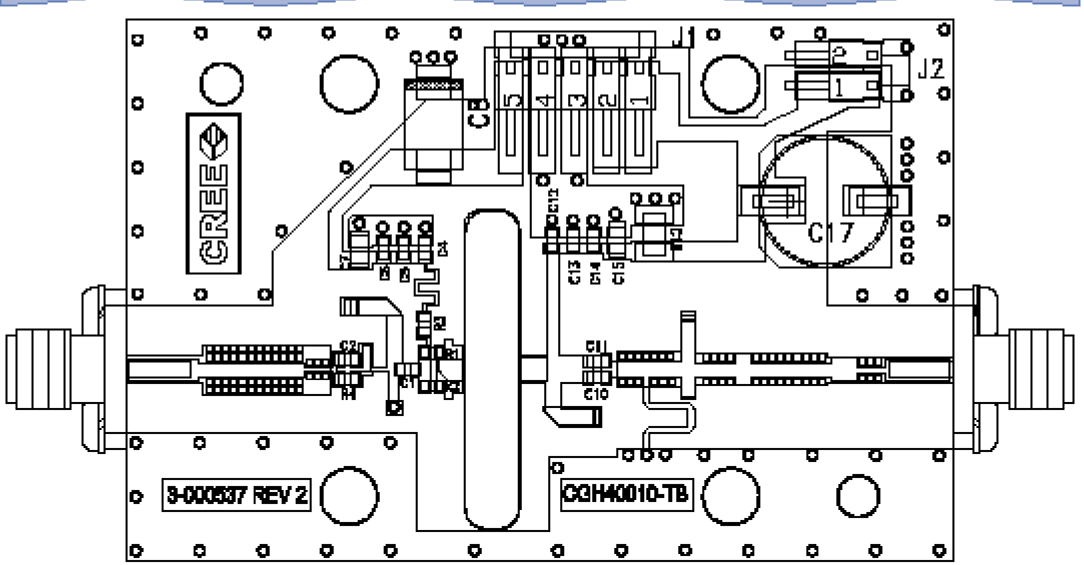
CGH40010-AMP Demonstration Amplifier Circuit Schematic



CGH40010-AMP Demonstration Amplifier Circuit Outline



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Typical Package S-Parameters for CGH40010
(Small Signal, V_{DS} = 28 V, I_{DQ} = 100 mA, angle in degrees)

Frequency	Mag S11	Ang S11	Mag S21	Ang S21	Mag S12	Ang S12	Mag S22	Ang S22
500 MHz	0.909	-123.34	17.19	108.22	0.027	21.36	0.343	-90.81
600 MHz	0.902	-133.06	14.86	101.82	0.028	15.60	0.329	-98.65
700 MHz	0.897	-140.73	13.04	96.45	0.028	10.87	0.321	-104.84
800 MHz	0.894	-146.96	11.58	91.78	0.029	6.84	0.317	-109.84
900 MHz	0.891	-152.16	10.41	87.61	0.029	3.33	0.316	-113.95
1.0 GHz	0.890	-156.60	9.43	83.82	0.029	0.19	0.318	-117.42
1.1 GHz	0.889	-160.47	8.62	80.31	0.029	-2.66	0.321	-120.40
1.2 GHz	0.888	-163.90	7.93	77.02	0.029	-5.28	0.326	-123.02
1.3 GHz	0.887	-166.99	7.34	73.90	0.029	-7.72	0.332	-125.36
1.4 GHz	0.887	-169.80	6.82	70.92	0.029	-10.01	0.338	-127.51
1.5 GHz	0.887	-172.39	6.38	68.05	0.029	-12.18	0.345	-129.50
1.6 GHz	0.887	-174.80	5.98	65.28	0.028	-14.24	0.353	-131.37
1.7 GHz	0.887	-177.07	5.63	62.59	0.028	-16.21	0.360	-133.15
1.8 GHz	0.887	-179.22	5.32	59.97	0.028	-18.09	0.369	-134.87
1.9 GHz	0.887	178.73	5.04	57.41	0.028	-19.91	0.377	-136.54
2.0 GHz	0.888	176.76	4.78	54.89	0.027	-21.66	0.385	-138.17
2.1 GHz	0.888	174.86	4.55	52.42	0.027	-23.35	0.393	-139.77
2.2 GHz	0.888	173.02	4.34	49.99	0.027	-24.98	0.402	-141.34
2.3 GHz	0.888	171.23	4.15	47.60	0.026	-26.56	0.410	-142.90
2.4 GHz	0.889	169.48	3.97	45.24	0.026	-28.08	0.418	-144.45
2.5 GHz	0.889	167.76	3.81	42.90	0.026	-29.55	0.426	-145.99
2.6 GHz	0.890	166.07	3.66	40.59	0.025	-30.98	0.434	-147.53
2.7 GHz	0.890	164.39	3.53	38.30	0.025	-32.36	0.442	-149.06
2.8 GHz	0.890	162.74	3.40	36.03	0.025	-33.69	0.450	-150.59
2.9 GHz	0.891	161.10	3.28	33.78	0.024	-34.97	0.458	-152.12
3.0 GHz	0.891	159.46	3.17	31.55	0.024	-36.20	0.465	-153.65
3.2 GHz	0.892	156.21	2.97	27.12	0.023	-38.51	0.479	-156.72
3.4 GHz	0.893	152.96	2.79	22.73	0.022	-40.63	0.493	-159.80
3.6 GHz	0.893	149.69	2.64	18.38	0.022	-42.52	0.505	-162.90
3.8 GHz	0.894	146.38	2.50	14.05	0.021	-44.17	0.517	-166.03
4.0 GHz	0.894	143.03	2.38	9.72	0.020	-45.56	0.527	-169.19
4.2 GHz	0.894	139.61	2.28	5.40	0.019	-46.67	0.537	-172.39
4.4 GHz	0.895	136.11	2.18	1.07	0.019	-47.46	0.546	-175.64
4.6 GHz	0.895	132.53	2.09	-3.29	0.018	-47.90	0.554	-178.95
4.8 GHz	0.895	128.85	2.01	-7.68	0.017	-47.96	0.561	177.69
5.0 GHz	0.895	125.06	1.94	-12.10	0.017	-47.61	0.568	174.25
5.2 GHz	0.895	121.15	1.88	-16.58	0.016	-46.84	0.573	170.72
5.4 GHz	0.895	117.11	1.82	-21.12	0.016	-45.67	0.578	167.10
5.6 GHz	0.895	112.94	1.77	-25.73	0.015	-44.12	0.582	163.38
5.8 GHz	0.895	108.62	1.72	-30.42	0.015	-42.30	0.586	159.54
6.0 GHz	0.895	104.15	1.68	-35.20	0.015	-40.33	0.589	155.56

To download the s-parameters in s2p format, go to the CGH40010 Product page and click on the documentation tab.

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(Small Signal, V_{DS} = 28 V, I_{DQ} = 200 mA, angle in degrees)

Frequency	Mag S11	Ang S11	Mag S21	Ang S21	Mag S12	Ang S12	Mag S22	Ang S22
500 MHz	0.911	-130.62	18.41	105.41	0.022	19.44	0.303	-112.24
600 MHz	0.906	-139.65	15.80	99.47	0.023	14.31	0.299	-119.83
700 MHz	0.902	-146.70	13.80	94.50	0.023	10.17	0.298	-125.50
800 MHz	0.899	-152.41	12.22	90.19	0.023	6.68	0.299	-129.85
900 MHz	0.898	-157.17	10.96	86.34	0.024	3.67	0.302	-133.28
1.0 GHz	0.896	-161.24	9.92	82.82	0.024	0.99	0.305	-136.05
1.1 GHz	0.896	-164.79	9.06	79.56	0.024	-1.41	0.309	-138.34
1.2 GHz	0.895	-167.95	8.33	76.49	0.024	-3.62	0.314	-140.30
1.3 GHz	0.895	-170.80	7.70	73.57	0.023	-5.66	0.320	-142.01
1.4 GHz	0.894	-173.41	7.17	70.78	0.023	-7.56	0.326	-143.54
1.5 GHz	0.894	-175.82	6.70	68.08	0.023	-9.35	0.332	-144.94
1.6 GHz	0.894	-178.09	6.28	65.47	0.023	-11.05	0.338	-146.24
1.7 GHz	0.894	179.78	5.92	62.92	0.023	-12.66	0.345	-147.48
1.8 GHz	0.894	177.75	5.59	60.43	0.023	-14.19	0.352	-148.68
1.9 GHz	0.894	175.81	5.30	57.99	0.023	-15.65	0.358	-149.84
2.0 GHz	0.894	173.94	5.04	55.59	0.022	-17.05	0.365	-150.99
2.1 GHz	0.894	172.13	4.80	53.23	0.022	-18.39	0.372	-152.12
2.2 GHz	0.894	170.37	4.58	50.91	0.022	-19.67	0.379	-153.26
2.3 GHz	0.895	168.65	4.38	48.61	0.022	-20.90	0.386	-154.39
2.4 GHz	0.895	166.96	4.20	46.33	0.021	-22.08	0.393	-155.54
2.5 GHz	0.895	165.30	4.03	44.08	0.021	-23.20	0.400	-156.69
2.6 GHz	0.895	163.66	3.88	41.84	0.021	-24.27	0.407	-157.85
2.7 GHz	0.895	162.04	3.74	39.63	0.021	-25.28	0.414	-159.03
2.8 GHz	0.895	160.43	3.60	37.43	0.020	-26.25	0.420	-160.22
2.9 GHz	0.896	158.83	3.48	35.24	0.020	-27.16	0.427	-161.42
3.0 GHz	0.896	157.24	3.37	33.06	0.020	-28.02	0.433	-162.64
3.2 GHz	0.896	154.06	3.16	28.74	0.019	-29.57	0.446	-165.13
3.4 GHz	0.896	150.87	2.98	24.44	0.019	-30.88	0.457	-167.69
3.6 GHz	0.896	147.66	2.82	20.16	0.018	-31.95	0.468	-170.31
3.8 GHz	0.897	144.41	2.68	15.89	0.018	-32.76	0.478	-173.00
4.0 GHz	0.897	141.10	2.56	11.61	0.017	-33.30	0.488	-175.77
4.2 GHz	0.897	137.72	2.45	7.33	0.017	-33.55	0.497	-178.61
4.4 GHz	0.897	134.26	2.35	3.03	0.017	-33.50	0.505	178.47
4.6 GHz	0.897	130.71	2.26	-1.31	0.016	-33.18	0.512	175.46
4.8 GHz	0.896	127.06	2.17	-5.68	0.016	-32.58	0.518	172.36
5.0 GHz	0.896	123.30	2.10	-10.09	0.016	-31.74	0.524	169.16
5.2 GHz	0.896	119.42	2.04	-14.57	0.016	-30.72	0.529	165.86
5.4 GHz	0.896	115.41	1.98	-19.10	0.016	-29.60	0.534	162.44
5.6 GHz	0.896	111.26	1.92	-23.71	0.016	-28.46	0.537	158.89
5.8 GHz	0.895	106.97	1.87	-28.40	0.017	-27.41	0.540	155.20
6.0 GHz	0.895	102.53	1.82	-33.19	0.017	-26.54	0.543	151.36

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Typical Package S-Parameters for CGH40010
(Small Signal, V_{DS} = 28 V, I_{DQ} = 500 mA, angle in degrees)

Frequency	Mag S11	Ang S11	Mag S21	Ang S21	Mag S12	Ang S12	Mag S22	Ang S22
500 MHz	0.914	-135.02	18.58	103.70	0.020	18.36	0.300	-126.80
600 MHz	0.909	-143.57	15.88	98.05	0.020	13.67	0.302	-133.51
700 MHz	0.906	-150.23	13.83	93.33	0.021	9.90	0.304	-138.40
800 MHz	0.904	-155.61	12.23	89.23	0.021	6.77	0.307	-142.08
900 MHz	0.903	-160.09	10.95	85.56	0.021	4.08	0.311	-144.94
1.0 GHz	0.902	-163.93	9.91	82.21	0.021	1.71	0.314	-147.23
1.1 GHz	0.901	-167.29	9.04	79.09	0.021	-0.41	0.319	-149.10
1.2 GHz	0.901	-170.29	8.31	76.15	0.021	-2.35	0.323	-150.69
1.3 GHz	0.900	-173.00	7.69	73.35	0.021	-4.12	0.328	-152.07
1.4 GHz	0.900	-175.50	7.15	70.66	0.021	-5.78	0.333	-153.29
1.5 GHz	0.900	-177.81	6.69	68.07	0.021	-7.32	0.338	-154.41
1.6 GHz	0.900	-179.98	6.27	65.54	0.021	-8.77	0.344	-155.44
1.7 GHz	0.900	177.96	5.91	63.08	0.020	-10.15	0.349	-156.43
1.8 GHz	0.899	176.00	5.59	60.67	0.020	-11.45	0.355	-157.38
1.9 GHz	0.899	174.12	5.30	58.30	0.020	-12.68	0.361	-158.30
2.0 GHz	0.899	172.31	5.04	55.97	0.020	-13.85	0.366	-159.22
2.1 GHz	0.899	170.54	4.80	53.67	0.020	-14.96	0.372	-160.14
2.2 GHz	0.900	168.83	4.58	51.40	0.020	-16.01	0.378	-161.06
2.3 GHz	0.900	167.15	4.39	49.16	0.019	-17.01	0.384	-161.99
2.4 GHz	0.900	165.49	4.21	46.94	0.019	-17.95	0.390	-162.93
2.5 GHz	0.900	163.87	4.04	44.73	0.019	-18.85	0.396	-163.88
2.6 GHz	0.900	162.26	3.89	42.54	0.019	-19.69	0.402	-164.86
2.7 GHz	0.900	160.66	3.75	40.37	0.019	-20.48	0.407	-165.85
2.8 GHz	0.900	159.08	3.62	38.21	0.019	-21.21	0.413	-166.86
2.9 GHz	0.900	157.51	3.50	36.05	0.018	-21.89	0.418	-167.89
3.0 GHz	0.900	155.93	3.39	33.91	0.018	-22.52	0.424	-168.95
3.2 GHz	0.900	152.79	3.18	29.65	0.018	-23.61	0.435	-171.12
3.4 GHz	0.900	149.64	3.00	25.40	0.017	-24.48	0.445	-173.38
3.6 GHz	0.900	146.45	2.85	21.17	0.017	-25.11	0.454	-175.73
3.8 GHz	0.900	143.23	2.71	16.93	0.017	-25.51	0.463	-178.17
4.0 GHz	0.900	139.94	2.58	12.69	0.017	-25.67	0.471	179.30
4.2 GHz	0.900	136.58	2.47	8.43	0.016	-25.60	0.479	176.67
4.4 GHz	0.899	133.14	2.38	4.15	0.016	-25.32	0.486	173.94
4.6 GHz	0.899	129.61	2.29	-0.17	0.016	-24.85	0.492	171.12
4.8 GHz	0.899	125.97	2.21	-4.53	0.016	-24.24	0.498	168.18
5.0 GHz	0.898	122.23	2.13	-8.94	0.016	-23.54	0.503	165.13
5.2 GHz	0.898	118.36	2.07	-13.41	0.016	-22.80	0.507	161.96
5.4 GHz	0.898	114.36	2.01	-17.95	0.017	-22.11	0.511	158.66
5.6 GHz	0.897	110.22	1.95	-22.56	0.017	-21.54	0.514	155.22
5.8 GHz	0.897	105.94	1.90	-27.26	0.018	-21.16	0.517	151.63
6.0 GHz	0.897	101.51	1.86	-32.04	0.019	-21.04	0.519	147.87

To download the s-parameters in s2p format, go to the CGH40010 Product Page and click on the documentation tab.

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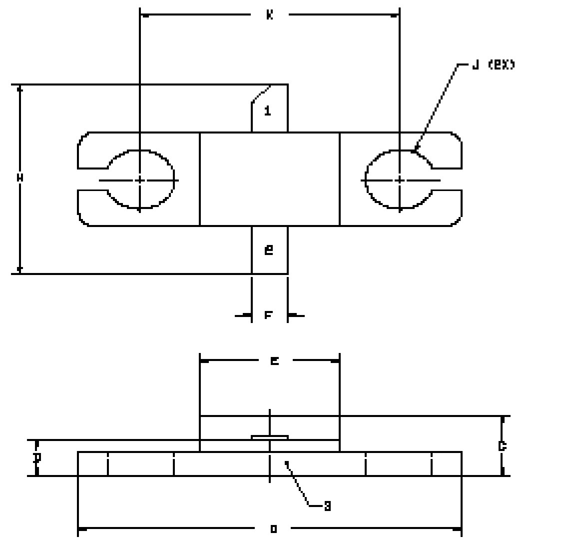
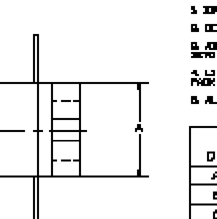
Product Dimensions CGH40010F (Package Type — 440166)





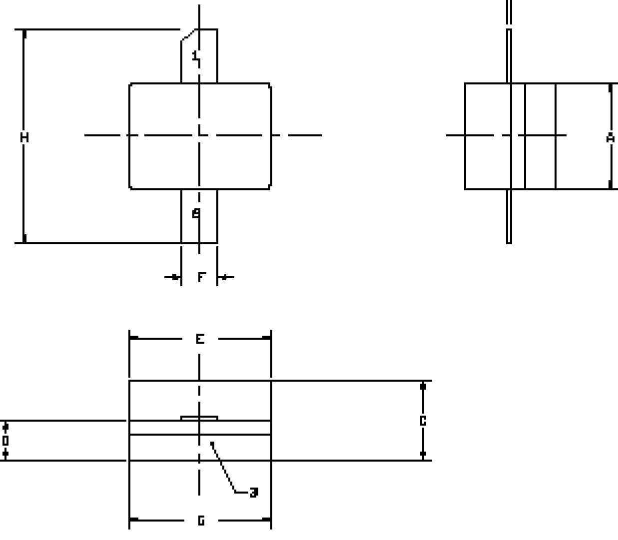
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.020" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF THE PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.
5. ALL PLATED SURFACES ARE NI/AU

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.155	0.165	3.94	4.18
B	0.004	0.006	0.10	0.15
C	0.115	0.135	2.92	3.43
D	0.057	0.067	1.45	1.70
E	0.195	0.205	4.95	5.21
F	0.045	0.055	1.14	1.40
G	0.545	0.555	13.84	14.09
H	0.280	0.360	7.11	9.14
J	ø .100		2.54	
K	0.375		9.53	

PIN 1. GATE
PIN 2. DRAIN
PIN 3. SOURCE

Product Dimensions CGH40010P (Package Type — 440196)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
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4. LID MAY BE MISALIGNED TO THE BODY OF THE PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.
5. ALL PLATED SURFACES ARE NI/AU

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.155	0.165	3.94	4.19
B	0.003	0.006	0.10	0.15
C	0.115	0.135	2.92	3.17
D	0.057	0.067	1.45	1.70
E	0.195	0.205	4.95	5.21
F	0.045	0.055	1.14	1.40
G	0.195	0.205	4.95	5.21
H	0.280	0.360	7.11	9.14

PIN 1. GATE
PIN 2. DRAIN
PIN 3. SOURCE

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Product Ordering Information

Order Number	Description	Unit of Measure	Image
CGH40010F	GaN HEMT	Each	
CGH40010P	GaN HEMT	Each	
CGH40010F-TB	Test board without GaN HEMT	Each	
CGH40010F-AMP	Test board with GaN HEMT installed	Each	

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