ENERGY DETECTION FROM VHF TO X-BAND USING SOFTWARE DEFINED RADIO TECHNOLOGY

by

Bruce Alistair van Niekerk

Baccalaureus Technologiae in Electrical Engineering,

Cape Peninsula University of Technology

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Supervisor:

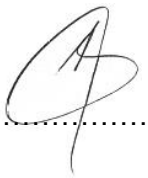
PROF MOHAMED TARIQ EKERAMODIEN KAHN

Co-supervisor:

DR VIPIN BALYAN

Declaration

I, Bruce Alistair van Niekerk, declare that the contents of this thesis represent my own unaided work, and that the thesis has not previously been submitted for academic examination towards any qualification. Furthermore, it represents my own opinions and not necessarily those of the Cape Peninsula University Technology.

Signed:  Date: 25/08/2022

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Dedication

I would like to dedicate this thesis to my dad Anthony Brian van Niekerk who passed away in 2014. I know you would be so proud of what I have achieved.

Abstract

The software-defined radio (SDR) is a wireless exchange system that performs analog to digital (ADC) translation directly to the carrier signal instead of shifting the carrier signal down to a baseband signal through analog circuits. The benefit of this is that after digitization various code can be performed to demodulate amplitude, frequency and phase modulated signals. The drawback to this is that higher carrier frequencies require faster ADCs which can be expensive and consume additional power which is the background to the problem statement. Also, in this research, to mitigate the necessity of fast and power-hungry ADCs for direct higher frequency digitization, an alternative front-end receiver architecture was studied. This alternative proposed design will permit the mobile SDR to perceive energy of frequencies greater than a low-priced SDR and suppress the image occurrence. The image occurrence is the unique signal that occurs at the frequency RF±2IF. The consequence of the image occurrence incident to the front-end of the receiver at the precise period as the carrier signal produces the same IF after the down conversion process and can't be removed by any form of filter.

The research was undertaken with a system level approach by evaluating receiver architectures that can translate the carrier signal down to a baseband signal where a new design was proposed that is suitable for the mobile SDR environment and thus can be used in conjunction with SDR technology. The proposed design with the various RF components that constitutes the design were established and the limits of each component were defined.

Cadence® Applied Wave Research (AWR®) Visual System Simulator™ (VSS) V16 software suite was used to develop a base model for each RF component after which the conceptualized down converter with its suitable specifications were derived.

The simulations presented in this research also demonstrated that the proposed design could observe frequencies and suppress the image occurrence from VHF to X-band. This was attained by increasing the linearity of the RF chain and not using filters. These features fundamentally steered the design to have a reduced circuit footprint and will ultimately consume less power compared to expensive SDR's using fast sampling ADCs to perceive higher frequencies.

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List of Abbreviations

Abbreviation	Definition
ADC	Analog-to-Digital Converter
AM	Amplitude Modulation
AMP	Amplifier
AWR	Applied Wave Research
BJT	Bipolar Junction Transistor
BPF	Bandpass Filter
BSPK	Binary Phase-Shift Keying
BW	Bandwidth
CMOS	Complementary Metal–Oxide–Semiconductor
CP	Charge Pump
DAC	Digital-to-Analog Converter
DAS	Direct Analog Synthesis
dB	Decibel
DC	Direct Current
DCO	Digitally Controlled Oscillator
DDS	Direct Digital Synthesis
DF	Digital Filter
DN	Down Signal
DPFD	Digital Phase Frequency Detector
DSB	Double-Sideband
DSP	Digital Signal Processing
DUT	Device Under Test
EM	Electromechanical
EMI	Electromagnetic Interference
F	Farad
FET	Field Effect Transistor
FM	Frequency Modulation
GA	Available Power Gain
GHz	Gigahertz
GT	Transducer Power Gain
GTU	Unilateral Transducer Power Gain
GZRT	Zero-Reflection Transducer Gain
HCMOS	High-Speed Complementary Metal Oxide Semiconductor
Hz	Hertz
IAS	Indirect Analog Frequency Synthesis
IC	Integrated Circuit
IDS	Indirect Digital Frequency Synthesis
IF	Intermediate Frequency
IIP	Input Intercept Point
IM2	Second Order Distortion
IM3	Third Order Distortion
IM4	Forth Order Distortion
IM5	Fifth Order Distortion

IMD	Intermodulation Distortion
IP1dB	Input Compression Point
IP2	Second Order Intercept Point
IP3	Third-Order intercept Point
IQ	In-Phase/Quadrature
IR	Image Reject
IRR	Image Reject Ratio
kHz	kilohertz
LF	Loop Filter
LNA	Low-Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
LVCMOS	Low-Voltage Complementary Metal–Oxide–Semiconductor
MAM	Metal to Air to Metal
MEMS	Micro Electro-Mechanical Systems
MHz	Megahertz
MIM	Metal to Insulator to Metal
MMIC	Monolithic Microwave IC
NF	Noise Figure
OCXO	Oven Controlled Crystal Oscillator
OIP	Output Intercept Point
OP1dB	Output Compression Point
P1dB	Compression Point
PCB	Printed circuit board
PFD	Phase Frequency Detector
PIN	Positive-Intrinsic-Negative
PLL	Phase-Locked Loop
PM	Phase Modulation
PN	P-N Junction
PPM	Parts Per Million
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RC-CR	Resistor Capacitor- Capacitor Resistor
RDS	Drain-Source On Resistance
RF	Radio Frequency
RFSW	Radio Frequency Switch
RL	Return Loss
RMS	Root Mean Square
SAW	Software-Defined radio
SDR	Surface-Acoustic Wave
SNR	Signal-to-Noise Ratio
SPDT	Single Pole Double Throw
SSB	Single-Sideband Modulation
TCXO	Temperature Compensated Crystal Oscillator
TDC	Time-to-Digital Converter
TEM	Transverse Electromagnetic
TSC	Temperature Sensor Circuitry
TTL	Transistor–Transistor Logic

UP	Up Signal
V	Volt
VCO	Voltage Controlled Oscillator
VCTCXO	Voltage Controlled, Temperature Compensated Crystal Oscillator
VCXO	Voltage Controlled Crystal Oscillator
VHF	Very High Frequency
VSS	Visual System Simulator
VSWR	Voltage Standing Wave Ratio
XO	Crystal Oscillator

Chapter 1

Introduction

1.1 Overview of the Software Defined Radio and Front-End Receiver

The idea of a software defined radio also known as SDR was conceived by Joseph Mitola in 1991. The purpose of the SDR is to have most of the receiver/transmitter sections implemented and processed through software in the digital domain, after an analogue-to-digital (ADC) or digital-to-analogue (DAC) converter. The ideal configuration is to have the SDR placed directly after the antenna as in Figure 1.1, but because of the limitations of the ADC/DAC's the desired RF signal first has to be down converted to a lower intermediate frequency (IF) so that the ADC/DAC can sample and digitize the IF signal to a baseband signal for processing (Mitola, 1992).

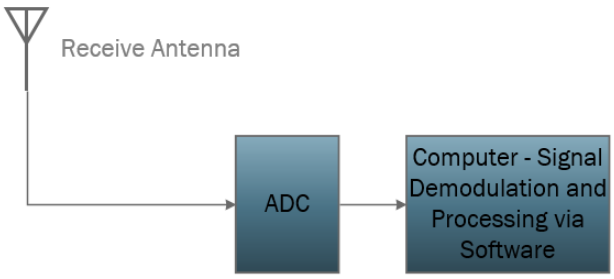

Figure 1.1: Ideal Software Defined Radio

The subsystem that down converts the desired RF signal to the IF signal is referred to as the RF front-end. The RF front-end as seen in Figure 1.2 is also known as the analogue-to-baseband part of a receiver (Li, 2008). The general components of this subsystem Figure 1.2 that follows directly after the antenna is:

- Band pass filter (BPF): Component that limits the input signal to what is known as a band limited signal. It also isolates the mixer from the antenna and prevents the mixer from radiating through to the antenna.
- Low Noise Amplifier (LNA): Component that amplifies the band limited signal by adding minimal noise.
- Local Oscillator (LO): Component which is used as a reference signal.
- RF Mixer: Component that mixes the band limited signal with the reference signal to a lower usable frequency that the ADC can sample and correctly digitize for processing.

(Carr, 2000:6,37-39).

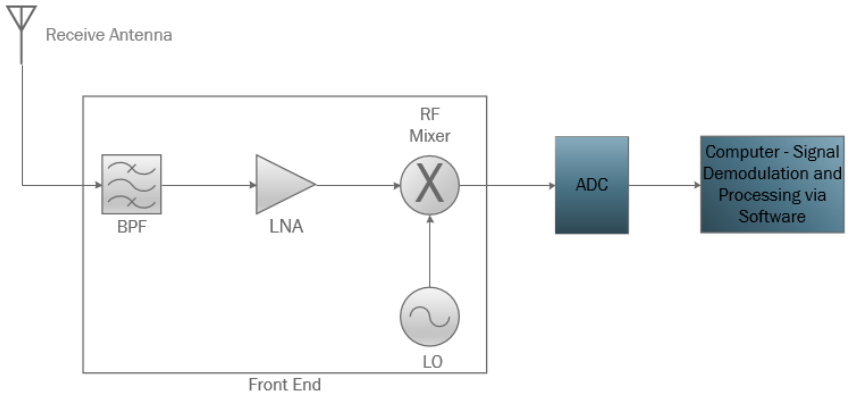

Figure 1.2: General Software Defined Radio

1.2 Background to the Research Problem

There are many front-end architectures to provide the IF signal to the ADC. The concern with most of the front-end or receiver architectures is that there is a signal at a specific frequency that will always interfere with the desired frequency after down conversion is done. This specific frequency is known as the image frequency as seen in Figure 1.3 and can't be filtered out by any type of filter once is it is down converted with the desired frequency (Phang, 2002:1-3).

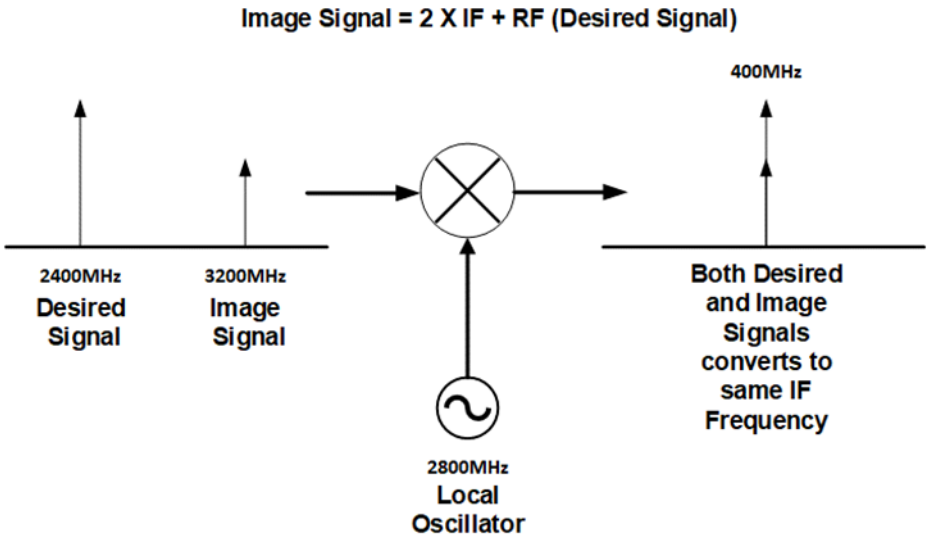

Figure 1.3: Image Problem

The receiver architectures that suppress this image frequency is the:

- Homodyne/ Direct Conversion/ Zero IF Receiver (Razavi, 1996:15-18).
- Super Heterodyne/ Heterodyne Receiver (Razavi, 1996:18).
- Low IF Receiver (Carrera, 2007:13).
- Hartley Image Reject Receiver (Razavi, 1996:18).
- Weaver Image Reject Receiver (Razavi, 1996:19).

All these different receiver architectures have their methods of dealing with the image frequency, but only one receiver architecture is best suited for the mobile SDR environment.

1.3 Objectives of the Research and Expected Outcome

The research purpose is to investigate and develop a non-complex, low power and low-cost RF front-end down converter for the mobile SDR environment. The objective of the research is to determine the suitable:

- Receiver architecture for the SDR environment.
- Low noise amplifier for the SDR environment.
- Mixer topology for the SDR environment.
- Local oscillator for the SDR environment.
- RF switch for the SDR environment.
- Quadrature coupler for the SDR environment.

The expected outcome is to demonstrate through computer aided software that a non-complex, low power and low-cost RF front-end down converter is attainable and can provide a suitable IF for the SDR to use for energy detection.

1.4 Research and Design Methodology

To achieve the objectives the following research and design methodology is followed:

- An investigation into receiver architectures.
- An investigation into low noise amplifiers.
- An investigation into mixer topologies
- An investigation into local oscillators.
- An investigation into RF switch.
- An investigation into Quadrature coupler
- Determine the suitable IF for the SDR environment.
- Design and simulate the suitable RF front-end down converter for the SDR environment.

1.5 Delineation of the research

The research investigation is to develop a RF front-end down converter that extends the common SDR range from 2GHz up to 12GHz. Therefore, the performance of the SDR will not be investigated and only the ability of the down converter to accept input signals from 2GHz-12GHz and to provide a suitable IF to the SDR is examined.

1.6 Signification of the Research

The ability of an SDR's to sample and convert the analogue signal to the digital where it can be demodulated depends on the capabilities of the ADC of the SDR. Therefore, the higher the frequency operation of the SDR, the more capable the ADC section needs to be of the SDR. The consequence is higher power consumption and price.
This research investigates an alternative to extend the frequency range of SDR's without implementing faster ADC's that are costly and consume more power to sample and convert signals from analogue to digital domain for demodulation through software.

1.7 Thesis Framework

The rest of the thesis consists of:

- **Chapter 2** which compares receiver architectures to select the suitable architecture for the SDR environment.
- **Chapter 3** particularises on the LNA to allow the selection of suitable component for the front-end receiver.
- **Chapter 4** particularises on the RF mixer to allow selection of suitable component for the front-end receiver.
- **Chapter 5** particularises on the local oscillator to allow selection of suitable component for the front-end receiver.
- **Chapter 6** particularises on the RF switch to allow selection of suitable component for the front-end receiver.
- **Chapter 7** particularises on the RF hybrid coupler to allow selection of suitable component for the front-end receiver.
- **Chapter 8** details the down converter design and simulation.
- **Chapter 9** details the conclusion and future work for this research.

Chapter 2

Receiver Architecture for the Mobile SDR Environment

2.1 Introduction

The mobile SDR environment requires a receiver that is compact and uses very litter power to operate. Therefore, before a receiver can be considered, chapter 2 will discuss the history of receiver architectures, their advantages and disadvantages, to allow an optimum receiver to be chosen for the mobile SDR environment.

2.2 Homodyne/Direct-conversion/Zero-IF Receiver

This category of frequency translation was first implemented in 1924 in a single vacuum-tube receiver, then again in 1947 for a carrier-based telephony system. It was only until 1980 that this receiver architecture was used in a radio-paging receiver. This architecture is distinctive of having the LO in sync with the desired RF to create a zero-frequency baseband signal (Abidi, 1995:1401). This process eliminates the need for a BPF filter before and after the mixer as seen in Figure 2.1. The image frequency is mixed down to zero. Consequently, the image and desired RF can be distinguished by their amplitude (Spiridon, 2016:16).
Also, in Figure 2.1 the quadrature of the LO is used. This is to detect frequency and phase modulation schemes (Razavi, 1996:17-18) and to prevent negative-frequency half-channels from folding over to the positive-frequency half-channels after the down conversation (Abidi, 1995:1401). The negative frequency half-channels are not used and filtered out with the LPF centred on 0Hz (Abidi, 1995:1401).
This receiver architecture therefore has an advantage of eliminating the BPF's before and after the mixers. Namely the image-reject filter and channel-select filter Figure 2.1, which are expensive and difficult to implement (Spiridon, 2016:16).
This receiver architecture also has its disadvantages. Because the desired frequency is frequency translated to a lower baseband signal, presents a great deal of interference on the desired signal at baseband level, even though the image is completely non-existence after the LPF. Other disadvantages are listed below:

- LO-RF feedback: The LO signal interferes with the RF port when the LO-RF isolation is not satisfactory. The LNA will then amplify this interfering signal called direct current (DC) which consequently saturates the LNA and therefore restricts the desired RF signal from being enhanced (Razavi, 1996:15-16).

- Even-order distortions: Since RF mixers are non-linear devices, they produce intermodulation distortion (IMD) products when the input RF port and LO port signals mix, giving a range of even and order harmonic products. The 3rd order products are only odd order products of high concern, but only regarding IP3 of the receiver chain. On the other hand, all the even order products can add to the baseband signal at DC and is known as the IP2 of DC receivers (John W. M. Rogers, Calvin Plett, 2013:93).
- Flicker noise/1/f noise: This is a type of noise that exists in all electronic components adds the DC offset and is inversely proportion with frequency (Razavi, 1996:17-18).

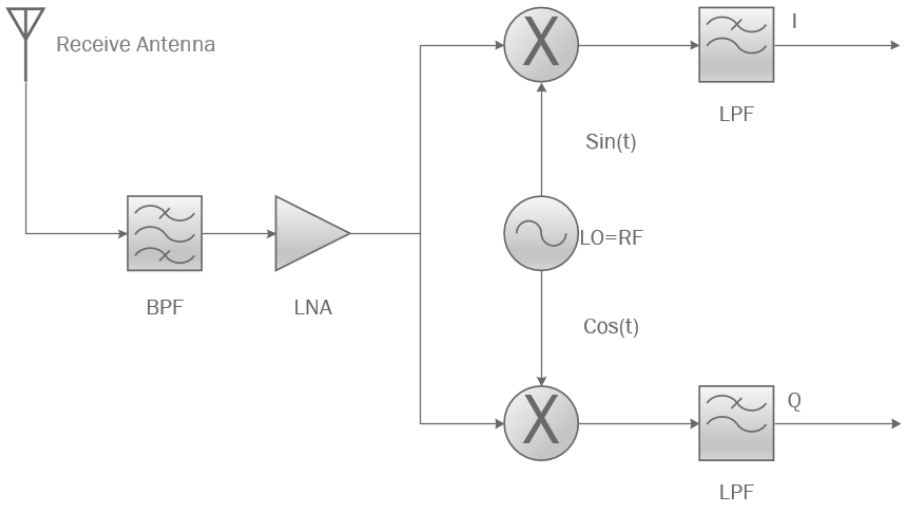

Figure 2.1: Homodyne Receiver

2.3 Super Heterodyne/Heterodyne Receiver

In 1918, Edwin Howard Armstrong first implemented this receiver architecture (Spiridon, 2016:14)

This receiver architecture in Figure 2.2 initiates by band limiting the desired RF signal into the LNA which amplifies and adds minimum noise to the band limited signal. The image signal is then attenuated from the band limited signal by the image-reject BPF. When the band limited signal is mixed with the LO through the RF mixer, results in the wanted IF and many other unwanted IMD products. The channel-select BPF removes the IMD products after the RF mixer. The stages to follow are usually the LO quadrature stage to allow phase and frequency modulation detection as in the homodyne receiver (Cruz, Gomes and Carvalho, 2010:496).

The advantage of having this arrangement is that the receiver has a very high ability to select the desired RF signal from a band limited signal (receiver selectivity) and has a high ability to detect weak signals (receiver sensitivity). Both high receiver selectivity and high receiver sensitivity cannot be achieved simultaneously therefore a trade-off must be made (Cruz, Gomes and Carvalho, 2010:496).

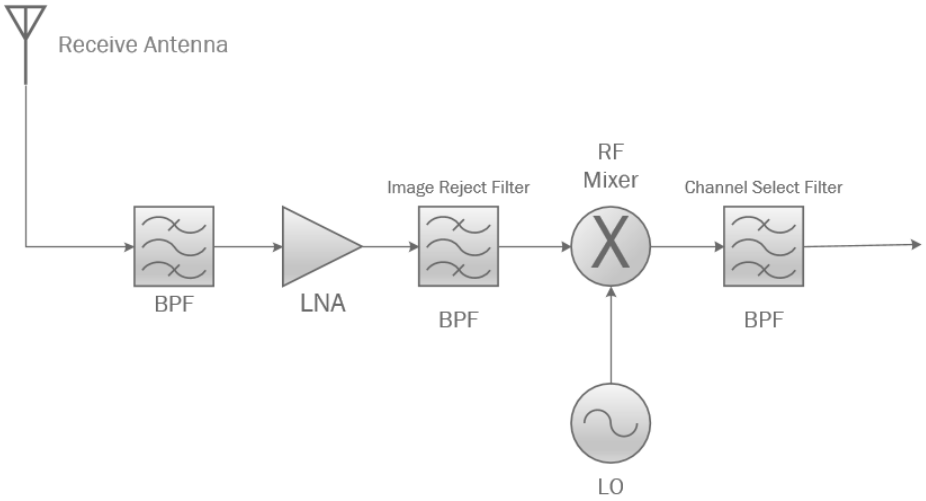

Figure 2.2: Heterodyne Receiver

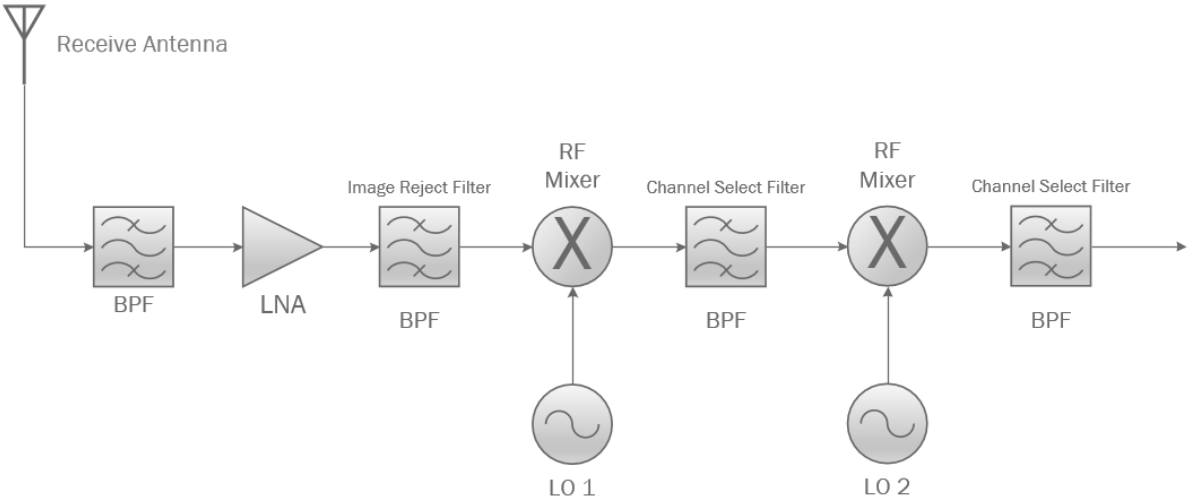

Figure 2.3: Super Heterodyne Receiver

High receiver sensitivity and thus good image rejection is achieved by allowing the IF signal to be as high as possible in frequency, away from the desired RF signal. To achieve this, the channel-select BPF after the RF mixer as in Figure 2.2**,** requires a high Q-factor because of the higher frequency. A high Q factor filter is expensive, difficult to implement, and has a higher insertion loss.

High receiver selectivity is achieved by allowing the IF signal as low as possible, close to the desire RF which allows for relaxed requirements for the channel-select BPF, the down side to this is the high Q actor of the image-reject BPF Figure 2.2 before the mixer must have a high Q factor because of the narrow bandwidth requirement. High Q-factor BPF's are difficult to implement and results in bad image suppression.

Towards satisfying both high sensitivity and high selectivity simultaneously, the double super heterodyne receiver was created as seen in Figure 2.3. The first LO frequency translates the desired RF signal to a higher IF. This satisfies the sensitivity parameter and the second LO

frequency translates the higher IF signal to a lower IF signal which satisfies the sensitivity parameter (Razavi and Behzad, 1998:124-128).

2.4 Low IF Receiver

The concept of this receive architecture was to eliminate the image-reject filter like the homodyne receiver, but still have the selectivity and sensitivity as the super heterodyne receiver (Puvaneswari and Sidek, 2004:2).

The process as in Figure 2.4 initiates by filtering the input signal to a band limited signal that is inputted to the LNA. This bandlimited signal is provided to the LO quadrature to provide phase and frequency modulation detection. Because the IF is lower than normal in the range of kilohertz, the use of a poly-phase filter Figure 2.4 is needed for image rejection and channel selection. The poly-phase BPF has an asymmetric frequency response and therefore filters all negative frequencies(Spiridon, 2016:20).

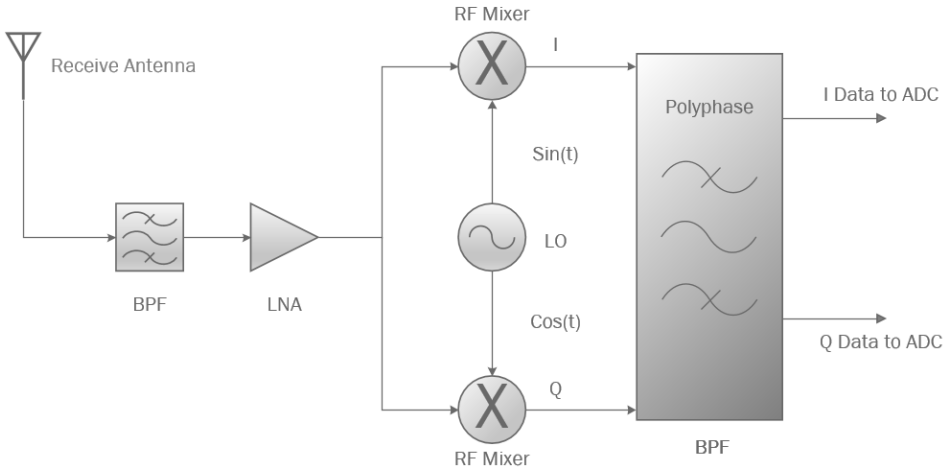

Figure 2.4: Low IF Receiver

The advantage of having this architecture is that there is no LO self-mixing, DC-offset and flick or 1/f noise influences (Puvaneswari and Sidek, 2004:2).

The disadvantage of using this architecture is that the wanted IF signal in the kHz is very close to the image signal and therefore needs a complex poly-phase BPF to filter out the unwanted image signal. This consequence in that there is now very little room for I/Q balance mismatch (Puvaneswari and Sidek, 2004:3).

2.5 Image Reject Receivers

The previous receive architectures all rely on passive components such as filters to remove the image frequency prior the frequency translation process by the RF mixer to the respective IF and baseband signals. The following receive architectures rely on changing the phase of the band limited signal so that when they combine, the wanted signals that are in-phase increases in power, while the unwanted image signals that are out-of-phase cancel out each other (Idachaba and Orovwode, 2011:201).

2.5.1 Hartley Image Reject Receiver

The process as in Figure 2.5 initiates by filtering the input signal to a band limited signal that is inputted to the LNA. This amplified band limited signal then becomes down converted by the quadrature of the LO for phase and frequency modulation detection. This down converted signal consisting of I and Q signals gets filtered by an LPF to limit higher frequencies from entering the stages to follow. Then the I signal is phase shifted by 90° while the Q signal is not shifted at all. Lastly, the I and Q signals combine to form a suppressed unwanted signal and an unambiguous-wanted signal.

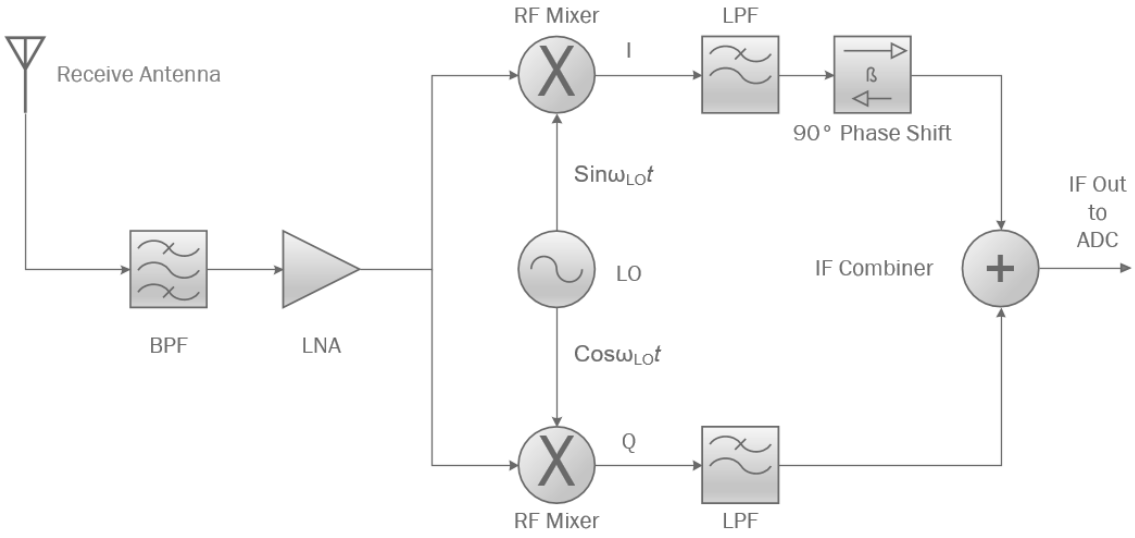

Figure 2.5: Hartley Image Reject Receiver

The advantage of using this architecture is that the component count is reduced with no image reject BPF's.

The disadvantage of this architecture is that the phase shift section and the LO must have decent phase and amplitude stability to sufficiently suppress the unwanted signal. Because of analogue component tolerance, it is difficult to implement an accurate 90° phase shift, thus a different approach is achieved by implementing 45° phase change on both the I and Q signal

paths via a Resistor Capacitor- Capacitor Resistor (RC-CR) network configuration as seen in Figure 2.6. This RC-CR configuration though is affected by temperature variations which impacts the phase and amplitude of the phase shifting (Idachaba and Orovwode, 2011:201-202).

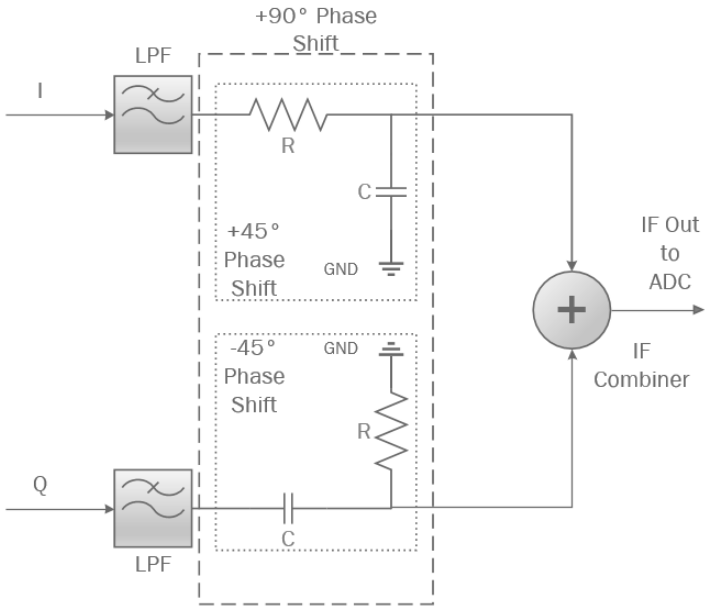

Figure 2.6: Phase Shifting Circuit

2.5.2 Weaver Image Reject Receiver

D.K Weaver invented this receive architecture Figure 2.7 which was to improve on the Hartley image-reject receiver by replacing the RC-CR network with an additional quadrature of the second LO.

This receiver architecture operates the same as the former but with the second LO stage that converts the IF signal from the first LO into I and Q components. These components are added and subtracted to cancel the unwanted and promote the wanted signals.

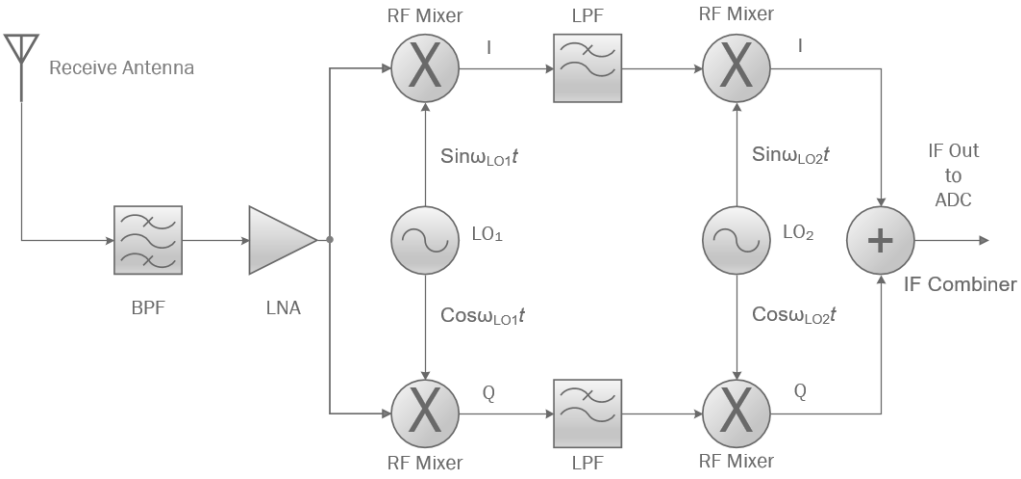

Figure 2.7: Weaver Image Reject Receiver

The benefit of this architecture over the former is more stability under process and temperature variations.

The disadvantage is still the same as the former where the LO needs to be phase and amplitude stable to ensure proper image rejection and because of the addition down-conversion stage, requires more mixers and more power to operate (Idachaba and Orovwode, 2011:202-204).

2.6 Chapter Summary

All receiver architectures use BPF's, which require high Q values for adequate filter-ing. This increases the cost and design complexity of the down converter. Therefore, the least amount of BPF's needs to be allocated to decrease the cost and difficulty of the design. All receiver architectures use LO's, which is essential in translating the higher desired signal into a lower usable frequency. This unfortunately advances the current required for the translation process. Therefore, the least amount of LO's are needed for lower current usage and consequently lowering the cost. Polyphase filters are used in the low-IF architecture to reduce adjacent and channel inference. These filters are more complex and inadvertently consumes more power which rules out the consideration of this receive architecture. In Table 1 the Hartley architecture is seen to use the average amount of components.

Table 2.1: Number of Components

Receiver Architecture	LNA	LO	BPF	LPF	Mixer	Phase Shifter	Combiner	Components
Homodyne	1	1	1	2	2	0	0	7
Super Heterodyne	1	1	3	0	1	0	0	6
Double Super Heterodyne	1	2	4	0	2	0	0	9
Low IF	1	1	2	0	2	0	0	6
Image-reject Hartley	1	1	1	2	2	1	1	9
Image-reject Weaver	1	2	1	2	4	0	1	11

The intention of this investigation is to deliver a receiver font-end for the mobile SDR environment that is simple to develop, uses the minimum amount of current and is less costly to implement. Research was completed in [16] where a front-end was added to the Realtek RTL2832U chipset SDR to extend the range to 6GHz. The proposed design is different where it will as in Figure 2.8 detect signals up to X Band. Include a high IP3 LNA, which will allow the BPF before the LNA to be removed. Include a MMIC I/Q mixer combined with MMIC IF quadrature hybrid combiner to form a Hartley image-reject mixer. This reduces the number of components down to 4 compared to 9 in Table 1. Lastly a RF switch is added, increasing the component count to 5 to allow the switching of the low and high frequency signals to the SDR.

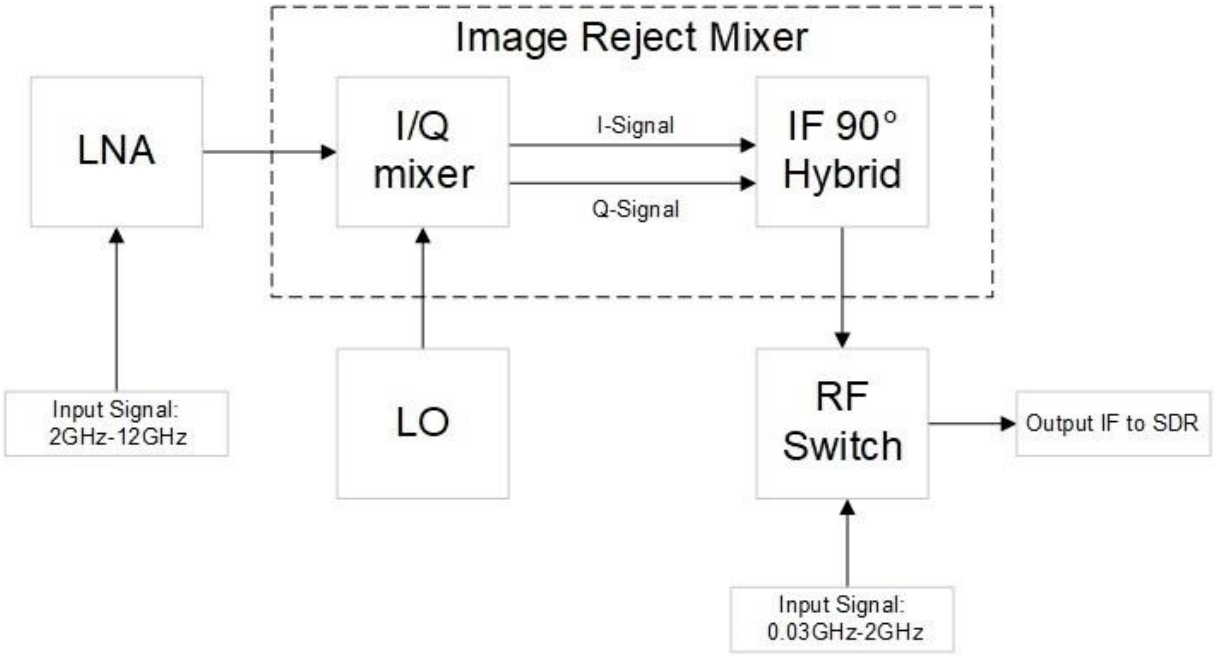

Figure 2.8: Conceptual Front-End for Software Defined Radio

Chapter 3

Lower Noise Amplifier

3.1 Introduction

The low noise amplifier (LNA) is very important as it amplifies small signals and adds as little amount of noise as possible to the desired signal. It is normally the first circuit to sample the incoming signal and it is therefore imperative to know the abilities of the LNA to prevent distortion of the amplified signal. LNA parameters are discussed in this chapter to assist by determining a suitable LNA Integrated Circuit (IC) for the down conversion section of the energy detection module. Parameters to be addressed are:

- Noise
- Gain
- Stability
- Linearity

3.2 Noise Theory

Noise is unavoidable and sets the minimum level at which desired signals can be perceived. It can only be managed by understanding where it originates from. When noise is generated external to components, it is known as extrinsic noise and is reduced either through grounding and shielding of sensitive components. It is generated through magnetic and electric coupling over conduction and radiation. This will not be considered in this chapter.

Intrinsic noise is noise generated inside a component. It can be reduced by using components that are designed in such a way that they essentially generate less noise than usual. Sources of intrinsic noise is thermal, shot, flicker and burst noise. These types of noise sources can further be categorized in 2 groups, namely white and pink noise. Since both thermal and shot noise has constant noise power levels for a given bandwidth, it is considered as white noise. Flicker noise power level decreases with frequency and is considered as pink noise. Burst noise is not considered to be white or pink noise since it is constant up to a cut-off frequency after which the noise behaves inversely with respect to the frequency. All these noise sources add to the overall noise figure of an active component.

(Pozar, 2012)

3.2.1 Shot Noise

Exceeded voltage potential barriers causes current to flow over the potential barriers. This generates shot noise by the non-specific movement of the holes and electrons through this potential barrier, and when the hole-electron pairs recombine after the potential barrier. As discussed in the previous section shot noise has a white noise response as indicated by the RMS shot-noise current Schottky formula. William Bradford Shockley Jr derived the formula in 1928:

$$I_{sh} = \sqrt{2qI\Delta f} \tag{3.1}$$

Where:

- q is the electronic charge.
- I is the DC current flowing through.
- Δf is frequency bandwidth.

(Leach and Member, 1994).

Therefore, it can be foreseen that components where holes and electrons do not move through a potential barrier the component do not generate any shot noise current. An example of this would be the field effect transistor.

(Bretchko, 2014).

3.2.2 Thermal Noise

Free electrons exist around atoms because the bond between the atom and the outer layer of electrons are weak. When any potential is applied to the conductive material the free electrons have enough energy to move to the neighboring atom and electricity is conducted.

Agitation of free electronics creates thermal noise and increases by the increasing the temperature, increasing the resistance of the material or by increasing the bandwidth when measuring noise voltage. William Bradford Shockley Jr discovered this phenomenon in 1928. Since John Bertrand Johnson first measured this phenomenon it is therefore called Johnson noise today. Later Harry Nyquist when approached by John Bertrand Johnson, derived a formula using thermodynamic arguments that the open circuit RMS thermal noise voltage across a resistor is:

$$V_n = \sqrt{4kTR\Delta f} \quad (3.2)$$

Where:

- k is the Boltzmann's constant.
- T is the absolute temperature.
- R is the resistance.
- Δf is frequency bandwidth.

Therefore, it can be foreseen that operating components at lower temperature, minimizing the resistance and bandwidth will improve the RMS thermal noise power. It can also be seen that according to the formula, capacitors and inductors do not add to the thermal noise power.

(Leach and Member, 1994).

3.2.3 Flicker Noise

A certain type of noise power is observed when direct current passes through the joining points of different conductors and resistive material. This noise is known as flicker/contact noise and more noticeable in carbon composition components. Examples are contacts of switches, potentiometers and relays. Components such as the metal film resistor produces the least amount of flicker/contact noise. This type of noise power also originates from the field effect and the bipolar junction transistor.

(Leach and Member, 1994).

Flicker/contact noise power is generated more at lower frequencies and peaks at DC, decreases with power level and generally is insignificant at frequencies above 1kHz.

(Fischer-Cripps, 2015).

3.2.4 Burst Noise

Metallic impurities in potential barriers exist because of substandard fabrication processes. When these barriers are overcome through a voltage potential, burst noise power is generated. It is more prevalent at lower frequencies and is known as pop noise because when these metallic impurities exist in audio amplifier components, it can be perceived as a pop sound on audio systems.

(Motchenbacher and Connelly, 1993).

3.2.5 Sign-Noise-Ratio (SNR)

The signal-noise-ratio refers to the level of the wanted signal at the either the input (S_i) or the output (S_o) with reference to the noise level at the input (N_i) or the output (N_o) as in Figure 3.1.

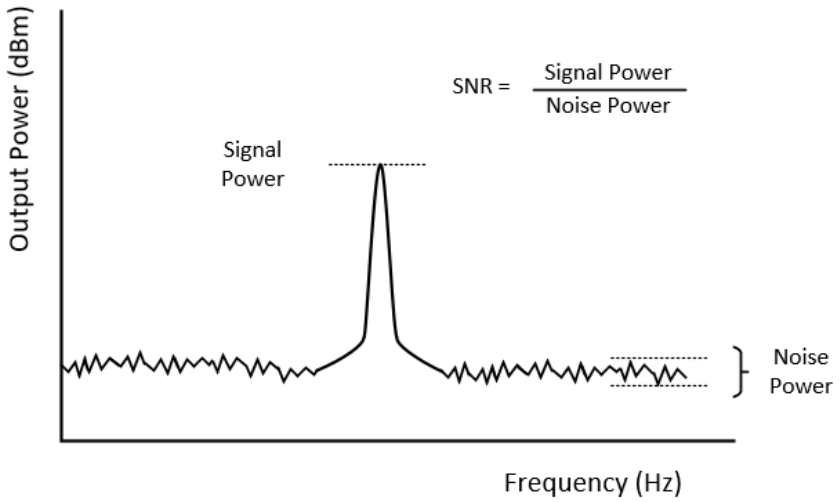

Figure 3.1: Signal to Noise Ratio

(Keysight Technologies, 2019a)

3.2.6 Noise Factor (F)

The noise factor is linear power ratio of the input SNR with the output SNR and is given as:

(Keysight Technologies, 2019a)

$$F = \frac{S_i/N_i}{S_o/N_o} \tag{3.3}$$

3.2.7 Noise Figure (NF)

The noise figure is a logarithmic power ratio in dBs of the noise factor:

$$NF = 10\log_{10} F\,[dB] \tag{3.4}$$

(Keysight Technologies, 2019a)

3.3 Gain Theory

The ability of a DUT to amplify an input signal by a defined amount is known as gain and is the fraction between the output power over input power. In radio frequency circuits this gain is called power gain and is defined in decibels as:

$$G = 10\log_{10}\frac{P_{OUT}}{P_{IN}}[dB] \tag{3.5}$$

This gain varies depending on the input and output impedance presented to the DUT and is given different names.

3.3.1 Operating Power Gain (G_P)

The operating power gain is the fraction between the power transferred to the load by the power applied to the DUT. Which mean means that it is the gain calculated that is not depended on the impedance of the input (Z_s). It is only depended on the impedance of the output (Z_L) because DUT impedance at the input is matched to the source impedance of the input. It is calculated as:

$$G_P = \frac{P_{LOAD}}{P_{INPUT}} = \frac{1}{1-|\Gamma_{IN}|^2} * |S_{21}|^2 * \frac{1-|\Gamma_L|^2}{|1-S_{22}*\Gamma_L|^2} \tag{3.6}$$

$$\Gamma_{IN} = S_{11} + \frac{S_{12}*S_{21}*\Gamma_L}{1-S_{22}-\Gamma_L} \tag{3.7}$$

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{3.8}$$

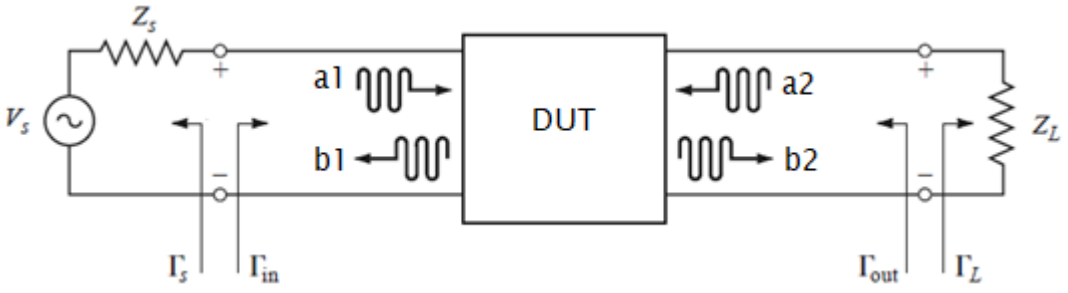

Figure 3.2: Generalized Two Port Network

As in Figure 3.2 a_1 is the incident wave to the DUT, a_2 is the reflected wave from the load, b_1 is the reflected wave from the DUT and b_2 is the reflected wave from the load. Therefore:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \tag{3.9}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \tag{3.10}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \tag{3.11}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \tag{3.12}$$

$$b_1 = S_{11} * a_1 + S_{12} * a_2 = S_{11} * a_1 + S_{12} * \Gamma_L * b_2 \tag{3.13}$$

$$b_2 = S_{21} * a_1 + S_{22} * a_2 = S_{21} * a_1 + S_{22} * \Gamma_L * b_2 \tag{3.14}$$

(Pozar, 2012)

3.3.2 Available Power Gain (GA)

The available power gain is the fraction between the power accessible from the DUT by the power accessible from the source. Which means that the gain is calculated where the impedance of the source (Z_S) is taken into consideration and not the impedance of the load (Z_L), because the DUT impedance at the output is matched to the impedance at the load. It is calculated as:

$$G_A = \frac{P_{AVAILABLE\ FROM\ DUT}}{P_{AVAIALBLE\ FROM\ SOURCE}} = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2} * |S_{21}|^2 * \frac{1}{1 - |\Gamma_{OUT}|^2} \tag{3.15}$$

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0} \tag{3.16}$$

$$\Gamma_{OUT} = S_{22} + \frac{S_{11} * S_{21} * \Gamma_S}{1 - S_{11} * \Gamma_S} \tag{3.17}$$

(Pozar, 2012)

3.3.3 Transducer Power Gain (GT)

The transducer power gain is the fraction between the power transferred to the load by the power accessible from the source. Which means that the gain is calculated where both the source (Z_S) and the load (Z_L) impedances are taken into consideration, because the DUT impedance of the input and output is not matched to the impedance of the source and load.

$$G_T = \frac{P_{LOAD}}{P_{AVAIALBLE\ FROM\ SOURCE}} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2} * |S_{21}|^2 * \frac{1-|\Gamma_L|^2}{|1-\Gamma_{OUT} * \Gamma_L|^2} \quad (3.18)$$

$$\Gamma_{OUT} = S_{22} + \frac{S_{12} * S_{21} * \Gamma_S}{1-S_{11}-\Gamma_S} \quad (3.19)$$

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0} \quad (3.20)$$

(Pozar, 2012)

3.3.4 Zero-Reflection Transducer Gain (GZRT)

The zero-reflection transducer gain is the fraction between the input and output reflection and is matched to nil and the gain is then reduced to:

$$G_{ZRT} = |s_{21}|^2 \quad (3.21)$$

(Pozar, 2012)

3.3.5 Unilateral Transducer Power Gain (GTU)

The unilateral transducer power gain is the fraction where $S_{12} = 0$ or considerably small. It is calculated as:

$$G_{TU} = \frac{|S_{21}|^2 * (1-|\Gamma_S|^2) * (1-|\Gamma_L|^2)}{|1-S_{11} * \Gamma_S|^2 * |1-S_{22} * \Gamma_L|^2} \quad (3.22)$$

(Pozar, 2012)

3.3.6 Maximum Available Power Gain

This is the gain when both the output and the input impedance of the amplifier is source and load impedance. In this scenario the gain is not depended on the source or the load impedance. Gain is calculated from the datasheet as:

$$Gain(dB) = 20\log_{10}(|S_{21}|) \tag{3.23}$$

3.4 Stability Theory

In the radio frequency environment, amplifier ports (Γ_{IN} and Γ_{OUT}) are attached with sources (Γ_S) that have varied impedances and are connected to loads (Γ_L) that have impedances other than the characteristic impedance of 50Ω. The ability of an amplifier to remain linear when these various input (Γ_S) and output (Γ_L) impedances are applied to is called the stability of the amplifier. The stability of an amplifier can be determined by using the s-parameters of the amplifier at the specific frequency of operation.

(Pozar, 2012)

3.4.1 Rollet's Stability Condition

The Rollet's condition is the first step to determine if an amplifier is stable. When K > 1 and |Δ|< 1, an amplifier is said to be unconditionally stable. This means any input (Γ_S) and output (Γ_L) impedance can be applied to the amplifier for the specific frequency of the s-parameters. K and |Δ| are calculated as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2 * |S_{12} * S_{21}|} \tag{3.24}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \tag{3.25}$$

(Pozar, 2012)

3.4.2 Stability Circles

The stability circles, illustrated on a Smith Chart are used to identify what values of the input (Γ_S) and output (Γ_L) impedances at the specific frequency of the s-parameters, will an amplifier be unstable and oscillate. The output stability circle is calculated as:

$$C_L = \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \quad (3.26)$$

$$R_L = \left|\frac{S_{12} * S_{21}}{|S_{22}|^2 - |\Delta|^2}\right| \quad (3.27)$$

The input stability circle is calculated as:

$$C_S = \frac{(S_{11} - \Delta S_{22}^*)^*}{|S_{11}|^2 - |\Delta|^2} \quad (3.28)$$

$$R_S = \left|\frac{S_{12} * S_{21}}{|S_{11}|^2 - |\Delta|^2}\right| \quad (3.29)$$

(Pozar, 2012)

3.4.3 Mu-Stability Test (Mu)

The mu-stability test is the easiest way to check if an amplifier will oscillate with different Γ_S and Γ_L impedances because there is only one parameter to check. It is calculated as:

If $\mu > 1$, an amplifier is unconditionally stable where the higher μ value, the more stable an amplifier is. If $\mu < 1$, an amplifier is potentially unstable and stability circles are required to identify which values of Γ_S and Γ_L will cause an amplifier to oscillate.

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} + S_{11}^*| + |S_{12} * S_{21}|} \quad (3.30)$$

(Pozar, 2012)

3.5 Linearity

Receiver linearity is the ability of the receiver to produce an output signal that is proportionate to the input signal. After parameters are exceeded, the behavior of the receiver is spurious and unpredictable and in the realm of non-linearity. The result is poor performance of the receiver and the ability to demodulate. The following parameters indicate how linear a receiver is and can potentially expose when the receiver will react non-linearly.

3.5.1 Return Loss

The return loss is part of the applied signal that was reflected from either a load where it is the output return loss (S_{22}) or the DUT where it is the input return loss (S_{11}). Mismatch between Γ_S and Γ_{IN} or Γ_L and Γ_{OUT} causes a return loss. Therefore, the smaller the return signal the better the matching and the more power is shifted from the source to the DUT and form the DUT to the load.

(Pozar, 2012)

3.5.2 Output (OP1dB) and Input (IP1dB) Compression

Amplifiers provides a constant gain over a specific frequency range. This is true when the amplifier is operated in the linear region. Gain can be anything from 1dB to 10dB. The P1dB compression is the point at which this constant increasing gain deviates by 1dB as seen in Figure 3.3. This indicates that the DUT is in compression. The output power begins to saturate where it starts operating in the non-linear region when more power is applied. The output power P1dB compression point (OP1dB) is therefore the maximum output power before the DUT performs non-linearly, while the input power P1dB compression point (IP1dB) is the maximum input power that can be applied to the DUT before it performs non-linearly. Amplifiers should always be operated below the P1dB compression point.

$$OP1dB = IP1dB + Gain\ at\ Compression\ Point \tag{3.31}$$

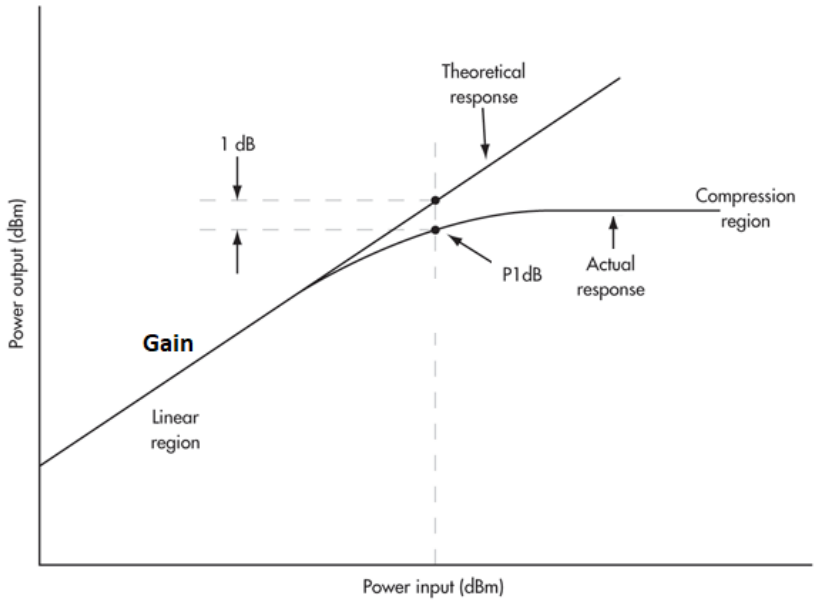

Figure 3.3: Input and Output P1dB

(Nanzer, 2012)

3.5.3 Third Order Intercept (IP3)

The 3rd order intercept is used to predict what power level the 3rd order products ($2f_1$-f_2 and $2f_2$-f_1) are when 2 signals of the same power and very close in frequency is presented to the DUT. The 3rd order products will increase by 3dB in power for every 1dB increase of input power. The higher the IP3 parameter of the DUT, the better the ability it can suppress the 3rd order products. The input 3rd order intercept is calculated as:

$$IIP_3 = OIP_3 - Gain \tag{3.32}$$

Where the change in power level between the output power and the 3rd order products ($2f_1$-f_2 and $2f_2$-f_1) of the DUT is calculated as:

$$\Delta IP_3 = 2[IIP_3 - Input\ Power] \tag{3.33}$$

and the power level of the 3rd order products is calculated as:

$$P_{OUT}(2f1 - f2\ and\ 2f2 - f1) = Output\ Power - \Delta IP_3 \tag{3.34}$$

(McClaning K and Vito T, 2001)

3.5.4 Second Order Intercept (IP2)

The 2nd order intercept is used to predict what power level the 2nd order products (2f1 and 2f2) will be when 2 signals of the same power and very close in frequency is presented to the DUT. The 2nd order products will increase by 2dB in power for every 1dB increase of input power. The higher the IP2 parameter of the DUT, the better the ability it can suppress the 2nd order products. The output 2nd order intercept is calculated as:

$$OIP_2 = IIP_2 + G \tag{3.35}$$

Where the change in power level between the output power and the 2nd order products (2f1 and 2f2) of the DUT is calculated as:

$$\Delta IP_2 = IIP_2 - Input\ Power \quad (3.36)$$

and the power level of the 2nd order products is calculated as:

$$P_{OUT}(2f1\ and\ 2f2) = Output\ Power - \Delta IP_2 \quad (3.37)$$

(McClaning K and Vito T, 2001)

3.6 Chapter Summary

Intrinsic noise which is noise generated inside the LNA's is generally called thermal noise since the other type of intrinsic noise sources are smaller than thermal noise and can't be distinguished from one another. Therefore, thermal noise is the key influence of noise for the LNA. Operating the LNA in a cooler environment, using less power or over a smaller bandwidth reduces the noise figure.

The LNA in form of a MMIC arrangement will be used since they provide internal input and output matching, where $Z_S = Z_{in}^*\ and\ Z_L = Z_{out}^*$. This is the least complex approach when designing the amplification section. On condition that the MMIC is connected to a 50Ω source and 50Ω load for maximum power to be transferred from the source to the LNA and for the maximum power to be transferred from the LNA to the load.

It is essential to check if the LNA is stable under various source and load impedances. By using the Rollet's stability condition, where K must be greater than 1 and |Δ| must be smaller than 1 will the LNA be stable and not oscillate. The μ-stability can also be used as a single test where the μ value needs to be greater than. 1. When either of the above values are not within their respective specifications to be stable, the stability circles can be used to determine at what source and load impedance the LNA will be unstable and oscillate.

The S_{11} and S_{22} of the LNA must be as high as possible, so that less power will be reflected by the load to the LNA (S_{22}) or from the LNA to the source (S_{11}). This also increases isolation of the input port of the DUT from the output port and ultimately good stability.

The P_1dB compression output power must be as high as possible, where it will be used to determine the maximum input power that can be applied for maximum gain before compression and distortion occurs.

The output third order intercept (IP3) is an important parameter as this indicates the ability of the LNA to suppress 3rd order products such as $2f_1$-f_2 and $2f_2$-f_1. The higher the IP3 the better

the LNA's suppression ability, the less complex pre-LNA filters are required to remove the 3rd order products before amplification. This parameter can be used to predict the 3rd order product power levels. Similarly, the output second order intercept (IP2) is also an important parameter. It represents the LNA's ability to suppress the 2nd order products $2f_1$ and $2f_2$. Where the higher this value, the less complex the pre-LNA filters are required to remove 2nd order products before amplification.

Chapter 4

Radio Frequency Mixer

4.1 Introduction

In 1902 Reginald Aubrey Fessenden patented the frequency translation process called heterodyning and described it in a classic paper in 1913 (L.C. Godara, 1999). Today, the radio frequency (RF) mixer, which is a three-port non-linear device, translates signals from one frequency to the other. It is used to up-convert frequencies for transmitting, or down-convert frequencies for receiving. The second purpose to use the RF mixer is to detect the phase of two signals. The former is known as frequency translation and latter is called phase comparison (Poisel, 2014)**,** (Analog Devices Inc., 2008)**.** The down-conversion process changes the RF input signal into a reduced frequency termed, IF. This allows easier processing of embedded information in the RF receiver section. The up-conversion process involves the conversion of the reduced in frequency IF to a higher in frequency RF to allow effective amplification for the RF transmitter section. These sum signals occur at LO plus the RF signal. The down-conversion process involves difference signals which are LO minus RF or RF minus the LO. In down-conversion there is also a high-side conversion when the LO is higher in frequency than the RF and a low-side conversion when the LO is lower in frequency than the RF (Rohde and Newkirk, 2000).

For this chapter, only the frequency translation capabilities of the passive radio frequency mixer for down-conversion (receivers) will be considered.

4.2 Ports of the RF Mixer

4.2.1 The radio frequency port (RF)

The RF mixer has an input port as in Figure 4.1, where the higher received signal is inputted to be down converted to produce the lower in frequency IF or the baseband signal.

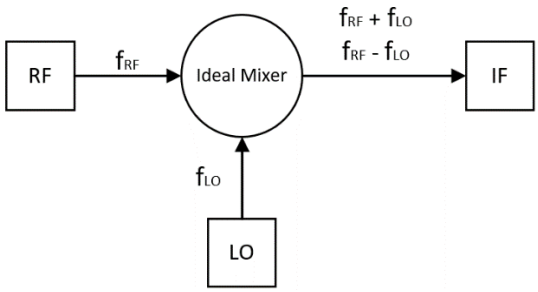

Figure 4.1: Ports of a Mixer

4.2.2 The local oscillator port (LO)

The LO port as in Figure 4.1 of all type of mixers can be considered as an input power to a switch. When the LO signal is above a predetermined threshold given in the mixer's datasheet, it is on. When the LO signal is below a predetermined threshold given in the mixer's datasheet, it is off. The LO is therefore always bigger than the RF port signal in terms of power (Manganaro, 2013).

4.2.3 The intermediate frequency port (IF)

The IF output of the receive mixer is the output port as in Figure 4.1**.** The ideal output will consist of 2 signals. The RF port signal ± LO port as in Figure 4.1**.** The ideal mixer produces the combination of LO and IF signals:

$$\begin{aligned} v_{RF}(t) &= K v_{RF}(t) v_{LO}(t) \\ &= K \cos 2\pi f_{RF} t \cos 2\pi f_{LO} t \\ &= \frac{K}{2}[\cos 2\pi (f_{RF} - f_{LO})t + \cos 2\pi (f_{RF} + f_{LO})t] \end{aligned} \tag{4.1}$$

K is the conversion loss constant, and the IF output comprises of:

$$f_{IF} = f_{RF} \pm f_{LO} \tag{4.2}$$

LO and RF signals will have harmonics which after mixing will produce odd-order products until the nth order at the IF output port. Generally, 2nd order products are the bigger in power signals and all the products above the 3rd order products will not be an issue as those products are lower in power and can be filtered out. Some of the 3rd order products will lie close to the down-converted IF frequency as in Figure 4.1 and requires a high Q filter to remove them. The IF also contains the image signal that occurs at two frequencies (McClaning K and Vito T, 2001).

The high-side conversion (LO higher than RF):

$$f_{IMAGE} = f_{RF} + 2 * f_{IF} \tag{4.3}$$

The low-side conversion (LO lower that RF):

$$f_{IMAGE} = f_{RF} - 2 * f_{IF} \tag{4.4}$$

4.3 Parameters of the RF Mixer

4.3.1 Conversion Loss/Gain

It is a ratio between the input and output ports of a receiver mixer. Gain is experienced with active mixers while loss is experienced with passive mixers. The formula to calculate this is:

$$Gain\ or\ Loss\ = IF_{output\ Power} - RF_{Input\ Power} \quad (4.5)$$

Gain or loss is in dBs and the output and input powers are in dBm (Marki, 2010). The majority of mixers experience conversion loss up to 9dB, with a minimum of 3dB loss experienced due to the power that dissipates in the sidebands of the IF signal. Conversion loss can also, in terms of S-parameters be called insertion loss of a mixer (S_{21}). Furthermore, conversion loss is also increased by more components in the transmission line of the mixer, by mismatch of the balun transformer and by the resistance in the diode. (Henderson, 1990).

4.3.2 Isolation

Isolation is required to suppress the LO at the RF input port where it can potentially radiate out of the receive antenna, to suppress the LO at the IF output port and to reduce the amount of electromagnetism induced on the ports of the mixer. The RF also needs to be suppressed at the output of the IF (Devlin, 2000).

4.3.2.1 LO-RF

The LO-RF output isolation is the extent of how much the feedthrough power originating from the LO is attenuated at the RF output. Decent isolation values start at about 25dB. The LO feedthrough power can interfere with input RF circuits such as the low noise amplifier prior to the mixer stage or even radiate out of the receiver antenna if no stage is used before the mixer.

4.3.2.2 LO-IF

The LO-IF port isolation is the extent of how much the feedthrough power originating from the LO is attenuated at the IF output. Decent isolation values start at about 25dB. The LO feedthrough power can interfere and saturate the IF amplifier after the mixer stage and complicate the IF signal.

4.3.2.3 RF-IF

The RF-IF port isolation is the extent of how much the feedthrough power originating from the RF input is attenuated at the IF output. This is not a significant parameter because the receive signal is magnitudes lesser than the LO feedthrough signal and therefore not a key concern. The lower the amount of conversion loss is an experienced by the mixer is an indication of how good the RF-IF isolation will be (Marki, 2010).

4.3.3 Input 1dB Compression Point

The RF port can handle a maximum amount of power before saturation is experienced. The point at which this occurs is termed the 1dB compression point as in Figure 4.2. This value is dependent on the LO level. The higher the LO level the higher this 1dB compression level will be. By examining when the conversion loss of a mixer increases by 1 dB, indicates the 1dB compression point. Increasing the RF port power level will result in heat being generated and higher-order intermodulation products are experienced. The 1dB compression power level is about 5-10dB lower than the LO input power applied at the LO port. In terms of dynamic range, the 1dB compression is the upper limit of the mixer IF port output (Henderson, 1981).

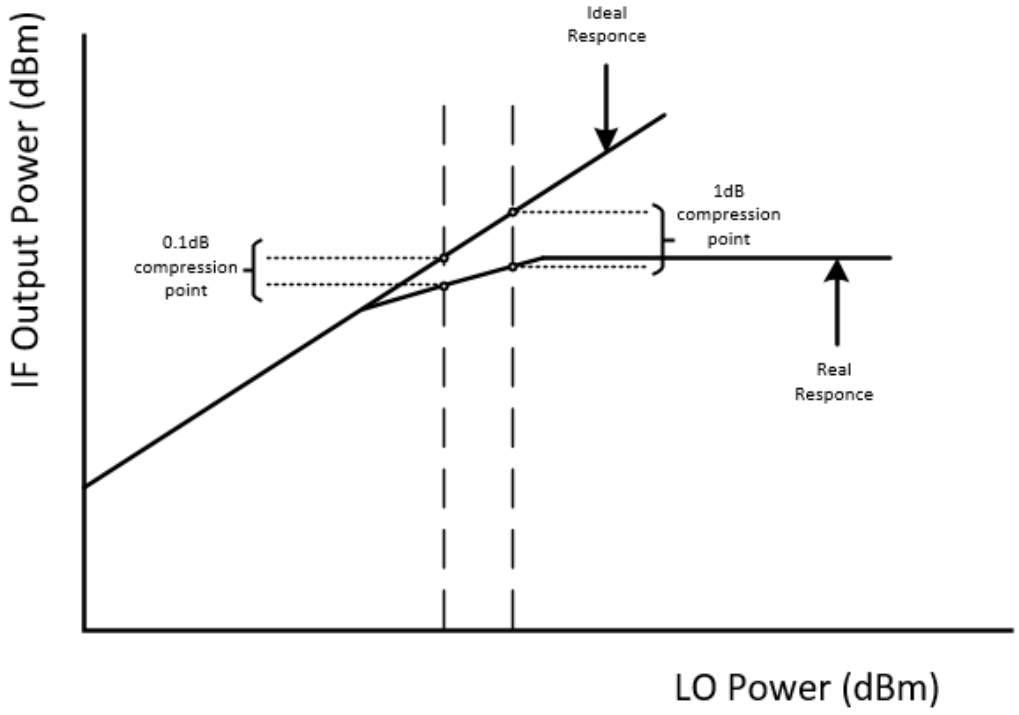

Figure 4.2: 1dB compression point

4.3.4 SSB and DSB Noise Figure

Practically, the value of the single side band (SSB) noise figure is approximate to the conversion loss of the mixer (Marki, 2010). The double side band (DSB) noise is double the SSB noise. This is accurate since noise from the source input is doubled at the output when the RF and image frequency noise is mixed. The formula to calculate this is:

$$NF_{Double\ side\ Band} = NF_{Signle\ Side\ Band} - 3dB \tag{4.6}$$

4.3.5 Input 3rd Order Intercept Point

The input 3rd-order intercept point IIP_3 stands as a theoretical location on the IF output vs the RF input curve that will never be reached in the normal operating conditions of the RF mixer. It relates to the 3rd-order intermodulation distortion (IMD_3) products for the lower in frequency translation process at frequencies:

$$2f_1 - f_2 - LO \tag{4.7}$$

$$2f_2 - f_1 - LO \tag{4.8}$$

$$2f_2 + f_1 - LO \tag{4.9}$$

$$2f_2 + f_1 - LO \tag{4.10}$$

IMD_3 products will always be lower than the desired IF. The mixer IF output will saturate before the IMD_3 products can get large enough to interference with the IF output. The IIP_3 though is an indication of the mixers IMD_3 performance. Therefore, the higher the IIP_3, the higher the RF input that can be applied to the mixer input before distortion and consequently saturating the IF port of the RF mixer occurs. The IIP_3 is generally 10-20dB higher than the 1dB compression point.

The IIP_3 level in dBm can be used to calculate the ability of the RF mixer to suppress the IMD_3 products within the IF band and given as:

$$IIP_n = P_{RFin} + \left[\frac{\Delta P_n}{n-1}\right] \tag{4.11}$$

where,

- N refers to the nth order point of intercept.
- P_{RFin} refers to the fundamental frequency output in dBm.
- ΔP_N refers to the suppressed intermodulation product of the order n with reference to the desired IF in dBc.

Therefore, the suppression capability of the mixer is:

$$IIP_n - P_{RFin} = \left[\frac{\Delta P_n}{n-1}\right]$$
$$\therefore \Delta P_n = [(n-1) * IP_n] - [(n-1) * P_{RFin}] \quad (4.12)$$

The intercept point of the IF output (OIP3) is:

$$OIP_3 = IIP_3 + Converion\ loss \quad (4.13)$$

(Li, 2012)

4.3.6 Input 2nd Intercept Point

The input 2nd-order intercept point (IIP_2) stands as of greater concern in broad bandwidth applications. While the IIP_3 is for narrow band applications. The mixer IIP_2 is one of the most important specifications for low-IF or direct conversion receivers and is the preventive requirement in making these kinds of receivers. It relates to the 2nd-order intermodulation distortion (IMD_2) products for the lower in frequency translation process at frequencies:

$$f_1 + f_2 - LO \quad (4.14)$$

$$f_2 - f_1 - LO \quad (4.15)$$

$$2f_1 - LO \quad (4.16)$$

$$2f_2 - LO \quad (4.17)$$

IMD_2 products are problematic mainly in homodyne receivers.

The IIP_2 level in dBm can be used to calculate the ability of the RF mixer to suppress the IMD_2 products which are outside the IF band of the super-heterodyne and image reject receivers, but inside the IF band of Homodyne/Direct-Conversion/Zero-IF and Low-IF Receiver. The same equation will be used as above where the nth term is 2 instead of 3 as for the IIP_3

Therefore, the IIP_2 suppression capability of the mixer is:

$$IIP_2 - P_{RFin} = \left[\frac{\Delta P_2}{2-1}\right]$$
$$\therefore \Delta P_2 = [(2-1) * IP_2] - [(2-1) * P_{RFin}] \quad (4.18)$$

The second-order intercept point at the IF output (OIP_2) is:

$$OIP_2 = IIP_2 + Converion\ loss \quad (4.19)$$

(Li, 2012)

4.3.7 VSWR

The VSWR is another way of describing the input port impedance of the RF, LO and IF ports. The input impedance is poor, meaning that because most RF systems are designed around 50Ω, RF mixer RF ports never reach 50Ω. Therefore, the VSWR is a measure of a mixer's actual impedance Z with respect to the desired characteristic impedance Z_0 of 50Ω. The reflection coefficient is derived from Z and Z_0 where,

$$\Gamma = \frac{Z - Z_o}{Z + Z_o} \quad (4.20)$$

$$\therefore VSWR = \frac{1+|\Gamma|}{1-|\Gamma|} \quad (4.21)$$

The VSWR value can only be accurately measured when taking into consideration the LO power and temperature at the examined bandwidth. The impedance of the device under test changes when the LO power is altered, producing change in VSWR. RF input power, which is at least 20dB lower than LO input power, does not noticeably alter the device under the test bias point, and consequently has little effect on VSWR. When the device under test impedance changes, the input impedances of all three ports change. Therefore, changing the LO power level will change the VSWR of all three ports (Henderson, 1981).

4.4 RF Mixer Topology

4.4.1 Active (Transconductance) and Passive (Resistive)

RF mixers can be operated passively where the LO is used to switch components such as diodes, BJT and FETs on and off to achieve the required mixing. This allows for less current to be used by the receiver circuit. When a higher-powered IF is required, amplifying circuits

using components such as BJT's and FET's can be used to either amplify the RF and LO input and the IF output itself. These are known as active mixers and mix signals through transconductance (Li, 2012).

Consequently, active mixers generate thermal noise, and this increases the noise figure of the RF mixer. Active mixers also require less power from the LO for adequate mixing to occur and have better ultimate LO-to-IF isolation. The disadvantage of this is that the 1dB compression is much lower and therefore passive RF mixers can receive higher power RF input signals than active RF mixers. This means that active mixers have lower IP3 than passive mixers (Vinet and Zhedanov, 2011).

Passive mixers have higher conversion loss and has an unavoidable 3dB loss at the output because the sum and difference output frequency sidebands, where only one side band is needed and output drops half the power after filtering the unwanted sideband (Vinet and Zhedanov, 2011). The switching process only allow 50% of window time to the IF which further increases the conversion loss. The conversion loss is up to 10dB because of other properties of passive components. (McClaning K and Vito T, 2001).

Passive RF mixers operate on a wider bandwidth as it is more realistically to produce passive mixers. The higher the frequency the more difficulty it is to build amplifying circuits (Li, 2012).

Table 4.1: Active vs Passive Mixer

Parameters	Active Mixer	Passive Mixer
Current usage	Inferior	Superior
LO Power	Superior	Inferior
Conversion Loss	Superior	Inferior
Noise Figure	Inferior	Superior
Bandwidth	Inferior	Superior
Reliability	Inferior	Superior
IP3	Inferior	Superior

4.4.2 Mixer Balance

The general purpose to balance the ports of the RF mixer is to reduce:

1. The RF feedthrough to the IF.
2. The LO feedthrough to the IF.
3. Infrequently, the IF feedthrough to the RF.

Mixer balance is a process by transforming the input signal from an unbalanced signal having a ground and a positive wire to a balanced signal having two wires for signal conduction and a common ground. Where the one signaling wire is the reverse polarity of the other with reference to the common ground. When these two signals combine, they cancel each other out and results in a reduced RF, LO or IF feedthrough, depending where the unbalanced to balance transformation is done. This is also known as port isolation (Vinet and Zhedanov, 2011). Hybrid couplers such as the 90° and 180° coupler transform the line from unbalanced to balanced. Mixers are also balanced through balun transformers. When balancing is done, more LO power is needed to sufficiently convert signals from unbalanced to balanced (Pozar, 2012).

4.4.2.1 Single Balanced Mixer

When the mixer is a single balanced variant, the LO or the RF port is balanced, but not both. Single balanced mixers are not involved but have substandard performance regarding the RF-IF or LO-IF isolation, depending where the balancing is done. Either the RF or the LO odd-order products (harmonics) are suppressed, depending on what port the balancing is done (Poisel, 2014).

4.4.2.2 Double Balanced

When the mixer is a double balanced variant, both the LO and the RF ports are balanced. This adds cost and complexity but increases linearity with a higher conversion loss compared with single balanced mixers. The harmonics of LO and RF ports are also suppressed (Poisel, 2014). Generally, double balanced mixers are diode ring mixers as in Figure 4.3 where a higher in power LO is needed because double the number of diodes are used. The odd-order of the LO and RF products are suppressed (McClaning K and Vito T, 2001).

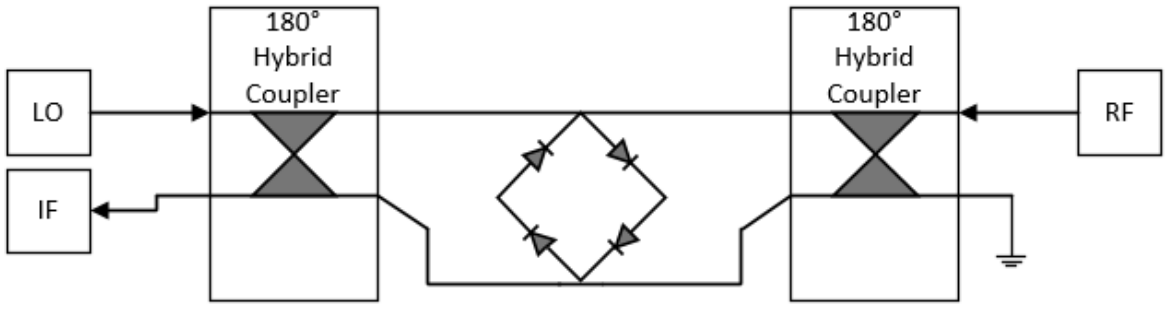

Figure 4.3: Double Balanced Mixer

4.4.2.3 Double Doubly Balanced (Triple Balanced Mixer)

When the mixer is a triple-balanced variant, also known as a double double-balanced mixer, balancing is done on all three ports as in Figure 4.4. Linearity and isolation between all 3 ports is increased. Since there are now 3 balancing conversions done, the LO power needed is increased, in case of a diode mixer configuration, the number of diodes also increases. This rises cost and current use (Vinet and Zhedanov, 2011).

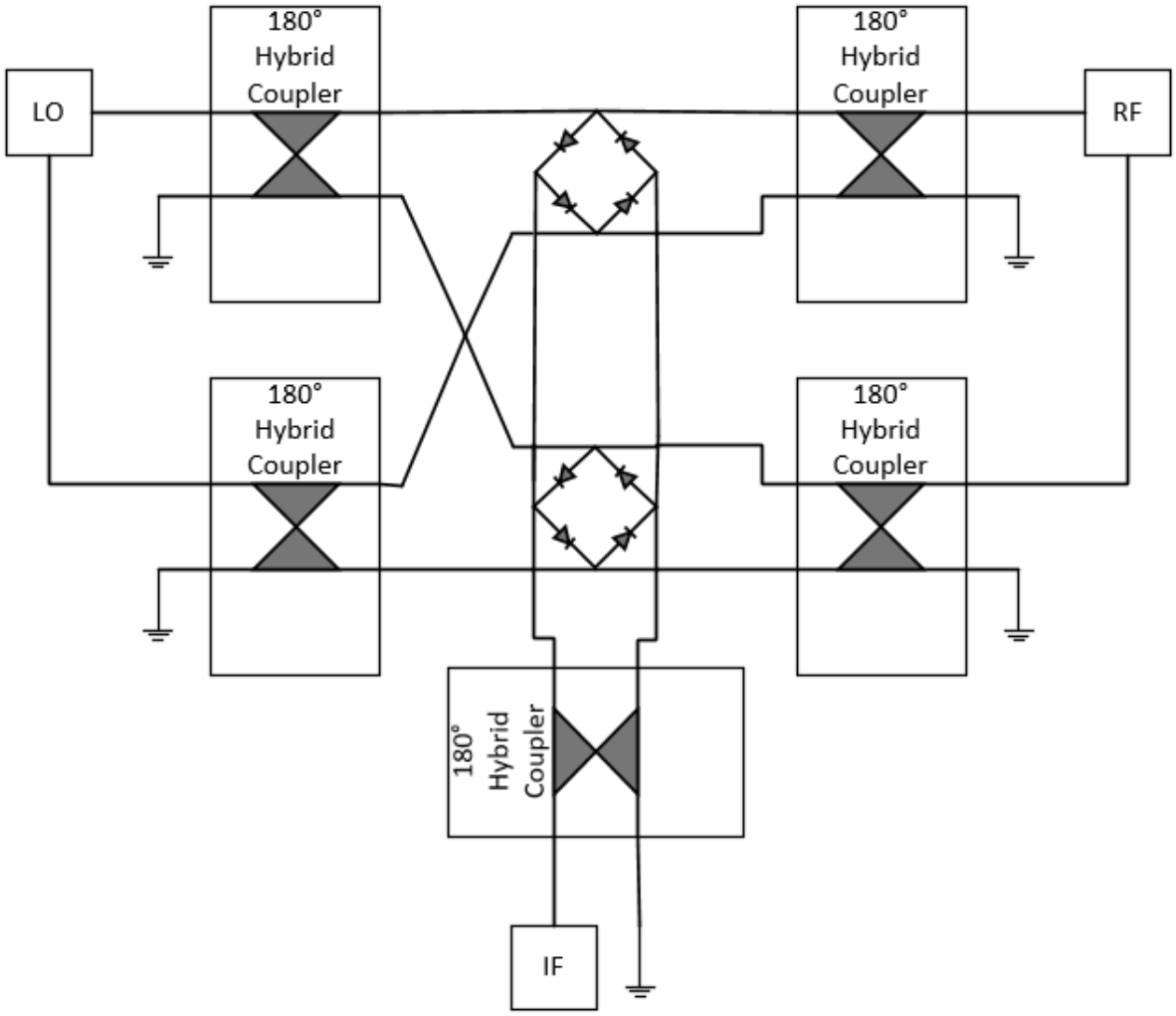

Figure 4.4: Triple Balanced Mixer

4.4.3 Single Ended Mixer (Diode)

This is the least involved kind of mixer where linearity performance is not priority, and where low LO power is required. A single diode element is used as in Figure 4.5. RF and LO inputs are combined through a diplexer and are superimposed on one another to drive the diode and produce a translation in frequency IF signal.

Because a single diode is used, LO power is low. It can be increased to reduce odd-order harmonics, but this requires more current for the receiver circuit to operate (McClaning K and Vito T, 2001). The low LO reduces the dynamic range of the mixer only allowing an RF input of less than 20dB than the LO power for the mixer to operate (Rohde and Newkirk, 2000). BPF's at the ports of this unbalanced mixer increases the isolation between the ports. Spreading apart the frequencies of the 3 ports will increase linearity. This topology is used in narrowband circuits (McClaning K and Vito T, 2001). To increase the linearity and LO power without balancing the ports for this topology, the number of diodes used needs to increase in the conduction path. This permits the LO power to increase which inherently increases the maximum RF input level allowed before distortion occurs (Vinet and Zhedanov, 2011).

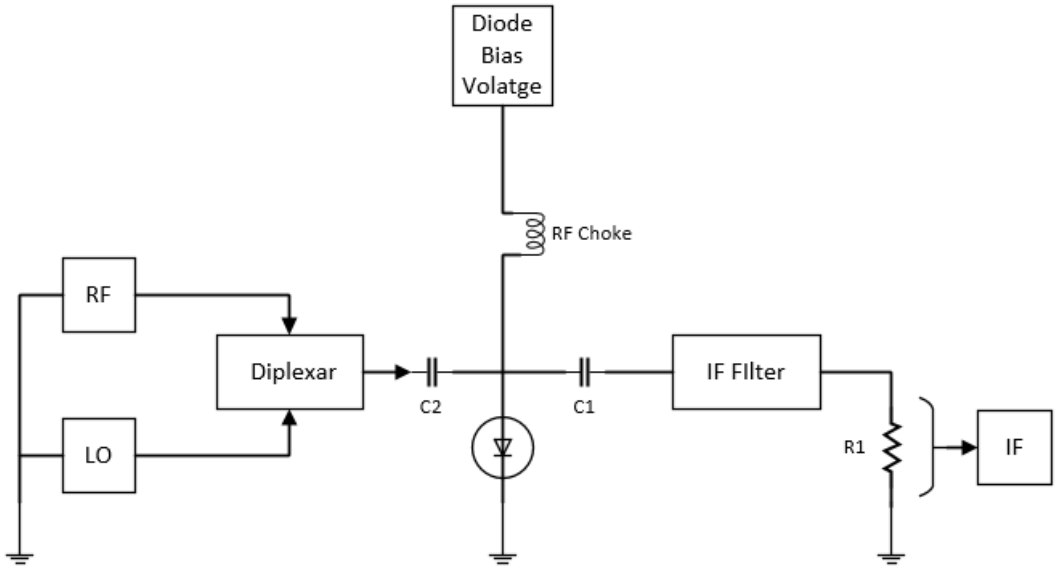

Figure 4.5: Single Ended Diode Mixer

4.4.4 Single Ended balanced Mixer (Diode)

An alternative method of increasing linearity and LO power is by balancing one of the ports of the 3-port mixer as in Figure 4.6 with opposing diodes. It can be either be accomplished through a transforming balun (a) or a hybrid coupler (b) as in Figure 4.6. This type of topology also removes all even-order products (Devlin, 2000).

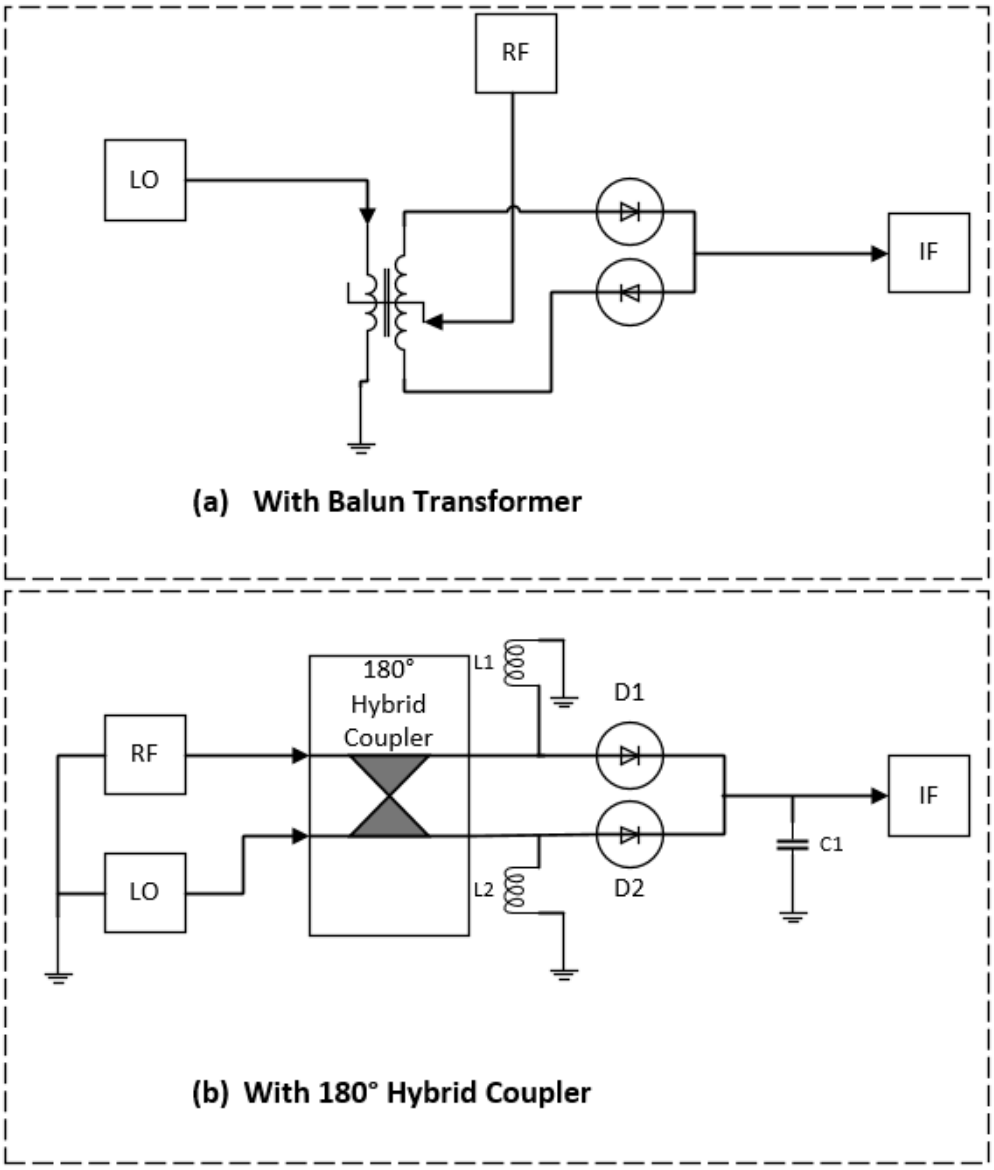

Figure 4.6: Single Ended Balanced Mixer with (a) Balun Transformer, (b) 180º Hybrid Coupler

Isolation is improved from balancing of the LO, where LO-IF and LO-RF feedthrough is reduced and consequently the LO and its harmonics are also suppressed at the output of the IF port. This configuration will cost more by the addition of the diodes and transformer. Increases current usage from the addition of the diodes and transformer. Therefore, more components and cost. Lastly, the conversion loss also increases now with more than 10dB (McClaning K and Vito T, 2001).

4.4.5 BJT Mixer

To reduce the conversion loss and provide gain, active mixers are implemented. The BJT is used for this purpose, but to use less current for high integrated circuits.

The disadvantage of these circuits are poor linearity and low intercept points that operate in narrowband circuits. RF-IF, LO-IF and LO-RF isolation are also inadequate.

To improve on this drawback, the use of multiple transistors in the Gilbert multiplier cell configuration, where even-order products are reduced and port isolation is improved.
The shortcoming of BJT's are that they have a high-impedance output, meaning non-standard filters must be used other than 50 Ohms, which increases complexity.
(Rohde and Newkirk, 2000)

4.4.6 FET Mixer

FET mixers are implemented in integrated circuits since they have a small footprint, where high input impedance prevents loading of the signal source are eliminated in FET. When using the FET passively requires matching networks at all the ports which increases the complexity of the receiver. When used actively the FET mixer has gain, but poor noise and a dynamic range similar to that of BJT mixers. Passive mixers have superior linearity over active FET mixers. This results in higher levels of intermodulation. The FET mixer output is load depended and works best with resistive loads. Cascading the FET in a Gilbert multiplier cell is therefore used to increase linearity which increases component and complexity (Rohde and Newkirk, 2000).

4.4.7 Gilbert Cell Mixer

This topology first described in the 1960s by Barrie Gilbert, uses symmetry in the form of a double balanced mixer in an integrated circuit to suppress the RF and LO signals from interfering with the IF output. Isolation is improved over the double balanced diode or FET mixer with less LO power. Subsequently, the increased isolation improves the IF output that is now less dependent on the load termination. The Gilbert cell mixer cannot handle as much signal as the passive meaning their 1dB compression point is much lower (Poisel, 2014).

4.4.8 I/Q Mixer and I/Q Modulator

The I/Q mixer and I/Q modulator are terms that are used to signify the mixing of I/Q signals where the former is used in receivers and the later in transmitters (Sweet, 2007)**.** The I and Q stands for in-phase and quadrature-phase (Vinet and Zhedanov, 2011). The I signal differs from the Q signal in phase by 90°. This makes them in quadrature with each other.

I/Q signals are generated as in Figure 4.7, when the RF signal is mixed with 2 different phased LO's. A LO that is like cosine (0°) and the other that is like sine (90°) (Sweet, 2007). When these I/Q signals are added together through the summation process, the result is a quadrature modulation process that can modulate/demodulate FM, AM, PM signals. The significance of

generating I/Q signals is that by changing the amplitude of the either the I or Q signal, changes the phase of the combined I/Q signal. Therefore, the amplitude and the phase can be modulated at the same time to create digital modulation schemes such as BSPK, QPSK and QAM. The advantage of using I/Q signals is to reduce the need for mechanical filters that are used to suppress the LO and the Image signal (Belov, 2012).

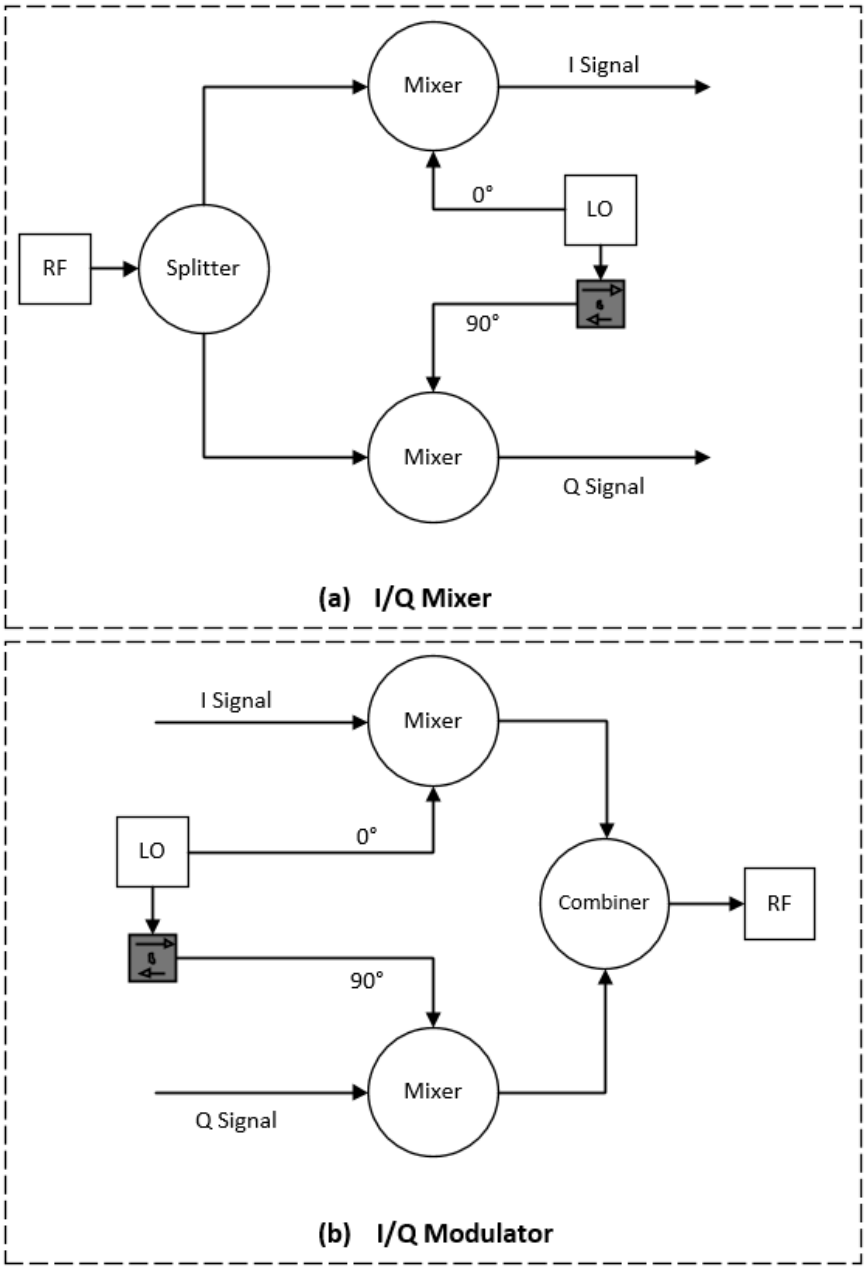

Figure 4.7: (a) I/Q Mixer, (b) I/Q Modulator

4.4.8.1 Single Sideband Mixer (Transmitter)

The single side band (SSB) mixer is derived from the I/Q modulator, but has an additional 90° phase shift in the path of the side band that is required to be suppressed as in Figure 4.8. In the non-phase shifting path the wanted side band is essentially doubled in power while in the

90° phase shift path, the unwanted side band is essentially halved in power and therefore suppressed.

(John W. M. Rogers, 2010)

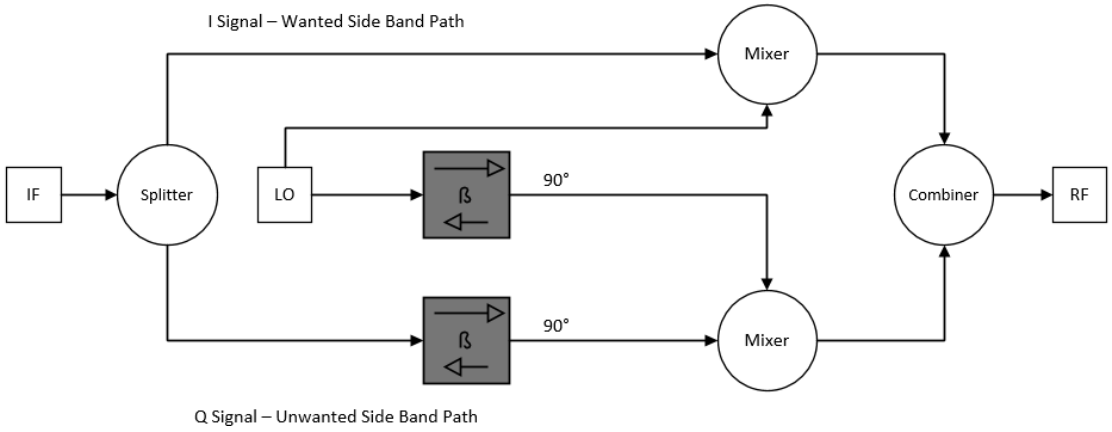

Figure 4.8: SSB Mixer (Transmitter)

4.4.8.2 Image Reject Mixer (Receiver)

The image reject (IR) mixer is derived from the I/Q mixer, but has an additional 90° phase shift in the path of the image signal that is required to be rejected as in Figure 4.9. In the non-phase shifting path the wanted side band is essentially doubled in power while in the 90° phase shift path, the unwanted image signal is essentially halved in power and therefore rejected.

(John W. M. Rogers, 2010)

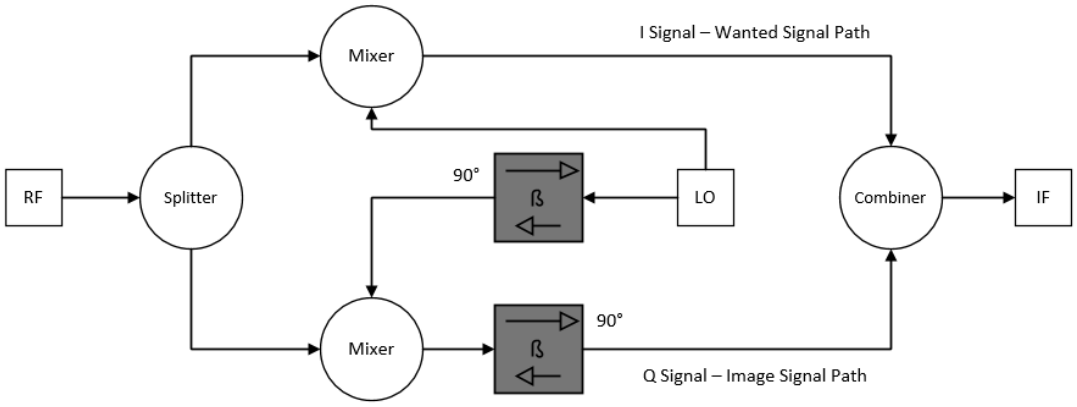

Figure 4.9: Image Reject Mixer (Receiver)

4.5 Additional Parameters of the IR Mixer

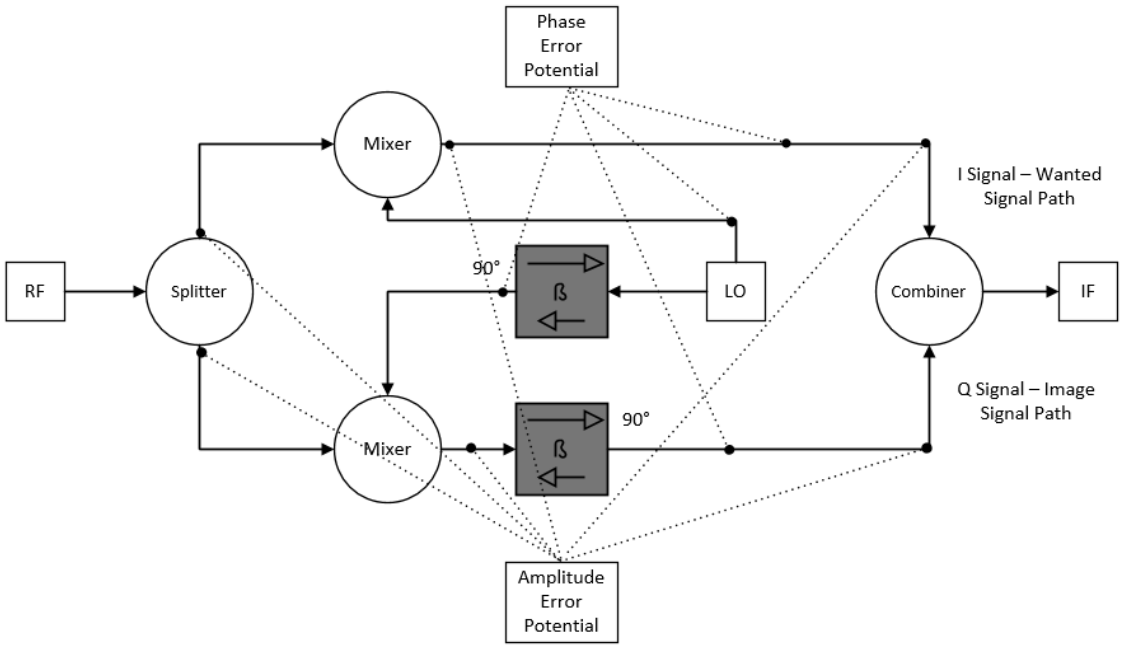

Figure 4.10: Amplitude and Phase errors of IR Mixer

4.5.1 I/Q Amplitude Balance

Amplitude error is caused as in Figure 4.10 by the:

- RF splitter within the IR mixer and the ability to split the signal power equally feeding the mixers.
- Mixers within the IR mixer and when these mixers don't have the same conversion losses.
- IF Combiner and its ability to combine the output of the mixers equally to form the IF signal.

The amplitude error needs to be as small as possible as this indicates the ability of the IR mixer to add the I signal and suppress or reject the Q signal.

4.5.2 I/Q Phase Balance

The mixers of the IR mixer cause the phase error as in Figure 4.10 by not having the ability to provide a 90° phase difference between the I and the Q signal. The phase error in degrees needs to be as small as possible as this indicates the ability of the IR mixer to add the I signal and suppress or reject the Q signal.

4.5.3 Image Reject Ratio

There are 2 requirements for a good image reject ratio as in Figure 4.10:

- An excellent amplitude match between the amplitude influencing components of the IR mixer. Meaning that the I and Q signals must have the same amplitude.
- An excellent phase match between the phase influencing the components of the IR mixer. Meaning there is exactly a 90° phase difference between the I and Q signals of the IR mixer.

This is obviously an ideal IR mixer and in reality, there will always be a small amplitude mismatch and a phase difference close to 90° and is calculated as the image reject ratio:

Where A is the amplitude error in dBs and B is the phase error in radians. When there is no phase and amplitude error the equation yields a value of infinity indicating that the image signal is completely rejected and non-existing as in Figure 4.11. This is only in an ideal world. From the equation it can also be deduced that the amplitude error needs to be as small as possible because even a 0.1dB difference in the amplitude between the I and the Q signal will only have 25dB of image reject. While a phase error of 0.1 degrees results in a 60dB rejection.

$$IRR = 10\log_{10}\frac{1+(1+A)^2+2(1+A)*\cos B}{1+(1+A)^2-2(1+A)*\cos B} \tag{4.22}$$

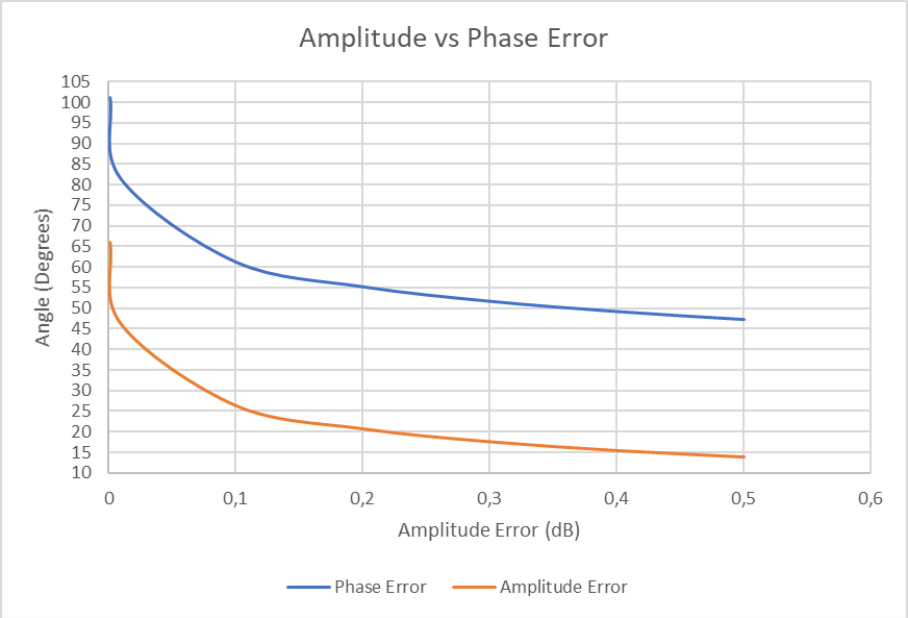

Figure 4.11: Amplitude vs Phase Error

(John W. M. Rogers, Calvin Plett, 2013)

4.6 Chapter Summary

The RF mixer generates the IF signal that consists of order products to the nth term. The influencing order products are the 2nd and 3rd order. Products larger than the 3rd order are usually too high in frequency or too small in power to influence the wanted signal of the IF. Difference products are down-conversion products when the LO is higher in frequency than the RF (high-side down-conversion) and when the LO is lower in frequency that the RF (low-side down-conversion). The down-conversion also produces an unwanted image signal IF when the image signal (RF+2IF) for high-side conversion or (RF-2IF) for low-side conversion, is presented to the RF port of the RF mixer. Filters placed before the RF mixer removes the image signal before the mixing process, or by phase cancellation when it is already mixed with the RF signal.

The generation of the sum frequencies results in one half of power loss. The generation of difference frequencies results in another one half of power loss. Since only one set of frequencies is only required, 3dB loss is unavoidable. Power is further lost through the diodes or transistors that do the mixing of the RF and LO signal. Active mixers can be used to decrease conversion losses but generates thermal noise and therefore increases the SSB noise figure. Amplification circuits such as BJT and FET or in a Gilbert Cell configuration mixer, become harder to implement at higher frequencies; therefore, passive mixers can have higher operating bandwidths with less complexity. The SSB Noise figure though is approximate to the conversion loss in passive mixers.

Isolation of the ports is needed to prevent the various signals that are present at the output and the input ports of the RF mixer from influencing one another. Namely between the LO-IF, LO-RF and IF-RF ports. This parameter is increased when the ports are balanced. Balancing the ports increases the conversion loss, but the added benefit of the odd order products that are suppressed outweighs the conversion loss disadvantage. Triple balancing, meaning balancing all 3 ports of the RF mixer can be used to increase isolation, but double balancing is preferred to achieve trade-off between conversion loss and isolation.

The more power that can be applied the LO port, the more power that can be applied to the RF port and therefore increasing the 1dB compression point of the RF mixer. The higher the 1dB compression point the greater the ability of the RF mixer to suppress the 2nd and 3rd order products and therefore better IP2 and IP3 specifications.

The RF I/Q mixer as in Figure 4.7 generates I and Q signals by having the LO in quadrature with the RF input signal. By adding an extra 90° phase change to the Q signal of the I/Q mixer

and combining it with the I signal, creates a suppressed image signal and an increase in power of the wanted IF. This is called an image reject (IR) mixer as in Figure 4.9.

The IR mixer uses 90° shifting of phase of the Q signals twice to create a total 180 degrees phase shift. The practical way of creating 90° phase change is to use a passive device called the quadrature hybrid coupler. It is a 4-port device that has a fixed phase conversion. An IR mixer with the quadrature hybrid can be seen in Figure 4.12. The RF mixers in the I/Q mixer is of double balanced configuration. Double balanced mixers on their own require filters to block the image from entering the mixers but the double balanced mixer in an I/Q mixer configuration handles the image by means of channelizing it into a port that can be terminated in 50Ω. The 50Ω termination is either internal to the I/Q mixer or quadrature Hybrid combiner or externally. The wanted IF signal therefore is separated into another port where it can be used. The challenge is to get the wanted IF signal to increase and consequently decreases the image IF in power. In order to do this, the amplitude of the I and the Q signal has to have a difference (error) in power of less than 0.01dB as in Figure 4.11, and the phase of the I and Q signals has to be off by less than 0.1° as in Figure 4.11 from the intended 90°. This enables an adequate IF signal for the next stage.

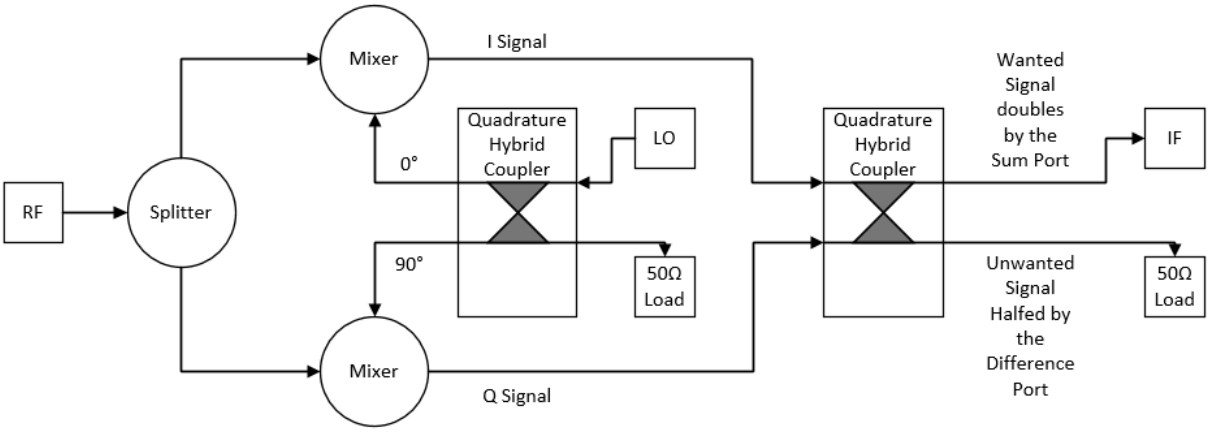

Figure 4.12: IR Mixer with Quadrature Hybrids

Chapter 5

Local Oscillator

5.1 Introduction

The local oscillator (LO) in this thesis is referred to the generated signal that has the essential frequency signal that can be used to down-convert the RF input signal to a suitable frequency signal. The LO as in Figure 5.1 fundamentally consists of 3 sections. The reference signal section that triggers the synthesizer section. A loop filter section which is used to set the bandwidth of the synthesizer. The synthesizer section also comprises of a phase-lock loop (PLL) and voltage-controlled oscillator (VCO).

The key purpose of the programable LO is to provide the I/Q mixer in this thesis with an accurate and clean signal to mix with the RF input signal. To achieve this, the LO must have reduced:

- Spurs – These are unwanted signal spikes that develops from the parasitic coupling of the stages in the synthesizer.
- Phase noise - This is the caused by thermal, shot and flicker noise within sections of the programable LO which results in a desensitized receiver,

Therefore, the correct reference oscillator, a synthesizer and loop filter need to be selected to provide the least number of spurs and phase noise to the I/Q mixer. Before this can be done, the types of reference oscillators, synthesizers, loop filters and their characteristics needs to be disclosed.

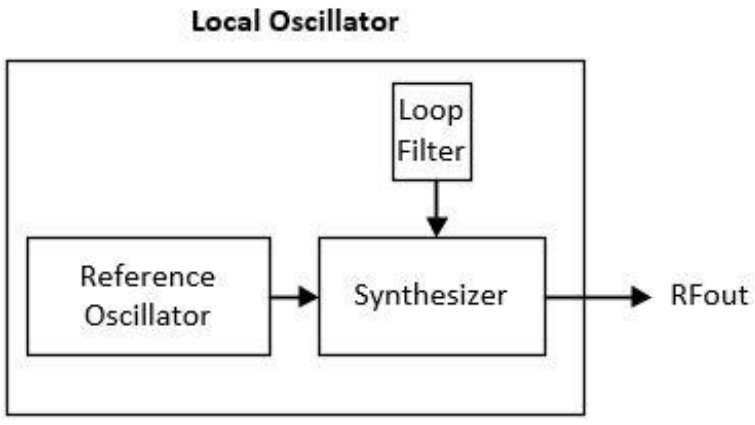

Figure 5.1: Local Oscillator

5.2 Reference to the Synthesizer

The synthesizer needs a stable and accurate reference to generate the required signal frequencies for the I/Q mixer. Stable reference meaning that its temperature stability is acceptable and only deviates within the allowable specified frequency over the rated operating temperature. Accurate reference meaning that it has a frequency tolerance that is acceptable and that it only deviates from the specified frequency at room temperature or 25 degrees Celsius. These specifications are given in parts per million (PPM). This reference to the synthesizer is known as the reference oscillator and there are different types of reference oscillators that can generate this stable and accurate signal. The additional requirement for the SDR environment, however, is to have a reference oscillator that also uses the least amount current to operate, occupy the least amount of physical space and produce the lease amount of phase noise that gets delivered to the synthesizer. Therefore, the reference oscillator will be low in frequency below 50MHz since higher frequency oscillators generally require higher current to operate.

(Rohde and Whitaker, 2001)

5.2.1 Types of Reference Oscillators

5.2.1.1 Oscillator vs Resonator

Generally, an oscillator consists of an active and passive sections as Figure 5.2.The passive section will house the resonator (MEMS, SAW or Quartz) and the active section will have the feedback and amplifier section which supplies the energy to keep the oscillations going. Some active sections will house a phase-lock loop (PLL) to achieve higher accuracy.

Therefore, the resonator is a passive device that will only oscillate when an energy source such as an external amplifier can keep it going. Since the amplifier is external, only oscillators will be disclosed since less components are used to generate an LO.

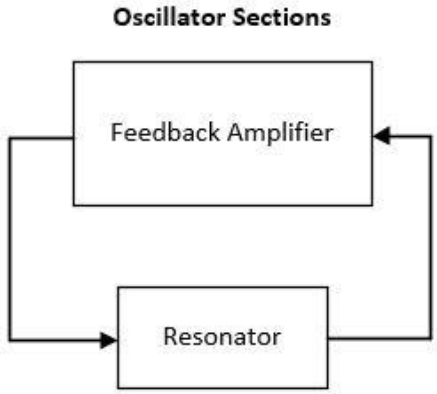

Figure 5.2: Oscillator Block Diagram

(Rhea, 2010)

5.2.1.2 Microelectromechanical System (MEMS) Oscillator

MEMS are the mechanical equivalent of resisters, inductors and capacitors, etched on a silicon substrate as in Figure 5.3 to resonate at the designed frequency. The advantage of this is that it will then come in a small package. The MEMS oscillator uses a factional-PLL active section to sustain accurate oscillations and a temperature sensor to stabilize the output through change in temperature. Because MEMS oscillators use this fractional-PLL they have a large frequency range. The disadvantage though as that this produces more spurs and use more current to operate.

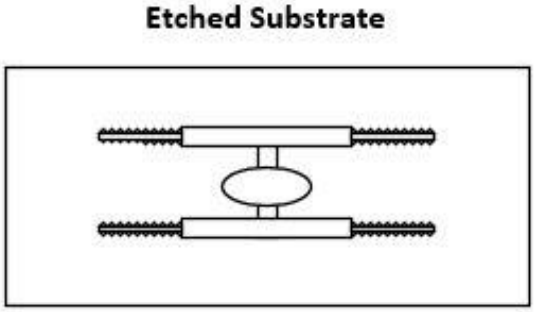

Figure 5.3: Etched Substrate

(Belov, 2012)

5.2.1.3 Surface Acoustic Wave (SAW) Oscillator

SAW oscillators operate differently compared with other types of oscillators as they use acoustic waves to propagate over a piezoelectric substrate to generate oscillations as in Figure 5.4. The substrate consists of an input transducer that translates an electric signal into acoustic waves and an output transducer then reconverts acoustic waves into electrical signals. The SAW oscillator uses FET's or BJT's for its active section therefore uses more current. The

SAW oscillator also increases in size with the decrease in frequency. Therefore, SAW oscillators are generally used at frequencies above 50MHz.

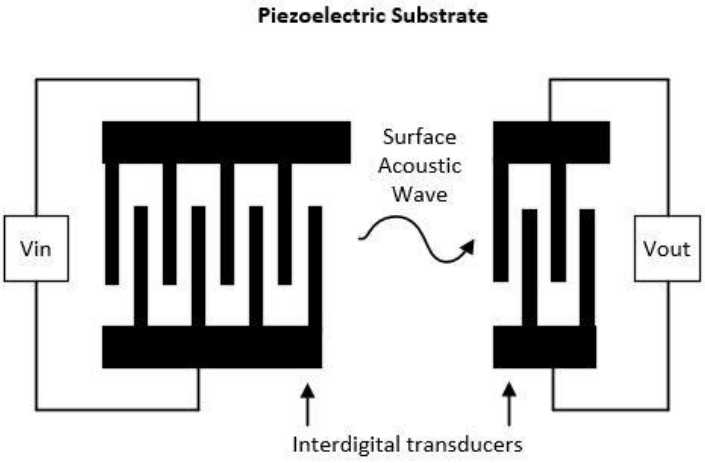

Figure 5.4: Piezoelectric Substrate

(Rhea, 2010)

5.2.1.4 Crystal Oscillator

Crystal oscillators operate by applying a small voltage source to a piezoelectric material such as a quartz crystal as in Figure 5.5 . The quartz crystal then responds by vibrating at the specific frequency. The output electrode then picks up these vibrations as an oscillating voltage that has a specific frequency determined by the cut and size of the quartz crystal. The active section which consists of BJT's, FET's or op-amps, amplifies and feeds this oscillating voltage back into the quartz crystal to sustain the voltage oscillations.

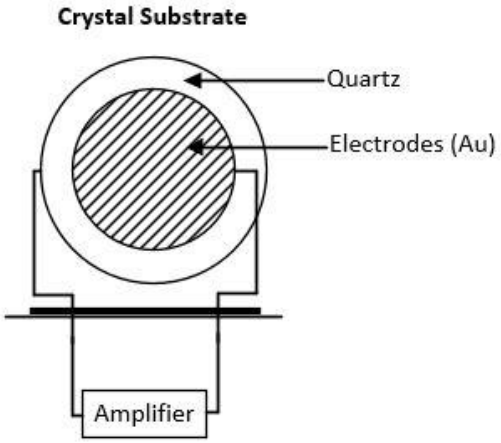

Figure 5.5: Crystal Substrate

(Rhea, 2010)

5.2.1.5 MEMS vs Saw vs Crystal

Reviewing of the https://www.mouser.co.za/ website, information of size and stability can be gathered regarding MEMS, SAW and crystal oscillators. This information as in Table 5.1, shows that the MEMS oscillator can be selected for the smallest package and highest stability. But MEMS oscillators use PLL circuits to increase accuracy and consequently generates more spurs compared with SAW and crystal oscillators. Therefore, MEMS oscillators will not be considered. SAW oscillators can be produced to the same package size as crystal oscillators but has lower stability and therefore will not be considered. Lastly, crystal oscillators have better stability than SAW oscillators, but not as respectable as MEMS oscillators. There are enhanced forms of crystal oscillators that have higher stability compared with MEMS oscillators. These forms of crystal oscillators will be disclosed, and the appropriate form will be considered.

Table 5.1: Types of Reference Oscillators

Type	Package Size (mm^2)	Max Stability (ppm)
SAW	2 x 1.6	50ppm
MEMS	1.6 x 1.2	10ppm
Crystal	2 x 1.6	25ppm

5.2.2 Forms of Crystal Reference Oscillators

5.2.2.1 Voltage-Controlled Crystal Oscillator (VCXO)

The VCXO is a crystal oscillator whose frequency is produced with the crystal inside the VCXO. It also as in Figure 5.6 consists of an active section to sustain the oscillations with an addition of a voltage controlling circuit. The voltage controlling circuit can increase or decrease, also known as pulling, the frequency at which the crystal oscillates. This controlling section consists of a varactor diode whose capacitance increases or decreases with a change in DC voltage and consequently changes the oscillating frequency of the crystal oscillator. The VCXO's ability to change the frequency with a DC voltage helps improve frequency accuracy. The amount of pulling is specified between 100ppm to 200ppm with a DC control voltage of 0V to 3V. Control can be changed manually or can be used in conjunction with additional circuit to adjust the frequency automatically but this results in slightly higher phase noise and circuit complexity. The stability is increased to about ±10ppm.

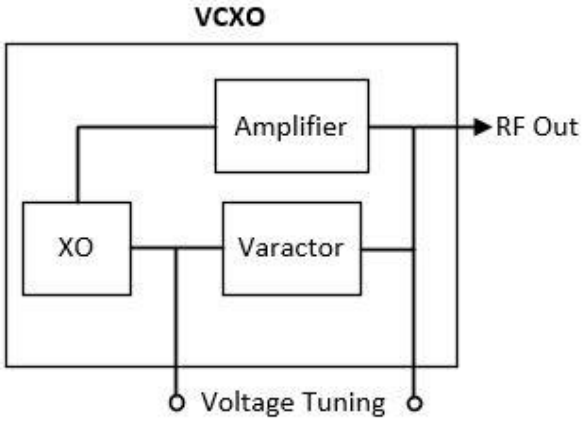

Figure 5.6: VCXO Block Diagram

(Belov, 2012)

5.2.2.2 Temperature Compensated Crystal Oscillator (TCXO)

The TCXO is much like a VCXO, as in Figure 5.7 has an additional temperature sensor and compensation network inside the TCXO package. The compensation network steers the control voltage section of the VCXO that adjusts the frequency automatically. The adjustment or pulling begins when the temperature sensor senses the change in temperature of the crystal (active and passive sections), then generates an output voltage that corresponds with a temperature curve related to the correct output frequency that is required. Since all these processes are built into the TCXO package, this results in better phase noise and less complex circuitry compared with VCXO for the same effect. The stability is increased to about ±1ppm.

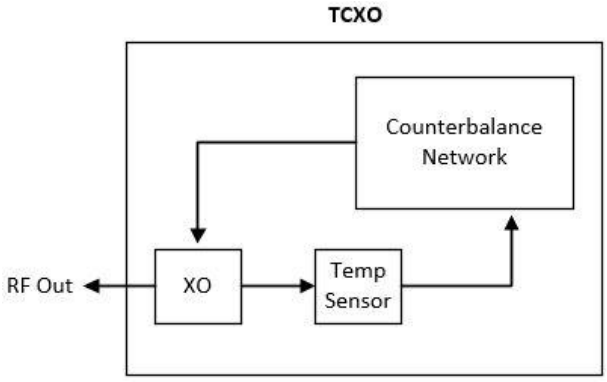

Figure 5.7: TCXO Block Diagram

(Belov, 2012)

5.2.2.3 Oven-Controlled Crystal Oscillator (OCXO)

The OCXO as in Figure 5.8 is like the TCXO where it also has a crystal (active and passive sections) and temperature sensor circuitry (TSC). They differ in that both the crystal and TSC

are housed in a temperature-controlled oven. This maintains the temperature of both the crystal and TSC that increases the stability to about ±0.1ppm. Lastly, the oven control circuitry acts as a VCXO that adjusts the control voltage for the crystal oscillator according to a temperature curve to provide the required frequency. The disadvantage of this is extra circuitry and an increase in package size and results is a higher power consuming module.

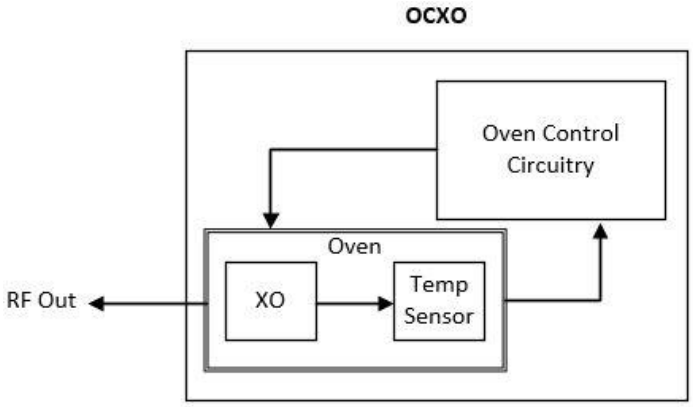

Figure 5.8: OCXO Block Diagram

(Belov, 2012)

5.2.2.4 Voltage-Controlled Temperature Compensated Crystal Oscillator (VCTCXO)

The VCTCXO as in Figure 5.9 also known as a temperature compensated and voltage-controlled oscillator (TCVCXO) is just like a TCXO, but has an advantage of having an external control voltage to adjust the frequency. The adjustment can be used to compensate after when the heat from soldering and PCB assembly is applied to the crystal oscillator that can change the characteristics of the crystal oscillator. It can also be used to adjust the frequency to compensate from the effects of aging. It has the stability of about ±0.5ppm.

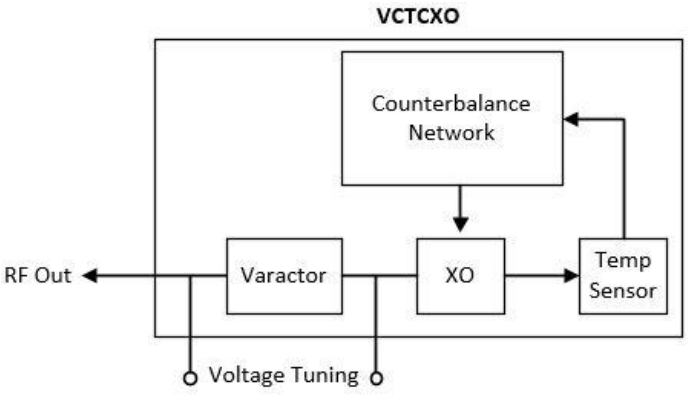

Figure 5.9: VCTCXO Block Diagram

(Goldmen, 2007)

5.2.2.5 VCXO vs TCXO vs OCXO vs VCTCXO

Reviewing the https://www.mouser.co.za/ website, information of stability, voltage supply, max current and phase noise can be gathered regarding VCXO, TCXO, OCXO and VCTCXO, and also considering the package size of the oscillator to be at least 2.5mm x 2mm in size for the SDR environment. This information as in Table 5.2 shows that the OCXO will be best suited for the highest frequency stability possible. But the OCXO will not be considered because it is the biggest of all the size packages compared and has the highest current use. The VCXO comes in a smaller package, but has the lowest stability compared with the others at the 2.5mm x 2mm package size. The VCTCXO has the second highest frequency stability and the smallest size. This amount of stability is not needed and can be expensive. It also needs an extra circuit to supply the control voltage which increases circuit complexity. Lastly, the TCXO with the temperature sensor inside achieves a second highest frequency stability of 2ppm and uses the average amount of current to operate. TCXO oscillators are easier to implement since it doesn't need an extra circuit to utilize the control voltage. Therefore, it will be considered as the reference oscillator for the synthesizer.

Table 5.2: Forms of XO

Type	Package Size (mm^2)	Frequency Stability (ppm)	Supply Voltage (V)	Max Current (mA)
VCXO	2.5 x 2	50	3.3	7
TCXO	2.5 x 2	2	1.8	3.5
OCXO	13 x 20	0.02	3.3	150
VCTCXO	2.0 x 1.6	0.5	1.8	1.5

5.2.3 Parameters

5.2.3.1 Load Capacitance Specification

The crystal manufacturer needs to know what that capacitive load value is to calibrate the crystal so that when placed in the circuit, the frequency of the oscillator will be within the calibration tolerance of the crystal. This is for parallel crystal resonators. The load capacitance refers to all capacitances in the oscillator feedback loop. It is set for what frequency range (15pF, 30pF and 50pF) capacitive loads affect frequency.

(Christiansen and Alexander, 2005)

5.2.3.2 Rise and Fall Time

In terms of logic signals, an ideal square wave has no delay when the output transitions from a high to a low or from a low to a high. In the real world, there is a delay because the square wave isn't perfectly square. Therefore, the rise time is the amount of time, usually in nanoseconds (ns) for the output to change from a logical low to a logic high. The fall time also in nanoseconds (ns) is the amount of time for the output to change from a logical high to a logic low. Where logical low is 10% of V_{DD} and logical high is 90% of V_{DD}.

(Martin, 2000)

5.2.3.3 Phase Noise

Phase noise is the frequency-domain representation of random noise sources such as, thermal, shot and flicker noise. As in Figure 5.10 it is seen as an envelope against the wanted signal and can "drown" the wanted signal and reduce the signal-to-noise ratio. It is measured at various points with reference to the wanted signal. These points are usually at 10Hz, 100Hz, 1kHz, 10kHz, 100kHz and 1MHz from the wanted signal. Phase is given as dBc/Hz because it is measured against a 1Hz bandwidth.

(Moreria and Werkmann, 2016)

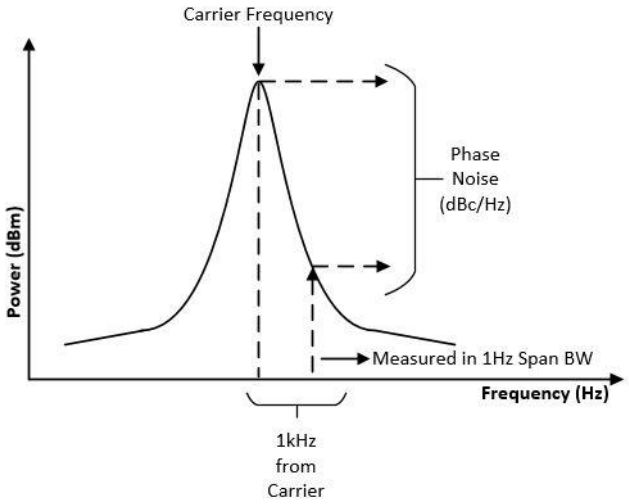

Figure 5.10: Phase Noise

5.2.3.4 Phase Jitter or RMS Phase Jitter

Phase jitter or RMS phase jitter is the phase noise at the carrier frequency integrated over a defined offset range. As in Figure 5.11, by integrating over a range offset of 12kHz to 20MHz

from the carrier frequency determines the phase jitter. This is the pseudo industry standard of calculating phase jitter. Phase jitter is usually in femtoseconds(fs) or picoseconds(ps).

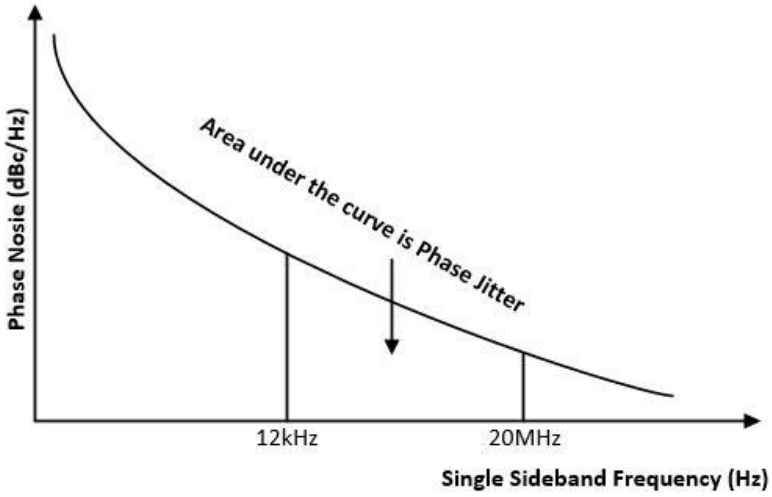

Figure 5.11: Phase Jitter

(Moreria and Werkmann, 2016)

5.2.4 Parameters for Frequency Tolerance and Stability

Frequency tolerance of an oscillator is the amount of deviation from the claimed output frequency due to impurities that are found in the materials that the oscillator is formed from. This deviation range needs to be known so that the engineer can design around this and is given on datasheets in parts per million (PPM) at a room temperature of 25°C ±2°C. For example, if an oscillator has a frequency tolerance of ±1PPM @ 10MHz, it means that the output frequency will be in a range of 9.999990MHz to 10.000010MHz.

Frequency stability of an oscillator is the amount of deviation from the claimed frequency caused by changes such as temperature, supply voltage, load and aging. The deviation range also needs to be declared so that the engineer can design around this and is given on datasheets in parts per million (PPM).

(Cerda, 2014)

5.2.4.1 Deviation caused by Temperature Change

This deviation range is declared since the oscillator might operate in an environment that has a change in temperature. Therefore, the deviation range is given on datasheets usually in a range of -40°C to +85°C. For example, if an oscillator has a frequency temperature stability of

±2.5PPM @ 10MHz for the temperature range of -40°C to +85°C, this indicates that the oscillator will output a frequency of between 9.999975MHz to 10.000025MHz when operated with a temperature range of -40°C to +85°C.

(Cerda, 2014)

5.2.4.2 Deviation caused by Supply Change

This deviation range is declared since the oscillator might operate with a power supply that has voltage tolerance. Therefore, the deviation range is given on datasheets usually at room temperature of 25°C ±2°C with supply tolerance of ±5%. For example, if an oscillator has a frequency voltage stability of ±0.3PPM @ 10MHz with a V_{DD} of 3.3V, this indicates that the oscillator will output a frequency of between 9.999997MHz to 10.000003MHz when operated with a supply voltage of between 3.135V to 3.465V.

(Cerda, 2014)

5.2.4.3 Deviation caused by Load Change

This deviation range is declared since the oscillator might operate with a load that has a certain amount of tolerance. Therefore, the deviation range is given on datasheets usually at room temperature of 25°C ±2°C with a load tolerance of ±5%. For example, if an oscillator has a frequency load stability of ±0.3PPM @ 10MHz with a load of 10pF, this indicates that the oscillator will output a frequency of between 9.999997MHz to 10.000003MHz when operated with a load of between 9.5pF to 10.5pF.

(Cerda, 2014)

5.2.4.4 Deviation caused by Aging

This deviation range is declared since the oscillator properties do change over time. This amount is usually indicated on datasheets as the amount of change per year in PPM when kept at room temperature of 25°C ±2°C. For example, if an oscillator has a frequency aging stability of ±1PPM per year, this indicates that the oscillator output frequency can drift up to 10Hz per year.

(Cerda, 2014)

5.2.5 Parameters for Type of Waveform Output – Single vs Differential

There are two groups that the output waveform of the reference oscillator can fall in. There is a single ended output where there are generally two transmission lines, a ground and positive. Then there is a differential output where there are generally 3 transmission lines, a positive, a negative and common ground.

The advantage of having a differential output is that it provides faster rise/ fall times. This is since differential output oscillators tend to have smaller voltage swings for a high to low state. They also have increased resistance to external EMI and crosstalk. This is since the negative transmission line is inverted and when the positive and negative transmission lines combine on the input of the next stage, EMI and crosstalk is reduced. The disadvantage of having such an output creates the need for more routing traces for the differential signals on the PCB's that can increase circuit complexity. To create the condition to reduce EMI and crosstalk the two differential traces need to be equal in width and length and run parallel with one another. Differential output oscillators also use PLL's to create the differential output and therefore uses more current compared with single ended oscillator output.

Since singled ended output circuits are less complex, use the least amount of current compared with differential output circuits. Therefore, the single ended output will be considered as an output waveform type reference oscillator to the synthesizer. Since there are different types of single ended output, the types and their characteristics first needs to be disclosed to choose the correct single ended output for the SDR environment.

(Sweet, 2007)

5.2.6.1 Single Ended Oscillator Output

5.2.6.1.1 TTL – Transistor to Transistor Logic

TTL singled ended output oscillator requires 5V to operate and are larger components compared with CMOS output. TTL use bipolar transistors to create the logic waveform output and therefore use more current to operate. The output waveform has a voltage range of 0V to 2.4V, where the "High" indicating a logic level 1 is 2.4V, and the logic "Low" indicating a logic level 0 is a 0.4 or 0.5V.

(Scherz, 2013)

5.2.6.1.2 Complementary Metal Oxide Semiconductor (CMOS)

CMOS are used for loads that required logic levels to operate. The output waveform has a voltage range of 0V to 5V, where the “High” indicating a logic level 1 is 4.5V or 90% of V_{DD}, and the logic “Low” indicating a logic level 0 is 0.5V or 10% of V_{DD}.

(Scherz, 2013)

5.2.6.1.1 Low-Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS are used where lower voltages are needed and are only accessible for loads that require logic levels to operate. There are 5 groups of LVCMOS that operate with a V_{DD} of 3.3V, 3V, 2.8V, 2.5V or 1.8V. The output waveform is the same as CMOS where the logic level “High”, indicating a 1 is 90% of V_{DD} and logic level “Low”, indicating a 0 is 10% of V_{DD}. Modern CMOS oscillators are manufactured to operate with LVCMOS voltage levels. Therefore, most modern CMOS oscillators are LVCMOS oscillators even though they are labelled as just CMOS oscillators.

(Pedroni, 2008)

5.2.6.1.3 High-Speed Complementary Metal Oxide Semiconductor (HCMOS)

HCMOS output waveform is a high-speed CMOS and refers to how fast the rise and fall times are per duty cycle. It can be described as the delay in time of the output shifting from a “High” to a “Low” or from “Low” to “High” state. Therefore, the squarer wave like the output the faster the rise and fall times of the output. The old CMOS 40000 series IC’s had 30ns of rise or fall periods and anything shorter than 10ns was referred to as HCMOS. Modern CMOS oscillators are produced with faster than 10ns rise or fall times. Therefore, most modern CMOS oscillators are HCMOS oscillators even though they are labelled as just CMOS oscillators.

(Pedroni, 2008)

5.2.6.1.4 Sine Wave

Sine wave output as in Figure 5.12 are meant to drive 50Ω impedance loads and where PCB traces are designed along 50 Ω impedance. Therefore, if the load is not 50Ω, a matching network must be implemented which can increase circuit complexity. The input voltages that are applied to these types of single ended output is generally 3.3V for a 0dBm output and 5V

for a 10dBm output and therefore require higher currents to operate. They are also generally bigger at about 12mm by 18 mm (L x H) compared with other single ended output TXCO's.

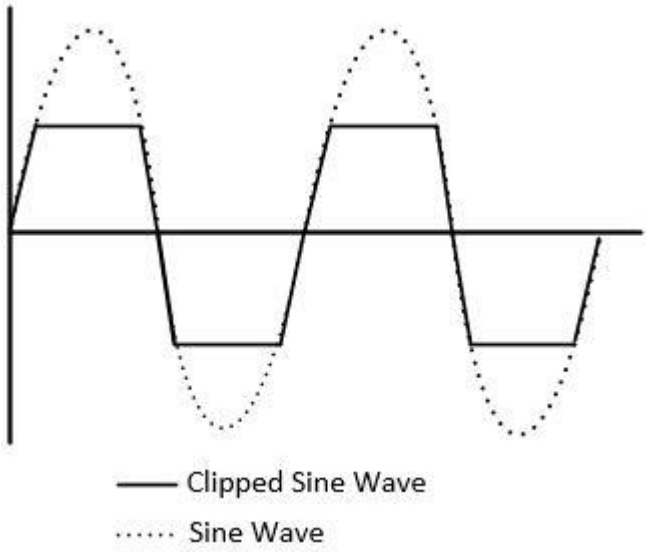

Figure 5.12: Sine Wave and Clipped Sine Wave Output

(Pedroni, 2008)

5.2.6.1.5 Clipped Sine Wave

As in Figure 5.12, by limiting a sine wave output by squaring off the waveform at the maximum and minimum forms the clipped sine wave. The clipped sine wave which is typically now at 0.8V peak to peak plus a DC offset, are used in circuits that can't tolerate the high voltage swings of the normal sine wave and comes with the advantage of having faster rise and fall times. This also allows less current to be drawn for a circuit operation compared with other singled ended output and therefore generates less heat. This attribute is exploited and used for TXCO oscillator designs. The disadvantage though is that now the spectral purity of the waveform is changed and consequently adds harmonics. Clipped sine wave output is intended to drive 10pF and 10kΩ loads.

(Pedroni, 2008)

5.2.6.1.6 TTL vs CMOS vs HCMOS vs LVCMOS vs Sine Wave vs Clipped Sine Wave

TTL oscillators as in Table 5.3 generally don't supply phase noise info on their datasheets and can't be gauged for noise performance. They are bulky and require 5V to function and will not be considered. Modern CMOS output waveform oscillators as in Table 5.3 achieves the same performance as LVCMOS for lower input/output voltage and HCMOS for fast rise and fall times. The sine wave waveform output as in Table 5.3 can offer the best frequency stability for a

TXCO, but because the output waveform has a high swing, the sine wave output oscillator uses the most current and will not be considered. The Clipped sine wave oscillator as in Table 5.3 has its output clipped and therefore uses less current to function with the benefit of having faster rise and fall times compared with the sine wave output oscillators. The stability is also the best at the lowest input voltage. Therefore, TCXO form will be considered as a single ended output waveform type for the reference synthesizer.

Table 5.3: Single-Ended Output Types

Type	**Phase Noise** (dBc/Hz)	**Frequency Stability (ppm)**	**Supply Voltage (V)**	**Max Current (mA)**	**Loads**	**Model**
TTL	N/A	3.5	5	15	10 TTL	ECS-500X
CMOS/LVCMOS/HCMOS	-145@10kHz	1.5	1.8V to 3.3V	6	15pF	ECS-TXO-2520MV or 2520 or AST3TQ53
Sine wave	-140@10kHz	0.5	3.3	12-20	50Ω	TCXO1212BE_Sine
Clipped Sine Wave	-145@10kHz	0.5	1.8V	2	10pf/10kΩ	GTXO-203T

5.3 Synthesizer

The synthesizer generates a range of frequencies for systems in this case for the RF mixer section by using a single reference frequency signal. The stability and accuracy of the synthesizer is dependent on this single reference frequency signal. It generates the range of frequencies by using techniques such as frequency multiplication, frequency division, direct digital synthesis, frequency mixing and the use of a PLL. Characteristics needed for an acceptable synthesizer is broadband operation, very fine frequency resolution, a low spurious signal generation, low phase noise, fast switching speed and low cost. There are 4 types of architecture that can provide these acceptable characteristics. These architecture as seen in Figure 5.13 are called the direct analog synthesis, the direct digital synthesis, the indirect analog synthesis, and indirect digital synthesis architecture.

(Chenakin, 2010)

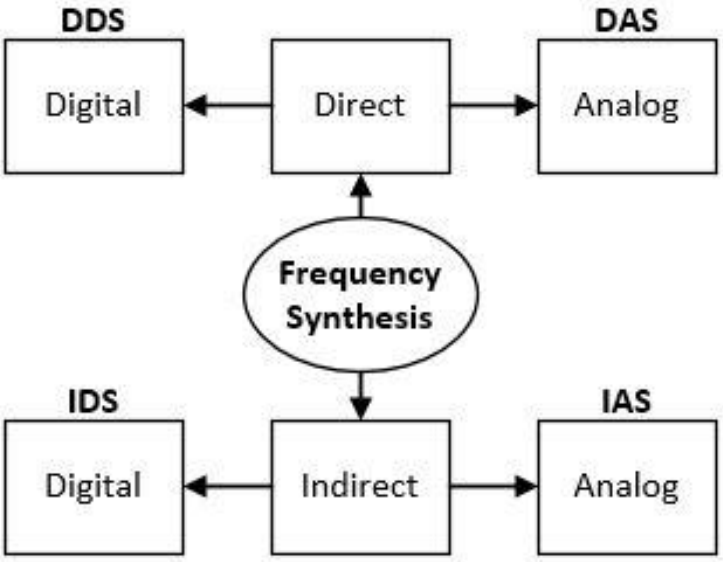

Figure 5.13: Types of Synthesizers

5.3.1 Direct Frequency Synthesis

The direct architecture is produced to create the output signal directly from the reference signal. Altering and merging signals in the frequency domain or building the output waveform in the time domain ensures this. Direct synthesis can be divided into two sub-groups, analog and digital.

(Teppati, Ferrero and Sayed, 2007)

5.3.1.1 Direct Analog Frequency Synthesis (DAS)

DAS as in Figure 5.14 generally consists of multiply references through a bank of crystal oscillators. Many mixers are included to achieve wide band operation. Also included are the use of multipliers and dividers to fine tune the output.

By using this configuration offers excellent purity and high-speed switching, but consequently produces a bulky and complex circuit and are therefore not used for portable devices. Also because of the many components used, consumes more power compared with other frequency synthesizers. Applications are medical equipment or military radar systems.

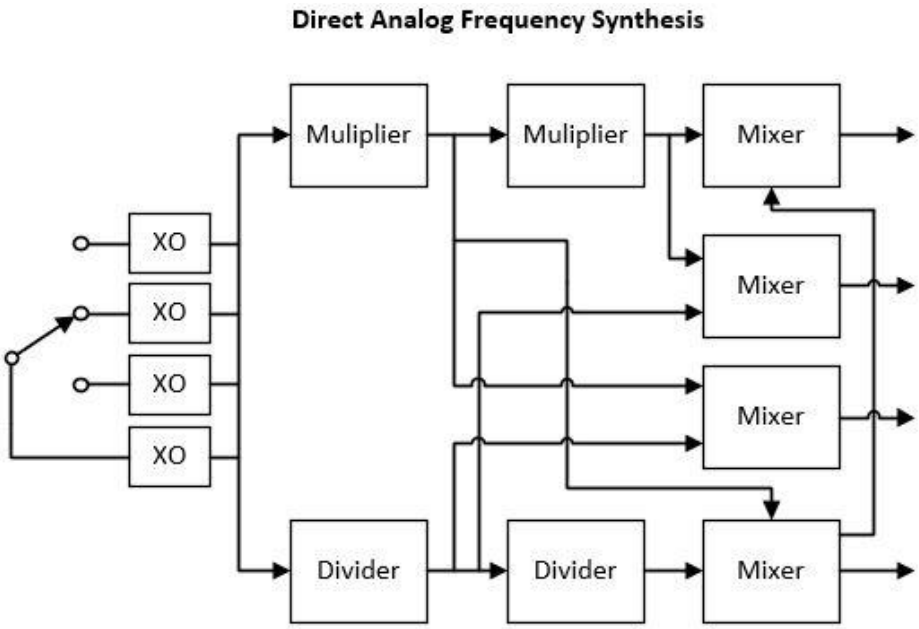

Figure 5.14: DAS

(Dai, Calvin and Rogers, 2006a)

5.3.1.2 Direct Digital Frequency Synthesis (DDS)

DDS as in Figure 5.15 generally consists of digital circuits such as a phase accumulator, phase-to-amplitude converter, a digital-to-analog converter (DAC) and a low pass filter. The frequency reference instructs the phase accumulator on each pulse to advance by a certain amount. The output phase of the phase accumulator is used to select from a lookup table of the phase-to amplitude converter to produce a digital sine-wave amplitude information. This information is then feed into the DAC to produce an analog sine-wave. Lastly, the low pass filter will filter out any high frequency components from the analog signal.

This type of configuration allows fast frequency switching, fine frequency-tuning resolution, and continuous-phase switching. It also allows direct phase and frequency modulations in the digital domain. The disadvantage of this is that there can be high levels of spurious output signals due to limitations of the DAC. To solve this a higher sampling DAC can be used but this increases power consumption.

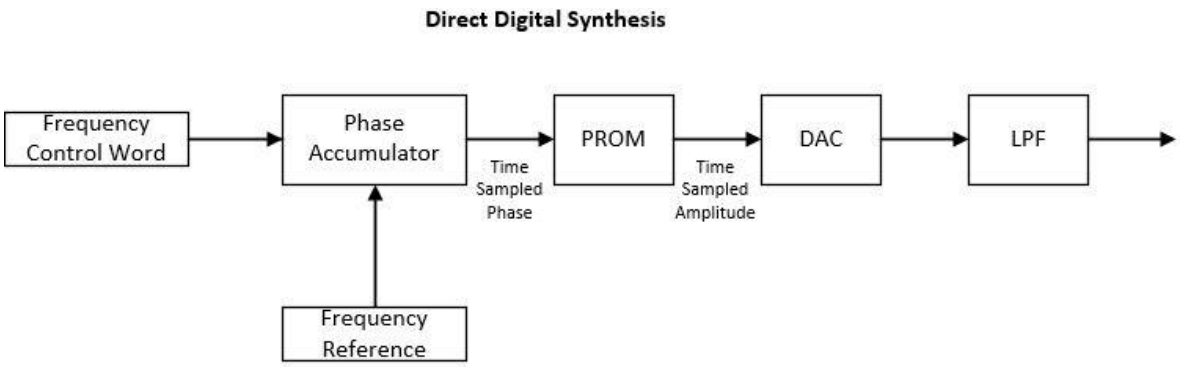

Figure 5.15: DDS

(Dai, Calvin and Rogers, 2006b)

5.3.2 Indirect Frequency Synthesis

The indirect architecture is produced to create the output signal from the reference signal and from a feedback loop oscillator such as a voltage-controlled oscillator (VCO). This consequently highlights the first disadvantage of indirect synthesis as the switching times are fundamentally slower than direct synthesis because of the feedback loop. Indirect frequency synthesis can be divided into two sub-groups, analog and digital.

(Teppati, Ferrero and Sayed, 2007)

5.3.2.1 Indirect Analog Frequency Synthesis (IAS)

IAS also known as analog PLL as in Figure 5.16 generally PLL system or feedback system that consists of analog circuits such as a phase frequency detector (PFD), charge pump (CP), loop filter (LF) and VCO. The PFD produces a current output which is derived from the phase difference between the refence signal and the feedback loop. This constant voltage is feed into the VCO to generate an oscillating signal.

This type of configuration allows a smaller step size and a lower complexity in comparison with direct analog schemes. With no DAC there are less spurious signals generated and use less power. The disadvantage to this type of architecture is that analog components produce long setting times due to narrow bandwidth of the LF. The LF needs to be external because passive components are hard to be scaled down when used in CMOS technology. Because the LF is external, it adds noise and requires additional PCB area.

(Wu, Staszewski and Long, 2015)

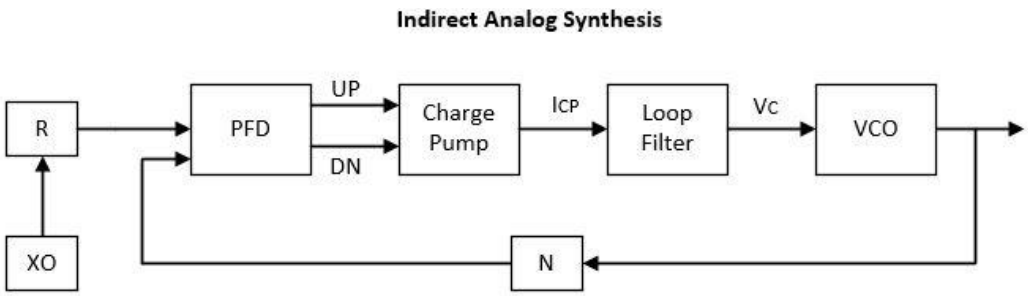

Figure 5.16: IAS

5.3.2.2 Indirect Digital Frequency Synthesis (IDS)

IDS also known as digital PLL as in Figure 5.17 is generally a semi-analog PLL system or feedback system that consists of digital components with no charge pump section since there is no current to voltage conversion required. The digital components are the digital phase frequency detector (DPFD) and the digital loop filter (DLF). The VCO on the other hand, is still in an analog form. When a digital controlled oscillator (DCO) instead of a VCO is used, the architecture is known as an all-digital PLL. The DPFD is called the time-to-digital converter (TDC) which produces a digital code in response to a phase/frequency difference between the output and reference signal. The DF filters the code and then transmits it to the DCO.

(Best, 2003)

This type of architecture being digital or all-digital has the advantage of being implemented in CMOS technology where no external loop filters is required that can influence the circuit negatively. The disadvantage is that now the analog signal is converted to digital form and therefore used in lower frequency applications. When higher frequency applications are needed, a higher bit ADC is needed which increases the power consumption of the circuit. The TDC circuit also have limitations of low resolution which affects frequency step size accuracy, and therefore affect phase noise.

(Chaivipas, Oh and Matsuzawa, 2006)

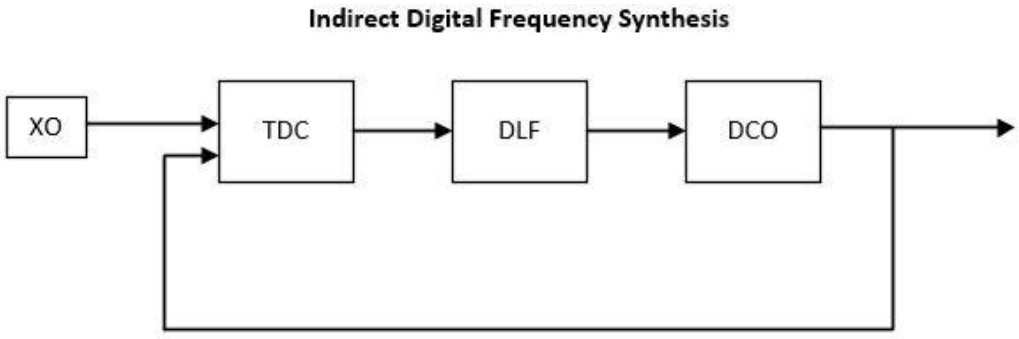

Figure 5.17: IDS

5.3.3 DAS vs DDS vs IAS vs IDS

DAS are generally big as they use banks of crystals to create multiple references and use multiple mixers to create the wide band operation therefore will not be considered. DDS converts the analog error from the reference and oscillator output into a digital form. This creates the higher number of spurious signals compared with analog version. To compensate for this, a higher ADC can be used but this increases power consumption and will therefore not be considered. IDS also suffers from spurious complications because of the limitation on the TDC section that converts signals from an analog to a digital form and therefore will not be considered. Lastly, the IAS architecture suffers from slower switching times, but has the advantage of having lower spurious signal levels. Since the signal remains in an analog form, power consumption is lower compared with the digital architecture and will therefore the IAS architecture will be considered.

5.3.4 Analog PLL Synthesizer

The indirect analog frequency synthesizer (IAS) is the most appropriate synthesizer for the SDR environment. It generally consists of 4 parts, the phase frequency detector (PFD), charge pump (CP), loop filter (LF) and VCO. The IAS in modern times is known as an analog PLL synthesizer and will be referred to as this. There are a variety of analog PLL synthesizers that can be considered for the SDR environment and to select the appropriate one, the analog PLL synthesizer and its characteristics needs to be disclosed.

5.3.4.1 Phase Frequency Detector (PFD)

The PFD section as in Figure 5.16 is sensitive to phase and frequency and the common type is the tristate phase detector. This type is a summing block that has a digital output signal which is feed to the charge pump section. The 3 digital states that it produces is the UP output when the reference signal is ahead of the feedback loop signal, the DN output when the reference signal lags the feedback loop signal, and no output when the reference and feedback loop signal is in phase with one another.

(Rogers, Plett and Dai, 2006)

5.3.4.2 Charge Pump (CP)

The CP section as in Figure 5.16 converts the UP and DN digital signals back to analog form and its main purpose is to provide current into or drain current to ground out of the loop filter.

The UP signal ensures current is provided to the loop filter while the DN signal sinks current to ground.

(Rogers, Plett and Dai, 2006)

5.3.4.3 Loop filter (LF)

The LF section as in Figure 5.16 is a low pass filter that limits high frequency pulses from entering the VCO and main purpose is to convert the current from the CP section to a voltage. By charging the LF's capacitor, increases the voltage over the VCO. This speeds the VCO up. When the VCO output is ahead of the reference signal less current is provided to the VCO through the CP section and therefore slows down the VCO output.

(Rogers, Plett and Dai, 2006)

5.3.4.4 Voltage-Controlled Oscillator (VCO)

The VCO as in Figure 5.16 increases the output frequency or lowers the output frequency in response to the output voltage of the LF. When the reference oscillator frequency is ahead, the PFD output an UP digital signal that causes the CP section to increase in current, that charges the capacitor of the LF and therefore increases the voltage of the VCO and therefore output frequency increases. When the feedback loop frequency is ahead, the PFD output a DN digital signal that causes the CP section to decrease in current, that discharges the capacitor of the LF and therefore deceases the voltage of the VCO and therefore output frequency decreases.

(Rogers, Plett and Dai, 2006)

5.3.4.5 The Division Ratio R

This is the division ratio that is in line with the reference oscillator just before the PFD. The function of the division ratio R is to generate the desired reference frequency for the applied N value and calculated the output signal as in:

$$Output\ Frequency\ =\ N\ \times\ Reference\ Frequnecy \tag{5.1}$$

(Rohde and Newkirk, 2000)

5.3.4.6 The Division Ratio N

This is the division ratio that is fed into the PFD and has the origin from the output of the VCO. The function of the section is to achieve smaller steps between channels of frequencies.
The division ratio N can be categorized into two modes called integer – N and fractional – N.

(Rohde and Newkirk, 2000)

5.3.4.6.1 Inter-N Frequency

The integer-N synthesizer only allows integer values of N to be used in this equation and allows for step sizes of tens of kilohertz. Since the N value used to achieve the calculated output frequency is generally in the thousands, inserting the N value into the equation:

$$Phase\ Noise = 20 * \log N \quad (5.2)$$

Results in a high phase noise. The higher N value also results in the loop filter bandwidth to be very low in order to operate. This causes slow lock times.

(Rohde and Newkirk, 2000)

5.3.4.6.2 Fractional -N Frequency

The fraction-N synthesiser allows for lower N values and for step sizes of tens of hertz. Consequently, this allows also for smaller N values from the division ratio R section. This also allows the noise performance to improve. Therefore, lower N values reduces the lock times because the loop filter can now use a wider bandwidth of operation.

(Rohde and Newkirk, 2000)

5.4 Loop Filter (LF)

The LF is generally a 2nd order low pass filter as Figure 5.18. The loop order can be increased which can offer better noise filtering but decreases loop stability and extra care needs to be taken to keep the loop stable. The loop bandwidth influences the lock time of the VCO, therefore wider bandwidths are preferred, but a trade-off is required since a higher bandwidth loop increases the level of spurious signals. The phase margin is kept between 30 and 60 degrees therefore 45 degrees is the general phase margin used.

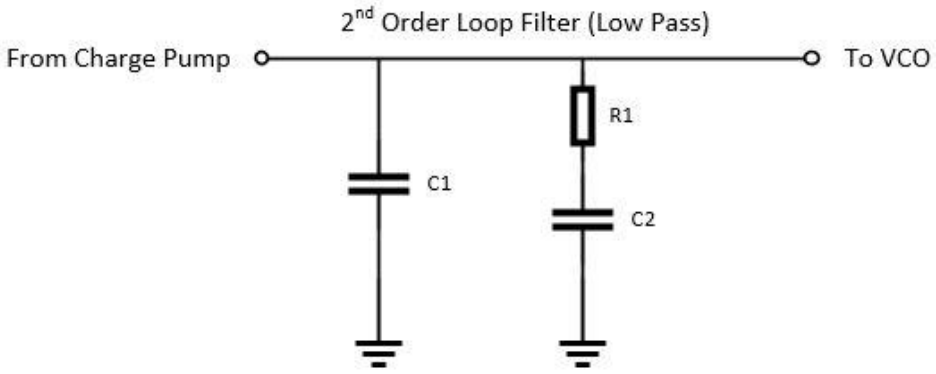

Figure 5.18: 2nd Order Low Pass Loop Filter

(Best, 2003)

5.4.1 Determining the Loop Filter

The LF is determined with known parameters of the system such as:

- The frequency Range.
- Channel Spacing.
- Loop Bandwidth.
- VCO Sensitivity.
- Charge Pump Current.

5.4.2 Term Definitions of the Loop Filter

The term definitions are given as:

- F_A is the center frequency.
- F_N Natural Frequency.
- F_{STEP} is the maximum frequency step.
- I_{CP} is the charge-pump current.
- K_{VCO} is the VCO sensitivity.
- T_S is the lock time.
- ξ is the damping factor which is 0.707.

5.4.3 Calculating the Loop Filter

The LF is calculated as:

$$Fstep = Maximum\,VCO\ frequency - minimum\,VCO\ Frequency \tag{5.3}$$

$$N = \frac{Maximum\,VCO\ Frequency}{Channel\ Spacing} \tag{5.4}$$

$$F_N = \frac{2 * Loop\ Bandwidth}{2\,\pi\left(\xi + \frac{1}{4 * \mathrm{Z}}\right)} \tag{5.5}$$

$$C_2 = \frac{I_{CP} * K_{VCO}}{N * (2\pi * F_N)^2} \tag{5.6}$$

$$R_1 = 2\,\xi * \sqrt{\frac{N}{I_{CP} * K_{VCO} * C_2}} \tag{5.7}$$

$$C_1 = \frac{C_2}{10} \tag{5.8}$$

$$T_S = \frac{-1 * \left(\ln \frac{F_A}{F_{STEP}}\right)}{F_N * 2\pi * 2\xi} \tag{5.9}$$

(Venkateswararao and S. Ramesh, 2012)

5.5 Chapter Summary

Section 5.2.1.5 surmises that the crystal type of oscillators is best suited for a synthesizer in the SDR environment even though it is not that accurate or tiny like the MEMS type of oscillator. Crystals produce less spurs than MEMS. The SAW type of oscillator comes in at the same size as crystal type oscillators but has lower stability and was not considered.

Section 5.2.2.5 surmises that the TCXO is the best form of the crystal oscillator even though it has the second highest frequency stability of 2ppm. TXCO's use an average amount of current to work compared with OCXO's, VCXO's and VCTCXO's. They are also easier to implement since it doesn't need an extra circuit for to utilize the control voltage.

Section 5.2.6.1.6 surmises that a single ended, clipped sine wave oscillator output is the best choice for TXCO, crystal oscillator. The clipped sine wave has the benefit of having faster rise and fall times compared with the sine wave output oscillators. The stability is also the best at the lowest input voltage compared with TTL, CMOS, HCMOS and LVCMOS single ended output.

Section 5.3.3 surmises the indirect analog frequency synthesis (IAS) is the best choice for frequency generation for a synthesizer. It is smaller than the digital analog frequency synthesis (DAS) that also uses more current, have less spurious signals compared with a direct digital frequency synthesis (DDS) and the indirect digital frequency synthesis (IDS). When DDS's and IDS's achieves lower spurious signals level it uses faster ADC's which in turn consumes more power.

Lastly, the loop filter for the synthesizer will be a 2^{nd} order filter to increase loop stability. The phase margin will be at 45 degrees to also keep loop stability.

Chapter 6

Radio Frequency Switch

6.1 Introduction

The radio frequency (RF) switch is used to switch signals from one or more inputs to generally a single output. In the case of the down converter, signals must be switched from two difference inputs. The 30MHz to 300MHz input and the 300MHz to 12Ghz input. Therefore, the correct RF switch needs to be selected to suite the application. Before this can be done, the types of RF switches and their characteristics needs to be disclosed.

6.2 RF Switch Categories

6.2.1 Poles and Throws

The poles signified with P, is the amount of input circuits the switch has. The throws signified by a T, is the amount of output circuits that can be linked to the input. Therefore, switches are named as a single pole single throw (SPST), indicating single input and single output, single pole 6 throw (SP6T), indicating single input with a possibility of 6 separate output circuits. Lastly, there are also named 4 pole 2 throw (4P2T), indicating a possibility of 4 different input circuits can be connected to 2 possible separate circuits. Most RF switches are bidirectional, meaning that it can be used in both directions. Where a SPDT switch can be used as a switch with one input to two outputs or two inputs to one output.

(Weisman, 2002)

6.2.2 Absorptive or reflective mode

The absorptive RF switch is a switch where the throw that is not connected to the common pole (off state) is terminated in 50 Ω. While the reflective RF switch is a switch where the throw that is not connected to the common pole (off state) is open/shorted with a high VSWR. Therefore, the absorptive RF switch will have a good VSWR on both throw ports even if then switch is in an off or on state.

(Keysight Technologies, 2017c)

6.2.3 Latching or Failsafe

The latching RF switch is a switch that always needs power and control signal to change the position of the switch and remains in that position until power and a control signal is used to switch the position of the switch. The failsafe RF switch will return to the default position when power is removed.

(Cigoy, 2008)

6.2.4 Make-Before-Break or Break-Before-Make Configuration

The most common configuration of a multi-position switch like this is one where the contact with one position is broken before the contact with the next position is made. This configuration is called break-before-make. While applications where it is unacceptable to completely open the circuit attached to the “common” wire at any point in time. For such an application, a make-before-break switch configuration is used.

(Cigoy, 2008)

6.2.5 Cold or Hot Switchable

When the RF switch is referred to as a hot RF switch, indicates that the switch will take no damage when changing switching states when there is a signal present at the common pole. While a cold RF switch will not be able to switch into different states when a signal is present at the common pole.

(Keysight Technologies, 2019)

6.3 The RF Switch Types

The RF switch can be divided into the way the switching of the throw is done. When contact is physically made through an electromagnetic induction it is called an electrotechnical (EM) switch. When contact is made without moving parts and through semiconductors, it is called a solid-state switch. Lastly, when the switch contains moving physically parts and integrated semiconductors to improve performance it is called a micro-electromechanical systems (MEMS) switch.

6.3.1 The Electromechanical (EM) RF Switch

The EM RF switch has the most favorable parameters of all the switch types. It can be used from DC to high frequencies, provide low insertion loss and good isolation when in off-state because there is no physical connection. It has from the highest power handling too. But because EM switches rely on mechanical moving contacts, they are susceptible to vibration and therefore has the lowest operating life. The switching mechanism also means the EM switch has the worst switching and settling time. The insertion loss over time increases because the contacts become damaged from continues switching of contacts from on to off-state.

(Keysight Technologies, 2017b)

6.3.2 Solid-State RF Switch

The main purpose of the creation of this switch is to remove all moving parts. This increases reliability and extends the switch characteristics by eliminating the possibly of erosion of the contacts or failing of the switch by shock and vibration effects. The solid-state switch is further categorized according to the type of semiconductor martial is created from.

(Christiansen and Alexander, 2005)

6.3.2.1 Positive-Intrinsic-Negative (PIN) Diode RF Switch

The PIN diode RF switch consists of P-type and N-type regions separated by a resistive intrinsic center I-region. The forward biasing current of the PIN diode controls the I-region. Where the current is inversely proportional to the resistance of the diode. When in forward biased mode, the forward current pushes the P-region to produce positive charges to the I-region and pushes the N-region to produce negative charges to the I-region. This increases the conductivity and thus decreases the insertion loss. To achieve an Off-state the PIN diode is reversed or zero biased, which decreases the I-region conductivity, and this increases the isolation. If the diode has high total capacitance the higher frequency signals tend to increase insertion loss and decrease isolation. Therefore, PIN diodes functioning at high frequencies will have a low total capacitance. Where the total capacitance of a diode is the junction capacitance and parasitic capacitance. At lower frequencies the minority carriers prevent the PIN diode from operating and therefore becomes more like a PN diode at lower frequencies. The minority carrier lifetime, known as τ is used in the equation:

$$f = \frac{1}{2\pi\tau} \quad (6.1)$$

This is used to calculate the point at which the PIN diodes stars operating as a PN diode. Thus, the PIN diode RF switch would not be used for low frequency processes.

(Keysight Technologies, 2017a)

6.3.2.2 Gallium Arsenide (GaAs FET) RF Switch

The FET has 3 functional pins. The gate, the source and the drain. When a voltage is applied the gate, a channel is created in the depletion layer for current to flow form from the drain to the source. This is called an RDS On-state and in general has a very low impedance and therefore a very low insertion loss. When in the RDS Off-state, the depletion region increases and prevents current from flowing. This results in a high impedance and therefore a high isolation in the Off-state. The disadvantage of the FET switch is that the higher the frequency the lower the Off-state impedance gets and therefore the isolation decreases. Thus, FET switches are not suitable for higher frequencies, but are suitable from DC where the isolation is at its highest.

(Keysight Technologies, 2017a)

6.3.3 MEMS Switch

The MEMS RF switch has smaller contacts. The electrostatic force is still used to switch the contacts to make the RF connection. They are further categorized into 2 groups.

(Lucyszyn, 2012)

6.3.3.1 Ohmic MEMS RF Switch

These switches operate with metal to air to metal (MAM) contacts that have a very small surface area. This provides a very low ON-state resistance for better insertion loss and when in Off-state, a small parasitic capacitance for better isolation. But since there are moving contacts, it is susceptible to corrosion and where contacts can bond together.

(Lucyszyn, 2012)

6.3.3.2 Capacitive MEMS RF Switch

These switches operate with metal to insulator to metal (MIM) contacts and as the name states it has an insulator in between contacts. This gives the switch the advantage of decreasing the ON-state resistance even further and thus the insertion loss. The disadvantage of this is because the electrode surface area increases, the Off-state isolation decreases. The advantage of these switches compared to ohmic switches, they have higher peak RF power levels, reduced damage during hot switching and thus longer lifetime.

(Lucyszyn, 2012)

6.4 Parameters of RF Switch

6.4.1 Voltage Standing Wave Ratio (VSWR)

Generally, RF switches are connected to sources and loads that have characteristic impedance of 50Ω. Therefore, the input and output of the RF switch needs to be matched to a 50Ω characteristic impedance so that all the power can be transferred to the source and load. If this is not implemented, some to all the power will be reflected to the RF switch where it will potentially heat up and oscillate. The VSWR of the RF switch is thus an indication of how much power will be reflected to the RF Switch by the system it connected too. It can also be an indicator of how well the RF switches' input and output is matched to the characteristic impedance of the system. VSWR ranges from 1 to infinity. When the VSWR of the RF switch is 1, it is matched to the characteristic impedance and no power will be reflected towards the RF switch. When the VSWR is infinity, all the power will be reflected towards the RF switch. VSWR is a unit less value.

(Keysight Technologies, 2017c)

6.4.2 Return Loss

The return loss of the RF switch is an indication of the amount of power that is lost. This is due to either the source or load impedance mismatch. The return loss is also a ratio between the power incident and reflected by the RF switch and is expressed in dBs. The higher the return loss, the better the RF switch is matched to the characteristic impedance.

(Keysight Technologies, 2017c)

6.4.3 Insertion Loss

In an ideal world, the RF switch will transfer power from a source to a load of a system without any losses. In the real world, the RF switch absorbs this power. The amount of power that is absorbed is known as the insertion loss of the RF switch. The insertion loss is thus the ratio expressed in dBs between the input power and output power of the RF switch.

(Keysight Technologies, 2017c)

6.4.4 Isolation

Isolation is the ability of the RF switch to prevent signals from the ports from leaking into one another. The higher the isolation between the ports the more higher-powered signals can be switched without interfering with one another. For a SPDT switch, the datasheets will give the isolation between the common (pole) and RF1 and RF2 ports (throws). The datasheet will also give the isolation between the RF1 and RF2 ports (throws).

(Keysight Technologies, 2017c)

6.4.5 3rd Input Intercept Point (IIP3)

IIP3 is an indication of how much the 3rd order products, specifically 2*F1-F2 and 2*F2-F1 are attenuated relative to their fundamental signals when the two signals F1 and F2 are presented at the input ports of the RF switch. The higher the value of IIP3, the more linear the RF switch will be. The 3rd order products can be seen in Figure 6.1.

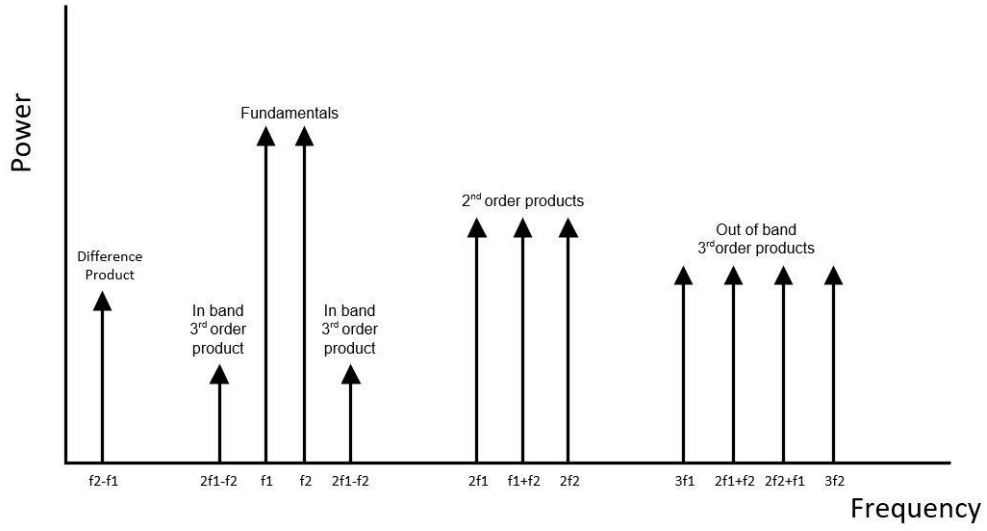

Figure 6.1: IM2 and IM3 Products

(Poisel, 2014)

6.4.6 2nd Input Intercept Point (IIP2)

IIP2 is an indication of how much the 2nd order products specifically 2*F1, 2*F2 and F1+F2 are attenuated relative to their fundamental signals when the two signals F1 and F2 are presented at the input ports of the RF switch. The higher the IIP2 the more linear the RF switch. The 2nd order products can be seen in Figure 6.1.

(Poisel, 2014)

6.4.7 0.1dB Input Compression Point

The 0.1db compression point is an indication at which input power level in dBm, the output power saturates and deviates from the ideal level by 0.1dB as in Figure 6.2.

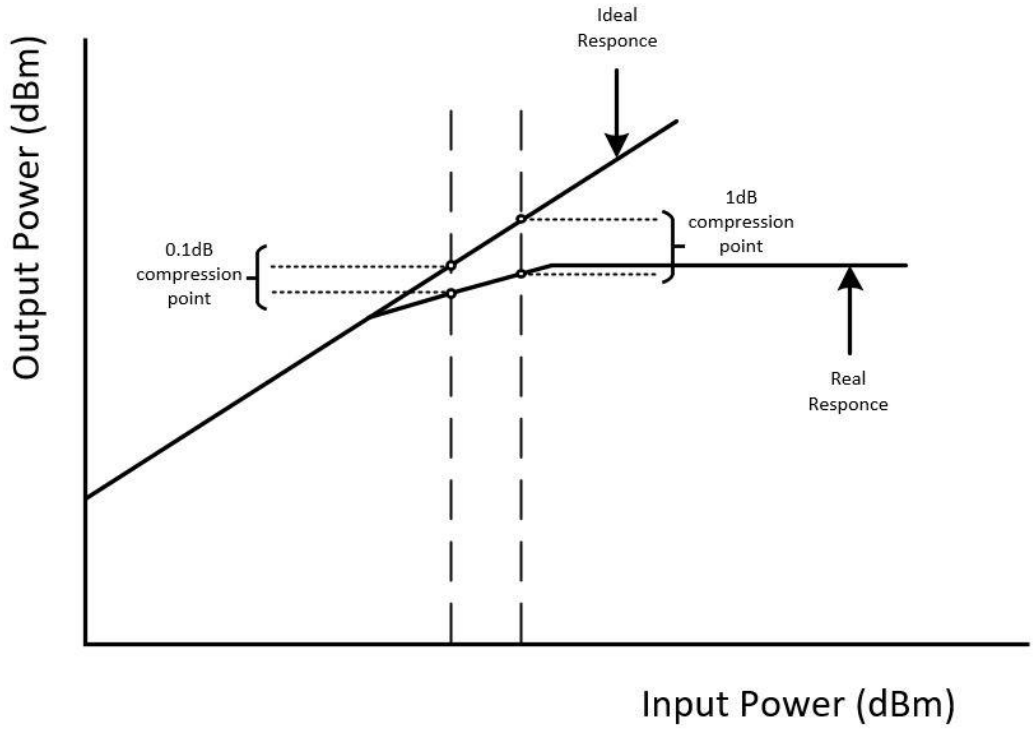

Figure 6.2: The Compression Point

The RF switch is never operated at the 0.1dB input power level as the RF switch will be very close to compression. It is typically operated 3db below the 0.1db input compression point.

(Poisel, 2014)

6.4.8 Switching Speed

The switching speed of the RF switch is the time it takes for the switch to change state, i.e. disabling one port and enabling the other to allow the RF signal to be transferred through the switch. This time is usually 90% of the final RF signal power level. The switching speed can be further divided into t_{RISE}/t_{FALL} and t_{ON}/t_{OFF}

6.4.8.1 Rise and Fall Timing

T_{RISE} is the time the RF switch takes to enable the desired port to transfer the RF signal. This is the duration of time taken where the transferred RF signal power level changes from 10% to 90% of the final RF signal maximum level as seen in Figure 6.3. T_{FALL} is the time the RF switch takes to disable the undesired port to not transfer the RF signal through and where the RF signal power level drops from 90% to 10% of its maximum level. These time durations do not include the delay caused by the switch driver control circuit.

(Keysight Technologies, 2017c)

6.4.8.2 On and Off Timing

The RF switch driver circuit also adds delay to the switching time. The t_{ON} time is therefore the time that the driver circuit control signal shifts from 50 to 90% plus the t_{RISE} time as seen in Figure 6.3. The t_{OFF} time is the duration of the time the driver control circuit signal shifts from 50% to 90% of its maximum level plus the t_{OFF} time as in Figure 6.3. Thus, the driver control-signal delay time for switching “on” the RF switch can be calculated by taking the $t_{ON} – t_{Rise}$ and the driver control-signal delay time for the switching “off” of the RF switch can be calculated as $t_{OFF} – t_{FALL}$.

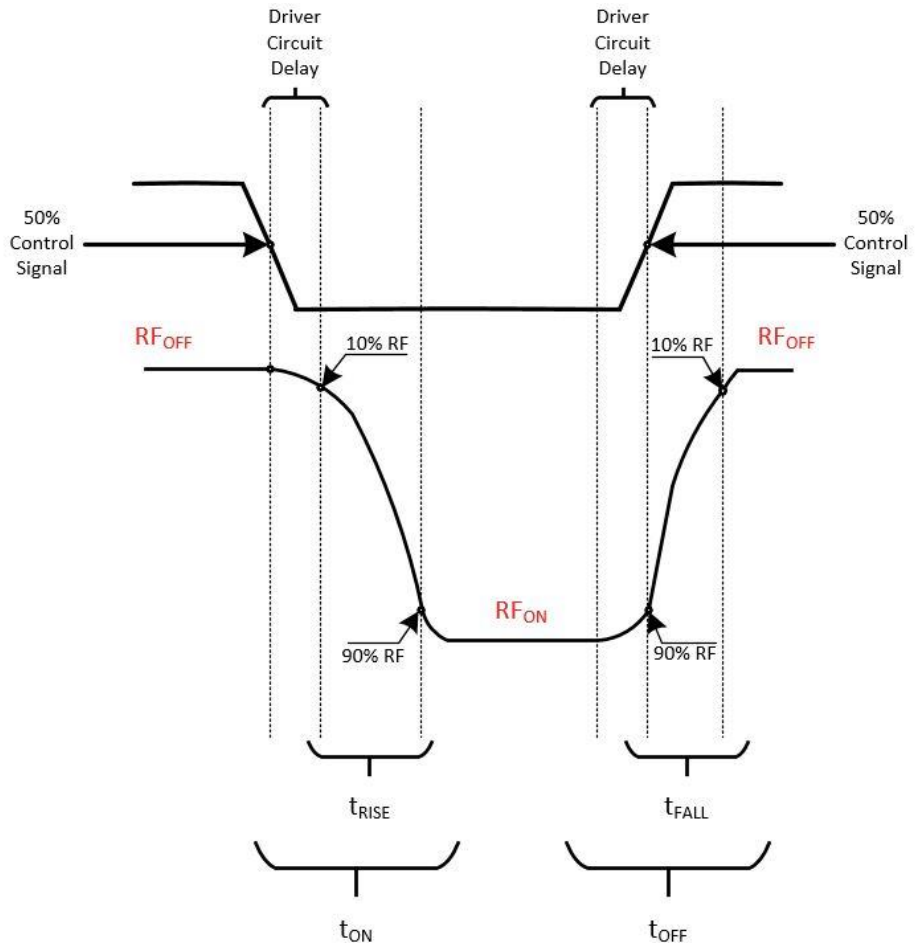

Figure 6.3: Switching Time of the RF Switch

(Keysight Technologies, 2017c)

6.4.9 Settling Time

For more accuracy, the settling time was derived and is given for either:

a. When the transferred signal through the switch reaches 99.77% of its maximum power level or within 0.01dB of the RF signal power level
b. When the transferred signal through the switch reaches 98.89% of its maximum power level or 0.05dB of the RF signal power level.

(Keysight Technologies, 2017c)

6.4.10 Video Leakage

These are spurious signals that are generated when the switching mechanism is operated when no signal is applied to the ports. The signals are generated from the switch driver control circuitry, specifically from the leading-edge voltage spike. Video leakage is specified on datasheets at a specific frequency with a maximum voltage measured in mV_{p-p}.

(Keysight Technologies, 2017c)

6.5 Chapter Summary

The SDR environment requires a device that is compact and operates with the least amount of current. Although the electro-mechanical switch has the overall best insertion loss, peak isolation and lowest VSWR, it is susceptible to shock and vibrations. It is also the largest in component size and will therefore not be considered. The MEMS have micro-mechanical parts and will wear faster over time compared to solid state switches. The solid-state switch will be considered since the switching speed is fast and the fact that the switch will be used to receive which doesn't require high power capabilities.

The down converter will have two receive windows. The low frequency window range that covers the VHF to 2GHz frequencies, and the high frequency window range that covers the 2GHz to X-band frequencies. Therefore, a bidirectional SPDT switch will be required to switch two receive signals to the SDR. The switch will be absorptive so that when it is in off mode, the port not used will be internally terminated to 50Ω load. The switch will be latching so that when power is removed, the last selected port will still be used. A break-before-make configuration will be used to not allow the two receive windows to momentarily short between one another and a hot switching configuration will also be used to as both receive windows will be active all the time.

Chapter 7

Radio Frequency Quadrature Coupler

7.1 Introduction

The radio frequency (RF) coupler is a passive 4-port device as in Figure 7.1 that commonly contains two transmission lines that run parallel with one another. These transmission lines don't physically touch one another and are known as directional or dual directional couplers. The RF coupler can sample high-power signals to feed sensitive test equipment by coupling a small sample of the full power. RF couplers that have continuous transmission lines that run in a loop are used to divide or combine signals where the coupler is known as a hybrid or quadrature coupler. These couplers can also be used to change the phase of a signal. In terms of the thesis the RF quadrature coupler would combine the I and Q signals generating the IF signal. There are different types of RF quadrature couplers, but only one type of coupler is suitable for this type of application. In order to select the correct RF quadrature coupler, the type of RF couplers and their characteristics needs to be disclosed.

(Maloratsky, 2012)

7.2 Types of RF Couplers

7.2.1 Directional Coupler

A Directional coupler as in Figure 7.1 is generally a linear 4-port passive device that has an input port, through port, coupled port and isolated port. Power flows in one direction from port 1 to port 2 and coupled to port 3, where some power gets reflected from the load connected to the directional isolated port internally.

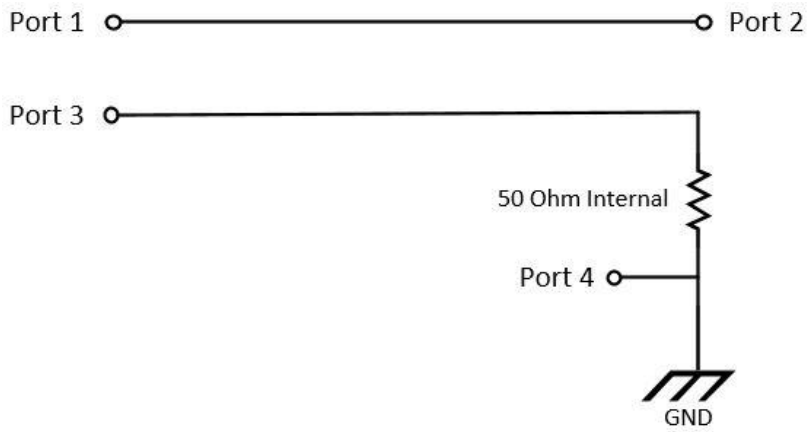

Figure 7.1: Directional Coupler

7.2.1.1 Input Port

Incident power is applied to the input port. Components inside the coupler limits the incident power level before the coupler acts non-linearly. This maximum incident power level value is provided on the datasheet of the coupler.

7.2.1.2 Through Port

The through port is directly connected to the input port and has a power level output of generally nine tenths of the input port (-1db).

7.2.1.3 Coupled Port

The coupled port physically doesn't touch the input or through port. The power level of the signal at the coupled port depends on how far the transmission coupled line is from the input port, transmission line as in Figure 7.2. Generally, the power level of the coupled signal is the other one tenth of the input port (-10dB).

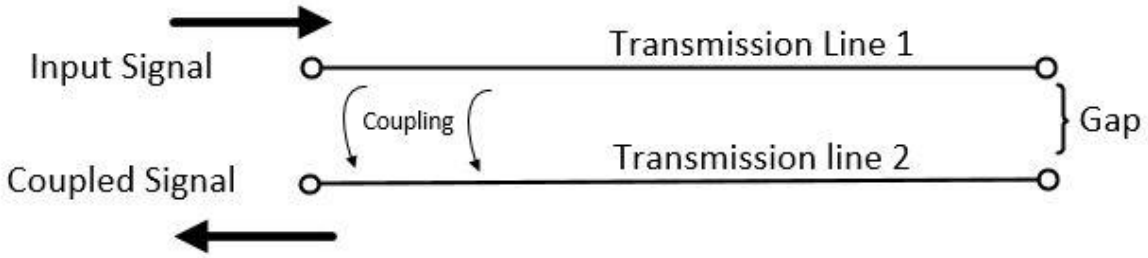

Figure 7.2: Through and Coupled Lines

7.2.1.4 Isolated Port

In an ideal directional coupler, there will be no signal at the isolated port. But generally, some power is reflected back from the load when the load, the directional coupler is connected to is not 50Ω impedance. Therefore, the isolated port needs to be terminated with a 50Ω impedance load to provide correct coupled power at the coupled port. The isolated port in some directional couplers in loaded internally and is offered as a 3-port directional coupler device.

(Laverghetta, 2005)

7.2.2 Bi-Directional Coupler

Directional couplers are bi-directional couplers that have an isolated port which is terminated in 50Ω. This helps absorb reflections. The 50Ω termination can be moved by the user between the coupled transmission line ports. When the power is incident on port 1 as in Figure 7.3, port 3 becomes the coupled port, port 4 becomes the isolated port and port 2 becomes the through port. Otherwise, when the power is incident at port 2 the coupled port is now port 4, the isolated port is now port 3 and through port is port 1.

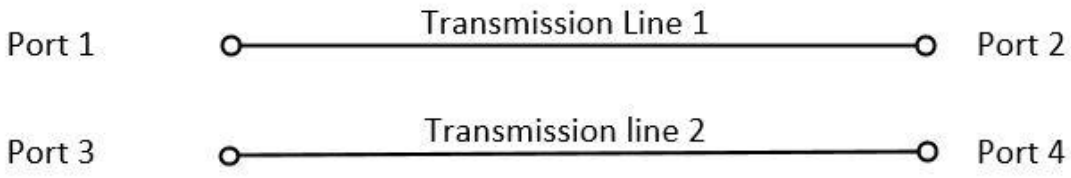

Figure 7.3: Bi-Directional Coupler

(Kinley, 2004)

7.2.3 Dual Directional Coupler

A dual directional coupler is a coupler that can sample forward and reflected power from the load it is connected to at the same time. As in Figure 7.4, if a signal is incident at port 1, the through port will be port 2, the sampled forward power will be on the output of port 4 and sampled reflected power will be on the output of port 3. This type of coupler can be visualized as two bi-directional couplers placed back-to-back, with a 50Ω load internally connected to port 4 and 3. This also enables the dual directional coupler to be connected to loads that are not 50Ω and will not affect the directivity of the coupled ports.

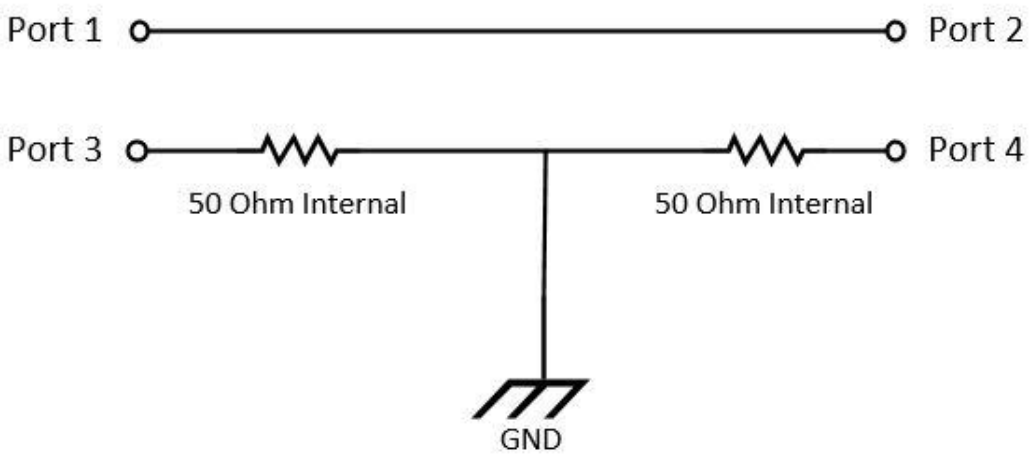

Figure 7.4: Dual Directional Coupler

(Maloratsky, 2012)

7.3 Types of Quadrature Directional Couplers

The types of RF couplers were disclosed in the previous section. For the next section, the type of couplers that adds a 90° phase to one of the inputs will be divulged. This type of coupler is known as a quadrature RF coupler. Since there are different types of quadrature RF couplers that can create this 90° phase shift, and in order to select the correct RF quadrature coupler, the type of quadrature RF coupler and their characteristics also needs to be disclosed.

7.3.1 Branchline Coupler

The branch-line coupler as in Figure 7.5 have two different characteristic impedances and four $\frac{\lambda}{4}$ lines. With $Z_1 = Z_2 * 0.707$ being the quarter-wavelength in length transmission lines above and below the coupler and $Z_2 = 50\Omega$ being the quarter-wavelength length transmission lines connecting the two. The through and coupled port has a 90° difference and equally divided power between the two. This coupler is easily implemented but has a disadvantage of having a narrow bandwidth of operation.

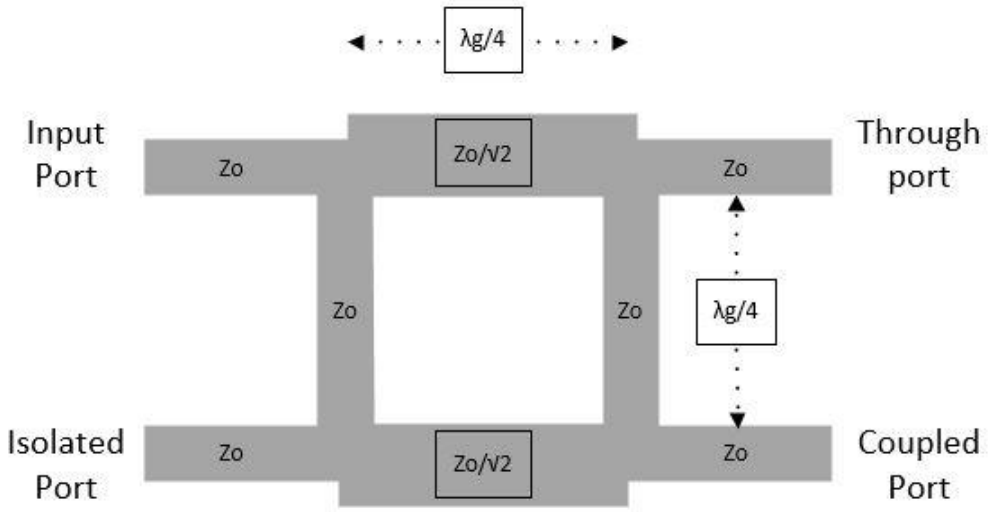

Figure 7.5: Branch Line Coupler

(Mongia,R.K, Bahl, I.J, Bhartia, P, Hong, 2007)

7.3.2 Schiffman Phase Shifting Power Divider

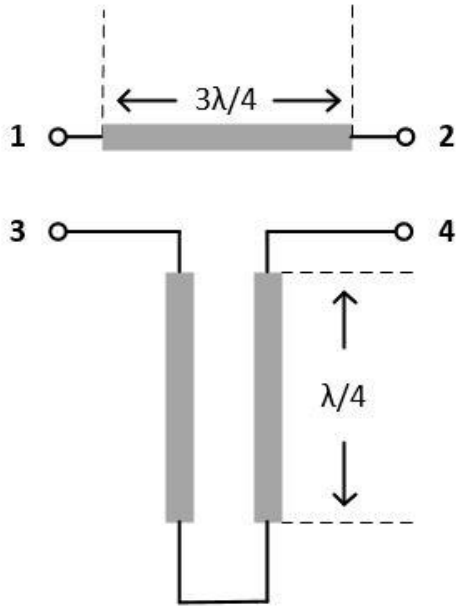

Figure 7.6: Schiffman Phase Shifter

In 1958 Bernard Schiffman derived the Schiffman phase shifter as in Figure 7.6. This phase shifter consists of two sections. The first section is a three-quarter-wavelength transmission line which has the input and through ports. The second section which generates the 90° phase shift, has two parallel quarter-wavelength transmission lines that are connected to form a c-shape and has the isolated and coupled ports. By increasing the distance between the parallel quarter-wavelengths creates a more linear 90° phase shift over frequency as in Figure 7.7**,** but this deceases the coupling factor of the phase shifter. By decreasing the distance creates a more s-shaped response over frequency, but has the advantage of increasing the coupling factor of the phase shifter.
(Morgan, 2019)

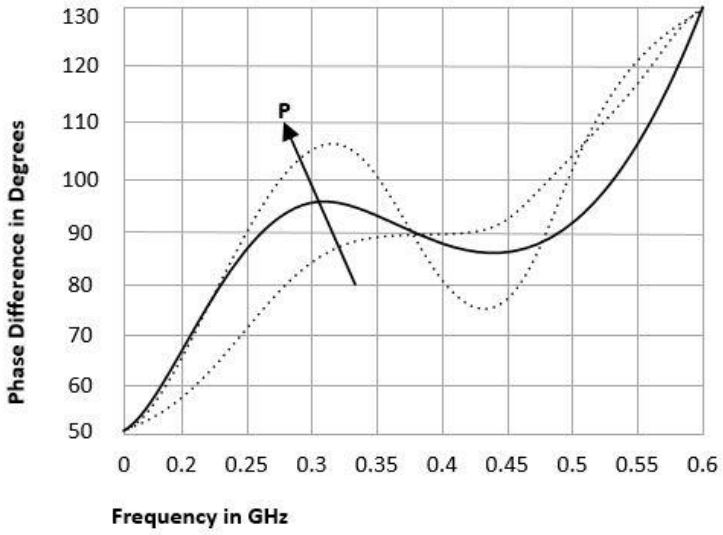

Figure 7.7: Coupling and Phase Relation

7.3.3 Lange Coupler

The Lange coupler as in Figure 7.8 is a 4-port directional coupler that has a through and a coupler port that has:

a. 3dB difference between the ports.
b. 90° difference in phase between the ports.

In 1969 by Julius Lange invented the Lange coupler to achieve an octave and higher operating bandwidth in a small package format. The coupled and input transmission lines are $\frac{\lambda_g}{4}$ wavelength away from the isolated and through ports. The number of fingers is generally an even amount. The Lange coupler is only available in MMIC format for above 1Ghz operation due to line widths and line spacing that become incredibly small and impossible to etch on a PCB.

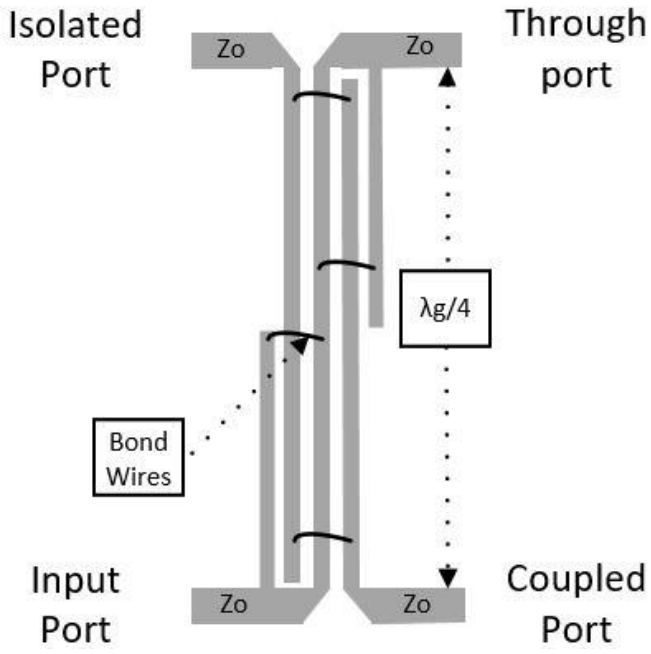

Figure 7.8: Lange Coupler

(Edwards, 2018)

7.3.4 Multi-sectional Strip-line 3dB Hybrid Coupler

Edge-coupled microstrip as in Figure 7.9 (a) can be used to form a hybrid coupler but has a disadvantage of only achieving coupling of up to 15dB as they are dispersive and lossy through quasi-TEM mode of propagation. Tighter coupling is achieved through edge-coupled stripline as in Figure 7.9 **(**b**)** because they are non-dispersive and less lossy through TEM mode of propagation. Finally, the coupling can be made even tighter to achieve the required 3dB coupling by using stripline in broadside-coupled configuration as in Figure 7.9 (c), by bringing the gaps closer and even overlapping when it is required.

The broadside-coupled stripline hybrid coupler is a very flexible component because the operating bandwidth can be easily increased by adding more quarter-wavelength sections as in Figure 7.10. A small length of transmission line joins each section. The quarter-wavelength sections are designed at the center frequency of the desired bandwidth. The even and odd mode impedances define the coupling of each quarter-wavelength section.

The broadside-coupled stripline can achieve a constant 90° phase difference between the coupled and through ports by having a symmetrical design, i.e., by having an even number of quarter-wavelength sections between physically connected ports as in Figure 7.11. When asymmetrical design is used, there are an odd number of quarter-wavelength sections between physical connected ports as in Figure 7.11. The asymmetrical configuration can't maintain a constant 90° phase difference between the through and coupled port and therefore can't be used as a 3dB Hybrid coupler.

(Mongia,R.K, Bahl, I.J, Bhartia, P, Hong, 2007)

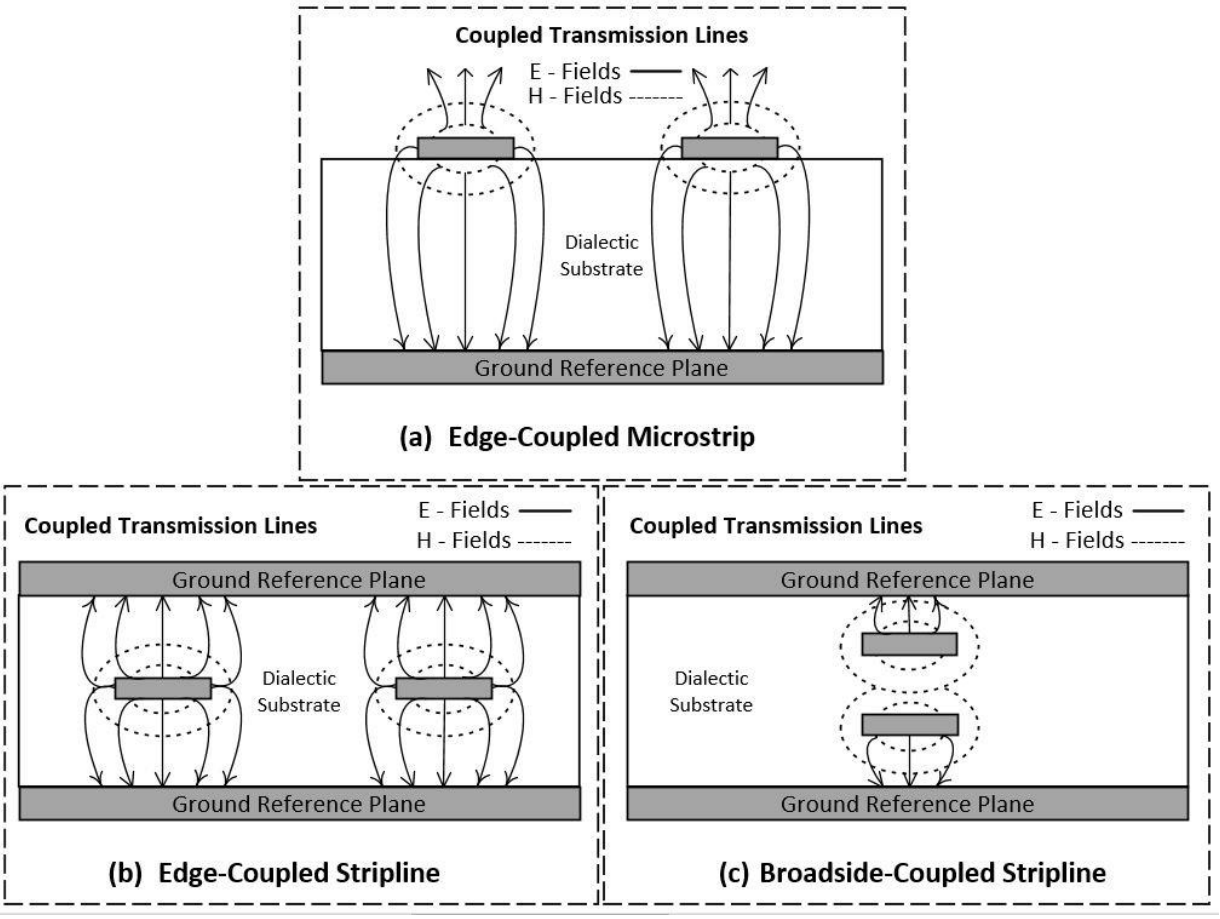

Figure 7.9: Edge-Coupled Microstrip vs Edge-Coupled Stripline vs Broadside-Coupled Stripline

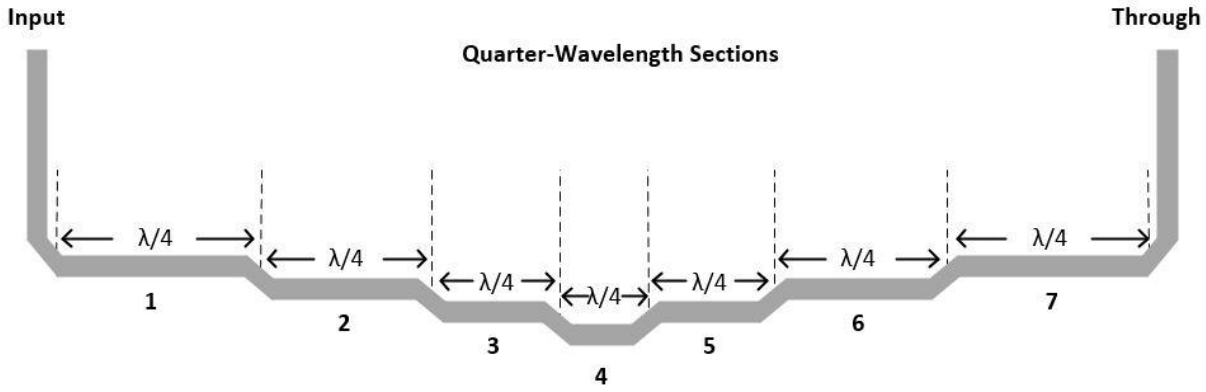

Figure 7.10: Quarter-wavelength sections

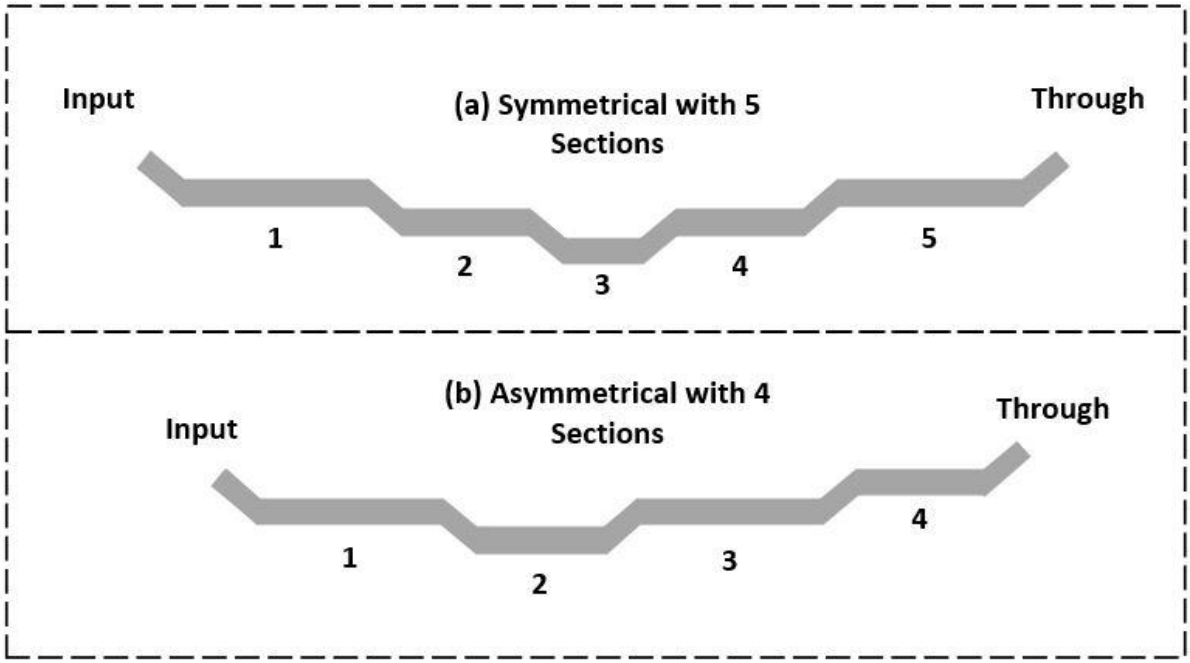

Figure 7.11: Symmetrical vs Asymmetrical with ports

7.4 Parameters of RF Coupler

7.4.1 Coupling

This is the ratio between the input (P1) and output (P3) ports of the coupler. It is usually 10dB or 10% of the input power for a 10dB directional coupler or 3dB or 50% of the input power for a 3dB quadrature Hybrid coupler and is calculated as:

$$Coupling\ (dB) = \ 10 * \log\frac{P1}{P3} \tag{7.1}$$

7.4.2 Phase Shift

This is the amount of phase shift in degrees that is formed over the operational frequency range between the through (P2) and coupling (P3) ports of the quadrature coupler.

7.4.3 Phase Balance

This is the upper and lower limit of how much different the phase can be in degrees of the actual phase shift over the operational frequency range between the through (P2) and coupling (P3) ports of the quadrature coupler.

7.4.4 Amplitude Balance

This is the upper and lower limit of how much different the amplitude can be in dB of the actual amplitude over the operational frequency range between the through (P2) and coupling (P3) ports of the quadrature coupler.

7.4.5 Main Line Insertion Loss (Directional Couplers)

This is the ratio between the input (P1) and the through (P2) ports of the coupler. It indicates the amount of power lost due to the main transmission line resistance and is calculated as:

$$Main\ Line\ Insertion\ Loss\ (dB) = \ 10 * \log\frac{P1}{P2} \tag{7.2}$$

7.4.6 Excess Insertion Loss (3dB Quadrature Coupler)

This is the ratio between the input (P1) and the through (P2) ports or the input (P1) and the coupling (P3) ports minus 3dB and is calculated as:

$$Excess\ Insertion\ Loss\ (dB) = \ 10 * \log\frac{P1}{P2} - 3dB$$
$$or\ \ 10 * \log\frac{P1}{P3} - 3dB \tag{7.3}$$

7.4.7 VSWR

This is the voltage standing wave ratio which indicates how well the impedance of the coupler is matched to the characteristic impedance of the system (Z_o). Less reflections are experienced the closer the VSWR is to the characteristic impedance This is calculated as:

$$VSWR = \frac{1+|P|}{1-|P|} \text{ and } P = \frac{Z-Z_o}{Z+Z_o} \quad (7.4)$$

7.4.8 Isolation

This is the ratio between the input (P1) and isolated (P4) ports of the coupler. It indicates the amount of power reflected from the load to the isolated port and is calculated as:

$$Isolation\ (dB) = 10 * \log\frac{P1}{P4} \quad (7.5)$$

7.4.9 Directivity

This is the ratio between the output power of the coupling (P3) and isolation (P4) ports of the coupler. It indicates how effective the coupler directs power to the load and not to the isolation (P4) port and is calculated as:

$$Directivity\ (dB) = 10 * \log\frac{P3}{P4} \quad (7.6)$$

7.4.10 CW power

This is the maximum input power the coupler can handle continuously before the coupler will behave non-linear over the operating frequency range.

(Mongia,R.K, Bahl, I.J, Bhartia, P, Hong, 2007)

7.5 Chapter Summary

The RF coupler is a passive device with 3 or 4 ports. Three ports signify that it is a directional coupler where the isolated port is matched internally to 50Ω. Four ports signify that it is either a bidirectional or a dual directional coupler. The ports 1 and 2, which is directly linked to the main line, known as the input port and the output port. The output port has a minimum loss in power to feed the next processing stage. Port 3 and port 4 are called isolation and coupled ports respectively. The coupled port, port 4, is the sampled power output, which is usually 3-10dB less than the main line, depending on the application. The isolation port, port 3, allows any reflections to be absorbed be the 50Ω load that it is attached too.

When the RF coupler is a directional coupler, it is used to sample the high power only in one direction from the main line to provide a reduced power for sensitive equipment to analyze through the coupled port. When the RF coupler is a bidirectional coupler, it is just like the directional coupler, where the only difference is where power can be sampled in both directions from the main line. When the RF coupler is a dual directional coupler, the forward and reflective power can be measured at the same time, which directional and bidirectional couplers can't do.

When the application is not just to sample the main line power, but also to shift the phase by 90°, a quadrature coupler is used. The RF quadrature coupler, also known as the RF hybrid coupler, has four ports where the only difference is that the coupled port is shift by 90° with reference to the through port.

There are many passive devices that can shift the coupled port by 90°. The branchline coupler accomplishes this task perfectly but only operates with a narrow band. The band of operation can be increased by cascading the branches as in (Rahim *et al.*, 2017), but consequently increases the physical size of the circuit. The Schiffman coupler, another type of hybrid coupler suffers from the same bandwidth issue. The bandwidth can be increased as in (Brown and Starski, 1999), but has the disadvantage where the phase is not stable. The Schiffman coupler can be loaded with lumped elements as in (Liu *et al.*, 2016) to increase the operational bandwidth, but this increases the complexity of the circuit. The Lange coupler is another device that creates the 90° phase shift and has a higher operational bandwidth of an octave and higher. The bandwidth can be increased by adding reflective type loads to the output and coupled ports but again adds complexity. The Lange coupler also has a disadvantage, because it uses bond wires to make connections between the conducting lines, it can only be used in applications where low power is used. The multi-sectional stripline used in broadside configuration is very flexible and non-complex device. The bandwidth can easily be increased by adding a quarter-wavelength piece of conductor to which frequency it corresponds to as in (Kim *et al.*, 2017). It can be used for high power applications, not expensive and is not physically a big circuit. It must be designed symmetrically and not asymmetrically. When designed asymmetrically, it can't provide a constant 90° phase shift over the frequency of operation as in (Mongia,R.K, Bahl, I.J, Bhartia, P, Hong, 2007).

In this project, the RF hybrid coupler forms part of the image-reject mixer. It is the component after the I/R mixer as in Figure 2.8 to:

- Create the additional 90° phase shift.
- Combine the I and Q signals which will provide the wanted signal to one port and the unwanted signal to the other port.

The multi-sectional stripline in the broadside asymmetrical configuration will be considered as the RF hybrid coupler.

Chapter 8

Simulations

8.1 Introduction

The proposed design is simulated in the Cadence® Applied Wave Research (AWR®) Visual System Simulator™ (VSS) V16 software suite. Engineers use this software to design complex communications systems by theorizing the system architecture accurately for the envisioned application and therefore develop suitable specifications for each component of the theorized system architecture. The overall system performance can also be visually examined through graphs.

As in Figure 8.1, the proposed design, the down converter, consists of 4 major sections:

- The Low noise amplifier
- Image reject mixer (I/Q mixer combined with IF 90º Hybrid Coupler)
- The local oscillator
- The RF switch

There are no filters used as in the standard front-end receiver architecture as discussed in chapter 2. Therefore, the purpose of this chapter is to demonstrate that the proposed design in (van Niekerk, Kahn and Balyan, 2020), through simulations is possible. Before this can be done, each of the 4 major sections needs to be simulated on their own to derive suitable specifications. After this is accomplished, the 4 major sections are simulated together, and the overall system performance is demonstrated.

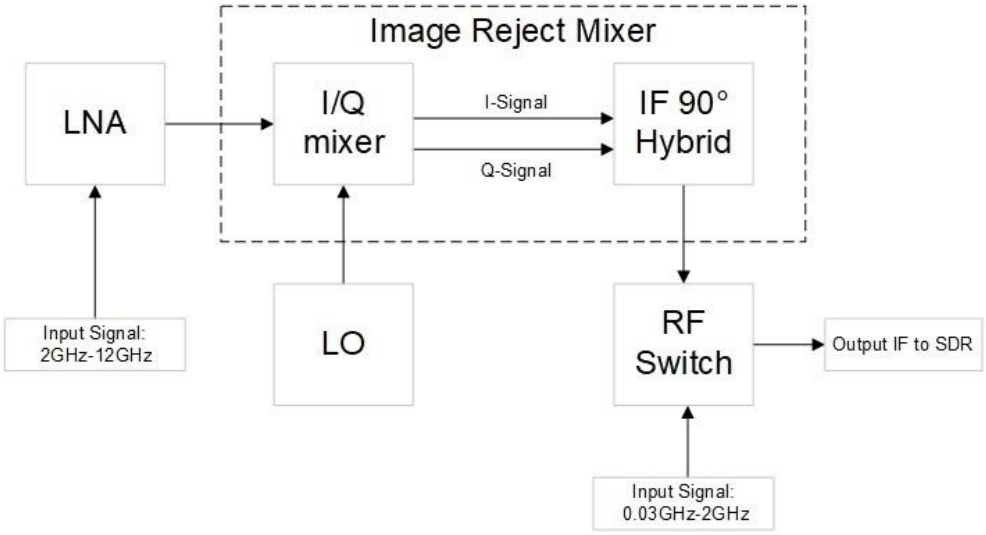

Figure 8.1: Down Converter Components

8.2 LNA

8.2.1 Core Requirements

The core requirements and parameters demonstrated in this section:

- The LNA operates over a range of 2GHz to 12GHz. Maximum available gain and noise figure are demonstrated in this section, but isolation and return loss are not demonstrated. Isolation and return loss are selected to be between 20dB and 15dB. This ensures that only 1% to 3% of power is reflected from the load or source to the DUT. This equates to a VSWR of between 1.222 and 1.433.
- The OP1dB, OIP3 and OIP2 are demonstrated by the simulator to see how it influences IMD products, where the acceptable parameter level is chosen for the LNA to function as a suitable component.
- The MMIC technology component is selected to allow for internal input and output matching to 50Ω on the same integrated circuit. The LNA needs to be unconditionally stable. If not, the load and source need to be identified when the LNA is unstable. These requirements are not demonstrated by the simulator.

8.2.2 Base Model Development and Simulation

The behavior model for the LNA amplifier in VSS is used as in Figure 8.2 and parameter values for OP1dB, OIP3 and OIP2 are all set to 10dBm to get a base LNA spectrum plot. Generally, gain for adequate amplification of small signals are specified at 15dB with NF specified at 3dB and these specifications will also be used for the LNA to the base model circuit as in Figure 8.3. The input power is at -14dBm to get the fundamental at 0dBm for reference.

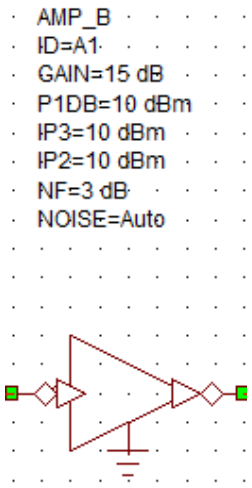

Figure 8.2: Nonlinear Behavior Model - AMP B

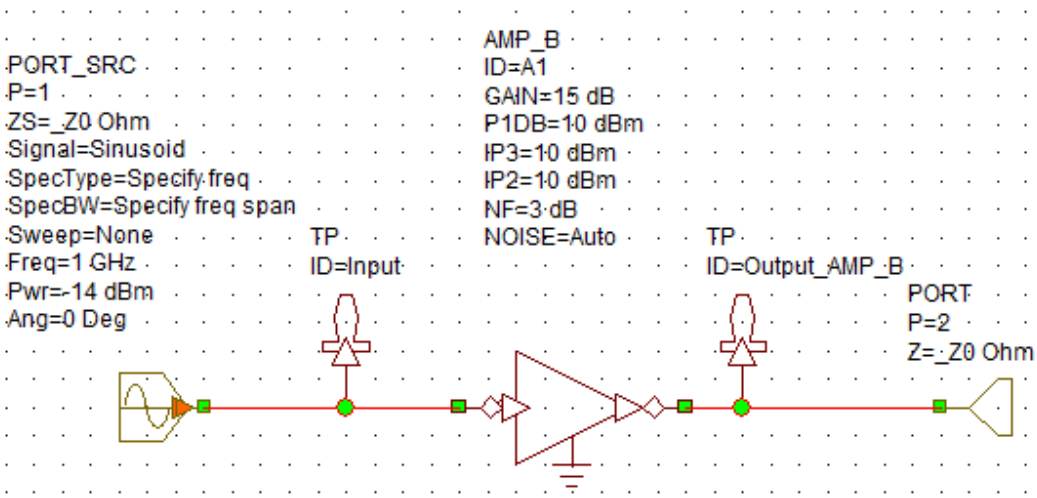

Figure 8.3: Base Model Circuit

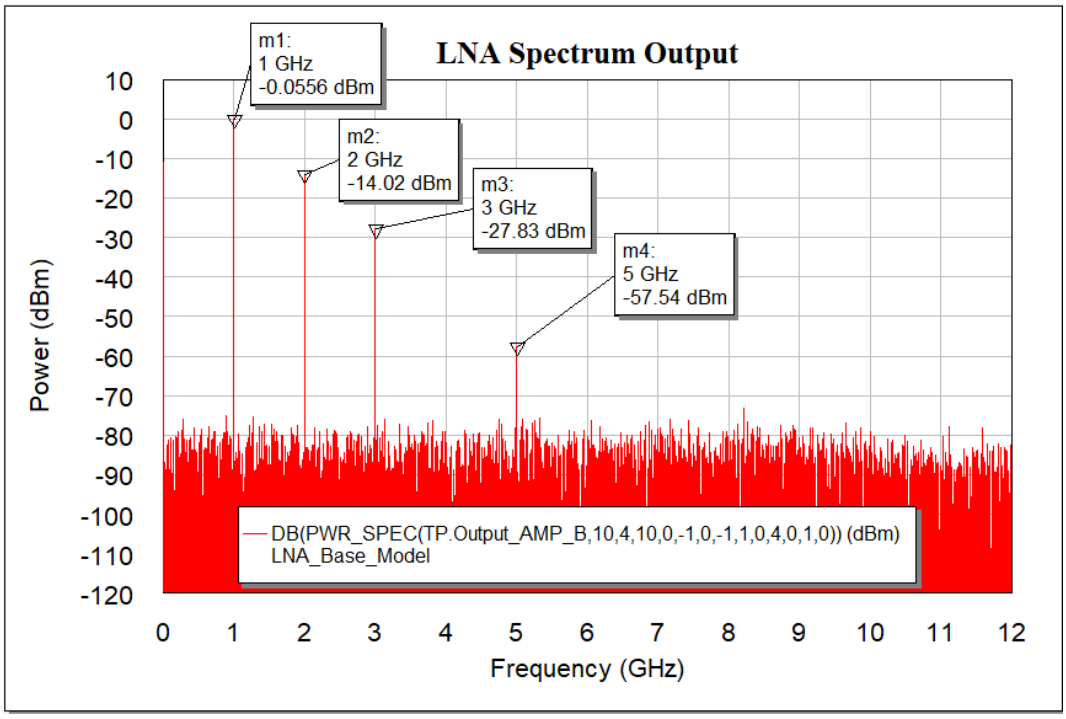

Figure 8.4: Output Base Model

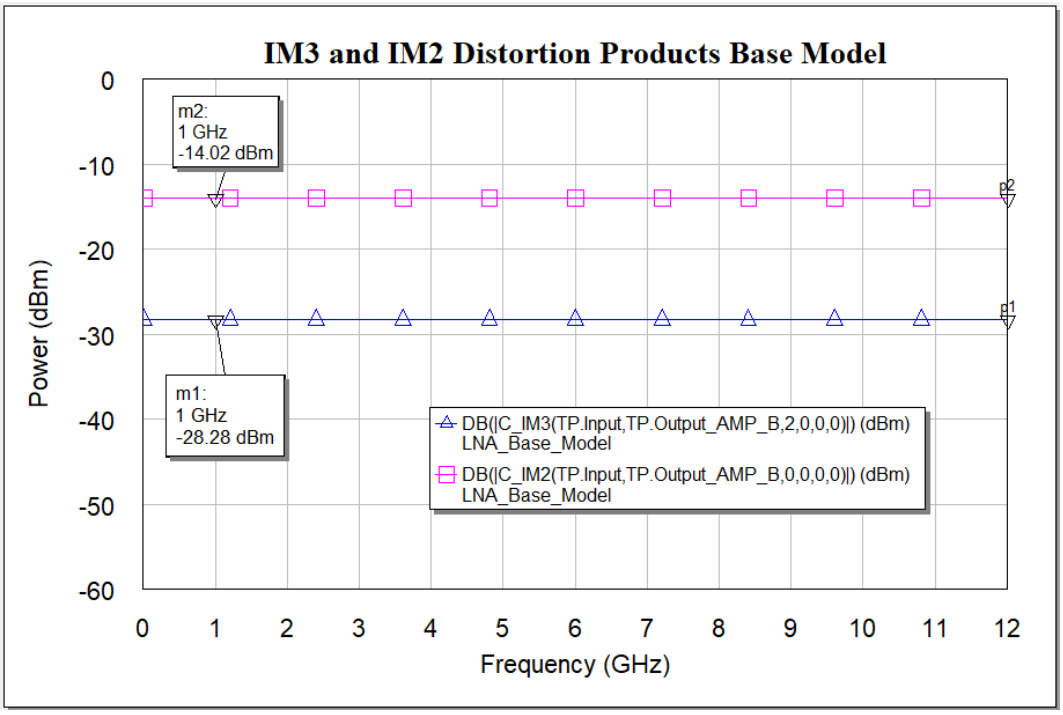

Figure 8.5: IMD Base Model

Figure 8.4 demonstrates that the base model circuit produces harmonics of the fundamental up to the 5th order, each decreasing by 10dB from the fundamental. Figure 8.5 demonstrates that the IM3 and IM2 distortion products are at -29dBm and -14dBm in turn simulated with the base model circuit.

By using 2x frequency sine wave tones at -10.8dBm as in Figure 8.6, one at 1000MHz and the other at 1010MHz it is demonstrated as in Figure 8.7 that the IM3 and IM2 distortion products have increased to -23.6dBm and -9.6dBm in turn simulated with the two-tone base model circuit. The individual IMD products can be seen in Table 8.1 and Table 8.2 from 0GHz to 3.5GHz.

8.2.3 Optimization of Base Model and Simulation

The next step is to reduce the large IM3 and IM2 distortion products as in Figure 8.8. In AWR the optimization goal function optimizes the OP1db, OIP3 and OIP2 parameters of the LNA so that the IM3 and IM2 distortion products are at acceptable levels. The acceptable level that the IMD is optimized for is chosen as -50dBm. Limits are set for OP1dB between 0dBm and 20dBm, OIP3 set between 0 and 30dBm and OIP2 set between 0 and 40dBm, to achieve the -50dBm IMD product level. After the optimization, the results as in Figure 8.10 demonstrates that the IM3 and IM2 distortion products were reduced to -59dBm and -40dBm in turn, with new parameters for OP1dB now at 17dBm, OIP3 now at 30dBm and OIP2 now at 40dBm.

These new parameters can be seen in Figure 8.9, where the individual IM3 and IM2 distortion product levels can be seen in Figure 8.11. Table 8.3 and Table 8.4 shows the improvement of the optimized base model over the base model.

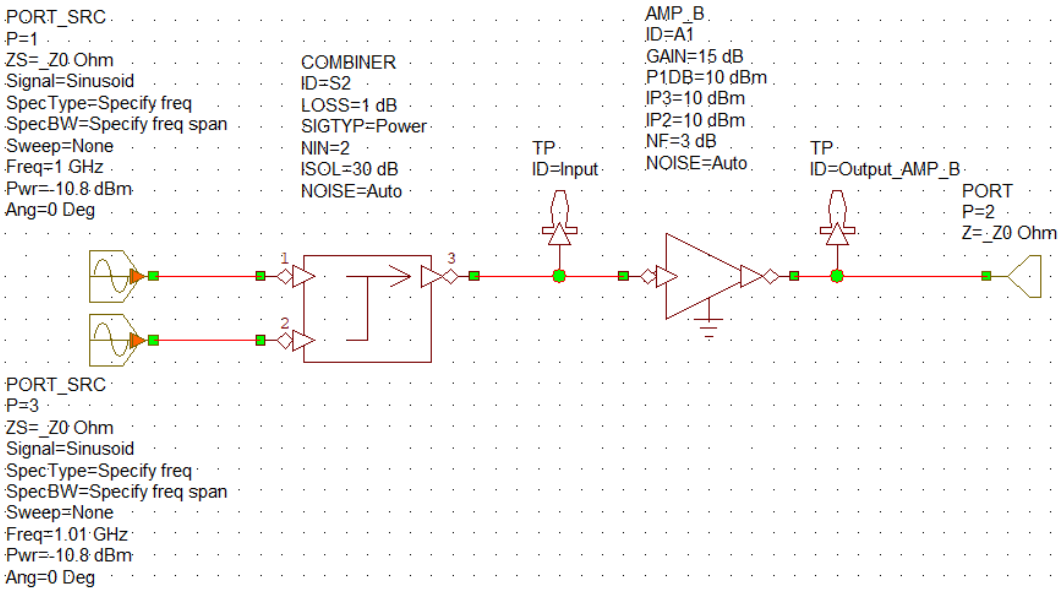

Figure 8.6: LNA Configured to Simulate IMD Products

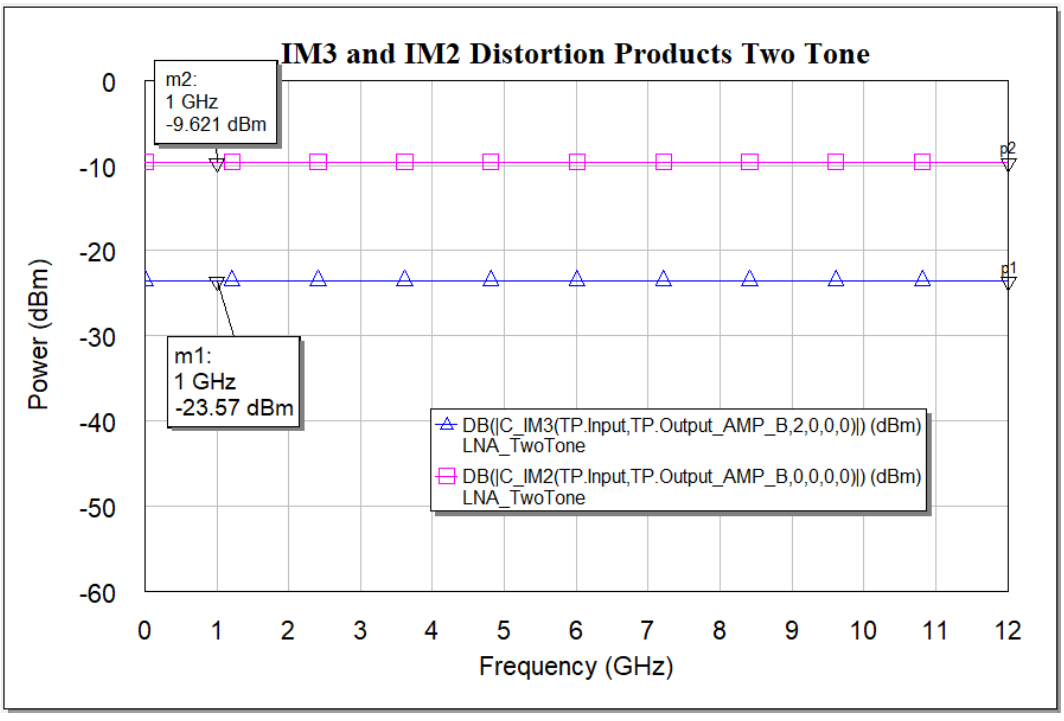

Figure 8.7: Base Model Circuit with Two Tones

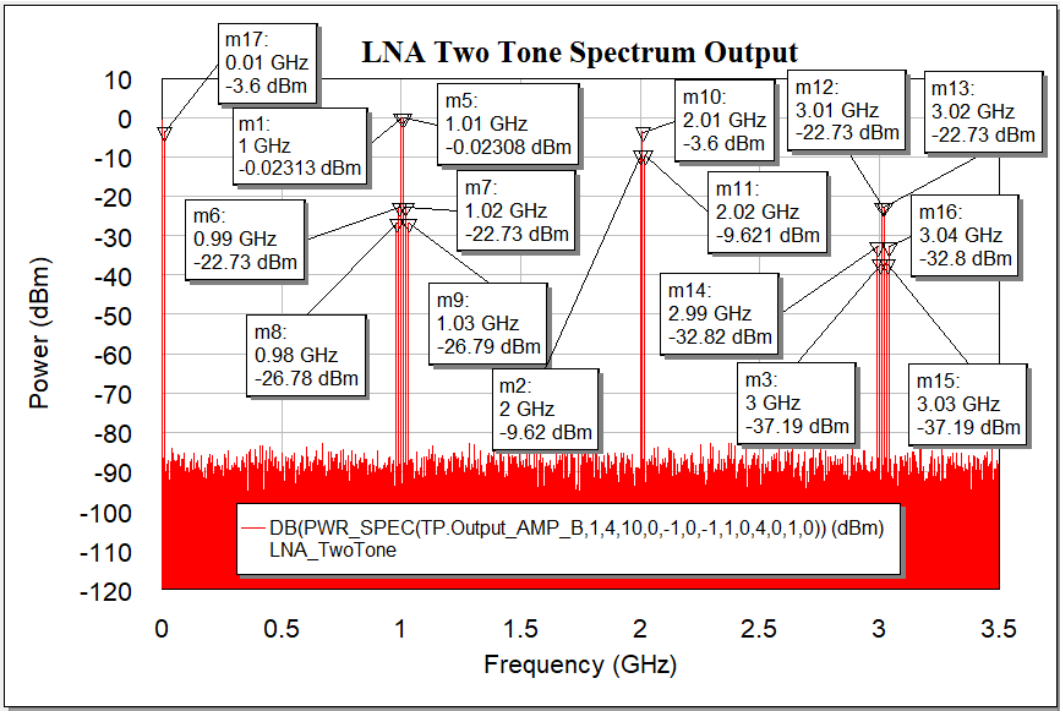

Figure 8.8: IM3 and IM2 Distortion Products Two Tone Base Model

Table 8.1: IM3 Distortion Products

IM3 Distortion Products						
Frequency	**In-Band**		**Out-Band**			
	$2f_1-f_2$	**$2f_2-f_1$**	**$2f_1+f_2$**	**$2f_2+f_1$**	**$3f_1$**	**$3f_2$**
	0.99GHz	1.02GHz	3.02GHz	3.01GHz	3GHz	3.03GHz
Power Level	-23dBc	-23dBc	-28dBc	-28dBc	-37dBc	-37dBc

Table 8.2: IM2 Distortion Products

IM2 Distortion Products				
Frequency	**Out-Band**			
	f_2-f_1	**f_2+f_1**	**$2f_1$**	**$2f_2$**
	0.01GHz	2.01GHz	2GHz	2.02GHz
Power Level	-4dBc	-4dBc	-10dBc	-10dBc

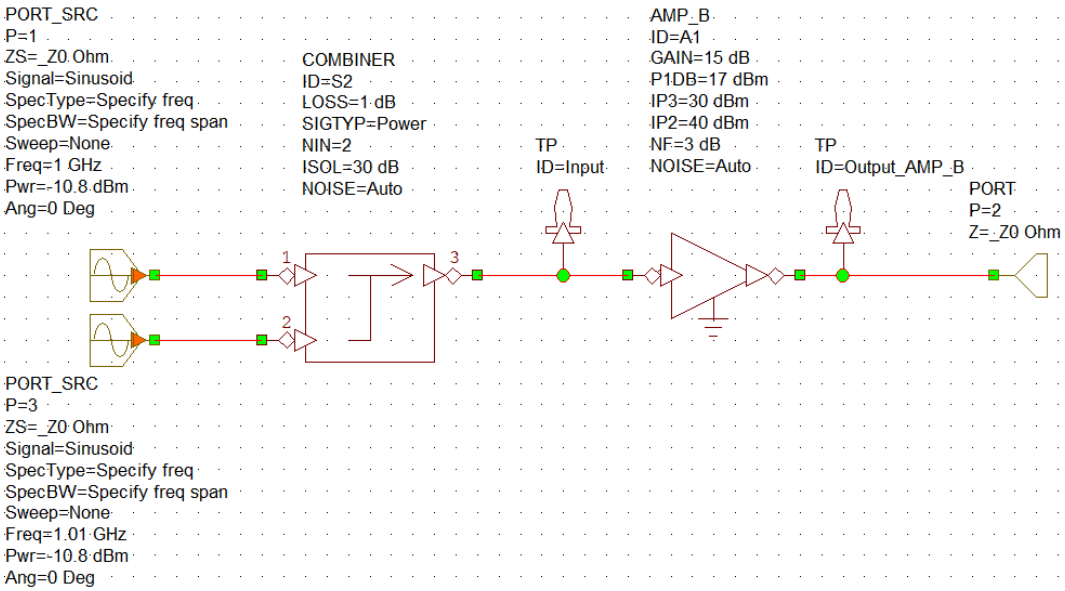

Figure 8.9: Optimized Model Circuit

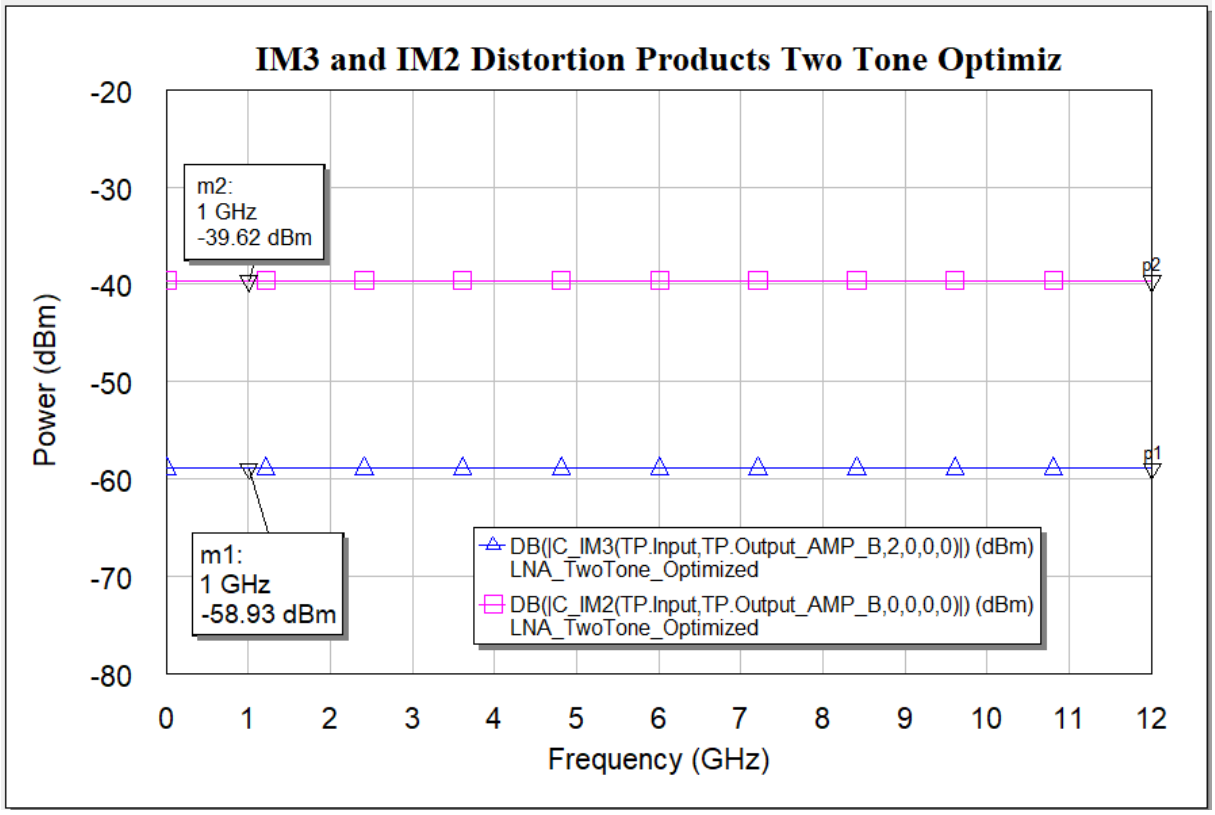

Figure 8.10: Optimized Base Model with Two Tones

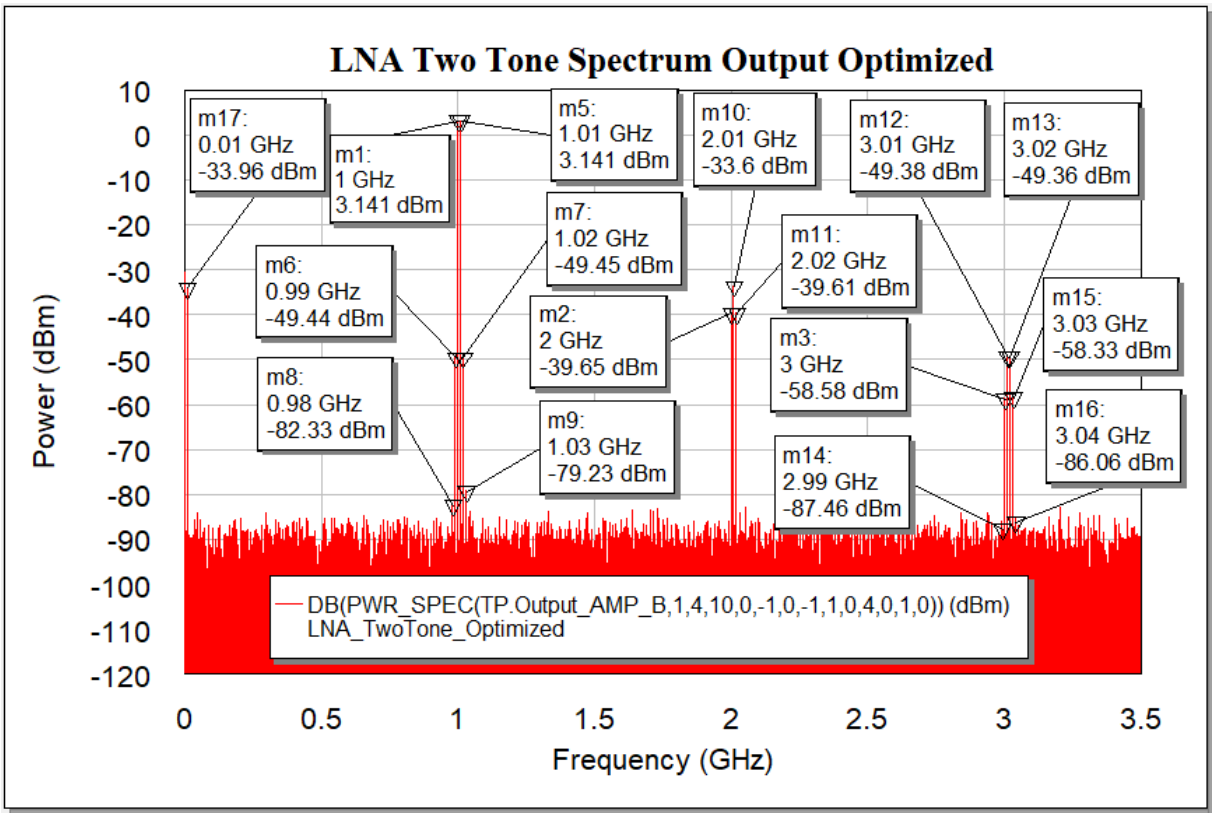

Figure 8.11: IM3 and IM2 Distortion Products Two Tone Optimized Model

Table 8.3: Optimized IM3 Distortion Products

Optimized IM3 Distortion Products						
Frequency	**In-Band**		**Out-Band**			
	$2f_1-f_2$	**$2f_2-f_1$**	**$2f_1+f_2$**	**$2f_2+f_1$**	**$3f_1$**	**$3f_2$**
	0.99GHz	1.02GHz	3.02GHz	3.01GHz	3GHz	3.03GHz
Power Level	-53dBc	-53dBc	-53dBc	-53dBc	-62dBc	-62dBc
Increase by	25dB	25dB	25dB	25dB	25dB	25dB

Table 8.4: Optimized IM2 Distortion Products

Optimized IM2 Distortion Products				
Frequency	Out-Band			
	f_2-f_1	**f_2+f_1**	**$2f_1$**	**$2f_2$**
	0.01GHz	2.01GHz	2GHz	2.02GHz
Power Level	-43dBc	-43dBc	-42dBc	-42dBc
Increase by	39dB	39dB	32dB	32dB

8.2.4 Final LNA Specifications

Table 8.5 displays the acceptable LNA specifications needed for the down converter to function.

Table 8.5: Final Specifications of the LNA

	Frequency Range	OP1dB	OIP3	OIP2	NF	Gain	Input/Output Return Loss
Parameter	2-12GHz	17dBm	30dBm	40dBm	3dB	15dB	15dB ≤ RL ≤ 20dB

8.3 RF I/Q Mixer and Image Reject Mixer

8.3.1 Core Requirements of IQ Mixer and Image Reject Mixer

The core requirements and parameters to be demonstrated in this section:

- The RF I/Q mixer and image reject mixer operates with an input range of 2GHz to 12GHz and has an output of 100MHz as an IF, which is demonstrated by the simulator.
- The return loss for RF, LO and IF ports are not demonstrated by the simulator but is selected between 10dB and 5dB. This ensures that only 10% to 32% of power is reflected from the load or to DUT. This is not critical as the RF I/Q mixer has low power input and output.
- The IP1dB, IIP3, conversion loss, LO-IF isolation, RF-IF isolation, NF, amplitude unbalance and phase unbalance are demonstrated by the simulator to see how it influences IMD products and the image reject ratio, where the acceptable parameter level are chosen for the RF I/Q mixer and image reject mixer to function as a suitable component.
- The MMIC technology component in a double balanced configuration is selected to allow for internal input and output matching to 50Ω on the same integrated circuit. This is not demonstrated.

8.3.2 Base Model Development and Simulation

The behavior model for the RF mixer in VSS is used as in Figure 8.12 and parameter values for IP1dB, IIP3 and NF are all set to 10dBm. RF-IF and LO-IF isolation are set to -10dB. Conversion loss is set to 10dB. The difference mode is used because it is a down-conversion process, albeit it also produces the sum process which is an IF of 2.1GHz. Therefore, it makes no difference if the sum/difference mode is selected. LO multiplication is set to 1, which produces the IF of 100MHz. IIP2 and LO-RF are not used to configure the RF mixer base model as it doesn't have any influence on the output in the simulation. As in Figure 8.13, the RF input is set to 1GHz at -10dBm and LO is set to 1.1GHz at 10dBm to produce an IF of -20dBm at 100MHz. Table 8.6, Table 8.7, Table 8.8, Table 8.9, Table 8.10 and

Table 8.11 shows the levels of IMD products up to the 5th order of the RF mixer base model circuit. The are no products above 7GHz and therefore the spectrum output is limited to 7GHz as in Figure 8.14 and for the rest of this section.

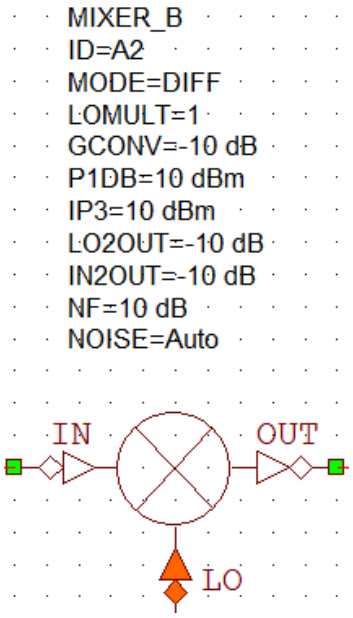

Figure 8.12: RF Mixer Base Model

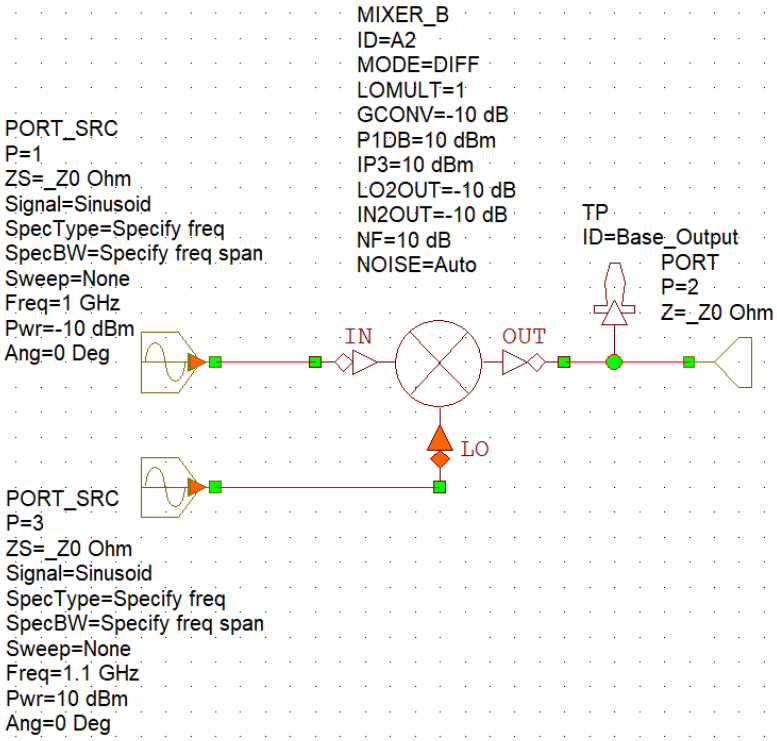

Figure 8.13: RF Mixer Base Model Circuit

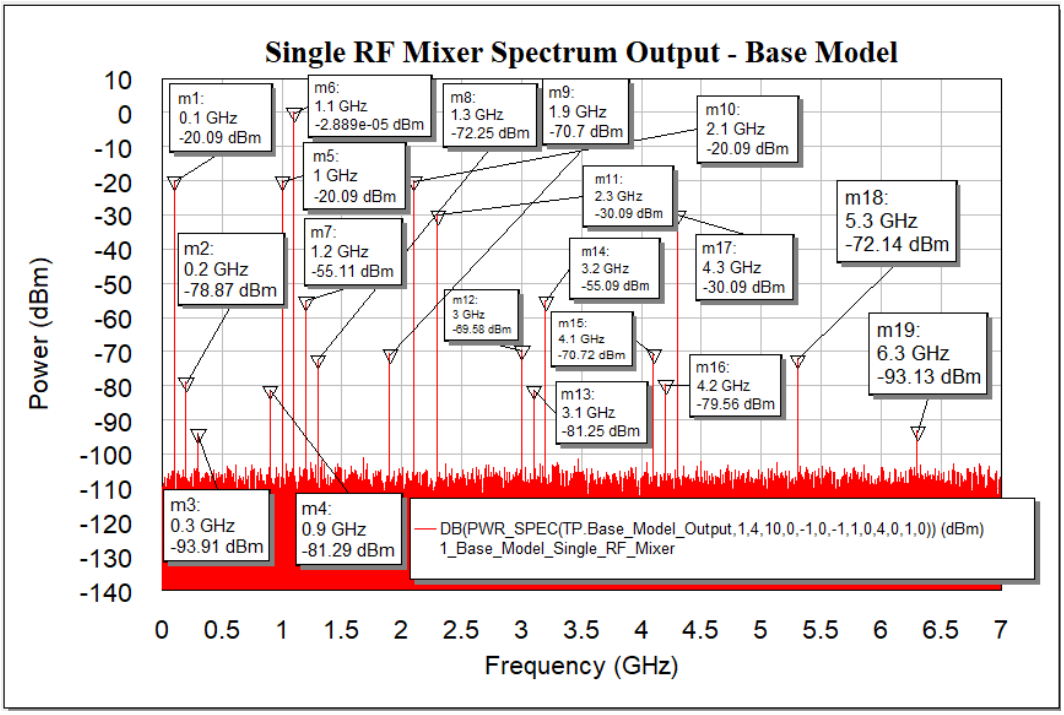

Figure 8.14: Single RF Mixer Output – Base Model

Table 8.6: RF Mixer - RF, LO and 3x IF Product Base vs Optimized

	3*IF	RF	LO
Frequency	**$3f_2$-$3f_1$**	**f_1**	**f_2**
	0.3GHz	1GHz	1.1GHz
Power Level	-94dBm	-20dBm	0dBm
Optimized	-78dBm	-40dBm	-20dBm

Table 8.7: RF Mixer - IM2 Distortion Products Base vs Optimized

IM2 Distortion Products		
Frequency	**f_1+f_2(IF Sum)**	**f_2-f_1(IF Diff)**
	2.1GHz	0.1GHz
Power Level	-20dBm	-20dBm
Optimized	-20dBm	-20dBm

Table 8.8: RF Mixer - IM3 Distortion Products Base vs Optimized

IM3 Distortion Products					
Frequency	**$2f_1$-f_2**	**$2f_2$-f_1**	**$2f_1$+f_2**	**$2f_2$+f_1**	**$3f_1$**
	0.9GHz	1.2GHz	3.1GHz	3.2GHz	3GHz
Power Level	-81dBm	-55dBm	-82dBm	-55dBm	70dBm
Optimized	-81dBm	-55dBm	-81dBm	-55dBm	-110dBm

Table 8.9: RF Mixer IM4 Distortion Products_1

IM4 Distortion Products		
Frequency	**$2f_2$+$2f_1$**	**$2f_2$-$2f_1$(2*IF)**
	4.2GHz	0.2GHz
Power Level	-79dBm	-79dBm
Optimized	-79dBm	-79dBm

Table 8.10: RF Mixer - IM4 Distortion Products_2 Base vs Optimized

IM4 Distortion Products				
Frequency	**$3f_2$-f_1**	**$3f_1$-f_2**	**$3f_2$+f_1**	**$3f_1$+f_2**
	2.3GHz	1.9GHz	4.3GHz	4.1GHz
Power Level	-30dBm	-70dBm	-30dBm	-71dBm
Optimized	-30dBm	-83dBm	-30dBm	-110dBm

Table 8.11: RF Mixer IM5 and IM6 Distortion Products Base vs Optimized

IM5 and IM6 Distortion Products			
Frequency	**$3f_2+2f_1$**	**$3f_2-2f_1$**	**$3f_2+3f_1$**
	5.3GHz	1.3GHz	6.3GHz
Power Level	-72dBm	-72dBm	-95dBm
Optimized	-72dBm	-72dBm	-79dBm

8.3.3 Optimization of Single RF Mixer Base Model and Simulation

The next step is to reduce the large IMD products as in Figure 8.14. The optimization goal function in AWR to optimizes the IP1dB, IIP3, RF-IF and LO-IF parameters of the RF mixer so that the IMD products are at acceptable levels. The acceptable level that the IMD is optimized for is chosen as -80dBm. Limits are set for IP1dB between 0dBm and 10dBm, IIP3 set between 0 and 20dBm and isolation set between 0 and 30dB, to achieve the -80dBm IMD product level from 0GHz to 7GHz as no other IMD products occur after 7GHz. After the optimization goal has been run, the results as in Figure 8.16 demonstrates that the IM2 distortion products did not change as the IP2 parameter wasn't optimized. One IM3 distortion product did improve, two IM4 distortion products did improve, and no IM5 distortion products did improve. The optimized RF base model circuit can be seen in Figure 8.15.

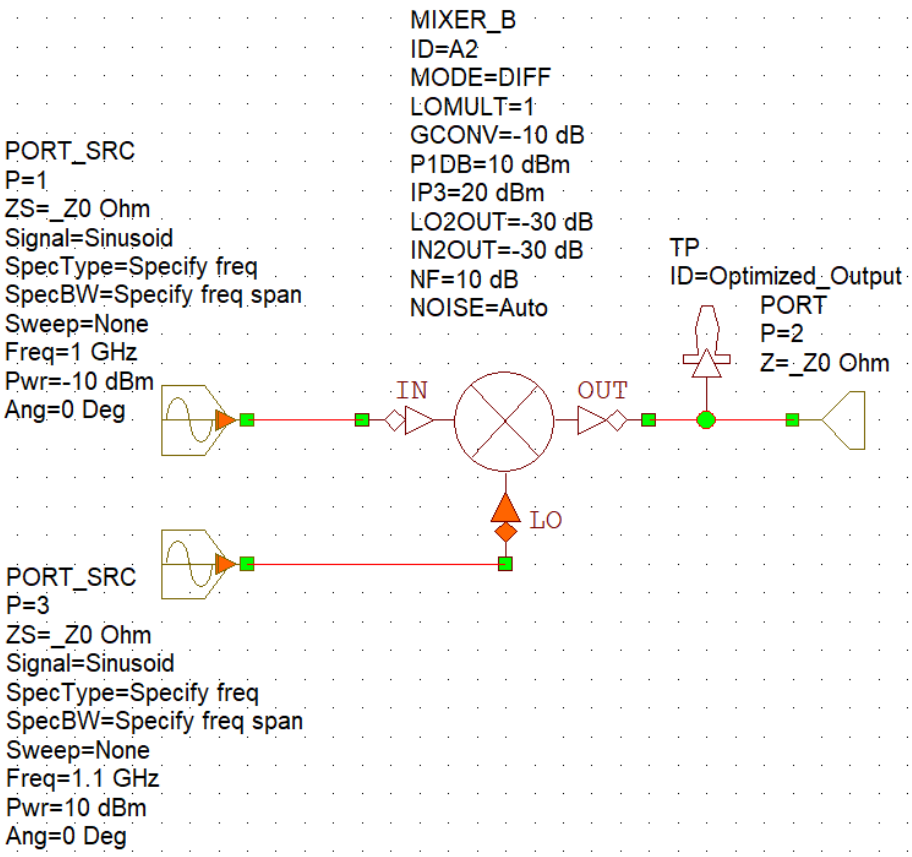

Figure 8.15: Optimized base Model Circuit

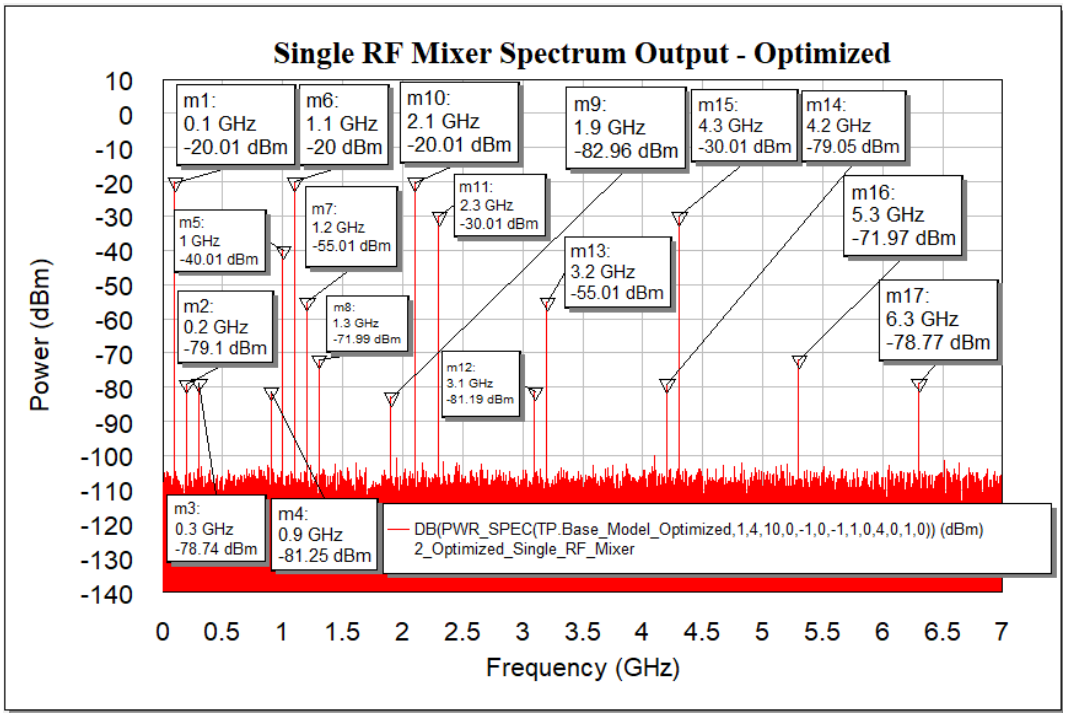

Figure 8.16: Optimized Output Spectrum

8.3.4 RF I/Q Mixer Base Model and Simulation

The RF IQ mixer as in Figure 8.17 uses the same values for the RF quadrature coupler as in section 8.6 to produce the quadrature of the LO. The RF mixer is also doubled with optimized values from section 8.3.3 to produce the quadrature of the LO, RF, IF and IMD products. The LO is set to 1.1GHz and the input RF is set to 1GHz to produce the 100MHz at the output of the mixers. The RF splitter has un unavoidable 3dB loss as part of its nature and a 0.5dB is added to reasonably represent the RF splitter, which is now at 3.5dB. RF input is set to -10dBm and LO is set to 10dBm. The RF quadrature splitter that forms part of the IQ mixer also have an unavoidable 3dB loss as part of its nature and a 0.5dB is added to reasonably represent the RF quadrature splitter.

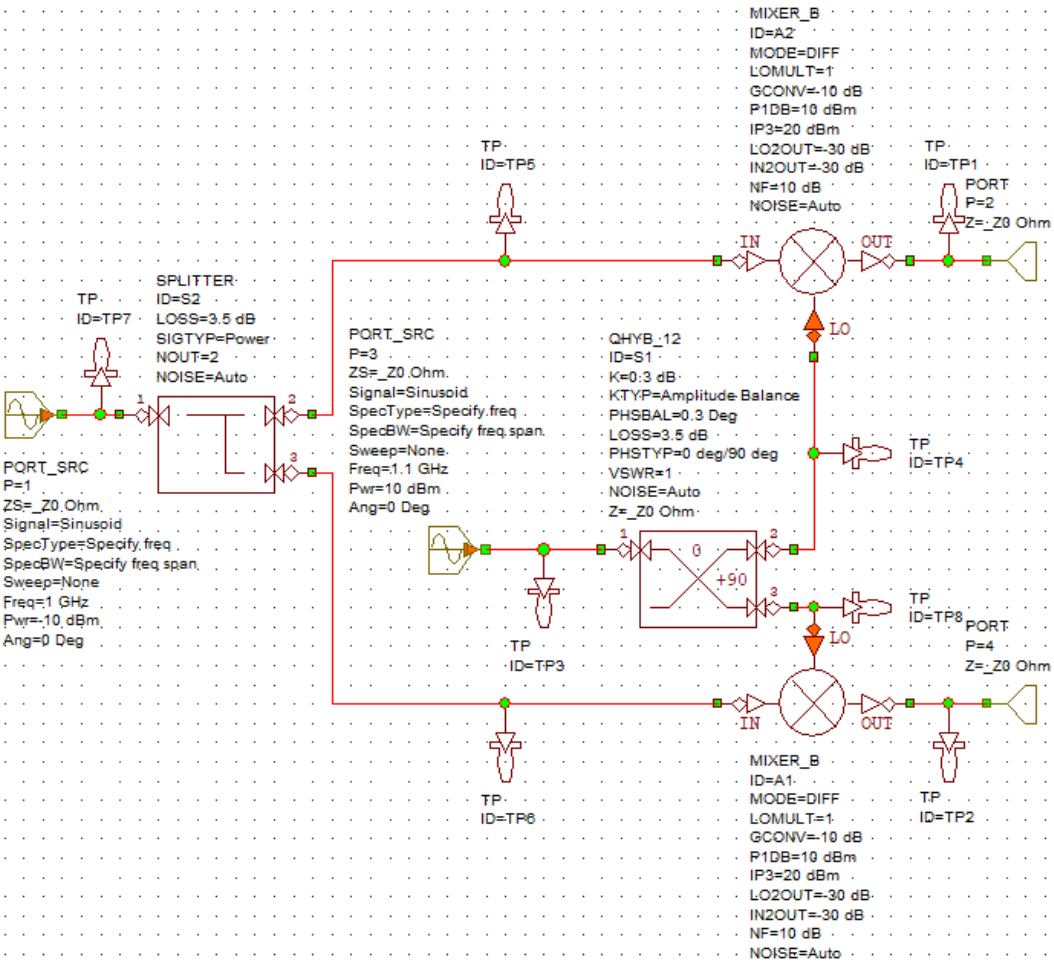

Figure 8.17: IQ Mixer Base Circuit

Figure 8.18 demonstrates a reduction of at least 3.5dB to the RF IQ mixer output which can be seen when it is taken with reference to the optimized RF mixer output (dotted light blue vs solid red). This is due to the inclusion of the reasonable attenuation of the RF input by the splitter and LO by the coupler. Except for output signals at 0.3GHz and 6.3GHz where the output wasn't affected. This could be due to the simulator not taking those signals into consideration. Also, there is a 4.1GHz signal that is produced. Figure 8.19 demonstrates the output of two mixers are indeed in quadrature with one another, and therefore are IQ signals.

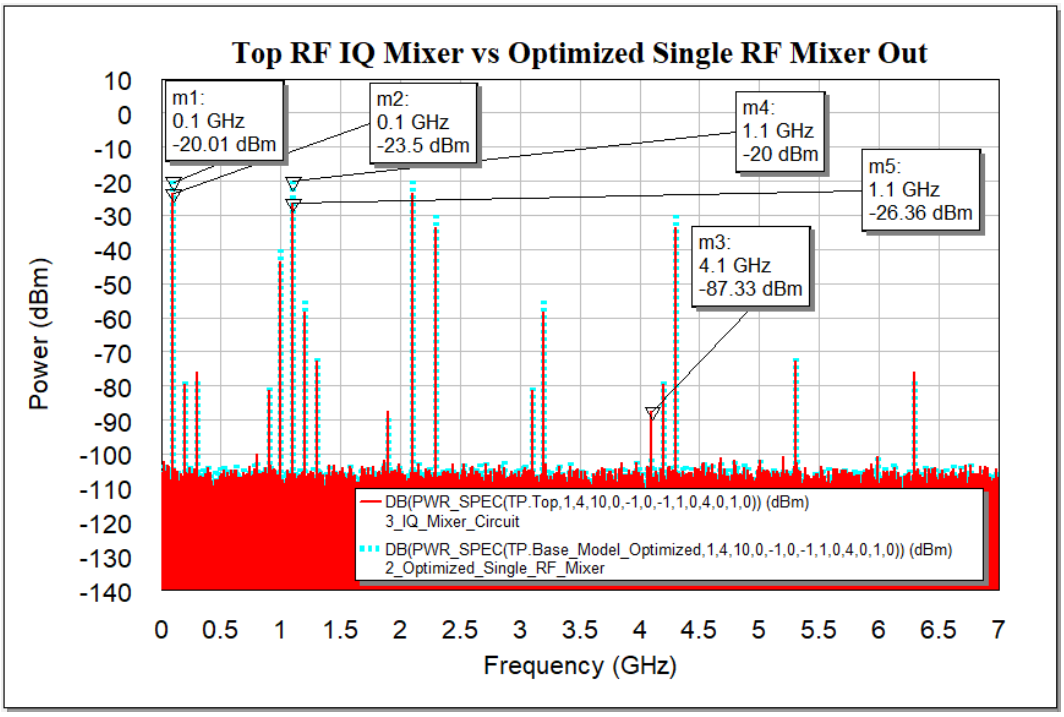

Figure 8.18: Top RF IQ Mixer vs Optimized Single RF Mixer Output Spectrum

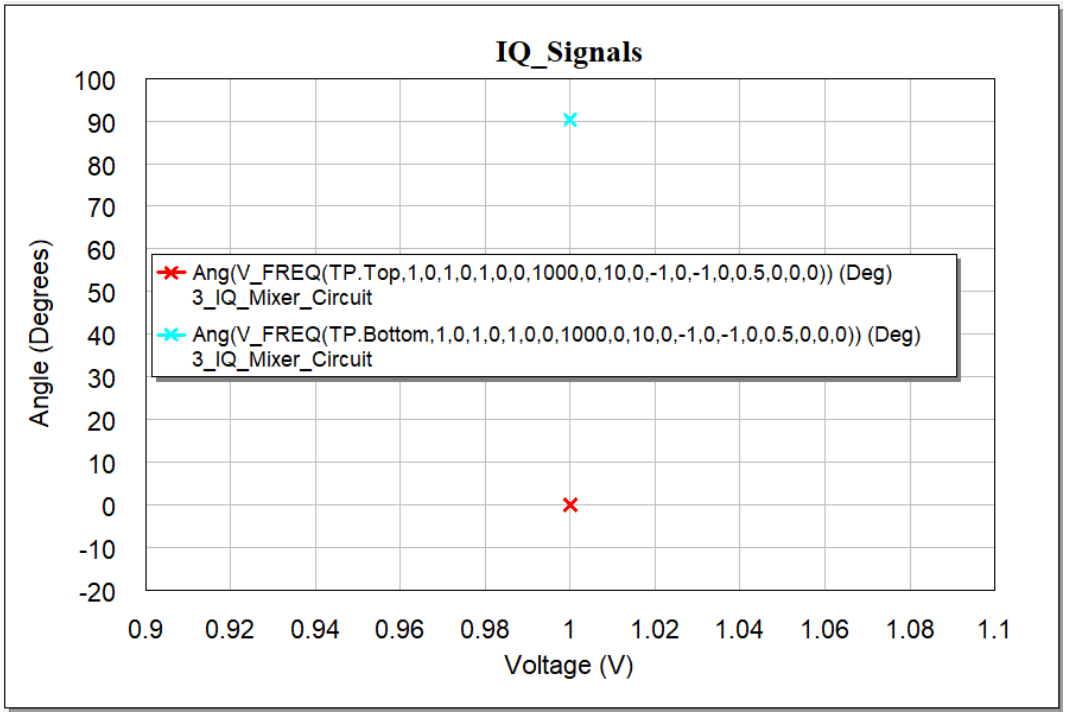

Figure 8.19: IQ Signals

8.3.5 Final IQ Mixer Specifications

Table 8.12 displays the acceptable RF IQ Mixer specifications needed for the down converter to function with a LO drive level of 0dBm.

Table 8.12: Final RF IQ Mixer Specifications

	Frequency Range	IP1dB	IIP3	RF-IF Isolation	LO-IF Isolation	NF	Conversion Loss
Parameter	2GHz - 12GHz	10dBm	20dBm	-30dB	-30dB	10dB	13.5dB

8.3.6 RF Image Reject Mixer Base Model and Simulation

As in Figure 8.20, with the addition of the RF quadrature coupler, creates an additional +90 degrees to have the unwanted sideband/image signal suppressed. Figure 8.21 demonstrates that when the IQ mixer LO output is 90 degrees advanced and together with the phase shift of +90 from the additional RF quadrature coupler, the wanted sideband 100MHz IF output power doubles from -23.5dBm to -20.5dBm. But has a final output of -24dBm because of the RF quadrature coupler loss of 3.5dB.

Figure 8.22 demonstrates that the unwanted sideband/image signal IF of 100MHz reduces by 35dB to a level of -59dBm. This occurs when the IQ mixer LO is set to a delay of 90 degrees with the addition of the +90 degrees phase shift of the RF quadrature coupler.

The operation of the RF image reject mixer configured where the IQ mixer LO set to -90 degrees and the RF quadrature coupler set to +90 degrees will allow the output IF to double. This configuration is used and can be conjectured to suppress the unwanted sideband/image signal by 35dB and theoretically be shorted to the 50Ω load inside a 3 port RF quadrature coupler of Figure 8.20.

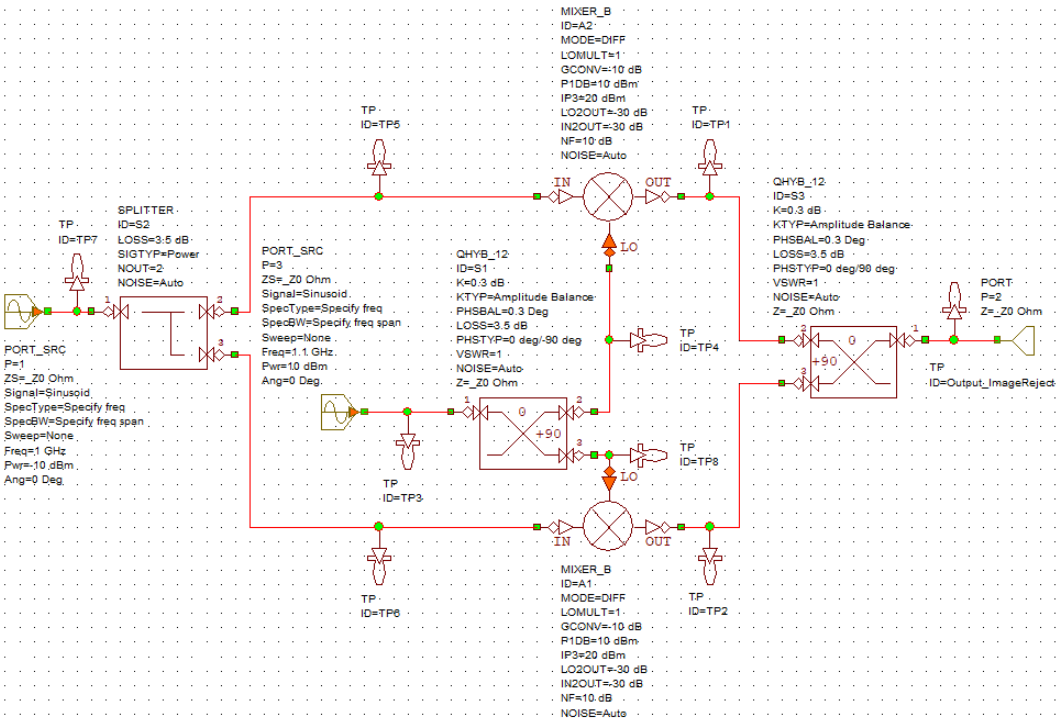

Figure 8.20: Image Reject Mixer Circuit

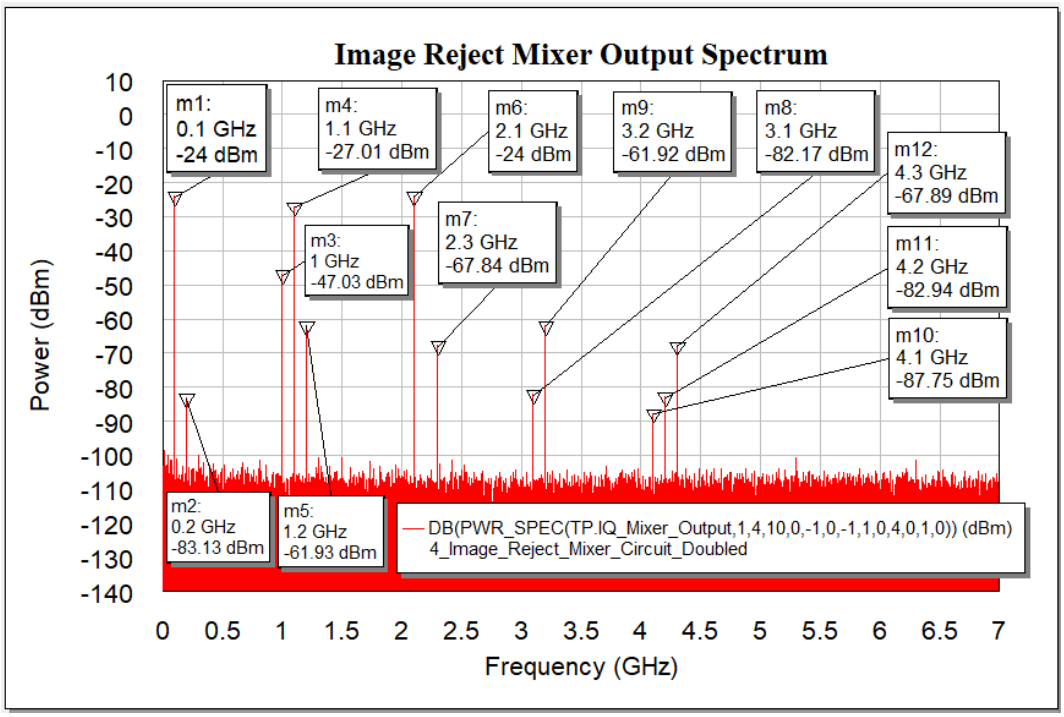

Figure 8.21: Image Reject Mixer Output Spectrum Doubled

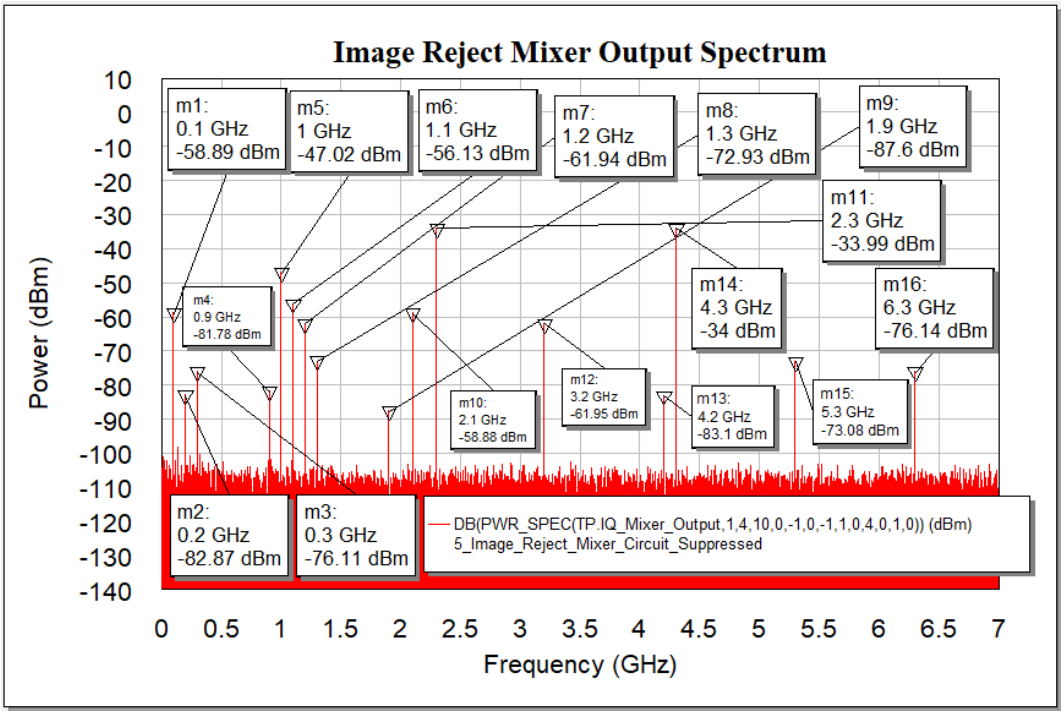

Figure 8.22: Image Reject Mixer Output Suppressed

8.3.7 Final Image Reject Mixer Specifications

When the IQ mixer is combined with the RF quadrature coupler it forms an image reject mixer. The final acceptable specifications for this are displayed in Table 8.13 where the IRR is 35dB for an LO input of 10dBm for the down converter to function.

Table 8.13: Final Specifications of the Image Reject Mixer

	Frequency Range	IRR	IP1dB	IIP3	RF-IF Isolation	LO-IF Isolation	NF	Conversion Loss
Parameter	2GHz - 12GHz	35dB	10dBm	20dBm	-30dB	-30dB	10dB	14dB

8.4 Local Oscillator

8.4.1 Core Requirements

The core requirements and parameters needed for the LO that are not demonstrated by the simulator in this section:

- The LO consists of 3 sections. The reference oscillator, synthesizer, and loop filter. The synthesizer has and output RF range of 2GHz to 12GHz from an input reference oscillator of 50MHz. The reference oscillator is a crystal TCXO that has a singled ended output which is a clipped sine wave.
- The loop filter is 2nd order to increase loop stability with a phase margin of 45 degrees and a BW of 3MHz.
- The synthesizer is an IAS type.

8.4.2 Final LO Specifications

Table 8.14 displays the acceptable LO specifications needed for the down converter to function.

Table 8.14: Final Specifications LO

	Frequency Range	**Reference Input Frequency**	**Reference Type and Output**	**Loop Filter BW**	**Loop Filter Order**	**Loop Filter Phase Margin**	**Synthesizer Type**
Parameter	2GHz - 12GHz	50MHz	Crystal TCXO with single ended output that is a clipped sine wave	3MHz	2nd	45 degrees	IAS

8.5 RF Switch

8.5.1 Core Requirements

The core requirements and parameters demonstrated in this section:

- The RF switch operates over a range of VHF (30Mhz) to 2GHz. Return loss is selected to be between 20dB and 15dB. This ensures that only 1% to 3% of power is reflected from the load or source to the DUT. This equates to a VSWR of between 1.222 and 1.433. This is not demonstrated by the simulator.
- The RF switch operates in a SPDT bidirectional format where one input is receives the 100MHz IF and the other input receives the SDR antenna range of 30MHz to 2GHz. This is demonstrated by the simulator.
- The IP1dB, IIP3, insertion loss and isolation are demonstrated by the simulator to see how it influences IMD products, where the acceptable parameter level is chosen for the RF switch to function as a suitable component.
- The MMIC technology component is selected to allow for internal input and output matching to 50Ω on the same integrated circuit. This is not demonstrated by the simulator.
- Other specifications that are not demonstrated, but is a core requirement to function as an acceptable component is that it is solid-state, absorptive, latching (so that when power is removed, the last selected port is still used), break-before-make configuration (not allow the two receive windows to momentarily short between one another when switching is enabled) and hot switching configuration (30dBm).

8.5.2 Base Model Development and Simulation

The behavior model for the RF switch in VSS is used as in Figure 8.23 and parameter values for IP1dB, IIP3 are all set to 10dBm to get the base RF switch model spectrum plot. Isolation is set to 10dB. AWR VSS doesn't consider IIP2 in the simulator and therefore can't be toggled on the base model as this is also not a priority or concern for RF switches. Generally, a good RF switch has an insertion loss of 0.5dB and will therefore use this value in the RF switch base model. Also, in Figure 8.24, ON_INP set to 1 allows IF signal pass and antenna signal to be attenuated while ON_INP set to 2 allows antenna signal pass and IF signal to be attenuated. In Figure 8.24, the two input signals are at 100MHz for the IF from the I/Q mixer and a random signal of 1500MHz will represent the SDR antenna input. Both signals are live and inputted to the switch at 1.9dBm so the output of the RF switch for the IF is at 0dBm as the reference

when the SDR antenna input on the output is at an off state relative to the isolation parameter of 10dB.

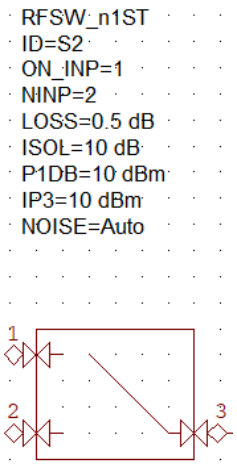

Figure 8.23: RF Switch Base RFSW_n1ST

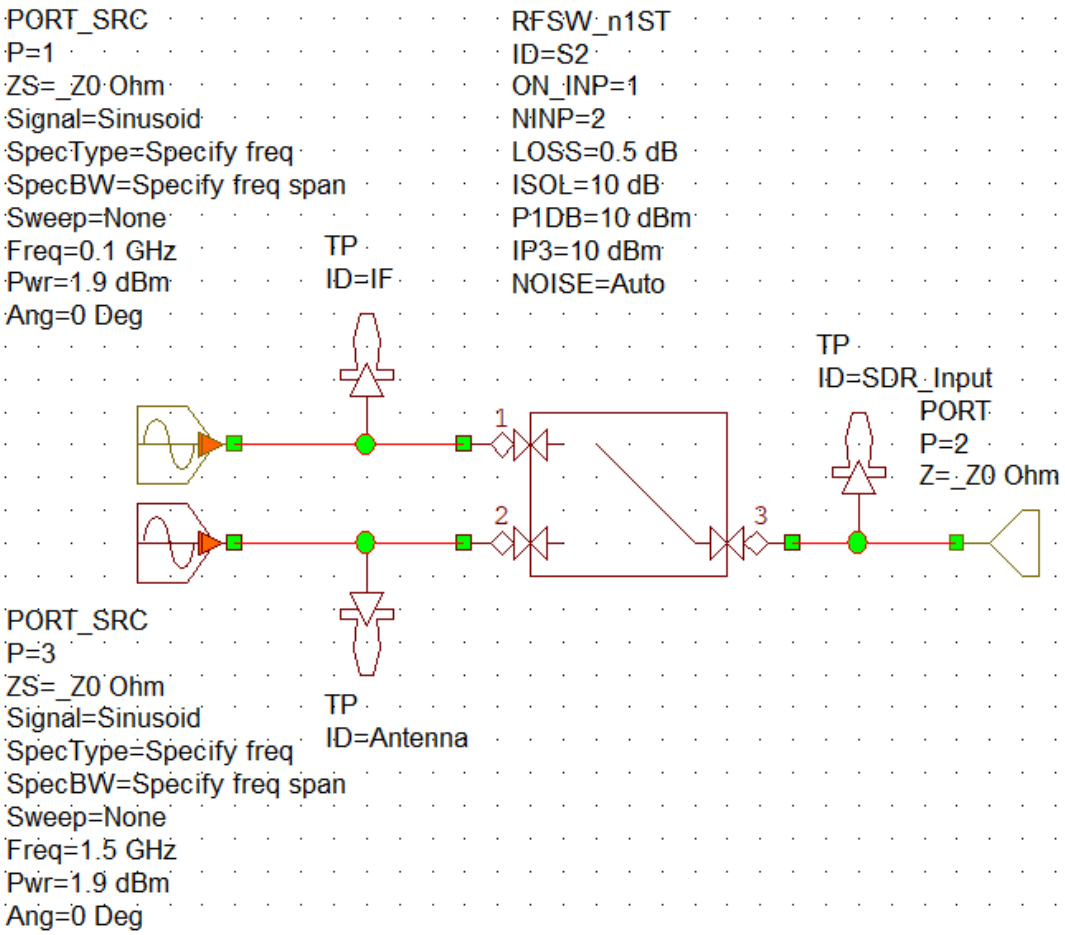

Figure 8.24: RF Switch Base Model Circuit

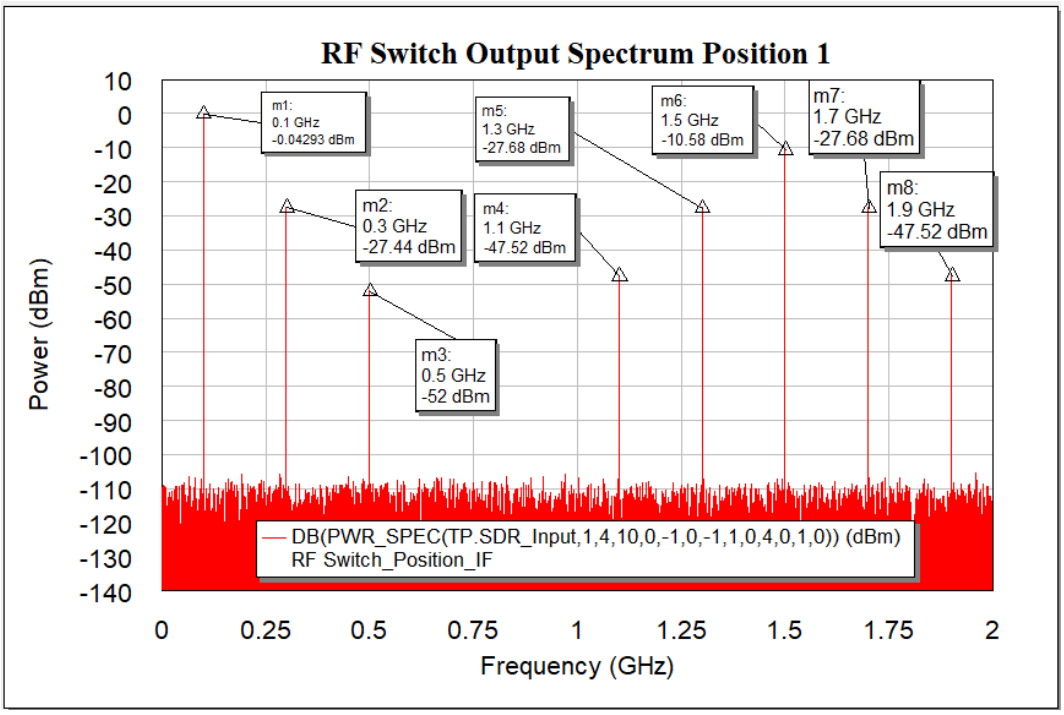

Figure 8.25: RF Switch IMD Products Base Model Position 1

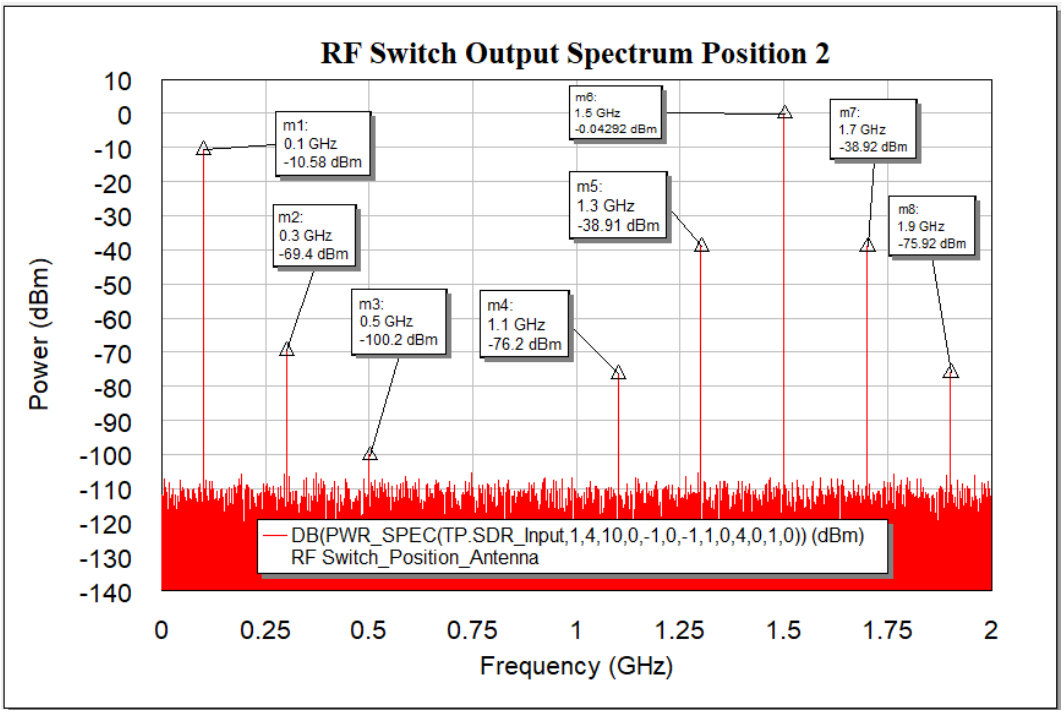

Figure 8.26: RF Switch IMD Products Base Model Position 2

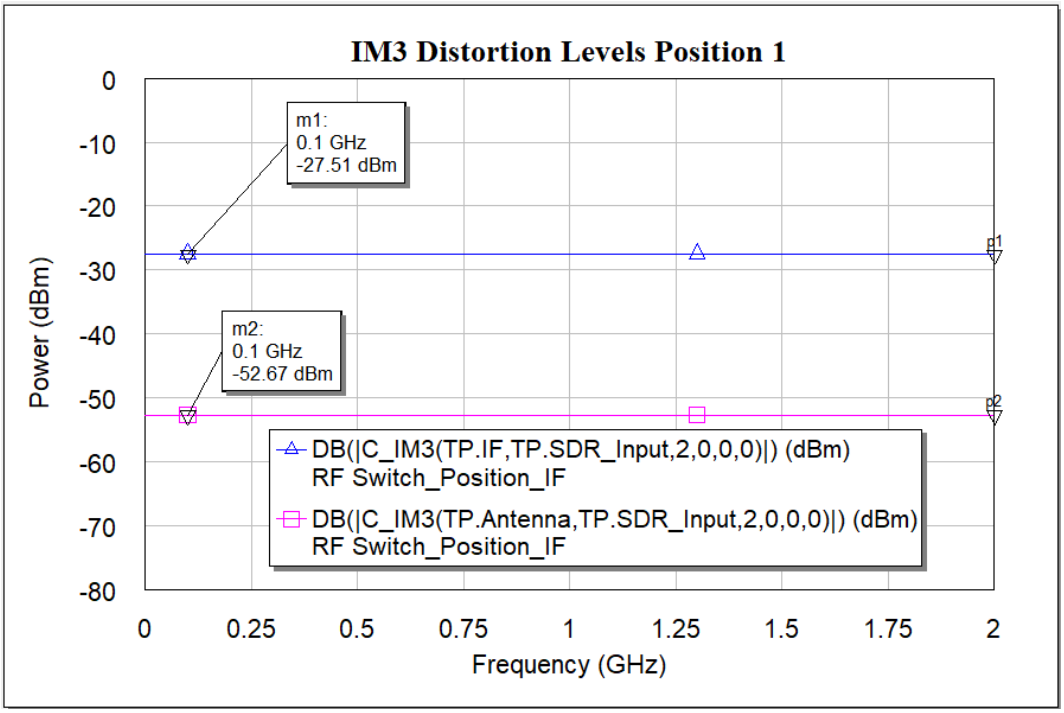

Figure 8.27: IM3 Distortion Level Base Model Position 1

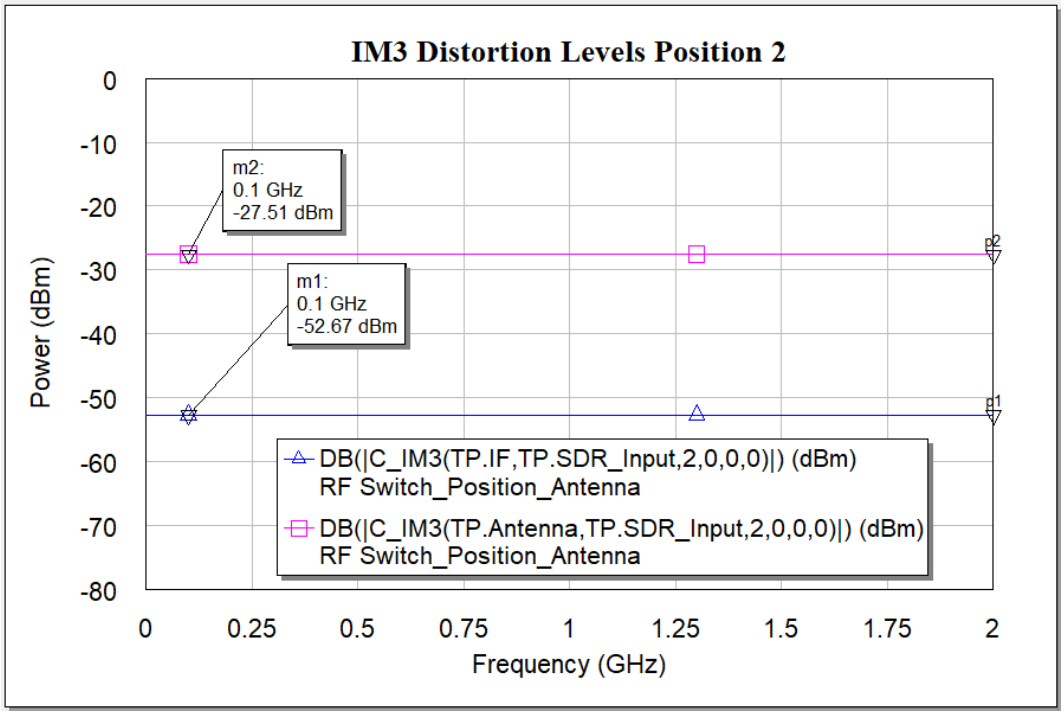

Figure 8.28: IM3 Distortion Level Base Model Position 2

Figure 8.25 representing RF switch in position 1 and Figure 8.26 representing RF switch in position 2, demonstrates that the RF switch base model circuit produces IMD distortion products of the two input signals of 100MHz and 1500MHz. When the RF switch is in position 1, the IF signal of 100MHz is at 0dBm and the antenna signal is at -10.6dBm. When the RF switch is set to position 2, the IF signal of 100MHz is -10.6dBm and the antenna signal is at 0dBm.

Figure 8.27 representing RF switch in position 1 and Figure 8.28 representing RF switch in position 2, demonstrates that the IM3 distortion products are at -28dBm (passed through signal)) and -58dBm (attenuated signal) from 0Ghz to 2GHz. The individual IM3 products can be seen in Table 8.15, Table 8.16, Table 8.17 and Table 8.18 from 0GHz to 2GHz for RF switch positions 1 and 2.

Table 8.15: RF Switch IM3 Distortion Products Position 1

IM3 Distortion Products Position 1		
Frequency	**$2f_2+f_1$**	**$3f_1$**
	1.7GHz	0.3GHz
Power Level	-28dBm	-27dBm

Table 8.16: RF Switch Other Distortion Products Position 1

Other Distortion Products Position 1				
Frequency	0.5GHz	1.1GHz	1.3GHz	1.9GHz
Power Level	-52dBm	-48dBm	-28dBm	-48dBm

Table 8.17: RF Switch IM3 Distortion Products Position 2

IM3 Distortion Products Position 2		
Frequency	**$2f_2+f_1$**	**$3f_1$**
	1.7GHz	0.3GHz
Power Level	-28dBm	-28dBm

Table 8.18: RF Switch Other Distortion Products Position 2

Other Distortion Products Position 2				
Frequency	0.5GHz	1.1GHz	1.3GHz	1.9GHz
Power Level	-52dBm	-28dBm	-28dBm	-48dBm

8.5.3 Optimization of RF Switch Base Model and Simulation

The next step is to reduce the large IM3 and the other distortion products as in Figure 8.27. In AWR the optimization goal function optimizes the IP1db, IIP3 and isolation parameters of the RF switch so that the IM3 and other distortion products are at acceptable levels. The acceptable level that the IMD is optimized for is chosen as -100dBm. Limits are set for IP1dB between 0dBm and 40dBm, IIP3 set between 0 and 60dBm and isolation set between 0 and 50dB, to achieve the -100dBm IMD product level from 0GHz to 2GHz. After the optimization goal has been met, the results as in Figure 8.30 demonstrates that the IM3 and other distortion products when the RF switch is in position 1, was reduced to -100dBm with the isolated SDR

antenna signal reduced to -48dBm. The IF signal though has increased to 1.4dB because of the improvement on the RF switch parameters. The new RF switch parameters are IP1dB = 40dBm, IIP3 = 50dBm and isolation = 50dB. Figure 8.31 demonstrates the result from RF switch in position 2 with the new RF switch parameters. Figure 8.32 confirms that the IM3 distortion products were reduced to below -100dBm. Figure 8.33 demonstrates that when the RF switch is in the position 2 it will allow the SDR antenna input signal through and isolate the IF signal by 48dB.

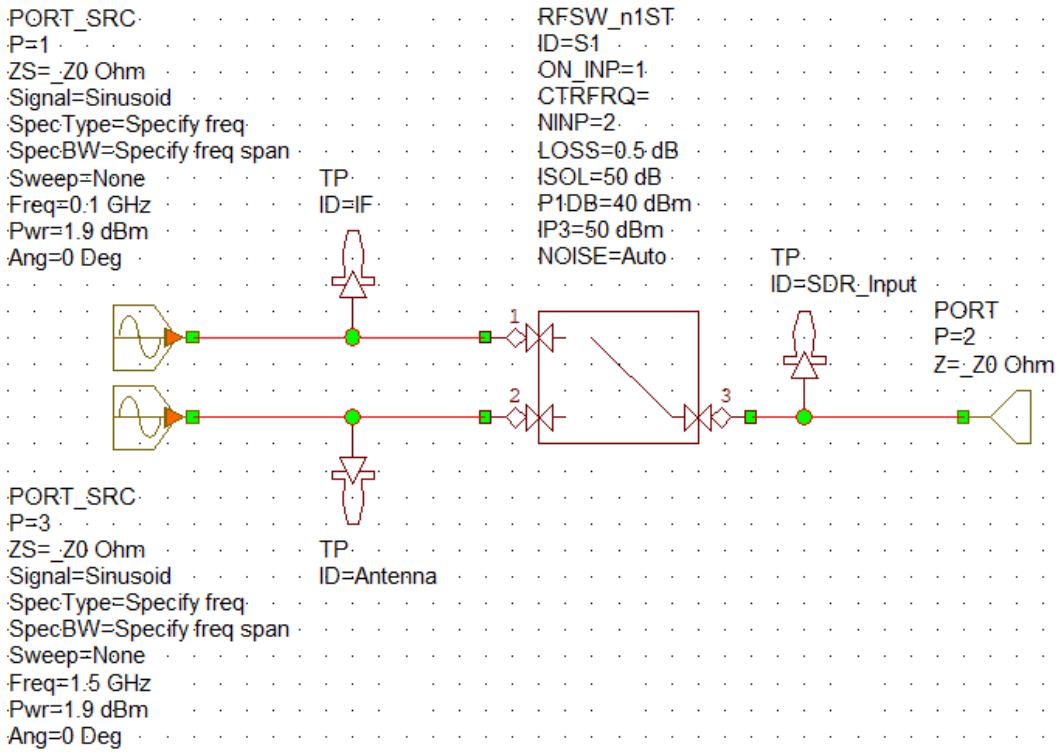

Figure 8.29: Optimized RF Switch Base Model

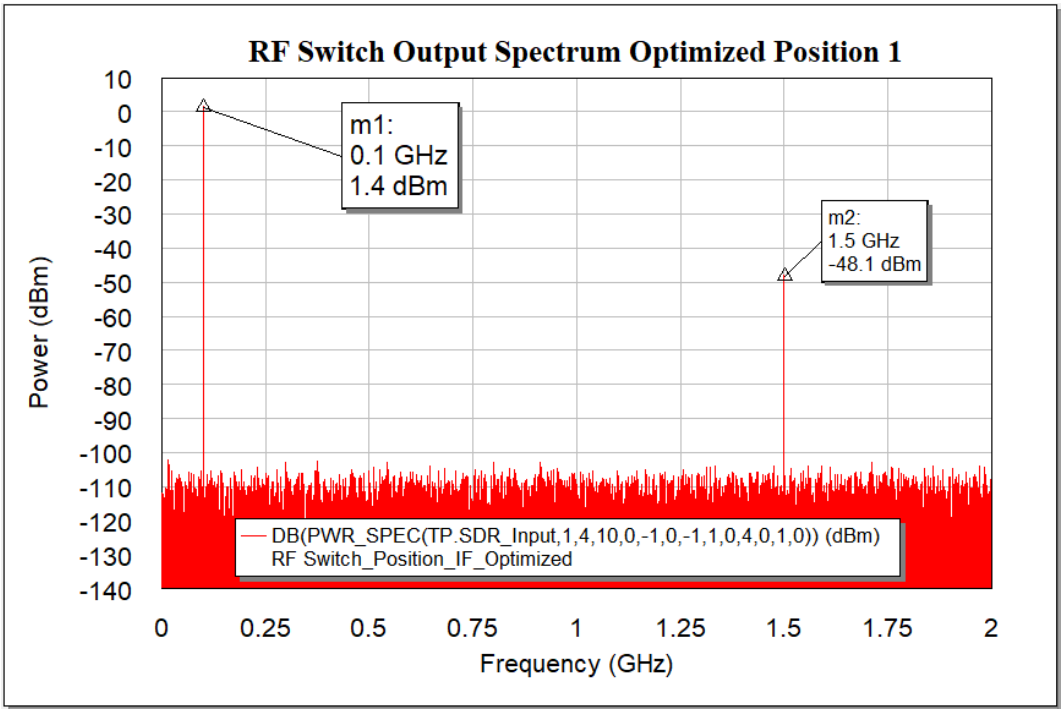

Figure 8.30: Optimized Output Spectrum IF Position 1

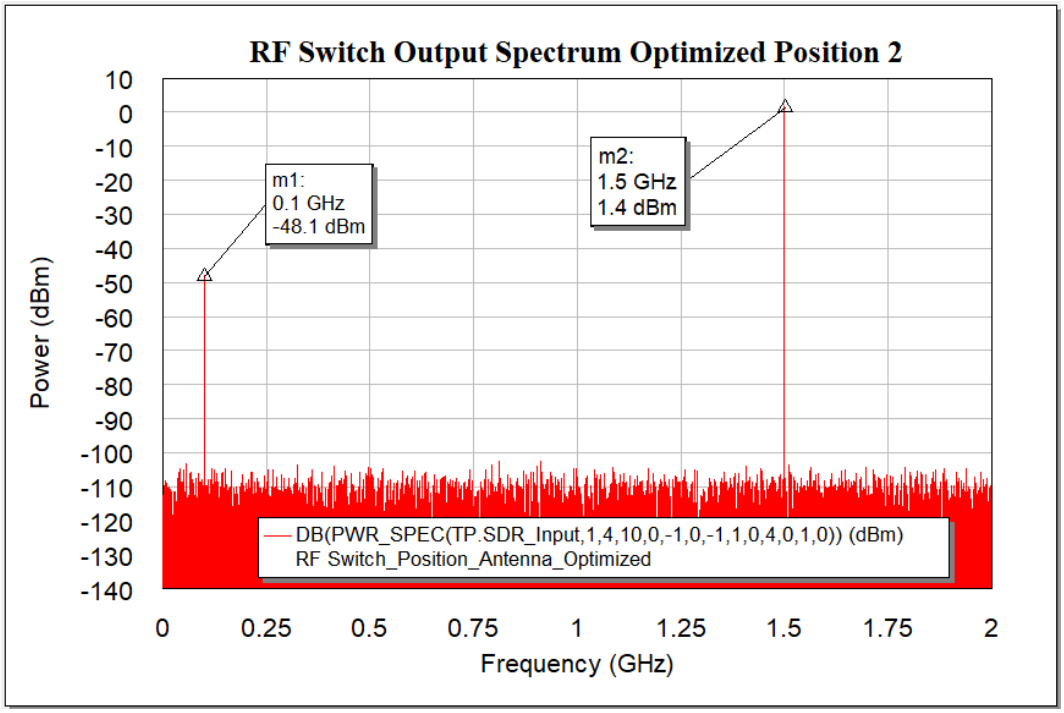

Figure 8.31: Optimized Output Spectrum Position 2

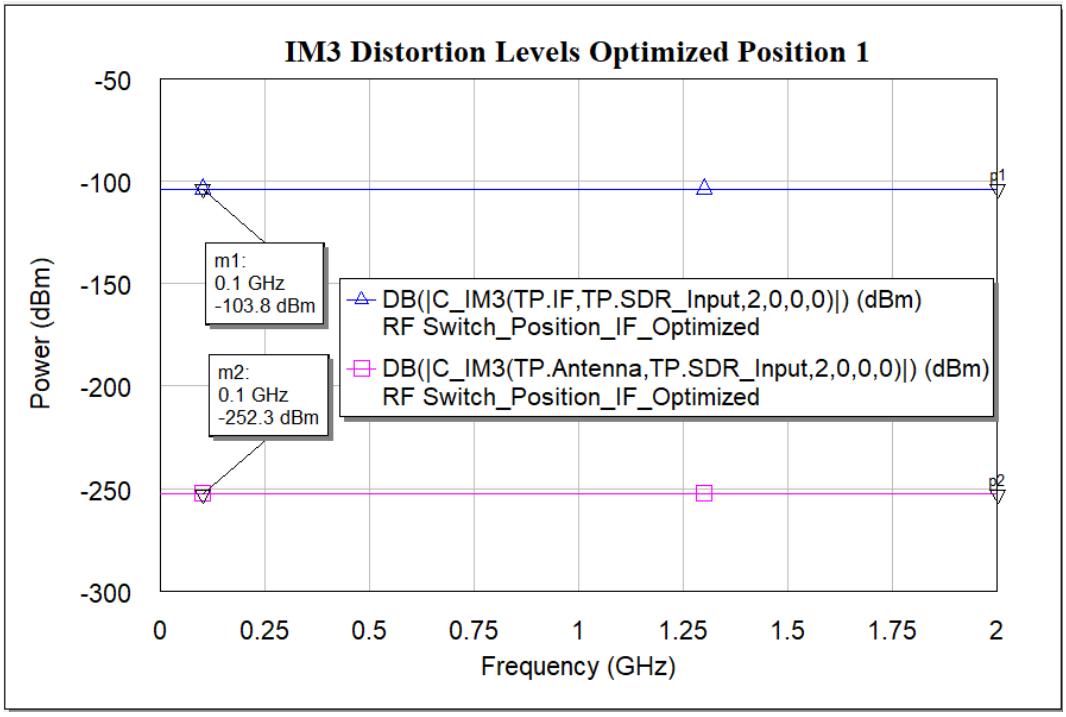

Figure 8.32: Optimized RF Switch IM3 Distortion Levels Position 1

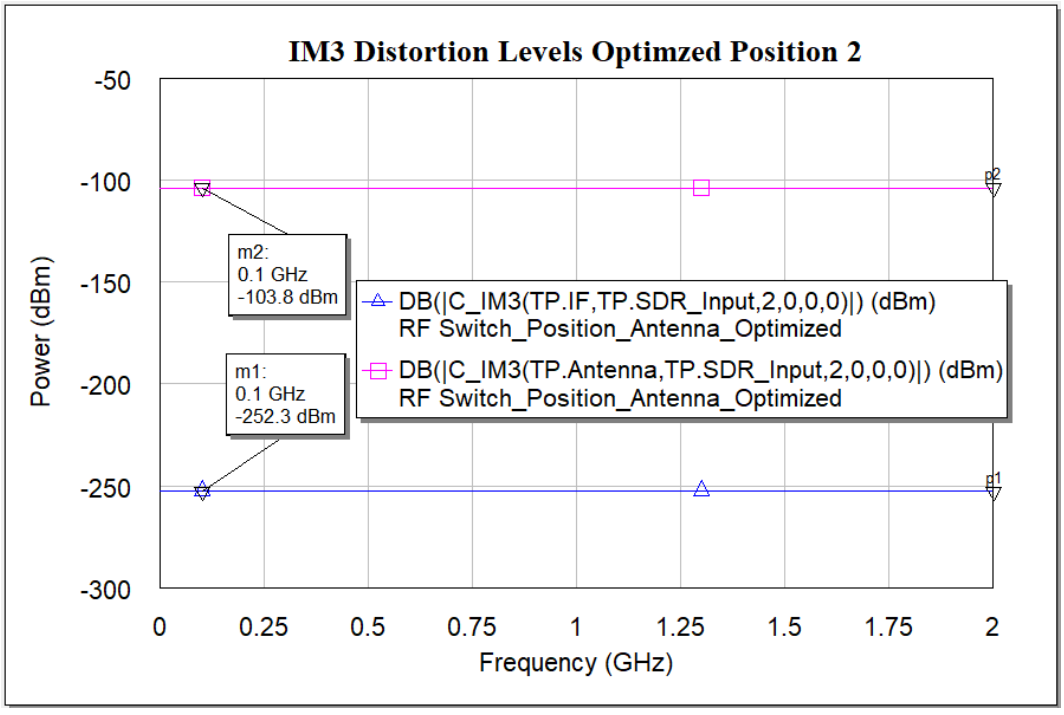

Figure 8.33: Optimized RF Switch IM3 Distortion Levels Position 2

8.5.4 Final RF Switch Specifications

Table 8.19 displays the acceptable RF Switch specifications needed for the down converter to function.

Table 8.19: Final Specifications of RF Switch

	Frequency Range	IP1dB	IIP3	Isolation	Insertion Loss	Input/Output Return Loss
Parameter	VHF - 2GHz	40dBm	50dBm	50dBm	0.5dB	15dB ≤ RL ≤ 20dB

8.6 Quadrature Coupler (IF 90º Hybrid Coupler)

8.6.1 Core Requirements

The core requirements and parameters to be demonstrated in this section:

- The RF quadrature coupler operates over a range of 50MHz to 150MHz. Return loss is selected to be between 25dB and 20dB. This ensures that only 0,32% to 1% of power is reflected from the load or source to the DUT. This equates to a VSWR of between 1.12 and 1.22. This is not demonstrated by the simulator.
- The amplitude and phase unbalance, insertion loss and isolation are demonstrated by the simulator to see how it influences the output, where the acceptable parameter level is chosen for the RF quadrature coupler to function as a suitable component.
- The MMIC technology component is selected to allow for internal input and output matching to 50Ω on the same integrated circuit. This is not demonstrated by the simulator.
- Other specifications that are not demonstrated, but is core requirement to function as an acceptable component that is a multi-sectional strip-line used in broadside configuration, is symmetrically designed, this provides a constant 90° phase shift over the frequency of operation.

8.6.2 Base Model Development and Simulation

The behavior model for the RF quadrature coupler in VSS is used as in Figure 8.34 and parameter values for amplitude unbalance (K) and phase unbalance (PHSBAL) are set to 0dB. VSWR is set to 1. The operation of the coupler advances by 90 degrees (+90) indicated by PHYSTYP=0 deg/90 deg. The input ports are port 1 and port 2. The output ports are port 3 which represents the wanted sideband and port 4 which is not shown on the circuit, represents

the unwanted sideband and is internally matched to 50Ω. The unwanted sideband is also known as the image sideband. Generally, a good coupler has an insertion loss of 0.5dB and will therefore use this value in the RF quadrature coupler base model. A further 3dB loss is added for the combiner/splitter function of the coupler. As in Figure 8.35, the two input signals are at 100MHz for the IF from the I/Q mixer. Both signals are live and inputted to the coupler at a level of 0.5dBm so the output of the coupler is at 0dBm as a reference. The phase shifter in Figure 8.35 shifts the second signal by 0, -90 and +90, to demonstrate what the RF quadrature coupler does to the two signals combined and will not be part of the final RF quadrature model. Isolation can't be measured or implemented by using this model and will therefore be set as 20dB for the final RF quadrature base model.

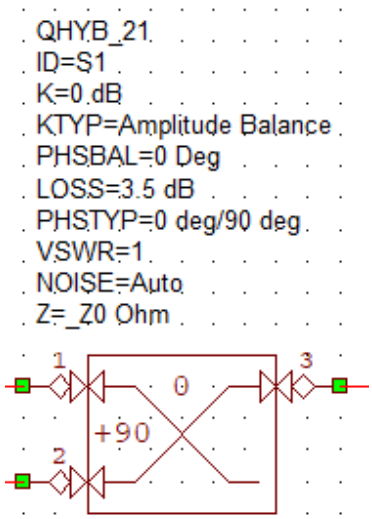

Figure 8.34: Base Model RF Quadrature Coupler

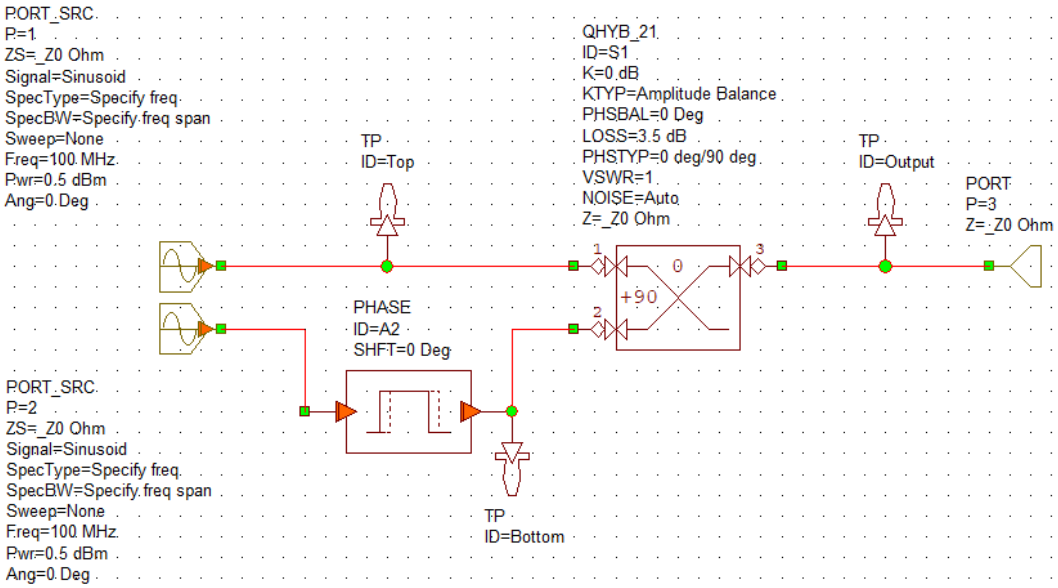

Figure 8.35 Quad Coupler Base Model Test Circuit

When the phase shifter is set to 0 degree phase shift, Figure 8.37 demonstrates that the two input signals are equal in phase at the input of the RF quadrature coupler. At the output of the RF quadrature coupler as in Figure 8.36, the two input signals are now +90 degrees out of phase within the quadrature coupler with each another and therefore produces a -3dBm output at 100MHz and acts as ordinary conductor with a loss of 0.5dB.

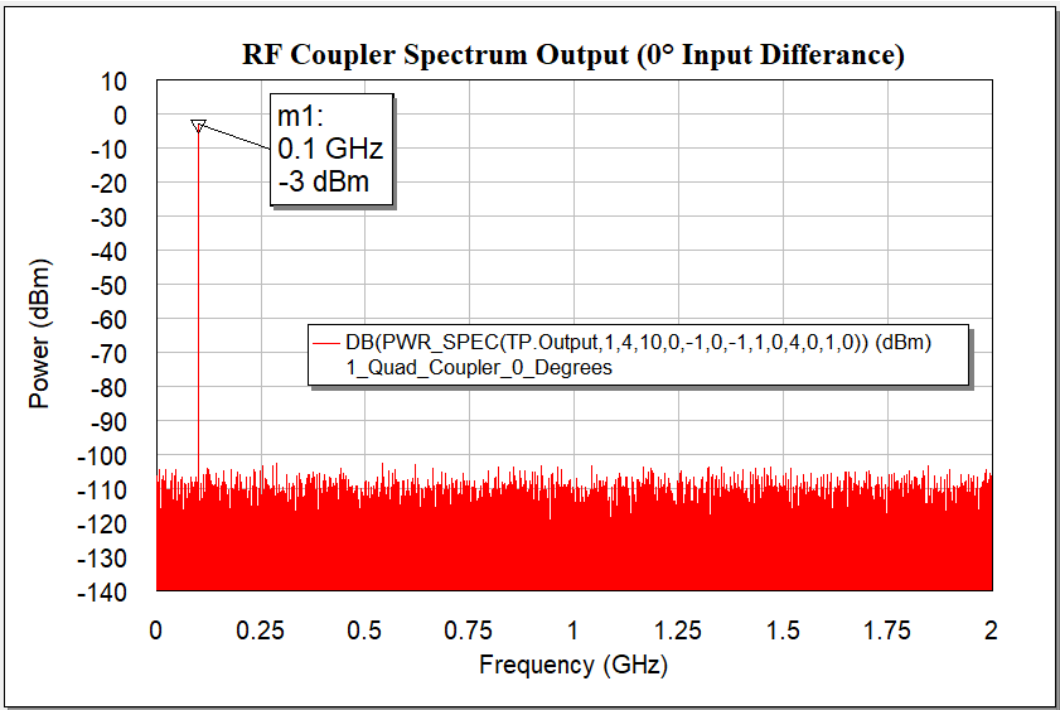

Figure 8.36: RF Quadrature Coupler Phase Shifter 0 degrees

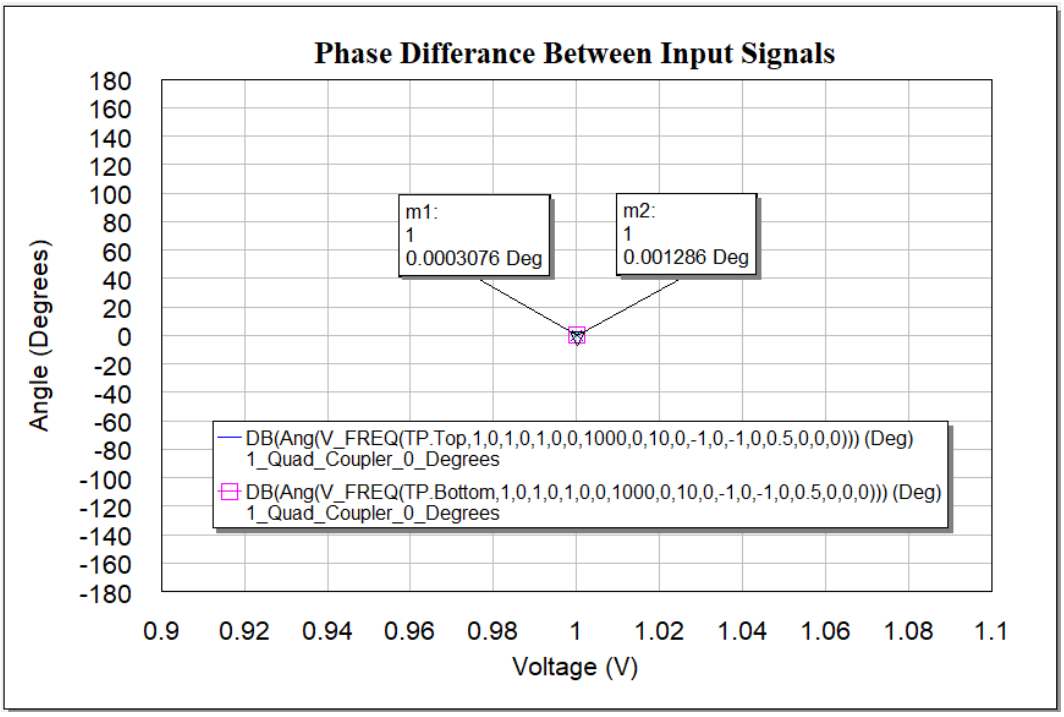

Figure 8.37: 0º Phase Difference Between Input Signals

When the phase shifter is set to +90 degrees, Figure 8.39 demonstrates that the bottom input signal advances by 90 degrees at the input of the RF quadrature coupler. At the output of the RF quadrature coupler as in Figure 8.38, the two input signals are now +180 degrees out of phase within the quadrature coupler with each another. Therefore, the input signals cancels out each another and produces no output at 100MHz. Port 4, within the quadrature coupler and not shown on the circuit in theory has the unwanted sideband output power doubled.

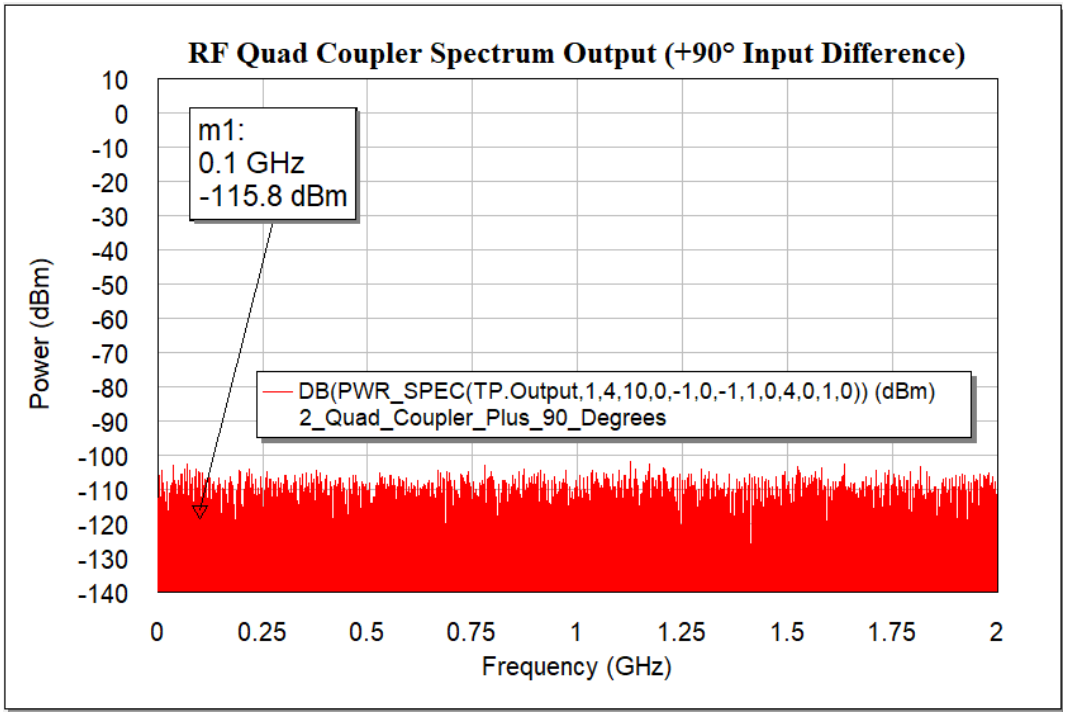

Figure 8.38: Output Signal Suppressed

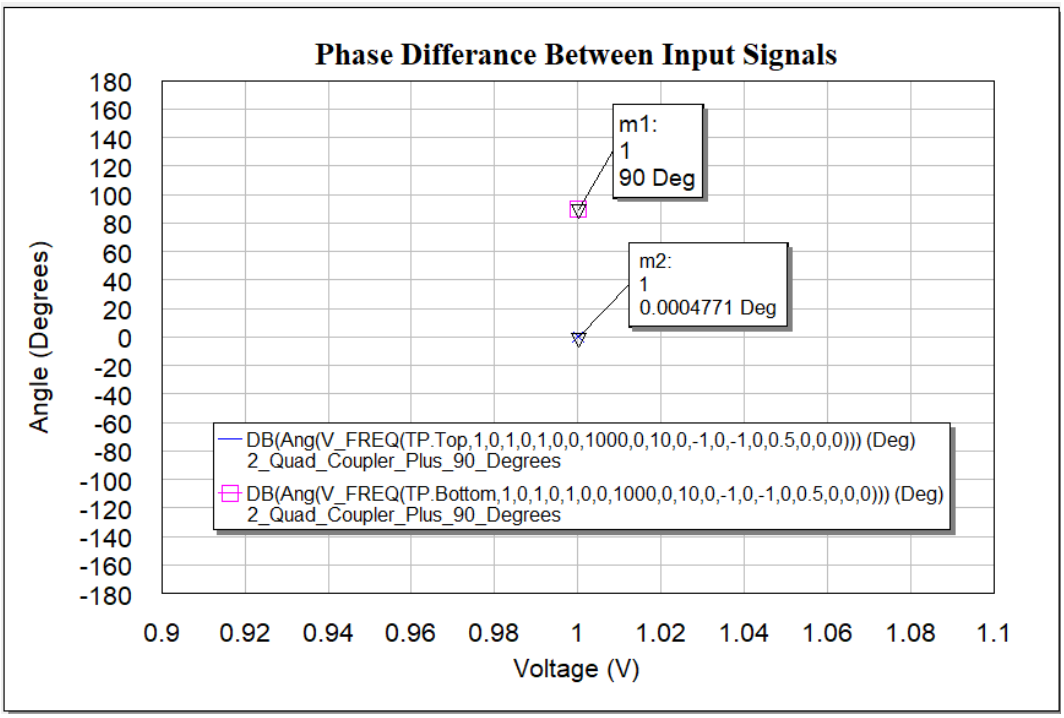

Figure 8.39: +90º Phase Difference Between Input Signals

When the phase shifter is set to -90 degrees, Figure 8.41 demonstrates that the bottom input signal is delayed by 90 degrees at the input of the RF quadrature coupler. At the output of the RF quadrature coupler as in Figure 8.40, the two input signals are now 0 degrees out of phase within the quadrature coupler with each another. Therefore, the input signals add and produces an output of 0dBm at 100MHz. The output power is thus doubled from the input of 0.5dBm. Port 4 not shown on the circuit but in theory has the unwanted sideband totally suppressed.

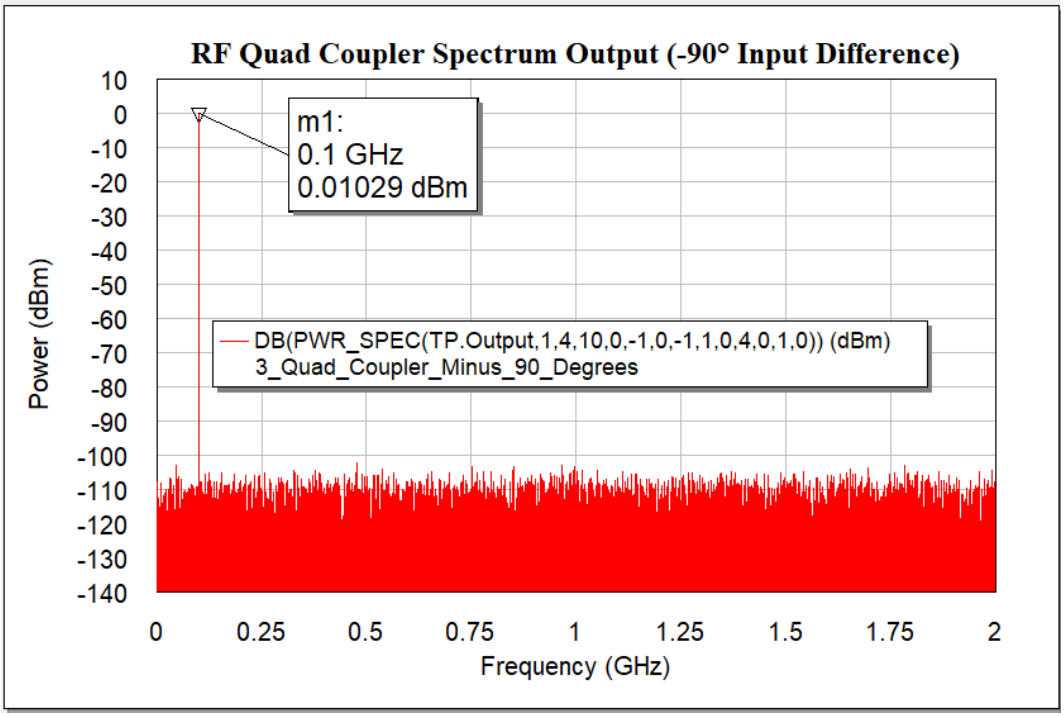

Figure 8.40: Output Power Doubled

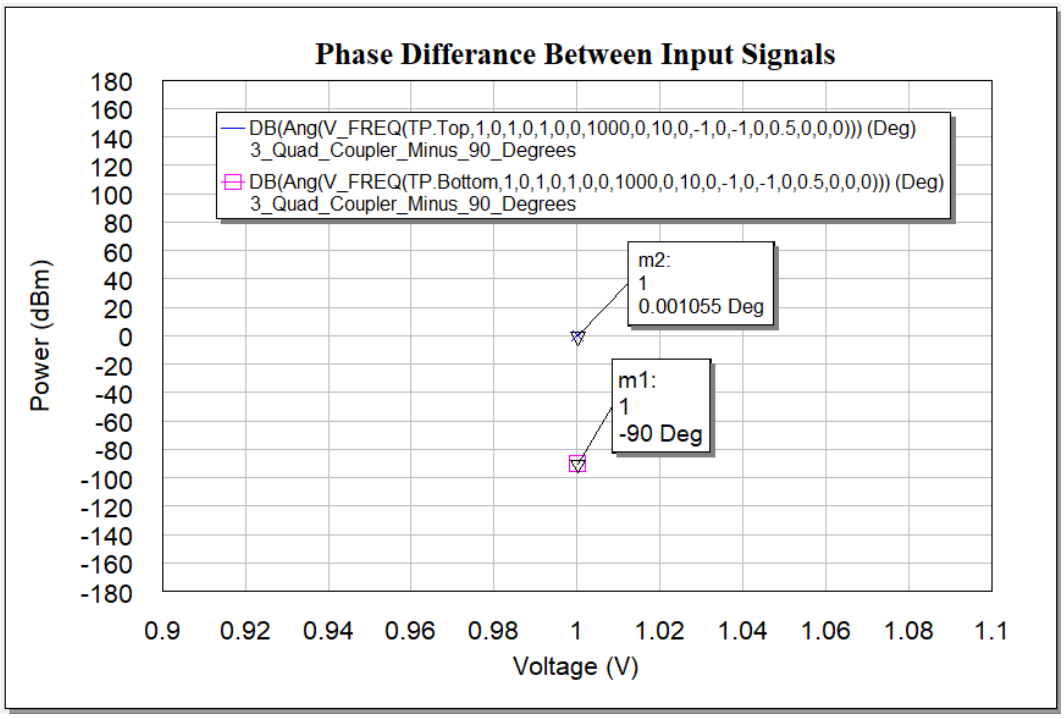

Figure 8.41: -90° Phase Difference Between Input Signals

8.6.3 Limit Specs of RF Quadrature Coupler Base Model and Simulation

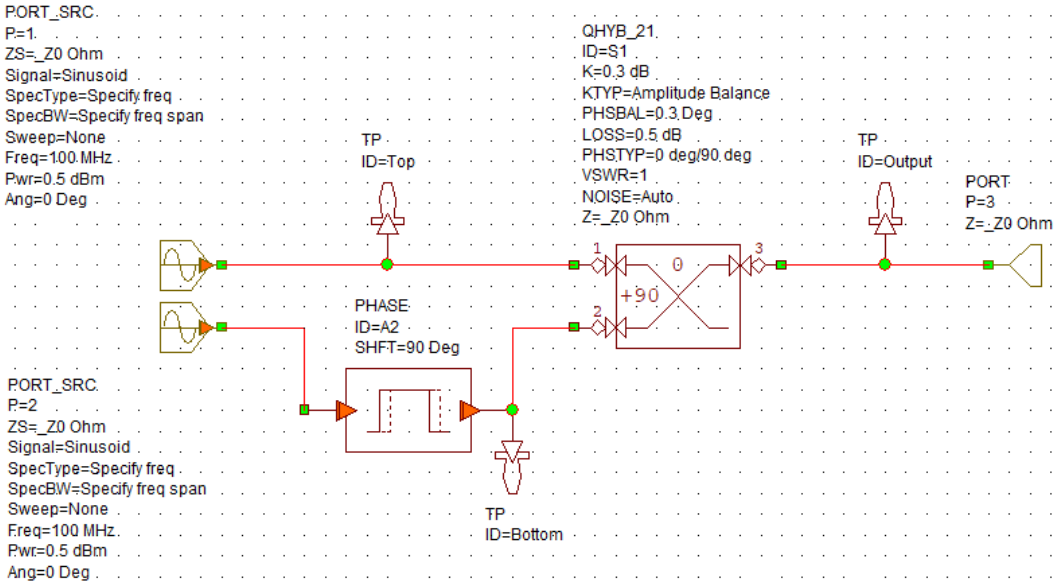

Figure 8.42: Limits for Amplitude and Phase Balance

Setting the phase shifter to +90 degrees as in Figure 8.42, the output is completely suppressed. This can be used to infer the level of the unwanted sideband or image signal. This level of suppression though, is not possible because the amplitude and phase will always have an imbalance. This imbalance is therefore presented in the base model to allow a realistic suppression level of 35dB as seen in Figure 8.43, where amplitude unbalance (k) is now ±0.3dB and phase unbalance (PHSBAL) is now ±0.3 degrees as in Figure 8.42 to achieve this level of suppression.

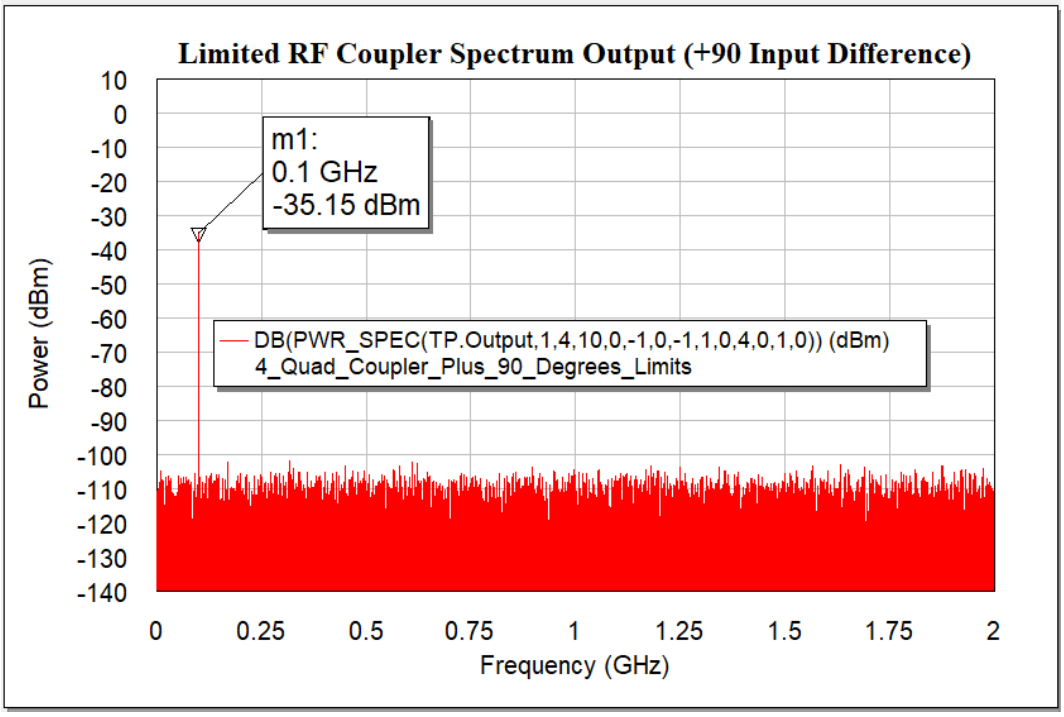

Figure 8.43: Inferred Suppression Level of Unwanted Sideband or Image Signal

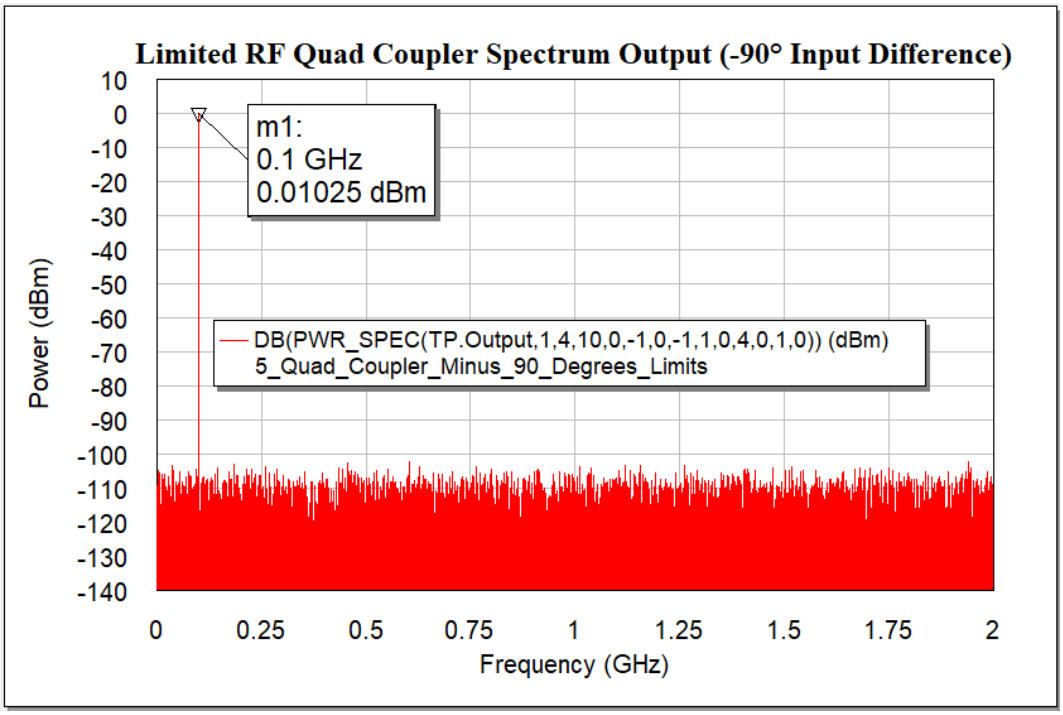

Figure 8.44: Wanted Sideband Output after Limits Added

By setting the phase shifter now to -90 degrees, Figure 8.44 demonstrates that the output power is still doubled in power and therefore not affected by a great deal when amplitude balance and phase balance changes by ±0.3dB and ±0.3 degrees respectively. Table 8.20 shows the new parameters for the RF quadrature coupler with the addition of 3dB of insertion loss that is unavoidable because of the nature of splitter/combiners. Isolation and VSWR couldn't be demonstrated with the VSS simulator. Therefore, isolation is chosen to be 25dB between the two input ports of the RF quadrature coupler and VSWR is chosen to be 1.15dB of the ports of the RF quadrature coupler.

8.6.4 Final RF Quadrature Coupler Specifications

Table 8.20: Final Specifications of the RF Quadrature Coupler

	Frequency Range	Amplitude Unbalance	Phase Unbalance	Insertion Loss	Isolation	Input/Output Return Loss
Parameter	50MHz – 150MHz	±0.3dB	±0.3 Degrees	3.5dB	25dB	20dB ≤ RL ≤ 25dB

8.7 Complete Down Converter

8.7.1 Introduction

The simulated down converter for the SDR environment, to detect energy from the VHF to X-Band can be seen Figure 8.45. There are no filters to reduce the number of RF components

used and complexity. The RF component specifications and parameters were chosen to provide acceptable levels for the down converter to detect energy from the VHF to X-Band. These acceptable levels are further examined through this section because all the individual RF components simulated and examined in chapter sections 8.1 to 8.6 will impact the final IF output of 100MHz that is provided to the SDR via the RF switch.

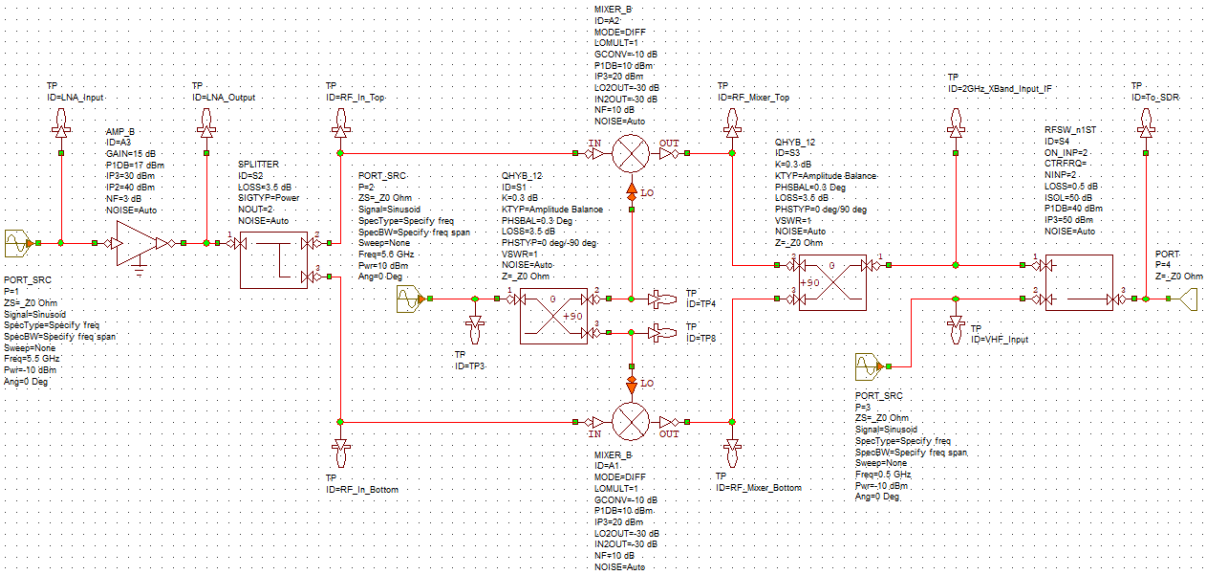

Figure 8.45: Down Converter from the VHF to X-Band

8.7.2 Results of Simulated Down Converter

A -10dBm level arbitrary signal at 5.5GHz is applied to the LNA as in Figure 8.45 and results in an output of 4.97dBm as in Figure 8.46 due the parameters of the LNA. Also seen in Figure 8.46 is the harmonic at 11GHz with power level of -36.03dBm. The harmonic is from the input signal at 5.5GHz. The splitter reduces the input signal at the IQ mixer by 3.5db to a power level of 1.47dBm and supplies the top and bottom RF mixers of the IQ mixer. A 10dBm arbitrary signal at 5.6GHz is used as an LO to produce the 100MHz IF. This LO is then used in quadrature and supplied to the LO inputs of the IQ mixer. This produces the equal amplitude 100MHz IF at -8.65dBm and other IMD product's as in Figure 8.47. They are in quadrature as indicated in Figure 8.48. The next section uses a quadrate coupler as in Figure 8.45 to combine the quadrature 100MHz IF and other IMD products with one another. This results in the output doubling in power but is at the same time attenuated by 0.5dB due to the loss of the quadrature coupler and is now at -9.15dBm, as in Figure 8.49. The unwanted signal or the image signal if present is attenuated by 34.87dB as in Figure 8.50 and is at -44.02dBm. Therefore, the IRR of the image reject mixer is at 34.87dB with the chosen parameters. Finally, the 100MHz IF is fed into the RF switch, which switches between the 2GHz to X-band input (Position 1) and the VHF input (Position 2) and when required. The output of the RF switch consists of the down converter IF and the VHF input. Therefore, when a -10dBm, 5.5GHz arbitrary signal is applied

to input of the LNA section, and a -10dBm, 500MHz (VHF) arbitrary signal is applied to the RF switch (Port 2), produces a -9.65dBm power level IF and -60dBm power level VHF as in Figure 8.51. This occurs only when the RF switch is set to position 1 which permits the IF to be switched through and attenuates the VHF signal. When the RF switch is set to position 2 this permits the VHF signal to switch through and attenuate the IF signal. This results in an IF now at -59.12dBm and a VHF signal of -10.5dBm as in Figure 8.52.

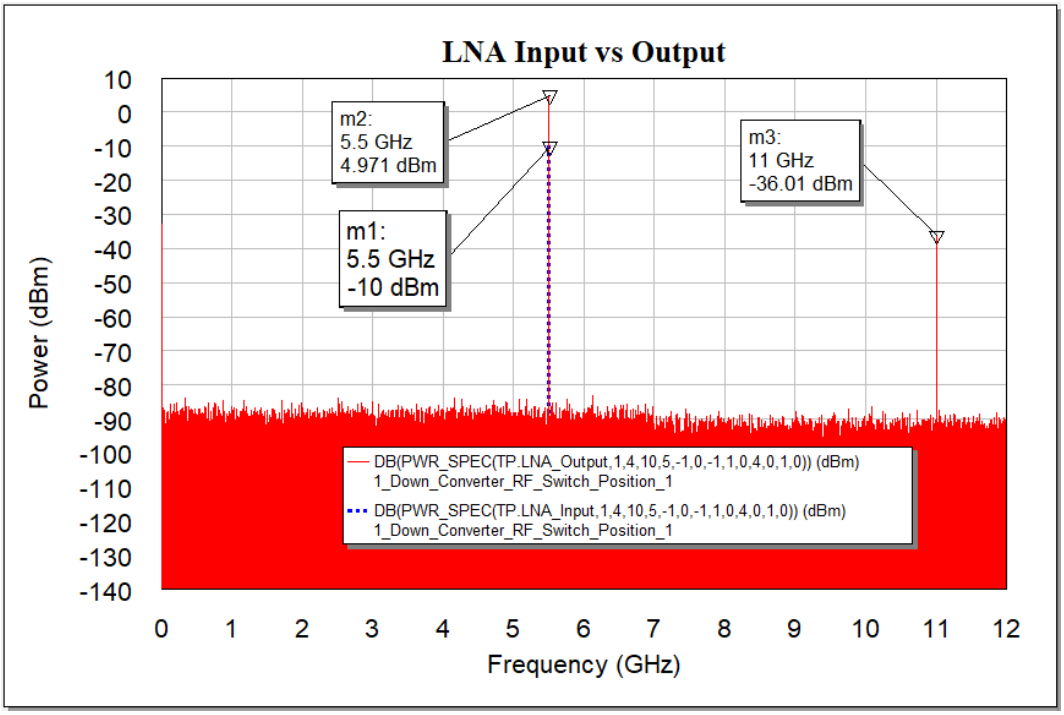

Figure 8.46: LNA Input (Blue) vs Output (Red)

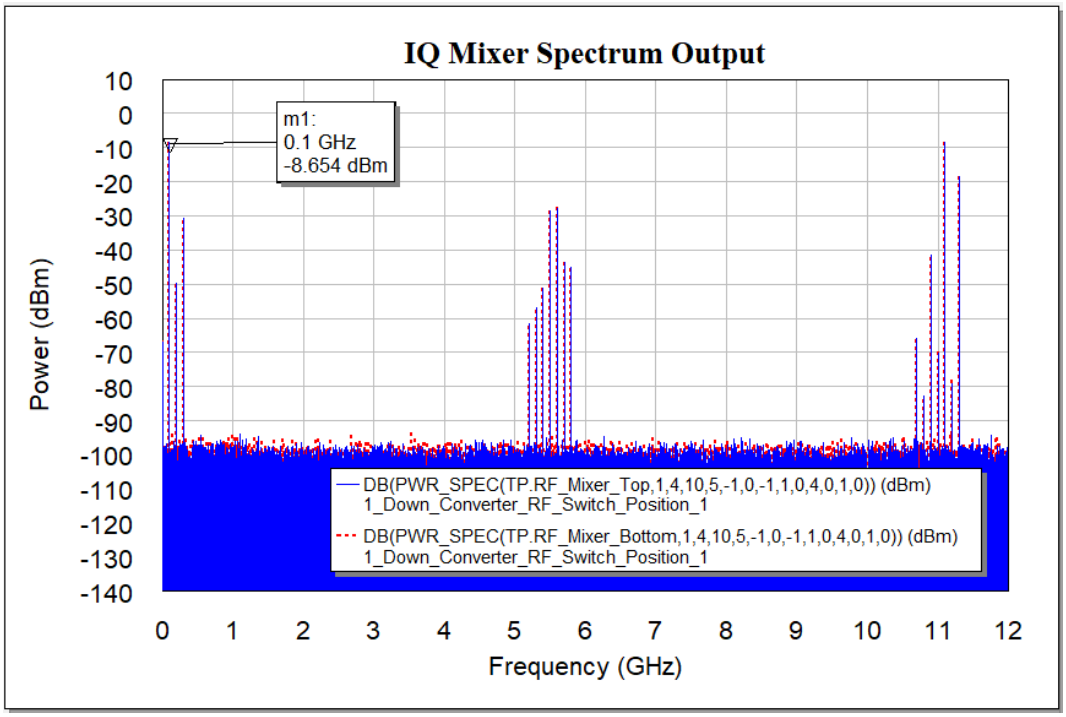

Figure 8.47: IQ Mixer Spectrum Output Top vs Bottom

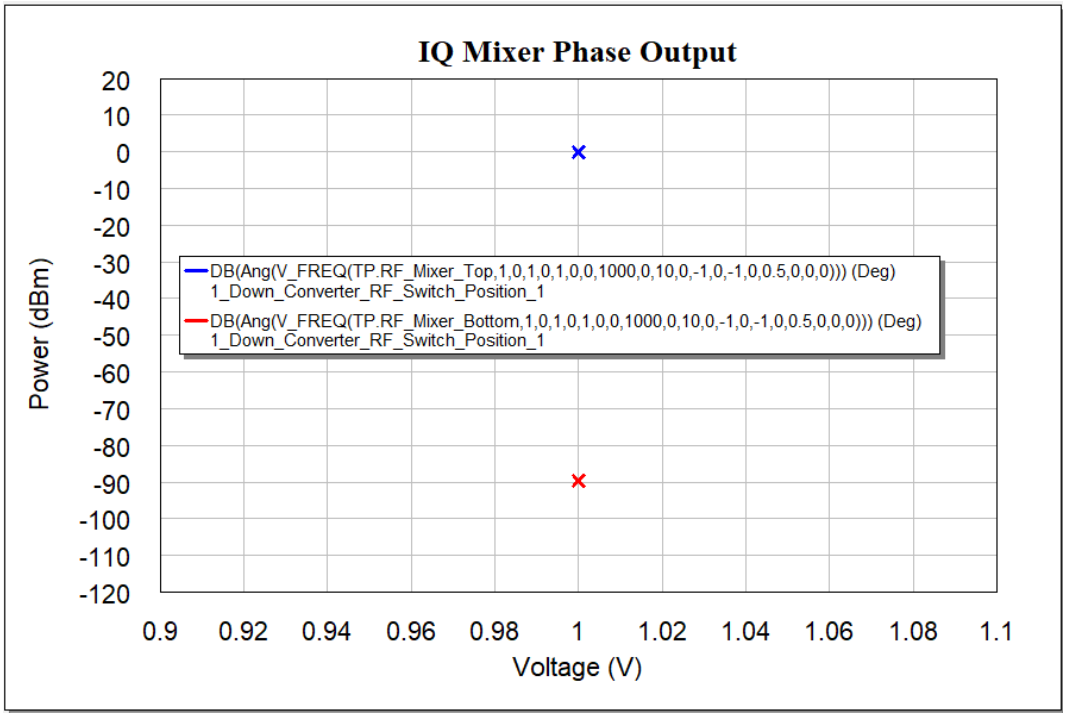

Figure 8.48: IQ Mixer Phase Output Top vs Bottom

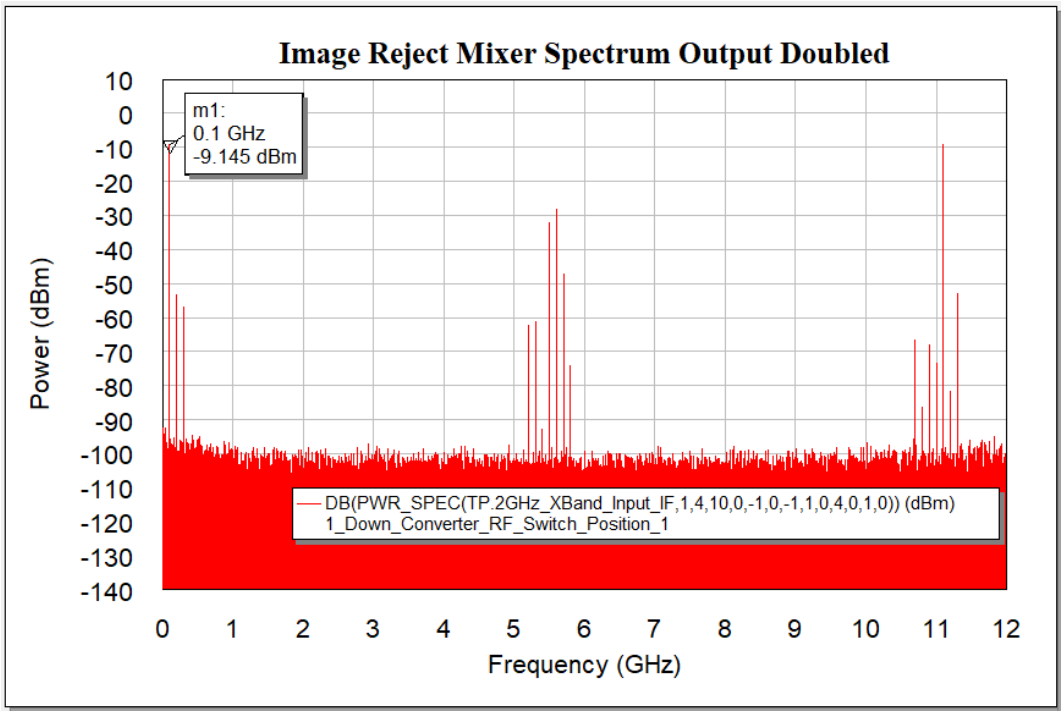

Figure 8.49: Image Reject Mixer Output Wanted

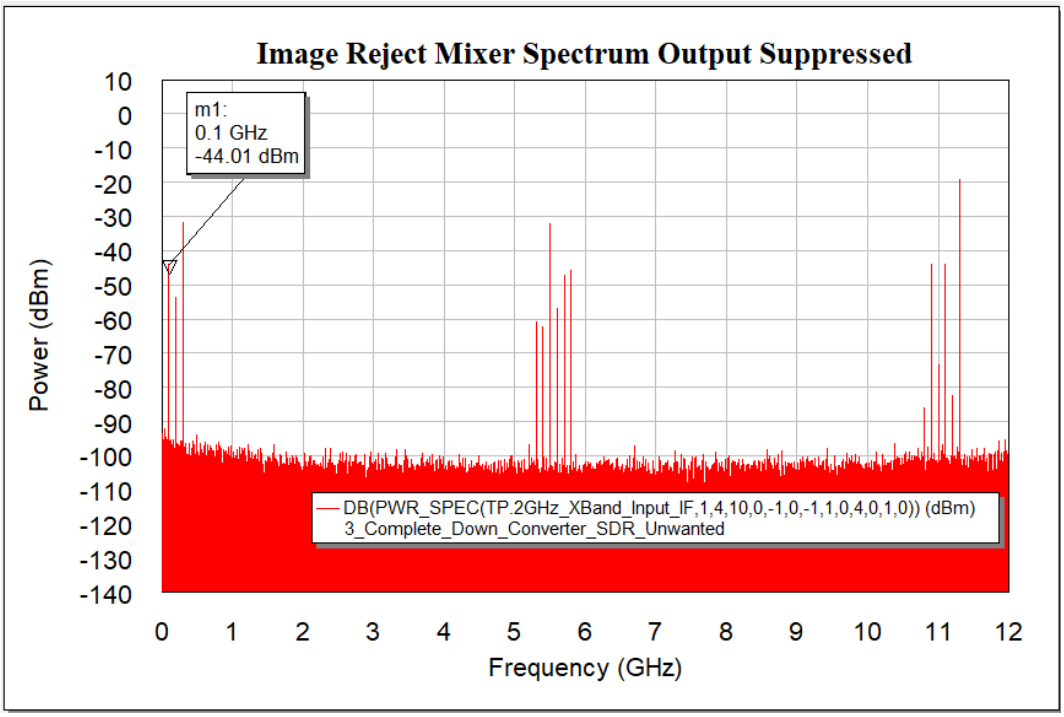

Figure 8.50: Image Reject Mixer Output Unwanted

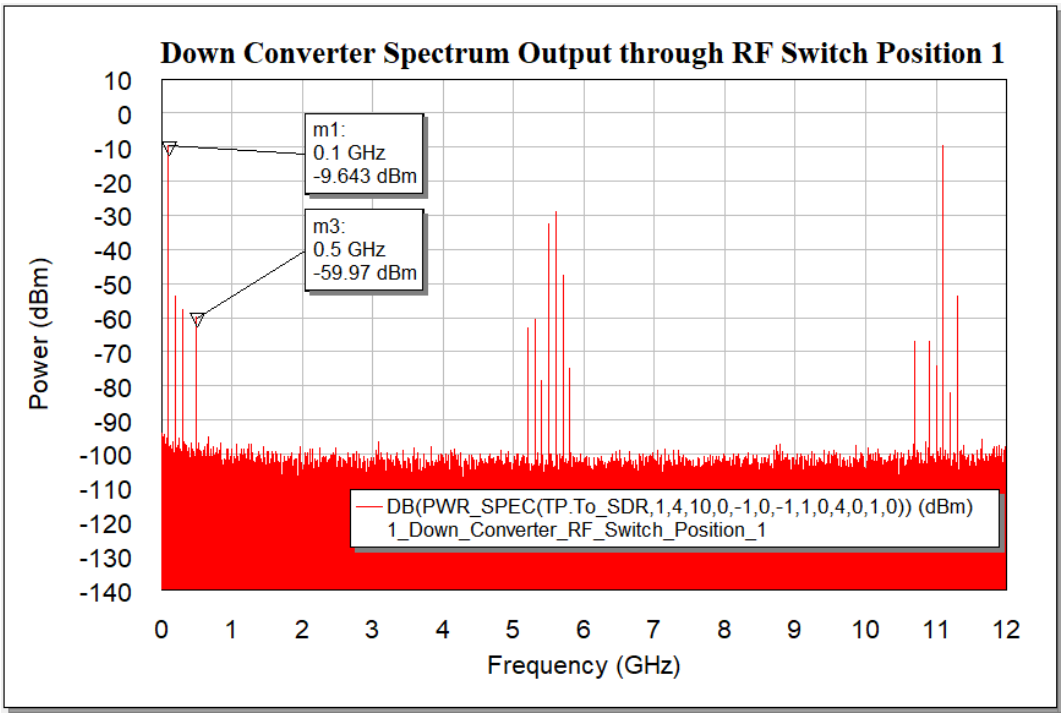

Figure 8.51: Spectrum Output RF Switch Position 1

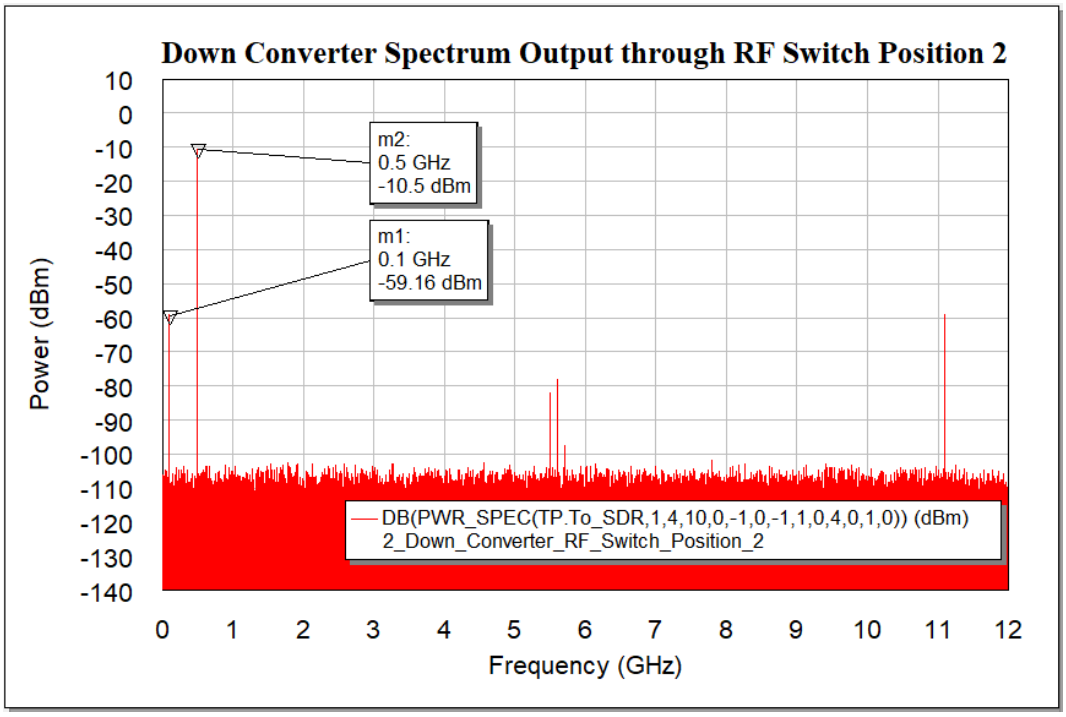

Figure 8.52: Spectrum Output RF Switch Position 2

8.8 Chapter Summary

In this chapter the specifications of each RF component as in Table 8.21, that constitutes the down converter to perceive energy from the VHF to X-Band was determined. An example was also used to prove the concept of the alternative front-end receiver architecture.

Table 8.21: Final Specifications of the RF Components that Constitutes the Down Converter

<table>
<tr><th>RF Component</th><th>LNA</th><th>I/Q Mixer (Image Reject Mixer)</th><th>Quadrature Coupler</th><th>RF switch</th><th>LO</th></tr>
<tr><td>Type</td><td>MMIC unconditionally stable over frequency range</td><td>MMIC Double Balanced Mixer</td><td>MMIC Multi-Sectional Strip-Line in Broadside Configuration</td><td>MMIC, Bidirectional solid state SPDT switch with absorptive, latching, break-before-make and 30dBm hot switching functions</td><td>50MHz Crystal TCXO reference with single ended output that is a clipped sine wave and IAS Synthesizer</td></tr>
<tr><td>Frequency Range</td><td>2-12GHz</td><td>2-12GHz</td><td>50MHz-150MHz</td><td>VHF-2GHz</td><td>2-12GHz</td></tr>
<tr><td>Loop Filter Order, BW and Phase Margin</td><td colspan="4">N/A</td><td>2nd, 3MHz and 45 Degrees</td></tr>
<tr><td>Gain</td><td>15dB</td><td>N/A</td><td colspan="2" rowspan="5">N/A</td><td rowspan="20">N/A</td></tr>
<tr><td>NF</td><td>3dB</td><td>10dB</td></tr>
<tr><td>OP1dB</td><td>17dBm</td><td rowspan="4">N/A</td></tr>
<tr><td>OIP3</td><td>30dBm</td></tr>
<tr><td>OIP2</td><td>40dBm</td></tr>
<tr><td>Input/Output Return Loss</td><td>15dB ≤ RL ≤ 20dB</td><td>20dB ≤ RL ≤ 25dB</td><td>15dB ≤ RL ≤ 20dB</td></tr>
<tr><td>IP1dB</td><td rowspan="14">N/A</td><td>10dBm</td><td rowspan="8">N/A</td><td>40dBm</td></tr>
<tr><td>IIP3</td><td>20dBm</td><td>50dBm</td></tr>
<tr><td>RF-IF Isolation</td><td>-30dB</td><td rowspan="7">N/A</td></tr>
<tr><td>LO-IF</td><td>-30dB</td></tr>
<tr><td>Conversion Loss</td><td>13.5dB (14dB)</td></tr>
<tr><td>IRR</td><td>(34.865dB)</td></tr>
<tr><td>IP1dB</td><td rowspan="7">N/A</td></tr>
<tr><td>IIP3</td></tr>
<tr><td>Isolation</td><td>25dB</td><td>50dBm</td></tr>
<tr><td>Insertion Loss</td><td>3.5dB</td><td>0.5dB</td></tr>
<tr><td>Amplitude Unbalance</td><td>±0.3dB</td><td rowspan="2">N/A</td></tr>
<tr><td>Phase Unbalance</td><td>±0.3 Degrees</td></tr>
</table>

Chapter 9

Conclusion and Future Work

9.1 Conclusion

The prime objective of this research was to establish the viability of an alternative front-end receiver architecture that can be implemented to extend the frequency range of a low-priced mobile SDR to perceive energy of frequencies well above the limits of the low-priced SDR and suppress the image occurrence. In this thesis it was to perceive energy of frequencies above 2GHz and up to X-band. Therefore, in theory the low-priced SDR is able to perceive the energy of frequencies from VHF to X-band, considering low-priced SDR's typically start to perceive the energy of frequencies from VHF.

The research established that the proposed design could observe the energy of frequencies and suppress the image occurrence from VHF to X-band. The concept was illustrated by simulating a case study of when a RF signal at 5.5GHz and a LO of 5.6GHz is applied to the alternative front-end receiver architecture (down converter), it produces an IF of 100MHz. The notion also demonstrated that the alternative front-end receiver architecture had the capacity to suppress the image occurrence by 35dB.

9.2 Future Work

- Cadence® Applied Wave Research (AWR®) Microwave Office® (MWO®) suite can be used to further examine the proposed design through:
  - DC analysis to determine DC operating points of the down converter.
  - AC noise analysis to determine the noise contribution of each noise generating element and the overall noise performance of the down converter.
  - Stability analysis to determine what input or output load will render the down converter to be unstable and therefore oscillate.
  - Load-pull analysis to determine what input or output load applied to the down converter will produce what level of output power.
- The subsequent phase can involve physically assembling the down converter with the derived RF components.

  The down converter with some effort can be used in conjunction with a Raspberry Pi mobile processing unit to act as a monitoring station once placed on high sites offering a cheaper alternative to expensive monitoring stations available.

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