Cape Peninsula
University of Technology

SYSTEM LEVEL IMPLEMENTATION OF A C-BAND DOWNCONVERTER FOR A NANOSATELLITE RECEIVER

by

LILIE NALITYE LEOPOLD

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Supervisor: Professor Vipin Balyan

Co-supervisor: Dr Nganyang Paul Bayendang

Bellville Campus

06 December 2023

DECLARATION

I, Lilie Nalitye Leopold, declare that the contents of this thesis represent my own unaided work, and that the thesis has not previously been submitted for academic examination towards any qualification. Furthermore, it represents my own opinions and not necessarily those of the Cape Peninsula University of Technology.

25 August 2023

Signed **Date**

ABSTRACT

In recent years, there has been a growing market interest in CubeSat missions around the world, particularly in the commercial sector for various applications. These include high temporal and spatial resolution imaging, which consist of a number of CubeSats forming a constellation. Consequently, the bandwidth requirements and associated regulatory challenges for these applications increase, which can respectively limit and delay a mission. Much research has focused on increasing data throughput over the lifespan of an operational CubeSat in orbit. Low earth orbit (LEO) CubeSats have popularly been using data rates typically around 9.6 kbps for uplink and sub 3 Mbps for downlink applications. However, this cannot keep up with the growing demand of new technologies. The trend nowadays is achieving high speed communication links. Thus, commercial applications favour frequencies above S-band (2.4 – 2.450 GHz), which will support high data rate downlinks in the order of about 3 Mbps – 1.7 Gbps. The congestion in the popular very high frequency (VHF: 144 – 146 MHz), ultra-high frequency (UHF: 435 – 438 MHz) and S-band frequencies for radio communications, require a shift to higher frequencies where more bandwidth is available, and there is less interference from other spectrum users when receiving weak signals. This research implements a C-band (4 – 8 GHz) downconverter for a CubeSat based receiver system. The goal of this study is to look at the usage of higher frequency bands that address the need for systems, which require high data rate. The research began with the literature study from which a research gap was identified, then a simplistic design workflow was implemented, followed by testing and validation of the downconverter system for a CubeSat receiver operating from 5.650 – 5.670 GHz. A system level approach using commercial-off-the-shelf components (COTS) was used to reduce development time and cost. To do this, each subsystem was implemented and tested individually before system level integration. The following performance parameters were validated: an input C-band frequency from 5.650 – 5.670 GHz with a center frequency of 5.66 GHz, an overall conversion gain of 40.205 dB, a noise figure less than 2.3 dB, a phase locked loop (PLL) based local oscillator frequency from 4.385 – 4.405 GHz, an output power of 4.52 dBm, a spurious response of -81.96 dBc/Hz, an out-band phase noise of -111 dBc/Hz at 1 MHz carrier frequency offset from a 4.395 GHz PLL carrier frequency and the output L-band frequency from 1.250 – 1.270 GHz at a center frequency of 1.268 GHz.

Key words: spaceborne receiver, CubeSat, system level, COTS, gain, noise figure, C-band, L-band, LNA, bandpass filter, mixer, PLL oscillator

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DEDICATION

This work is dedicated to my dearest mother Mrs Saara Tuyeimo Valombweleni, my husband Mr Paulus Vatileni Kateya, my son Emmanuel Nyanyukweni Kateya, my siblings and my entire family. I thank you all for the continued moral support, love, patience, courage, and prayers rendered during my studies.

I have done this work in loving memory of my beloved father Tate Leopold Valombweleni (1956 - 2014). You are dearly missed.

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GLOSSARY

Terms/Acronyms/Abbreviations	Definition/Explanation
ADS	Advanced Design System
AFSK	Audio Frequency Shift Keying
AX.25	A data link layer protocol for radio amateurs
BAT	Battery
BPF	Band Pass Filter
Bps	Bits Per Second
CAD	Computer Aided Design
C-band	Frequency range from 4 - 8 GHz
CPUT	Cape Peninsula University of Technology
CW	Continuous Wave
COTS	Commercial-Off-The-Shelf
dB	Decibels
dBc	Signal strength relative to carrier in decibel
dBi	Antenna gain relative to an isotropic radiator in decibel
DDC	Digital down converter
DRO	Dielectric Resonator Oscillator
EPS	Electrical Power System
F	Noise Factor
F'SATI	French South African Institute of Technology
GMSK	Gaussian Minimum Shift Keying
GS	Ground Station
HPF	High Pass Filter
IF	Intermediate Frequency
IP	Intermodulation Products
IP3	3rd Order Intercept Point
I^2C	Inter-Integrated Circuit
IARU	International Amateur Radio Union
ITU	International Telecommunications Union
K-band	Frequency range from 18 - 27 GHz
Ka-band	Frequency range from 27 - 40 GHz
Ku-band	Frequency range from 12 - 18 GHz
kB	kilobyte
kbps	kilobit per second
LEO	Low Earth Orbit
LO	Local Oscillator
LNA	Low Noise Amplifier
LNB	Low Noise Block
LPF	Low Pass Filter

Terms/Acronyms/Abbreviations	Definition/Explanation
MAG	Maximum Available Gain
MB	Megabyte
Mbps	Megabit per second
MMIC	Monolithic Microwave Integrated Circuit
NF	Noise Figure
NIR	Near Infrared
OBC	Onboard Computer
*P*1dB	1 dB Compression Point
PCB	Printed Circuit Board
PD	Phase Detector
PFD	Phase Frequency Detector
PLL	Phase Locked Loop
ppm	parts per million
P-POD	Poly Picosat Orbital Deployer
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
Rx	Receiver
SAW	Surface Acoustic Wave
SDR	Software Defined Radio
SMT	Surface Mount
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
Sps	Samples per second
TCMD	Telecommand
TLM	Telemetry
TT&C	Telecommand, Telemetry and Control
TRF	Tuned Radio Frequency
Tx	Transmitter
UHF	Ultra High Frequency
V-band	Frequency range from 40 - 75 GHz
VCO	Voltage Controlled Oscillator
VHF	Very High Frequency
VSWR	Voltage Standing Wave Ratio
X-band	Frequency range from 8 - 12 GHz

CHAPTER ONE : INTRODUCTION

1.1. Research Overview

The French South African Institute of Technology (F'SATI) and the Africa Space Innovation Centre (ASIC) at the Cape Peninsula University of Technology (CPUT) are commercialising in-house developed satellite communication subsystems compatible with the CubeSat standard spanning in the very high frequency (VHF), ultra-high frequency (UHF), S-band and recently X-band frequencies. Therefore, there is a need for F'SATI to develop future CubeSat communication subsystem products at C-band and higher frequency bands to facilitate more bandwidth for the upcoming nanosatellite missions (van Zyl et al., 2013). As a result, this thesis focuses on a spaceborne single stage C-band downconverter system depicted in Figure1.1 that has been developed at CPUT for future nanosatellites receiver front-end applications. The downconverter system will receive radio frequency (RF) signals at C-band (5.65 − 5.67 GHz), condition them using filters and amplifiers in this signal chain, and downconvert them to a lower intermediate frequency (IF) or IF signal at L-Band (1.265 − 1.27 GHz) for further processing and data recovery. Down conversion is achieved by mixing the incoming RF signal with a stable carrier signal generated from a phased locked loop (PLL) based local oscillator (LO), in this case operating from 4.385 − 4.405 GHz. The PLL provides a stable and low phase noise LO signal operating from 4.385 − 4.405 GHz, with output power levels adequate to drive the mixer. This thesis is organized as follows: A brief theory of the downconverter is reviewed, followed by the downconverter parameters/specifications, then the downconverter design, the simulations and implementation, the results, and the results interpretation, as well as the validations and finally concluding remarks are drawn and some recommendations are made for further studies.

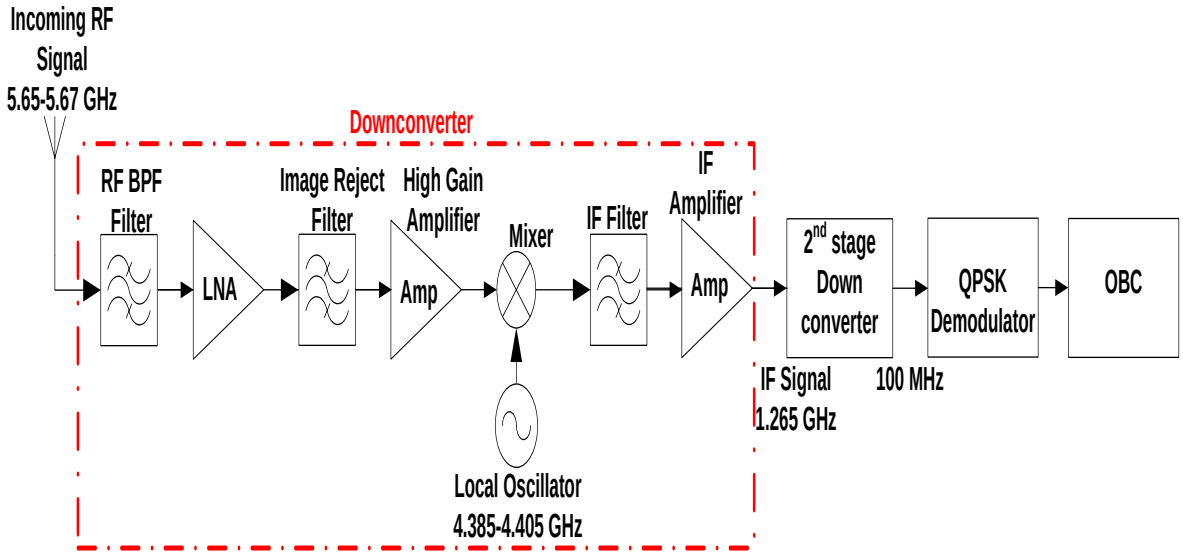


Figure 1.1: Downconverter system block diagram (adapted from Leopold et al, 2022)

1.2. Research Problem Background

Nanosatellites categorised in Figure 1.2, have gained popularity in the past two decades with the introduction of the CubeSat standard[1]. The CubeSat standard formally resulted from a collaboration between Prof. Jordi Puing-Suari from California Polytechnic State University (Cal Poly) and Prof. Bob Twiggs from Stanford University in 1999, primarily as an educational platform providing university students hands-on experience in building, launching and operating a CubeSat.

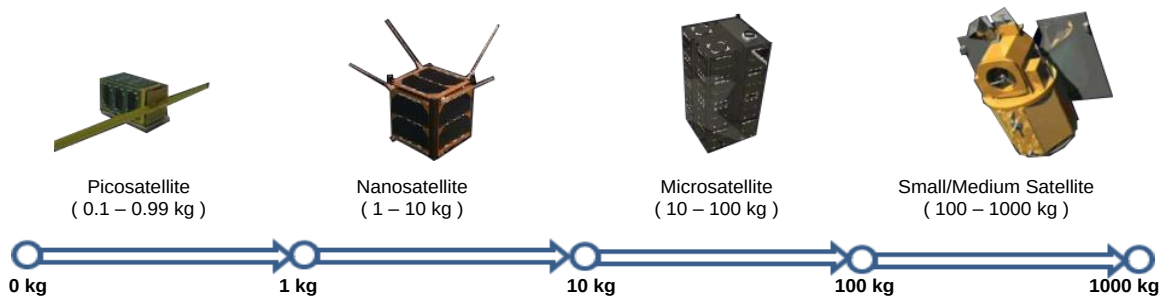


Figure 1.2: Satellite categories (Space Works, 2018:5)

The CubeSat standard specifies a 10 cm cube, popularly known as a one unit (1U) CubeSat to weigh approximately 1 kg. 1U is defined as a volume of approximately 10 cm x 10 cm x 10 cm. This form factor can be scaled to a stack of double or triple1U's, referred to as 2U and 3U (most predominant) CubeSats respectively. Applications trends towards 6U, 12U and 16 U in the near future (Puig-Suari *et al*., 2001:1). Table 1.1 indicates that the 1U can be scalable to a larger volume and mass constraints.

Table 1.1: Variations on the CubeSat standard regarding size and mass (adapted from Mabrouk, 2017)

CubeSat Designation	Size (max)	Mass (max)
Cube (1U)	10 cm x 10 cm x 10 cm	1 kg
Double Cube (2U)	10 cm x 10 cm x 20 cm	2 kg
Triple Cube (3U)	10 cm x 10 cm x 30 cm	3 kg
6 Pack (6U)	10 cm x 20 cm x 30 cm	6 kg

Figure 1.3 illustrates standardised modular CubeSats configuration in units. The modular and standardised format of CubeSats enables re-use of COTS hardware, modular and terrestrial components and subsystems, re-use of software designs, quick assembly, integration and testing schedules, simple launch interfacing, saving cost and reducing long-term risks.

[1] https://www.cubesat.org/s/CDS-REV14_1-2022-02-09.pdf

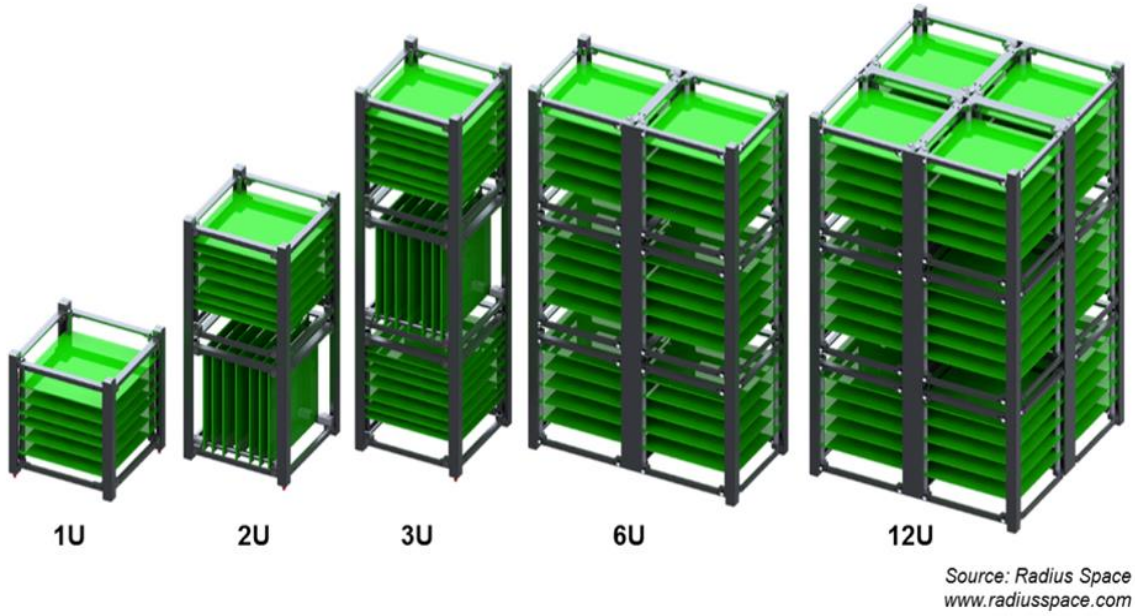


Figure 1.3: CubeSats modular standard structures (Radius Space, 2017)

When compared to traditional satellites, CubeSats platform offer a low-cost access to space for academic institutions, private companies, and government entities to develop and deliver space mission within a short period of time. However, the CubeSat platform has its own limitations, which include size, power, and mass. A compromised has to be made between these limitations and the system performance to achieve the desired mission objectives. However, advances in secondary/shared launch opportunities, such as recently from the International Space Station (ISS), readily available commercial-off-the-shelf (COTS) components and subsystems, unlicensed radio bands, amateur frequency allocation, integration and miniaturization technologies have diminished the trade-off between these constraints (National Academies of Sciences, Engineering, and Medicine, 2016).

As the CubeSat phenomena advanced, various applications in government, private, research and education entities around the world have increased, resulting in a limited spectrum for amateur radio/ university satellite operations. According to National Academies of Sciences, Engineering, and Medicine (2016), merely 5 MHz of bandwidth is available in the most popular bands. Figure 1.4 shows high usage of VHF, UHF and S-band frequencies for radio communications and less usage of frequencies from C-band and above. CubeSat developers still favour lower frequencies because of cheaper and readily available components even though they are the most congested. Higher frequencies are associated with high cost and design complexity. High frequency bands allow the use of wider bandwidth and the interference from adjacent channels is also minimal.

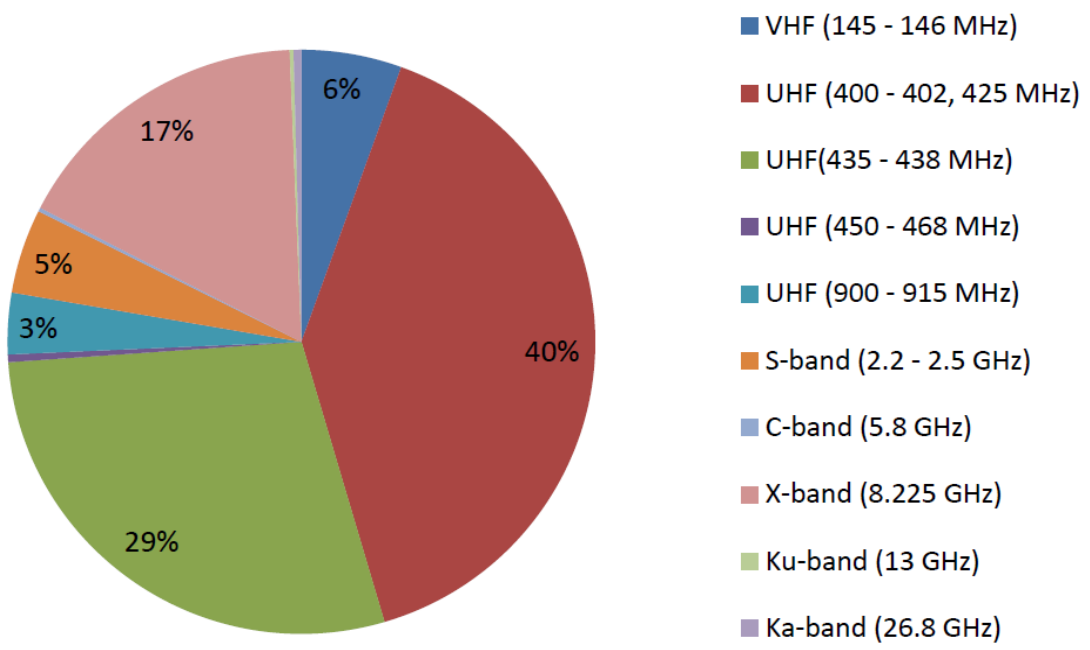


Figure 1.4: Trend in CubeSats frequency bands (Maheshwarappa, 2016)

Figure 1.5 shows a growing market interest in CubeSat missions around the world, especially in the commercial sector for various space applications. The sudden rise of CubeSat launches in recent years is from missions launched by participating organisations across the space sector, including education, commercial services, and technology demonstration. Key industry players include but not limited to; National Aeronautics and Space Administration (NASA)[2], Planet Labs—which is a commercial entity aimed at building and launching a constellation of several hundred 3U imaging CubeSats covering the entire surface of the Earth every day[3] and lately Space X's Starlink—which is the world leading constellation of small satellites aimed at providing high-speed, low latency broadband internet across the globe[4]. In recent years, there have been a growing number of commercial organisations exploring new business models using the CubeSat platform. Future growth is predicted as a result of more participation from the commercial sector as technology advances. Consequently, more bandwidth requirements and associated regulatory challenges have increased (SpaceWorks, 2020).

[2] https://www.nasa.gov/mission_pages/smallsats
[3] https://www.planet.com/
[4] https://www.starlink.com/technology

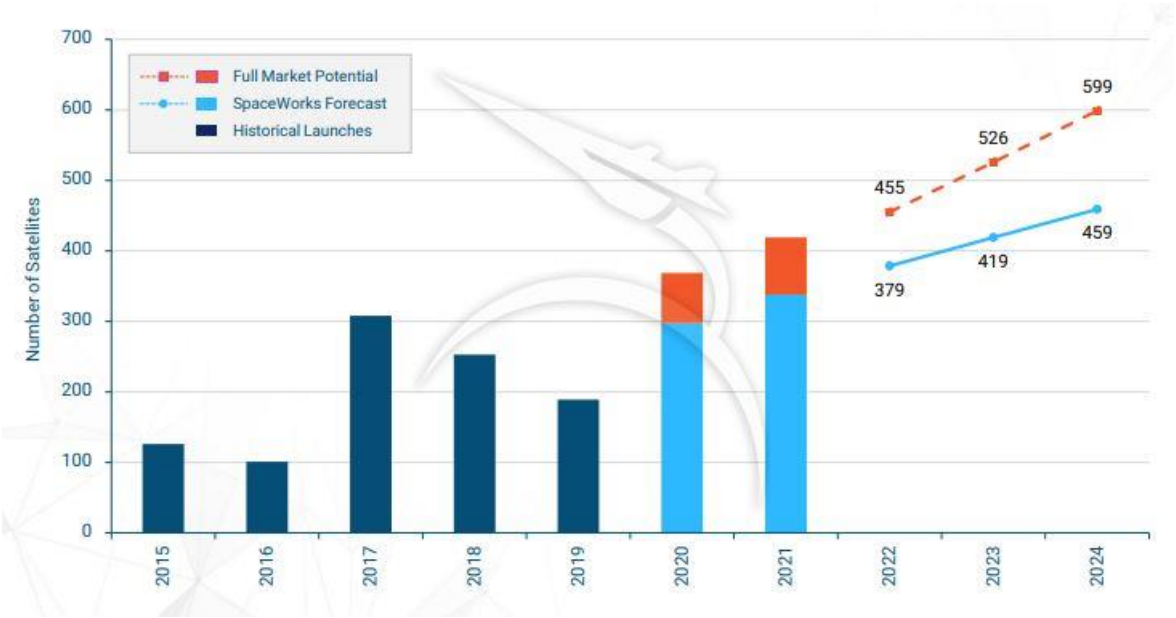


Figure 1.5: Growing interest in CubeSats (Space Works, 2020)

F'SATI at CPUT in Cape Town, South Africa, is actively participating in the nanosatellites industry. Figure 1.6 gives a brief overview of the F'SATI CubeSat program since its inception, and past establishments. The highlight is in 2013 after successfully developing, launching, and operating South Africa's first 1U CubeSat Zacube-1 (TshepisoSat) in collaboration with the South African Space Agency (SANSA). ZACUBE-1 depicted in Figure 1.7 was primarily aimed at human capacity development, ionospheric propagation studies, and technology demonstration (van Zyl et al., 2013:52).

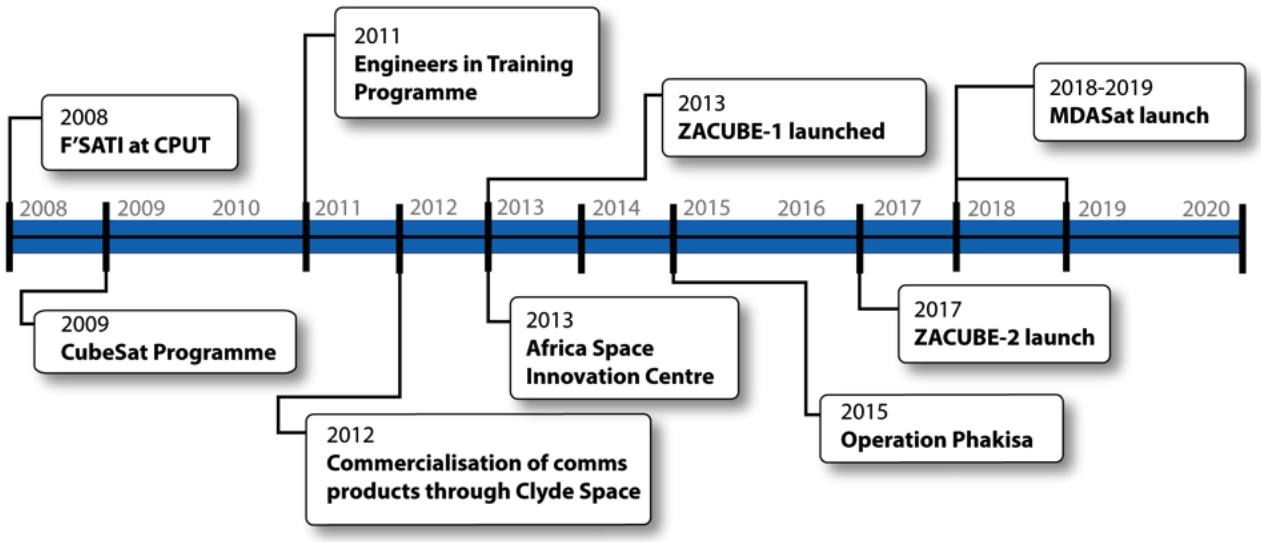


Figure 1.6: F'SATI roadmap (van Zyl, 2017)

F'SATI in collaboration with SANSA developed a follow-up mission to ZACUBE-1, ZACUBE-2—a 3U CubeSat depicted in Figure 1.7. According to de Villiers & van Zyl, ZACUBE-2 is aimed at demonstrating a software-defined radio (SDR) as a primary payload, and a medium resolution near infrared (NIR) imager as the secondary payload.

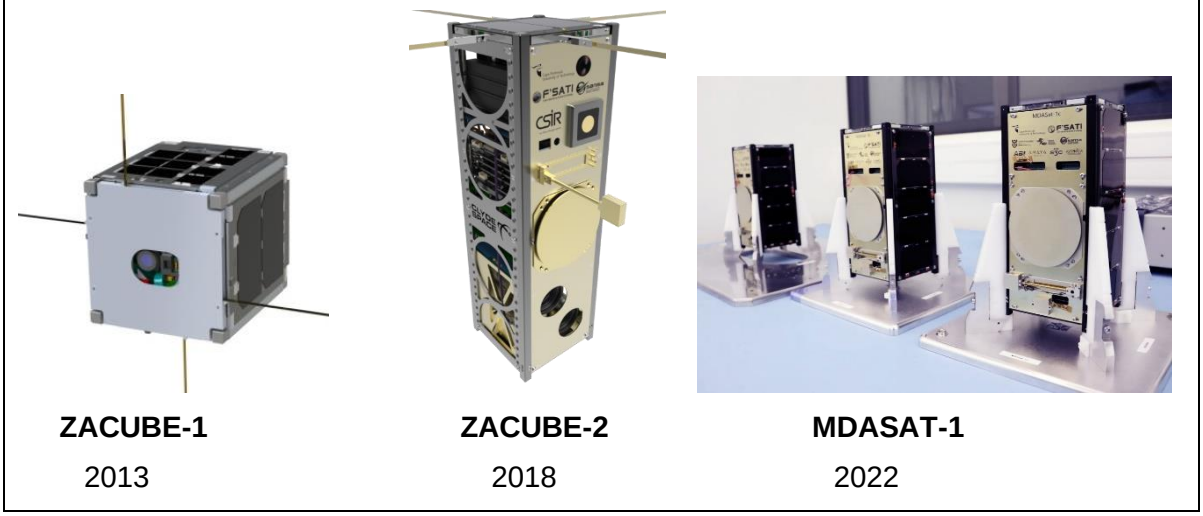


Figure 1.7: F'SATI CubeSat missions (F'SATI, 2023)

The trend in SDR platforms save time and cost for upgrading infrastructure with more flexible hardware, hence it was adapted for the ZACUBE-2 mission. This technology enables reconfiguration and software updates of the primary payload while in orbit. The mission objective was to provide vessels automatic identification system (AIS) and VHF data exchange service (VDES) data, from a constellation of 3 (2U) Maritime Domain Awareness nanosatellites, named, MDASat-1, to monitor South African maritime activities. ZACUBE-2 was a precursor to the MDASat-1 constellation mission launched on 13 January 2022 (Royi, 2022). In light of all these, there was a need for F'SATI to develop future CubeSat communication products at C-band and higher frequency bands to facilitate more bandwidth for upcoming CubeSats missions and commercialisation (van Zyl et al., 2013). Figure 1.8. shows CubeSat COTS products developed by CPUT's F'SATI/ASIC and previously distributed by Clyde Space in the UK. These included but not limited to; S-band transmitter, VHF/UHF transceiver, S-band patch antenna and X-band transmitter[5].

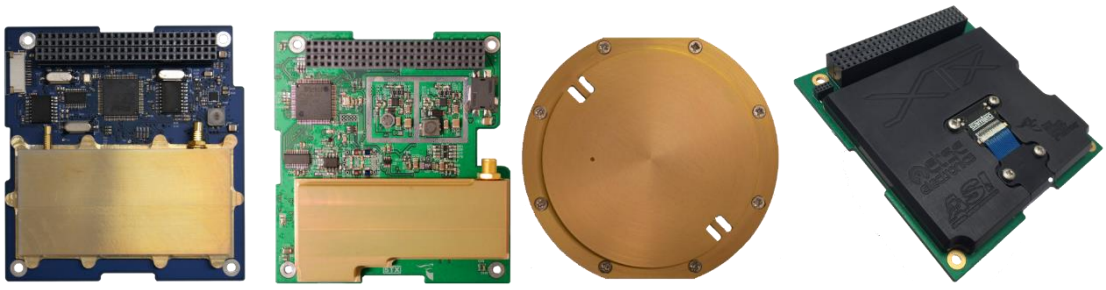


Figure 1.8: Commercial CubeSat communication radio products developed by F'SATI (Clyde Space, 2014)

[5] https://blogs.cput.ac.za/fsati/products/

1.3. Research Problem Statement

Most CubeSats are launched into low earth orbit (LEO) at an altitude of about 600 km. LEO enables the CubeSats to orbit Earth 15 times a day and to use RF links for communication with ground stations. The growing interest for the use of nanosatellite to perform space missions have resulted in congestion in the amateur frequency bands and the novel technology require systems with higher data rates. This necessitates a shift to higher frequency for lower percentage bandwidth usage. A CubeSat needs to transfer onboard mission data to the ground station during this limited time, hence a downconverter with higher data rate is required, which is the basis of the research.

1.4. Research Objectives

The scientific objective of any CubeSat communication subsystem is high data rate, small size, light weight, low power consumption, mechanically rigid, thermally stable, low electromagnetic interference (EMI) and radio frequency interference (RFI) (Klofas *et al*., 2008). The goal of this thesis lies in the design and implementation of the C-band to L-band amateur downconverter in a CubeSat communications receiver subsystem. The downconverter follows a system level approach by making use of COTS that can meet suitable specifications and survive the environmental conditions of a CubeSat in orbit. The downconverter should conform to the specifications listed in Table 1.2.

Table 1.2: C-band downconverter preliminary specifications (F'SATI, 2013)

Parameter	Specified
Downconverter frequency range	5650 – 5670 MHz (center freq. = 5660 MHz)
IF range	1250 – 1270 MHz (center freq. = 1260 MHz)
Local Oscillator (LO) frequency range	4390 – 4410 MHz (center freq. = 4400 MHz)
DC power supply voltage	6 – 15 V
Power consumption	<0.25 W
Gain	25 dB
Noise Figure	<4 dB
Sensitivity	-112 dBm
Bandwidth	20 MHz
Modulation	QPSK
Spurious Frequencies	Better than -70 dBc
Operating temperature	-45 ºC to 85 ºC

1.5. Research Investigative Questions

The questions used during the development process of the downconverter are as follows;

- What C-band frequencies are usable for CubeSats?
- What is the suitable receiver architecture to implement the downconverter?
- What available COTS components will be suitable for the chosen architecture?
- How would the different subsystems integrate and on which substrate for the final solution?
- How will this integration affect the overall downconverter system performance?

1.6. Research Outcome / Impact / Scientific Contributions

The physical outcome of this research is a prototype C-band to L-band downconverter for high data rate uplink communications, which conforms to initial specification and performance parameters listed in Table 1.2. The downconverter will form part of F'SATI CubeSat communication suite of products used both as part of the CubeSat platform and/or the ground station equipment to receive and condition future C-band transmitted signals. The CubeSat industry is growing at a fast rate worldwide; thus, the impact of this research will broaden the scope of CubeSat communications systems available worldwide which will in turn serve as an enabling technology for advancements in other subsystems and CubeSats missions as a whole. The research scientific contributions include the final thesis documentation, a published conference paper, an accepted conference paper and a submitted journal article that is currently under third round of peer review; as indicated below.

1. Leopold, L. N., Bayendang, N. P., and Balyan, V. 2022. "Analysis, Design and Implementation of a PLL Synthesizer for a C-Band to L-Band Downconverter for a CubeSat Receiver System," *2022 International Conference on Electrical, Computer, Communications and Mechatronics Engineering (ICECCME)*, Maldives, Maldives, 2022, pp. 1-6, doi: https://doi.org/10.1109/ICECCME55909.2022.9988086.

2. Leopold, L. N., Bayendang, N. P., and Balyan, V. 2023. "A Nanosatellite Receiver Downconverter C-band to L-band Bandpass Filters—Review and Design", *International Conference on Electrical, Computer and Energy Technologies (ICECET 2023) 16-17 November 2023, Cape Town-South Africa*. pp. 1-7, doi: 10.1109/ICECET58911.2023.10389197..

3. Leopold, L. N., Bayendang, N. P., and Balyan, V. 2023. "A CubeSat Receiver Subsystem C-Band to L-Band Downconverter: Analysis, Design and Implementation. Submitted to Elsevier's Expert Systems With Applications Journal. Manuscript ID: ESWA-D-23-14320 (under peer review).

1.7. Research Delineation

- This research does not cover component level designs of individual subsystems but focus on system level implementation.
- This research only looked at the uplink CubeSat receiver and not the downlink ground station receiver, although the CubeSat receiver can also be used in the ground station receiver and not necessarily vice versa.
- The number of down conversion stages is restricted to one (from C-band to L-band), based on complexity, cost and time constraints associated with high frequencies.
- Antenna design and digital signal processing as part of every RF receiver, are out of scope of this research. Therefore, only topics relating to the downconverter are discussed.
- Spaceborne validation tests are not conducted due to lack of resources.

1.8. Research Methodology

The following methods of investigation are followed to achieve the research objectives:

- Conducting a literature review through consultation of relevant research materials to have a broad understanding of the research field.
- Obtaining suitable specifications for the receiver and designing a concept for the front-end and downconverter.
- Trade studies to motivate a chosen configuration.
- Comparing various off-the-shelf modules that are available in terms of power consumption, size, reliability and performance.
- Simulations of various downconverter subsystems.
- Building and testing a prototype to verify initial specifications.
- Evaluation and validation of results.
- Conclusions and recommendations.

1.9. Summary

This work began by introducing CubeSats and why it's important. From which it was opined that advances in CubeSats require a receiver downconverter with high data rate. As a result, a C-band to L-band downconverter is researched, designed and implemented as follows:

- Chapter 1 gives a general introduction and overview of what the study is about.
- Chapter 2 reviews the literature supporting the research.
- Chapter 3 details the design specifications, and methodology used in designing the subsystems that constitute the downconverter and as well presents simulations of the downconverter.
- Chapter 4 details the construction and measurements of the downconverter.
- Chapter 5 concludes the study, summarises key findings and gives recommendations for future research.

CHAPTER TWO : LITERATURE REVIEW

2.1 Introduction

This Chapter reviews the literature supporting the research. A brief theory of CubeSat communication receiver systems, spaceborne downconverters and downconverter parameters / specifications are examined to identify the research gap. Special focus is on the frequency spectrum allocations, receiver architectures and receiver system-level design considerations / trade-offs. The comprehensive list of applicable past studies reviewed, and their highlights are presented herein.

2.2 CubeSat System Architecture

Innovation and technology advancements of the nanosatellite communication subsystem has increased tremendously since the beginning of the CubeSat standard in the late 1990s. The communication module is essential in the establishment of a reliable communication link between CubeSats in orbit and the ground station/s. This includes telemetry, tracking and command (TT&C), data acquisition and uploads. Figure 2.1 depicts the basic elements of a CubeSat communication system.

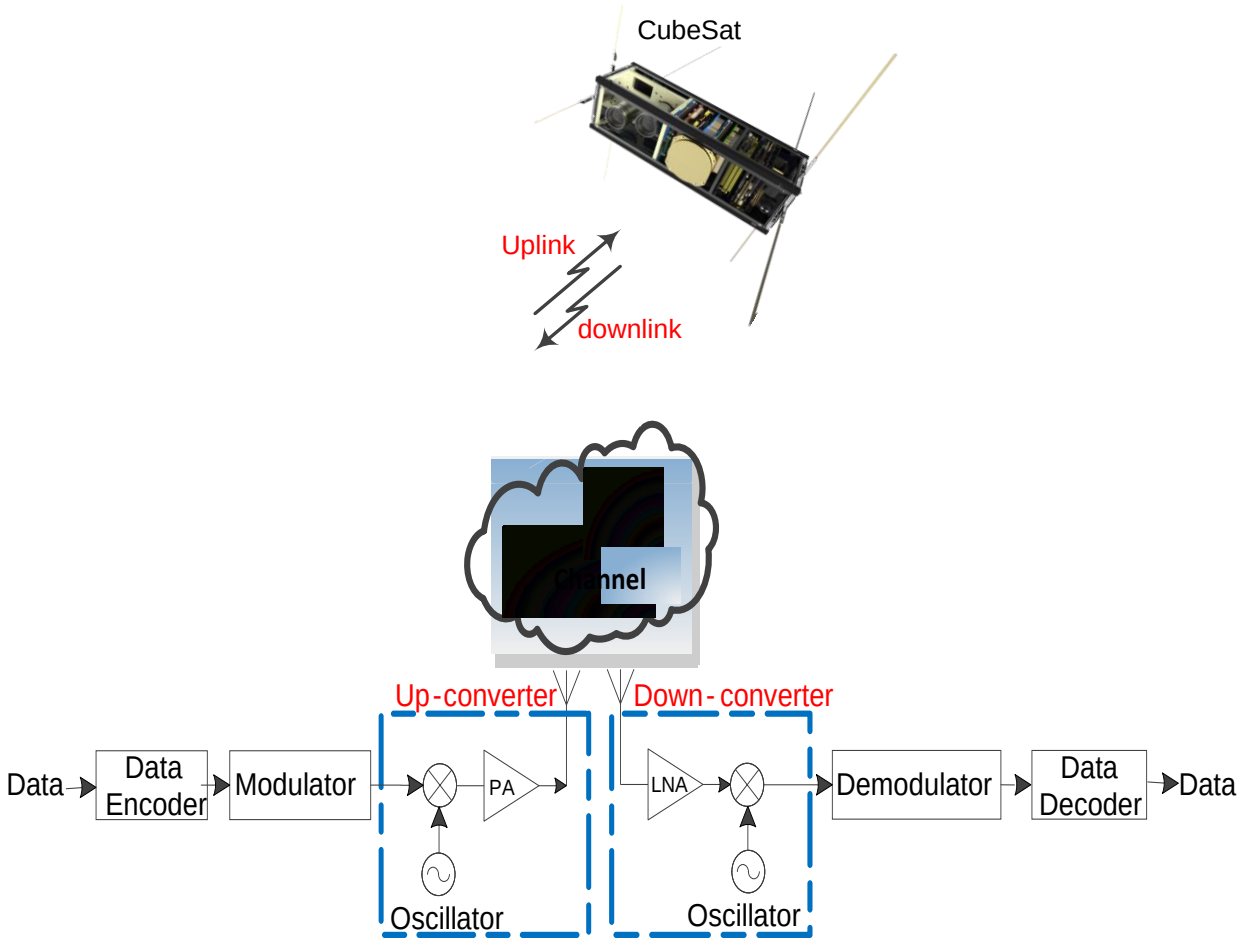


Figure 2.1: The satellite communication system (adapted from Maral & Bousquet, 1999:3)

With reference to Figure 2.1, the space segment represents the CubeSat in orbit, and the ground segment consists of at least one TT&C ground station to command the satellite and receive data. When the transmitter on the ground sends a signal (telecommand data) via an antenna, and through the communication channel, to the satellite's antenna, it is referred to as the uplink. The signal is then handled within the satellite and transmitted back to the ground station as telemetry data, and this is called the downlink (Ippolito, 2008). The downconverter as a front-end of the receiver communication subsystem highlighted in Figure 2.1, is the focus of this research. It is made up of various RF modules to amplify, filter and isolate signals of interest. In this context, the downconverter is essential for receiving, conditioning, and translating the received high radio frequency (RF) signal to a lower intermediate frequency (IF) signal for further processing and recovering of the original data. The incoming RF signal is mixed down to the IF signal, with a carrier signal generated from a stable local oscillator (LO).

The standard CubeSat hardware is categorized in different subsystems that make up the CubeSat; namely the power (EPS), communication (transceiver) which assist in the transmitting and receiving of data to and from the ground station, an on-board computer (OBC) which controls the entire CubeSat and an attitude determination & control system (ADCS) that maintains CubeSat stabilization and orientation of the desired direction and position as well to enable the camera to take images at a certain position and location (Gildeh, 2003). Figure 2.2 shows a typical internal architecture for ZACUBE-2 3U CubeSat (van Zyl *et al*., 2013). The main focus area of this research is the communication subsystem of the CubeSat, specifically the downconverter subsystem for nanosatellites receiver applications at amateur C-band which forms part of the transceiver.

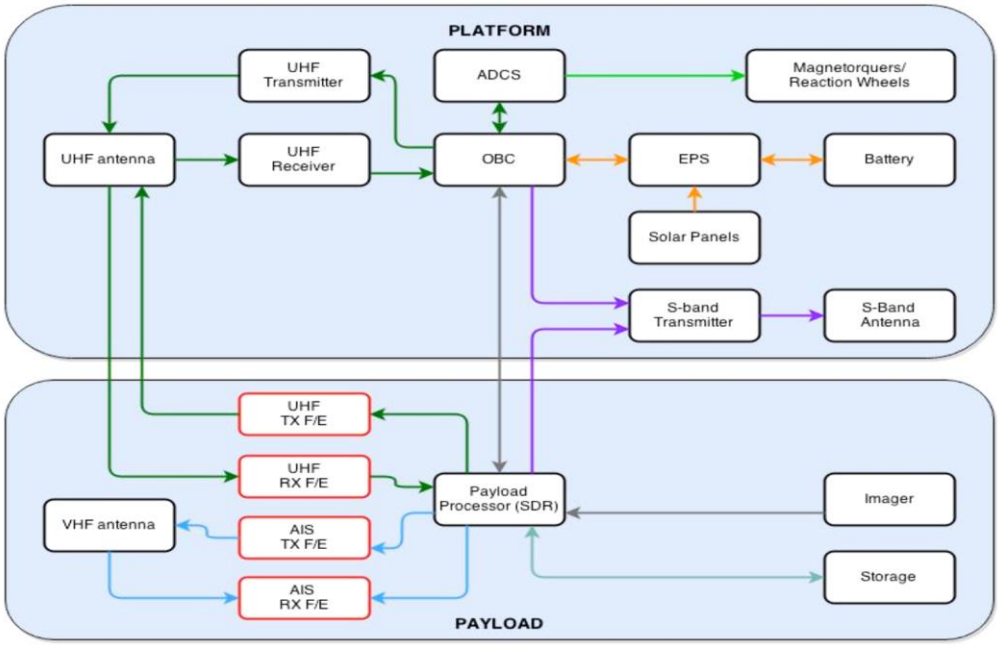


Figure 2.2: ZACUBE-2 internal architecture (adapted from de Villiers & van Zyl, 2016)

2.3 Radio Frequency Communication System

The basic blocks of a radio communication system shown in Figure 2.3, consists of an information source, a transmitter, a transmission medium, a receiver and an information destination. The transmitter superimposes the low frequency information signal onto a high frequency carrier signal, to form a modulated signal suitable for transmission over the communication channel. According to McPherson & Whaits (2007:1.14), this is the process of modulation. The communication channel is a propagation medium for the electromagnetic wave with added noise, responsible for the connection between the transmitter and the receiver. The receiver, which is the focus of this research, is responsible for reproducing the original message being transmitted over the channel, through signal processing techniques such as demodulation.

The performance of RF communication systems is determined by how much the output signal differs from the input signal. These variations occur during the process of information transfer, whereby the transmitted signal is susceptible to noise and interference. Noise effects are detrimental and to an extent, can lead to total loss of the transmitted information.

Electrical noise is any form of random signal that tends to interfere with the reception and reproduction of the desired signal. Noise originates from external sources and can also be generated internally. In a satellite communication system, external noise enters through the antenna and is generally caused by extra-terrestrial sources such as thermal radiation from the Sun and atmospheric noise. Internally generated noise is caused by thermal energy produced when there is a flow of current in the circuitry (resistive material) and is the major contributor to the total noise of the system. Noise can be minimized by carefully designing the RF system (MacPherson, 2002).

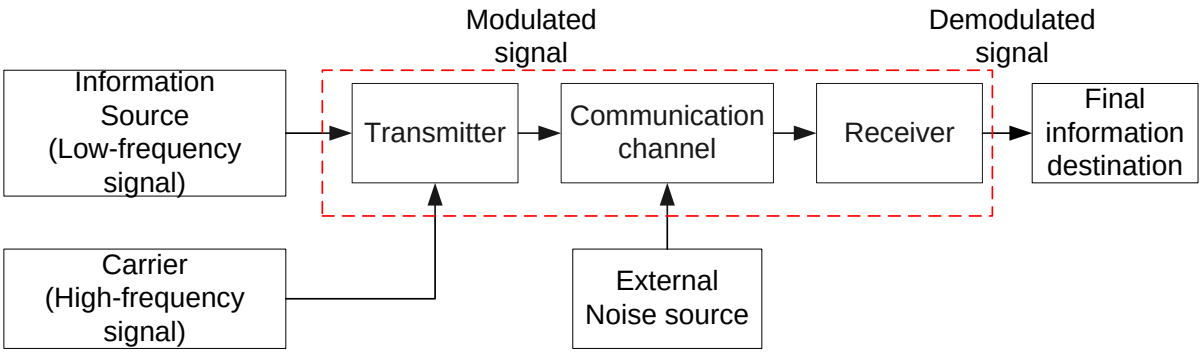


Figure 2.3: Basic block diagram of a radio communication system (adapted from McPherson & Whaits, 2007)

Figure 2.4: shows concepts of radio waves and an overview of how to add information (0- or 1-bit pattern) on RF signal. A pure RF signal which include no data is called a carrier. A sent or received digital data (e.g. text format “hello word”), is called a baseband—which is generally

the zero over one-bit pattern sent or converted from the original digital data. There are four major ways to achieve modulating the baseband unto the carrier. The first approach is ON or OFF of the carrier signal transmission, this is called continuous wave (CW). If the ON state of the carrier signal is defined as equal to 1, the OFF state is 0. The baseband is from the ON and OFF pattern. However, if the OFF state of the carrier corresponds to zero, if it's not possible to discriminate if it's a meaningful zero or not being able to receive the carrier, therefore it is best to define three states bar (-), dot (.) and space ()—this is referred to as Morse code. In the case of Morse code transmission, the length of bar is defined as three times the length of dot. This approach is basic, legacy but robust and requires no modulation.

The second approach is the amplitude change of the carrier signal, during which if the large amplitude state of the carrier signal is defined as 1, the small amplitude state is 0. The baseband is from the amplitude changing pattern. The third approach is a frequency change of the carrier signal, whereby if the higher frequency of the carrier signal is defined as 1, the lower frequency state is 0. The baseband pattern is from the frequency changing pattern. The fourth approach is the phase change, in which if the zero degree start state of the carrier signal is defined as 1, the 180 degree start case is 0. The baseband is from the phase changing pattern (KiboCube Academy, 2022).

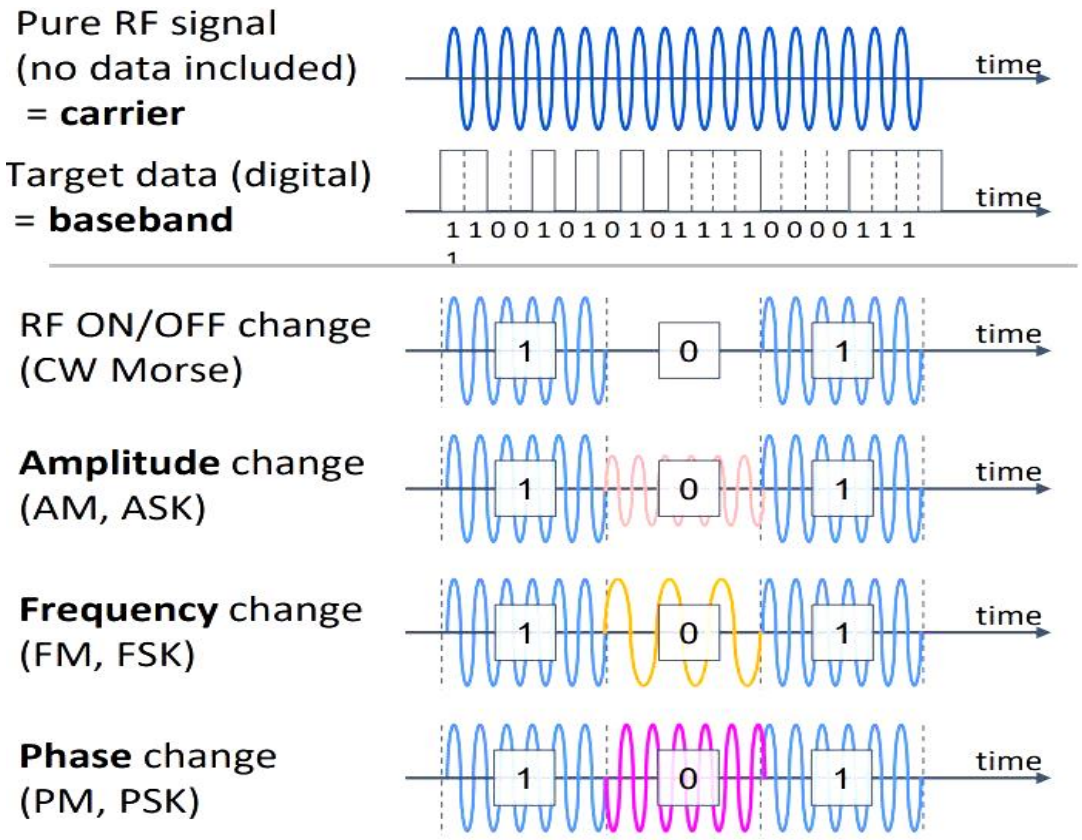


Figure 2.4: Modulation schemes (adapted from KiboCube Academy, 2022)

Communication rate or data rate, refers to the rate at which bits (0s and 1s) are transmitted through a communication system. It is measured in bits-per-second (bps). Higher data rate allows more information to be transmitted in a given time. In a digital communication system, bits are often grouped into symbols before transmission into a communication medium to make a system bandwidth efficient. The relationship between data rate (R_d) and symbol rate (R_s) is represented by Equation 2-1.

$$R_d = R_s 3.32 log_{10}(M)\ bps \qquad 2\text{-}1$$

Where, $M = 2^n$, and n = bits per symbol

The modulation scheme determines the number of bits represented by each symbol. for instance, to achieve a data rate of 9600 bps, the symbol rate should be 4800 sps and each symbol represents 2 bits.

Key points of information transfer are amplitude, frequency, and phase of a carrier signal. Superimposing of the carrier and baseband signals, in other words, data conversion from digital to analog signal, is called modulation and the reverse process is called demodulation. Table 2.1 shows the major terms of modulation methods. To send digital data packets, FM + FSK or audio frequency shift keying (AFSK) is the most popular way for university CubeSat missions to communicate digital data—which is based on the AX.25 amateur radio protocol. The bit rate is 1200 bps in nominal usage. In the case of GMSK, the bit rate is 9600 bps or higher speed. Signal processing integrated circuits (IC) can be investigated to realise these functionalities. To achieve higher communication bit-rate, advanced modulation methods like QPSK or GMSK must be considered. QPSK modulation scheme is specified for the CubeSat C-band receiver in this research.

Table 2.1: Modulation methods

Modulation scheme	Description
AM	Amplitude Modulation
FM	Frequency Modulation
PM	Phase Modulation
PQM	Phase Quadrature Modulation
PCM	Pulsed-Code Modulation
PPM	Pulse Position Modulation
ASK	Amplitude Shift Keying
FSK	Frequency Shift Keying
PSK	Phase Shift Keying
BPSK	Bi-Phase Shift Keying
QPSK	Quadrature Phase Shift Keying
GMSK	Gaussian Minimum Shift Keying

2.4 CubeSat Frequency Allocation and Regulations

Many CubeSat missions typically use amateur radio frequency bands due to easily accessible COTS and inexpensive terrestrial hardware, and licence availability (Klofas & Leveque, 2012). Table 2.2 lists uplink frequency bands allocated for CubeSat operations by the International Amateur Radio Union (IARU). Figure 2.5 shows the allocation of frequency bands coordinated by the member countries of the IARU and these are[6]:

- IARU Region 1 includes: Europe, Africa, Middle East and Northern Asia
- IARU Region 2 includes: The Americas (North, Central & South)
- IARU Region 3 includes: Asia-Pacific

Table 2.2: IARU frequency allocation for amateur satellite services (adapted from IARU, 2020)

Band	Uplink Frequency (MHz)
VHF	144 - 146
UHF	435 - 438
L-band	1260 - 1270
S-band	2400 - 2450
C-band (1)	3400 - 3410
C-band (2)	5650 - 5670

Figure 2.5: 04-AM-ART5 Services and frequency bands for small satellites (adapted from IARU, 2020)

[6] https://www.iaru.org/about-us/organisation-and-history/regions/

When designing a wireless RF system, all radiating devices must adhere to their portion of the frequency allocation table, as well as power levels and bandwidth allocations. The IARU bands in the 5.65 - 5.67 GHz and 1.26 - 1.27 GHz assigned for Earth to space communication in the C-band and L-band, respectively, was specified for the implementation of the C-band to L-band down converter (IARU, 2006:20).

2.5 System Level Considerations

When designing a radio communication system, the designer should take into account the following system level considerations.

2.5.1 Link Budget

The link budget looks at the elements that will determine the signal strength arriving at the receiver. Figure 2.6 depicts a typical satellite trajectory, relative to the Earth, upon which a link budget is based.

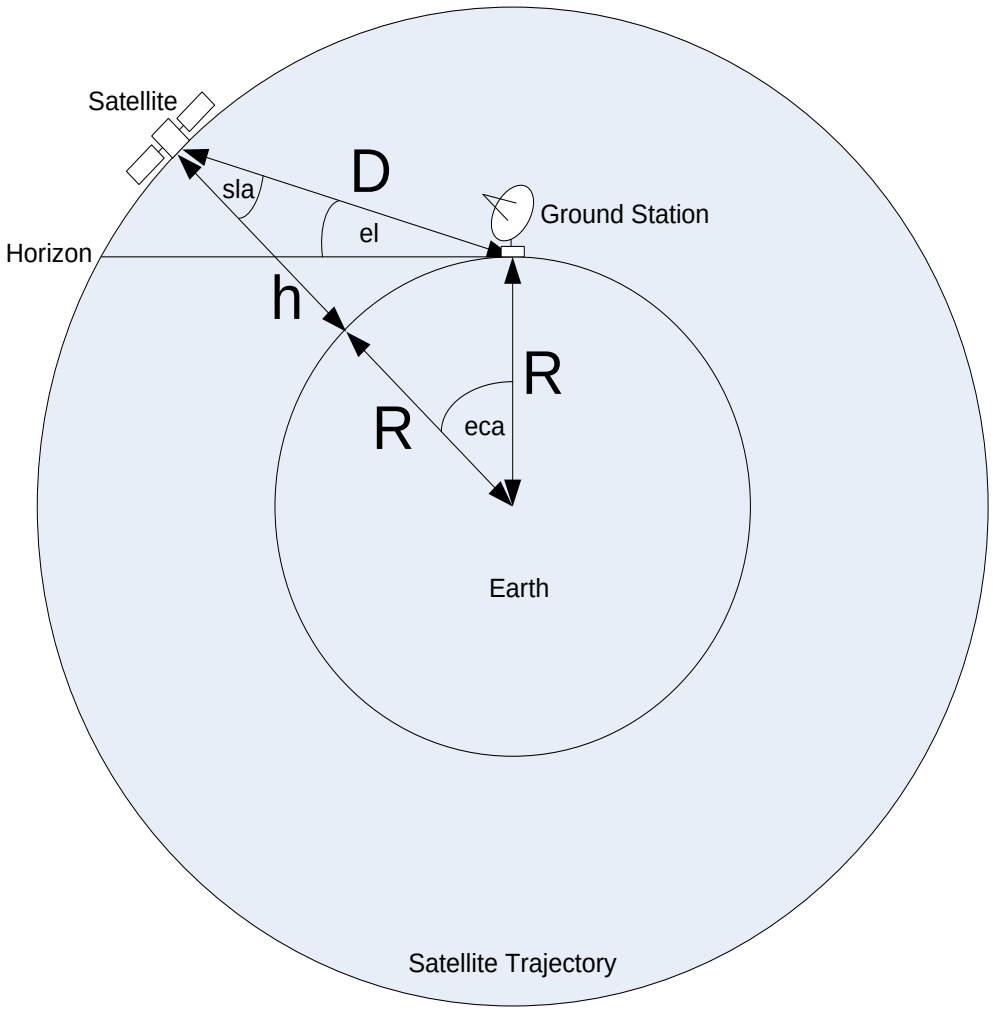


Figure 2.6: Satellite trajectory relative to the earth (F'SATI, n.d.)

The signal strength weakens as the distance between the transmitter and the receiver increases. This can be mathematically verified using Friss's transmission Equation 2-2. From Equation 2-2, it can be seen that the received power is proportional to the square of the distance (D^2) and this means that the furthest away the receiver is from the transmitter, the weaker the signal will be. To implement a receiver that will operate according to the given specifications, a link budget is necessary to analyse the signal levels throughout the downconverter chain. A link budget involves relatively simple addition and subtraction of gains and losses within a RF link. When the gains and losses of various components are determined and summed (in units of dB), the result is an estimation of end-to-end system performance in the real world. To arrive at an accurate answer, various factors such as the uplink power amplifier gain and noise factors, transmit antenna gain, path length, elevation angle and corresponding atmospheric loss over distance, satellite transponder noise levels and power gains, receive antenna amplifier gains and noise factors, cable losses, adjacent satellite interference levels, and climatic attenuation factors must be taken into consideration (Pozar, 2005).

The Friis equation is a fundamental equation used in link budget calculations to predict and analyse an attenuated RF signal transmitted through space to a receiver (Pozar, 2005).

$$P_r = \frac{P_t G_t G_r \lambda^2 F}{(4\pi)^3 D^4 L} \qquad 2\text{-}2$$

Where:

P_r : Received power at the receiving antenna in W;

P_t : Transmitted power at the transmitting antenna in W;

g_t : Transmitting antenna's power gain;

g_r : Receiving antenna's power gain;

D : Distance between the satellite and ground station in meter;

λ : Wavelength of the propagating signal in meter;

F : Propagation factor; and

L : Total link losses.

Equation 2-2 can be applied to both the uplink and downlink RF link budget calculations, converted to decibels (dB), Equation 2-2 can be written as:

$$P_r = P_t + G_t + G_r - L \qquad 2\text{-}3$$

Where, in units of dB

L: Free space loss + polarisation loss + insertion loss + atmospheric absorption loss + antenna pointing loss + receiver/transmitter loss

$L_p = 20\log\left(\frac{4\pi D}{\lambda}\right)$: Free space path loss in dB;

G_t : Transmitter antenna gain in dB; and

G_r : Receiver antenna gain in dB

The C-band command uplink budget for the F'SATI CubeSat is depicted in Table 2.2. The link margin calculation determines the required RF transmit power to achieve good communication between the GS and the CubeSat. Typical required margins for adequate CubeSat communication links are greater than 3 dB (Visser, 2009).

Table 2.2: Link budget for armature C-band uplink

C-band Command (CMD) Uplink	
Orbit (km)	600
Uplink frequency (MHz)	5660
Satellite Tx power (W)	5.00
Rx antenna gain at boresight (dB)	-10.00
Slant range (km)	2829.35
Total extra losses (dB)	6.5
Modulation	QPSK
Receiver antenna noise temperature (K)	100.00
Receiver noise figure (dB)	2
GS Rx antenna gain (dBi)	32.6
Eb/No (dB) @ GS	10.01
Link margin (dB)	3.23

2.5.2 Sensitivity and Selectivity

Radio receivers must be sensitive and selective enough to select only the desired signal among all the signals intercepted by the antenna and rejecting all the others. Sensitivity and selectivity are known as the most important receiver technical performance measures (TPMs). The selectivity of a receiver is a measure of its ability to reject unwanted signals and select only the desired signals. The receiver's selectivity is defined in terms of its adjacent channel rejection. The IF contributes most to the selectivity in the receiver. Most of the selectivity in the receiver comes from the amplifier stages and the RF filter characteristics of the coupling networks between the amplifier stages (Sayre, 2008: 498). Most of the gain in a receiver is provided in the IF amplifier stages of the receiver. In addition, sensitivity is normally defined in terms of the signal voltage amplitude that must be applied to the receiver's input to provide a

standard output power, measured at the receiver's output terminals. It is often expressed in dBm at a given signal-to-noise, distortion ratio (SINAD) and IF bandwidth (Sayre, 2008: 484).

Sensitivity is a measure of the receiver's ability to detect and amplify very weak signals. The sensitivity of the receiver is defined by the smallest signal that leads to an acceptable signal to noise ratio (SNR) as shown in Figure 2.7. SNR is the quantitative measure that compares the wanted signal to noise levels. The greater the difference between the wanted signal and the noise, the better the sensitivity performance of the system (Agilent Technologies, 2010).

Mathematically,

$$SNR = \frac{\text{Signal power}}{\text{Noise power}} = \frac{P_{\text{signal}}}{P_{\text{noise}}} = 10\log\left(\frac{P_{\text{signal}}}{P_{\text{noise}}}\right) \text{ dB} \qquad 2\text{-}4$$

From Figure 2.7, it can be deduced that the degradation in the performance of a receiver depends on the amount of noise the system adds on the received signal. For example, a signal applied to an amplifier will be amplified, however, the device will add some noise on this applied signal. If the internally generated noise is not minimal, the signal-to-noise ratio (SNR) at the output terminal will worsen. Methods used to improve the noise performance of a receiver system are therefore covered in this research.

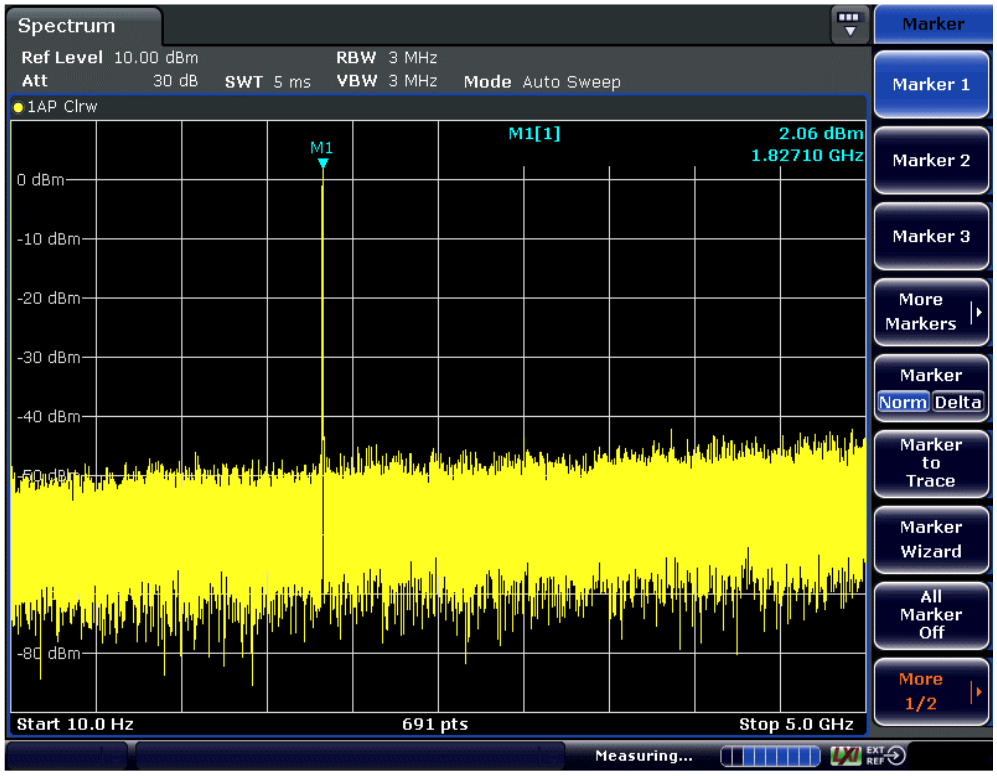


Figure 2.7: Spectrum analyser display of a transmitted RF signal (adapted from Agilent Technologies, n.d.)

2.6 Receiver System Architectures

The radio receiver is the most important part of the CubeSat communication subsystem and presents the most significant design challenge as stated by Klofas (2008:27). It is the last element in the communication system chain to ensure accurate and error free transmission of information. It is a critical requirement that any radio receiver should be able to:

- ✓ Select the wanted signal from a given frequency band.
- ✓ Recover the information from the modulated wave.
- ✓ Represent the information in a suitable manner (voice, audio, video or data)
- ✓ Minimise the degradation of the SNR.

Radio receivers can be characterized into different receiver architectures depending on the application as follows:

2.6.1 Amplitude Modulation (AM) Detector Receivers

The AM detector receiver is known as the simplest of radio architectures or implementations for detecting a modulated signal. According to Bowick *et al*. (2008:189), the name evolved from the fact that information (speech or music) could be converted into voltage or amplitude modulated signals onto a carrier wave. The resulting RF signal could therefore easily be demodulated at the receiver end by means of a simple diode detector.

The basic AM receiver architecture consists of an antenna for AM broadcasting; a RF filter or a variable capacitance filter for selecting the operating frequency band while rejecting out of band or unwanted signals such as noise; a detector to demodulate the AM signal and an optional amplifier to boost the recovered information to a level suitable for a listening device, such as a speaker or headphone as depicted in Figure 2.8 (Bowick *et al*., 2008:187).

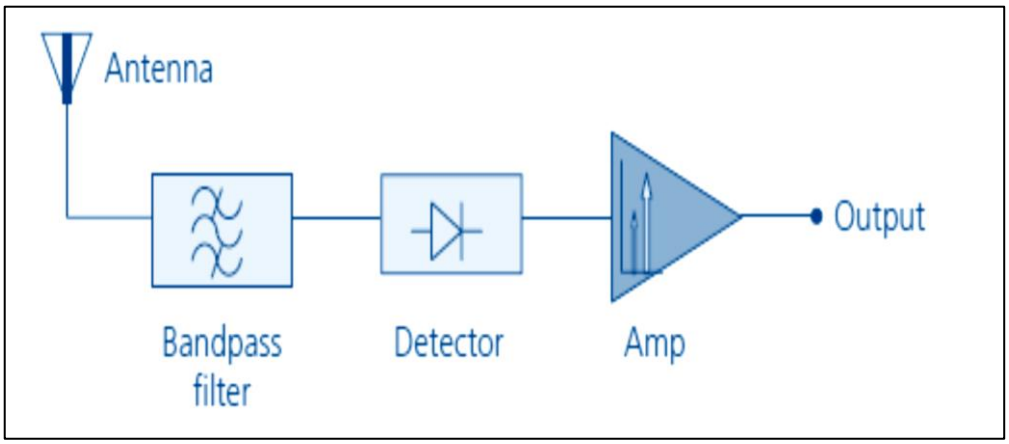


Figure 2.8: The simple AM radio receiver architecture block diagram (adapted from Janine et al., 2009: 37)

2.6.2 Tuned Radio Frequency (TRF) Receiver

The TRF receiver architecture is less complex compared to the AM detector receiver and emphasis is more on the additional multiple tuned filters as shown in Figure 2.9. In the history of receiver designs, the TRF receiver was one of the first to make use of amplification techniques to enhance the quality of the received signal or level. The TRF receiver architecture consists of several RF stages tuned simultaneously to the received frequency before detection and subsequent amplification of the desired audio signal. Each tuned stage consists of a bandpass filter such as a surface acoustic wave (SAW) filter, a dielectric cavity filter, or even an inductor-capacitor (LC) tank filter (Bowick et al., 2008:189).

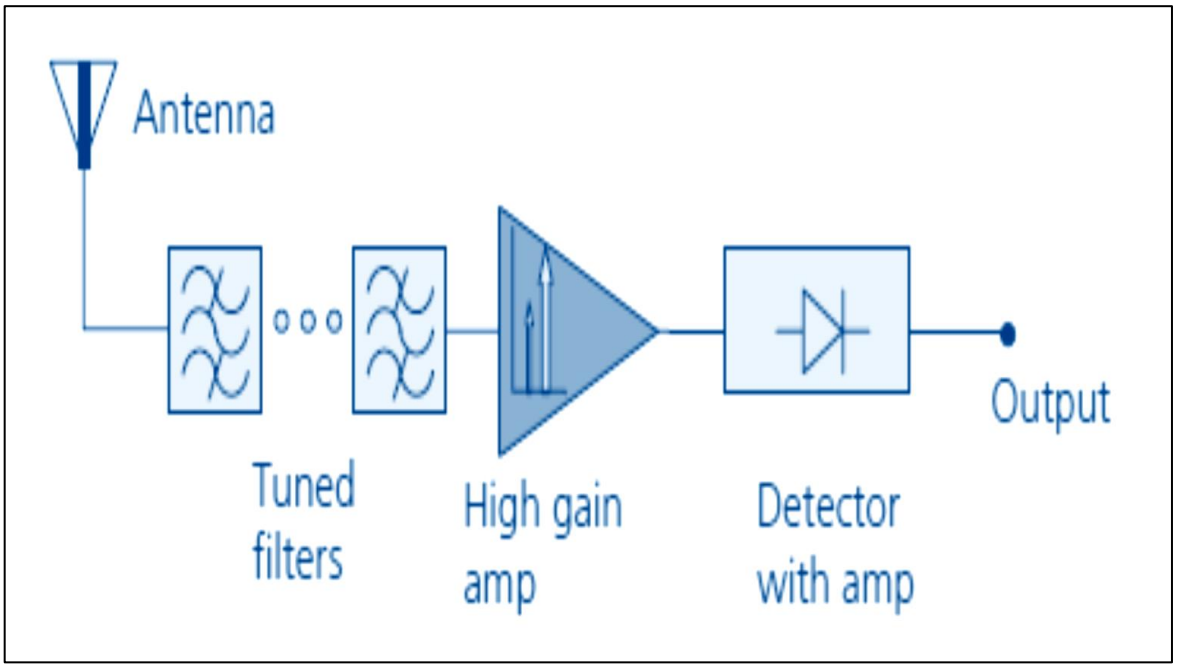


Figure 2.9: The TRF receiver architecture (adapted from Janine *et al.*, 2009: 40)

The final stage of the design is a combination of a diode rectifier and audio amplifier, together known as a grid-leak detector for demodulation. The advantage of this simple architecture is the fact that it does not generate the image signals that are common to other receiver architectures using frequency mixers, such as the superheterodyne receiver architecture covered later in this section. However, the main disadvantage of the TRF receiver is that the selectivity and amplification are not constant (Bowick *et al*., 2008:189).

2.6.3 The Direct-Conversion Receiver

The direct conversion receiver (DCR) also known as the zero IF receiver is depicted in Figure 2.10. This receiver architecture has a translation in frequency of the input signals and mixing of these input signals with those from a tunable local oscillator. Using only one mixing stage, this results into a lower frequency carrying the modulation which is deemed to be easier to detect and demodulate. The lowpass filter after the mixer is responsible for removing the

remaining higher frequency bands after downconversion. This will directly translate the input signals to baseband frequencies after subsequent amplification (Bowick *et al*., 2008:189).

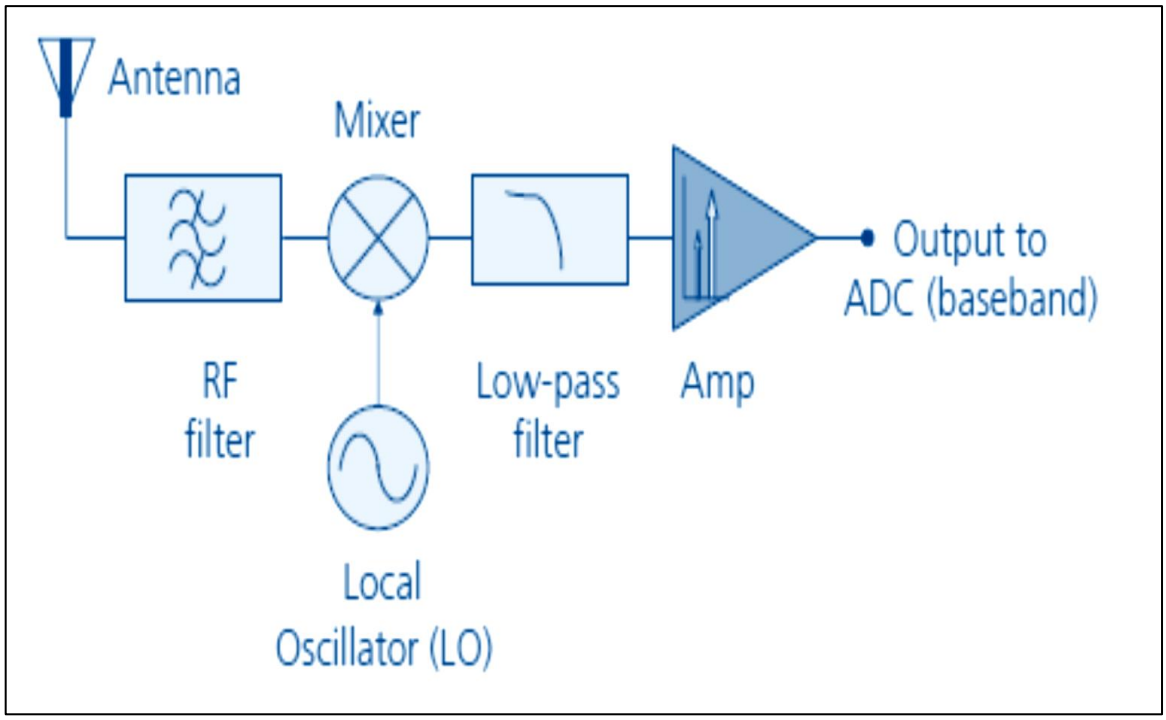


Figure 2.10: The direct conversion receiver (DCR) architecture (adapted from Janine *et al*, 2009:42)

The DCR is called a zero IF receiver because when the LO signal is chosen to be equal to the RF signal, the result out of the mixer is an IF at zero. The main advantage of the DCR is the one translation stage that it has, making it a simple approach in comparison to the superhet receiver architecture. In comparison to the TRF receiver, it has improved or higher selectivity due to the replacement of the multiple tuned filters by a single RF filter. The major drawbacks however, is the susceptibility to spurious LO leakage that can generate DC offsets and vulnerability to various noise sources at DC (Bowick *et al*., 2008:189).

2.6.4 The Superheterodyne Receiver

The Superheterodyne or superhet receiver depicted in Figure 2.11, is the most popular amongst all receiver architectures and hence commonly used. Even though the architecture is complex and requires more mixing stages, it offers good selectivity and sensitivity in comparison to the amplitude modulation (AM) detector, tuned radio frequency (TRF) and direct conversion receiver (DCR) architectures. Unlike the DCR in which the LO frequencies are synchronised to the input RF signals, a superhet receiver uses a LO frequency that is offset by a fixed amount from the desired signal. This fixed amount results in an IF at the mixer output generated by mixing the LO and RF signals. The major drawback of this receiver architecture is that it generates image signals that can be larger than the desired signal frequency and may cause resolution challenges for the demodulator (Bowick *et al*., 2008:190).

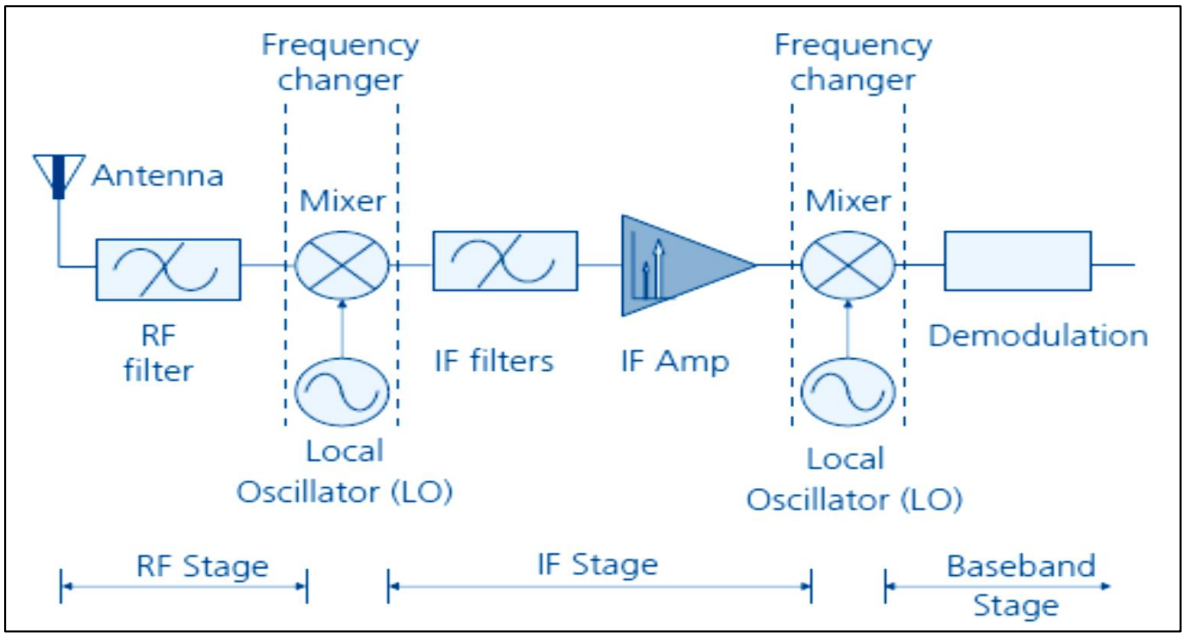


Figure 2.11: The superheterodyne architecture (adapted from Janine *et al.*, 2009: 44)

Figure 2.12 shows what the superheterodyne receiver's frequency spectrum looks like. The superhet receiver function is divided into two stages; the RF and IF bands to allow for optimal performance mixing of the RF signal and the LO signal to generate the IF or audio signal as shown in Figure 2.12. Image signals are also generated, which are copies of the RF and IF signals. The effects of these undesired signals are removed by using a filter around the desired signal frequencies.

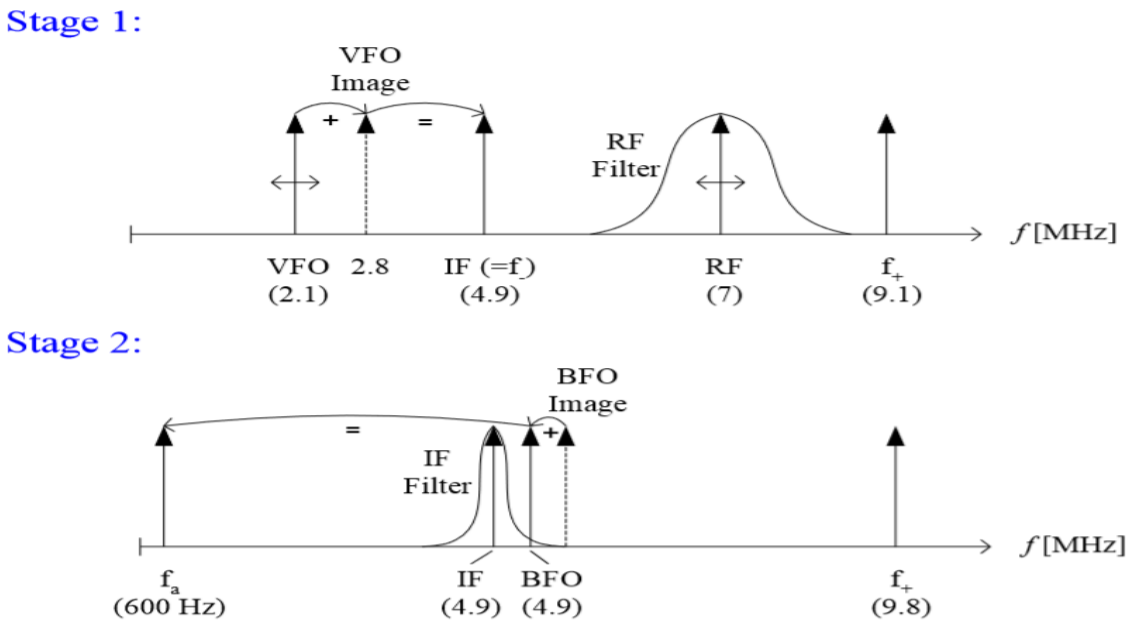


Figure 2.12: Superheterodyne receiver spectrum (adapted from Agilent Technologies, n.d.)

Table 2.3 depicts a comparison of four different receiver architectures, each architecture has its own set of advantages and draw backs. Choosing an appropriate architecture is based on the specific application requirements and the trade-offs that best matches the requirements. The superheterodyne receiver architecture was implemented for the C-band downconverter.

Table 2.3: Summary of receiver architectures

Parameter	Heterodyne	Direct conversion	Sub-sampler	Low-IF
Selectivity	High	High	High	High
Analog requirements	High	Moderate	Moderate	Low
Flexibility	Low	Low	High	High
CMOS capability	Low	Moderate	Moderate	High
Noise	Low	Moderate	High	Low
Dynamic range	High	High	High	High

2.6.5 SDR Implementation Approach

The SDR concept was first introduce by Mitola in the early 90's by Joseph Mitola (Mitola, 1992). Many CubeSat missions in recent years have adopted the use of SDR architectures for satellite communication applications. The SDR architecture includes essential hardware components within the radio such as the analog-to-digital converters (ADCs), digital-to-analog converters (DACs), field-programmable gate arrays (FPGAs) and integrated circuit radios. The SDR receiver implementation approach typically involves feeding an incoming RF signal from the antenna to an ADC to be digitized and passed along to the digital baseband processor. The transmitter side mirrors the receiver. The SDR architecture is popular in the satellite industry because it allows for flexibility as it is fully configured in software and it can be reconfigured over the air. The availability of components, power consumption, and low noise performance are the key design drivers in CubeSat applications. According to Crockett (2023), there are three main SDR architectures. Figure 2.13 depicts a high level direct-RF SDR architecture, whereby almost all functionality is implemented digitally and requires minimal analog processing. The front-end mostly consist of the RF antenna, amplifiers and filters. This architecture is applicable for higher sampling rate applications in the order of 10 GSps (Crockett, 2023).

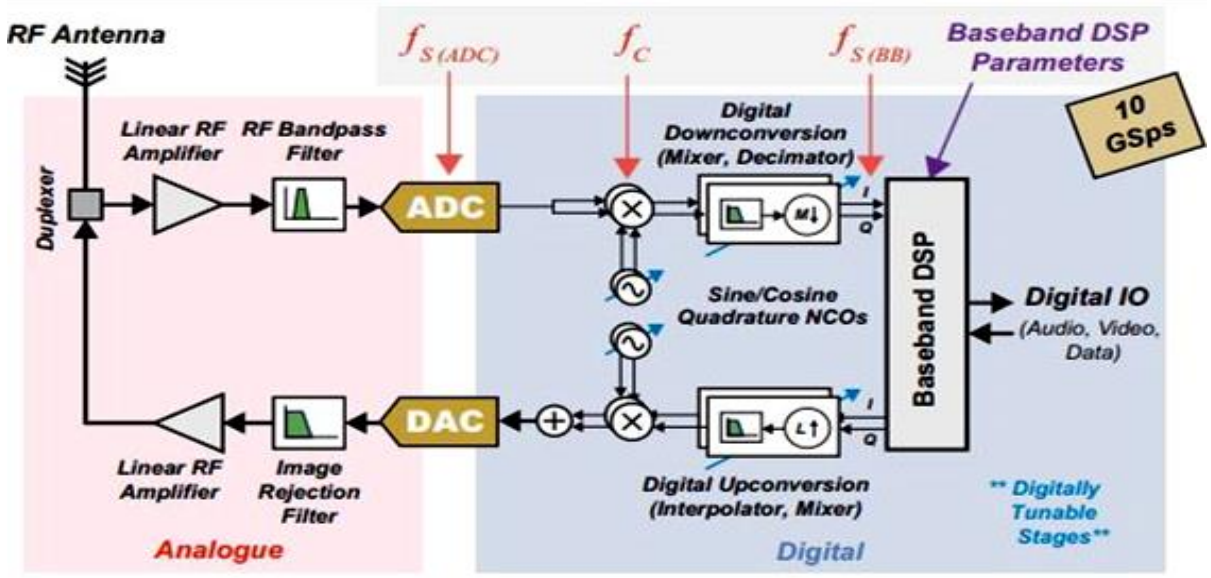


Figure 2.13: A direct-RF (almost-all-digital) radio (Crockett, 2023)

Depicted in Figure 2.14 is a high-level architecture of an IF-sampling SDR. This architecture is used in applications where the RF signal is higher than the available ADC and DAC sampling rates. A down conversion stage based on the superheterodyne architecture is therefore required to translate the higher RF signal to a lower IF signal. The down conversion stage is mainly implemented in the analog domain with few exceptions of the control circuitry. The demodulation and modulation between the IF and baseband are implemented in the digital domain. The sampling rate for this architecture is in the order of 10 MSps (Crockett, 2023).

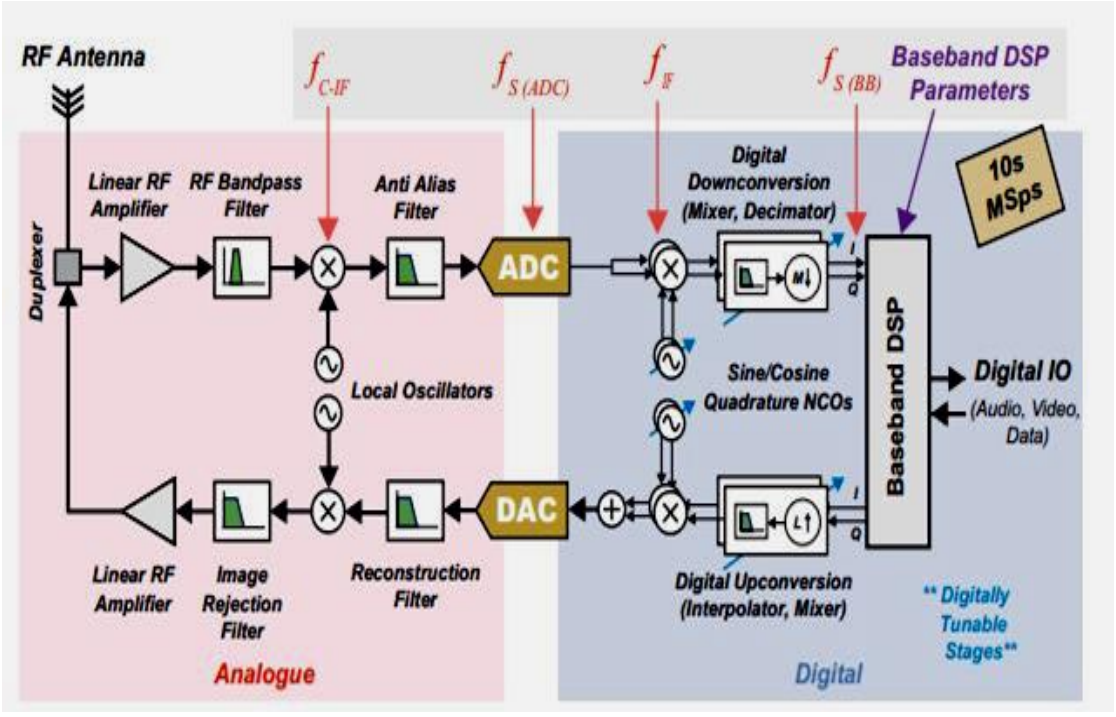


Figure 2.14: An IF-sampling software-defined radio (Crockett, 2023)

Figure 2.15 shows a high-level baseband-sampling SDR. All the modulation and demodulation are performed in the analogue domain; this is achieved by using multiple or single conversion stages. According to Crockett (2023), baseband sampling was one of the earlier methods used due to limitations of the ADC and DAC technologies. This architecture can be adopted for applications requiring low data rates, low-cost and receiving wider bandwidth signals (Crockett, 2023).

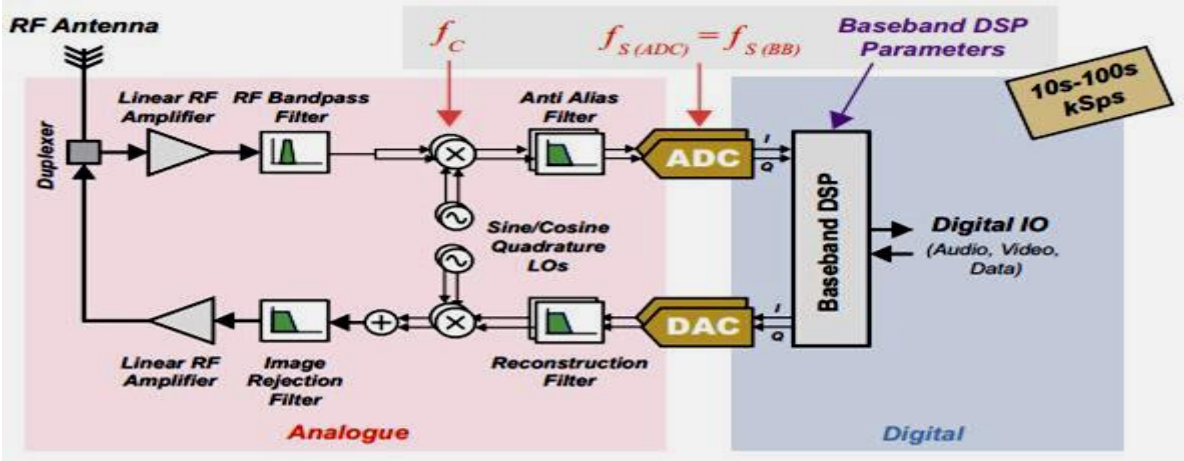


Figure 2.15: A baseband-sampling software defined radio (Crockett, 2023)

2.6.6 CubeSat Receiver System Architectures

The CubeSat receiver subsystem is critical, and its architecture can influence a mission success. The receiver architecture's flexibility, configurability through software, and the ability to be reconfigured remotely are highlighted as the key features. Additionally, the design is driven by factors such as power consumption, low noise performance, and component availability. A brief review for typical CubeSat receiver architectures was conducted to ascertain what is available on the market, and as a result the following receiver architectures were investigated. The first CubeSat architecture that can be implemented is shown in Figure 2.16. This architecture is based on the digital down-conversion (DDC). The DDC is typically achieved by extensive firmware operations using a high-end field programmable gate array (FPGA) device (Mitola,1992).

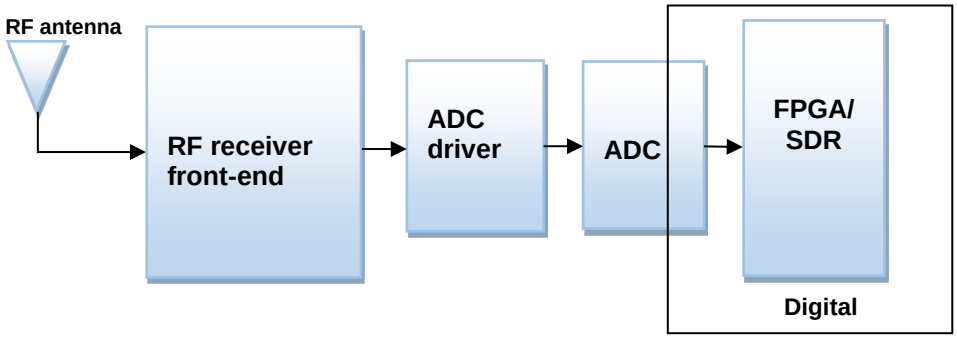


Figure 2.16: SDR based on digital down-conversion (DDC) implementation

The advantage of this implementation is flexibility, as it can be fully configured in software and reconfigured while in space. The drawback for this implementation is the firmware development that tends to be a complex and time-consuming process. Additionally, the FPGA tends to be the highest cost component in many systems (Mitola, 1992).

SDR technology is advanced in recent years and as a result, many demodulator/modulator COTS components are readily available for various applications. Table 2.4 shows a shortlist of demodulators/modulators available on the market. From this table, demodulators /modulators at 1 GHz and below operate at reasonable power levels for CubeSat applications. Few demodulators/modulators exist at 6 GHz and above, and the power consumption associated with these higher frequencies tend to be more.

Table 2.4: Data demodulator and modulators IC's shortlist (Mouser, 2023)

Mfr Part Number	Mfr.	Pricing	Type	Modulation Format	Maximum Frequency	Minimum Frequency	Operating Supply Voltage	Operating Supply Current
ADMV4540ACCZ	Analog Devices	$83.55	Demodulator	Quadrature	22 GHz	17 GHz	3.3 V	980 mA
ADRF6850BCPZ	Analog Devices	$26.51	Demodulator	Quadrature	22.5 MHz		3.15 V to 3.45 V	350 mA
ADL5387ACPZ-R7	Analog Devices	$13.32	Demodulator	Quadrature	2 GHz	30 MHz	4.75 V to 5.25 V	180 mA
ADL5375-05ACPZ-R7	Analog Devices	$13.94	Modulator	Quadrature			4.75 V to 5.25 V	174 mA
TRF3705IRGET	Texas Instruments	$12.54	Modulator	Quadrature	4 GHz	300 MHz	3.3 V	306 mA
TRF3722IRGZT	Texas Instruments	$20.18	Modulator	Quadrature	4.2 GHz	400 MHz	3.3 V, 5 V	374 mA
TRF370417IRGET	Texas Instruments	$22.33	Modulator	Quadrature	6 GHz	50 MHz	4.5 V to 5.5 V	205 mA
AD8348ARUZ-REEL7	Analog Devices	$12.89	Demodulator	Quadrature	1 GHz	50 MHz	2.7 V to 5.5 V	48 mA
AD8345AREZ	Analog Devices	$13.87	Modulator	Quadrature	1 GHz	140 MHz	2.7 V to 5.5 V	65 mA
ADL5380ACPZ-R7	Analog Devices	$14.63	Demodulator	Quadrature	6 GHz	400 MHz	4.75 V to 5.25 V	245 mA
LT5575EUF#PBF	Analog Devices	$20.52	Demodulator	Quadrature	2.7 GHz	800 MHz	4.5 V to 5.25 V	132 mA
LT5546EUF#PBF	Analog Devices	$10.30	Demodulator	Quadrature	500 MHz	40 MHz	1.8 V to 5.25 V	24 mA
LTC5598IUF#PBF	Analog Devices	$13.79	Modulator	Quadrature	1.6 GHz	5 MHz	4.5 V to 5.25 V	165 mA
LTC5585IUF#PBF	Analog Devices	$15.90	Demodulator	Quadrature	4 GHz	400 MHz	4.75 V to 5.25 V	200 mA
ADRF6821ACPZ	Analog Devices	$38.37	Demodulator	Quadrature	2.8 GHz	450 MHz	3.1 V to 3.5 V	-
AD8346ARUZ	Analog Devices	$11.96	Modulator	Quadrature	2.5 GHz	800 MHz	2.7 V to 5.5 V	45 mA
8348ARUZ	Analog Devices	$13.85	Demodulator	Quadrature	1 GHz	50 MHz	2.7 V to 5.5 V	48 mA
MAX2021ETX+	Analog Devices / Maxim Integrated	$13.25	Modulator/ Demodulator	Quadrature	1.2 GHz	650 MHz	4.75 V to 5.25 V	271 mA
AD8333ACPZ-WP	Analog Devices	$22.04	Demodulator	Quadrature	50 MHz	0 Hz	5 V	44 mA
ADRF6755ACPZ	Analog Devices	$21.22	Modulator	Quadrature	2.4 GHz	100 MHz	4.75 V to 5.25 V	380 mA
ADL5382ACPZ-R7	Analog Devices	$14.63	Demodulator	Quadrature	2.7 GHz	700 MHz	4.75 V to 5.25 V	220 mA
TRF372017IRGZT	Texas Instruments	$13.46	Modulator	Quadrature	4.8 GHz	300 MHz		
ADL5375-15ACPZ-R7	Analog Devices	$13.92	Modulator	Quadrature	6 GHz	400 MHz	5.25 V	203 mA
LT5516EUF#PBF	Analog Devices	$11.95	Demodulator	Quadrature	1.5 GHz	800 MHz	4 V to 5.25 V	117 mA
LTC5588IPF-1#PBF	Analog Devices	$15.14	Modulator	Quadrature	6 GHz	200 MHz	3.15 V to 3.45 V	303 mA

The second CubeSat architecture that can be implemented is shown in Figure 2.17. This architecture is based around a low power transceiver chipset with a built-in DDC feature. Instead of using extensive FPGA-based logic, it is possible to utilize the built-in DDC feature

which simplifies the system architecture. The drawback is that the transceiver chip tends to limit the system capability in terms of flexibility and available modulation.

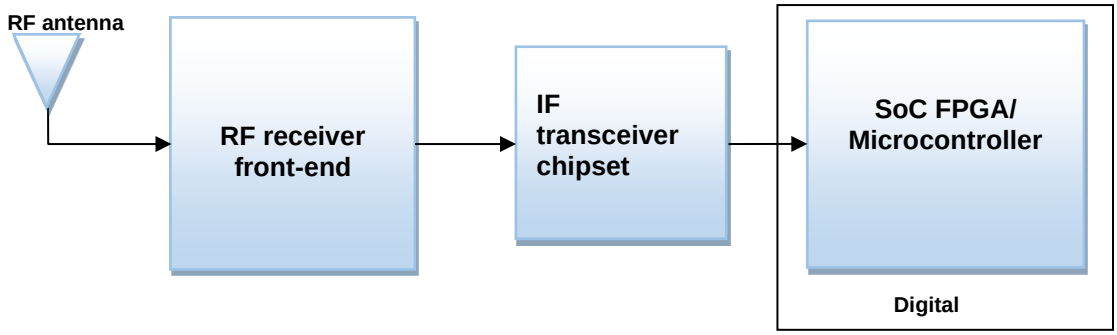


Figure 2.17: SDR based on a transceiver chipset with built in digital down-conversion (DDC)

Table 2.5 shows COTS semiconductor devices that consist of a receiver and a transmitter in a single package. Transceiver IC's are designed to function proficiently within a standard such as LTE, Bluetooth, ISM, VHF, cellular and radar. They are further classified by the type of modulation and the specific protocol versions as indicated.

Table 2.5: RF transceiver IC's shortlist (Digikey, 2023)

Mfr Part #	Mfr	Description	Price ($)	Function	LO Frequency	RF Frequency	P1dB	Gain	Noise Figure	Current - Supply	Voltage - Supply
AD8333ACPZ	Analog Devices Inc.	DUAL I/Q DEMODULATOR	261.56333	Demodulator	100kHz ~ 200MHz	0Hz ~ 50MHz	14.5dBm	4.7dB	11dB	44 mA	4.5V ~ 6V
HMC908ALC5	Analog Devices Inc.	I/Q DOWN-CONVERTER 9-12 GHZ	1342.82	Downconverter	8.5GHz ~ 15.5GHz	9GHz ~ 12GHz	-8dBm	-	-	100 mA	4V
MAX2309EGI-B50070	Analog Devices Inc./Maxim Integrated	CDMA IF VGA AND I/Q DEMODULATOR	83.5525	Demodulator, Amplifier	40MHz ~ 300MHz	40MHz ~ 300MHz	-9dBm	61dB	-	25.9 mA	2.7V
MAX2314EEI	Analog Devices Inc./Maxim Integrated	CDMA IF VGA AND I/Q DEMODULATOR	86.54279	Demodulator, Receiver	-	40MHz ~ 300MHz	-6.4dBm	63.4dB	62.9dB	25.9 mA	2.7V
MAX2308EGI	Analog Devices Inc./Maxim Integrated	CDMA IF VGA AND I/Q DEMODULATOR	91.64397	Demodulator, Amplifier	40MHz ~ 300MHz	40MHz ~ 300MHz	-9dBm	61dB	-	25.9 mA	2.7V
MAX2314EEI+	Analog Devices Inc./Maxim Integrated	CDMA IF VGA AND I/Q DEMODULATOR	119.612	Demodulator, Receiver	-	40MHz ~ 300MHz	-6.4dBm	63.4dB	62.9dB	25.9 mA	2.7V
MAX2309EGI	Analog Devices Inc./Maxim Integrated	CDMA IF VGA AND I/Q DEMODULATOR	161.12455	Demodulator, Amplifier	40MHz ~ 300MHz	40MHz ~ 300MHz	-9dBm	61dB	-	25.9 mA	2.7V

The CubeSat receiver architecture involves down-converting the received RF signal to an IF that is suitable for ADC/DAC processing. The ideal receiver architecture requires a direct connection between the antenna and SDR. However due to limitations of the ADC/DAC components, as well as limited available transceiver IC's at higher frequencies, this necessitates the need for downconversion. This process allows for efficient digitization and subsequent processing of the received signals (Mitola, 1992).

Figure 2.18 shows a S-band CubeSat receiver block diagram based on a transceiver chip with built-in DDC. This architecture employs a super-heterodyne single stage conversion architecture. The received RF signal is down-converted to a lower IF so that the ADC can sample and digitise the IF signal to a baseband signal for processing. The C-band downconverter system implemented in this research forms part of a C-band receiver front-end and employs the super-heterodyne architecture. It is essentially an upgrade of the S-band receiver front-end highlighted in yellow in Figure 2.18 to a C-band receiver front-end, with exception of the antenna and diplexer. Table 2.6 gives a summary of the reviewed spaceborne receiver / downconverter / transceiver implementation and their highlights.

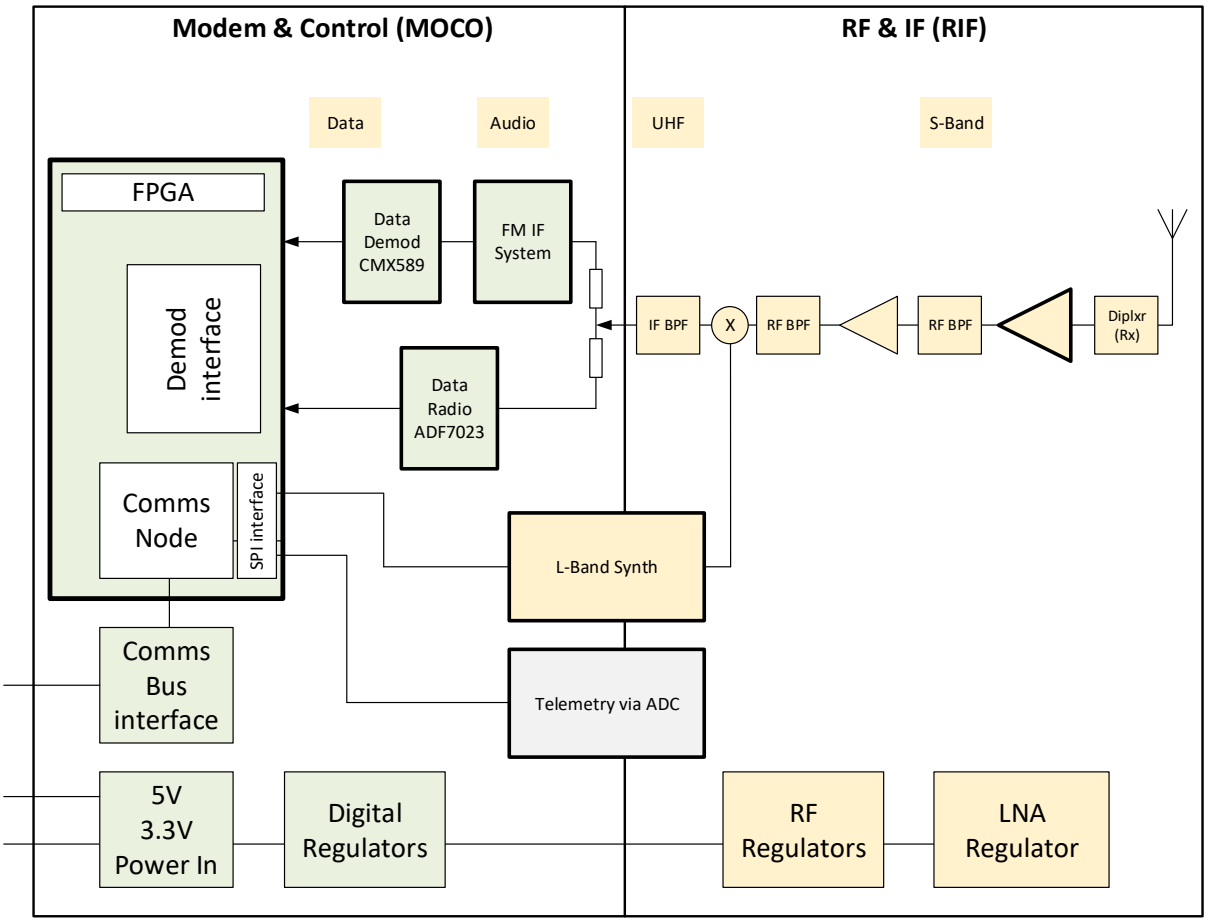


Figure 2.18: CubeSat S-band receiver block diagram (F'SATI, 2020)

Table 2.6: Spaceborne receiver/ downconverter/ transceiver

Satellite Downconverter Analysed	Highlights
Chang et al., 2005	Developed a receiver downconverter module for Ka-band satellite payload, which has a low noise amplification in front stage and frequency downconversion, ranging from 30.6 - 31.0 GHz to 20.8 - 21.2 GHz. The module has a noise factor (NF) of 1.9 dB and Gain of 55 dB.
Butters & Raad, 2014	Designed a 2.4 GHz high data rate radio for pico-satellites. Employed a quadrature amplitude modulation (QAM) with a zero-intermediary frequency (ZIF, known also as direct-conversion receiver. The Maxim MAX2837 highly integrated transceiver was chosen. The radio can potentially attain bits rates in the order of 60 Mbps with 0.3 W in receive mode and 0.5 W in transmit mode plus an extra 2 W for the power amplifier.
Lurie, 2016	Bitbeam modular SDR. Frequency Band: 100 – 6000 MHz. Rx Daughter Board: 2.0 - 2.1, 2.4 - 1.5 GHz. Tx Daughter Board: 8.1 - 8.5 GHz. Data Rate 100 kbps - 200 Mbps. Size & Mass 90.2 x 96 x 13.8 mm / 97 g. Power 1 - 4 W.
Lovascio et al., 2019	Design of a COTS-based RF receiver for CubeSat applications. Workflow for RF systems based on different strategies, such as the use of the COTS components, system-based modelling and the electromagnetic analysis of 50 Ω impedance lines. This workflow was exploited to design a satellite receiver that has a very low NF of 1 dB, with improved sensitivity of -115 dBm. An adjustable gain control (AGC) of 52 dB was obtained by cascading two COTS amplifiers with an inherent AGC. The receiver was made compliant to TMTC applications by designing the input filter with a 2.025 - 2.110 GHz bandwidth. Furthermore, the receiver was radiation hardened up to 20 krad. Used a single stage superheterodyne downconverter.
Alimenti et al., 2020	A Ka-Band receiver front-end having noise injection calibration circuit for CubeSats inter-satellite links. The receiver was capable to support very high data rates (up to 100 Mbit/s) in quadrature phase-shift keying (QPSK). The receiver feasibility was demonstrated based on a class of miniaturized and low-cost microwave integrated circuits, presently obtainable in the market. Their receiver was based on a novel combination of integrated low-noise amplifiers (LNA) having an image rejection filter, with the latter exploiting the substrate integrated waveguide (SIW) technology. COTS integrated circuits and SIW technology can be used to lower the electronic hardware cost and the need to shield apparatuses. The front-end operates between 27.5 and 30 GHz was implemented, and it exploits custom PCBs and features a 80 dB gain, a 2.8 dB NF and an image rejection >70 dBc. These findings give a new state-of-the-art for Ka-band active front-ends rooted on SIW technology.
Rastinasab & Weindong, 2021	A CubeSat with a 500 km altitude design/ implementation of a RF-front-end telemetry, tracking and command subsystem. VHF/UHF transceivers smartly realised based on three separate PCBs: receiver, transmitter and filters.
Abdullah, 2021	An enhanced S-Band CubeSat communication subsystem design and implementation with an uplink / downlink at frequency bands respectively from 2.025 - 2.11 GHz and from 2.2 - 2.29 GHz. The transceiver system is based on the Analog Devices AD9361 chip and controlled by Xilinx Zynq-7000 FPGA. The RF output signal is

	amplified to approach 33 dBm output power to the antenna port via QORVO chip that operates from 700 - 2700MHz.
Nguyen et al., 2021	Design of a S-Band transceiver for CubeSats. The transceiver can render a 96 kbps of data rate with maximum power output of 39.3 dBm (8.5 W) and a total volume of 87.4 x 93.4 x 20 mm^3 with total mass of 252 g including aluminium housing.
Theoharis et al., 2021	CubeSat applications software-defined radios (SDR): a brief review and methodology. Two different techniques were suggested for designing SDRs for highly integrated and miniaturized platforms such as CubeSats. The radio was equipped with a FPGA system on chip (SoC), thus approximating an ideal SDR architecture. Their design has the possibility to reach a data rate of 60 Mbps and only consuming 0.4 W when receiving and 2.6 W when transmitting. It is flexible, on-the-fly re-configurable with the ability of high data rate communications under low power consumption. The proffered platform addresses the current communication drawbacks of CubeSats and pioneers the capability to form swarms of CubeSats.
Barigelli et al., 2022	W-band to Ka-band frequency converter for ultra-high throughput satellite systems. Frequency ranges from 81–86 GHz to 17.2 - 20.2 GHz with a 65 dB gain conversion. NF of 5.5 dB and total third order intercept point (OTOI) of +30 dBm. LO signal was < −40 dBm. Several custom MMICs were developed for their project by using the space qualified PH10 GaAs process from UMS. According to the authors, their work is the first “Docon” operating in W-band realised ever for space applications.
Moaro et al., 2022	Their paper presented the design of a low complexity digital front-end (DFE) for CubeSats SDR applications. A multi-stage sample rate conversion (SRC) design process was executed to achieve the low complexity DFE. A low-power DFE direct-sampling receiver for versatile radios.
Orecchini et al., 2023	Ku-band low-noise block (LNB) downconverter for Cubesat transponders operating at 2.185 GHz. The front-end consist of a low-noise amplifier (LNA) and two switchable substrate integrated waveguide (SIW) filters, providing a re-configurable frequency to the system. The LNB is completed by a downconversion unit, consisting of a mixer, a PLL frequency synthesizer and an IF amplifier. A first breadboard features a total gain of 54 dB with a NF of 2.3 dB. Measured power gain and noise figure of the entire receiver front-end for the 13 and 14 GHz switch configurations. Center frequency performance (including the coaxial adapter): 15.5 dB gain and 2.4 dB NF (13 GHz configuration); 17.8 dB gain and 2.3 dB NF (14 GHz configuration). The front-end draws a current of ~54 mA at 3 V (LNA) and 7 mA at 5 V (both switches). The overall power consumption was < 162 mW.
AAC Clyde Space, n.d.	AAC SpaceQuest RX-2000 space qualified S-band receiver for MicroSats and small satellites. Has a frequency range from 2 - 2.4 GHz. Implements GMSK modulation and up to 26 customer programmable channels with 20 MHz bandwidth, enabling configuration control. Had a data rates between 9.6 – 153.6 Kbps.
Alén Space, n.d.	TOTEM flight-proven SDR. Wide RF range transceiver (AD9364). High-performance System-On-Chip (SoC) - Xilinx Zynq-7000. Can be reconfigured in-orbit. SDR transceiver across several frequency bands: UHF, VHF, S-band and L-band. Wide band transceiver 70 MHz - 6 GHz. Up to 56 MHz bandwidth. Have x2 TX and x3 RX channels. Used the fronted interface as piggyback board.
CesiumAstro, n.d.	Adjustable space qualified SDR-1001, frequency range 300 - 6000 MHz, UHF, L, S, C. up to 62.500 kbps data rate. 100 g mass. Size of

	5 x 8.4 x 1.3 cm. Has x4 100 MHz receive channels. Has x4 200 MHz transmit channels. Modulation BPSK/QPSK. DC input voltage from 9 - 13 V. Operating temperatures -24 to 61 °C.
Cubecom, n.d.	S-band and X-band downconverter, frequency: 2.2 - 2.29 GHz and 8.025 - 8.4 GHz. Output frequency: 1.330 GHz. Bandwidth: 80 MHz. form factor: 19 inch rack mount.
GomSpace, n.d.	Flight proven NanoCom SDR MK3. Frequency range 70 - 6000 MHz. Frequency band VHF, UHF, L, S, X. AD9361 IC. 2 × 2 transceiver with integrated DACs and ADCs. Channel bandwidth is tuneable from 200 kHz to 56 MHz. Xilinx Zynq 7030/7045 Programmable SoC. Operational temperature: -40°C to +85°C. Mass 240 g. Dimensions 95 x 95 x 31.5 mm (with 3 x TR600). x2 Rx and x2 TX transceiver RF Inputs/Outputs. Resolution is 12-bits DACs and ADCS.
IQ Spacecom, n.d.	XLink is an advanced transceiver system SDR for X-band and S-band communication links for small satellites with a flight grade tested COTS design. Radio interfaces and protocols are compatible to standard CCSDS and DVB-S2 specifications. Gigabit Ethernet is provided as on-board control and high-speed data interface. X-band Rx operation: 7.145 - 7.250 GHz. S-band Rx operation: 2.025 - 2.110 GHz. Data rate Sat2Ground: 16 kbps up to 200 Mbps. Data rate Ground2Sat: 3.5 kbps up to 896 kbps. Downlink/TM & Payload up to 200 Mbps. Uplink / Telecommand 56 kbps. Proven compatibility of space and ground segments.

2.7 Downconverter Building Blocks

The design and selection of each downconverter building block is crucial for achieving the desired system performance in terms of frequency selectivity, dynamic range, NF, and sensitivity. The functionality and characteristics of these components must be clearly understood to ensure that the requirement of the application receiver system is met. The downconverter components are discussed as follows:

2.7.1 Filters

Filters ensure that the unwanted signals that are received by the receive antennas are filtered out to achieve optimum signal quality of the desired signal and reduce interference caused by unwanted frequencies. Working through the downconverter architecture shown in Figure 2.19 from input to output, the first component right after the antenna is referred to as the pre-selector filter, the main aim of this filter is to attenuate all RF frequencies outside of the RF band of interest.

The second filter which follows the LNA is referred to as the image filter. The primary function of this filter is to attenuate any signal or noise present as the image frequency. The image frequency is determined by the sum of 2*IF+RF in the case of low side LO's and by the difference of the RF and 2*IF in the case of high side LO's. If this frequency is not properly and sufficiently attenuated by the image filter, any signal or noise present there will be mixed directly into the RF band and will degrade the receiver performance.

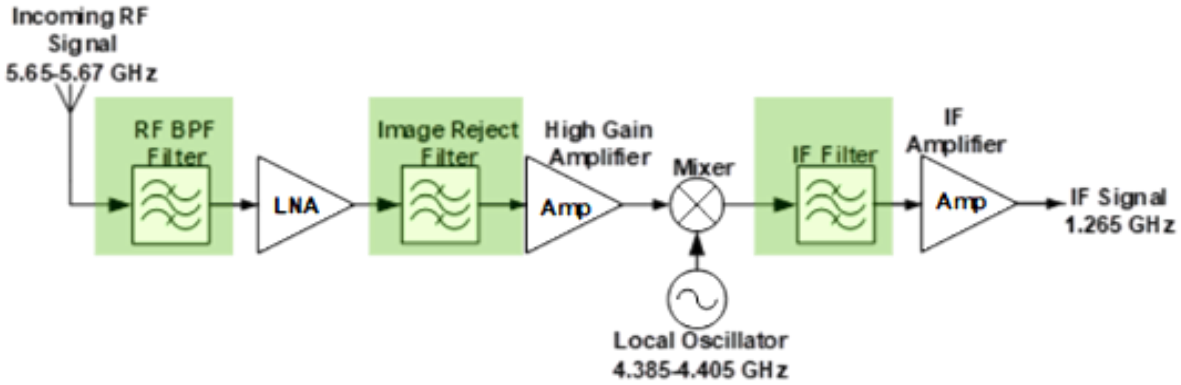


Figure 2.19: Downconverter filters

The third filter which follow the mixer is the IF Filter. The IF Filter determines the overall selectivity in the receiver, and it would usually be a saw-based technology. This filter must also remove unwanted mixing products generated by the mixer. In choosing the receiver IF frequency, selection is usually limited to some of the standard IF frequencies where saw filters are readily available, such as 10 MHz, 70 MHz, 100 MHz, 1.575 GHz etc. At the same time, ensure the IF frequency is high enough to enable adequate image rejection/suppression as discussed previously. Selecting IF frequency requires careful consideration as mixers generate intermodulation products which could potentially fall inside the IF band.

2.7.1.1 Filter Types

Filters are classified into different operational types based on their frequency response characteristics. Common RF filter types include low pass, high pass, band bass and band stop filters. Figures 2.20 to 2.25 Illustrate frequency responses of low pass, high pass, band bass and band stop filters, respectively. A low pass filter allows frequencies below a certain frequency referred to as the cut-off frequency (Fc), to pass through with minimum attenuation while blocking high frequency signals. Fc is determined and specified at the point where the filter insertion loss is equal to 3 dB. Insertion loss of a filter measured in dB, is referred to as the amount of signal power loss or the difference in RF signal power measured at the input and output of a filter within a passband frequency range. In a 50 ohm impedance RF system, the insertion loss is a cumulative sum of three loss factor; one is the loss due to the impedance of mismatch at the filter input, the second is due to the mismatch at the filter output and the third is due to the dissipative loss associated with each reactive element withing the filter. When designing and selecting filters, a lower insertion loss is often desirable in a receiver system because it indicates how well a filter is receiving a signal with minimum attenuation and power loss. The lower the insertion loss the better the filter performance and the better the overall system performance in terms of increased signal quality and optimal signal reception with minimum degradation (Pozar, 2001:271).

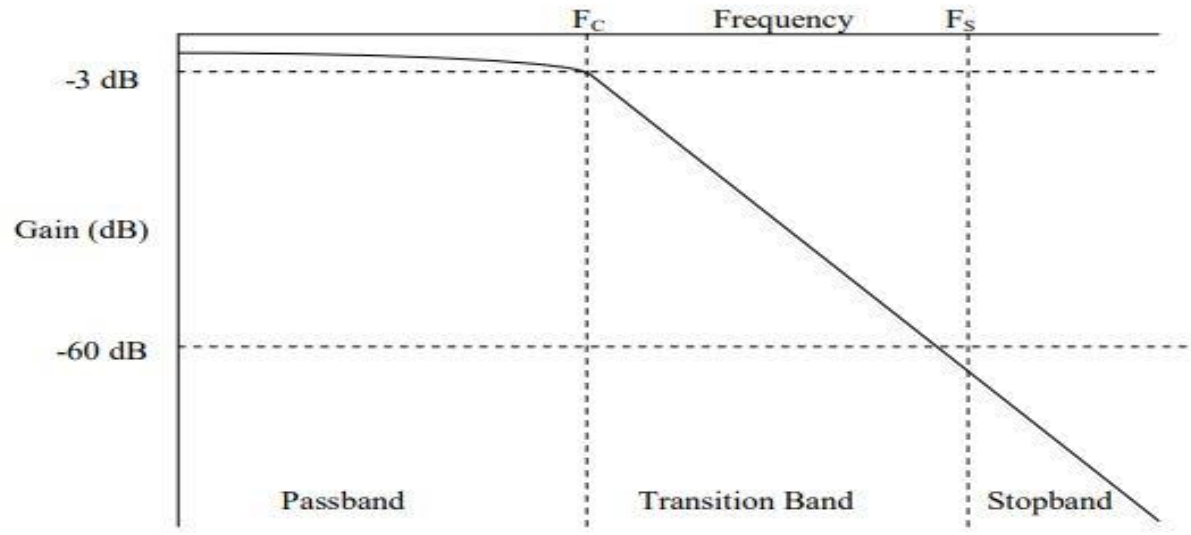


Figure 2.20: Frequency response of a lowpass filter (Pozar, 2001:271)

The Fc point express the passband, transition band and stopband boundary points in the frequency response of a filter. The passband represents the frequency range of interest for the desired signal reception. Signals within the passband of a filter can pass through with minimal attenuation and loss. The passband frequency is an essential parameter to consider when designing and selecting a filter for a receiver system because it determines the specific frequency range that can pass through while attenuating and rejecting frequencies outside that range. The stopband, often referred to as isolation of a filter, is the frequency range where signals are attenuated or suppressed. The higher the attenuation the better. Ideal filters perfectly allow frequencies in the passband and completely reject frequencies in the stopband. However, in real world applications, filters are not ideal, and satellite receivers are no exception.

The design method and simulation type of a filter is normally characterised based on their order and amplitude characteristic or the type of polynomial that describes the filter. Figure 2.21 illustrates the four basic filter topologies, each filter type has its own advantages and disadvantages. The choice of filter topology depends on the specific requirements of the receiver system, such as the desired frequency response, passband stopband characteristics and the trade-off between passband ripple and stopband attenuation. The Butterworth filter has a frequency response that is maximally flat in the passband and an adequate rate of roll-off. The Butterworth filters are used in applications that requires a flat frequency response and a gradual roll-off in the stopband. The Chebyshev filter frequency cut-off is steeper compared to that of the Butterworth filter, at the expense of ripples or amplitude variations in the passband. Chebyshev filters are commonly used in applications that require a sharper transition between the passband and stopband. The Elliptic also known as Cauer filter has a

steeper roll-off in the stopband compared to all the four filter types. As a result, the Elliptic filter allows ripples both in the passband and stopband as shown in Figure 2.21. Elliptic filters are often used in applications that require a high level of stopband attenuation, and at the expense of passband ripple. The Bessel filter has a flat magnitude response in the passband at the expense of a less steep cut-off in the stopband. The Filter performance can effectively be evaluated and optimised for the RF satellite receiver application by selecting the appropriate filter design method.

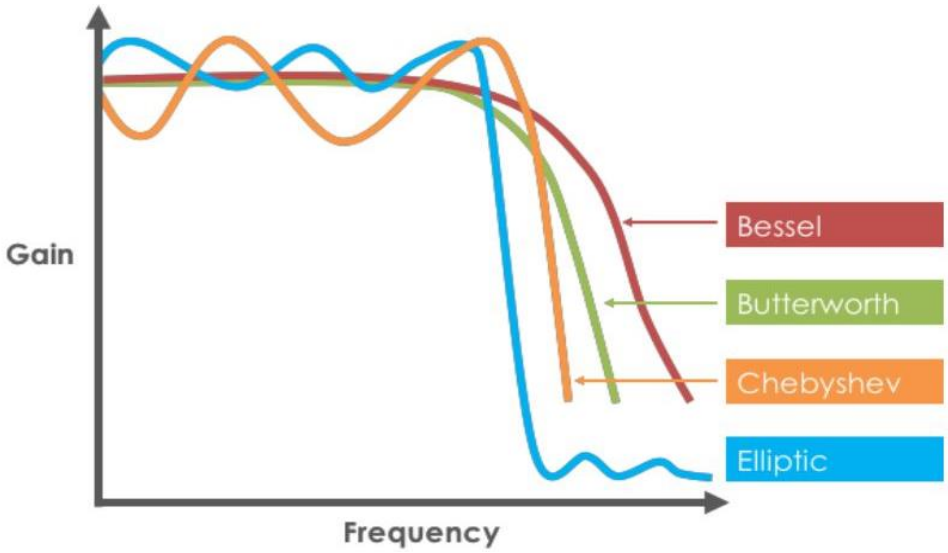


Figure 2.21: Filter design topologies (Analog devices, 2023)

Group delay of a filter refers to the variation in signal propagation time across different frequencies. Figure 2.22 depicts amplitude and group delay vs. frequency for various filter types normalized to a 1-rad bandwidth (Analog devices, 2023).

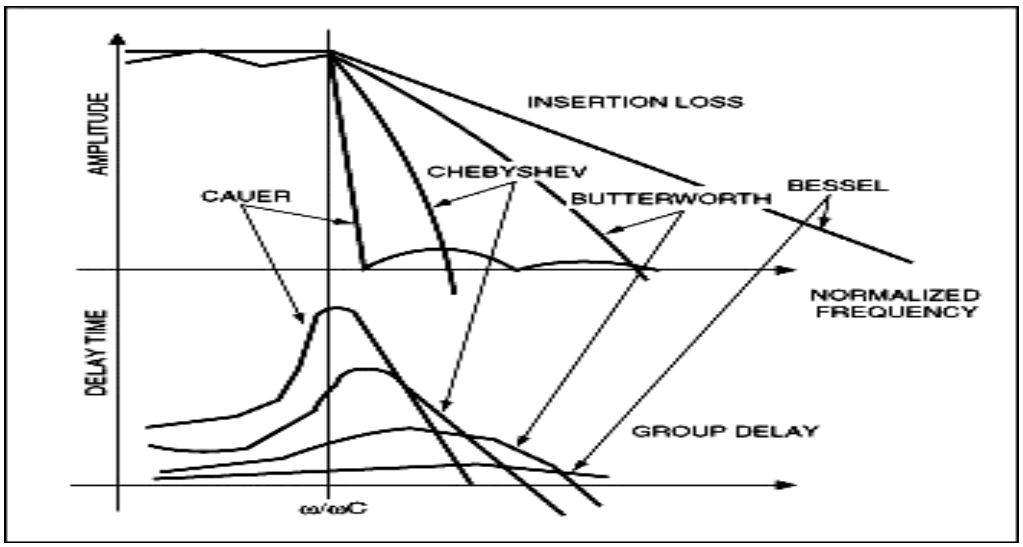


Figure 2.22: Amplitude and group delay vs. frequency for various filter types normalized to a 1-rad bandwidth (Analog Devices, 2023).

The high pass filter shown in Figure 2.23 allows frequencies above the cut-off frequency to pass while attenuating lower frequencies.

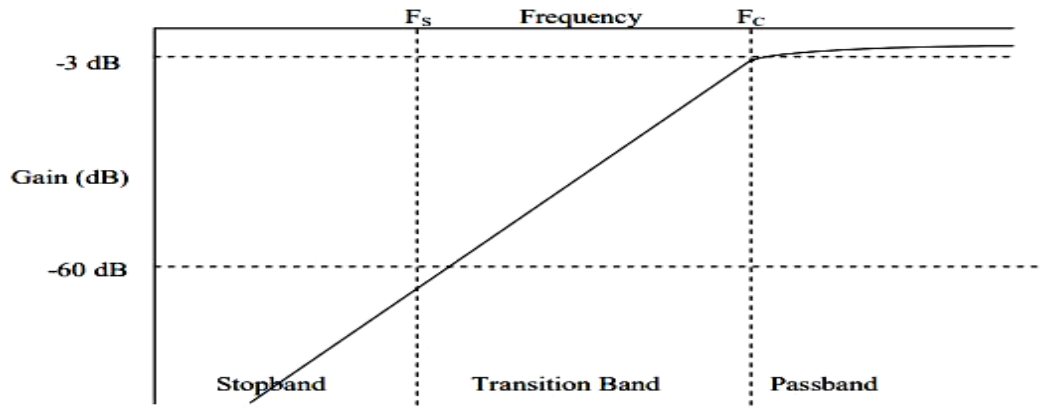


Figure 2.23: Frequency response of a high pass filter (Pozar, 2001:271)

A band pass filter restricts the frequency range of incoming signals to a particular frequency band as shown in Figure 2.24. The passband performance minimizes the degradation of the desired frequencies while attenuating signals outside the passband. The bandwidth is defined by the 3 dB drop in signal level on either side of the centre frequency. Another critical parameter specification is keeping the insertion loss or the amount of power loss across the desired frequency range to a minimum to preserve overall signal strength and improve the downconverter and satellite receiver sensitivity. A bandpass filter was implemented at different stages of the downconverter. This filter is used in the downconverter for rejecting signals outside the operating band and attenuating undesired mixer intermodulation products as explained previously. A band stop filter, also known as a notch filter, functions in the opposite direction than that of the bandpass filter by attenuating signals within a specific band and passing signals outside that range. Notch filters are popular in applications where a deep attenuation at a specific frequency or narrow frequency range is required (Pozar, 2001:271).

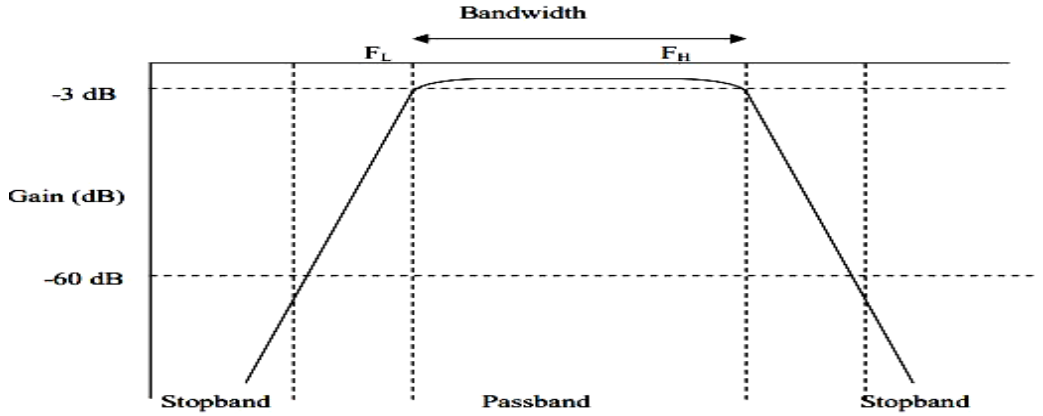


Figure 2.24: Frequency response of a bandpass filter (Pozar, 2001:271)

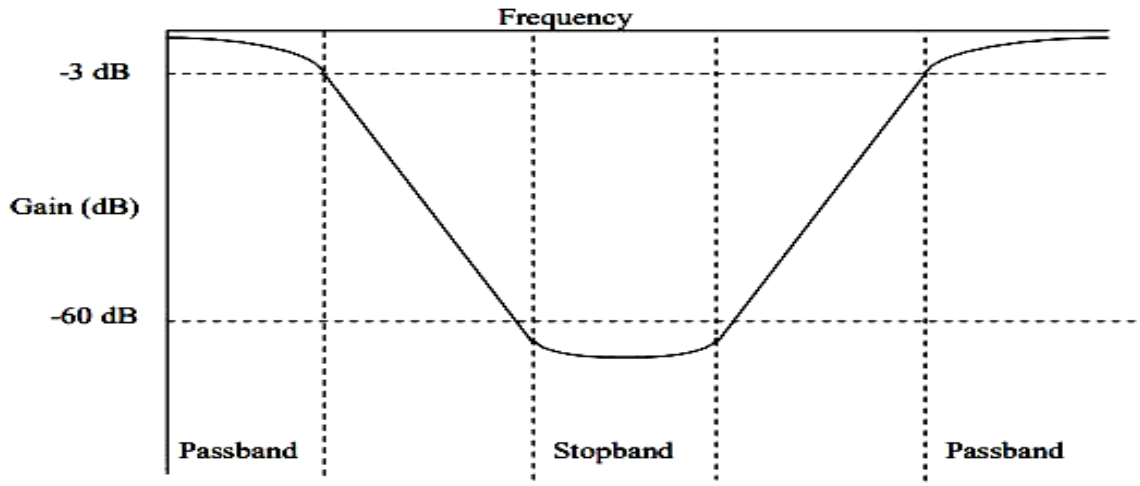


Figure 2.25: Frequency response of a bandstop filter (Pozar, 2001:271)

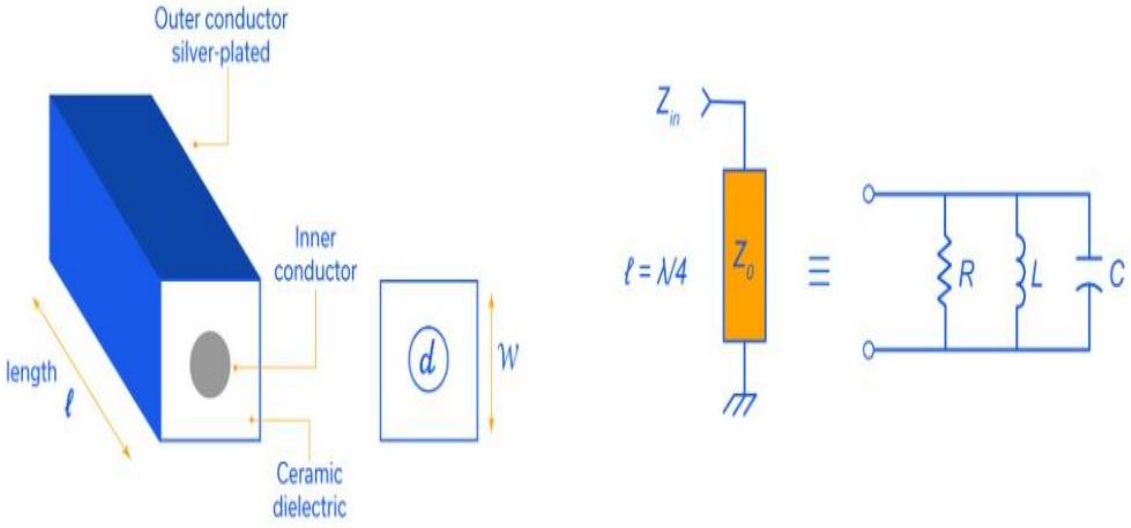
2.7.1.2 Filter Technology

Filters can be active or passive. Active filters use active components such as transistors or operational amplifiers (op-amps) in addition to resistors and capacitors except inductors to achieve desired filtering characteristics. Active filters are popular for very low frequencies applications and they provide voltage gain which passive filters cannot. In contrast, passive filters only include passive components such as resistors, capacitors, and inductors. The limitations at higher frequencies are because of parasitic capacitances and inductances, and at lower frequencies the capacitance and inductance are quite large. Careful design practices are normally employed, and hence passive filters are popularly used in high frequency RF circuits.

Filters are available as component level products which are designed to be incorporated into various electronic applications such as assembly PCB's or IC's. Filters can also be found as modular, connectorized products used in laboratory and test equipment, allowing for easy integration and reconfiguration in different setups. The choice of filter type depends on the specific requirements of the RF system and the desired signal interference rejection. In satellite applications, it mostly depends on technology, size, cost, design complexity and performance in terms of interference rejection or suppression. Several types of filter technologies covering the applicable RF band are available on the market and the vendors include Digikey, Mouser etc, as well as specific filter technology manufacturers such as Minicircuits, Murata, Echo Microwave etc. These filters are often based on the following various devices at the RF design frequency, such as low loss RF ceramic devices shown in Figure 2.26, which offer small and lightweight filters that use piezoelectric properties of ceramics for filtering. Ceramic filter products provide a frequency dependent characteristic useful for suppressing or selecting

signal content over some range of frequencies. Some devices use the piezoelectric properties of a ceramic material to achieve this end and are effectively electro-mechanical systems, whereas others use multi-layer construction techniques, incorporating inductive elements to create an integrated inductor-capacitor (LC) style filter as shown in Figure 2.27. Ceramic filters provide a good comprise between cavity and lumped element designs, by offering high performance in a small size and low cost. Ceramic filters offer high Q-factor which ensures low insertion loss and high temperature stability. Ceramic filters can be customised for specialised mounting configurations and input/output connector types, manufacturers such as Minicircuits, Echo Microwave etc offer both leaded and surface mount devices.

(a)



(b)

Figure 2.26: Ceramic filters (a) construction and (b) schematic (Minicircuits, n.d.)

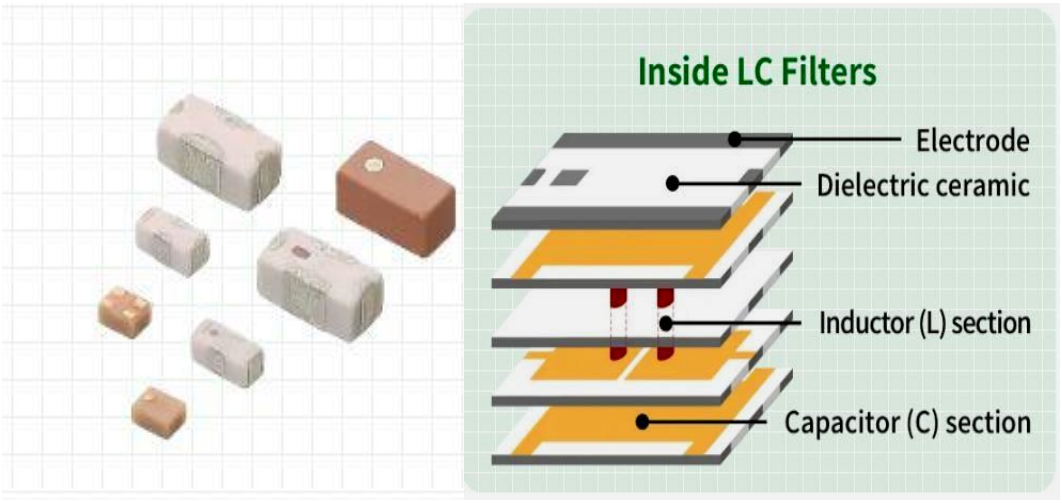


Figure 2.27: LC filters (Murata, n.d.)

Surface acoustic wave (SAW) filters are another common technology used in RF receiver applications. SAW filter uses interdigital transducers (IDT's) which consist of comb-shaped metal electrodes on a piezoelectric substrate surface to convert an input electrical signal to a acoustic wave and then back to an electrical signal. This is achieved by using an electrode to receive radio waves that propagates on the surface of a piezoelectric substrate circuit board as shown in Figure 2.28. The piezoelectric substrate vibrates and turns the radio waves into moving surface acoustic waves. The electrode only allows the surface acoustic waves that are desired to pass and then attenuate the rest. SAW bandpass filters are popularly used in RF receiver applications because of advantages such as small size, good performance in terms of low insertion loss, high frequency operation (SAW filters are limited to frequencies up to 3 GHz), low cost, and fast time to market.

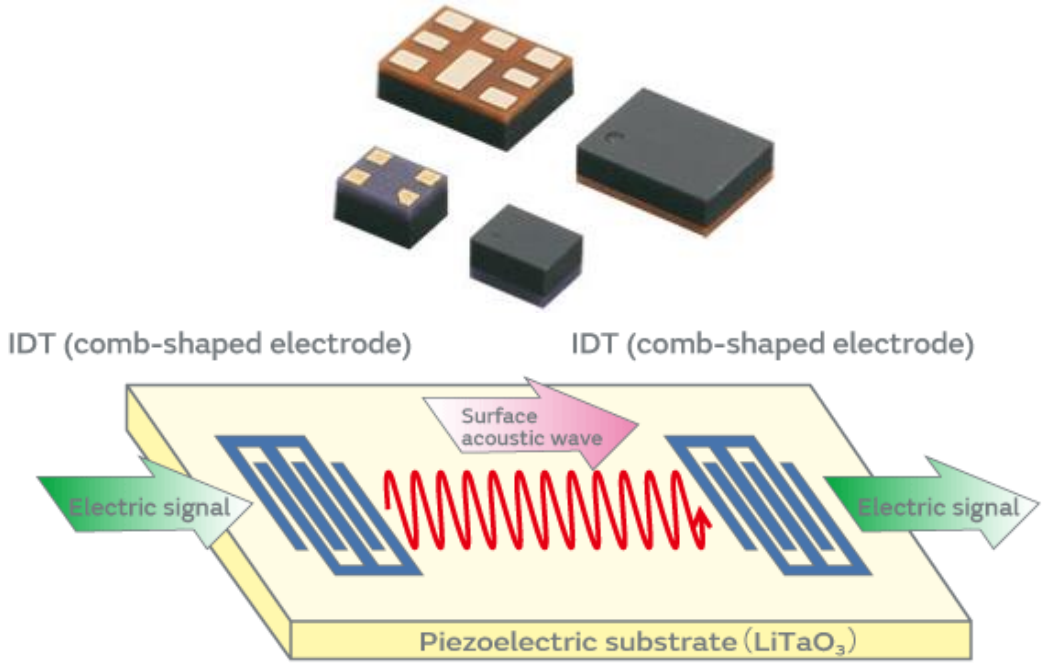


Figure 2.28: Surface acoustic wave (SAW) device (Murata, n.d.)

SAW filters exhibit a high-quality factor (Q-factor). The Q-factor indicates the sharpness of the resonance peak. The higher the Q-factor the smaller the loss in the filter which is better for filter characteristics. Figure 2.29 shows Murata's I.H.P SAW and traditional SAW filters Q characteristics comparison.

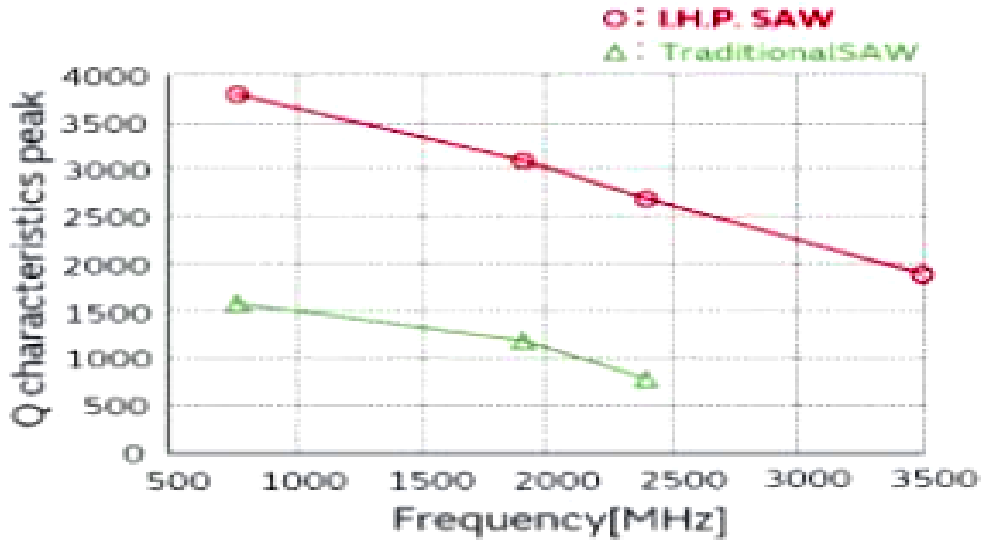


Figure 2.29: I.H.P SAW and traditional SAW filters Q characteristics (Murata, n.d.)

Other common filter technologies used in RF applications include cavity resonator filters, which use resonant cavities to achieve frequency selectivity. Cavity resonator filters are available over a wide frequency range up to 25 GHz and provide low insertion loss, high Q-factor, and narrower bandwidths than ceramic filter solutions. Cavity filters shown in Figure 2.30 are constructed using hollow metal cavities that resonate at specified frequencies. Cavity filters over good selectivity but are larger in size compared to other filter technologies. Other popular filter technologies include thin film and suspended, microstrip and waveguide filters shown in Figure 2.31 to Figure 2.33, respectively.

Figure 2.30: Cavity filters (Adams, 2022)

Figure 2.31: Thin film and substrate suspended filters (Echo Microwave, n.d.)

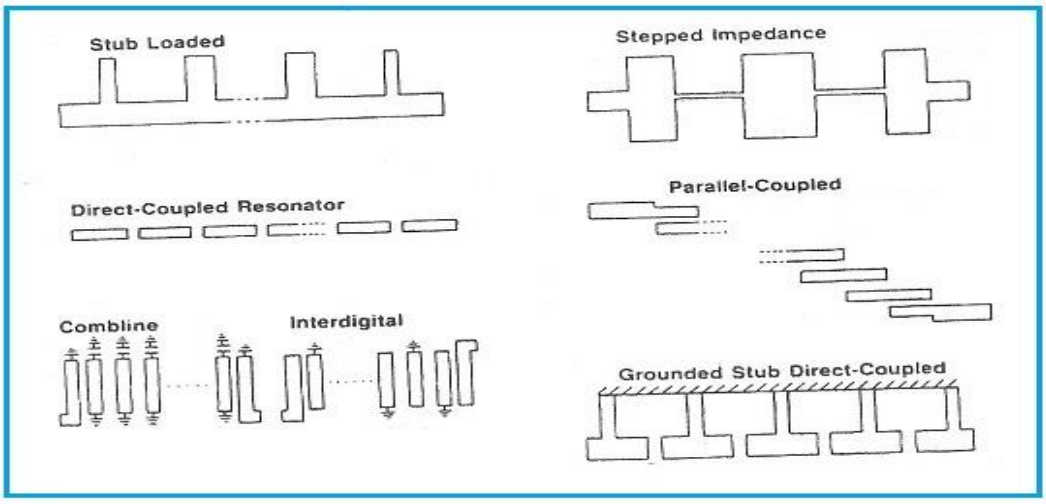


Figure 2.32: Microstrip filter configurations (RF Wireless, n.d.)

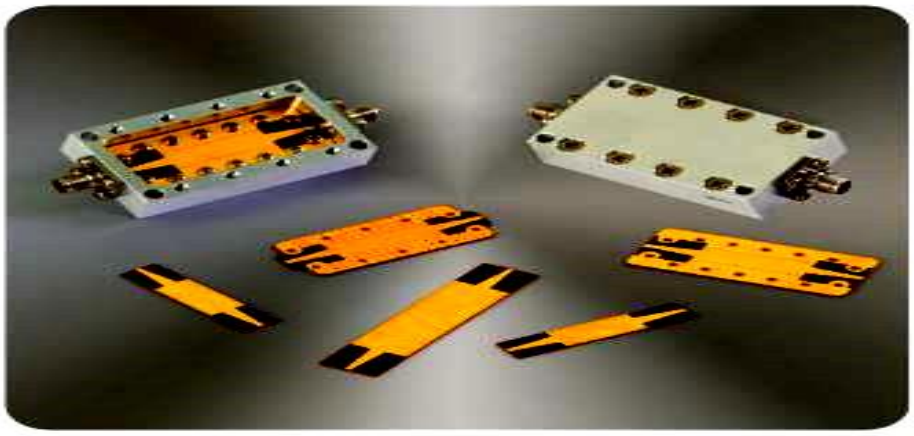


Figure 2.33: Waveguide filters (Echo Microwave, n.d.)

Table 2.7 gives a summary of the reviewed airborne filter implementation with their highlights.

Table 2.7: Spaceborne filters literature summary

Satellite Filters Analysed	Highlights
Nguenouho et al., 2017	Implementation of RF and microwave filters between 2.2 and 2.3 GHz using ceramic coaxial resonators. A radiation level test was conducted on the filter to verify the use of the metallic enclosure. The test presented a low level of radiation measured at the filter centre frequency of 2.25 GHz. The filter was also subjected to temperature cycling.
Astuti et al., 2017	Implemented a substrate integrated waveguide bandpass filter for very small aperture terminal (VSAT) transceiver station downlink. The uplink frequency spanned 5.925 - 6.425 GHz while the downlink frequency covered 3.7 - 4.2 GHz. The measured results gave an insertion loss (-S21) value of 3.871 dB and a return loss (-S11) value of 30.87 dB.
Pelliccia, et al., 2017	Miniaturized high-performance bandpass filters for satellite applications. A 2 GHz very compact input narrowband filter for mobile satellite service (MSS) applications based on high permittivity TM010 mode dielectric resonators was studied. The second filter was a broadband filter centred at 6.175 GHz. The filter had a total of 9 resonators (i.e. 5 TM mode resonators and 4 comb-line resonators) making it very compact.
Stepien, 2021	Review of SIW S-band and X-band antennas and filters for both maritime and space applications. The main advantage of substrate integrated waveguide (SIW) technology is the highest level of isolation between the beams and polarizations. This also ensures a high Q factor (> 1000) and relatively low insertion losses. The filters successfully used in X-band have a fractional bandwidth (FBW) of 8% at 3dB and FBW of 20% at 40 dB. Measured Q factors are 500 and S21 of <1 dB for the filter orders of 4 and 5.
Orecchini et al., 2023	Two switchable image-reject filters implemented in SIW technology for a Ku-band LNB downconverter CubeSat application. A 14 GHz filter response with center frequency insertion losses of 6.8 dB and 4.4 dB.

2.7.2 Amplifiers

The downconverter system employs amplifiers at various stages of the downconverter chain as shown in Figure 2.34. The downconverter amplifier function is to increase the received signal amplitude as well as to minimise the distortion and the noise added to the relatively weak received RF signal. A low-noise amplifier (LNA) is specifically required to i) amplify a very low-power RF signal fed to its input and ii) add as little noise as possible to the receiver system. Ideally, the amplifier would add no noise and would not distort the signal in any way; however, electronic devices are not ideal which makes it difficult to operate them properly in a noisy environment created also by the electronic device circuitry. An amplifier will increase the power of both the signal and the noise present at its input, but the amplifier will also introduce some additional noise. LNAs are designed to minimise that additional noise. Minimum

additional noise can be achieved choosing low-noise components, selecting the right operating points, and selecting the right circuit topologies. Minimising additional noise must balance with other amplifier design goals such as power gain and impedance matching specifications. In this case the IF amplifier tends to boost the IF signal to a level adequate for demodulation. Parameters such as gain and linearity, drives the selection of this device (Bowick, 20008) (Pozar, 2005).

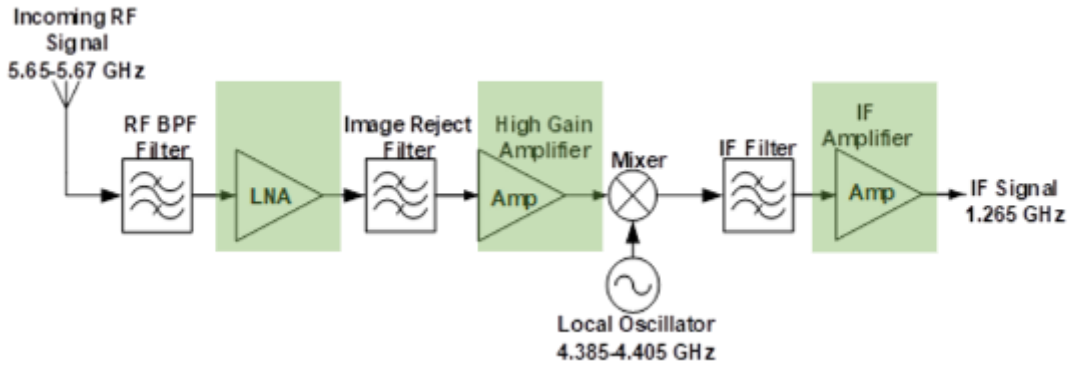


Figure 2.34: Downconverter amplifiers

2.7.2.1 Amplifier Theory and Fundamentals

Figure 2.35 shows a basic single stage amplifier. It is comprised of the active device, biasing network, input and output matching networks that in most cases are terminated with a load and a source impedance equal to the system characteristic impedance, which is usually 50 Ω. In amplifier design, the most common design considerations are the stability of an active device, power gain, circuit bandwidth, noise figure, linearity and the direct current (DC) bias.

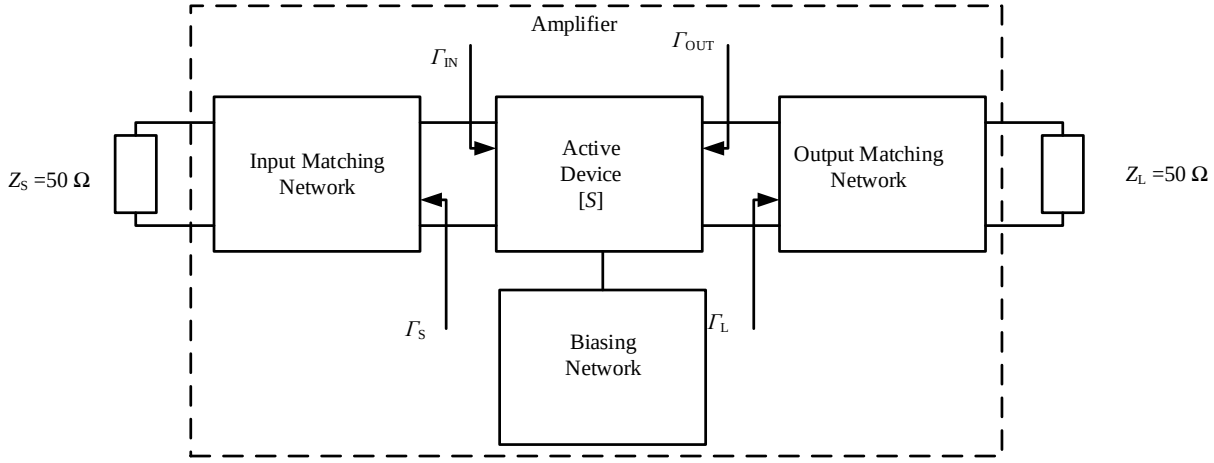


Figure 2.35: Single stage amplifier (adapted from MacPherson, 2002)

2.7.2.2 Stability of the Active Device

Stability is a measure of the amplifier's tendency towards oscillation. It is possible to predict the degree of stability of an amplifier/ transistor before using it in the design. It is important that the amplifier does not oscillate in the desired frequency range of operation. Unconditional stability allows any source and load terminations to be presented to the amplifier without the possibility of oscillation. It can be verified by using the scattering parameters generated at a defined frequency of operation. This is determined by two parameters namely the Rollet stability factor (*K*) and the magnitude of the determinant of the scattering matrix (|Δ|). The active device is said to be unconditionally stable at the bias point chosen if $K > 1$ and $|\Delta| < 1$. This entails that, any possible source and load impedance for the device can be chosen, and the amplifier would remain stable. These parameters are calculated using equation 2-5 and 2-6 respectively (MacPherson, 2002).

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \qquad 2\text{-}5$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \qquad 2\text{-}6$$

If *K* is less than 1, the active device is said to be potentially stable and will most likely oscillate with certain combinations of source and load impedance. Several approaches are considered to achieve unconditional stability:

- Connecting a resistor in series with the base of the transistor.
- Connecting a resistor in shunt with the base of the transistor.
- Connecting a resistor in series with the collector of the transistor.
- Connecting a resistor in shunt with the collector of the transistor.

Connecting a resistor in shunt with the collector of the transistor is said to be the most common used configuration because it gives a good compromise between *NF* and power gain. The first two options are not normally considered because of their poor *NF* performance (MacPherson, 2002).

2.7.2.3 Scattering Parameters

Scattering parameters or *S*-parameters are often used to characterise the two-port network description of practically all microwave and RF circuits by using the concept of normalised incident and reflected travelling waves at each network port. *Y* and *ABCD* parameters for any two-port network are determined by implementing open-circuit, short-circuit or combinations of

open and short circuit techniques. In the case of *S*-parameters, the RF devices or circuits are characterised without requiring terminal conditions or causing damage to the device under test (DUT). Instead, the network is always terminated in the characteristic impedance of the measuring system which is deemed to be 50 ohms (purely resistive) for most of the measuring systems. In addition, the 50-ohm source and load seen by the two-port network forces the DUT, if active, to be stable and not oscillate. However, such terminations can cause the active device, such as a transistor, to become unstable in the case of short circuit measuring system which in turn makes measurements impossible to carry out (Bowick, 1989) (Pozar, 2005).

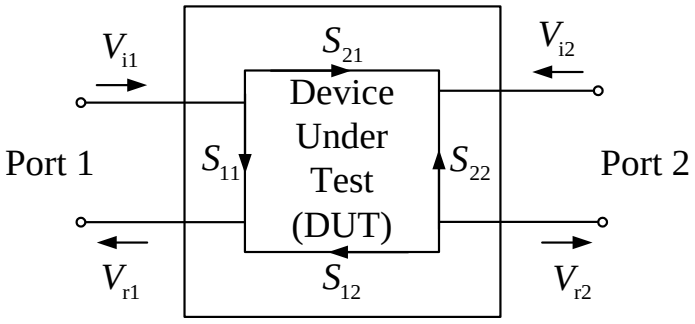


Figure 2.36: *S*-parameter representation of a two-port network (adapted from Pozar, 2005)

With respect to Figure 2.36, V_{i1} represents the power wave incident on port one and V_{i2} represents the power wave incident on port two. Part of the incident wave is transmitted as S_{21} and part is reflected as S_{11}. Consequently, S_{11} is called the input reflection coefficient and S_{21} is called the forward transmission coefficient. Similarly, for port two, the incident wave on port two is decomposed into the reflected component S_{22} and the transmitted component S_{12}. Consequently, S_{22} is called the output reflection coefficient whereas S_{12} is the reverse transmission coefficient.

The relationship between the input port and output port parameters is given by equation 2-7 and 2-8.

$$V_{r1} = S_{11}V_{i1} + S_{12}V_{i2} \qquad 2\text{-}7$$

$$V_{r2} = S_{21}V_{i1} + S_{22}V_{i2} \qquad 2\text{-}8$$

where,

$$S_{11} = \frac{V_{r1}}{V_{i1}} \Big|_{V_{i2}=0} \quad \text{2-9}$$

$$S_{12} = \frac{V_{r1}}{V_{i2}} \Big|_{V_{i1}=0} \quad \text{2-10}$$

$$S_{21} = \frac{V_{r2}}{V_{i1}} \Big|_{V_{i2}=0} \quad \text{2-11}$$

$$S_{22} = \frac{V_{r2}}{V_{i2}} \Big|_{V_{i1}=0} \quad \text{2-12}$$

and in matrix form:

$$\begin{bmatrix} V_{r1} \\ V_{r2} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_{i1} \\ V_{i2} \end{bmatrix} \quad \text{2-13}$$

S-parameters are thus widely used in the design of amplifiers and oscillators because they are easier to measure and understand. Active device manufactures typically provide the *S*-parameter information in the form of data sheets at several biasing conditions and over a wide range of frequencies (MacPherson, 2002). If the provided data is out of range of use to the designer, interpolation of the available data is usually carried using computer aided design (CAD) software in order to generate new sets of *S*-parameters. For this project, interpolation of the *S*-parameter data used to design the amplifier / LNA was implemented using Advanced Design System (ADS®).

2.7.2.4 Impedance Matching

Any unnecessary loss in a sensitive circuit, for instance the receiver front-end that is already carrying extremely weak or small signal levels cannot be tolerated. Impedance matching is often the necessary tool used for this type of circuitry to provide the maximum possible transfer of power between a source and a load and minimize the amount of standing waves. In order to avoid unwanted loss of power each device in the front-end receiver chain must be correctly matched to its load. This process relies on the use of a matching network, which transforms a load impedance to the system characteristic impedance, which is usually 50 Ω. The effectiveness of this transformation can be quantified by either the reflection coefficient, voltage standing wave ratio (VSWR) or the return loss (RL).

There are several types of matching networks used for matching, such as lumped elements (capacitors and inductors) and distributed elements (micro strip lines). Examples of lumped element matching include the L, Pi and T matching networks. The L matching network is most

widely used because of its simplicity. The common drawback however is that the quality factor (*Q*), and hence the bandwidth of this circuit cannot be specified. Pi and T matching networks are well suited for narrow-band matching network for the latter. Impedance matching networks can be designed either mathematically or graphically with the aid of Smith Chart. The Smith Chart can be described as a graphical tool useful in solving transmission line and impedance matching problems by determining the topology and component values (MacPherson, 2002).

Figure 2.37 shows a typical block diagram of an amplifier with its input and output matching networks. Reflection coefficient (Γ) is a figure of merit indicating the degree of matching; it varies between 0 and 1, for a good match $\Gamma = 0$, for a poor match $\Gamma = 1$. For maximum power transfer between the 50-ohm source and the load, the source reflection coefficient Γ_S of the input matching network must be equal to the complex conjugate of the input reflection coefficient Γ_i seen looking from the input port of the active device. Similarly, the load reflection coefficient Γ_L for the output matching network must be equal to the complex conjugate of the output reflection coefficient Γ_o seen looking from the output port of the active device.

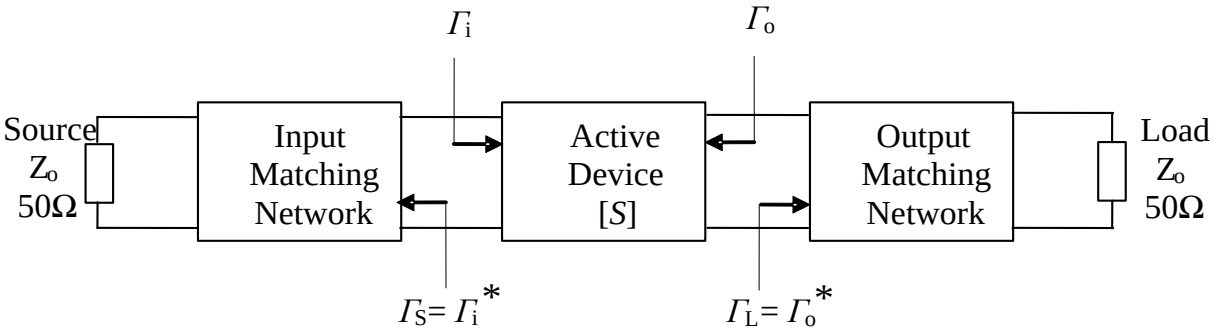


Figure 2.37: Input and output matching networks of an amplifier (adapted from MacPherson, 2002)

Table 2.8 gives a summary of the parameters that determine the degree of matching. The first case: $Z_L = Z_0$, $\Gamma = 0$, the load absorbs all the energy which means that no signals are reflected back to the source. The second case: $Z_L = 0\ \Omega$, all incident waves are reflected to the source and they are 180º out of phase. This causes the resultant sum of the waves measured across the shorted termination to be zero. And lastly, the third case: $Z_L = \infty\ \Omega$, $\Gamma = 1$, the reflected waves are equal and in phase to the incident waves which results in doubling. RL varies between 0 and ∞, for a good match RL= ∞ and poor match RL=0.

Table 2.8: Comparison of reflection coefficient (Γ), voltage standing wave ratio (*VSWR)* and return loss (RL)

Parameter	Good	Poor
Γ	0	1
VSWR	1	∞
***RL* [dB]**	∞	0

MacPherson (2002) outlined a simple design procedure used to determined possible component values for the L matching network using the Smith Chart. If the normalised load impedance lies inside the unit resistance circle, then the configuration of Figure 2.38 (a) can be used. The possible components for this configuration are series capacitor and shunt inductor or series inductor and shunt capacitor. If the normalised load impedance lies outside the unit resistance circle, then the configuration of Figure 2.38 (b) can be used. The possible components for this configuration are shunt inductor and series capacitor or shunt capacitor and series inductor. Series capacitor and shunt inductor in both the input matching and output matching is deemed to be the optimum layout for minimum component count in the design of a LNA.

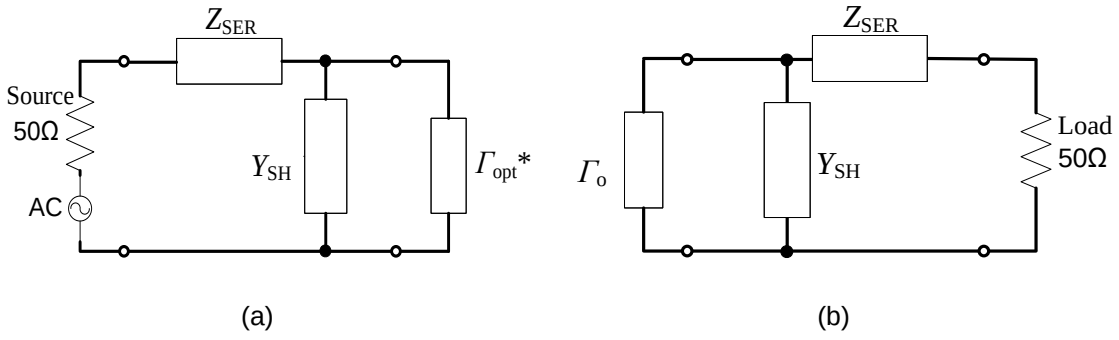


Figure 2.38: L-section matching networks (adapted from MacPherson, 2002)

2.7.2.5 Power Gain

Power gain is referred to as the ratio of power dissipated in the load (ZL) to the power delivered to the input of the two-port network as shown in Figure 2.39. This performance parameter is important because it compensates for wide variations of impedance levels existing in RF circuitry. The variation on impedance level in RF circuit causes the voltage and current gain to change simultaneously and they become meaningless but the variation in impedance does not have major effect on the power gain relative to the change in current and voltage gains. With reference to Figure 2.39 the following powers can be defined as follows:

- Power available from the source (P_{AVS}) which is determined by terminating the source with the load reflecting coefficient equal to Γ_S^*.
- The input power to the network (P_i), if the impedance presented at the input port of the network is conjugately matched to its source impedance than $P_i = P_{AVS}$.
- Power available from the network (P_{AVN}) is determined by terminating the network with a load reflection coefficient equal to Γ_O^*.
- Power delivered to the load (P_L), if the impedance presented at the output port of the network is conjugately matched to its output impedance than $P_L = P_{AVN}$.

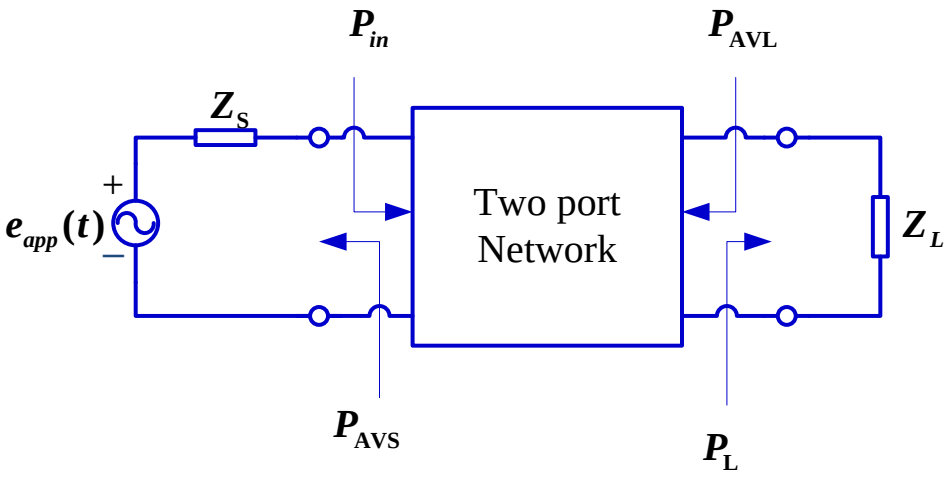


Figure 2.39: Power gain of a two-port network (adapted from MacPherson, 2002)

With reference to Figure 2.42 the following powers can be defined as follows:

- *Transducer power gain* (G_T)

The ratio of the output power that is delivered to the load by the source (P_L) to the maximum power available from the source (P_{AVS}). G_T is dependent on both Γ_L and Γ_S as shown by equation 2-14.

$$G_T = \frac{P_L}{P_{AVS}} \qquad 2\text{-}13$$

$$G_T = \frac{|S_{21}|^2\left(1-|\Gamma_L|^2\right)\left(1-|\Gamma_S|^2\right)}{\left|1-S_{11}\Gamma_S-S_{22}\Gamma_L+\Delta\Gamma_L\Gamma_S\right|^2} \qquad 2\text{-}14$$

- *Operating power gain* (G_P)

The ratio of the power delivered to the load (P_L) to the power input from the network (P_i). G_P is independent of Γ_S.

$$G_P = \frac{P_L}{P_i} \qquad 2\text{-}15$$

- *Available power gain* (G_A)

The ratio of power available from the network P_{AVN} to the power available from the source P_{AVS}. Available power gain is considered when designing amplifiers for low noise application. G_A is independent of Γ_L.

$$G_A = \frac{P_{AVN}}{P_{AVS}} \qquad 2\text{-}16$$

$$G_A = \frac{|S_{21}|^2\left(1-|\Gamma_S|^2\right)}{\left(1-\left|\frac{S_{22}-\Delta\Gamma_S}{1-S_{11}\Gamma_S}\right|^2\right)\left|1-S_{11}\Gamma_S\right|^2} \qquad 2\text{-}17$$

- *Maximum available gain* ($G_{A\,(max)}$)

A figure of merit for the transistor, which indicates the maximum theoretical power gain expected from the active device when it is conjugately matched to its source and load impedance (MacPherson, 2002).

$$G_{A\,(max)} = G_T = G_P \qquad 2\text{-}18$$

2.7.2.6 Noise Figure

Noise is any unwanted form of energy interfering with the reception and reproduction of wanted signals. Noise in any dynamic electrical or electronic system can be categorised into external noise and internal noise. External noise is generated outside the receiver circuitry and may take the form of atmospheric noise (caused by the immense energy of the sun), solar noise, cosmic noise and man-made noise. Internal noise occurs inside the receiver which may be something minor as the thermal noise (associated with carbon resistor) or shot noise often called Schottky noise (common to the particle-like nature of the charge carriers) and flicker noise. It is very important that a receiver is able to process low level signals in the presence of noise. Noise Figure (*NF*) or Noise Factor (*F*) and power gain are the most significant performance parameters of a amplifier / LNA (Bowick, 2008).

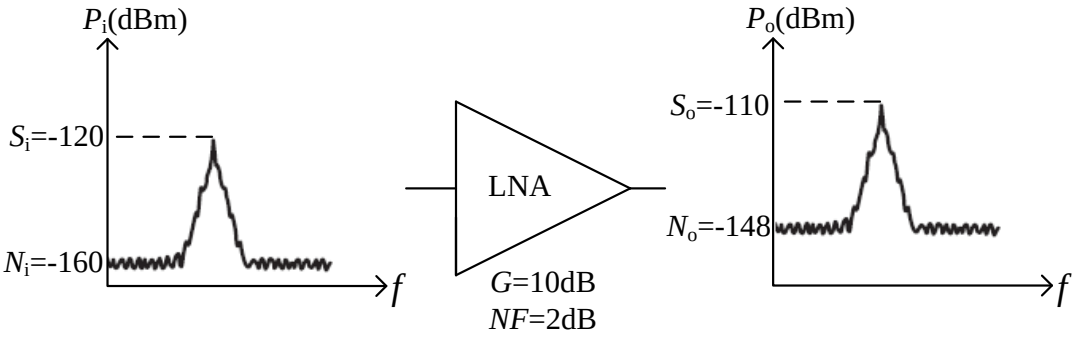


Figure 2.40: Noise figure concept of two port network (adapted from Agilent Technologies, 2010:6)

NF may be defined as the ratio of signal-to-noise ratio (SNR_o) at the output to the signal-to-noise ratio (SNR_i) at the input of any two-port network. Figure 2.40. shows a typical signal, with noise levels independent of the frequency at the LNA's input and at its output ports. The signal illustrated at the input port of the LNA is 40 dB above the noise floor. The amplifier has increased the signal and the noise level at the output of the network by 10 dB and added its own noise level of 2 dB. Thus, the noise level rises more than the signal level due to added noise by the LNA. This relative increase in noise level is expressed by the amplifier NF.

Mathematically *F* is given by Equation 2-19

$$F = \frac{SNR_{\mathrm{i}}}{SNR_{\mathrm{o}}} = \frac{S_{\mathrm{i}}/N_{\mathrm{i}}}{S_{\mathrm{o}}/N_{\mathrm{o}}} \qquad 2\text{-}19$$

Whereas *NF* is a logarithmic value, given by the *F* expressed in dB and is given by Equation 2-20.

$$NF = 10\log(F)\ \mathrm{dB} \qquad 2\text{-}20$$

The *NF* of the receiver system may be improved by either increasing the amount of power the receiving antenna is intercepting, which means increased antenna size which can be costly, or improving the noise performance of the receiver front-end hence the design for minimum *NF*. Friis's formula is used to calculate the total noise factor of a cascade of stages, each with its own noise factor and power gain, assuming that the impedances are matched at each stage. The total noise factor can then be used to calculate the total noise figure. According to Friiss' formula, the noise factor of the overall receiver system is given by equation 2-21.

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots\ldots \qquad 2\text{-}21$$

In Equation 2-21, G_1 and G_2 are the gains of the first and second stage respectively. F_{i} represents the *F* of each stage where, *i* = 1, 2, 3 as shown in Figure 2.41.

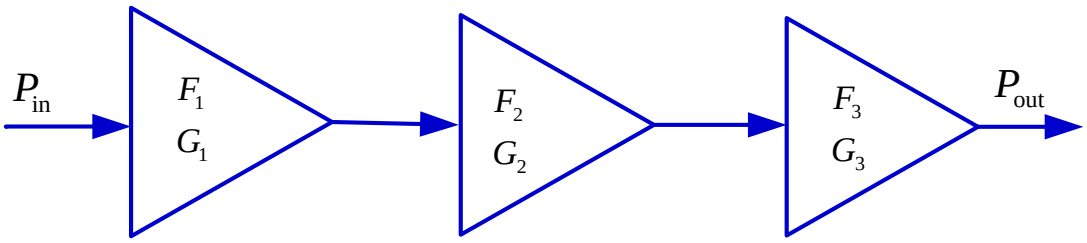


Figure 2.41: A cascade system

A careful analysis of Equation 2-21 reveals that the major contribution to the *F* of the overall receiver system is the *F* of the first stage. If subsequent stages following the first amplifier have a high cumulative *F*, more gain is required to compensate for the *F* of those stages, thus providing the lowest system noise. The LNA is always placed at the front end of the receiver system therefore it must be designed or selected for minimum *NF* as much as possible.

2.7.2.7 Linearity

Linearity is a measure of how well the amplifier can reproduce a RF signal at its input port. A transistor has non-linear characteristics, which enables it to add or amplify signals; however,

these characteristics can lead to undesired effects such as gain compression and the generation of unwanted frequency components. This may result in signal distortion and possible interference. The 1 dB compression point (1P1dB) and the third order intercept point (TOI) are the performance parameters that are used to determine the linearity of an amplifier.

2.7.2.7.1 1dB Compression Point

The 1 dB compression point ($1P_{1dB}$), as indicated in Figure 2.42, is a non-linear performance parameter of the amplifier / LNA, which gives an indication of the maximum power that the amplifier is able to deliver to the load. As the power of the input signal is increased beyond the amplifier's linear region of operation, the point referred to as the P_{1dB} point is reached where the amplifier is driven into compression. This occurs at the point where the system gain has dropped to 1 dB below the theoretical linear gain response curve.

The OP_{1dB} is determined by Equation 2-22.

$$OP_{1dB} = IP_{1dB} + G_A \text{ dBm} \qquad 2\text{-}22$$

The dynamic range (DR) as indicated in Figure 2.42 is defined as the linear operating region for the amplifier between the noise floor and the 1 dB compression point.

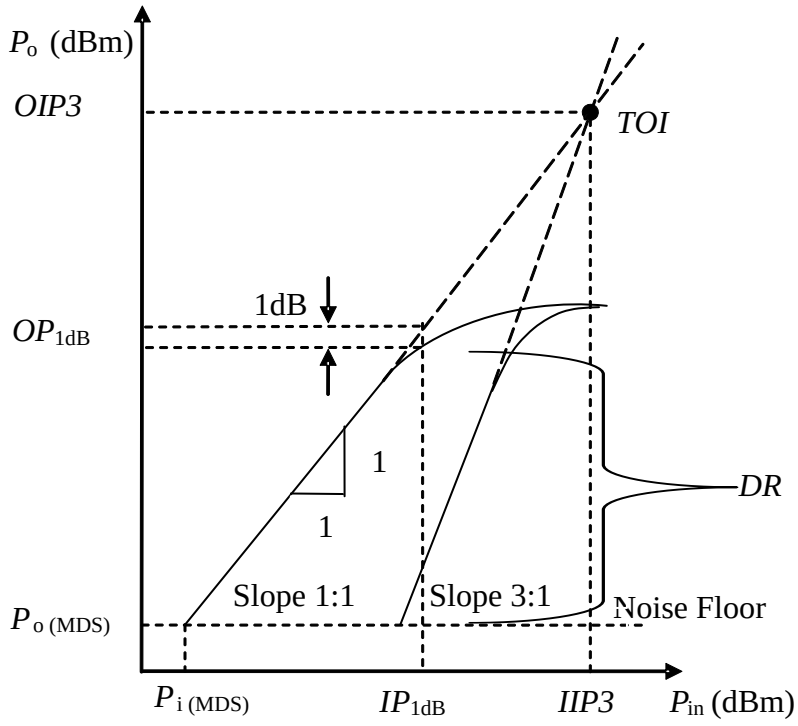


Figure 2.42: Third order intercept point, 1 dB compression and dynamic range (adapted from McPherson & Whaits, 2007:6.5)

2.7.2.7.2 Third Order Intercept Point

The output third order intercept, another non-linear performance parameter of an amplifier, is a figure of merit indicating the linearity of the amplifier. It indicates the theoretical point where the linear gain response would intersect with the third order product. The output third order intercept is calculated using Equation 2-23.

$$OIP3 = P_{out} + \frac{P_{out} - P_{3rd}}{2} \text{ dBm} \qquad 2\text{-}23$$

Figure 2.43 shows the third order intermodulation products 2f1−f2 and 2f2−f1 which are unwanted harmonics generated by the non-linear behavior of the active device and occurs when two or more signals with different frequencies are fed to an amplifier. Consequently, these signals can fall in the passband and cause distortion to the required signal. However, these intermodulation products need to be accounted for as they define the linearity of the system. The amplitude difference between the fundamental tone and the third order intermodulation tone is called the third order intermodulation distortion. For every 1 dB increase in the fundamental tone, the third order tone is increased by 3 dB and the point where the 3rd order intermodulation products reach the same amplitude as the fundamental tones is referred to as the third order intercept point (Pozar: 2012:514).

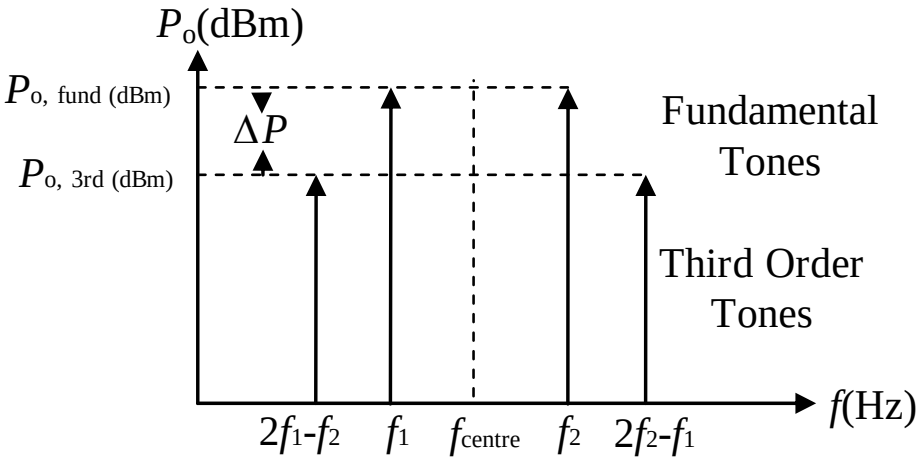


Figure 2.43: Third order intercept point (adapted from McPherson & Whaits, 2007:6.5)

2.7.2.8 Amplifier Design

Depending on which of the performance parameters is the most important, a design method can be chosen either for maximum available gain (MAG) or Low NF or trade-off design between low NF and MAG. Design trade-offs allow designers to obtain the best possible performance from a particular device.

An excellent amplifier / LNA must exhibit the following parameters:

- Low *NF*
- High *power gain*
- High OP_{1dB}
- High OP_{IP3}
- Unconditional stability
- Good input and output return loss
- Low DC power consumption

NF and power gain are conflicting performance parameters and cannot be attained simultaneously, thus a trade-off between these two performance parameters must be made for the optimum performance of the amplifier. In order to obtain the listed parameters without degrading the overall amplifier performance, the designer must take careful precautions like for instance making sure the circuit is properly grounded, as well as designing for minimum component count in order to reduce cost and size for the amplifier. Some recommendations are drawn towards the end of this work in order to eradicate the degrading factors of achieving these parameters. Figure 2.44 depicts amplifier design options with their comparative summary in Table 2.9 highlighting the advantages and disadvantages of each design option. Table 2.10 gives a summary of some of the airborne amplifiers reviewed.

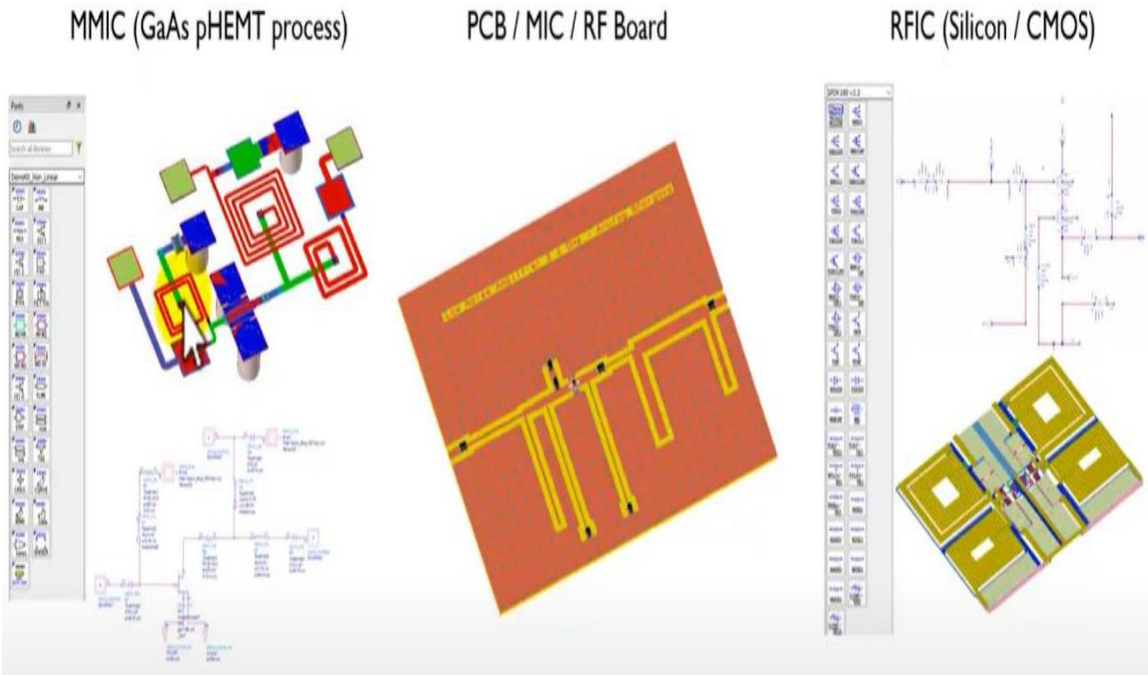


Figure 2.44: Amplifier design options (adapted from Bhargava, 2020)

Table 2.9: Comparison and summary of amplifier design options (adapted from Bhargava, 2020)

Amplifier Design Process	Advantages	Disadvantages
MMIC (GaAs pHEMT)	• Good performance and mass production friendly • Less size (few microns) • Can be designed up to very high frequencies (>30 GHz) • Octave bandwidth possible	• Cost is prohibitive if large quantities are not needed • Performance tuning not possible after fabrication
PCB/MIC/RF Board	• Good performance and low cost • Decent performance up to Ku-band (~18 GHz) • Easy tuning after fabrication	• Octave bandwidth matching very difficult • Large physical size (compared to MMIC/RFIC)
RFIC (Silicon/CMOS)	• Decent performance and mass production friendly • Less size (few microns) and can be integrated into SoC's	• Inferior noise figure compared to GaAs due to Silicon • Cost is prohibitive if large quantities are not needed • Performance tuning not possible after fabrication

Table 2.10: Spaceborne amplifiers reviewed

Amplifiers Reviewed	Highlights
Chang et al.,2005	Ka-band LNA module with 1.9 dB NF for communications satellite payload. The noise figure is 1.9 dB and gain 33.3 dB. The mass of the module is 94 g. Two low noise amplifier MMIC chips were fabricated using 0.15 /spl mu/m GaAs pHEMT process. MMIC design included.
Kauvi, 2011	COTS amplifier for an ultra-high frequency (UHF) CubeSat receiver.
Lovascio et al.,2019	Design of COTS-Based RF receiver for Cubesat applications. Two cascaded GaAs pHEMT MMIC low noise amplifiers (LNAs). Each selected LNA has about 17 dB gain and 0.92 dB noise figure within the 2025 - 2110 MHz frequency band.

2.7.3 Mixer

The Downconverter system consist of a single mixer stage as shown in Figure 2.45. All heterodyne receiver systems depend on a frequency mixer to enable the up or down frequency conversion of RF signals to an IF signal by multiplying the incoming RF signal with a locally generated carrier frequency from the local oscillator. A mixer is basically a nonlinear device based on different semiconductor devices, such as diodes and field effect transistors (FETs). In addition to the desired output frequency IF signal, mixers produce many other output frequencies at both the sum and difference, due to the nonlinear mixing, or intermodulation of the input signal (RF) frequency and the LO signal frequency as shown in Figure 2.46.

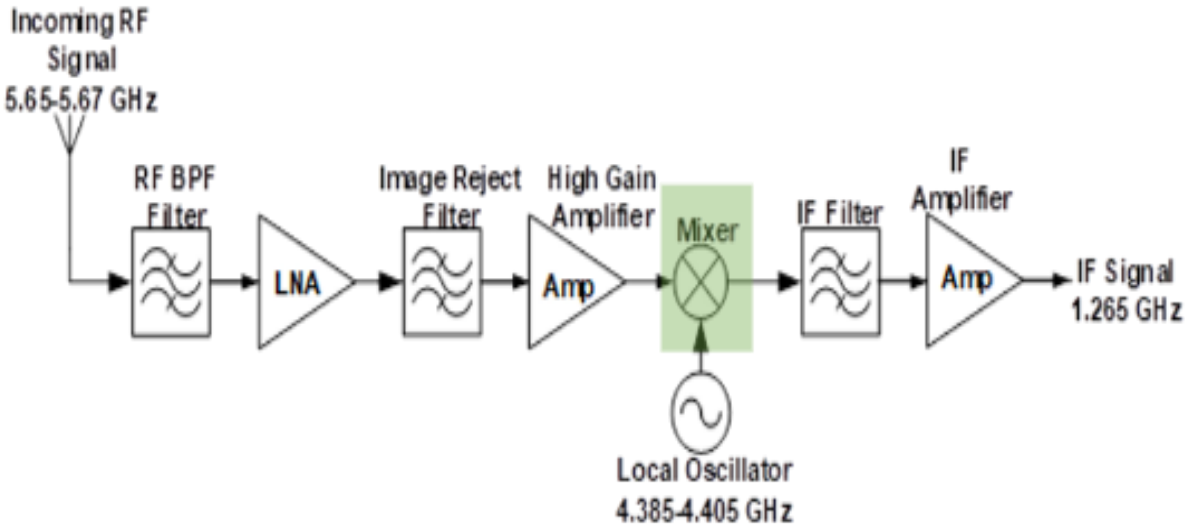


Figure 2.45: Downconverter mixer

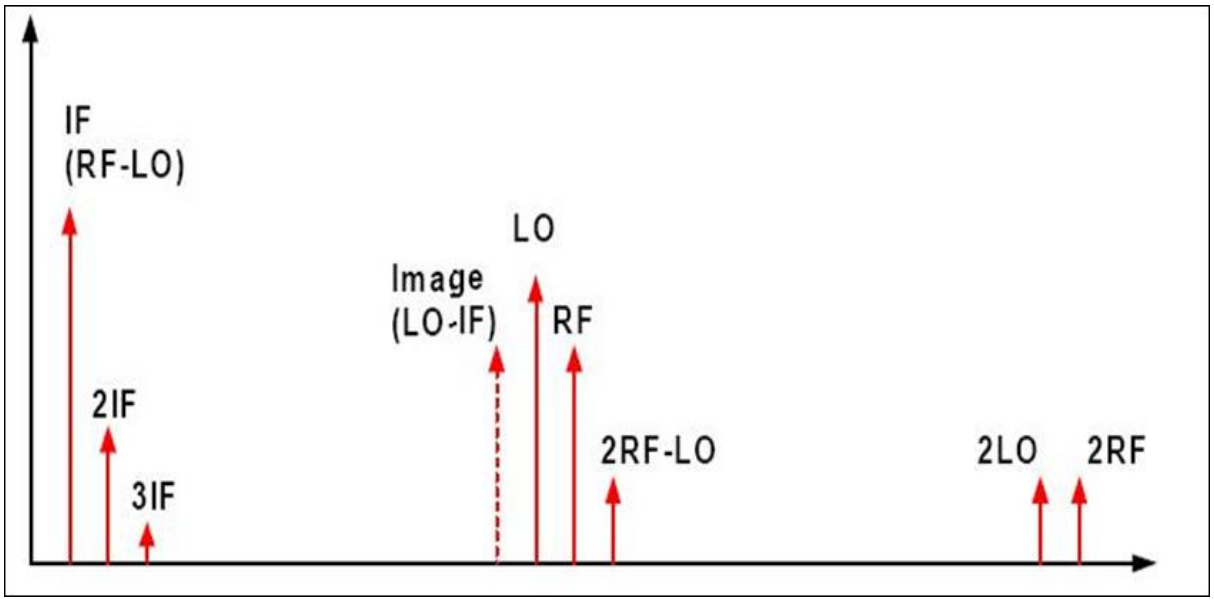


Figure 2.46: Mixer spectral output

Most mixers can be used to frequency translate, either as up converters or as down converters as shown in Figure 2.47. But not at all cases, careful attention to a particular mixer because it may only go one way or the other. Because the mixing function is inherently nonlinear, achieving good linearity is very important. Paying close attention to the third order intercept and the 1 dB compression point will help to minimise signal distortion. Figure 2.47 depicts a circuit symbol of a typical diode mixer, clearly indicating the input and output frequencies of the mixer (Bowick, 2008:191; Minicircuits ,n.d; Faria et al., 2011:24).

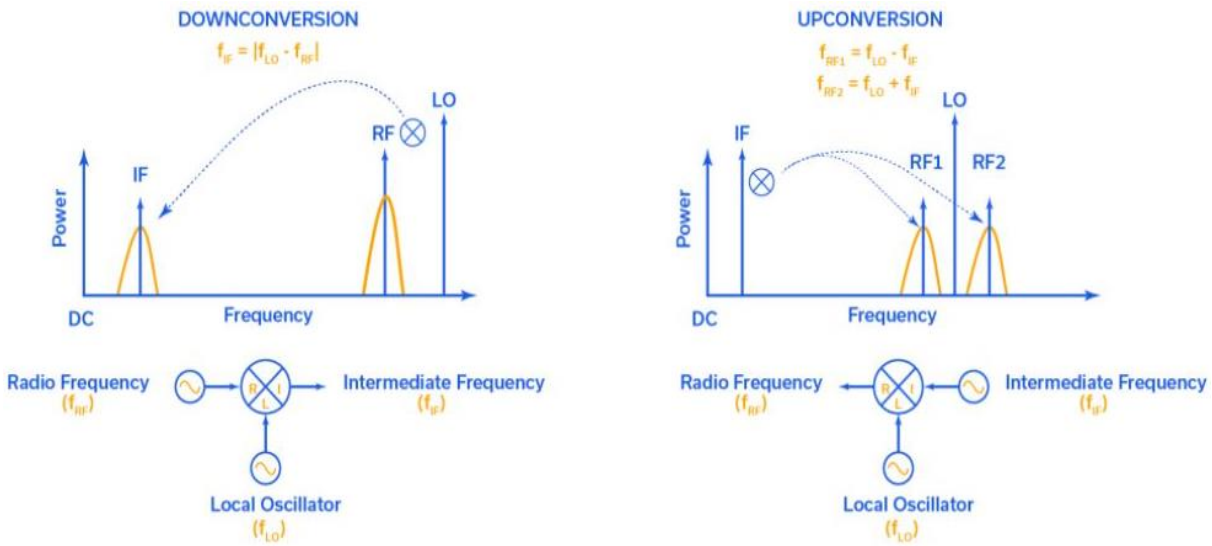


Figure 2.47: Radio frequency mixer schematic and down conversion and up conversion (Cox, 2022)

Mixers are categorized by how much conversion gain or loss, distortion, and noise they introduce during the frequency translation. Conversion loss defines the ratio of the input power to the output power of the mixer. In addition, isolation of an un-converted signal between any two of the mixer ports, P1dB and OP1dB are always defined at the input to the mixer unlike at the output in an amplifier design.

Dynamic range, bandwidth and cost are some of the crucial parameters to consider in choosing or specifying a mixer for a certain application. FET mixers normally have higher IP3 than diode mixers for a given LO level but generally operate over narrow bands than diode mixers. Dual FET quad mixers have wider bandwidth than single quad mixers but may need more LO power and active FET mixers need external DC bias, which can be a source of concern if the bias is not filtered properly. According to Faria *et al*. (2011: 24), the first steps in selecting the right mixer is to first consider the physical interface (connectorized or surface mount), the frequency plan and the LO level. While mixers play a critical role of moving signals to the proper frequency range, they can also be contributors for noise into the desired signal. Filtering plays a key role for reducing the effects created by unwanted mixer products.

Mixer technology varies widely such as passive diode ring mixers which have very good linearity, and other desirable characteristics which requires large levels of LO power, to active mixers requiring low level LO power, and typically having lower performance. The benefit of active mixers is that they offer conversion gain, as well as the mixing function; and they also offer generally easy to drive LO. All these aspects can be missing on passive diode-based mixers. In selecting a receive mixer, one must consider the conversion loss or gain, noise figure, linearity, as well as other parameters such as LO to RF isolation and the impact all these specifications have on the overall receiver performance as summarised in Table 2.11. a double balanced passive mixer was chosen for the downconverter system in this research.

Table 2.11: Mixer topologies comparison summary (adapted from Cox, 2022)

Parameter	Unbalanced	Balanced		
		Single	Double	Tripple
Inherent Isolation	None	RF or LO	RF and LO	
Filtering Required	Yes	Yes	No	No
Broadband	No	No	Yes	Yes
LO level Required?	Lowest	Lower	Greater	Greatest
Linearity	Worst	Worse	Better	Best
Spurs	Worst	Worse	Better	Best
LO AM Suppress?	No	Yes	Yes	Yes
Cost	Lowest	Lower	Greater	Greatest
Complexity	Lowest	Lower	Greater	Greatest

2.7.4 Local Oscillator (LO)

Almost all RF and microwave communication systems require a local oscillator driving a mixer or modulator, which up-converts the baseband signal carrying information to a RF signal that can be transmitted. In receivers the RF signal is down converted to an IF using the reverse process. The local oscillator (LO) is critical because it provides the signal that drives the rest of the RF signal chain. The Downconverter system employs a local oscillator highlighted in Figure 2.48. Down conversion is achieved by mixing the incoming RF signal with a stable carrier signal generated from a LO. According to Bowick (2008), there are three main types of LO that can be used for the downconverter, which are:

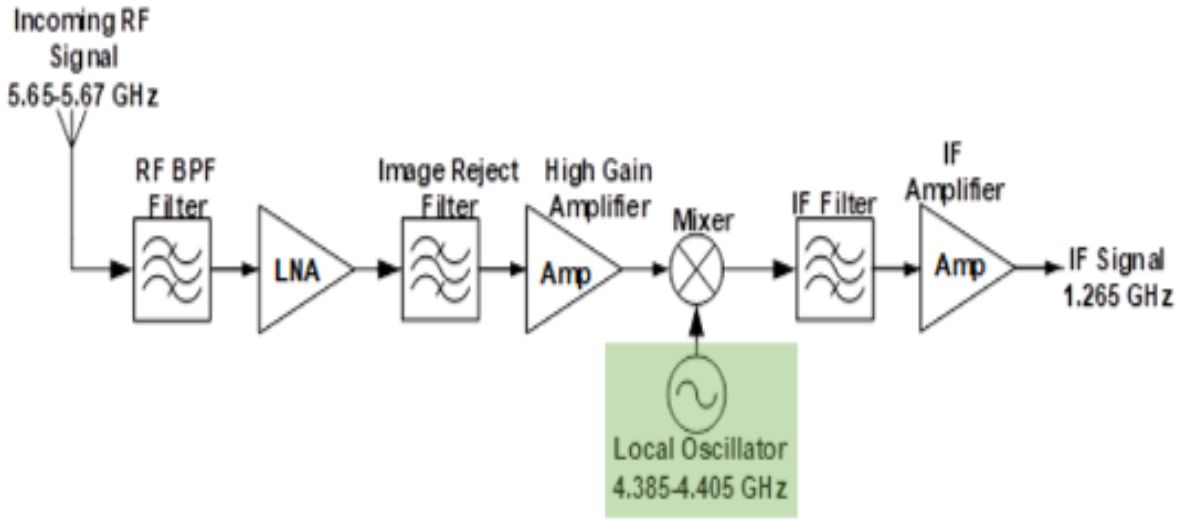


Figure 2.48: Downconverter local oscillator

2.7.4.1 Dielectric Resonant Oscillator (DRO) LO

The downconverter's conversion oscillator frequency is determined by a free running oscillator, which frequency determining element is a piece of feroceramic material referred to as a puck.

2.7.4.2 External Referenced Phase Locked LO

The downconverter's conversion oscillator frequency is determined by a reference oscillator located outside of the downconverter. This reference frequency in most cases is 10 MHz.

Normally, a PLL is preferably chosen to generate the downconverter's LO signal, because it is easy to implement and can provide a stable and low phase noise LO signal. The LO must be able to deliver the required signal, with output power levels adequate to drive the mixer.

2.7.4.3 The Phase Locked Loop (PLL) LO

The downconverter's conversion oscillator frequency is determined by an internal located temperature compensated crystal oscillator and a digital phase locking circuit. PLL categories include: a linear PLL (LPLL) or analog PLL, in which a linear element is used as a phase detector, whereas the loop filter and VCO are analog elements. A digital PLL (DPLL) is where a digital phase detector is used and everything else is analog. All-digital PLL (ADPLL) is built exclusively digitally without any passive components or linear elements and the software PLL (ADPLL) is developed in the software domain. Most of the PLL's in the market are analog PLL's, hence the focus is on analog PLL's in this research, as depicted in Figure 2.49—which illustrates a basic block diagram of the PLL synthesizer operation. A PLL basically takes a low frequency reference signal and multiplies it up to a high frequency output signal. This high frequency signal comes from a VCO. The higher frequency signal is divided down, compared

to the reference and then the frequency of the VCO is adjusted to match the desired multiples of the reference signal. It is essentially a standard negative feedback control loop where the VCO output frequency is divided, compared and adjusted to maintain lock (adapted from Mike Curtin and Paul O'Brien, 1999).

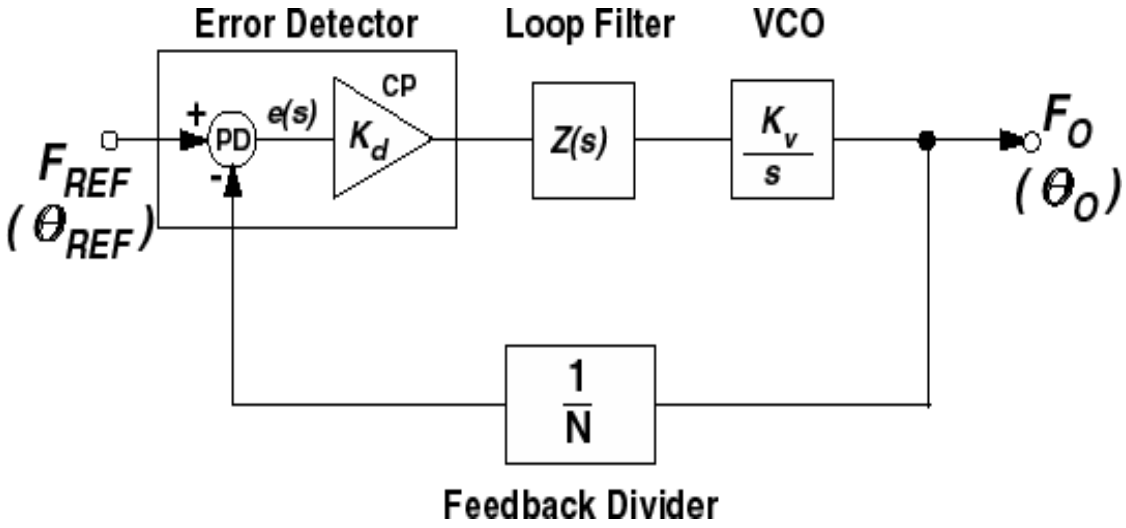


Figure 2.49: Basic PLL model (adapted from Mike Curtin and Paul O'Brien, 1999)

A closed loop feedback system is implemented to accurately control the voltage, and hence the VCO frequency. A PLL uses a reference frequency (from a crystal oscillator), together with feedback dividers, to compare the reference frequency with a feedback frequency and implement closed loop control of the VCO voltage. A phase frequency detector (PFD) compares the reference and feedback frequencies and outputs a steady DC tuning voltage to lock the phase locked loop.

The VCO frequency is divided down to a suitable frequency where it can be compared with the reference frequency and then using some extra circuitry, in this case using a charge pump which is used to generate current pulses. The current pulses are then integrated in an external low pass filter, and the resulting voltage is fed to control the VCO. As a result, any drift that may occur on the VCO due to temperature, aging or any effect like that is accounted for. When the reference and feedback counters are in alignment, the PLL is locked. The PFD is a critical part of the PLL, which is the circuit that compares the reference and the feedback dividers. The use of a low frequency crystal reference means the frequency error of the output frequency is reasonably low (adapted from Mike Curtin and Paul O'Brien, 1999). The following PLL components are discussed in details:

2.7.4.3.1 Frequency Reference

A low frequency and highly stable reference signal is required for the PLL system. The following are few popular techniques and technology used to generate the PLL reference signal normally below 100 MHz depending on application. The downconverter PLL requires a 10 MHz reference signal. The quartz crystals oscillate at a particular frequency and its size and cut (shape) determine the frequency of the oscillation. Very useful for fixed, and low frequency applications. There are a few modifications made to the quartz crystal oscillators to make up different quartz crystal oscillators which include:

2.7.4.3.1.1 Crystal Oscillator (XO)

A basic XO requires external voltage and external capacitance. It's cheap and used in low-cost applications. The key specification for XO's is frequency accuracy (expressed in parts per million, ppm), and drift over temperature can be problematic.

2.7.4.3.1.2 Voltage Controlled Crystal Oscillator (VCXO)

Crystal oscillator with frequency compensation circuitry, usually a variable capacitance diode (varactor), operating in forward bias. This requires a control circuit to compensate for variations over temperature suffered by XO.

2.7.4.3.1.3 Temperature Compensated Crystal Oscillator (TCXO)

Little more expensive than the first two. Uses a temperature sensitive circuit to compensate for temperature changes. Correct the inherent temperature drift that occurs with XO's.

2.7.4.3.1.4 Oven Controlled Crystal Oscillator (OCXO)

OCXO is the most expensive because of additional circuitries and consumes lot of power. A self-contained oven heats the crystal to a known frequency, essentially maintaining perfect frequencies because the temperature is always the same.

Limitations of XO's include:

- Low frequency: XO's are generally unavailable above 200 MHz.
- Drift with temperature, due to change in size over temperature. Can be corrected by additional circuitry.
- Tuning: Crystals inherently have a very high quality (Q) factor, compared to a LC resonant circuit. Low Q/high bandwidth and high Q/ low bandwidth.

- Tuning circuitry allows frequency tuning in few parts per million. Generally unsuited for local oscillators which must cover over 10's of MHz. For this reason, crystals are used as fixed low frequency clocks, or frequency references for PLL's.

2.7.4.3.2 Voltage Controlled Oscillator (VCO)

Generally, an oscillator is a nonlinear circuit that convert DC power to an AC waveform. A solid state-oscillator uses an active device, such as a field effect transistor (FET), bipolar junction transistor (BJT) or miniature monolithic integrated circuit (MMIC) in conjunction with a resonator circuit to produce a steady-state RF signal. Figure 2.50 shows another type of oscillator called the voltage-controlled oscillator (VCO), used for higher frequencies. For higher frequencies applications, it is useful to model the active element as a negative resistance and to apply resonant circuits at the desired frequency of operation. An oscillator can be modelled as the combination of an amplifier with a frequency dependant forward loop transfer function $G(j\omega)$, and a frequency dependant feedback loop transfer function $H(j\omega)$.

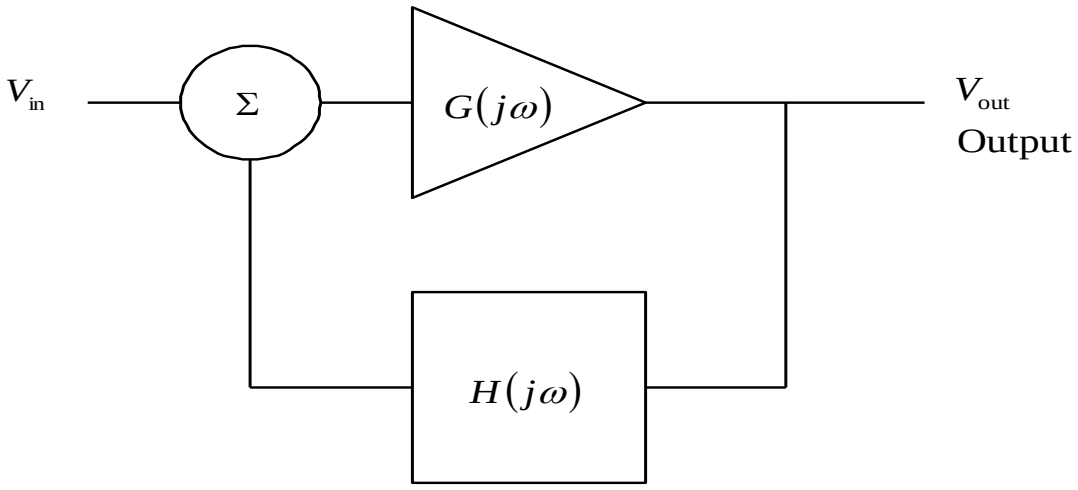


Figure 2.50: Block diagram of the VCO

The output signal from the system is given by Equation 2-24.

$$V_{out} = \frac{V_{in}G(j\omega)}{1 - H(j\omega)G(j\omega)} \text{ Volts} \qquad 2\text{-}24$$

The general expression for the transfer function is given by Equation 2-25. The system will oscillate when it approaches unity and when the total loop phase shift is equal to 0° or 360° provided there is enough sufficient gain margin at this frequency for the oscillator to start.

$$\frac{V_{out}}{V_{in}} = \frac{G}{(1 - HG)} \qquad 2\text{-}25$$

Apart from the cost, size and power consumption, another important parameter that has been actively investigated in oscillator design is the phase noise. Phase noise is used to specify the short-term stability of an oscillator and is influenced by the loaded Q of the resonator, noise sources inside the active device and noise modulated onto the power supply. Oscillator phase noise can be effectively reduced by incorporating high Q resonators. VCO phase noise typically depends on the Q factor of the resonant circuit. According to Leeson's equation: Higher Q = higher performance. But, higher Q tends to have lower frequency. In practice this means that trade-offs of frequency range verse noise are made for the application.

Leeson's Equation 2-26 is used to predict the noise elements in a VCO (Curtin and O'Brien, 1999):

$$L_{PM} \cong 10\log\left[\frac{FkT}{A}.\frac{1}{8Q_L^2}\left(\frac{f_c}{f_{off}}\right)^2\right] \qquad 2\text{-}26$$

: is Single-sideband phase noise density (dBc / Hz).

: is the Device noise factor at operating power level A (linear).

: is Boltzmann's constant, 1.38 x 10^{-23} J/K.

: is Temperature(K).

: is oscillator output RF power (W).

: is Loaded Q (dimensionless).

:fo is the Oscillator carrier frequency.

:fm is the frequency Offset from carrier.

The VCO is a very simple device that takes a voltage input, typically 0 - 5 V or 0 - 15 V and outputs a corresponding frequency, typically higher voltages give higher frequencies. Figure 2.51 shows a graph of the VCO tuning voltage versus the output frequency. As the tuning voltage increase, the output frequency increases. One interesting observation is the fact that the curve of the VCO is not linear; this is why a closed loop system is required. The slope of the VCO sensitivity typically measured in MHz/V, defines the VCO performance. A typical number might be approximately 50 MHz/V which means if the input voltage is increased by 1 V, the corresponding frequency is 50 MHz. Kv is the VCO sensitivity in MHz/V (Curtin and O'Brien, 1999).

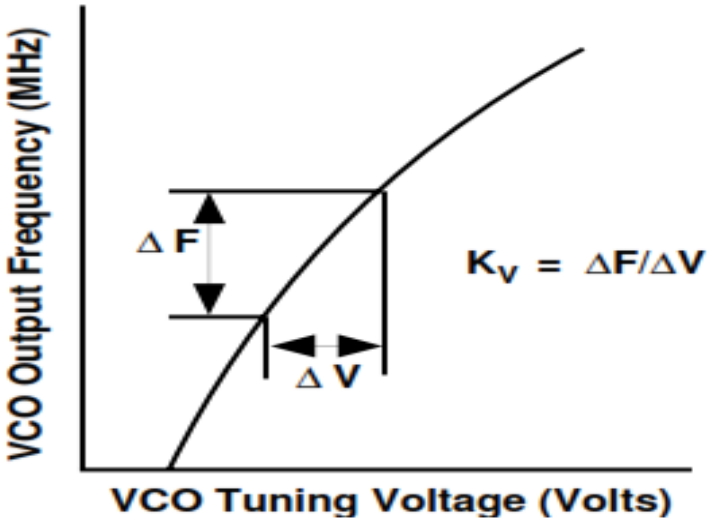


Figure 2.51: VCO tuning voltage versus the output frequency (adapted from Curtin and O'Brien, 1999)

2.7.4.3.3 Phased Detector and Charge Pump

The error detector (phase detector and charge pump) this is the block that compares the divided signal from the VCO with the reference signal. If the divided signal from the VCO is too slow, the phase detector compares this with the reference and alerts the VCO to speed up. Figure 2.52 depicts the phase detector and charge pump block diagram. On the diagram, there are two input signals and an output signal, and they are not synchronised as shown in Figure 2.53. This means that the PLL is out of lock, because if it were synchronised the two signals should be the same frequency with the same phase and because the two signals are out of lock, the result is an output waveform/signal which in this case, has more time high than it has low—this is alerting the VCO that it needs to adjust its output frequency so that the negative in the signal, matches the positive in the signal (MT-086 Analog Devices, 2009).

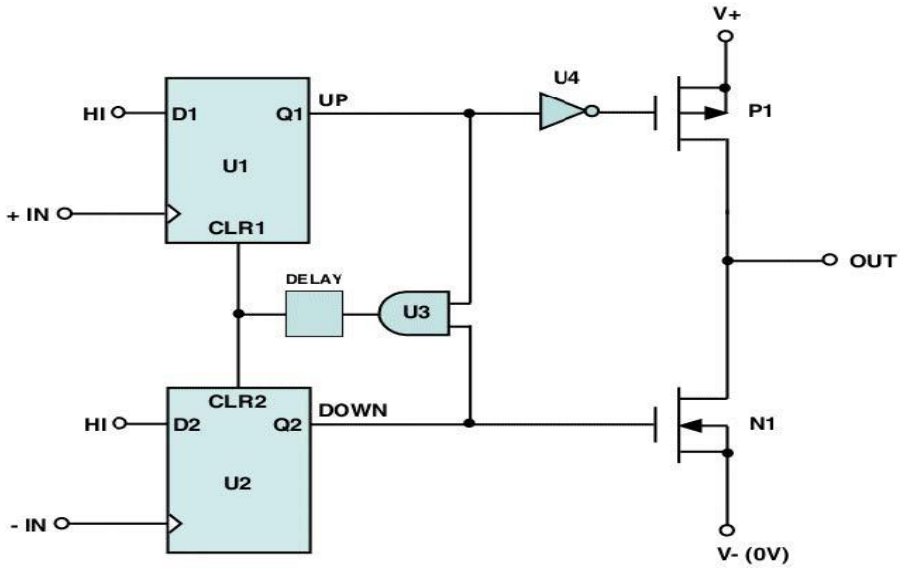


Figure 2.52: Phase detector and charge pump block diagram (MT-086 Analog Devices, 2009)

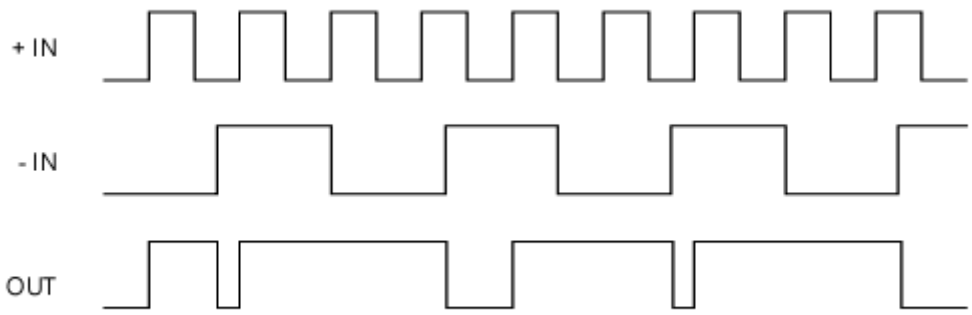


Figure 2.53: Out of frequency lock and out of phase lock (MT-086 Analog Devices, 2009)

Figure 2.54 shows a situation where the two signals are in lock. It is visible that the negative IN and positive IN are the same, the output signal has a balanced proportion of up and down pulses. This basically alerts the VCO to remain where it is, that is to remain locked.

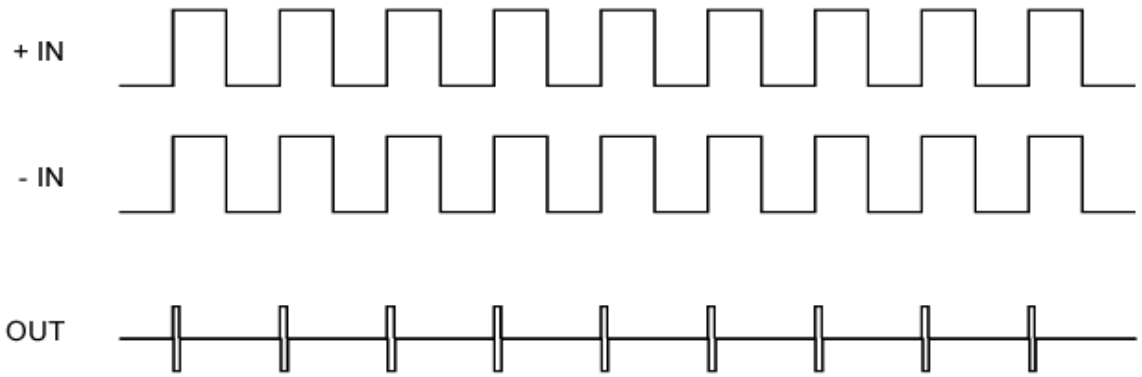


Figure 2.54: Frequency locked and in phase (MT-086 Analog Devices, 2009)

2.7.4.3.4 The Loop Filter

The low pass filter takes the output of the phase detector and charge pump, which is a current signal, converts it to a voltage that drives the VCO and in addition perform filtering of noise present in the loop. The loop filter can be passive or active. In its most basic passive form, it is comprised of three capacitors and two resistors and this takes the current output from the PFD, integrate it to a voltage which drives the VCO. Figure 2.55 shows a 3rd order passive loop filter topology chosen for the downconverter PLL. Depending on the components selected for the filter, the loop filter bandwidth can be defined—defining the loop filter bandwidth affects how the phase noise appears at various offsets from the carrier signal. Analog Devices Inc. offers a design tool called ADIsimPLL that allows the user to define loop filter and set the phase noise profile of the PLL. ADIsimPLL was used in this research.

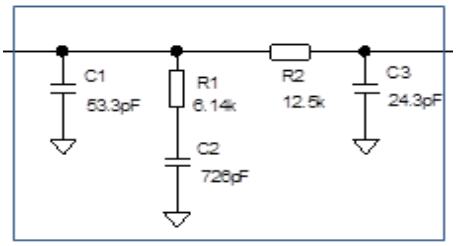


Figure 2.55: 3rd order PLL loop filter topology (ADIsimPLL, n.d.)

2.7.4.3.5 Frequency Divider

The feedback counter/divider takes the VCO output signal, divides that by an N value, and that is fed back to the phase detector and compared to the reference. Typically, the N-integer value is programmable and gives a range of output frequencies. N determines the output frequency from the PLL, for a fixed reference input frequency. N can be an integer value or a fractional value. The fractional N divider allows decimal values for the N, giving a finer resolution. The benefits of fractional-N based PLLs are that they tune very quickly. That however comes at an expense—that they have generally higher phase noise, as well as spurs than the integer-N counter parts (Bowick, 2008).

Figure 2.56 shows an integer-N block diagram. The reference divider is used to divide down the reference frequency to a lower PFD frequency, and the resolution at the VCO output becomes the new PFD frequency. The RF prescaler allows very high frequency operation of the RF stage (>10 GHz), this is actually built into the N divider. There tends to be a maximum frequency that the N divider can reliably operate to and the RF prescaler is required to divide down the VCO signal to a signal that the N divider can handle (Bowick, 2008) (Analog Devices, n.d.).

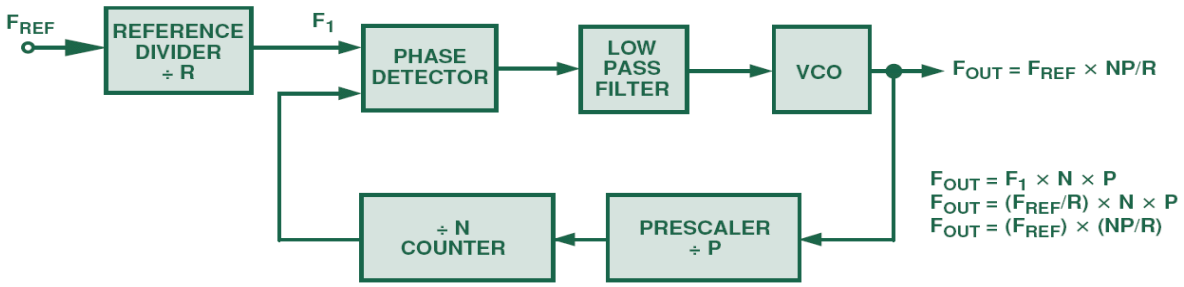


Figure 2.56: Integer-N reference divider block diagram (Bowick, 2008)

2.7.4.3.6 VCO Phase Noise

Phase noise appears in the time domain as the jitter or phase noise component added on the desired signal. In frequency domain, phase noise is measured by the normalised phase noise floor, or the flicker noise. Flicker noise appears closer into the carrier, and the importance is that lower is better. The higher the PFD comparison frequency, the lower the N divider, the

better the phase noise performance. The VCO phase noise is measured by phase noise power at certain offsets, for example if there is a 10 GHz VCO, it might be specified by the phase noise at a 100 kHz or 1 MHz or both. Again, lower is better.

Figure 2.57 shows the kind of signal at the VCO output of PLL output, locked on a spectrum analyser. Ideally, there would only be a straight line at zero point, the yellow dash line, but in reality, there are a number of imperfections present. As a result, the phase noise creates the skirts around the desired signal, at various offsets there is certain power of phase noise. Additionally, there is undesired spurious signals, which appear both on the left and right of the desired signal. All this create system imperfections that needs to be dealt with.

Phase noise is specified in the frequency domain and the unit is dBc/Hz, hence this is dBc/Hz at certain offsets from the desired signal. The noise in the 1 kHz bandwidth at the given offsets from the desired signal. Generally lower is better here.

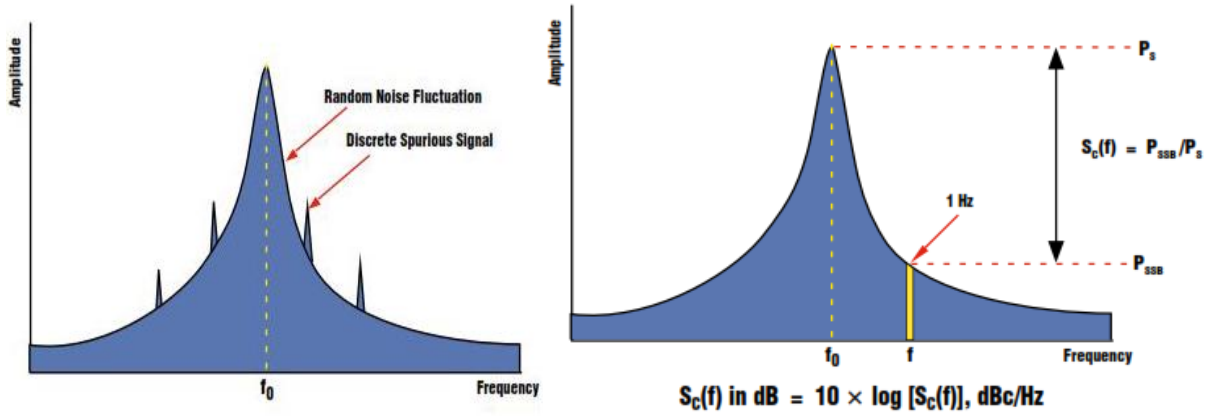


Figure 2.57: Phase noise specification in frequency domain

Figure 2.58 shows the reciprocal mixing process. The spectrum on the left of the received signal, and the desired signal is highlighted in the middle, however there is also an unwanted blocker in the same spectrum, and both of these are received by the RF receiver. If there is a LO signal with some finite phase noise as it is indicated in blue; typically, that is used to downconvert the RF wanted signal. The problem is that, as shown on the right, the LO signal also mixes with the unwanted blocker, and if the blocker is near the desired signal, then the phase noise from the LO signal lands on the blocker signal, and that can leak onto the desired signal which can cause system distortion and degrade performance. Therefore, it is important to minimise phase noise so that this interference is reduced or removed.

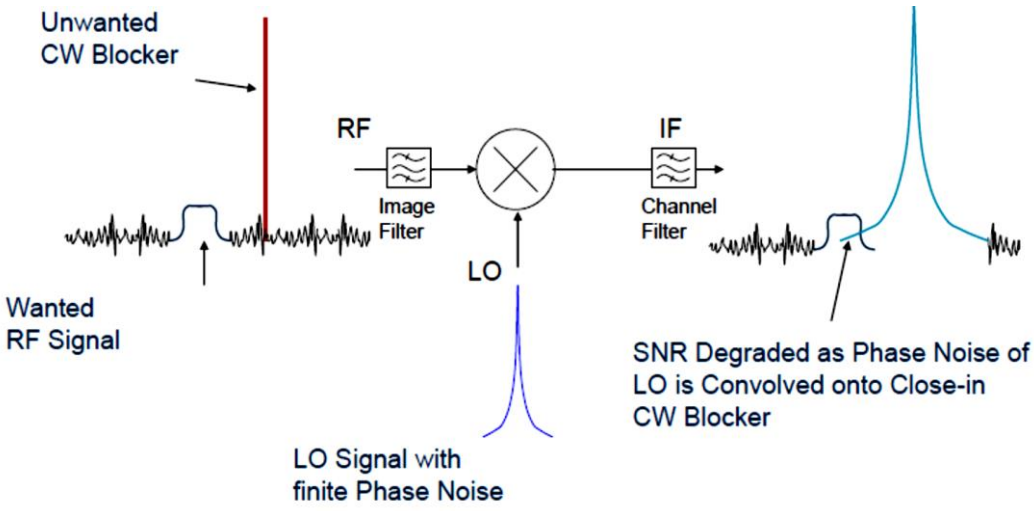


Figure 2.58: Reciprocal mixing process

2.7.4.3.7 Phase Noise in the PLL Chip

The PLL normalised phase noise floor, is a metric for measuring phase noise which can be used to compare any PLL. This is the noise that comes from the actual PLL synthesizer chip. There are several components that contribute to the phase noise, and this is the metric for measuring that which comes from the PLL, ideally the lower is better. One key detail here is that, for any given PLL, the normalised phase noise floor is usually fixed, sometimes it is frequency dependent and the N divider value and the PFD, go together in an equation that gives the actual phase noise performance from the system.

Equation 2-27 indicates that the N divider contribution is scaled at 20 log N while the PFD frequency is only scaled by 10. Ideally, N divider can be set as low as possible, and our PFD as high as possible, this reduces the phase noise contribution of the PLL. The rule of thumb is that for every doubling of PFD frequency, half the N divider get a 3 dB improvement in phase noise. The limitation here is that the PFD frequency tends to be maximum (there's a limited frequency that the PFD can handle). Newer devices can go up to 200/300 MHz.

- **PLL Normalised Noise Floor**

$$PN_{TOT1} = PN_{SYNTH} + 20 \log (N) + 10 \log (f_{PFD}) \quad 2\text{-}27$$

- **PLL 1/f Noise**

$$PN_{TOT2} = PN_{1/f} + 20 \log (f_{RF}/1\ GHz) + 10 \log (10\ kHz/f) \quad 2\text{-}28$$

- **Total PLL Noise**

$$L(PN_{TOT}) = \text{Square Root}\{L(PN_{TOT1})^2 + L(PN_{TOT2})^2\} \quad 2\text{-}29$$

Figure 2.59 shows a phase noise response plot of an integer-N PLL synthesizer. As mentioned, there are various contributors to phase noise. Looking at the black line, the dominant signal is what is displayed on spectrum analyser measurements. Close on to the carrier, on the extreme left,the y axis is the carrier signal. The desired signal of the VCO, then everything to the right is signal offsets from that signal. The light green signal is the reference noise contribution; this is dominant close into the carrier signal. moving away from the carrier signal, the PLL noise contribution becomes dominant. and finally moving further away again, then the VCO phase noise becomes dominant. Looking at the dashed lines, that is the effect of the loop filter on the various phase noise contributors. It is visible, for example, close into the carrier, the VCO noise is actually filtered by the loop filter, and it's represented by the red dashed line. Thus, the VCO noise is not dominant close into the carrier. Far off from the carrier the PLL and reference noise are filtered by the loop filter and that's why the VCO noise becomes dominant.

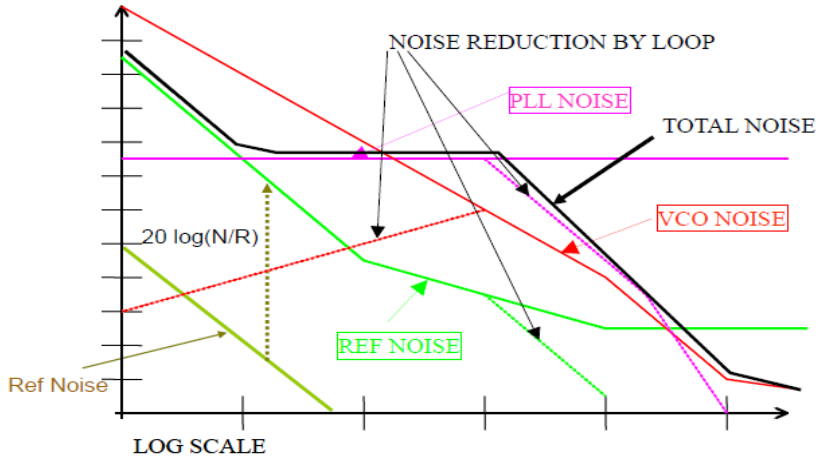


Figure 2.59: Phase noise of an integer-N PLL synthesizer (adapted from Analog Devices Inc. n.d.)

Figure 2.60 shows a phase noise response plot of an integer-N PLL synthesizer. This is another look at a similar plot examining the loop filter effect. Again, the centre frequency is on the extreme left of the plot and the frequency offsets are towards the right, the orange is again the reference noise, the green is the PLL noise, and the purple far out is the VCO noise. Some undesirable spurs are visible at the far out at around 5 MHz. The loop filter bandwidth can be increased or decreased to shape the phase noise profile. Typically, if the loop filter bandwidth is increased, it results in a lower in-band phase noise, but the far-out phase noise will degrade. The other performance metric is the settling time and typically a wider loop filter bandwidth will give faster settling times. Basically, there is a trade-off between phase noise and settling time and often the loop filter needs to be defined to get the best of both or the best trade-off.

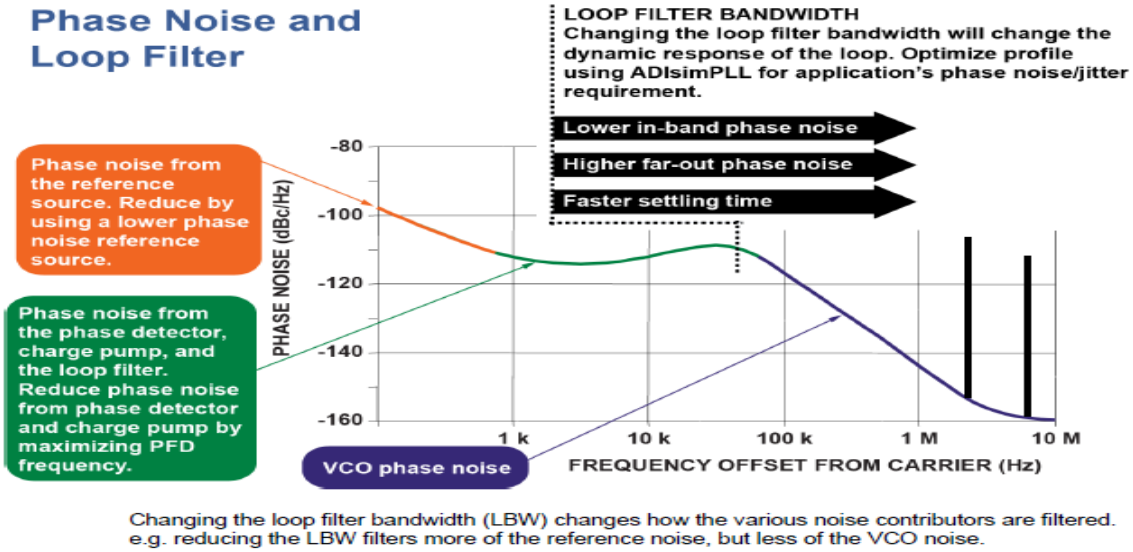


Figure 2.60: Phase noise and loop filter (adapted from Analog Devices Inc. n.d.).

2.7.4.3.8 PLL Performance: Spurious

Normally there is an ideal signal on the left, which is only one single tone, but in reality, this single tone is wrapped into some phase noise and spurious signals.

2.7.4.3.9 PLL Performance: VCO Spurious

Spurious frequencies happen because of coupling everywhere around the PLL. Coupling normally occurs between the reference input block, the N divider block and the VCO input. The coupling or the interference between these various/different blocks results in undesirable signals at the VCO output and these are signals that are called spurs that create interference down the line. Interference can be reduced by physically separating the various components and or by adding isolation and several other ways to minimise this interference or crosstalk.

2.7.4.3.10 PLL Lock Time

Lock time is one of the key metrics of a PLL. Lock time is quantified by the jump from one frequency to another frequency—that is a measure of how long it takes to settle to a new frequency. This is typically controlled by the loop filter bandwidth, where wider loop bandwidth yields a faster settling time and narrower loop bandwidth yields a slower settling time. Figure 2.61 shows a system that has a settling or lock time of 11 microseconds, this time requires a loop bandwidth up to 500 kHz. However, there is a limit on how wide the loop bandwidth can go, the wider the loop bandwidth, there is a phase noise contribution from the integer-N engine or demodulator, this phase noise contribution becomes dominant, and makes the loop unstable. A typical number for that maximum is single digits MHz, or approximately 5 MHz. Wider loop bandwidth results in faster lock times but increase far-out phase noise especially around PFD/2 offset.

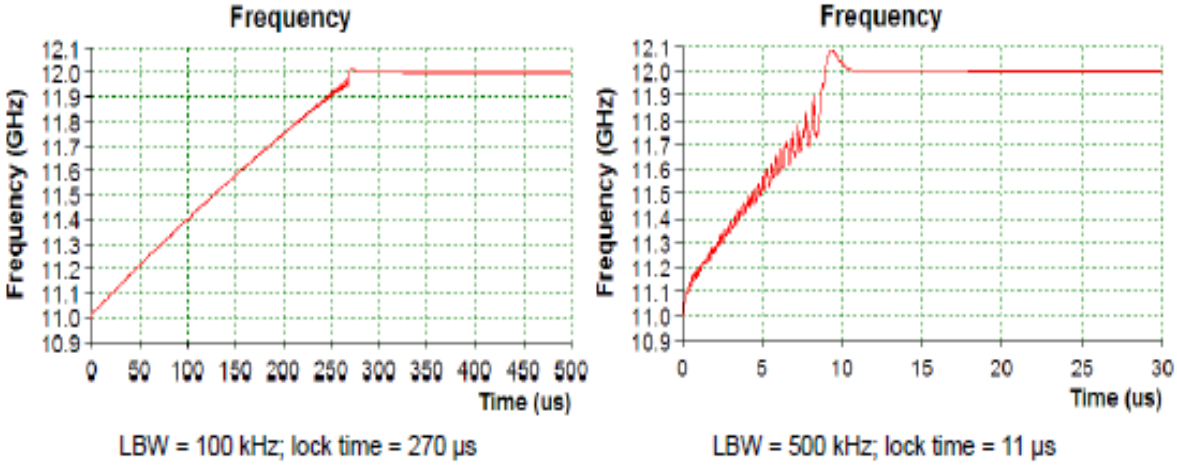


Figure 2.61: PLL lock time

2.7.4.4 Spaceborne PLL Literature Review

The reviewed spaceborne research with PLL relevant to the study are summarised with their highlights in Table 2.12.

Table 2.12: Spaceborne PLL literature review

Satellite PLL's Analysed	Highlights
M. Zamazal, 2004	PLL synthesizer for the AMSAT phase 3E satellite L-band front-end. Conventional solution uses a quartz oscillator with frequency multipliers.
S. A. Osmany et al, 2010	An integrated low phase noise VCO and high speed dividers and synthesizer that is tunable within 0.64 – 4.6 GHz, 5.1 – 6.9 GHz, 10.2 – 13.8 GHz and 20.4 – 27.6 GHz, enabling the integration of multiple bands and multiple standards in a single device.
P. Wang et al, 2011	1980-2010 MHz PLL synthesizer using ADF4107 chip for satellite Ku-band up conversion and down conversion sections.
S. Li et al, 2014	2 PLL synthesizers optimized for multimode GNSS receivers in 55 nm CMOS. Phase noise lower than -83 dBc/Hz and -110 dBc/Hz at 10kHz and 1 MHz offset respectively. PLL time is 20 micro seconds. Each PLL consumes 12 mA from a 1.2 V supply and occupies small area size. 1.25mm^2
V. Pandit et al, 2014	X-band and Ka-band PLL using Peregrine's integer-N PE83336 chip. 22.8 MHz TCXO reference. Frequency resolution 5.8 MHz. active loop filter provides wide operating range. Phase noise better than 81 dBc/Hz at 1 kHz offset. Fabricated on RT-dudroid 6010 substrate. Stable and low phase noise for space applications.
J. Roeber et al, 2014	4.34 - 4.70 GHz frequency synthesizer for digital satellite receiver systems. PLL components discretely developed and analyzed. Phase noise is -100.50 dBc/Hz at 1 MHz offset.

R. Xu et al, 2015	Multi-PLL with 2 stage fusion algorithm for GPS receiver's frequency loss of lock. Performs more robustly than the single-PLLs.
F. Aguirre et al, 2015	COTS based Ka-band tone generator for the ISARA Cubesat exciter. Frequency multiplier based phase locked loop (PLL), 26 GHz output tone multiplied from a 25 MHz reference temperature compensated crystal oscillator (TCXO). 25 dBm of RF output power from a buffer solid state power amplifier (SSPA). Used mixed technologies of both solder and chip and wire methods. Total mass is 190 grams, volume less than ½ U and total DC power less than 10 Watts. Key performance is overall stability highly depended on assembly technology. Recommends custom integrated circuit or multi-chip module for further mass and volume reduction.
M. Miao et al, 2015	Digital-PLL Redundant design method with more atomic clocks. Undesired phase and frequency hopping. Have little drift and auto adjusting loop bandwidth by feedback improves fast lock and reduces phase noise significantly.
B. Eppe et al, 2017	1.5 - 2.3 GHz traditional PLL synthesizers for a second stage frequency down conversation of a IRS series of satellites in X-band frequency 36 MHz crystal controlled reference oscillator. MATLAB simulated down converter system.
Z. Liu et al, 2017	9.75 GHz and 10.6 GHz fractional-N HMC778 PLL/VCO for dual band digital broadcast satellite (DBS) applications. 4^{th} order active loop filter. Phase noise -108 dBc/Hz at 100 kHz for both frequencies. Reference spurs are below -80 dBc. Size: 52 x 40 x 20 mm
B. S. Himani et al, 2017	S-band PLL synthesizer for a Ku-band transmitter for Geostationary satellites. Designed using Peregrine Semiconductors and RFMD devices. 62.5 MHz TCXO referenced. Synthesizer output fed to varactor diode based modulator module, BJT and MESFET based active frequency multipliers and a MMIC based low power amplifier. Spurious levels found below -50 dBc and phase noise performance is -71 dBc/Hz @10 kHz offset.
Z. Berber et al, 2018	Simulated 81 - 86 GHz Integer-N PLL/VCO using ADF4155 chip. 3^{rd} order passive loop filter. 1GHz channel spacing. Trade-off between fast lock and low noise.
D. Li et al, 2018	2.5 - 20/7 GHz Fractional-N PLL synthesizers of SerDes for satellite laser communication. TSMC 55 G process. Low power consumption of 27 mW at 1.8 V.
S. Li et al, 2018	Parallel FLL-assisted-PLL for QPSK carrier tracking in satellite communications. Less complex method of module reuse, smaller variance and larger pull-in range.
A. Lovascio et al, 2019	1635 - 1720 MHz low-side injection type integer-N PLL for Cubesat COTS based RF receiver. 40 MHz TCXO reference signal. Output filtered by COTS low pass filter to reduce harmonics power level and COTS amplifier to have a fixed power level at mixer LO port.

L. Kuai et al, 2019	17.45 - 20.2 GHz ADF5356 PLL/VCO synthesizer chip. 100 MHz OCXO reference signal. External Loop filter, harmonic suppression filter, amplifiers and frequency doubler are designed. Phase noise -112.97dBc at 1MHz offset frequency of 18.8 GHz. Reference spurs lower than -54 dBc. Output power greater than 13dBm.
S. Kameche et al, 2019	Design and simulation of a S-band (2 - 4GHz) Integer-N PLL for satellite transceivers. Using ADF4106 synthesizer chip. Phase noise -119.6 dBc/Hz at 1 MHz. latch time of 48.55 micro seconds for a frequency jump of 2 GHz. RMS phase error of 0.92 deg. Optimized for spectral purity and acquisition time.
J. P. Chaudhari et al.,2020	6.9 GHz and 7 GHz Highly stable PLL for the D-band (138 - 140 GHz) microwave interferometer. Used two approaches using a 7 GHz dielectric resonator oscillator (DRO) to achieve stability, output power of 17.62 dBm and phase noise of -120 dBc/Hz. This method is complex, large in size and expensive. Whereas the ADF4107 chip PLL synthesizer approach has medium design complexity, is cost effective and medium in size, designed at 6.7 - 7.2 GHz frequency, output power of 7.2 dBm and phase noise of -93 dBc/Hz at 100 kHz carrier offset.
V. K. Kanchetla et al., 2021	1.17 - 2.5 GHz Fully integrated on-chip fractional-N PLL with a single LC-VCO for a reconfigurable receiver for satellite navigation systems. Based on CMOS technology. Phase noise -109.73 to -116.43 dBc/Hz at 1 MHz offset. Low power consumption and active die occupying small area of a 32-pin QFN package.
M. R. U. Rehman et al., 2021	Ultra-low power 2.402 - 2.480 GHz all-digital PLL with injection-locked frequency multiplier and continuous frequency tracking. Fabricated 55 nm CMOS technology. Phase noise -111.15 dBc/Hz at 1 MHz offset of 2.4 GHz. consumes 0.46mW power and active area 0.129 mm^2
M van Wanum et al., 2021	Fractional-N PLL for a Ku-band up converter for satellite M2M applications. Loop bandwidth 400kHz and VCO phase noise of -95dBc/Hz at 100kHz offset. Power consumption 65mW. Halving the loop bandwidth quadruples the power consumption to 260mW which is not desirable.
J. L. Alvarez-Flores et al., 2022	Modeling and fabrication of a reconfigurable RF output stage that includes digital/analog conversion, mixer, and filters based on COTS, operating from 0.070 - 6 GHz.

2.7.4.5 PLL Performance Parameters

The PLL performance parameters are discussed and summarised in Table 2.13. This includes the phase noise—which occurs in-band, which is generally the PFD and the Charge Pump (CP), as depicted in Table 2.13. What is crucial here is the normalised phase noise floor. The design axiom is, the lower it is, the better. On the contrary, the higher the PFD frequency, the better, because it enables lower N—which is good for keeping the phase noise at a minimum. The

VCO also contributes to the phase noise profile, which occurs at certain offsets from the carrier and again, the lower it is, the better. Another important performance parameter is the PLL output power, the more the better depending on the specification. The spurs or spurious frequencies—the unwanted products of frequency generation also affect the PLL performance. The lower the spurs, the better (Leopold et al, 2022).

Table 2.13: Spaceborne PLL parameters and requirements

Key Parameters	Requirements	Remarks
PLL phase noise	Normalised phase noise floor	Lower is better
PFD comparison frequency	Maximum PFD frequency	Higher is better
VCO phase noise	Phase noise power at certain offsets	Lower is better
Output power	RF power level	Higher is better
Spurs	Worst case spur power	Lower is better

2.8 Spaceborne Downconverters Literature Review

The reviewed spaceborne research downconverter applicable to the study is summarized with their highlights in Table 2.14, as well as in Table 2.6.

Table 2.14: Spaceborne downconverters literature review

Spaceborne Downconverter's Analysed	Highlights
P. Yan et al., 2005	RF front end for BeiDou satellite navigation system. A prototype composed of a RF receiver module and an active antenna module. frequency range 2483.5 - 2500 MHz. NF is below 0.8 dB and the maximum gain of the RF module is 90dB.
R. Pelleriti et al., 2005	A 2.3 GHz SiGe RFIC front-end for U.S. satellite radio applications. SiGe BiCMOS double-conversion digital audio satellite radio receiver with on-chip RF and IF PLL. -97 dBm input sensitivity, 3.5 dB NF, 35 dB RF and 90 dB IF gain range, with >30dB image rejection and 30dBm on-channel OIP3. The RF VCO features a phase noise of -107 dBc/Hz at 100 kHz offset.
J. Spacek et al., 2006	Front-end module for GNSS software-defined receiver. consists of three independent channels with the bandwidth of 24 MHz each that use a single conversion superheterodyne concept with intermediate frequency 140 MHz.
J. -S. Jeon, 2006	Front-end module to receive satellite DMB service, planar structure, a microstrip patch was produced for the dielectric substrate in the upper layer and a LNA module was produced for the dielectric substrate in the bottom layer. The impedance bandwidth of antenna is 7.04 % (186 MHz), and the axial ratio is below 2 dB as good properties for the bandwidth of 25 MHz which is a DMB service band.
Z. Deng et al., 2009	Ku-band (10.5 − 13 GHz) to L-band (0.75 − 2.25 GHz) single-conversion low-noise block (LNB) front-end in a 0.18 µm CMOS technology. The in-

Spaceborne Downconverter's Analysed	Highlights
	band noise figure is between 2.8 − 4.2 dB. It achieves a gain of 50 dB with ±2 dB variation.
L. Zhao et al., 2010	The paper focuses on the Zarlink's ultra-compact RF front-end chip GP2015. High-frequency signals on the 1575.42 MHz would be converted to intermediate frequency. All local reference signals on 1.4 GHz, 140 MHz, 5.71 MHz are produced in one single-phase loop, the PLL reference signal frequency is 10 MHz generated by a temperature-compensated crystal oscillator. The implementation verifies that the hardware platform could effectively achieve the signals frequency conversion and analog-digital conversion.
J. Zhang et al., 2011	RF front-End design of large dynamic range receiver for satellite communication. Super heterodyne digital intermediate design scheme. The results of their simulation and tests showed that in the condition of NF=4.07 dB, the RF front-end maximum gain=74 dB, SFDR=59.61, which can satisfy the satellite communication receiver's need of high sensitivity, low noise figure and large dynamic range.
S. K. Jain et al., 2012	S-band receiver front-end design for portable satellite ground terminal. Converts RF 2.56 – 2.59 GHz to IF 67 MHz with the 2.493 – 2.523 GHz synthesizer.
G. Mannocchi et al., 2013	A L-band transmit/receive module for satellite telecommunications. In Rx mode, the module has a NF<1.6 dB and a TOI>20 dBm.
H. Tran et al., 2013	Low noise block downconverter designed and fabricated for satellite receiver system Vinasat 1 operating at C-band: 3.4 - 4.2 GHz. Conversion gain of 41 dB. **T**he noise figure is about 2 dB. Local oscillator frequency at 2.45 GHz, output power of the oscillator is 5.25 dBm, phase noise is less than -107.8 dBc/Hz at 100 kHz, the output frequency from 950 − 1750 MHz.
Ping-Yi Wang et al., 2014	A fully integrated Ku-band down-converter front-end for digital broadcast satellite (DBS) receivers. RF range (10.7 – 13.45 GHz) with four LO frequencies, and down convert the RF signal to L-Band (950 – 2150 MHz). Low noise figure (< 6 dB) and high gain (> 51 dB).
S. S. H. Hsu et al., 2015	Design of Ku/Ka-band down-converter front-end for digital broadcast satellite receivers. SiGe BiCMOS technology for DBS down-converter. Focused only on individual blocks LNA, mixer, balun, and IF amplifier Ku-band design with a low NF (< 5.8 dB) and a high conversion gain up to 47.7 dB. Ka-band design achieving a NF < 6.6 dB with a conversion gain up to 49.4 dB. The output P1dB of the two designs are 5.8 dBm and 4.2 dBm, respectively.
D. Roy et al., 2018	Design and realisation of Ku-band (12.75 - 13.25 GHz) telecommand and ranging receiver for satellite application. The receiver has a command

Spaceborne Downconverter's Analysed	Highlights
	threshold of -110 dBm and ranging threshold of -105 dBm. The receiver is qualified for space use.
D. Roy et al., 2020	Design of miniaturized wideband microwave Front-end using novel implementation techniques. C-band (5.8 − 7.0 GHz). A modular based LNA design, compact planar filter with transmission zeros, wideband mixer with low power LO drive, simple sequential bias circuit with minimum variables to adjust bias, lumped filter for image rejection of 60 dB are the highlights of the front end. Paper focuses on the individual design aspects and features of the circuits, implementations with qualification processes to meet the space quality assurance. LO not implemented as part of the design.
G. F. De Andrade et al., 2020	Systemic analysis and measurements of a heterodyne radio frequency front-end receiver for satellite communications in Ku-band alongside with the design and characterization of its single stage LNA. Active radio-frequency front-end receiver PCB for vehicular satellite communications has been designed and characterized in this work showing a gain of 40.1 dB in Ku-band. A single stage Ku-band LNA using CE3512K2 transistor was designed with 10 dB gain to minimize cost of PCB.
V. Rastinasab et al., 2021	Very high frequency (VHF) uplink 165 MHz, double stage superheterodyne architecture, the first mixer downconverts from 165 MHz frequency to 21.4 MHz. The second mixe mixes down the frequency from 21.4 MHz to 455 kHz.
Z. -L. Xu et al., 2021	Four-channel integrated K-band receiving front-end module for satellite communication. Operating frequency band of 17.7 − 20.2 GHz. In-band channel gain is greater than 31.5 dB, with the noise figure of 2.3 − 2.6 dB, and the suppression against the transmitting band of 28 - 30 GHz is over 50 dB.
E. Ollars, 2021	System design and characterization of a satellite communication radio receiver based on an Analog Devices ADC evaluation board. SNR of 26 dB sufficient for BPSK modulation scheme application.
Cardillo E et al., 2022	Wideband Versatile Receiver for CubeSat Microwave front-ends. 2 – 18 GHz, COTS components, double frequency conversion stages, gain 8.4 dB, minimum spurious. Suppression level of -45 dBc. 1 Watt power consumption. Not space qualified.

2.9 Summary

The downconverter is essential in a CubeSat receiver system for selecting, conditioning, and translating the received high RF signal to a lower IF signal for further processing and

recovering of the original data. There are multitude of RF receiver architectures to choose from and those of interest were reviewed in Chapter 2. Each receiver architecture has notable benefits and trade-offs to be made. The function and performance of the RF and IF components have great commonality. The architectures go from highly analog centered in their processing, to a more highly digital towards the bottom. A significant advantage of the superheterodyne receiver is that it is easier and much more economical to have the gain and selectivity of a receiver at one IF, than to have the gain of frequency selective circuits tune over a band of frequencies.

With the advent of higher performance, higher speed ADCs and DACs, the ability to convert higher frequency signals has become possible. This is what the revolution towards using more digital approach has been shown in the direct conversion architecture. Although the components for a direct receiver are now available, a single down conversion stage was chosen followed by an IQ demodulator running at a lower IF frequency. This allows for higher selectivity, more robust design in terms of interference immunity and it should not suffer from stability issues encountered when a considerable amount of gain is all in the RF band. Another approach would have been to use a RF sampling ADC, and to perform the IQ demodulation in the digital realm. Although this approach works, it increases the ADC processing requirements. This approach is commonly used in SDR's where bandwidth and demodulation parameters can easily be changed in software.

Working through the downconverter signal chain from input to output, the RF filter is a pre-selector, attenuating all RF frequencies outside of our RF band of interest. Although several types of filter technologies are available, these are typically low loss RF ceramic and SAW devices covering the design RF band. The selection of the filter type and specifications depends on the specific requirements of the downconverter system, such as the desired frequency range, insertion loss, passband and stopband characteristics and the trade-off between passband ripple and stopband attenuation.

The LNA is the key factor in determining the ultimate sensitivity of the receiver. As the overall noise figure or noise floor is ideally set by the noise figure of the LNA. Noise contributions of subsequent stages are reduced by a factor of 1/Gain of the LNA. Therefore, it's important to keep the LNA gain as higher as practical, but still meeting the linearity requirements of the receiver. Other key considerations in the selection of a LNA, is it 1 dB compression point and it's linearity, usually measured by the third order intercept point. The compression point determines the level of signals the LNA can handle, both desired and undesired before the gain starts to worsen. The third order intercept point is a measure of the level of intermodulation products generated inside the device in the presence of multiple signals. This is particularly

important in multi-channel systems where intermodulation products fall directly in the band of interest that significantly degrade the receive sensitivity. A LNA is a key component at the front-end of any radio receiver circuit to help reduce unwanted noise. In most receivers, the overall NF is dominated by the first few stages of the RF front end. By using a LNA close to the signal source, the effect of noise from subsequent stages of the receive chain in the circuit is reduced by the signal gain created by the LNA, while the noise created by the LNA itself is injected directly into the received signal. The LNA boosts the desired signals power while adding as little noise and distortion as possible. The work done by the LNA enables optimum retrieval of the desired signal in the later stages of the system.

Mixer technology varies widely such as passive diode ring mixers which have very good linearity, and other desirable characteristics which requires large levels of LO power, to active mixers requiring low level LO power, and typically having lower performance. In selecting a receive mixer, one must consider the conversion loss or gain, noise figure, linearity, as well as other parameters such as LO to RF isolation and the impact all these specifications have on the overall receiver performance.

In single conversion architectures, one of the choice between using a low side or high side LO, that is a LO with frequencies residing up or below the RF frequency by an offset equal to the IF frequency. This is determined by several factors, such as the potential preference of high-level energies of the image frequency, or the possibility of the LO frequency falling in the band restricted by the regulatory agencies. One of the key issues in selecting a phase locked loop based local oscillator, is selecting the LO frequency range. Since PLL based local oscillators provide the underlying frequency basis of the entire system, it must be stable over both time and temperature. Once passed the basics, the most important specification is that of the phase noise. Phase noise will impact selectivity and sensitivity, as well as greatly impacting the overall noise and distortion performance of the system.

In sum, CubeSat receiver is a critical subsystem for a satellite mission success. This chapter covered in depth exploration of the CubeSat communication receiver from system architecture, downconverter building blocks and frequency regulatory considerations. Fundamental concepts, key parameters and specifications of the downconverter were presented in Chapter 2. The concept of SDR is introduced. Existing literature on spaceborne downconverters were examined and highlighted to ascertain the research gap that the research aims to address. The knowledge from this chapter forms basis for the subsequent chapters which will delve into the design, simulations, implementation and validation of the C-band to L-band downconverter for a CubeSat receiver.

CHAPTER THREE : DOWNCONVERTER SYSTEM DESIGN AND SIMULATIONS

3.1 Introduction

This chapter details the design specifications, simulations and methodology used in designing the subsystems that constitutes the downconverter and the overall downconverter system. The downconverter design workflow is first presented. Design specifications for the downconverter, the system architecture block, the frequency planning, and the RF link budget (gain and NF) calculations are done to carefully select suitable COTS such as amplifiers, filters, mixers and PLL parts for the downconverter system. Simulations are performed and the circuits are optimised to realize the specifications and finally the designs are built and tested.

3.2 Design Methodology and System Level Approach

The following steps were followed in the design of the C-band downconverter (CDC):

- Define specifications for the overall CDC.
- Concept design; create system architecture block.
- Frequency planning.
- RF link budget (gain and NF) calculations.
- Carefully select suitable COTS such as amplifiers, filters, mixers, PLL, DC power circuitry and mechanical parts for the CDC subsystems.
- Design matching networks for the chain and stabilise the chosen amplifiers if not already stable.
- Design the input and output matching networks for minimum component count.
- Design DC biasing circuits.
- Perform simulations and optimise the circuit to realize the specifications.
- Schematics design in Altium design software, make suitable symbol for each part and create and assign footprint to each part.
- Design PCB layout and generate Gerber and manufacturing files.
- Generate bill of materials (BOM), order components and manufacture PCB.
- Build, debug and functional test PCB to verify CDC performance/specification.

The downconverter design workflow is presented as follows:

3.3 Design Specifications of Downconverter

The downconverter design requirements / specifications are first established and summarized in Table 3.1 as shown.

Table 3.1: Spaceborne downconverter system parameters and specifications

Parameters	Specifications
RF Range (GHz)	5.650 – 5.670
IF Range (GHz)	1.250 – 1.270
LO Frequency Range (GHz)	4.385 − 4.405
Gain (dB)	>25
Noise Figure (dB)	< 3
Output Power (dBm)	> 4
Phase Noise (dBc/Hz) @ 1MHz Offset	< −100
DC Power Supply (V)	6 − 15
Spurious Response (dBc/Hz) @ 1MHz Offset	< −60

3.4 Downconverter System Architecture

The chosen architecture for the downconverter is the popular super-heterodyne architecture consisting of a single stage that multiplies the RF input frequency by the local oscillator frequency. Any frequency in the amateur designated C-band receive range of 5.65 – 5.67 GHz can be mixed down to an amateur designated IF range of 1.265 – 1.270 GHz with a phase locked loop (PLL) synthesizer working from 4.385 - 4.405 GHz. Figure 3.1 shows the block diagram of the downconverter that was implemented.

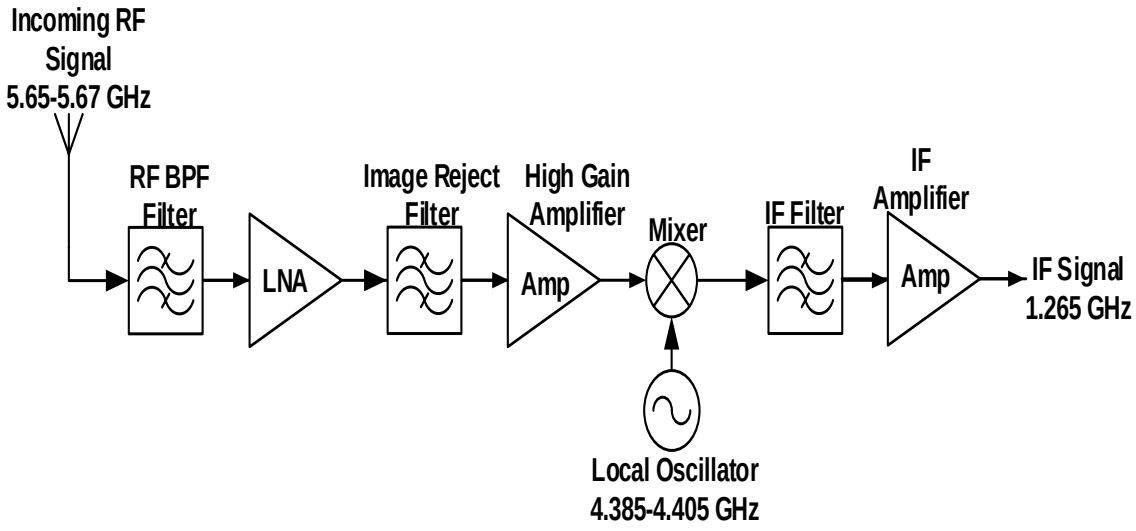


Figure 3.1: Downconverter block diagram

3.5 Frequency Planning

As part of the planning phase, frequencies at various stages of the downconverter system were chosen and calculated as follows; RF = 5.66 GHz, IF = 1.265 GHz (fixed) and LO = RF – IF = 4.395 GHz. The image signal is an unwanted primary mixing product that is also mixed down to IF. In this case it was calculated as follows; Image = RF – (2*IF) = 3.13 GHz. If the IF filter bandwidth is narrow enough, the image should be suppressed. The downconverter covers the amateur C-band according to the ITU frequency allocation as illustrated in the specifications of Table 2.1.

- RF frequency range (MHz) 5650 – 5670 (5660 centre frequency)
- IF frequency range (MHz) 1250 – 1270 (1260 centre frequency)
- LO frequency range (MHz) 4390 – 4410 (4400 centre frequency)

Table 3.2: Downconverter frequencies plan

Frequency Band	Low Frequency F_L (MHz)	Upper Frequency F_H (MHz)	Center Frequency F_O (MHz)	Bandwidth (MHz)
RF	5650	5670	5660	20
LO	4390	4410	4400	20
IF	1250	1270	1268	20

Frequency planning is beneficial for selecting an IF that eliminates and/or minimises in-band and out-of-band spurious frequencies. Spreadsheets were traditionally used to figure-out spur-free IF's. However, Keysight WhatIF Frequency Planner was used to aide in the elaboration of a chart of all IF's at the mixer output. The WhatIF Frequency Planner computes all harmonic combinations of the RF and LO signals and shows their spurious performance, as well as the spurious free regions of the spectrum on the same graph as depicted in Figure 3.2. The chart information includes bandwidth and spurious responses amplitude. There are several spur-free regions in which an IF frequency can be selected, in this case the highlighted coloured column shows a valid spur free region in which the IF frequency was selected.

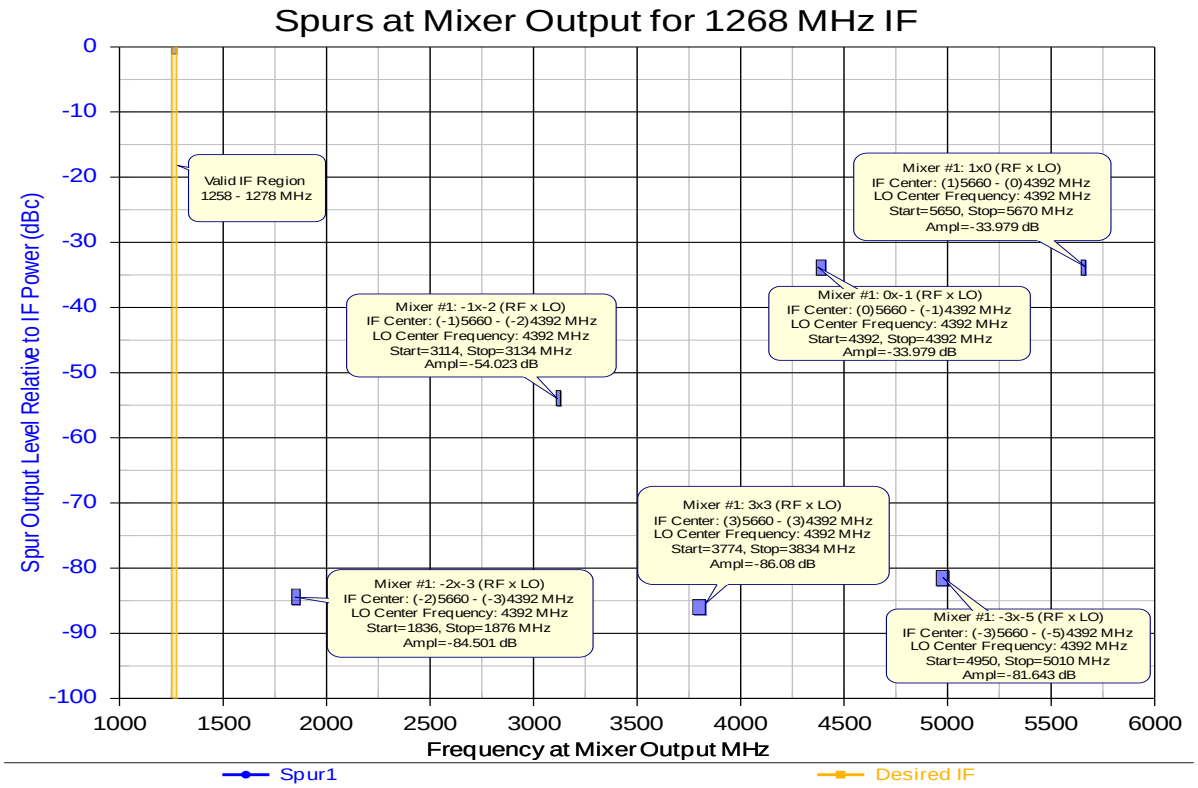


Figure 3.2: WhatIF frequency planner simulation for a typical RF mixer.

3.6 System Level/Casacade Analysis

The SysCalc6 software was used to perform system level analysis of the downconverter as illustrated in Figure 3.3. An overall gain of 53.79 dB and a *NF* of 3.44 dB were simulated.

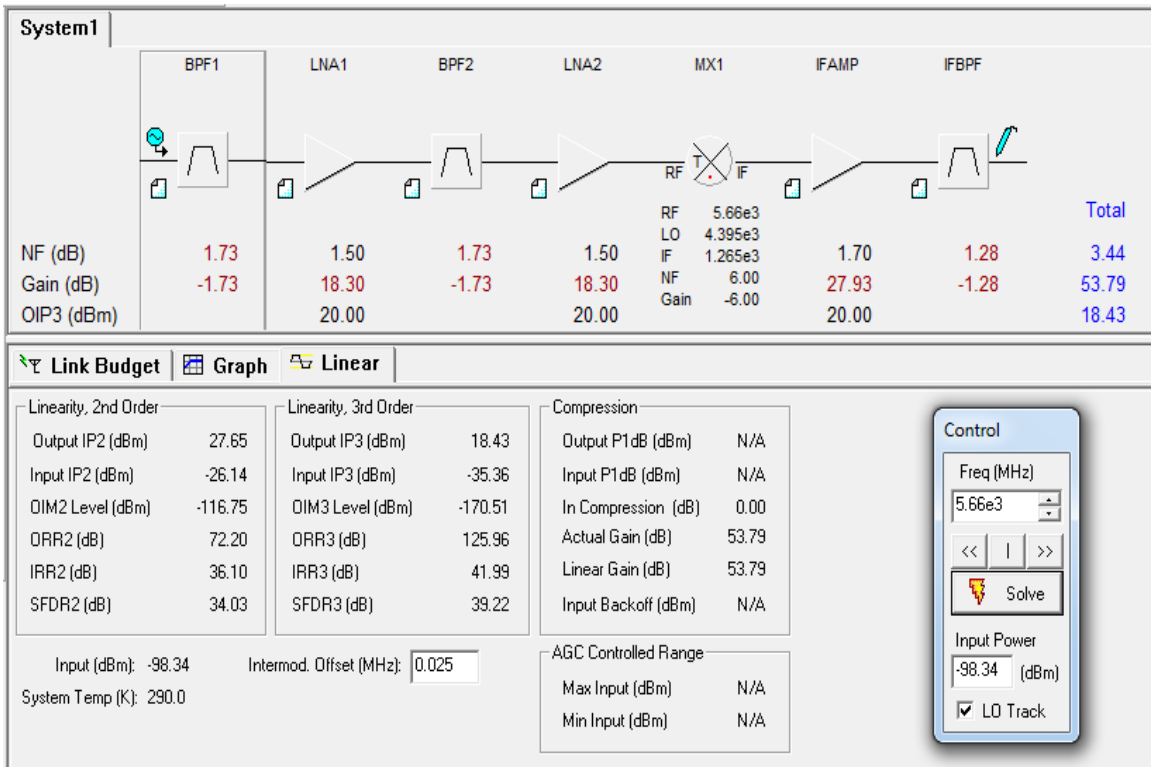


Figure 3.3: Downconverter system level SySCalc6 simulations

3.6.1 COTS Based RF and IF Amplifiers Design

With reference to the downconverter system block diagram in Figure 3.1, a LNA and RF gain amplifies are implemented in the front-end stage to enhance the received signal strength and improve sensitivity of the downconverter. The IF amplifier is required in the IF stage for additional amplification of the IF signal. Each amplifier is required to have sufficient gain and minimum *NF* for overall downconverter performance. The specifications for the amplifiers were generated as shown in Table 3.3.

Table 3.3: Amplifier specifications

Parameter	LNA	RF Amplifier	IF Amplifiers
Centre Frequency (GHz)	5.66	5.66	1.265
Noise Figure (dB)	1	1.5	2
Gain (dB)	15	20	30
Supply Voltage (V)	<=5	<=5	<=5
Impedance (ohm)	50	50	50

Various COTS amplifiers from different manufactures listed in Table 3.4, were compared and traded-off in order to select the best amplifiers for the downconverter system. The VMMK3803 from Avago Technologies and Hittite's HMC718LPEE were initially chosen as the RF LNA and IF amplifier respectively, because of low NF, high gain and low power consumption in comparison to others. After implementation, the MGA665P8 COTS amplifier was selected for all the downconverter system amplification needs due to better performance stability over the entire operating frequency band of the downconverter.

Table 3.4: COTS amplifiers

Part #	Manufacturer	Frequency Range (GHz)	NF (dB)	Gain(dB)	P1dB (dBm)	Voltage (V)/ Isupply (mA)
VMMK3803	Avago Technologies	3 - 11	1.5	20	7	3/20
RF3376	RFMD	DC – 6	2	22.5	11.5	3.3/35
HMC718LPEE	Hittite	0.6 – 1.4	0.75	27.5	15.7	3/187
HMC474SC70E	Hittite	DC - 6	3.9	10	6	5/25
MGA675T6	Avago Technologies	4.9 - 6	1.75	17.8	-10	3/10
MGA665P8	Avago Technologies	0.5-6	1.2	18.4	18.1	3/20.5

3.6.2 COTS BASED RF and IF Filters Design

With reference to Figure 3.1, three bandpass filters (BPFs), namely, the RF band select filter (BPF1), the RF image reject filter (BPF2) and the IF filter (BPF3) are required for the downconverter system. The first RF BPF1 placed right at the front-end is required to reject the frequencies outside the passband. The second BPF2 is required mainly to reject the image frequency and is placed just before the RF amplifier to filter out the noise and harmonics that might have been introduced by the LNA. The last BPF3 is placed after the mixer to reject unwanted mixer's products. Since selectivity is decided at this stage, a narrow bandwidth is often required. The specifications for the filters were based mainly on ensuring that the image frequencies are rejected as shown in Table 3.5.

Table 3.5: Filter specifications

Parameter	RF BPF1	RF BPF2	IF BPF3
Centre Frequency (GHz)	5.66	5.66	1.265
Bandwidth (MHz)	10	5	20
Stop Band Attenuation (dB)	>50	>50	>50
Return Loss (-S11) (dB)	>15	>10	>20
Insertion Loss (-S21) (dB)	<5	<5	<5

Various COTS BPF's from different manufacturers were compared in terms of the filter performance specifications as shown in Table 3.6. Some of the trade-offs during component selection include cost, stock availability and component lead-time. Therefore, Murata Electronics LFB215G37SG8A185 was chosen for BPF1, Johanson Technology 5515BP15B730 was chosen for BPF2 and Murata's SF2186E was chosen for BPF3 for the downconverter application.

Table 3.6: COTS filters

Part #	Manufacturer	Center Frequency (GHz)	Bandwidth (MHz)	Insertion Loss (dB)	Input/Output Impedance (ohm)
LFB215G37SG8A185	Murata Electronics	5.375	475	2.2 max	50
5515BP15B730	Johanson Technology	5.5	725	2.8 max	50
1200BP44A575	Johanson Technology	1.2	575	2.8 max	50
SF2186E	Murata Electronics	1.26852	20.46	1.7 typ	50

The first RF BPF1 placed right at the front-end is required to reject the frequencies outside the RF passband. Figure 3.4 depicts the S-parameters simulations in ADS® of the actual selected COTS BPF1 LFB215G37SG8A185 from Murata. The center frequency of 5.66GHz represents the frequency that the filter is primarily designed to pass without significant attenuation. The simulation indicates that the bandwidth is sufficient to cover the 20 MHz band of interest. The stopband is indicated by the range of frequencies outside the passband where the filter starts to attenuate signals. The image frequency of 3.13 GHz also falls in this band. The insertion loss (-S21), is indicated by the transmission coefficient (S21) which signifies the reduction in signal power as it passes through the filter. The insertion loss (-S11) value surpasses the specification. Return loss relates to the impedance mismatch between the filter and the source. The input reflection coefficient (S11) indicates good matching at the design RF.

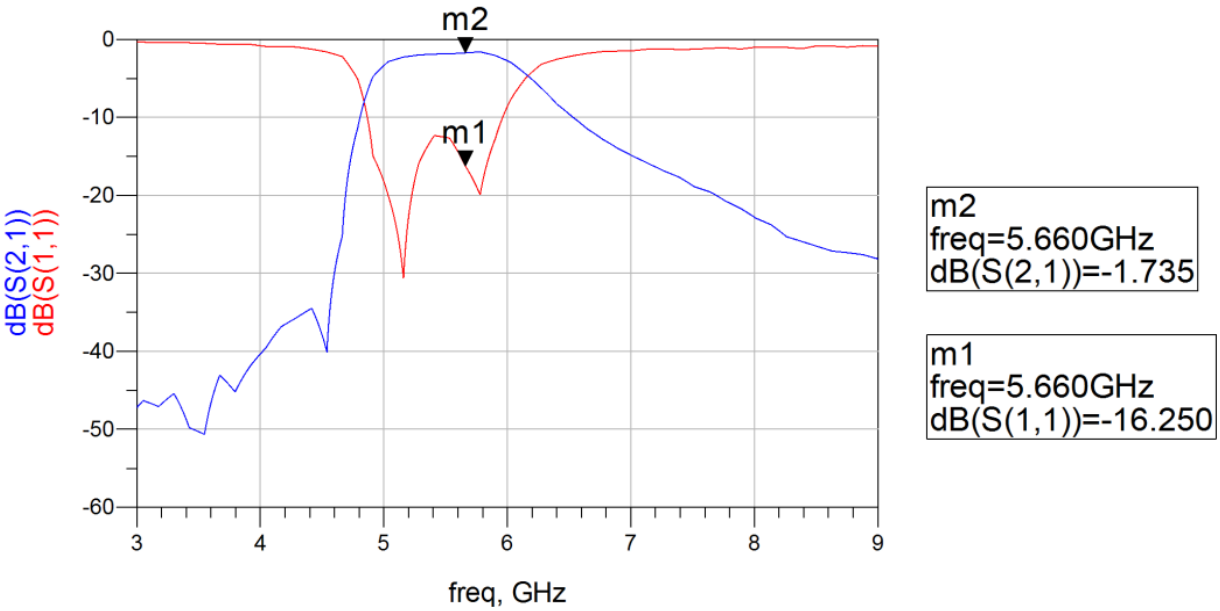


Figure 3.4: RF BPF1 S-parameter simulation

The selected IF BPF S-parameter simulations were also done in ADS and yielded results shown in Figure 3.5. It is evident that the bandwidth is sufficient and narrow enough for RF and LO leakage suppression, as well as anti-aliasing for digitization. The insertion loss and the reflection coefficient are adequate at the design IF frequency.

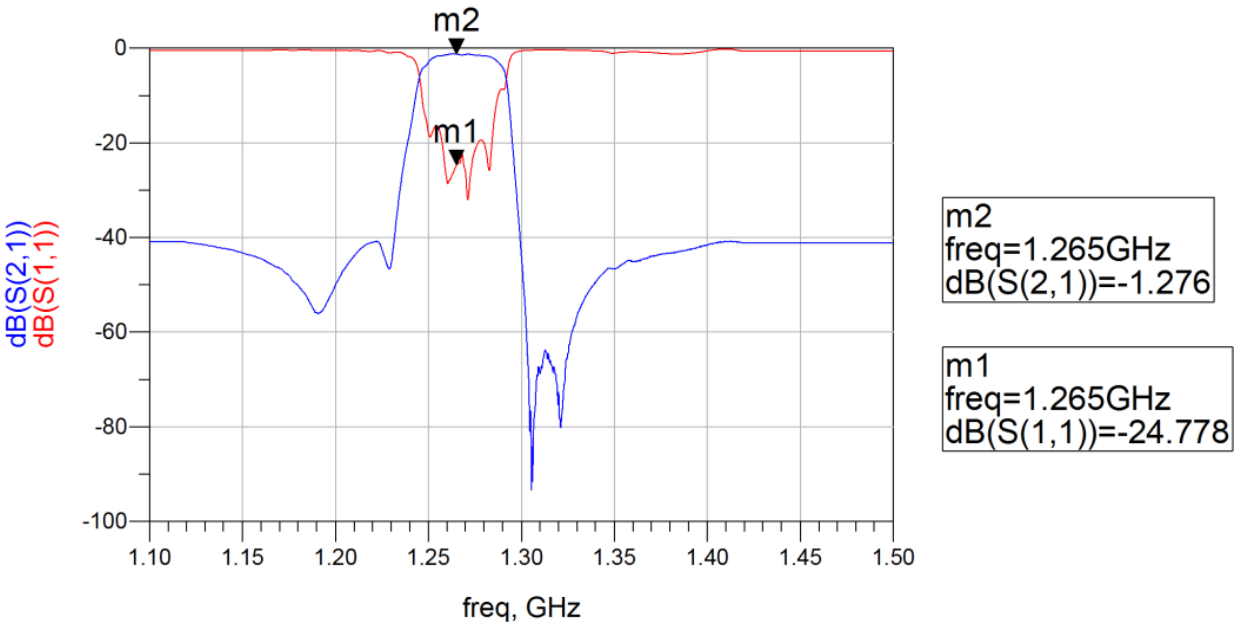


Figure 3.5: IF BPF3 S-parameter simulation

3.6.3 COTS Based Mixer Design

A double balanced mixer was selected as it offers better performance in terms of isolation, the third order intermodulation distortion as well as the RF and LO signals suppression at the IF port. Table 3.7 illustrates the parameters essential in comparing the performance of the COTS double balanced mixers. The MCA-12GL+ from Minicircuits performs relatively well in terms of isolation and was chosen for the downconverter application because of availability. Other options like the Minicircuits MAC- 60LH+ and Hittite's HMC787LC3B could be considered because of respectively low conversion loss and excellent isolation at all ports but was out of stock and the lead times were too long.

Table 3.7: COTS mixers

Part #	Manuf-acturer	LO/RF (GHz)	IF (GHz)	Conversion Loss (dB)	LO/RF Isolation (dB)	LO/IF Isolation (dB)	IP3 (dBm)	LO Power drive (dBm)
MCA-12GL+	Mini-circuits	3.8 – 6.5	DC – 1.5	6.8	32	13	9	+4
MAC- 60LH+	Mini-circuits	1.6 – 6	DC – 2	6.1	36	15	13	+10
HMC787LC3B	Hittite	3 – 10	DC – 4	9	55	42	23	+17
SIM-73L+	Mini-circuits	4.2– 7	DC – 3	6	23	18	9	+4

3.6.4 Local Oscillator Design and Simulations

The local oscillator is responsible for generating a highly stable carrier signal. Down conversion is achieved by mixing the incoming RF signal with a stable carrier signal generated from a LO operating within 4.385 - 4.405 GHz. A PLL was selected to generate the downconverter's LO signal, because it is simple to implement and can deliver a steady as well as low phase noise LO signal. The PLL must be able to deliver the specified carrier, with output power levels sufficient to drive the mixer. The frequency range and output power level specifications for the LO are illustrated in Table 3.8.

Figure 3.6 shows a basic block diagram of the PLL synthesizer. The PLL uses a reference frequency (from a crystal oscillator), together with feedback dividers, to compare the reference frequency with a feedback frequency to implement a closed loop control of the VCO voltage (Leopold et al, 2022).

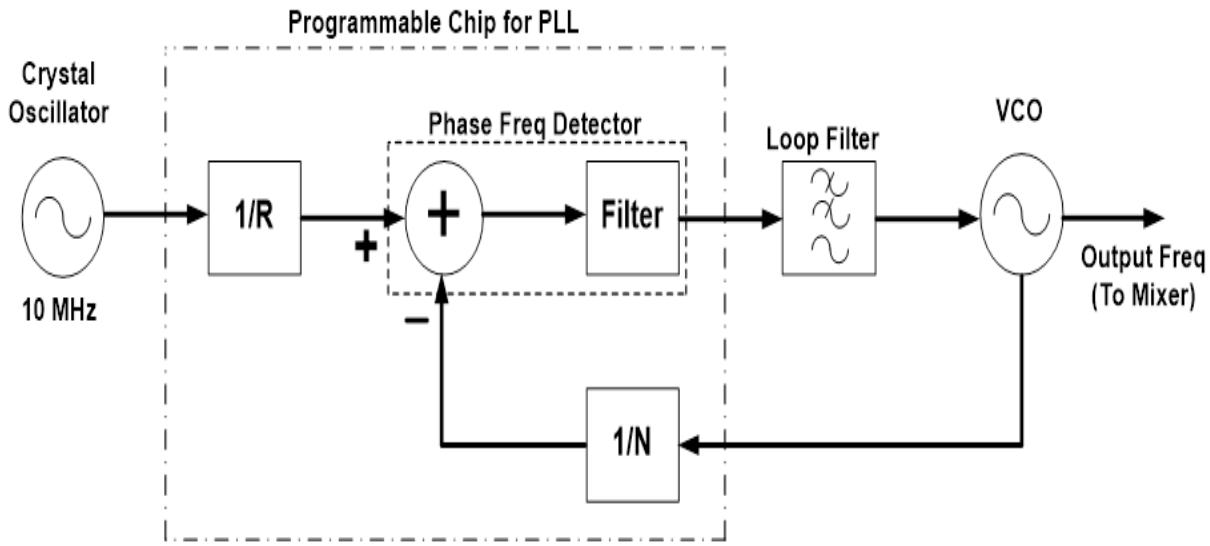


Figure 3.6: PLL block diagram (adapted from Leopold et al, 2022)

The PLL system uses a programmable PLL synthesizer chip, which consist of the phase detector and divide-by-N counter. Here the divided down signal is applied to the phase detector, which compares the phase of the divided down signal and that of the reference signal. If the two signals have the same frequency and phase, the error signal usually generated by the phase detector will be zero and the loop is said to be locked. Otherwise, there is an error signal which consists of a DC and AC components. However, the AC component is desired and is filtered out by the loop filter, whereas the remaining DC component is applied to the VCO, to account for any drift that may occur on the VCO due to temperature fluctuations or aging. The VCO serves as an integrator and the applied DC voltage will increase and decrease the frequency of the signal generated by the VCO to restore the error signal and therefore making sure the loop is always locked. The engine of the PLL is the PFD, which is the circuit that compares the reference and the feedback dividers. The use of a low frequency crystal reference, enables that the frequency error of the output frequency is relatively low (Leopold et al, 2022).

The PLL design workflow is simply presented as follows:

3.6.4.1 PLL Design Specifications

The design specifications / requirements are first established and summarized in Table 3.8 as shown.

Table 3.8: Spaceborne PLL specifications (adapted from Leopold et al, 2022)

Parameters	Specifications
Tuning Frequency Range (GHz)	4.385 − 4.405
Output Power (dBm)	> 4
F_{ref} (MHz)	10
Loop Bandwidth (kHz)	70
Step Frequency (MHz)	1
Phase Noise (dBc/Hz) @ 1MHz Offset	< −100
DC Power Supply (V)	6
Spurious Response (dBc/Hz) @ 1MHz Offset	< −60

3.6.4.2 Selection of the Reference Oscillator

The choice of a highly stable reference oscillator that will provide the reference signal of 10 MHz to the phase detector. The TCXO from Euroquartz shown in Table 3.9 was selected because it was available in stock at F'SATI and has proven its robustness in previous F'SATI CubeSat missions (Leopold et al, 2022).

Table 3.9: COTS TCXO (adapted from Leopold et al, 2022)

Part #	Manufacturer	Frequency (MHz)	Phase Noise @10kHz (dBc/Hz)	Stability (ppm)	Operating temp (degree Celsius)
MB57T3310	Euroquartz	10	-152	2.5	- 30 to + 85

3.6.4.3 Selection of the PLL Synthesizer Chip

Selection and programming of the PLL synthesizer chip, which consist of the phase detector and divide-by-N counter. Here, the divided down signal is applied to the phase detector, which compares the phase of the divided signal and that of the reference signal. If the two signals have the same frequency and phase, the error signal usually generated by the phase detector will be zero and the loop is said to be locked. Otherwise, if there is an error, the error signal consists of a DC and AC component. However, the AC component is desired and is filtered out by the loop filter. Whereas the remaining DC component is applied to the VCO. The VCO serves as an integrator and the applied DC voltage will increase and decrease the frequency of the signal generated by the VCO to restore the error signal and therefore making sure the

loop is always locked (Leopold et al, 2022). Table 3.10 outlines various Analog Device's COTS synthesizer chips with their specifications.

Table 3.10: Analog Devices Inc COTS PLL synthesizer chips (adapted from Analog Devices Inc, n.d.)

Part#	Config	Type	VCO	Fmin	Fmax	PN Floor	Max Ref	VCC (min)	VCC (max)	Vp	Icc
HMC704	single	both		0	8000	-217	350	2.7	3.3	5	58
HMC439	PFD	Int-N		0	200000	-233	1300	4.8	5.3		96
ADF5356	single	both	yes	53	13600	-227	500	3.1	3.5		81
ADF5355	single	both	yes	53	13600	-223	500	3.1	3.5		81
ADF4356	single	both	yes	53	6800	-227	500	3.1	3.5		81
ADF4355-3	single	both	yes	54	6600	-223	500	3.1	3.5		81
ADF4169	single	both		0	13500	-224	260	2.7	3.3	3.3	21
ADF4157	single	Frac-N		0	6000	-211	250	2.7	3.3	5.5	21
ADF41513	single	both		0	26500	-234	2250	2.7	3.3	3.3	21
ADF41512	Single	both		0	18000	-234	2250	2.7	3.3	3.3	21
ADF4108	single	Int-N		0	8000	-223	250	3.2	3.6	5.5	15
ADF4107	single	Int-N		0	7000	-223	250	2.7	3.3	5.5	15
ADF4106	single	Int-N		0	6000	-223	300	2.7	3.3	5.5	10
ADF4007	single	Int-N		0	7500	-219	240	2.7	3.3	5.5	15

The ADF4107 PLL synthesizer from Analog Devices shown in Figure 3.7 was selected because it is specified to operate up to 7 GHz. The ADF4111 used for F'SATI missions could potentially be used but it only operates up to 3 GHz.

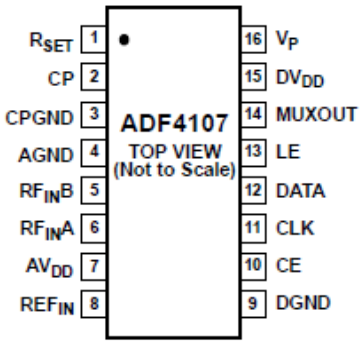


Figure 3.7: ADF4107 synthesizer chip (adapted from Analog devices Inc, n.d.)

Figure 3.8. shows a block diagram of the internal architecture of the ADF4107 integer-N system from Analog Devices Inc. On the top left-hand side of the block diagram, there is a reference input, proceeded by a buffer and followed by the 14-bit R counter, which is the reference counter, and this is fed to another buffer, and finally fed to the PFD. On the bottom left-hand side is the RF input and this is generally a higher frequency than the reference input. CMOS circuitry is generally good enough up to 200 MHz and it can handle most reference frequencies that are generated by the crystals. Whereas in many communication systems, there are frequencies upwards of 6, 8, 10 GHz etc and some more complicated circuitry is needed to divide the high frequencies down to 1 MHz or 200 kHz for the PFD. Therefore, what tends to happen is, there is a pre-scaler, which is basically a fixed block of circuitry, which uses what is called a dual modulus pre-scaler to implement a fairly high feedback divide values. This high frequency is divided to the same frequency as the PFD, and then the CP circuitry outputs the current pulses which are output to the filter and sent to the VCO. There is also extra circuitry for the manufacturer production purposes and also for indicating lock. For most of the CubeSat communication circuit's applications, for instance the power amplifier is not on until/unless all other circuits are working properly. Hence the PLL has a lock detect circuitry to indicate lock at the right frequency, so that it is actually safe to turn on the transmitter.

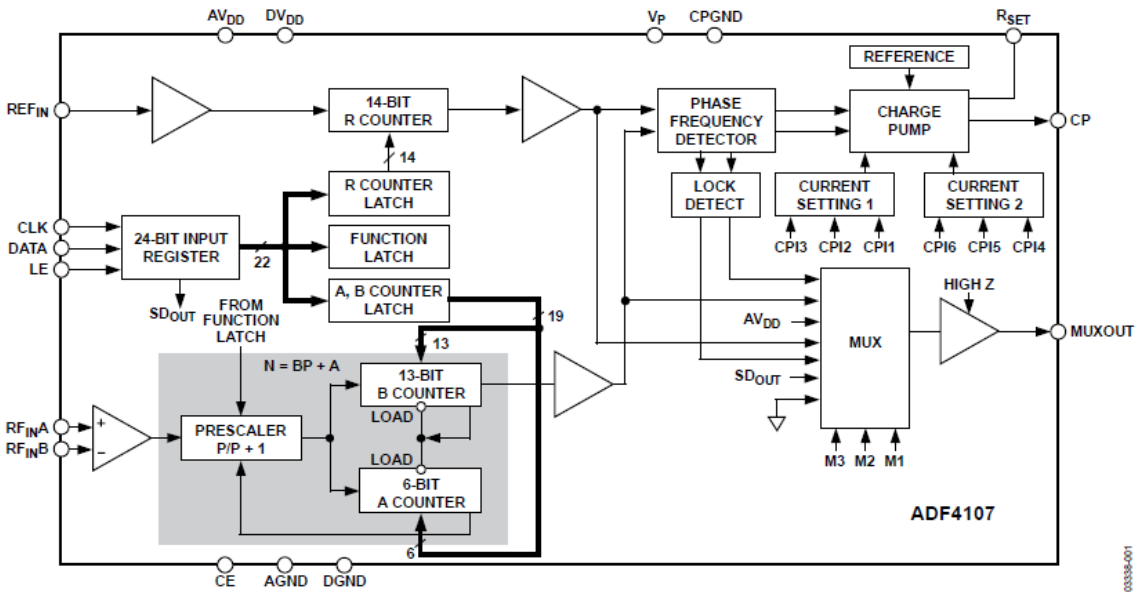


Figure 3.8: ADF4107 internal architecture (adapted from Analog devices Inc, n.d.)

3.6.4.4 Choosing a Suitable VCO

In order to achieve good performance from the PLL synthesizer in terms of phase noise, the choice of a VCO matters. A VCO with good phase noise and harmonic suppression is often required. The V940ME05 VCO from Z-Comm was selected because it covers the required LO

frequencies for the given band 4.385 - 4.405 GHz with good phase margin and delivers sufficient power to drive the mixer. Table 3.11 outlines the specifications for the VCO.

Table 3.11: COTS VCO specifications

Part #	Manufacturer	Fmin (MHz)	Fmax (MHz)	Tuning Sensitivity (MHz/V)	Vmin (V)	Vmax (V)	Phase Noise @10kHz (dBc/Hz)	Output Power (dBm)	Vcc (V)
HMC391LP4E	Analog devices Inc.	3900	4450	80	0	10	-86	5	3
398490S12	APA Wireless	3980	4900	50	0.2	23	-105	-2	12
CVC055CC	Crystek	4267	4442	14.8	0.1	16	-106	5	8
ROS-ED12752/1	Mini-Circuits	3900	4700	115	0	9	-89	4	10
ROS-ED12485/2	Mini-Circuits	3300	4550	80.9	0	22	-85	4	5
RQRE	Raltron	4000	4500	54	0	12	-85	8	12
DCMO250512-5	Synergy	1826	5255	156	0	22	-76	2	5
DCRO310430-5	Synergy	2405	4709	154	0	15	-81	4.5	5
V940ME05	ZComm	4280	4420	100	0.5	4.50	-87	0	5

3.6.4.5 Design of the Loop Filter

ADISimPLL software was used to design the loop filter and generates the overall PLL schematic. The PLL was designed with the following additional inputs (adapted from Leopold et al, 2022):

- F_{ref} = 10 MHz
- Channel spacing = 1 MHz
- Loop Bandwidth = 70 kHz
- Phase margin = 45^{o}
- N= F_{out}/F_{ref}=4395

Figure 3.9 illustrates the final PLL schematic, with the resulting loop filter component values. Figure 3.10 and Figure 3.11 depicts the phase noise of the PLL, with all contributing components in the legend, and the step response of the PLL respectively.

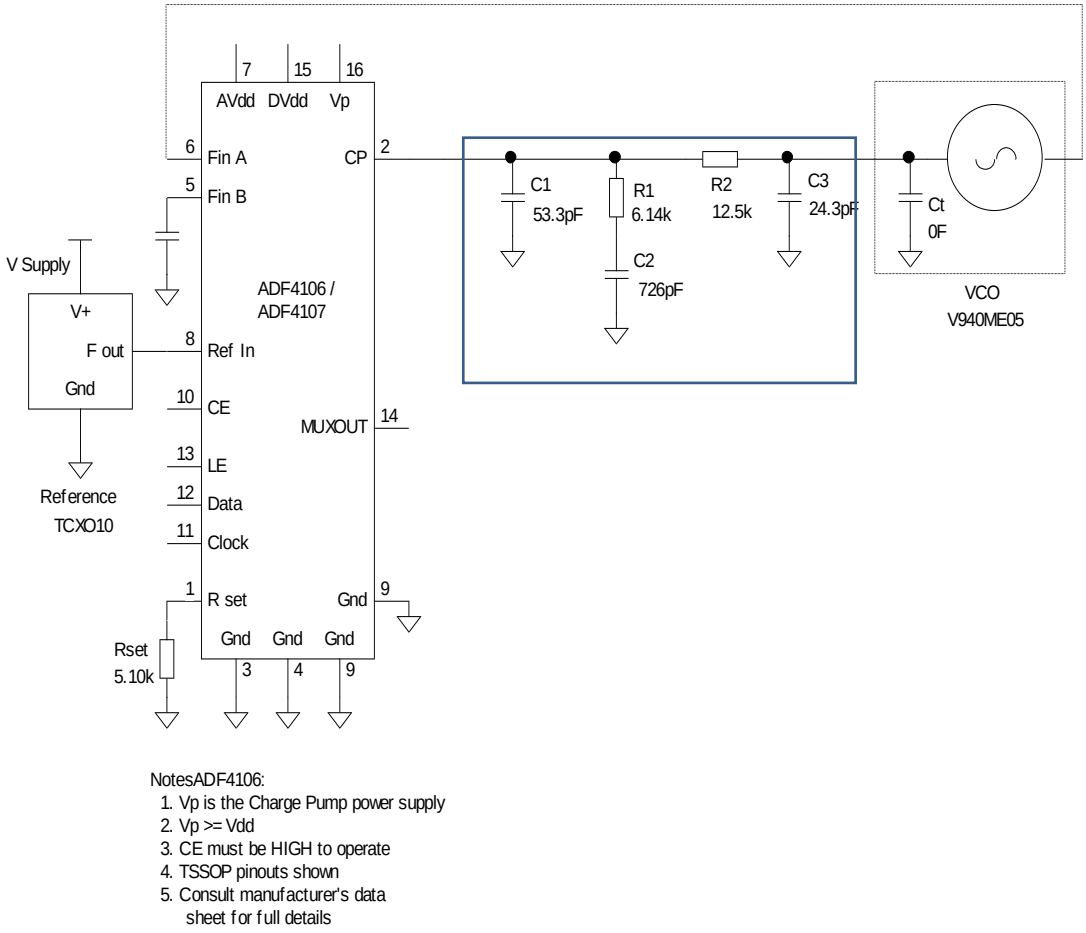


Figure 3.9: PLL schematic (adapted from Leopold et al, 2022)

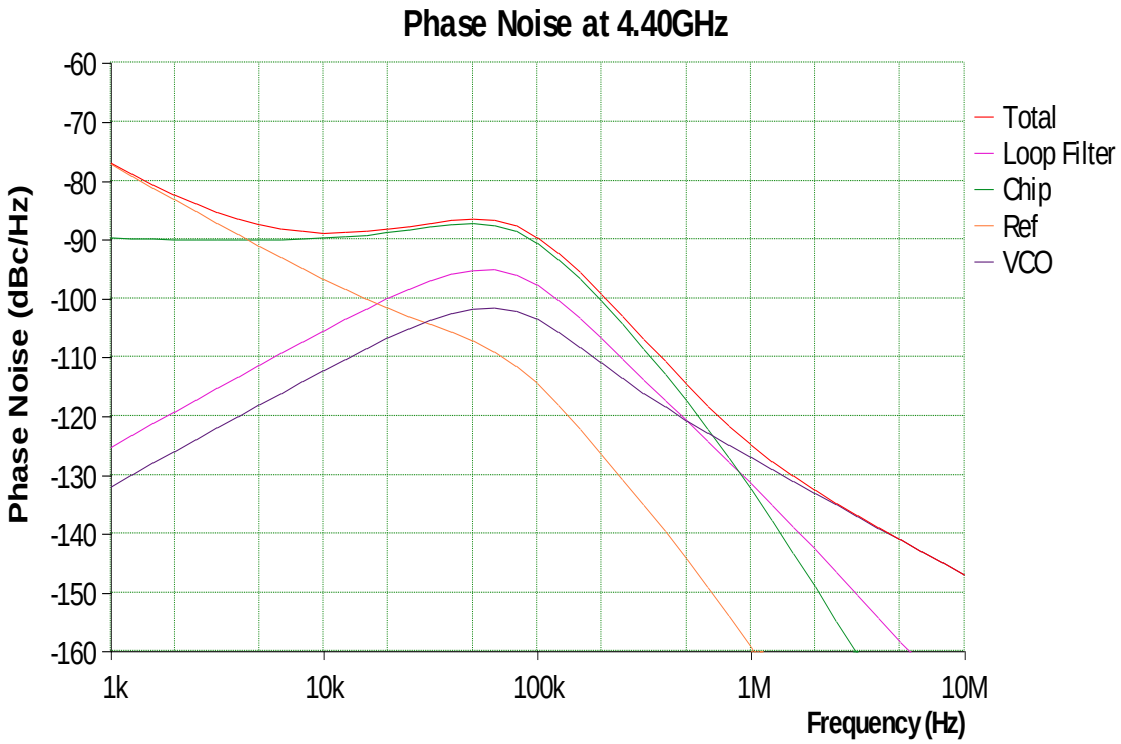


Figure 3.10: PLL phase noise estimation (adapted from Leopold et al, 2022)

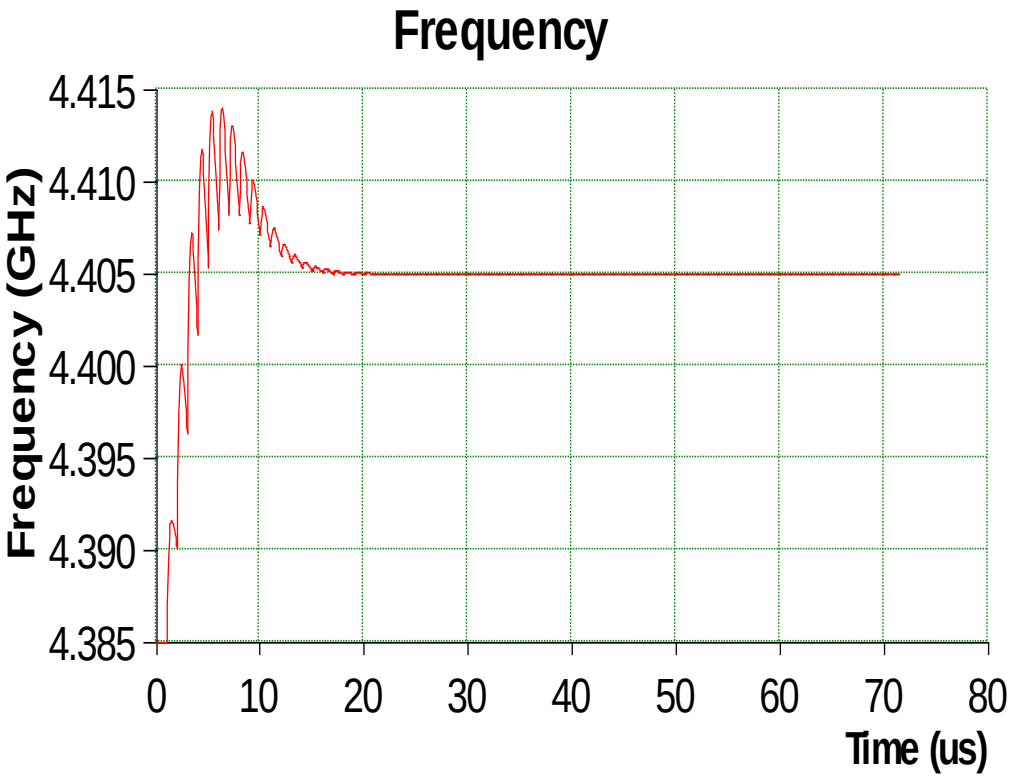


Figure 3.11: PLL Step response (adapted from Leopold et al, 2022)

3.7 Summary

This chapter covered the methodology used to design the C-band to L-band downconverter for a CubeSat receiver front-end. The design specifications for the downconverter are established. A superheterodyne receiver architecture was chosen for the single stage downconverter system design block diagram. This COTS configuration was chosen in addition to minimise design complexity associated with high frequencies, as well as implementation cost and time. The downconverter is designed to operate at C-band of 5.650—5.670 GHz, LO frequency band of 4.385—4.4 GHz and L-band IF of 1.2650 —1.2670 GHz. The WhatIF frequency planner tool from Keysight was introduced as an effective frequency planning tool to optimise signal quality and to manage / mitigate potential interference from nearby spurs. A system level / cascade analysis was performed to assess the overall performance of the downconverter. A system gain of 53.79 dB and NF of 3.44 dB values were calculated using the SySCalc6 simulations software. Suitable COTS such as amplifiers, filters, mixers, and PLL parts were carefully selected for the downconverter system. Design details are presented and simulations performed to validate their functionality and optimised to realize the design specifications. The insight from this chapter paves the way for the subsequent phase of constructing and measuring the downconverter as detailed in the following chapter.

CHAPTER FOUR : IMPLEMENTATION AND PERFORMANCE VERIFICATION

4.1 Introduction

Chapter 4 details the construction and measurements of the downconverter subsystems and the integrated downconverter system. Altium software is used to design the schematics (make suitable symbol for each part, create and assign footprint to each part). Thereafter the PCB layout is designed, Gerber and manufacturing files are generated, as well as bill of materials (BOM). Components are ordered and the PCB is manufactured. The downconverter is built, debugged and functionally tested to verify its performance /specification. Finally the results are compared between the simulated and the measured and then validated with some past studies.

4.2 Downconverter Subsystems Fabrication and Performance Evaluation

The downconverter subsystems detailed construction and measurements are presented as follows.

4.2.1 RF Front-end VMMK3803 LNA Implementation and Measurements

The constructed downconverter RF stage LNA is depicted in Figure 4.1. The PCB layout was designed in Altium designer software and manufactured on Rogers RO4003C double-sided high frequency substrate. Through-hole plated vias were incorporated in the circuit to connect the bottom layer ground plane to the top layer ground plane. Via placement is an effective technique used for preventing the formation of ground loops which causes unwanted feedback and instability in high frequency circuits. SMA connectors were used for input and output port terminations. The LPKF Laser & Electronics rapid prototyping machine was used to manufacture the PCB's. Agilent Technologies 8753ES 30 kHz - 6 GHz vector network analyser (VNA) was used to measure the circuit response in terms of S-parameters (S_{11}, S_{21}, and S_{22}). A full two port calibration was performed on the VNA using the Agilent 85033D 3.5 mm calibration kit and the SOLT (Short-Open-Load-Thru) calibration procedure. Calibration is a crucial first step used for equipment test setup to account for any losses associated with cables losses, and to setup the equipment to measure over a wide frequency range and points. The S-parameter measurements were performed at the RF center frequency of 5.66 GHz by connecting a 3V DC power supply and connecting port 1 of the VNA to the input port of the LNA and port 2 of the VNA to the output of the LNA. The NF performance of the LNA was done using the Agilent N8974A 10 MHz to 18 GHz series noise figure analyser. The measurements were performed by first calibrating the NF analyser, powering the LNA with a low noise DC power supply, connecting port 1 of the NF analyser to the input port of the Agilent N4001A 10 MHz to 18 GHz series noise source, connecting the noise source output to the input of the

LNA and connecting the LNA output to port 2 of the NF analyser. The S_{11}, S_{22}, Gain (S_{21}), and NF measurements are respectively shown in Figures 4.2 and 4.3 and abridged in Table 4.1.

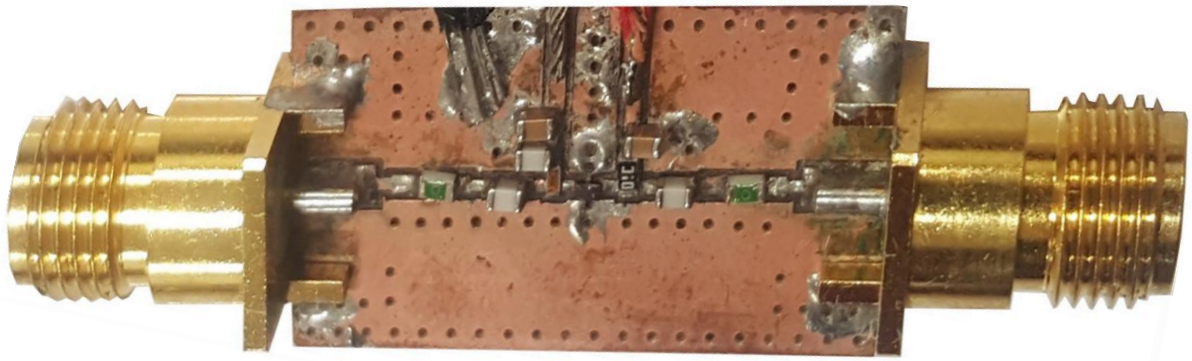


Figure 4.1: Constructed VMMK3803 LNA

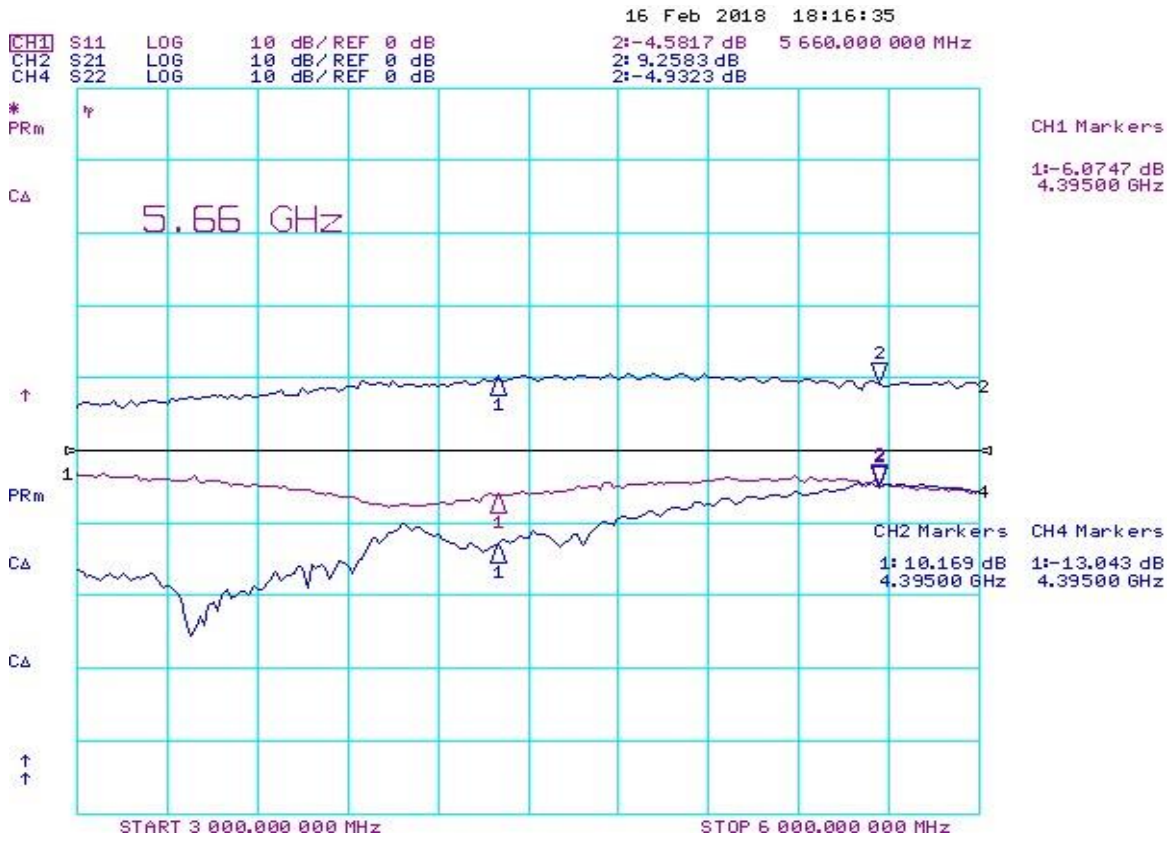


Figure 4.2: Measured power gain (S_{21}), S_{11} and S_{22} of the VMMK3803 LNA

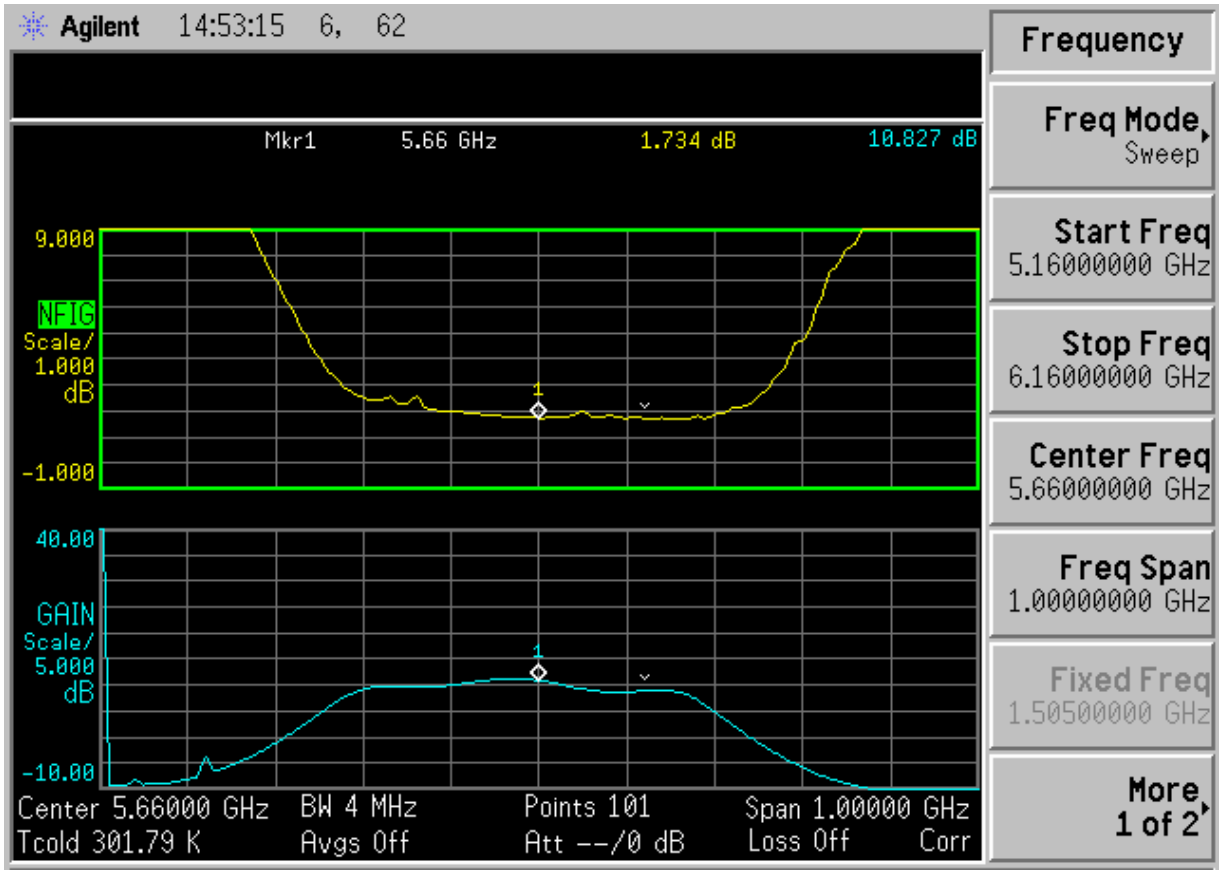


Figure 4.3: Measured noise figure *(NF) of* the VMMK3803 LNA

Table 4.1: Summary of measured results for the VMMK3803 LNA

Parameters	NF	Gain	S_{11}	S_{22}
Measured Results	1.734 dB	9.258 dB	−4.581dB	−4.932 dB

4.2.2 The Downconverter LO Buffer MGA665P8 Amplifier Implementation and Measurement

A buffer amplifier was implemented to boost the signal levels at various stages of the downconverter system. In this case it was required to boost the output power of the PLL based LO and is portrayed in Figure 4.4. The PCB layout was designed in Altium designer software and manufactured on Rogers RO4003C double-sided high frequency substrate. The ground connection was implemented using vias connecting the top and bottom ground planes. The amplifier was manufactured and tested in the similar manner as the LNA. The S-parameters and NF measurements were performed at the LO center frequency of 4.395 GHz. The measurements for S_{11}, S_{22}, Gain (S_{21}), and NF are shown in Figures 4.5 and 4.6 respectively and summarised in Table 4.2.

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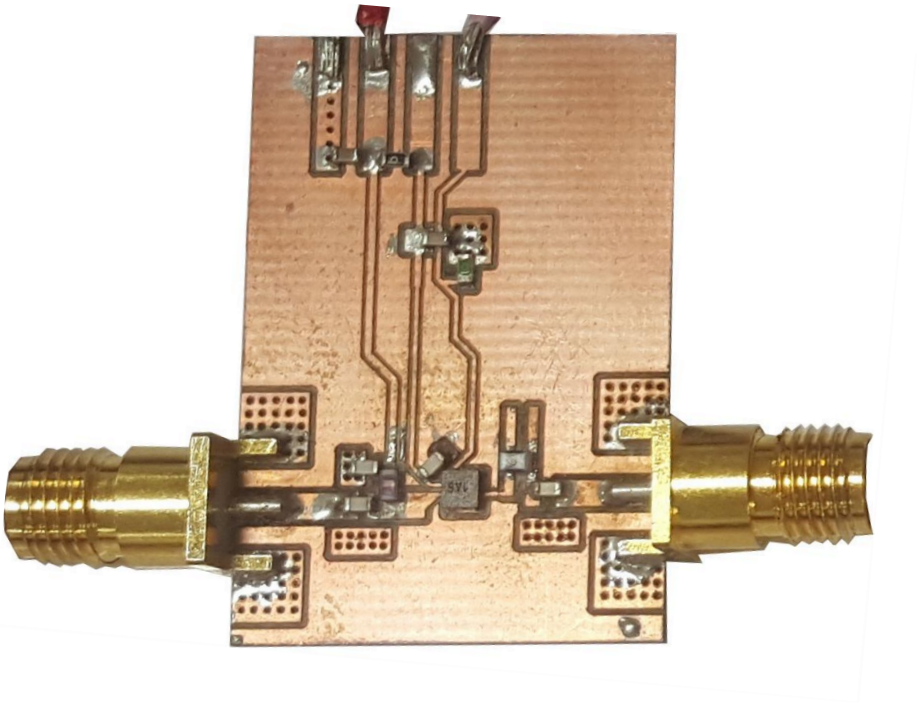


Figure 4.4: Constructed LO buffer MGA665P8 amplifier

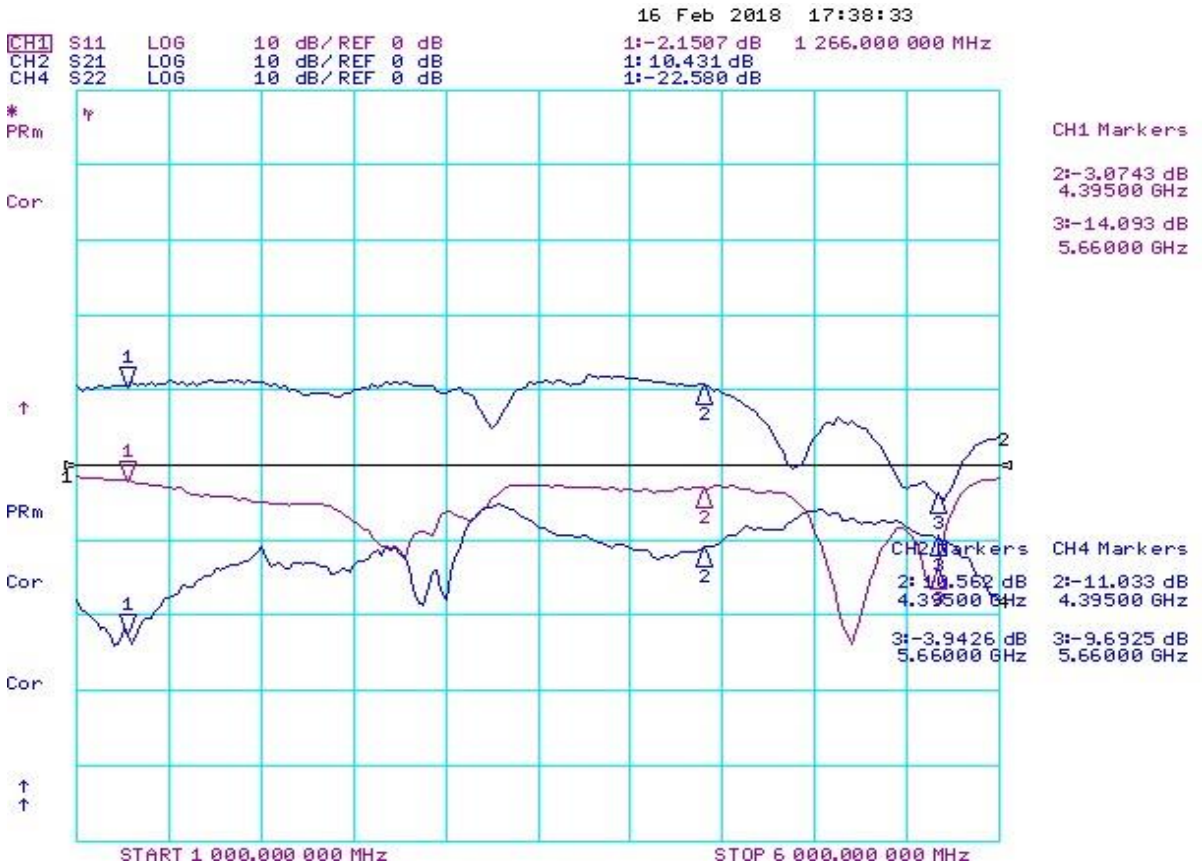


Figure 4.5: Measured power gain (S_{21}), S_{11} and S_{22} of the MGA665P8 LO buffer amplifier

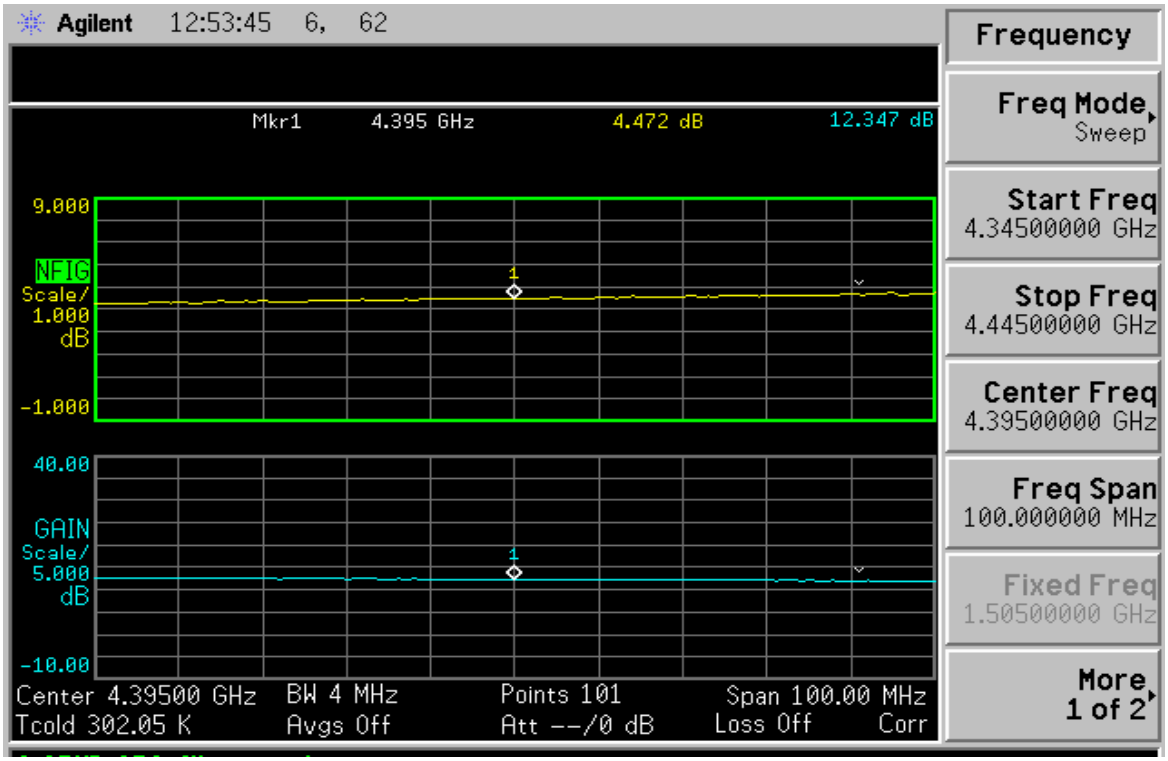


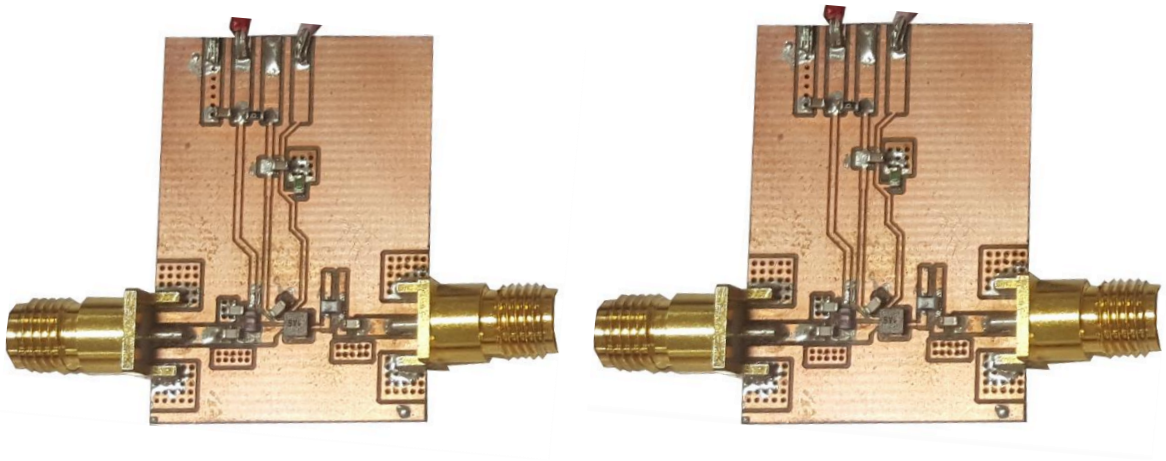
Figure 4.6: Measured noise figure (*NF*) of the MGA665P8 LO buffer amplifier

Table 4.2: Summary of measured results for the MGA665P8 LO buffer amplifier

Parameters	NF	Gain	S_{11}	S_{22}
Measured Results	4.472 dB	10.562 dB	−3.074dB	−11.033 dB

4.2.3 The Downconverter IF Stage MGA665P8 Amplifiers

In addition to the IF amplifier, a second (buffer) amplifier was required to increase gain at the IF stage (downconverter output). The MGA665P8 amplifier was implemented in both cases in order to save design time and cost. The constructed IF stage amplifiers are shown in Figure 4.7. The PCB layouts were designed in Altium designer software and manufactured on Rogers RO4003C double-sided high frequency substrate. The ground connection was implemented using vias connecting the top and bottom ground planes. The amplifiers were manufactured and tested in the similar manner as the LNA. The S-parameters and NF measurements were performed at the IF center frequency of 1.266 GHz. The measurements for gain (S_{21}), S_{11}, S_{22}, and NF are respectively shown in Figures 4.8 and 4.9 and abridged in Table 4.3. The IF amplifiers yielded the same results, hence only one amplifier results is presented.



(b)

Figure 4.7: Constructed IF stage MGA665P8 amplifiers: (a) IF amplifier and (b) IF buffer amplifier

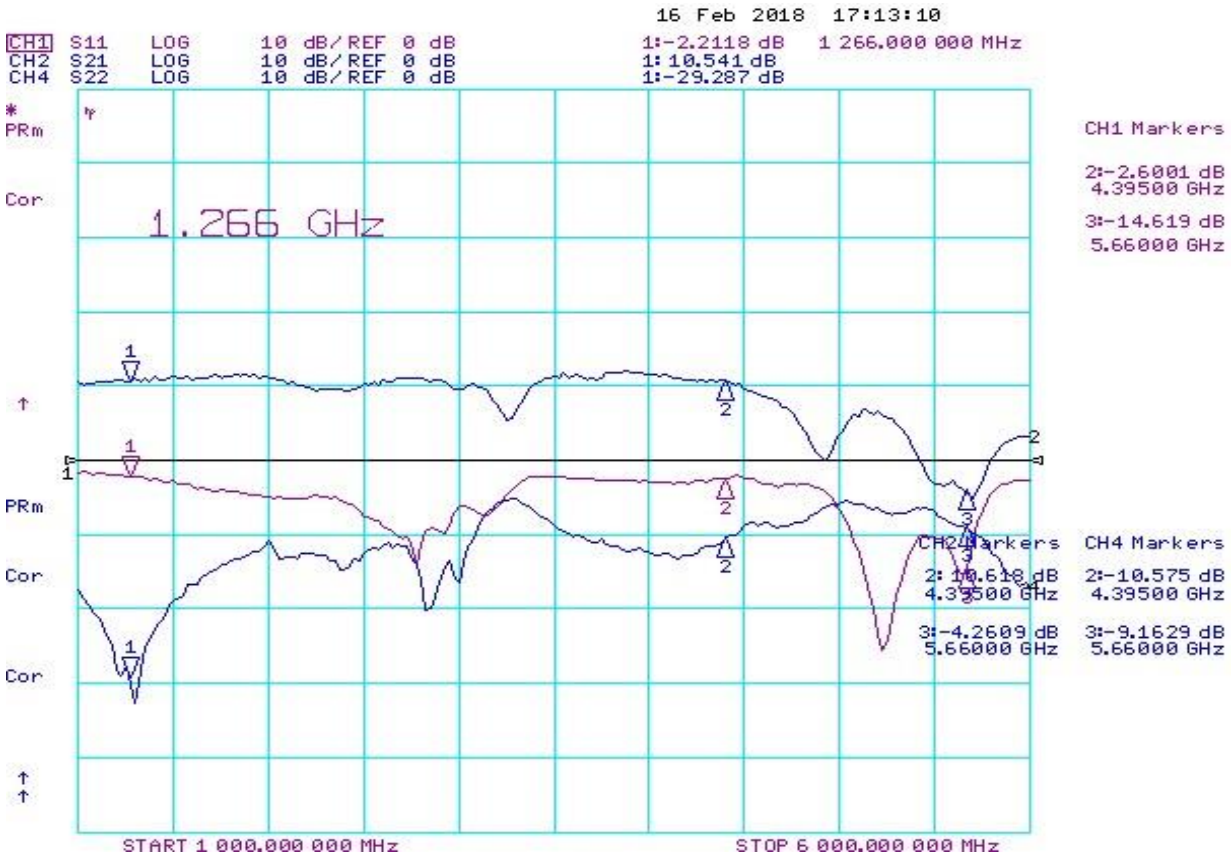


Figure 4.8: Measured power gain (S_{21}), S_{11} and S_{22} of the MGA665P8 IF stage amplifiers

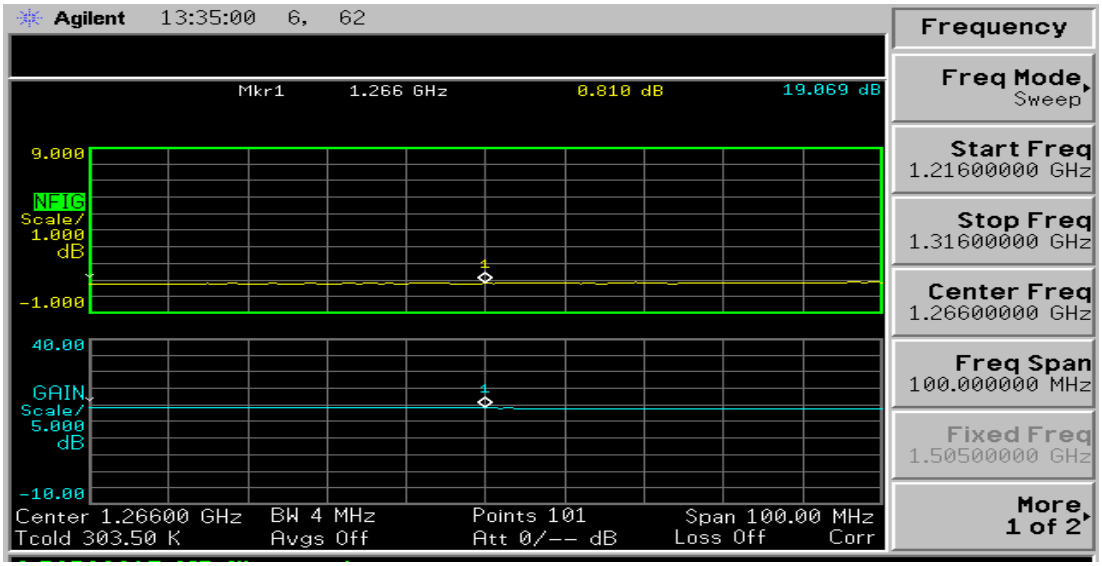


Figure 4.9: Measured noise figure (*NF*) of the MGA665P8 IF stage amplifiers

Table 4.3: Summary of measured results for the MGA665P8 IF stage amplifiers

Parameters	NF	Gain	S_{11}	S_{22}
Measured Results (IF amplifier)	0.810 dB	19.069 dB	−2.212dB	−29.287 dB
Measured Results (IF buffer amplifier)	0.810 dB	19.069 dB	−2.212dB	−29.287 dB

The amplifiers measured results for the downconverter RF, LO and IF stages are summarised in Table 4.4. The amplifiers meet the desired specification. The specified and measured results reasonably correlate. Factors that can contribute to the difference between the simulated and measured results are i) the dielectric losses of the substrate used to construct the PCB, ii) lumped component behaviour at high frequency and iii) perhaps the disturbances from power generators operated near the measuring equipment.

Table 4.4: Summary of the measured and specified amplifiers results for the downconverter RF, LO and IF stages

Parameters	VMMK3803 LNA		MGA665P8 LO Buffer Amplifier		MGA665P8 IF Stage Amplifiers		
	Specified	measured	Specified	measured	Specified	Measured (a)	Measured (b)
F_C(GHz)	3 - 11	5.66	0.5 - 6	4.395	0.5 - 6	1.266	1.266
Gain (dB)	10	9.258	16.99	10.562	18.4	19.069	19.069
***NF* (dB)**	1.5	1.734	1.45	4.472	1.2	0.810	0.810
S_{11} (dB)	-	−4.581	-	−3.074	-	−2.212	−2.212
S_{22} (dB)	-	−4.932	-	−11.033	-	−29.287	−29.287

4.2.4 The Downconverter RF COTS BPF Construction and Measurements

The RF BPF was isolated from the rest of the downconverter circuit and its response measured using a VNA. The VNA used for the circuit measurements is the Agilent 8753ES 30 kHz - 6 GHz network analyser and the Agilent 85033D 3.5 mm calibration kit was used for calibration. The PCB layout was designed in Altium designer software and manufactured on Rogers RO4003C double-sided high frequency substrate. The ground connection was implemented using vias connecting the top and bottom ground planes. The constructed RF BPF filter is pictured in Figure 4.10 and its measured findings are depicted in Figure 4.11 and summarised in Table 4.5. The measurement was done at the RF center frequency of 5.66 GHz indicating that the filter is operating at the desired frequency. The measured S_{11} value of -20.341 dB is lower (more negative) than the simulated S_{11} value of -16.250 dB, indicating that the filter has better return loss or impedance matching in the measured data. A lower S_{11} value is generally better because it means less power is reflected back to the source. The measured S_{21} of -1.5295 dB is better than the simulated value of -1.735 dB which indicates the filter's insertion loss (1.5295 dB) and signifies that less signal power is lost as it passes through the filter. Overall, the simulated and measured results correlated well.

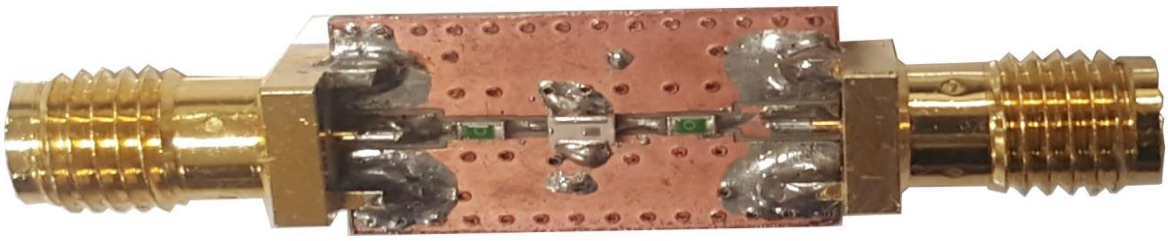


Figure 4.10: Constructed RF COTS BPF

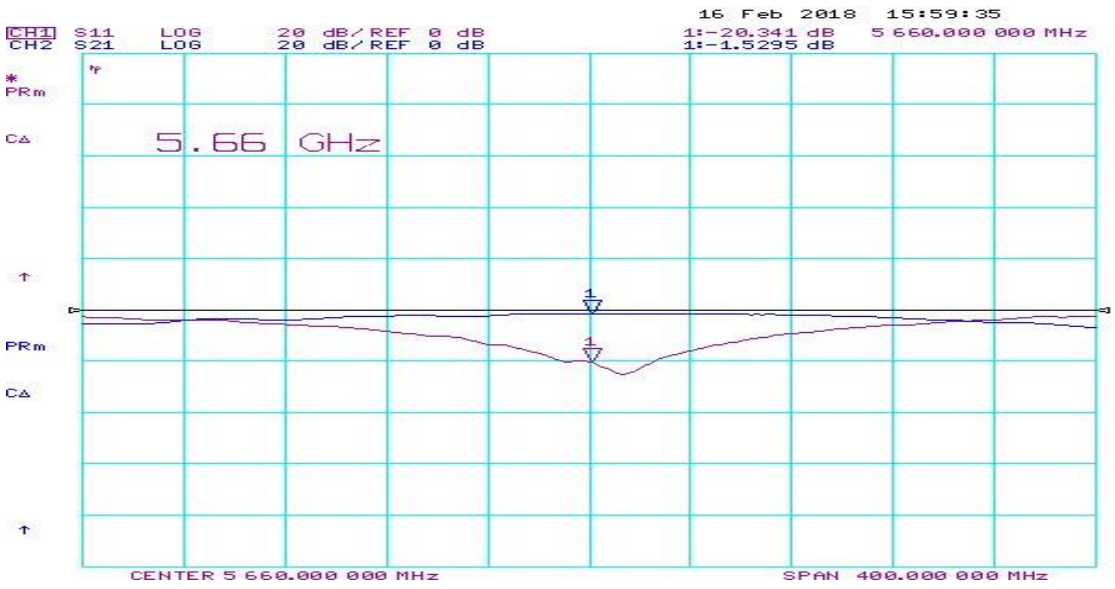


Figure 4.11: Measured S_{11} and S_{21} of the RF BPF

Table 4.5: Summary of the simulated and measured results for the RF BPF

Parameter	Simulated	Measured
F_C(GHz)	5.66	5.66
S_{11} (dB)	-16.250	-20.341
S_{21} (dB)	-1.735	-1.5295

4.2.5 The Downconverter IF SF2186E Saw BPF Construction and Measurements

The IF BPF was isolated from the rest of the downconverter circuit and its response measured using a Vector Network Analyser (VNA). The VNA used for the circuit measurements is the Agilent 8753ES (30 kHz - 6 GHz). The Agilent 85033D 3.5 mm calibration kit was used for calibration. The PCB layout was designed in Altium designer software and manufactured on Rogers RO4003 double-sided high frequency substrate. The ground connection was implemented using vias connecting the top and bottom ground planes. The constructed IF Saw BPF filter is depicted in Figure 4.12 and its measurements are shown in Figure 4.13 and summarised in Table 4. 6.

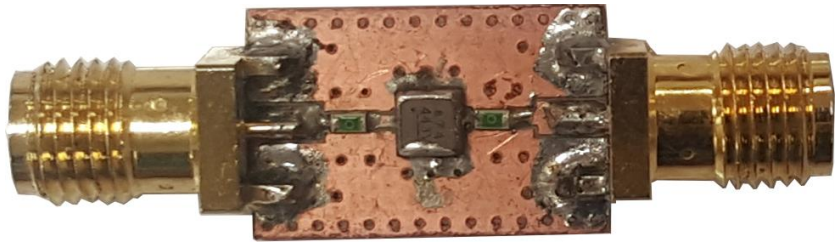


Figure 4.12: Constructed IF SF2186E saw BPF

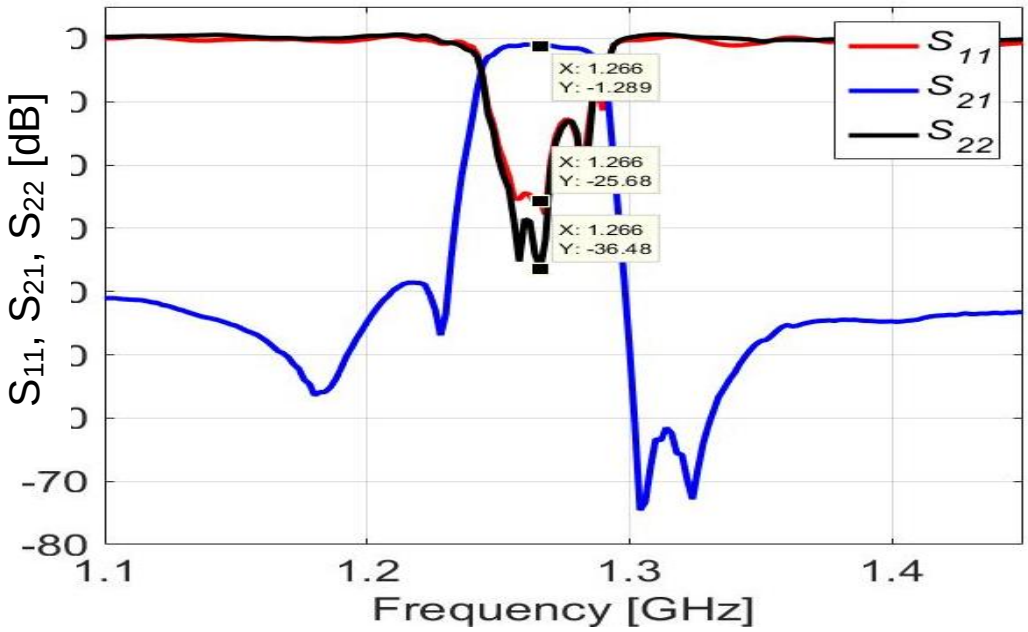


Figure 4.13: Measured S_{11} and S_{21} of the IF SF2186E saw BPF

Table 4.6: Summary of the simulated and measured results for the IF SF2186E saw BPF

Parameter	Simulated	Measured
F_C(GHz)	1.265	1.266
S_{11} (dB)	-24.778	-25.68
S_{21} (dB)	-1.276	-1.289

The measurement was done at the IF center frequency of 1.266 GHz indicating that the filter is operating at the desired frequency. The simulated and measured center frequencies are very close, with only a slight difference, indicating that the filter is operation within the desired frequency band. The measured S_{11} value of -25.68 dB is more negative than the simulated value of -24.778 dB which is favourable and indicates better return loss or impedance matching. In this case, the measured return loss is slightly better than the simulated value. The measured S_{21} value of -1.289 dB is slightly less than the simulated value of -1.276 dB. This value indicates the filter insertion loss (attenuation) of 1.289 dB. However, the difference is minimal and or negligible indicating that that the insertion loss is consistent between the simulation and the measurement. The bandwidth is narrow, and the stopband shows an excellent attenuation of signals outside the passband including the image signal. Overall, the simulated and measured results correlated well. It is worth mentioning that after the simulations and designs were done, it was realised that the image reject filter (BPF2) has little performance effect. This is likely due to BPF1 and BPF3 good designs performance in suppressing the 3.13 GHz image signal. As a result, BPF2 was left out in the final BPF designs and constructions.

4.2.6 The Downconverter MCA-12GL+ Mixer Construction and Measurements

The mixer PCB layout was designed in Altium designer software and manufactured on Rogers RO4003C double-sided high frequency substrate. The ground connection was implemented using vias connecting the top and bottom ground planes. SMA connectors were used for RF, LO and IF port terminations. The mixer performance was measured using Agilent N5183A MXG analog signal generator to generate frequencies in the RF range connected to the RF mixer port. A second signal generator for frequencies in the LO frequency range was connected to the LO mixer port and the IF mixer port connected to Agilent N9010A spectrum analyser. The RF and LO signal power levels were set as required for the downconverter. The constructed MCA-12GL+ Mixer is illustrated in Figure 4.14 and its measured results are respectively depicted in Figures 4.15 and 4.16 and summarised in Table 4.7.

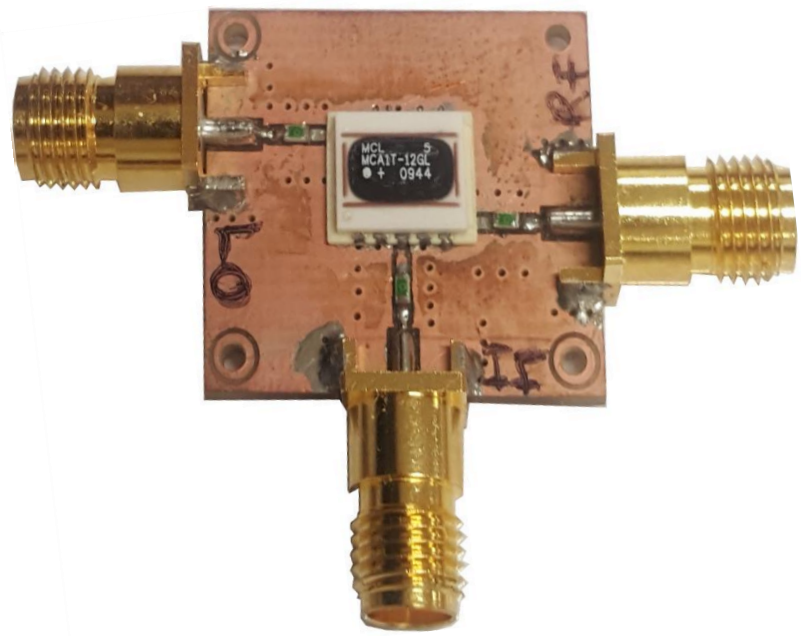


Figure 4.14: Constructed MCA-12GL+ mixer

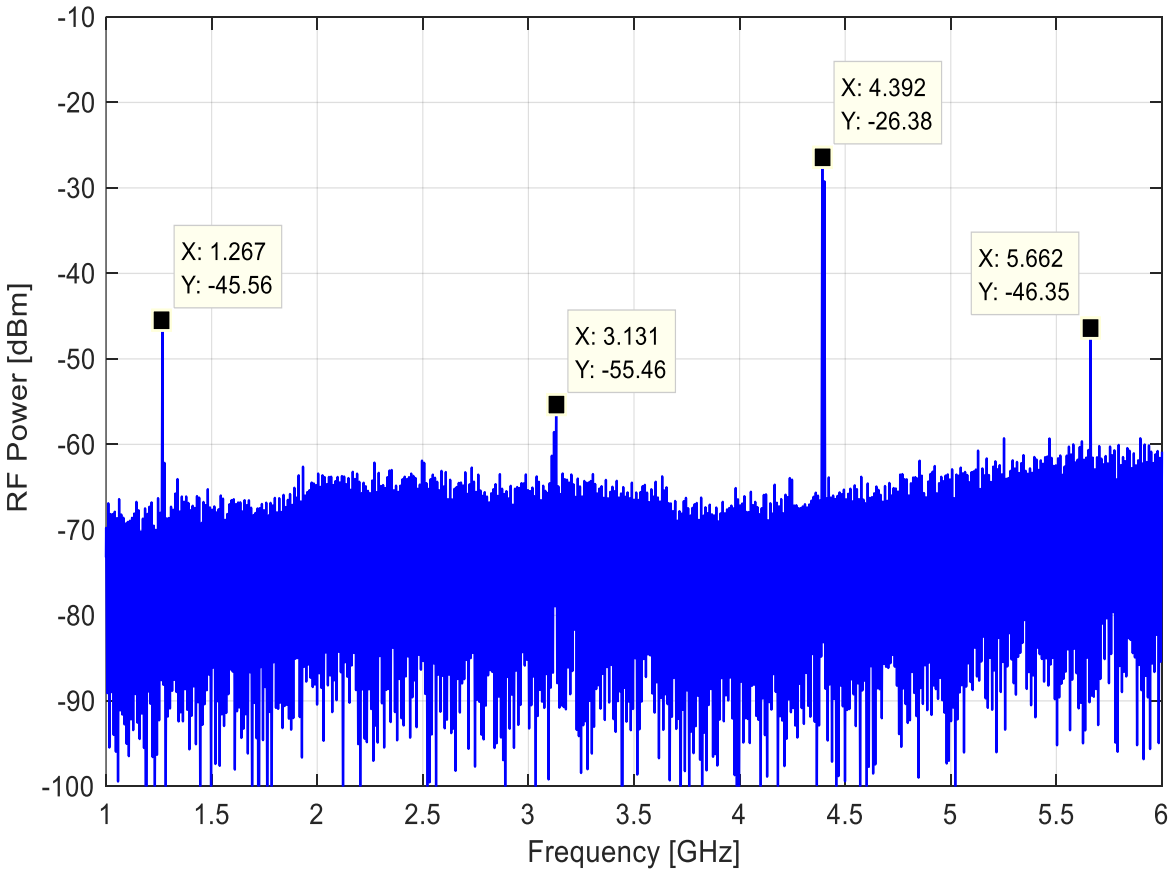


Figure 4.15: MCA-12GL+ mixer measured response (MATLAB plot)

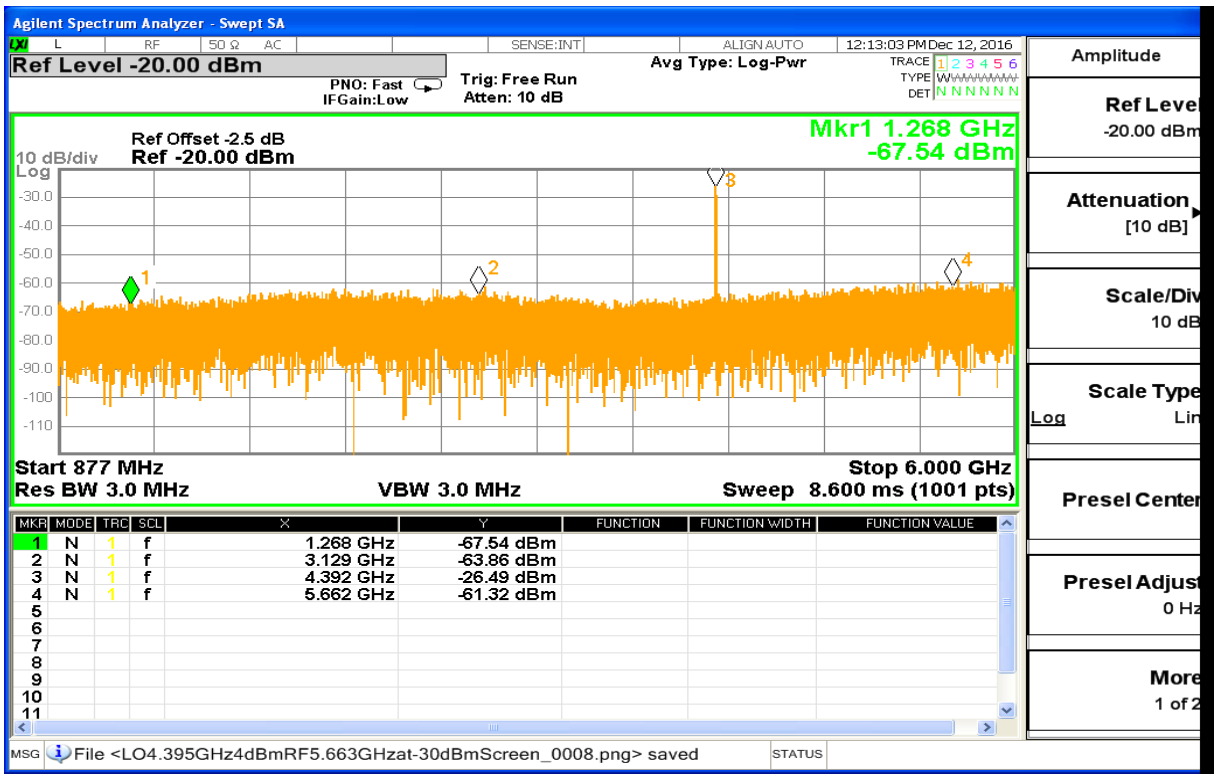


Figure 4.16: MCA-12GL+ mixer measured response (screenshot)

Table 4.7: Summary of the specified and measured results for the MCA-12GL+ downconverter mixer

Parameter	MCA-12GL+ Mixer	
	Specified	Measured
F_{RF} (GHz)	3.8 - 12	3.8 - 6
F_{LO} (GHz)	3.8 - 12	3.8 - 6
F_{IF} (GHz)	DC - 1500	DC - 1500
***Conversion Loss* (dB)**	6.8 – 8.5	6
LO Power (dBm)	+4	4.39

The MCA-12GL+ mixer accepts RF signals from 5650—5670 MHz and LO signals from 4385—4405 MHz at a nominal level of +4 dBm to produce IF output signals from 1250—1270 MHz. Several frequencies are generated at the mixer output port as shown in the output spectrum and these include the desired signals and the undesired image frequency present at 3.13 GHz as calculated in Section 3.5. The mixer performed frequency downconversion with typical conversion loss of 6 dB. The mixer's conversion loss performed consistently well with frequencies at other LO drive levels. The variation with LO drive power is negligible across the 20 MHz measured bandwidth. Overall, the mixer exhibits the desired conversion gain at different LO frequencies.

4.2.7 Downconverter PLL Implementation and Measurements

The PLL was isolated from the rest of the downconverter circuit and its response measured using Agilent A5052B signal source analyser. The implemented PLL is shown in Figure 4.17 and highlighted in red in Figure 4.26. The practical measurement as well as the testing setup is portrayed in Figure 4.18 and the practical measurement results are pictured in Figures 4.19 − 4.25. The PLL phase noise results and the overall PLL results are respectively summarised in Tables 4.8 and 4.9.

The test setup to measure phase noise and spurious frequencies requires the following equipment:

- Microcontroller for programming the synthesizer chip.
- Spectrum analyser.
- Oscilloscope.
- Low noise 6V DC power supply.
- Agilent A5052B signal source analyser.
- Device under test (DUT): PLL.
- 50 ohm input and output port terminations.
- RF surface mount (UFL) connectors were utilised at different stages of the downconverter, in this case to isolate the PLL subsystem from the rest of the downconverter circuitry to ease testing.

A detailed code used to control the ADF4107 PLL synthesizer chip is included in Appendix A. A summary of the programming details/settings are as follows:

- Frequency range: 4385 - 4405 MHz.
- Output frequency: 4395 MHz.
- Fref: 10 MHz.
- PFD: 1 MHz.
- Channel spacing: 1 MHz.
- P/P+1:32/33.
- Reference divider (R counter): 10.
- Main divider (B counter): 137.
- Main divider (A counter): 11.
- Latches/Registers.
- R counter latch: 0x28.
- N counter latch: 0x8929.
- Function latch: 0x9F8082.

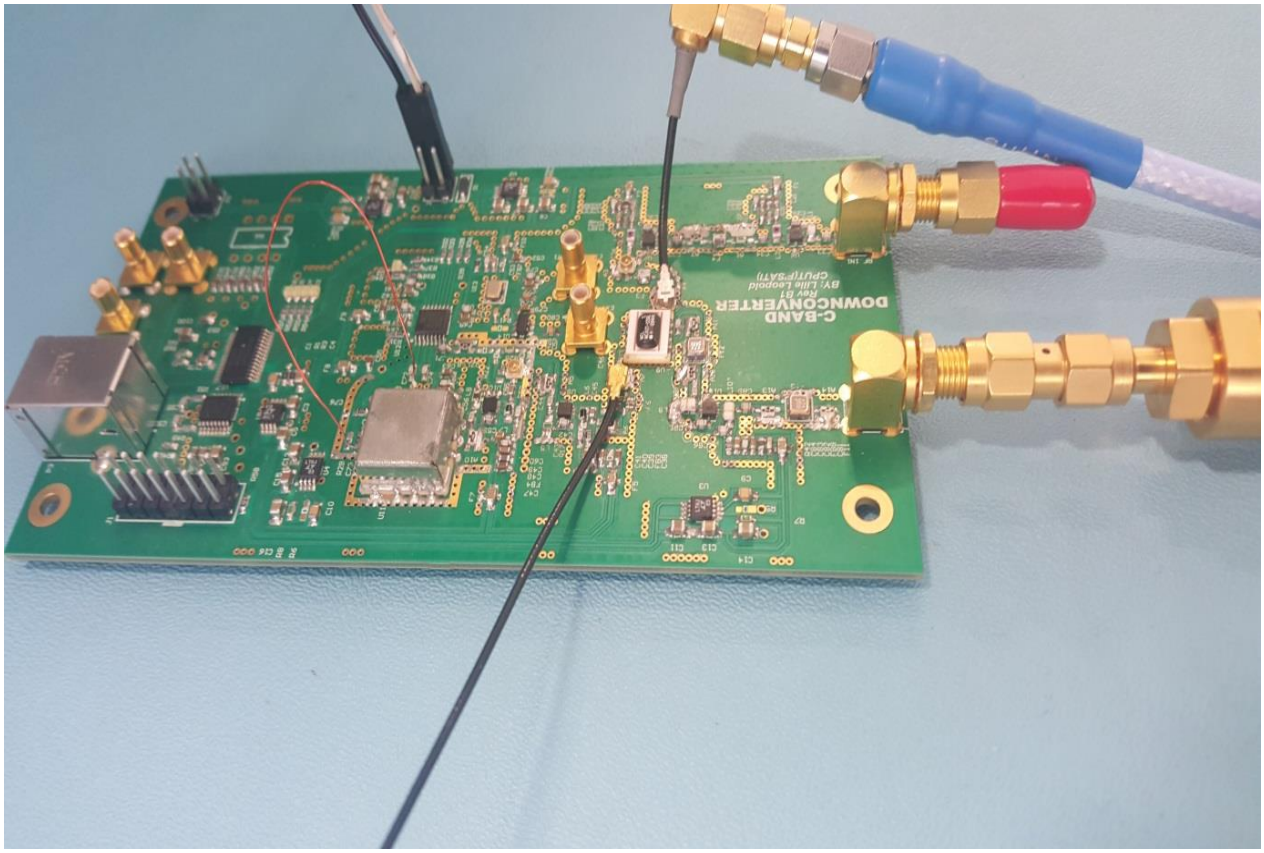


Figure 4.17: Constructed PLL subsystem

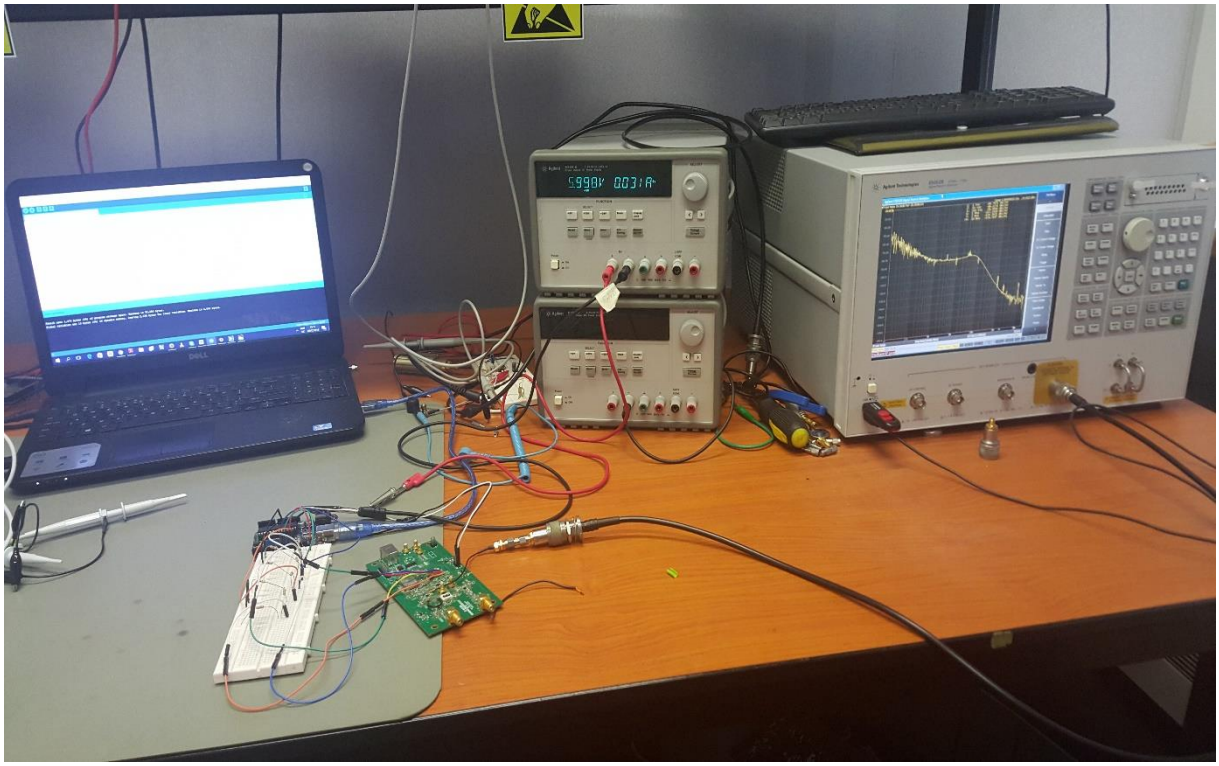


Figure 4.18: PLL laboratory test setup (adapted from Leopold et al, 2022)

4.2.7.1 Phase Noise Measurements

The phase noise measurements were done at 4.385 GHz, 4.395 GHz and 4.405 GHz, as exemplified respectively in Figure 4.19 – 4.21 as well as summarised in Table 4.8.

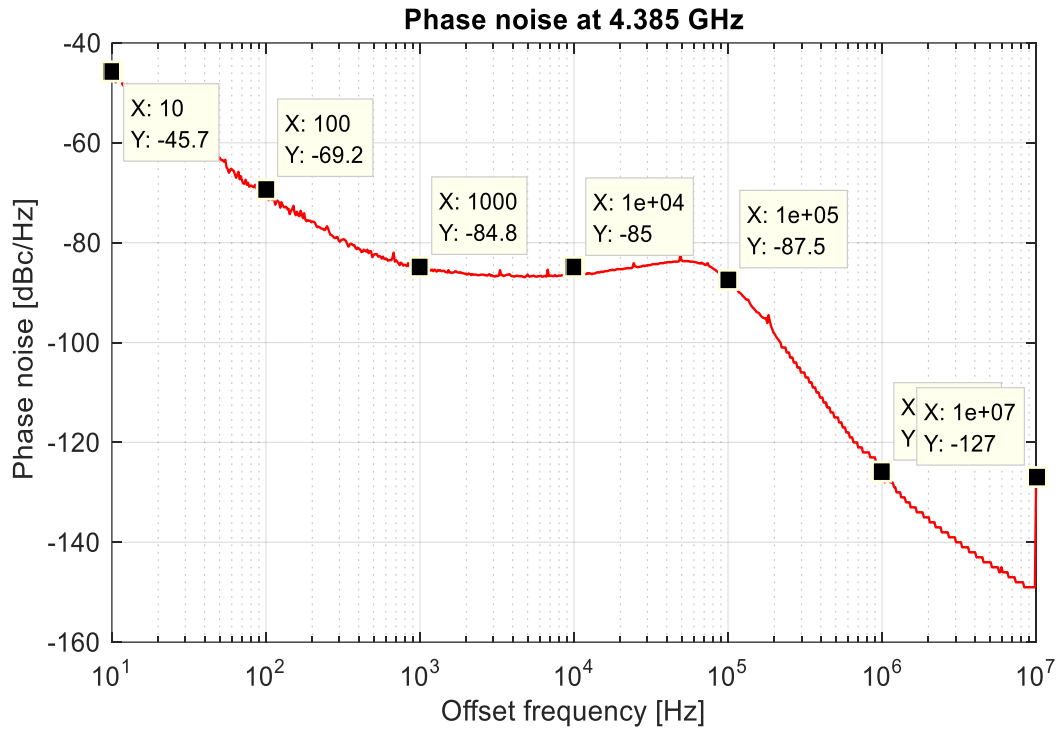


Figure 4.19: Measured PLL phase noise at 4.385 GHz (adapted from Leopold et al, 2022)

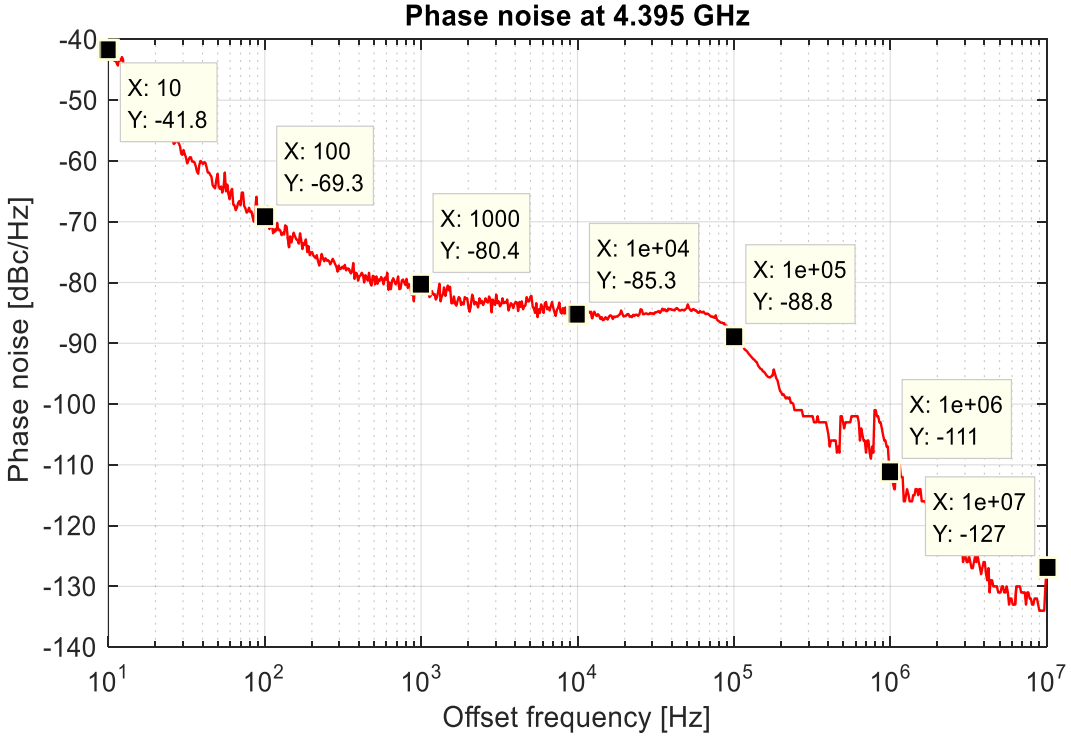


Figure 4.20: Measured PLL phase noise at 4.395 GHz (adapted from Leopold et al, 2022)

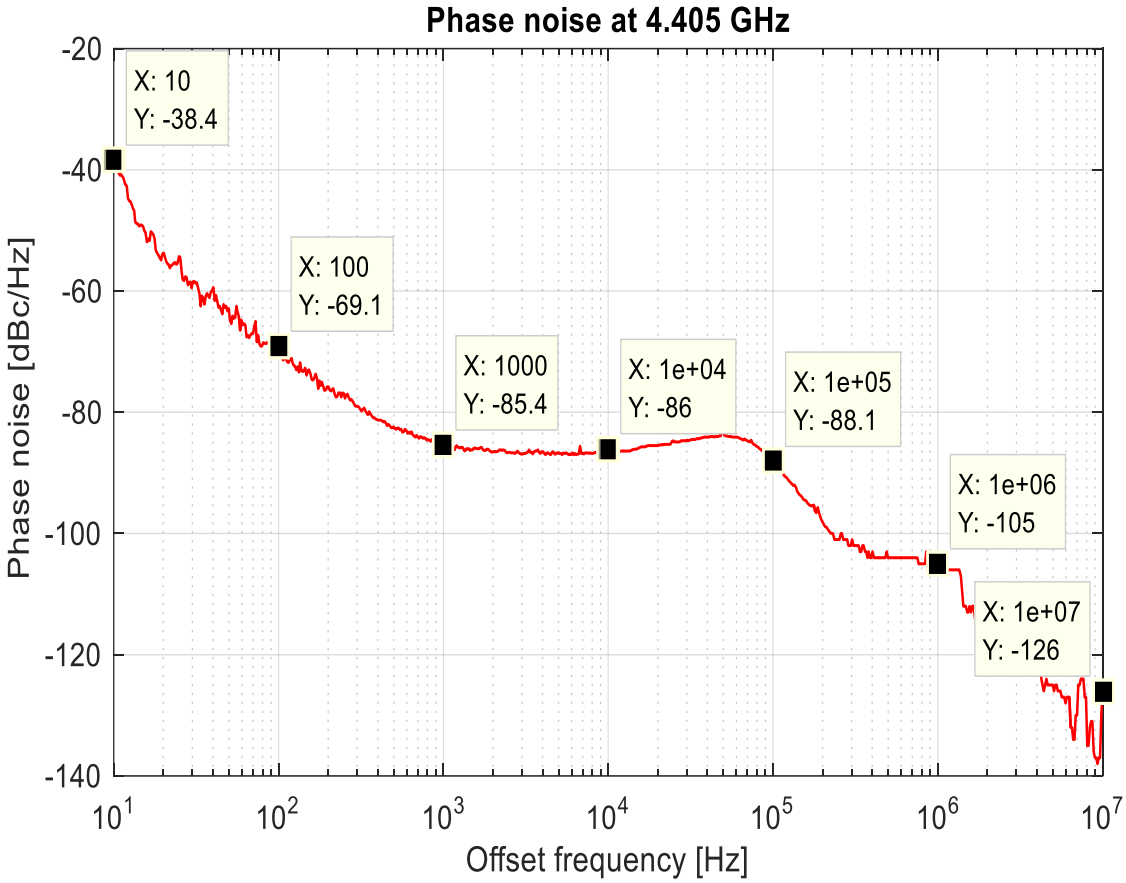


Figure 4.21: Measured PLL phase noise at 4.405 GHz (adapted from Leopold et al, 2022)

Table 4.8: Summary of the measured PLL phase noise at different frequency offsets (adapted from Leopold et al, 2022)

Frequency (MHz)	Phase noise (dBc/Hz) at frequency offsets +25°C						
	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	1 MHz	10 MHz
4385	−47.07	−69.02	−84.08	−85.00	−87.05	−126.00	−127.00
4395	−41.08	−69.03	−80.04	−85.03	−88.08	−111.00	−127.00
4405	−38.04	−69.01	−85.04	−86.00	−88.01	−105.00	−126.00

4.2.7.2 Harmonic Suppression Measurement

The harmonic suppression measurement was done at 1 MHz offset from a 4.395 GHz carrier, as exemplified in Figure 4.22.

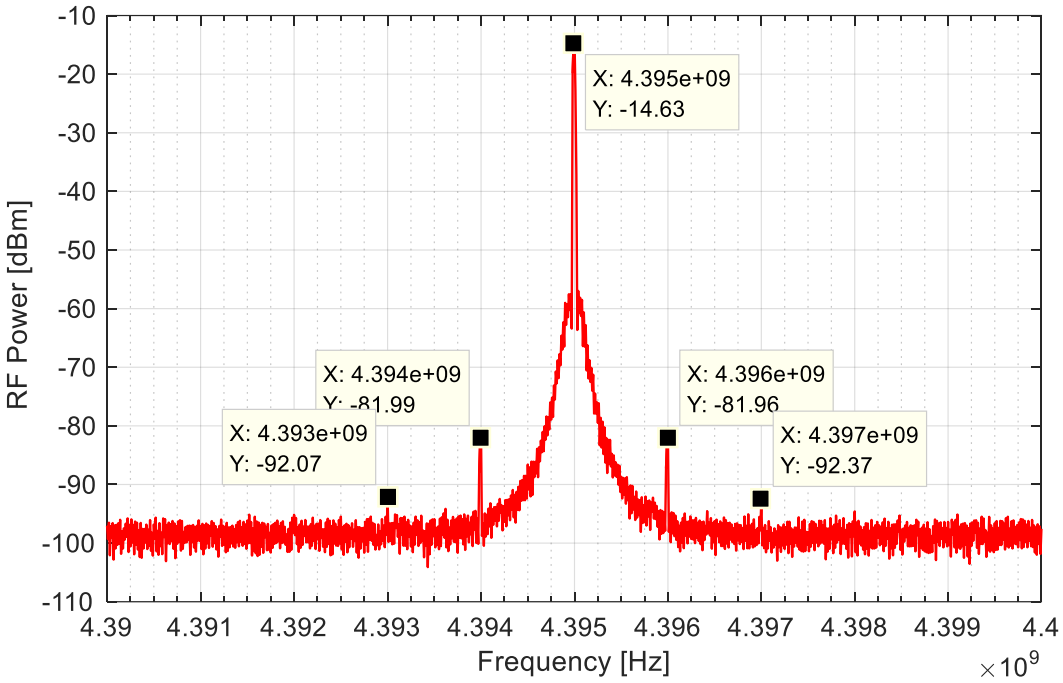


Figure 4.22: Measured harmonic spectrum of the PLL spur at 1MHz=-81.96 dBc (adapted from Leopold et al, 2022)

4.2.7.3 Output Power Measurement

The output power measurements were done at 4.385 GHz, 4.395 GHz and 4.405 GHz, as exemplified respectively in Figure 4.23 − 4.25.

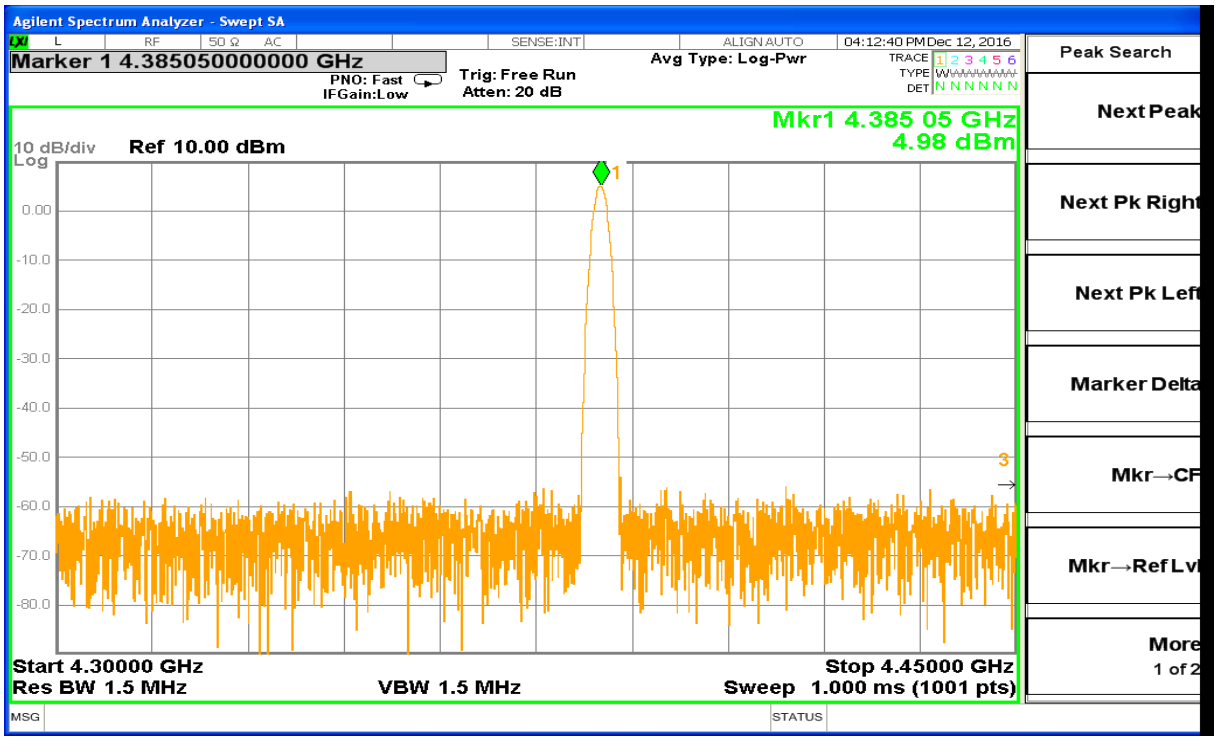


Figure 4.23: Measured PLL output power=4.98dBm at 4.385GHz (adapted from Leopold et al, 2022)

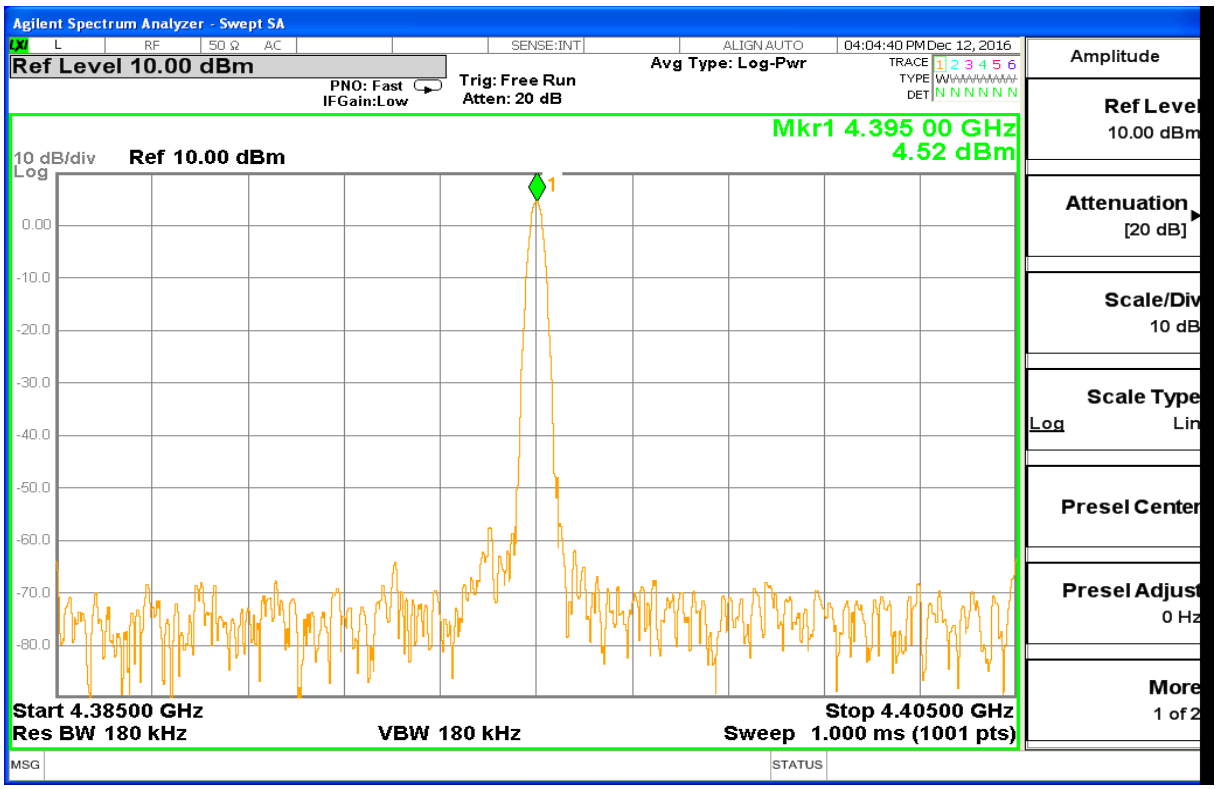


Figure 4.24: Measured PLL output power=4.52dBm at 4.395GHz (adapted from Leopold et al, 2022)

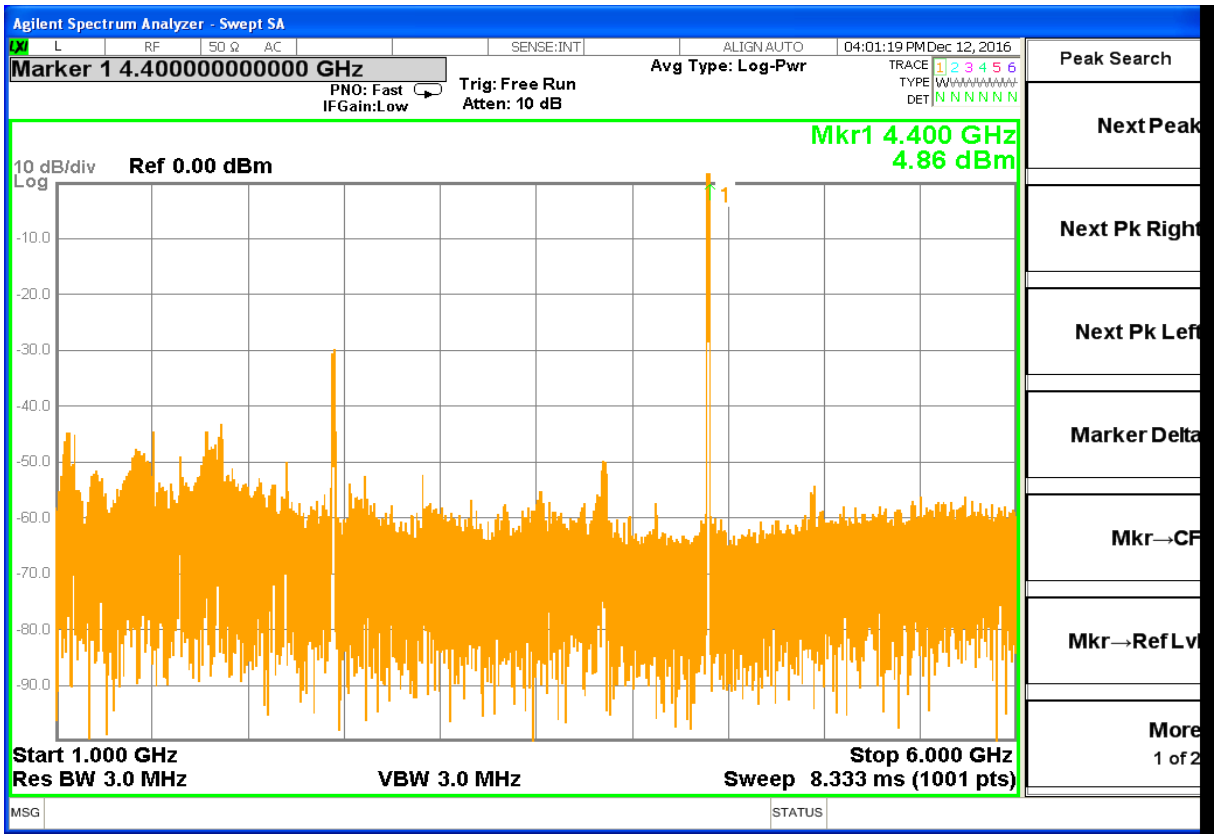


Figure 4.25: Measured PLL output power=4.86dBm at 4.400GHz (adapted from Leopold et al, 2022)

4.2.7.4 PLL Results Comparison, Analysis and Validation

The downconverter integer-N PLL was designed, simulated, constructed, and measured for a frequency range of 4.385 − 4.405 GHz with a step frequency of 1 MHz. The in-band phase noise and the out-band phase noise was respectively measured as -85.03 dBc/Hz and -111 dBc/Hz at 10 kHz and 1 MHz offsets from a 4.395 GHz carrier center frequency. Adequate output power of 4.52 dBm was achieved better than the 4 dBm specified to drive the mixer and a spurious response of -81.96 dBc/Hz. The results were validated as summarized in Table 4.10 (Leopold et al, 2022).

Table 4.9: Summary of the measured results for the PLL based oscillator (adapted from Leopold et al, 2022)

Parameter	Measured (this study)	Measured (Osmany et al, 2010)
Tuning frequency range (MHz)	4385 − 4405	0.64 – 4600
Output power (dBm)	4.52 − 4.98	-
F_{ref} (MHz)	10	-
Loop bandwidth (kHz)	70	10 – 200
Step frequency (MHz)	1	-
In-band phase noise (dBc/Hz) @10 kHz offset	-85.03 @ F_c=4.395 GHz	-105 @ F_c=3 GHz
Out-band phase noise (dBc/Hz) @1MHz ffset	-111 @ F_c=4.395 GHz	-122 @ Fc=3 GHz
Spurious response (dBc/Hz) @1MHz offset	-81.96 @ F_c=4.395 GHz	-70

4.3 Downconverter System Integration and Measurements

The implemented downconverter prototype is shown in Figure 4.26 highlighting the different subsystems. The PCB layout was designed in Altium designer software and manufactured on Rogers RO4003C 4-layer high frequency substrate. The PCB size is 68.453 mm x 130.175 mm. The detailed Altium schematics, PCB layout, BOM, PCB layer stack up information and PCB manufacturing instructions are included in Appendices B and C. Through-hole plated vias were strategically incorporated in the circuit to connect the multi-layer ground planes. SMA connectors were used for input and output port terminations. The experimental measurement and the modular testing setup are exemplified in Figure 4.27 and finally the practical measurement results are portrayed in Figures 4.28 and 4.29.

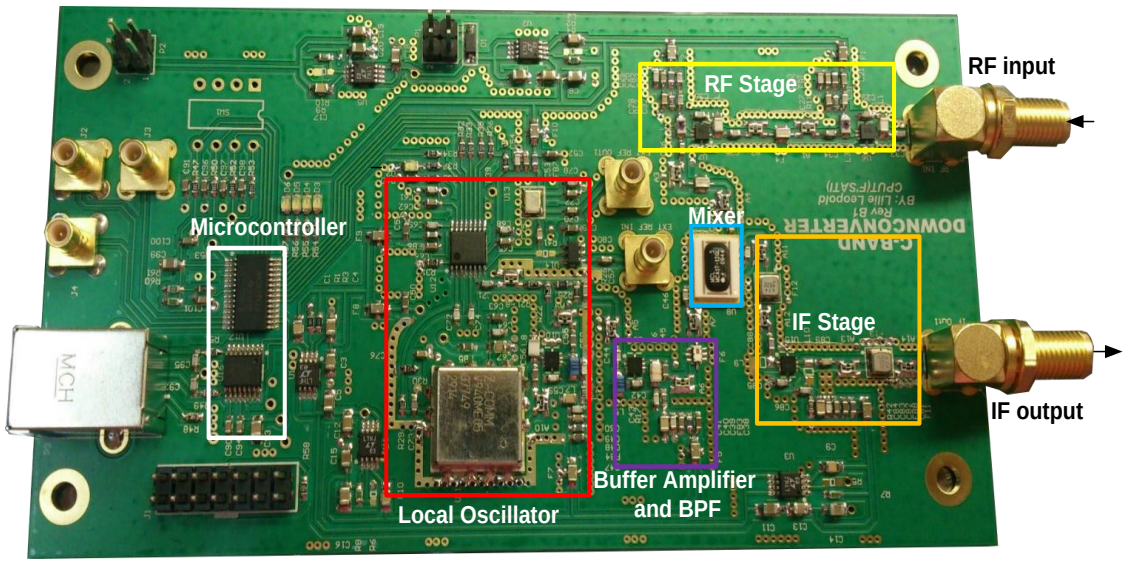


Figure 4.26: Fabricated downconverter prototype board (adapted from Leopold et al, 2022)

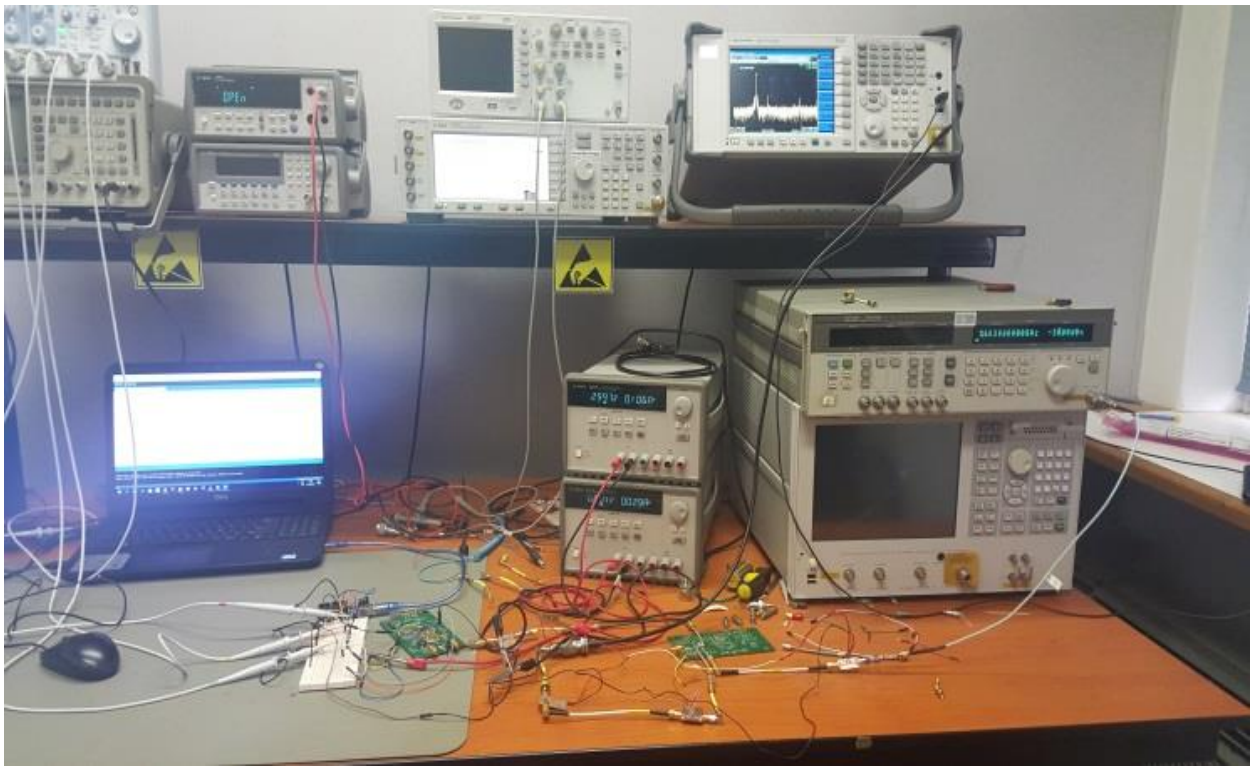


Figure 4.27: Modular downconverter laboratory test setup.

4.3.1 Downconverter System Noise Figure and Gain Measurements

The subsystem total noise figure and the gain performance measurements were done on the downonverter using the following equipment:

- Agilent N8974A 10 MHz – 18 GHz series noise figure analyser.
- Agilent N4001A 10 MHz – 18 GHz series noise source.
- 2 x SMA RF cables.
- Downconverter DC power cable.
- PC configured with downconverter control.
- Low noise 6V DC power supply.
- Device under test (DUT) downconverter.

The measurements were done by connecting the Agilent N4001A 10 MHz–18 GHz series noise source to the input port of the downconverter after the instrument was calibrated. The subsystem NF of 2.297dB and cascaded gain of 40.205dB were measured as displayed in Figure 4. 28.

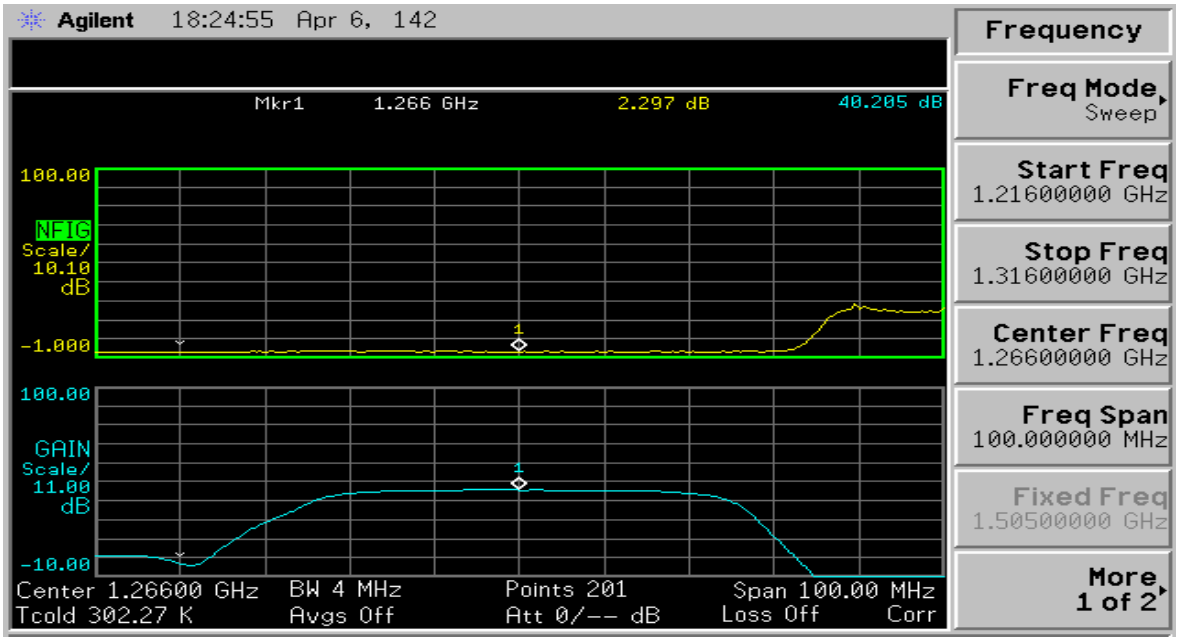


Figure 4.28: Measured downconverter subsystem noise figure response.

4.3.2 Downconverter System Output Frequency Spectrum Measurements

The following equipment were used to perform the output frequency spectrum measurements on the downconverter subsystem:

- Agilent N5183A MXG analog signal generator.
- Agilent N9010A spectrum analyser.
- 2 x SMA RF cables.
- Downconverter DC power cable.
- PC configured with downconverter control.
- DC power supply.

The measurements were done by using a signal source to inject a -43 dBm sinusoidal test signal at 5.66 GHz in the downconverter RF input port. The measurements were taken at the downconverter IF output port. The spectrum analyser was configured for a centre frequency of 1.268 GHz and the results is displayed in Figure 4.29. Spurious signals are likely due to the mixer non-linearities or LO leakage; however, these spurious signals are within acceptable limits for the downconverter application.

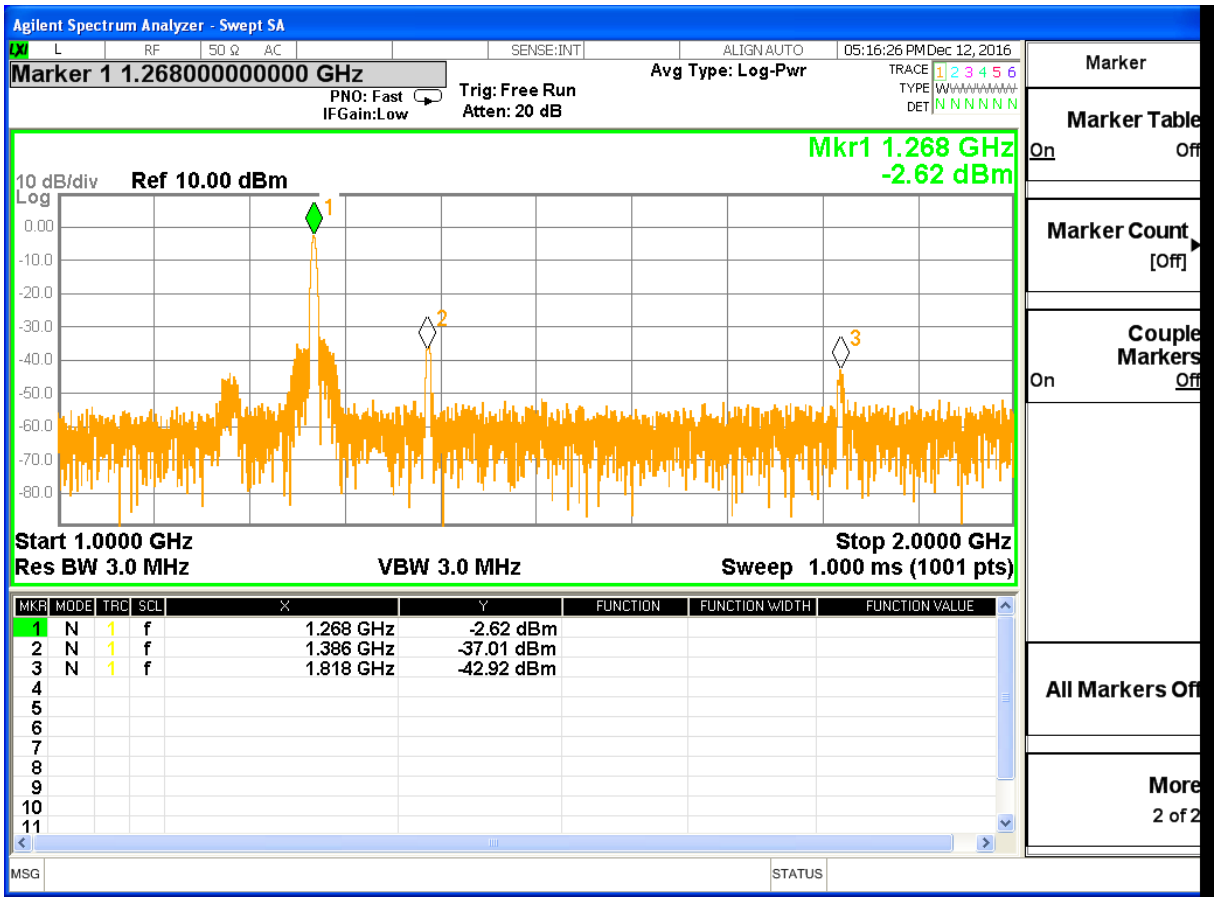


Figure 4.29: Measured downconverter subsystem output frequency spectrum response.

4.4 Comparison, Analysis and Validation of Results

The downconverter was implemented and measured for a RF frequency range of 5.650 − 5.670 GHz with a 5.66 GHz centre frequency, a LO frequency range of 4.385 − 4.405 GHz with a 1 MHz step frequency and an IF range of 1.250 – 1.270 GHz, an overall conversion gain of 40.205 dB, a noise figure of less than 2.3 dB, a PLL based local oscillator frequency from 4.385 – 4.405 GHz, an output power of 4.52 dBm, a spurious frequency response of -81.96 dBc/Hz, an out-band phase noise of -111 dBc/Hz at 1 MHz carrier frequency offset from a 4.395 GHz carrier and the L-band output frequency from 1.250 − 1.270 GHz centered at 1.268 GHz. DC current consumption from 3V DC power supply was 80.5 mA, while 29 mA was drawn from the 6V DC power supply, giving a total power consumption of 415.5 mW. This value is

below the specified value as expected because of the omitted second amplifier in the RF section of the downconverter due to sufficient system gain. In addition, this also impacted the downconverter overall gain and noise figure performance which were measured below simulated specifications in section 3.6. Study (Roy et al., 2020) was used to validate the results as abridged in Table 4.10.

Table 4.10: Comparison, analysis, and validation of results

Parameter	Specified	Measured (this study)	Measured (Roy et al., 2020)
RF Frequency Range (GHz)	5.650 – 5.670	5.650 – 5.670	5.8 − 7.0
IF Frequency Range (MHz)	1250 – 1270	1250 – 1270	215
LO Frequency Range (GHz)	4.385 − 4.405	4.385 − 4.405	6.415
Gain (dB)	>25	40.205	30
Noise Figure (dB)	<3	<2.3	<2.5
LO Output Power (dBm)	>4	4.52	1-5
Mixer Conversion Loss (dB)	7	6	7.5
DC power supply (V)	6 − 15	6 − 15	5 − 15
DC power consumption (W)	0.492	0.415	0.7
LO Step Frequency (MHz)	1	1	-
LO In-band Phase Noise (dBc/Hz) @10 kHz Offset	< -70	-85.03 F_c=4.395 GHz	-
LO Out-band Phase Noise (dBc/Hz) @1MHz Offset	< -100	-111 F_c=4.395 GHz	-
LO Spurious Response (dBc/Hz) @1MHz Offset	Better than -60	-81.96 F_c=4.395 GHz	-

The presented downconverter demonstrates similar and different attributes with study (Roy et al., 2020), as each downconverter was done for a specific satellite mission. The selected carrier frequency falls in the amateur radio frequency C-band from 4—8 GHz, hence why this

study and Roy et al., 2020 have carrier frequency within that range. This C-band enables less interference and supports higher data rate. The downconverter system operates in the 5.650 to 5.670 GHz range with respect to the ground station transmitter. This downconverter system IF range is 1.250－1.270 GHz—which is generated when the PLL based LO generates a stable signal that mixes with the incoming RF signal to produce the IF. The specified LO frequency range is critical for maintaining the desired frequency conversion.

The PLL frequency range is 4.385－4.405 GHz. The capability of tuning the LO in steps of 1 MHz offers more flexibility in adjusting the local oscillator's frequency. The LO generates an output power greater than 4 dBm. This power is important to ensure that the LO signal is strong enough for mixing with the RF signal. The mixer has a conversion loss of 6 dB. Conversion loss is the loss of power that occurs during the mixing process. A lower conversion loss is preferred, as it indicates more efficient frequency conversion. The system has a gain of 40.205 dB. Gain indicates the amplification capability of the system. A higher gain is generally desired for improved signal strength. The system's noise figure is less than 2.3 dB. NF quantifies the system's ability to preserve the quality of the incoming signal in the presence of noise. A lower NF is better, as it indicates less degradation of the signal quality due to noise. LO in-band phase noise (dBc/Hz) @10 kHz offset: This is the measure of phase noise of the LO signal within the bandwidth of interest. Lower values indicate a cleaner and more stable LO signal. LO out-band phase noise (dBc/Hz) @1 MHz offset: This measures the phase noise of the LO signal at a frequency offset from the carrier frequency. Lower values are desirable to prevent interference with neighbouring channels. LO spurious response (dBc/Hz) @1MHz offset: This parameter describes unwanted signals or responses that appear in the LO output at a frequency offset. Lower values indicate better suppression of unwanted signals. These higher gain, lower noise figure, increased LO output power, superior phase noise performance, enhanced spurious response suppression, and broader RF and IF coverages, are what makes the receiver downconverter system unique. These improvements collectively contribute to improved signal quality, better interference rejection and overall enhanced performance in various RF applications and in this case, a CubeSat receiver downconverter.

4.5 Summary

This chapter detailed the construction process, implementation, and measurements for the downconverter. Amplifiers, filters, mixers, and PLL subsystems were implemented and tested individually before system level integration. Schematics and PCB’s layout were designed using Altium design software. The boards were built / soldered, debugged and functional testing was performed to verify the downconverter subsystems and overall downconverter system performance / design specifications. A comparison was made between the specified and measured results, as well as validated with a past study.

CHAPTER FIVE : CONCLUSIONS AND RECOMMENDATIONS

5.1 Introduction

This chapter concludes the study, summarises key findings and gives recommendations for future research. Refer to Appendix B for the design schematics and PCB layout and Appendix C for the PCB layer stack-up information and the manufacturing instructions.

5.2 Conclusions

CubeSats during overpass need to communicate with the ground station within a particular period and this must occur effectively within the uplink and downlink contact time-frames; if not, then until the next overpass. As a result, this research focused on a CubeSat downconverter subsystem, in which assorted spaceborne downconverters literature were analysed to determine the research gap and to find and employ profound practices. Consequently, a COTS based C-band downconverter was designed, constructed, tested and validated with the receiver performance parameters as follows; the input C-band frequency from 5.650 – 5.670 GHz centered at 5.66 GHz, an overall conversion gain of 40.205 dB, a NF of < 2.3 dB, a PLL controlled local oscillator frequency from 4.385 – 4.405 GHz, a 4.52 dBm output power, a spurious frequency response of -81.96 dBc/Hz, an out-band phase noise of -111 dBc/Hz at 1 MHz carrier frequency offset from a 4.395 GHz carrier and the L-band output frequency from 1.250 – 1.270 GHz centered at 1.268GHz. The chosen COTS solution provided a generic approach for both ground and spaceborne applications. The thesis contributions are i) an abridged literature analysis of progressive downconverters and bandpass filters for spaceborne applications, ii) a simplistic C-band downconverter implementation and framework that can be applied to design CubeSats receiver front ends and iii) two published conference papers and a submitted journal paper under peer review.

5.3 Recommendations

The following recommendations were made:

- A metal enclosure can be used on the downconverter board to provide RF isolation from other nearby electronics and to provide a thermal heat removal path.
- Designing with discrete components offers more flexibility and high performance but consumes more power and space.
- LNA’s are designed to minimise additional noise. Minimum additional noise can be achieved by choosing low-noise components, selecting the right operating points, and

selecting the right circuit topologies. Minimising additional noise must balance with other amplifier design goals such as power gain and impedance matching specifications.

- Integer-N or Fractional-N PLL with Integrated VCO are becoming more popular in recent years. The main difficulty is the inherently low Q resonators available on Silicon. The benefit is one single PLL VCO product that can cover over 2 decades of frequency range in one small 5 mm x 5 mm part. Low component count leads to lower system cost and power consumption critical in CubeSat system design applications.
- For best PLL in-band phase noise performance, use highest PFD frequency possible, because all in-band noise is multiplied by 20 log N. Hence, keeping N low is always good for integer N applications. Fractional-N is most suitable for high resolution applications (benefit).
- Better improvement for the in-band phase noise can be made by inserting the mixer in the place of the N-divider.
- Spurs and feed-throughs are very likely to occur. Different stages should be well isolated from each other to avoid coupling and feed-through.
- Optimise PLL loop filter. Wider bandwidths may improve in-band noise, (but at an expense of wideband noise). The optimal bandwidth gives the lowest root mean square (rms) jitter. Use a clean reference source. OCX's are best, but most expensive. XO's are inexpensive but drift over temperature and have varying performance. TCXO's are a good compromise.
- Consider an up-converted / multiplied DDS as a choice for a local source.
- Ensure adequate power supplies and decoupling as well as good RF layout practice.
- In RF design, it can be very problematic to overdrive the component. When components are over-driven to their operational limits in terms of trying to deliver too much power, distortion increases because parts start operating in the non-linear region of their operating range. Therefore, when looking for various components (mixers and amplifiers), it can be beneficial to find devices where the drive components are linear. This is one of the reasons why gain is spread out in a radio receiver. Also, every additional component added to the signal chain also adds noise.
- The downconverter system can further be optimised in terms of performance and can be integrated onto a single PC104 standard board with the rest of the receiver and transmitter circuitry to form a complete flight model radio/SDR.
- Even though the devices used in the research are commercially-of-the-shelf components manufactured for space use, a real-time space performance validation test including space radiations, extreme temperatures and pressures, vacuum, acoustics, shock and vibration as well as the Doppler frequency shift tests, were not performed in this study and these drawbacks are recommended for further research.

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APPENDICES

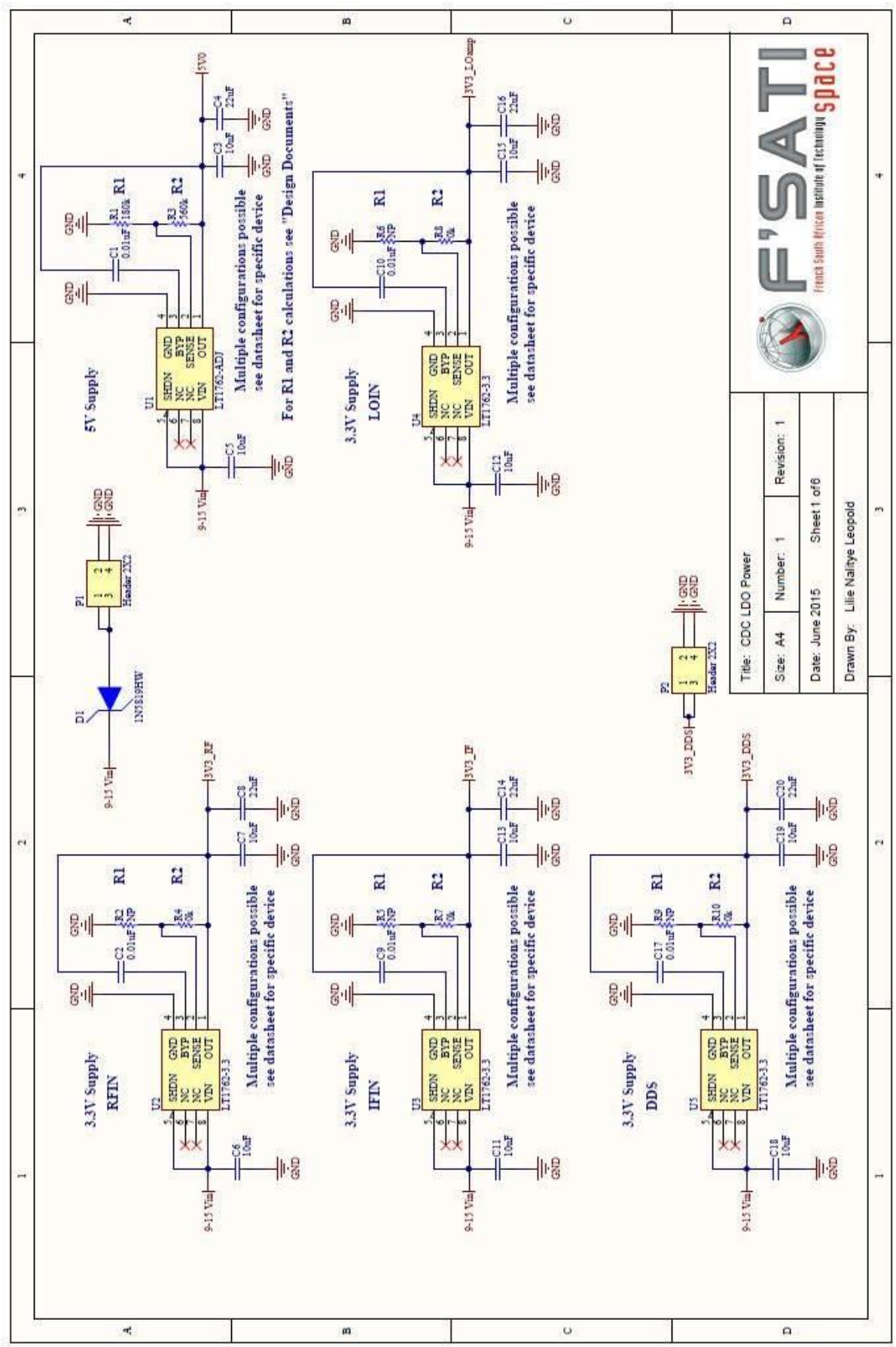
APPENDIX A: ADF4107 PLL Synthesizer Chip Configuration and Source Code

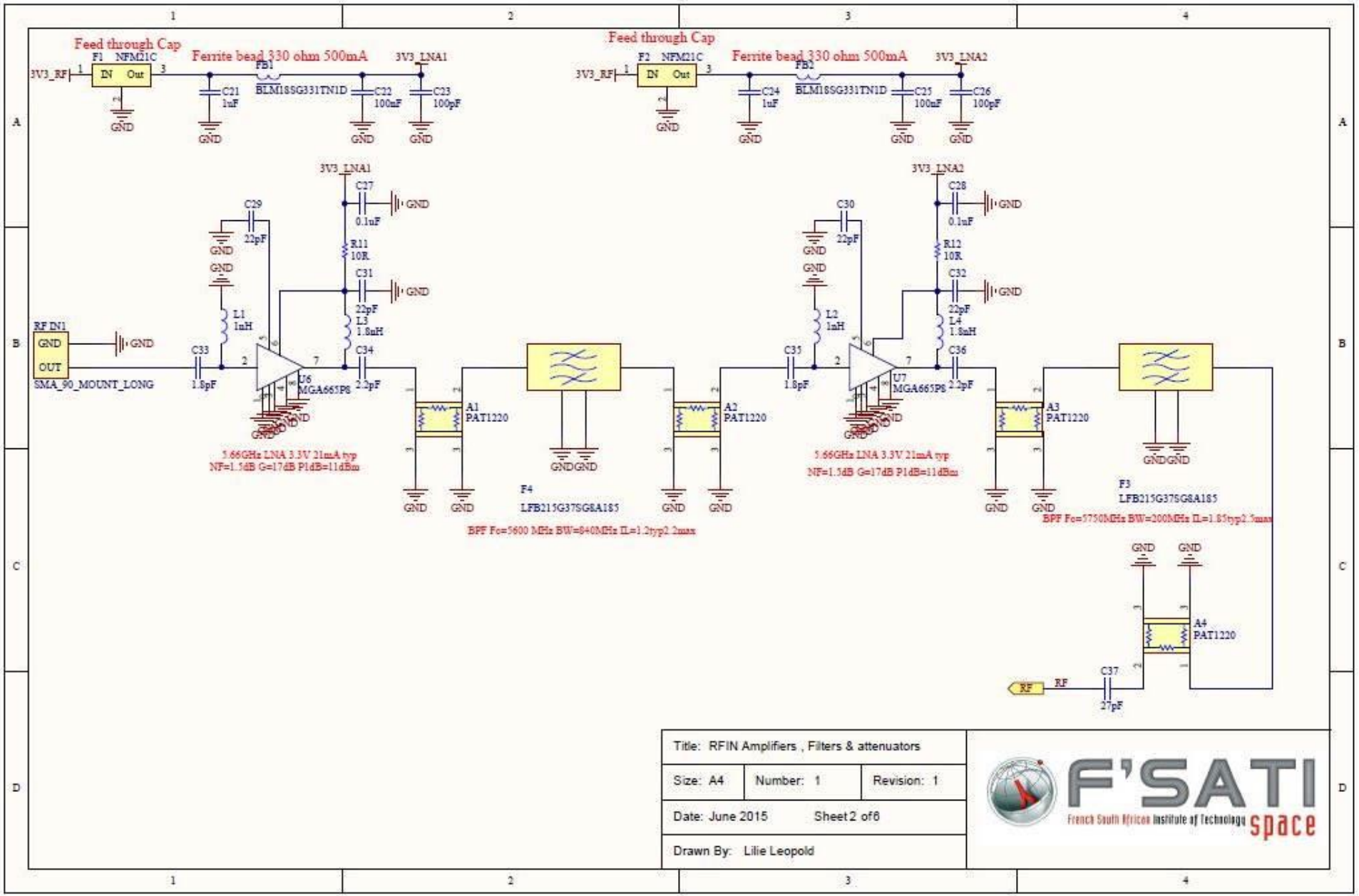
```
/*
  Phase Locked Loop

  This code controls Analog Devices ADF4107 PLL Frequency Synthesizer.

  The ADF4107 consists of
  1 low noise digital PFD(phase frequency detector)
  2 a precision charge pump
  3 a programmable Reference divider
  4 programmable A(6-bit,0-63) and B(13-bit, 3 to 8191)counters
  5 a dual modulus prescaler(P/P+1)==>8/9,16/17,32/33,64/65==>the minimum(p^2-p)
  4&5 above implement an N divider (N=BP+A)
  R(14-bit, 1-16383)counter allows selectable REFin freq's at PFD i/p
  6 MUXOUTand lock detect controlled by M3,M2 and M1 in the Function latch
  Digital lock detect is active high

 The ADF4107 digital section include:
 a)24-bit input shift register
 b)14-bit R counter
 c)19-bit N counter

 The ADF4107 is SPI-compatible,and to command it,
 *Data is clocked in MSB first on each rising edge of the CLK
 *Data is transfered from the shift reg to one of the four latches on the rising edge of LE
 *The destination latch is determined by two control bits (C2,C1)in the shift register. LSBs, DB1 and DB0

 Initialisation Method:
*Apply VDD
*Programm the initialisation latch, set C2 and C1 to 11
*Make sure F1 bit is programmed to 0,Resets R, AB counters
*Function latch load,set C2 and C1 to 10
*Make sure F1 bit is programmed to 0,Resets R, AB counters
*R load,set C2 and C1 to 00
*AB load,set C2 and C1 to 01

ADF4107 Programming Details:
Frequency Range: 4385-4405 MHz
Output Freq:4395MHz
Fref:10 MHz
PFD:1 MHz
Channel spacing: 1MHz
P/P+1:32/33
Ref divider(R counter):10
Main divider(B counter):137
Main divider(A counter):11
Latches/Registers
R counter latch:0x28
N counter latch:0x8929
Function latch:0x9F8082

The circuit:
  * CE - to digital pin 10  (SS pin)==>green pin 10
  * DATA - to digital pin 11 (MOSI pin)==>Red Pin 12
  * CLK - to digital pin 13 (SCK pin)==>orange pin 11
  * (MUXOUT pin)==>Blue pin 14
  * (LE pin)==>yellow pin 13
```

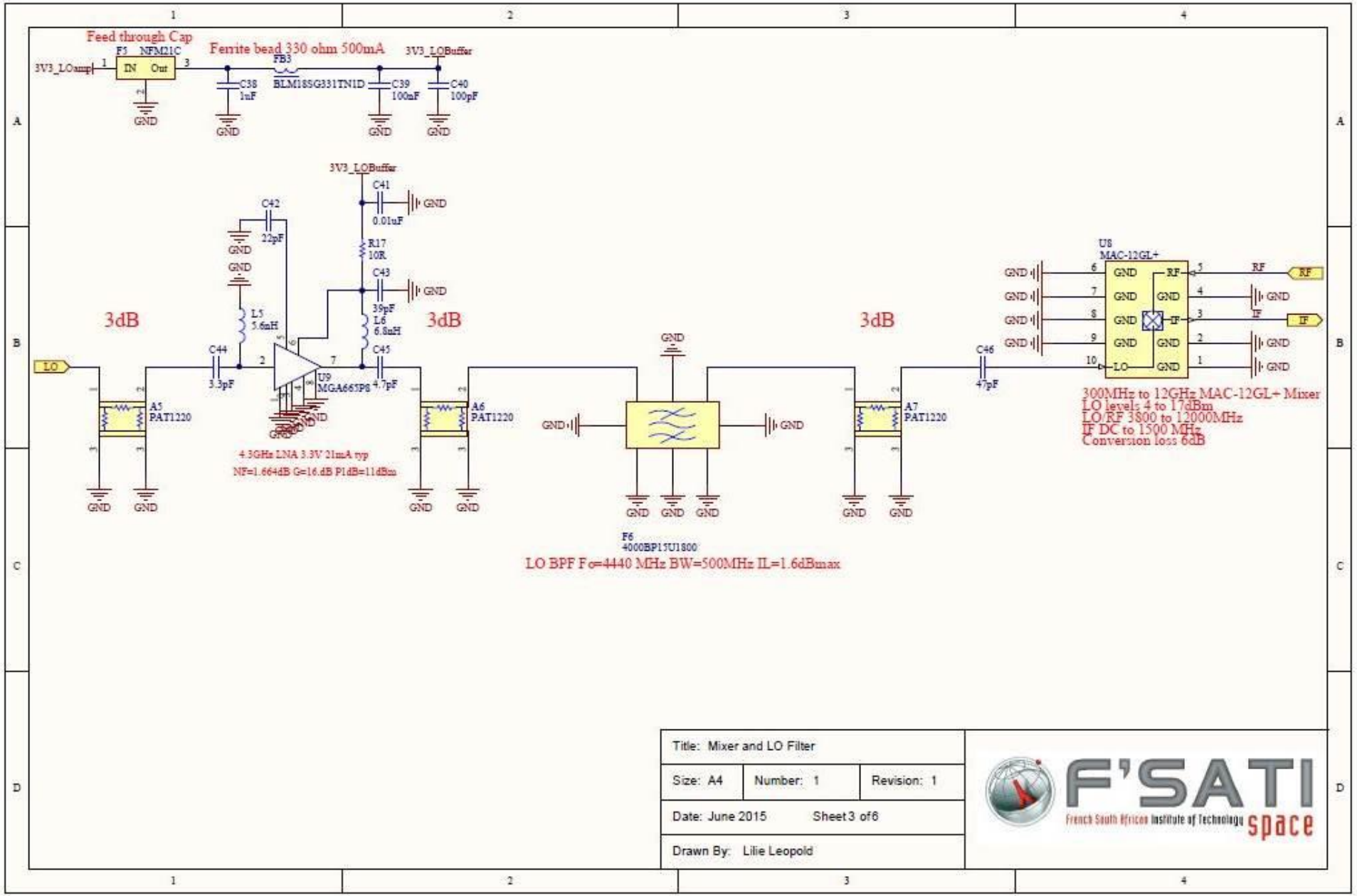
```
created by Lilie Nalitye Leopold
*/

// the Synthesizer communicates using SPI, so include the SPI library:
#include <SPI.h>

// set pin 10 as the slave select for the SYNTHESIZER:
const int slaveSelectPin = 10;//SS,CE,green10
const int DataPin = 11;//MOSI(Red12),serial data in, MSB
const int CLKPin = 13;//SCK, Orange11, clk in serial data into the 24 bit register
const int LEPin = 8;//Load Enable,LatchPin, Yellow13, when LE=1,data in the 24 bit register is loaded
into one of the 4 latches
const int MUXOUTPin = 9;//Lockdetect, Blue14

//SPI.beginTransaction(SPISettings(clockspeed, MSBFIRST, SPI_MODE0))
//SPI.beginTransaction(SPISettings(20000000, MSBFIRST, SPI_MODE0));
//The clock speed should be the maximum speed the SPI slave device can accept=20MHz
SPISettings ADF4107SPIsettings(20000000, MSBFIRST, SPI_MODE0);

const int 24bitsShiftReg = 24;//24bits Shift Register

void setup() {
// put your setup code here, to run once:
//Configuring pins as input and output
pinMode(slaveSelectPin,OUTPUT);// set the slaveSelectPin as an output:
pinMode(DataPin,INPUT);
pinMode(CLKPin,INPUT);
pinMode(MUXOUTPin,OUTPUT);
pinMode(LEPin,OUTPUT);
SPI.begin(); // initialize SPI interface
SPI.setClockDivider(SPI_CLOCK_DIV8); //Slow down the master clock rate by 8//9600
}

void loop() {
  // put your main code here, to run repeatedly:
  //Your void loop() function needs to make a call to digitalSynthWrite() once.
  //Set a flag (boolean variable) that will set it to program only once (if statement)
 /*
  //CLK(rising edge)->send (data) into the 24 bit shift register bit by bit
   CLKPin=0;
  if (CLKPin==1||CLKPin==0){24bitsShiftReg<=DATAinbitbybit}
  */
//CLK, High
//send data DB23(MSB),
//data to clock setup delay(10ns)
//CLK, Low
//send data DB22
//data to clock hold time delay(10ns)
//and so on until DB0(LSB)
   CLKPin=0;
  if (CLKPin==1||CLKPin==0)
  {
     24bitsShiftReg=DATAinbitbybit
     delay(10);
    }

 void digitalSynthWrite() {
    //  send in the address and value via SPI: if (CLKPin==1||CLKPin==0)

SPI.beginTransaction(ADF4107SPIsettings);
// take the SS pin low to select the chip:
  digitalWrite(slaveSelectPin, LOW);
//Programm the initialisation latch, set C2 and C1 to 11
```

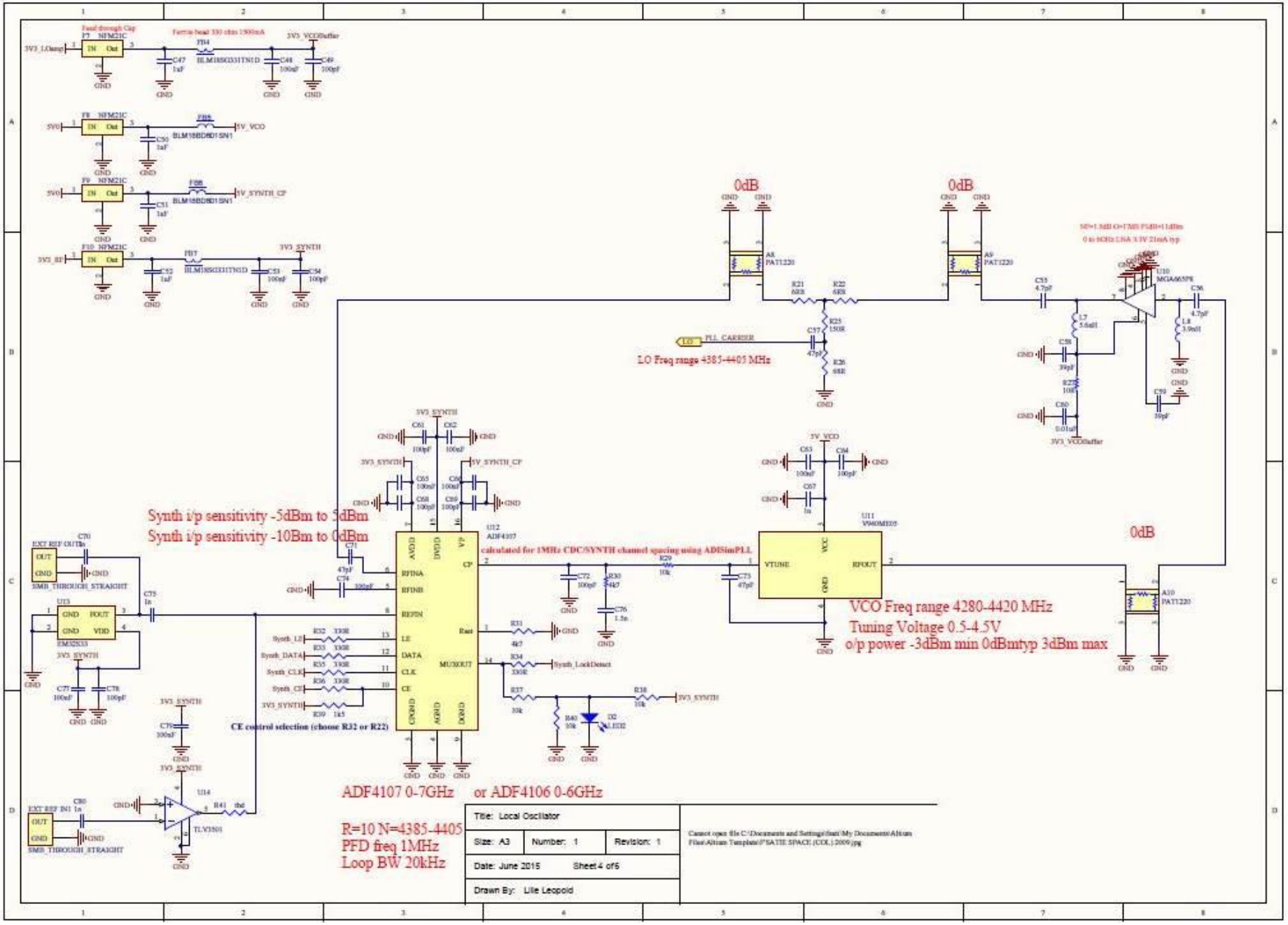
```
  SPI.transfer(0x9F8083); ////Make sure F1 bit is programmed to 0,Resets R, AB counters
//Function latch load,set C2 and C1 to 10
  SPI.transfer(0x9F8082);  //Make sure F1 bit is programmed to 0,Resets R, AB counters
//R load,set C2 and C1 to 00
  SPI.transfer(0x28);
//AB load,set C2 and C1 to 01
  SPI.transfer(0x8929);//N counter latch:
// take the SS pin high to de-select the chip:
  digitalWrite(slaveSelectPin, HIGH);
  SPI.endTransaction()
delay(10);

// handle the LE signal correctly to load the values from the shift register
//into the latch after each spi write
//LE (high=>the stored 24 bits in the shift register are transferred to the appropriate latches
// Data is transferred to one of the 4 latches when LE is high
LEPin=1;
//if (LEPin==1){Oneof4Latches<=24bitsShiftReg}
//J=stored 24 bits values
for (int j = 0; j < 24; j++) {
    //ground latchPin and hold low for as long as you are transmitting
    digitalWrite(LEPin, LOW);
    digitalWrite(CLKPin, LOW);//clock pin is pulsed (taken high, then low) to indicate that the bit is
available
    shiftOut(DataPin, CLKPin, MSBFIRST, j);//shiftOut(dataPin, clockPin, bitOrder, value)
    //return the latch pin high to signal chip that it
    //no longer needs to listen for information
    digitalWrite(LEPin, HIGH);
    delay(10);

  }
```

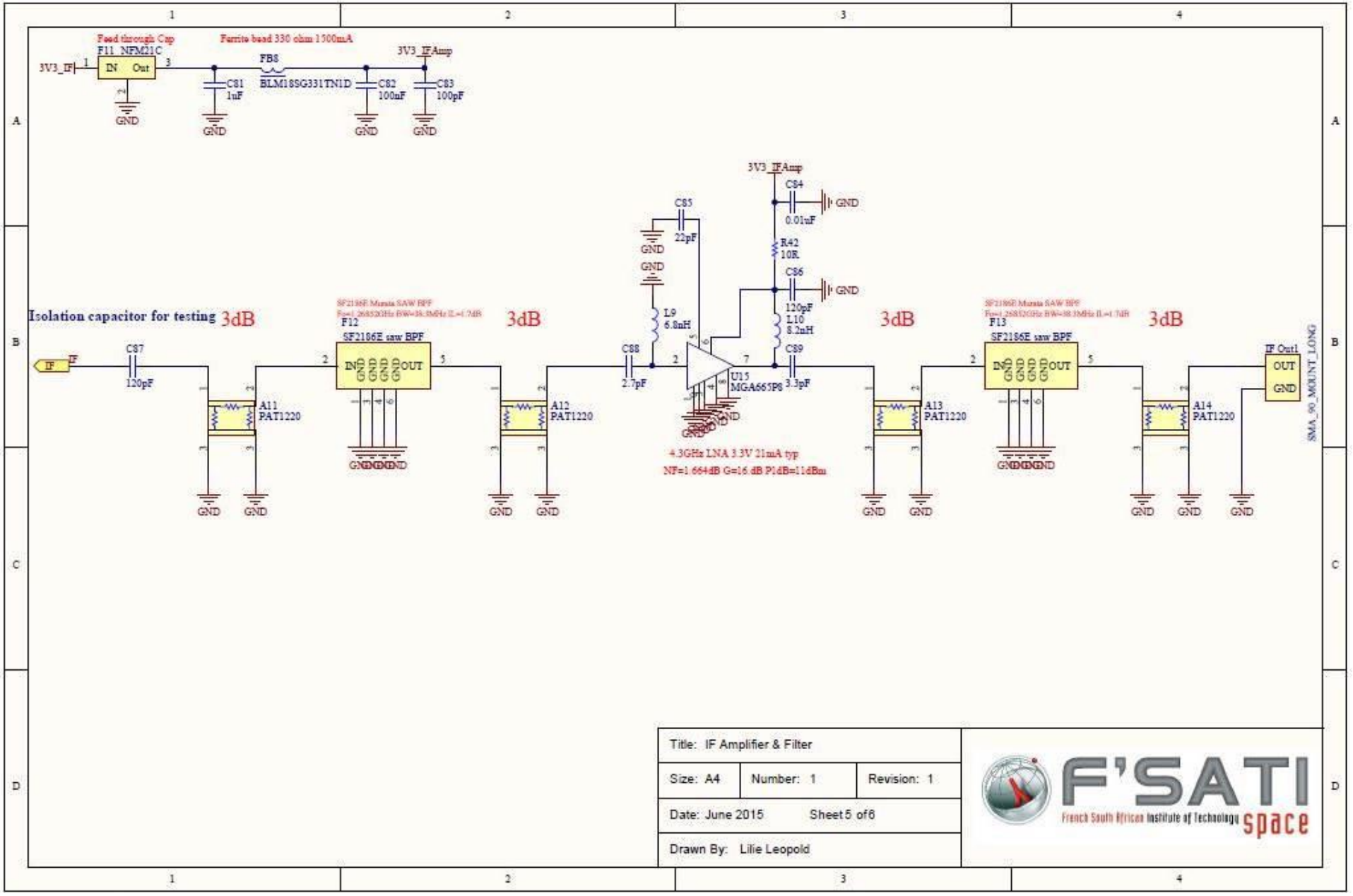
APPENDIX B: Altium Design Schematics, PCB Layout and Bill of Materials (BOM)

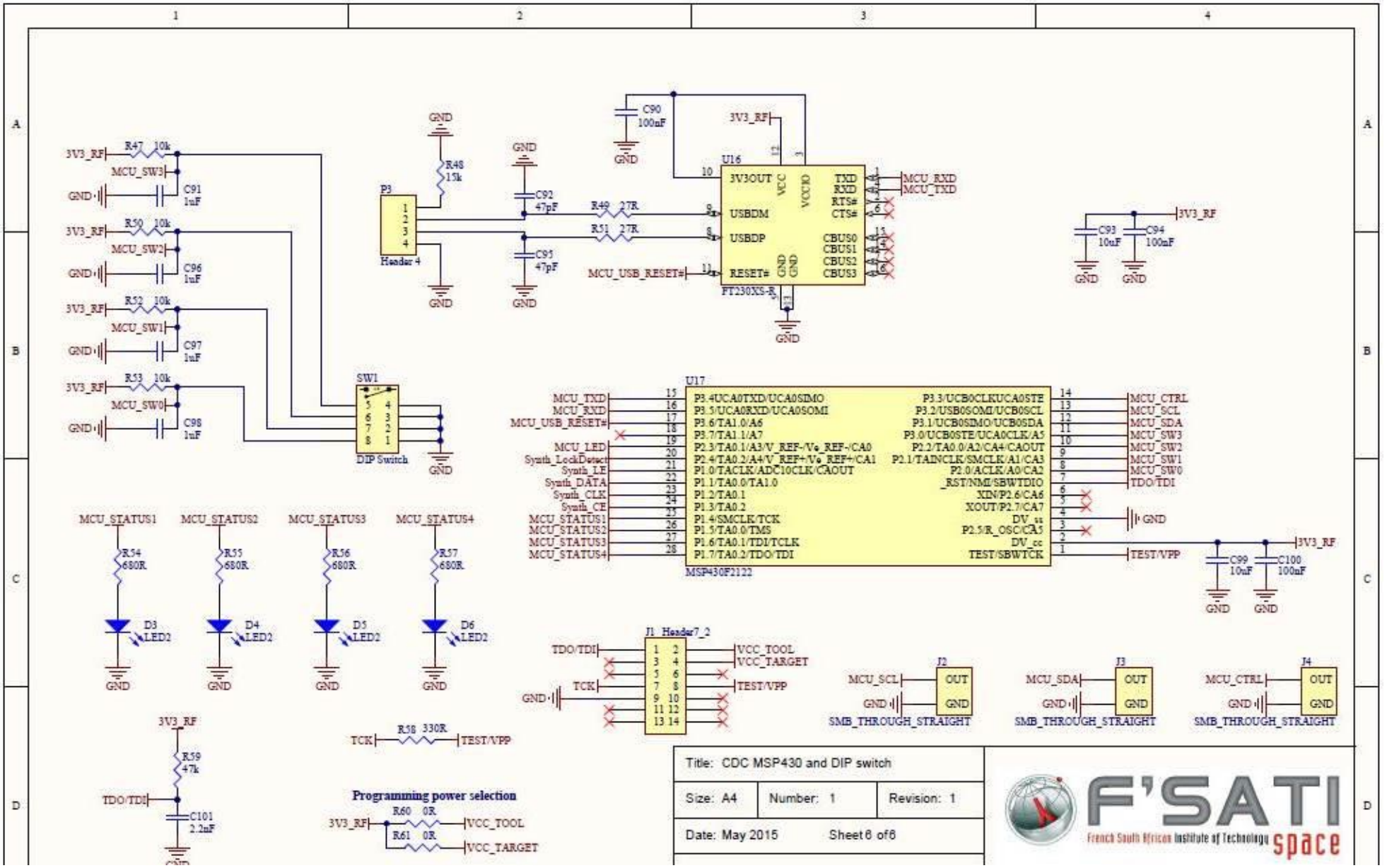


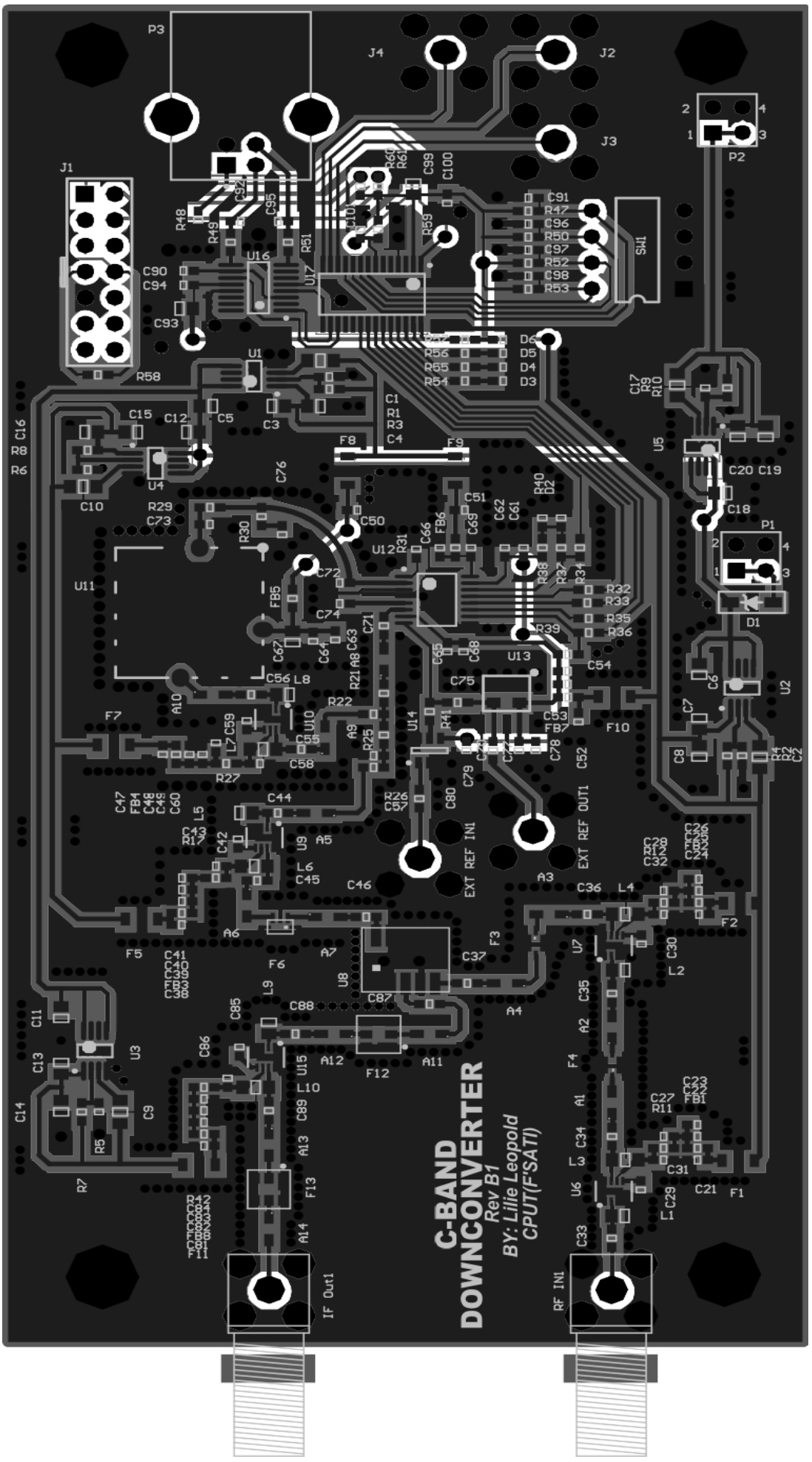

Feed through Cap
F1 NFM21C
3V3_RF
IN Out
Ferrite bead 330 ohm 500mA
FB1
BLM18SG331TN1D
3V3_LNA1
C21 1uF
C22 100nF
C23 100pF
GND
Feed through Cap
F2 NFM21C
3V3_RF
IN Out
Ferrite bead 330 ohm 500mA
FB2
BLM18SG331TN1D
3V3_LNA2
C24 1uF
C25 100nF
C26 100pF
GND
3V3_LNA1
C27 0.1uF
C29 22pF
R11 10R
C31 22pF
L1 1uH
L3 1.8nH
RF IN1
GND
OUT
SMA_90_MOUNT_LONG
C33 1.8pF
C34 2.2pF
U6 MGA665P8
5.66GHz LNA 3.3V 21mA typ
NF=1.5dB G=17dB P1dB=11dBm
A1 PAT1220
F4 LFB215G37SG8A185
BPF Fc=5600 MHz BW=840MHz IL=1.2typ2.2max
A2 PAT1220
3V3_LNA2
C28 0.1uF
C30 22pF
R12 10R
C32 22pF
L2 1uH
L4 1.8nH
C35 1.8pF
C36 2.2pF
U7 MGA665P8
5.66GHz LNA 3.3V 21mA typ
NF=1.5dB G=17dB P1dB=11dBm
A3 PAT1220
F3 LFB215G37SG8A185
BPF Fc=5750MHz BW=200MHz IL=1.85typ2.3max
A4 PAT1220
RF
C37 27pF
Title: RFIN Amplifiers , Filters & attenuators
Size: A4
Number: 1
Revision: 1
Date: June 2015
Sheet 2 of6
Drawn By: Lilie Leopold
F'SATI
French South African Institute of Technology
space

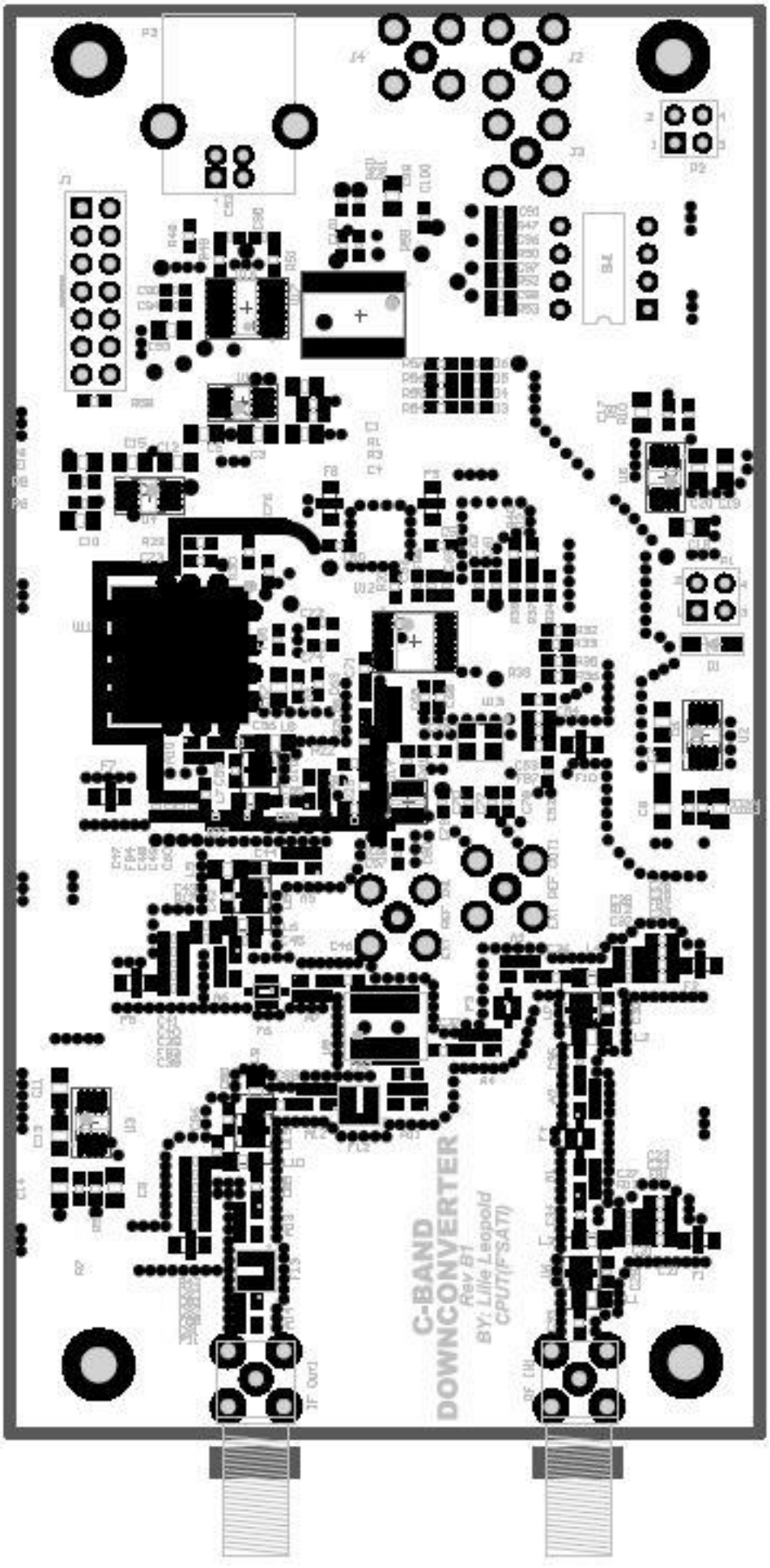

Feed through Cap
F5 NFM21C
Ferrite bead 330 ohm 500mA
3V3_LOamp
IN Out
FB3
BLM18SG331TN1D
3V3_LOBuffer
C38 1uF
C39 100nF
C40 100pF
GND
3V3_LOBuffer
C41 0.01uF
C42 22pF
R17 10R
C43 39pF
L5 5.6nH
L6 6.8nH
3dB
3dB
3dB
LO
C44 3.3pF
C45 4.7pF
U9 MGA665P8
A5 PAT1220
A6 PAT1220
A7 PAT1220
C46 47pF
4.3GHz LNA 3.3V 21mA typ
NF=1.664dB G=16.dB P1dB=11dBm
F6
4000BP15U1800
LO BPF Fo=4440 MHz BW=500MHz IL=1.6dBmax
U8
MAC-12GL+
GND
RF
IF
LO
300MHz to 12GHz MAC-12GL+ Mixer
LO levels 4 to 17dBm
LO/RF 3800 to 12000MHz
IF DC to 1500 MHz
Conversion loss 6dB
Title: Mixer and LO Filter
Size: A4
Number: 1
Revision: 1
Date: June 2015
Sheet 3 of 6
Drawn By: Lilie Leopold
F'SATI
French South African Institute of Technology
space


Feed through Cap
Ferrite bead 330 ohm 1500mA
3V3_VCODuffer
5V_VCO
5V_SYNTH_CP
3V3_SYNTH
0dB
0dB
PLL_CARRIER
LO Freq range 4385-4405 MHz
Synth i/p sensitivity -5dBm to 5dBm
Synth i/p sensitivity -10Bm to 0dBm
calculated for 1MHz CDC/SYNTH channel spacing using ADISimPLL
CE control selection (choose R32 or R22)
VCO Freq range 4280-4420 MHz
Tuning Voltage 0.5-4.5V
o/p power -3dBm min 0dBmtyp 3dBm max
0dB
ADF4107 0-7GHz or ADF4106 0-6GHz
R=10 N=4385-4405
PFD freq 1MHz
Loop BW 20kHz
Title: Local Oscillator
Size: A3
Number: 1
Revision: 1
Date: June 2015
Sheet 4 of 6
Drawn By: Lilie Leopold


Feed through Cap
F11_NFM21C
Ferrite bead 330 ohm 1500mA
3V3_IF
3V3_IFAmp
FB8
BLM18SG331TN1D
C81
1uF
C82
100nF
C83
100pF
GND
Isolation capacitor for testing
3dB
3dB
3dB
3dB
IF
C87
120pF
A11
PAT1220
F12
SF2186E saw BPF
IN
GND
OUT
A12
PAT1220
C88
2.7pF
C85
22pF
L9
6.8nH
C84
0.01uF
R42
10R
C86
120pF
L10
8.2nH
C89
3.3pF
U15
MGA665P8
4.3GHz LNA 3.3V 21mA typ
NF=1.664dB G=16 dB P1dB=11dBm
A13
PAT1220
F13
SF2186E saw BPF
A14
PAT1220
IF_Out1
OUT
GND
SMA_90_MOUNT_LONG
Title: IF Amplifier & Filter
Size: A4
Number: 1
Revision: 1
Date: June 2015
Sheet 5 of 6
Drawn By: Lilie Leopold
F'SATI
French South African Institute of Technology
space


3V3_RF
R47 10k
MCU_SW3
C91 1uF
R50 10k
MCU_SW2
C96 1uF
R52 10k
MCU_SW1
C97 1uF
R53 10k
MCU_SW0
C98 1uF
SW1
DIP Switch
GND
P3
Header 4
R48 15k
C92 47pF
C95 47pF
R49 27R
R51 27R
MCU_USB_RESET#
C90 100nF
U16
3V3OUT
USBDM
USBDP
RESET#
VCC
VCCIO
GND
TXD
RXD
RTS#
CTS#
CBUS0
CBUS1
CBUS2
CBUS3
FT230XS-R
MCU_RXD
MCU_TXD
C93 10uF
C94 100nF
U17
MCU_TXD
MCU_RXD
MCU_USB_RESET#
MCU_LED
Synth_LockDetect
Synth_LE
Synth_DATA
Synth_CLK
Synth_CE
MCU_STATUS1
MCU_STATUS2
MCU_STATUS3
MCU_STATUS4
P3.4/UCA0TXD/UCA0SIMO
P3.5/UCA0RXD/UCA0SOMI
P3.6/TA1.0/A6
P3.7/TA1.1/A7
P2.3/TA0.1/A3/V_REF-/Ve_REF-/CA0
P2.4/TA0.2/A4/V_REF+/Ve_REF+/CA1
P1.0/TACLK/ADC10CLK/CAOUT
P1.1/TA0.0/TA1.0
P1.2/TA0.1
P1.3/TA0.2
P1.4/SMCLK/TCK
P1.5/TA0.0/TMS
P1.6/TA0.1/TDI/TCLK
P1.7/TA0.2/TDO/TDI
P3.3/UCB0CLKUCA0STE
P3.2/USB0SOMI/UCB0SCL
P3.1/UCB0SIMO/UCB0SDA
P3.0/UCB0STE/UCA0CLK/A5
P2.2/TA0.0/A2/CA4/CAOUT
P2.1/TAINCLK/SMCLK/A1/CA3
P2.0/ACLK/A0/CA2
_RST/NMI/SBWTDIO
XIN/P2.6/CA6
XOUT/P2.7/CA7
DV_ss
P2.5/R_OSC/CA5
DV_cc
TEST/SBWTCK
MCU_CTRL
MCU_SCL
MCU_SDA
MCU_SW3
MCU_SW2
MCU_SW1
MCU_SW0
TDO/TDI
TEST/VPP
MSP430F2122
C99 10uF
C100 100nF
MCU_STATUS1
MCU_STATUS2
MCU_STATUS3
MCU_STATUS4
R54 680R
R55 680R
R56 680R
R57 680R
D3 LED2
D4 LED2
D5 LED2
D6 LED2
J1_Header7_2
TDO/TDI
TCK
GND
VCC_TOOL
VCC_TARGET
TEST/VPP
J2
J3
J4
MCU_SCL
MCU_SDA
MCU_CTRL
OUT
GND
SMB_THROUGH_STRAIGHT
3V3_RF
R59 47k
TDO/TDI
C101 2.2nF
TCK
R58 330R
TEST/VPP
Programming power selection
R60 0R
R61 0R
VCC_TOOL
VCC_TARGET
Title: CDC MSP430 and DIP switch
Size: A4
Number: 1
Revision: 1
Date: May 2015
Sheet 6 of 6
F'SATI
French South African Institute of Technology
space


C-BAND
DOWNCONVERTER
Rev B1
BY: Lilie Leopold
CPUT(FSATI)
IF Out1
RF IN1
EXT REF IN1
EXT REF OUT1
P1
P2
P3
J1
J2
J3
J4
SW1
D1
D2
D3
D4
D5
D6


C-BAND
DOWNCONVERTER
Rev B1
BY: Lilie Leopold
CPUT(FSATI)

Footprint	Comment	Designator	Description	Quantity
PAT1220	PAT1220	A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14	3dB pad	14
RF0805	0.01uF	C1, C2, C9, C10, C17		5
RF0805	10uF	C3, C5, C6, C7, C11, C12, C13, C15, C18, C19, C93, C99		12
RF0805	22uF	C4, C8, C14, C16, C20		5
RF0603	1uF	C21, C24, C38, C47, C50, C51, C52, C81, C91, C96, C97, C98	Capacitor, Capacitor, Capacitor	12
RF0603	100nF	C22, C25, C39, C48, C53, C62, C63, C65, C66, C77, C79, C82, C90, C94, C100	Capacitor, Capacitor, Capacitor	15
RF0603	100pF	C23, C26, C40, C49, C54, C61, C64, C68, C69, C72, C74, C78, C83	Capacitor	13
RF0603	CAP	C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C41, C42, C43, C44, C45, C55, C56, C58, C59, C60, C84, C85, C86, C88, C89		25
RF0603	27pF	C37	Isolation capacitor for testing	1
RF0603	47pF	C46, C57, C71, C73, C92, C95	Capacitor, Capacitor	6
RF0805	1u	C67	Capacitor - Surface Mount Pins 1 and 2: Gen	1
RF0603	1n	C70, C75, C80	Capacitor	3
RF0603	1.5n	C76		1
RF0603	120pF	C87	Isolation capacitor for testing	1
RF0603	2.2nF	C101		1
1N5819	1N5819HW	D1		1
RF0603	LED2	D2, D3, D4, D5, D6	Typical RED, GREEN, YELLOW, AMBER Ga	5
SMB	SMB_THROUGH_STRAIGHT	EXT REF IN1, EXT REF OUT1, J2, J3, J4		5
NFM21C	NFM21C	F1, F2, F5, F7, F8, F9, F10, F11	EMI Filter	8
LFB21_SG8	LFB215G37SG8A185	F3, F4	LFB21_SG8 Chip Multilayer LC BPF	2
4000BP15U1800	4000BP15U1800	F6	4000BP15U1800 BPF	1
SF2186E Murata BPF	SF2186E saw BPF	F12, F13	1268.52MHz Saw Filter, SF2186E saw BPF	2
RF0603	BLM18SG331TN1D	FB1, FB2, FB3, FB4, FB7, FB8	EMI Filter Bead	6
RF0603	BLM18BD601SN1	FB5, FB6	EMI Filter Bead	2
SMA 90 deg - Extended	SMA_90_MOUNT_LONG	IF Out1, RF IN1	SMA connector	2
Header 7x2 - 2.54MM	Header7_2	J1		1
RF0805	1nH	L1, L2, L5, L8, L9	Inductor	5
RF0805	6.8nH	L3, L4, L6, L7, L10	Inductor	5
HDR2X2	Header 2X2	P1, P2	Header, 2-Pin, Dual row	2
USB2.5-2H4D	Header 4	P3	Header, 4-Pin	1
RF0603	180k	R1	Resistor	1
RF0603	NP	R2, R5, R6, R9	Resistor	4
RF0603	560k	R3	Resistor	1
RF0603	0k	R4, R7, R8, R10	Resistor	4
RF0603	10R	R11, R12, R17, R27, R42	Resistor	5
RF0603	6R8	R21, R22	Resistor	2
RF0603	150R	R25	Resistor	1
RF0603	68R	R26	Resistor	1
RF0603	10k	R29, R37, R38, R40, R47, R50, R52, R53	Resistor	8
RF0603	4k7	R30, R31	Resistor	2
RF0603	330R	R32, R33, R34, R35, R36, R58	Resistor	6
RF0603	1k5	R39	Resistor	1
RF0603	tbd	R41	Resistor	1
RF0603	15k	R48	Resistor	1
RF0603	27R	R49, R51	Resistor	2
RF0603	680R	R54, R55, R56, R57	Resistor	4
RF0603	47k	R59	Resistor	1
RF0603	0R	R60, R61	Resistor	2
DIP8 - 4 DIP SW	DIP Switch	SW1		1
LT1762	LT1762-ADJ	U1	LDO 5V	1
LT1762	LT1762-3.3	U2, U3, U4, U5	LDO 3.3V	4
MGA665P8	MGA665P8	U6, U7, U9, U10, U15	Amplifier	5
MAC12G+	MAC-12GL+	U8	Mixer	1
MINI-14S	V940ME05	U11	VCO	1
TSSOP-16	ADF4107	U12	PLL Synthesizer	1
3.2x2.5 4-SMD	EM32S33	U13	Euroquartz TCXO	1
SOT23-6	TLV3501	U14	4.5ns Rail-to-Rail, High-Speed Comparator	1
SSOP-16_N	FT230XS-R	U16	USB to Basic UART Interface Chip, UHCI/OH	1
TSSOP-28 pins	MSP430F2122	U17	TI MSP430 MCU	1
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APPENDIX C: Trax PCB Manufacturing Instructions

********** NOTES **********

AUTHOR: Lilie Leopold

COMPANY: F'SATI, CPUT, BELLVILLE CAMPUS PROJECT: CDC Rev B1

FILENAME: PCB Manufacturing Instructions File

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1) Attached are the photoplots in a zip file.
2) Prior to baking ensure that an Additional 2nd Stage 3200mJcm-2 UV Exposure is done. This translates to an additional cure of about 5min. This is to ensure that the Silkscreen or Solder Mask does not outgass.
3) The PCB is a 4 layer board with CONTROLLED IMPEDANCE ON THE TOP LAYER RELATIVE TO PLANE LaYER 1.

PCB Specs / Layer Details:

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a) Dimensions: 68.453mm x 130.175mm
b) Number of Layers: 4 layers
c) Minimum Track Width: 10 mil
d) Minimum Finished Hole Size: 12 mil
e) Minimum Clearance: 5 mil all layers
f) Material Type: Rogers 4003C
g) Board Thickness: ~1.5 to 1.6 mm
h) Number of pad/via holes 827
i) Copper Thickess and layer sequence: * Top Layer (RF) - 35um Thick
* Power Plane 1 (GND) - 70um
* Routing 3V3 (PWR) - 35um
* Bottom Layer (GEN)- 35um
j) Final Finish: Auto Catalytic Silver Imersion Gold (ASIG)
k) No of Gold Tabs: None
l) Component Side Legend: White
m) Solder Side Legend: White
n) Solder mask: Top and Bottom
o) Solder Mask Color: Green
p) Number of Boards 2

---------- Controlled Impedance Layer Information ----------

q) Layer separation distance:

---------- Top Layer ----------

0.3mm (MUST BE EXACT for CONTROLLED IMPEDANCE): 1080 + 1080 + 7628 + 1080

---------- Power Plane 1 (GND Plane) ----------

0.75 mm: NY2150 0.71 mm 35/35

---------- Routing (General routing layer----------

0.3mm: 1080 + 1080 + 7628 + 1080

-------- Bottom Layer (General routing layer)--------

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r) IMPORTANT NOTE PLANE LAYERS

There should be a Gap of about 10mil or greater running along the border edges.

PHOTOPLOT NOTES:
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i) Attached is the photoplot files for the above project.

ii) There are two power planes of which both are split planes. See below for more details.

iii) Also note that the electrical layer sequence are as follows:
Top Layer, Power Plane Layer 1, Routing Layer 1,
Bottom Layer.

iv) Ensure that the split planes does not short out @ the PC Board border edges. The voids should run right up to the border edge.

v) Ensure that you 'Tent' all silkscreen that overlaps the SMT pads.

vi) There are no Gold Fingers on this PCB

GENERAL INFO
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a) The photoplots below were generated by Altium Designer DXP.

b) The board is a 4 layer board

c) Ensure that the Inner Planes do not go to the edge of the PCB. There should be at least a 0.5mm clearance or more from the Board Edges.

d) Ensure that the clearance of 5mil (Track to Track; Pad to Track; and Pad to Pad) is adhered too. If you find clearances less than that specified, please contact me ASAP. I ran the Altium DRC Check without any problems.

e) The Gerber Format specified in Altium was 2:4

f) Ensure that the PCB is bare-board (Flying Probe) tested properly.

FILE INFO AND ADDITIONAL INFORMATION
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1) Enclosed is a zip file of all the photoplot and text files.
2) The supplied files are as follows:
LilieCDC8PCB.APR - Aperture Listing
LilieCDC8PCB.DRL - NCD EIA format Drill file
LilieCDC8PCB.DRR - Text Report on NCD Drill file Outputs
LilieCDC8PCB.GBL - Gerber Photoplot Bottom Layer
LilieCDC8PCB.GBO - Gerber Photoplot Bottom Silkscreen
LilieCDC8PCB.GBP - Gerber Photoplot Bottom Paste
LilieCDC8PCB.GBS - Gerber Photplot Bottom Solder Mask
LilieCDC8PCB.GD1 - Gerber Photoplot Drill Drawing
LilieCDC8PCB.GG1 - Gerber Photoplot Drill Guide
LilieCDC8PCB.GM13 - Gerber Photoplot Mechanical Layer 13 - This layer is the Board Outline
LilieCDC8PCB.GM15 - Gerber Photoplot Mechanical Layer 15
LilieCDC8PCB.GP1 - Gerber Photoplot Power Plane 1 - This is the ground layer
LilieCDC8PCB.GP2 - Gerber Photoplot Power Plane 2
LilieCDC8PCB.GTL - Gerber Phototplot Top Layer
LilieCDC8PCB.GTO - Gerber Photoplot Top Silkscreen
LilieCDC8PCB.GTP - Gerber Photoplot Top Paste
LilieCDC8PCB.GTS - Gerber Photoplot Top Solder Mask
LilieCDC8PCB.TXT - NCD Drill file Text Output
LilieCDC8PCB.REP - Statistics

3) There are two solder masks: viz Top and Bottom because of SMT
components on the top and bottom layers.
4) Solder Mask Swell size is 4mil (ie: 2mil on each side) on average. However,
it varies from component to component where the mask swell size should be
keep virtually zero keep virtually zero [On BGAs]. Adjust Solder Mask to zero on BGAs if the current
solder mask is abnormally higher than required.
5) There are no solder mask on gold edge connectors (ie: the fingers).

If any discrepancies exist or if there is a problem with the files, please
contact me at number listed at the top of this document

Thanks
Lilie Leopold

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