Design and Development of a Generic Switch-Mode Power Supply Hold-Up Module for Pulsed Power Amplifiers

By

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DECLARATION

I, Nhlanhla Mashabane, declare that the contents of this thesis represent my own unaided work, and that the thesis has not previously been submitted for academic examination towards any qualification. Furthermore, it represents my own opinions and not necessarily those of the Cape Peninsula University of Technology.

Signed

10/03/2025

Date

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Abstract

This study describes the design and development of a Switch-Mode Power Supply (SMPS) based power hold-up module for Radio Frequency (RF) power amplifiers. High power solid-state power amplifiers require high power at low voltages, which means that they must be supplied with high peak currents. This can be achieved by utilizing an energy storage capacitor bank placed closely to the RF power amplifier. The energy storage bank would then supply the high peak currents, while keeping the source power supply current low, and thus reducing the capacity (and size) requirements for the source power supply.

The power supply is designed to maintain a tightly regulated supply voltage at the onset of each transmit pulse. During the transmit pulse, the regulator function is disabled and load power is provided in total from the energy stored in electrolytic capacitors. The module must be able to generate these outputs from the ma

in power-conditioning unit, with the minimum and maximum pulse lengths, as well as, at the required Pulse Repetition Frequency (PRF).

The use of a SMPS is introduced to the charging circuitry for its efficiency, size and weight benefits. The design is such that the switching intervals of the SMPS are configured to accommodate the transmitting windows to ensure that a following pulse is available when the next transmit command is set.

Simulations, calculations and test results are presented and the test results are compared with the theoretical simulated design results to conclude the hypothesis. The results demonstrated that the SMPS implementation yielded great benefit to the efficiency, sensitivity and physical size of the power hold-up module.

Keywords: *Pulsed Power Supply, Radio Frequency, Power Management, RF Power Amplifier, Solid-State Circuits, Radar, DC-DC Switch-Mode Power Supply, Buck Converter, Boost Converter*

Contents

List OF Figures

Chapter 1

Chapter 2

Chapter 3

Chapter 4

List of tables

GLOSSARY

Al-Cap	- Aluminum Capacitors
BIM	- Built-in Monitoring
CPUT	- Cape Peninsula University of Technology
DC	- Direct Current
EDLC	- Electric double layer capacitor
ESL	- Equivalent series inductance
ESR	- Equivalent series resistance
HPA	- High Power Amplifier
IC	Integrated Circuit
HUM	- Hold-up Module
LDO	- Low Dropout
LPF	- Low Pass Filter
MOSFET	- Metal Oxide Silicon Field Effect Transistor
PA	- Power Amplifier
PFC	- Power Factor Corrector
PPS	- Pulsed Power Supply
PRF	- Pulse Repetition Frequency
PRT	- Pulse repetition Time
RF	- Radio Frequency
RRS	- Reutech Radar Systems
SC	- Super Capacitor
SMPS	- Switch-mode power Supply
SSPA	- Solid State power amplifier

Chapter 1

Introduction

Reutech Radar Systems developed a power supply (Also known as the Hold-up Module, HUM) to provide DC power to pulsed microwave power amplifiers in the kilowatt range for one of their radar systems. The power supply works and is stable. The challenge with this hold-up module is that it generates a lot of heat in the analogue controller used in line with the load calling for a substantial heat sink and forced air circulation. Second challenge is the high sensitivity of the dissipation to the input voltage, thus a 1% change in the input voltage results in a 5W increase in dissipation while the 1% drop in the input drop may degrade performance.

This then creates the need to design, manufacture and test a new power supply for the microwave power amplifiers. This new power supply should be configured in a topology with high efficiency and stability, generating less heat compared to the current one and also provide increased tolerance on the input voltage fluctuation.

1.1. Statement of Research Problem

In pulsed power amplifiers, Analogue controllers are most commonly used to provide a stable regulated output. However, they generate significant amount of heat and often require a substantially sized heat sink, as well as, forced air circulation. This results in a large and inefficient transmitter system.

Due to the nature and operation of the pulsed power amplifier and its needs, this study proposes the use of a hold-up module (HUM) at power amplifiers front end, and offers great advantages over the traditional low dropout regulators integrated with analogue controllers. The introduction of a HUM provides stability from pulse to pulse while ensuring that voltage droop during the transmit pulse is within specification. It will further convert the pulsed current to a current with small ripple content. This is very crucial in a pulsed radar system, as it defines the stability of the transmitter.

The above mentioned challenge calls for the development of an improved HUM, based on a SMPS topology that will ease the input voltage stress, the heat dissipation in the analogue controller and the ration between the input and output variation.

1.2. Background to the Research Problem

Pulsed radars determine the range of a target by transmitting a pulse and measuring the time delay to the corresponding received pulse. By the same mechanism, it can compare the received signal phase shift, from pulse to pulse, in order to determine the velocity of the target. A pulsed radar needs to transmit high peak power to achieve sufficient average power. The power supply of a high power pulsed solid-state radar transmitter requires special design considerations. They supply large amount of current at relatively low voltages.

A modern technique to resolve this challenge, is to supply the high peak currents via a capacitor bank which is in close proximity with the RF power amplifier itself. The current supplying capacitor bank must be charged by the power supply to the nominal voltage, this charging must take place before the next pulse occurs. The time taken to recharge the capacitors is defined as the function of the Pulse Repetition Time (PRT). A further design complication is that the PRT and the duty cycle can be varied at any given time which is another design consideration to be catered for.

The power supply then acts as a precision charging mechanism. The power supply is an integral part of the transmitter design, and must be designed in such a way that it caters the RF amplifier requirements and stability, as the stability of the power supply is a contributing factor to the performance of the radar as a whole. This is due to the fact that the pulses generated and transmitted by the power amplifier are dependent on the charge of the capacitor bank, the capacitor bank is charged by the power supply. So if the power supply is not stable, precise and consistently charging the capacitor bank, the voltage droop and the charge of the capacitor bank will be different with every pulse and the generated pulses transmitted will not be identical and as a result the radar will see false targets.

The need for this study is based on the following challenges that the current technology has; the current Solid State Power Amplifier (SSPA) power supplies are functional, but inefficient and bulky. The heat and power dissipation in the analogue controller is high, and the input tolerance is very tight since the dissipation is highly sensitive to variation of the input voltage. There is therefore a significant need for study to develop alternative solutions and to optimise the HUM.

1.3. Aim and Objectives

The aim is for the Switch mode power supply based Hold-up module development, for the developed HUM to be more efficient and meet other specified subsystem requirements. The primary objective is to successfully develop and test an efficient and reliable SMPS based HUM. The proposed configuration, design, construction and testing of the systems is shown in the later chapters. The designed PCB must be designed to meet all other subsystem requirements. The core research questions are:

1. How effective is using a Switch-mode based power supply in pulsed RF power Amplifiers?
2. How efficient is using a Switch-mode based power supply in pulsed RF power Amplifiers?
3. Is the proposed configuration an optimal solution (the use of SMPS based HUM)?
4. What technology can be used to nullify the switching noise of the SMPS circuitry?
5. What are the overall benefits of SMPS over Linear controllers or analogue controllers?

1.4. Approach to the Problem

The research would follow the generic engineering research and development process. Start off by looking at pulsed radar power amplifier, pulsed radar power amplifier power suppliers, power amplifier control logic and power and heat analysis with a focus on the power supply of the power amplifier. The power supply application in radar application and other power supply options thus looking at linear regulators with LDOs against SMPS. Looking at applicable topologies both advantages and disadvantages. The best feasible topology will then be selected and further research will be conducted with a focus on it.

1.5. Delineation of Research

The scope of this research will be limited to the study of a power supply for a pulsed power amplifier and development of a switch mode based power supply. Therefore, the literature review will look at:

- Pulsed power amplifiers
- Linear regulators
- Switching regulators

1.6. Thesis Structure

The layout of the remaining part of this thesis is as follows:

Chapter 2:
Pulsed radar power supply subsystem is looked at as the main focus of the study, and how it is integrated with the power amplifier. The power supply design for these power amplifiers is the primary focus of this chapter. It compares linear vs. SMPS's, its topologies, operation, Stability, power supply effects on microwave power amplifiers as well as the benefits and short comings of each converter discussed. The chapter is concluded with a brief of the primary focus areas which have emerged from the literature research.

Chapter 3:
This chapter's is focus is on the SMPS topology that is selected from the study. The evaluation of the controller is discussed in this chapter, looking at how it the controller is configured to meet the desired specifications as well as the design specification and concept of operation.

Chapter 4:
In this chapter, the power hold-up module concept of operation integrated with the design of the HUM is discussed. This is with an aid of the simulation done to prove the concept of the SMPS based power hold up module. Results and measurements are discussed in the chapter as well.

Chapter 5:
The PCB design procedure is documented here. This Chapter discusses the PCB schematic design, along with detailed component placement. It will also outline the PCB layout procedure, as well as, the assembly of the PCB. The evaluation of the hardware is discussed in detail with results.

Chapter 6
This chapter details the conclusions and recommendations for future work on this study. It also provides a summary of the findings.

Chapter 2

Literature Review

2. Hold-up Module Background

The HUM ensures that the pulsed load from the power amplifier is converted to a virtually constant current requirement from the power conditioner module. The regulation is achieved by ensuring that the storage capacitors are charged with precision, to the same voltage for every pulse. The HUM also ensures that the voltage droop during the transmit pulse meets the prescribed requirements. The design of the HUM carters for the control of the charging along with the switching times between the pulses.

The voltage droop is a significant parameter as it directly impacts the pulse to pulse stability of the transmitter, thus every pulse transmitted should be identical for precise return measurements of the radar. Pulse to pulse instability would be defined as radar false target classification. The hold-up module ensures that the voltage droop is precisely maintained.

2.1. First generation hold-up module

The first-generation HUM was developed to provide power to an L-band power amplifier for a dual band experimental radar and a single band production radar. The main functions of the HUM are to:

1) Provide a DC voltage to the power amplifier that will remain stable from pulse to pulse. Stable meaning it is meant that the DC supply voltage waveform will be exactly replicated from pulse to pulse.

2) To ensure that the voltage droop during the transmit pulse meets a prescribed requirement.

3) To convert the pulsed current load, typically 50 A peak rectangular pulses with a duty cycle of 10 to 20%, to a constant current with a small ripple content at the input terminal of the HUM. Figure 2.1 shows a block diagram of the HUM I.

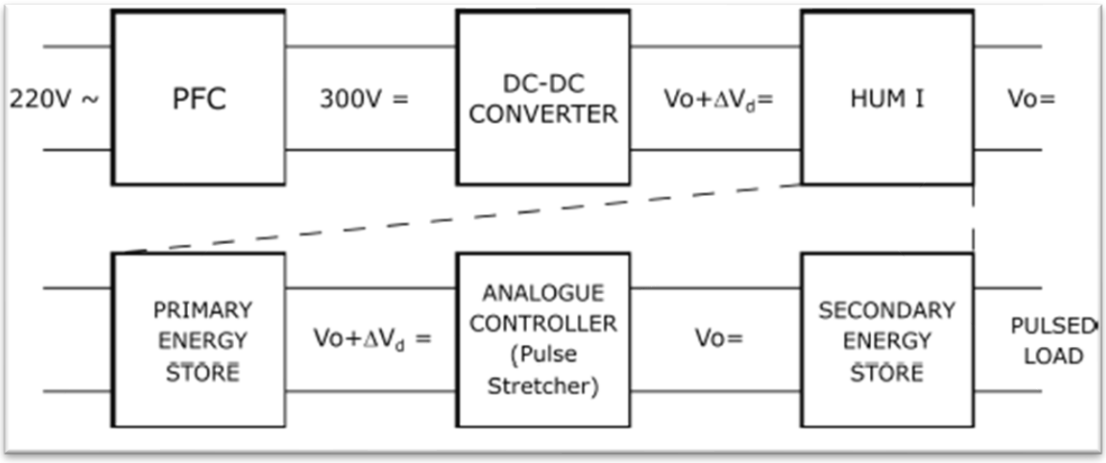

Figure 2.1: HUM I

The supply system consists of an off the shelf Power Factor Corrector (PFC) that converts 220 VAC mains to 300 VDC. The PFC feeds a standard DC-DC converter that provides power to the HUM. The HUM consists of two energy stores and an analogue controller, a series connected P channel MOSFET, that regulates the output voltage at a level of about 1.5 - 2 V below the DC supply voltage.

The HUM must be capable of generating the required output while meeting other defined requirements such as the duty cycle, pulse length and PRF, it also caters for the entire SSPA control and BIM interfaces.

The energy storage capacitors at the output stage of the HUM is given by:

$$i = C\frac{dv}{dt} \qquad 2.1$$

$$C = i\frac{dt}{dV} \qquad 2.2$$

Where:

The $i\ dt$ section is the peak current of the pulse duration

dV Is the amount of voltage droop allowed during the pulse.

The PFC converts the mains supply (220VAC) to dc 300V which is fed into the dc-dc converter and to the HUM I. the analogue controller is switched off in the pulse transmission time, the load SSPA current is then supplied by the secondary energy storage capacitors. The output total capacitance is calculated to be large enough to ensure that an acceptably small voltage drop during the transmit time and is given by:

$$\Delta V_o = \frac{I_{peak}}{C_{ss}}\ T_{pw} \qquad 2.3$$

Solid-state Amplifier Architecture

Solid state power amplifier is an amplifier that makes use of solid-state devices mostly power MOSFETs. Pulsed amplifiers operate in the principle of amplification of RF pulses generated by an electrical device without altering its waveform. Figure 2.2 below shows a typical block diagram of a solid-state transmitter.

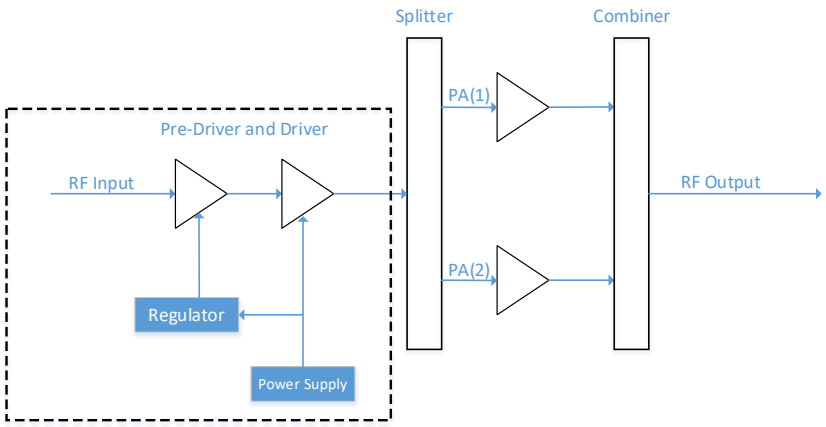

Figure 2.2: Solid-state Transmitter Configuration

SSPA has great benefits including reliability over tube amplifiers but due to the intrinsic properties of these types of technologies, it is a challenge to achieve good performance.

To maximise the input return loss, the input of the SSPA begins with a low power isolator, the rest of the SSPA is then the Pre-Driver stage, Driver stage and the output stage.

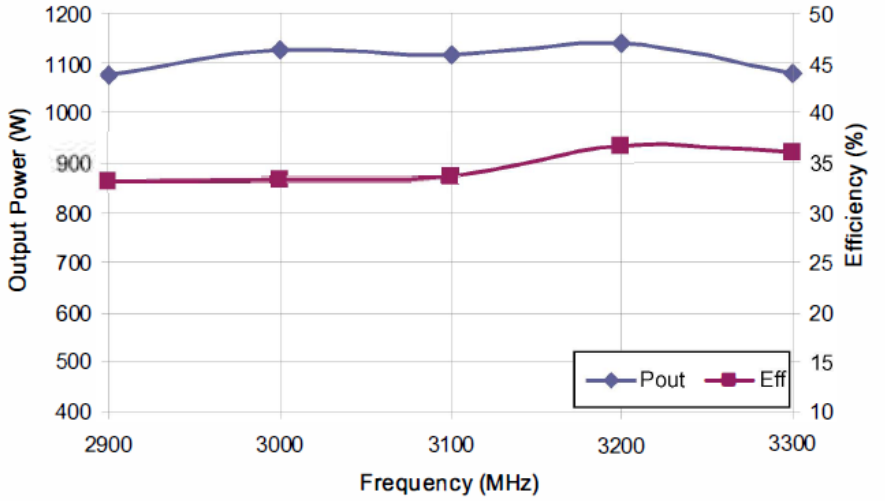

Figure 2.3: Typical performance of a 1Kw SSPA [1]

A critical component in the application of this SSPA is the power supply. The value of the voltage at the moment of pulse is critical for both the phase stability and the amplitude of the transmitter, thus maintaining the ripple. The system used to power this transmitter must be capable of recharging the storage capacitors with the same voltage for each pulse, this is precision in the millivolts range. This is due to ending up with false results resulting from different energy levels in the generation of the pulse and comparing received pulses that were different from transmission. This means that you are transmitting pulse of different energy levels and receiving pulses that are already seeing a target even if there is no potential target.

2.2. SSPA power Supply

A Pulsed Power Supplies (PPS) is a device that produces high power in the microseconds or nanoseconds period. The output of the PPS is of high accuracy, so that the ripple is very small. Given the nature and setup of such power supplies, it is necessary to add energy storage unit to compensate the pulsating power [2]. Because the output of the PPS is pulsed, it is then considered a special power supply and can then be categorized to high frequency PPS, Low frequency PPS, High Voltage PPs and Low Voltage PPS.

And the above mentioned category is according to the PRF and the output voltage level [2]. In the application of this technology in radar transmitters, to compensate for the pulsating power the output capacitor is increases. Energy efficient dc-dc power supplies are becoming more and more essential for power hungry circuits such as High Power Amplifiers (HPAs), however the challenge of switching noise tends to degrade the performance of the HPAs both directly and indirectly [3]. A commonly known approach to achieve reduced switching noise of a dc-dc power supply is to use additional passive filtering after the dc-dc power supply, thus introducing a LDO linear regulator that will act as a post regulation stage of the circuit [3].

The above mentioned approach works as a function of smooth low noise regulation but contributes greatly towards the inefficiency of the power supply due to the fact that LDOs are not very efficient due to the power dissipation that they carry.

2.3. Switch-mode power supply topology

Switch mode dc-dc converters are used to convert unregulated dc inputs into a controlled dc output desired voltage level [4]. Figure 2.4 below shows a typical block diagram of an AC/DC converter system. From AC in through the rectifier from AC to unregulated DC feeding into a capacitor filter and into a DC/DC converter that converts and regulated the output power of the systems.

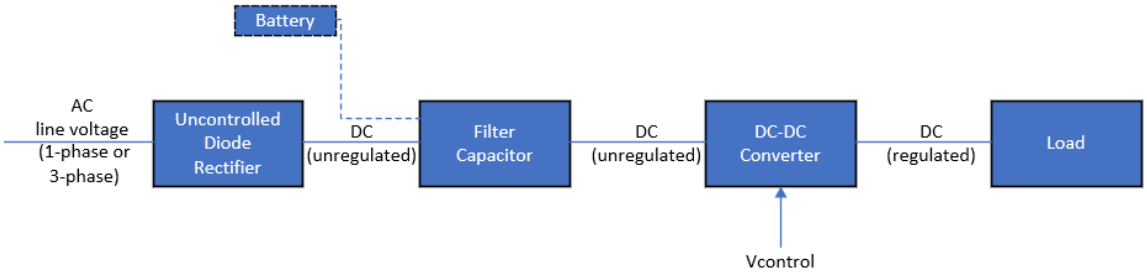

Figure 2.4: AC-DC Converter system [4]

2.3.1. Buck Converter

A Buck converter is also referred to as step-down converter, a step-down converter produces a lower average output voltage than the dc input voltage V_d [4]. The average output voltage is given by:

$$Vo = \frac{1}{T_s}\int_0^{T_s} v_o(t)dt \qquad 2.4$$

$$= \frac{1}{Ts}\left(\int_0^{t_{on}} v_d\, dt + \int_{t_{on}}^{T_s} 0\, dt\right)$$

$$= \frac{t_{on}}{T_s} V_d$$

$$= DV_d$$

Duty Cycle:

$$(V_d - V_o)DT_s = V_o(1-D)T_s$$

$$V_d D = V_o$$

$$D = \frac{V_o}{V_d} = \frac{t_{on}}{T_s} \qquad 2.5$$

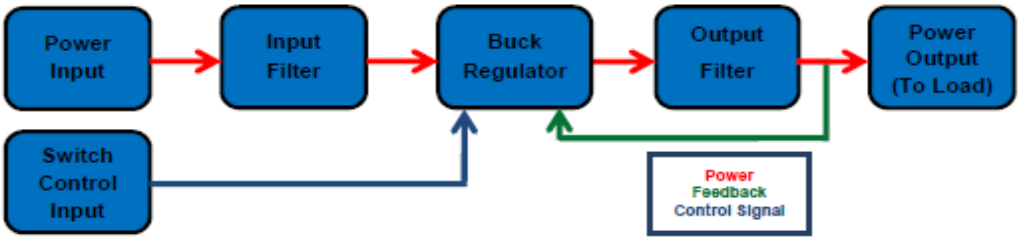

Figure 2.5: Buck Block Diagram [5]

The step-down converter has the capability of producing a well regulated output average voltage, less than the input voltage with a high output current by utilizing a synchronous switch [6], thus simultaneously stepping down the average output voltage while stepping up the output current. High step down application results in small operating duty cycle which causes shorter regulation time and as this causes high current stress of the circuit elements [7]. The topology is then given by the circuit shown in figure 8 below, thus a source voltage, a switch, and inductor, a diode, and a capacitor.

The Components in the circuit are given by:

Inductor

$$v = L\frac{di}{dt} \qquad 2.6$$

$$i = \frac{1}{L}\int v\, dt \qquad 2.7$$

$$E = \frac{1}{2} Li^2 \qquad 2.8$$

Capacitor

$$i = C\frac{dv}{dt} \qquad 2.9$$

$$E = \frac{1}{2}Cv^2 \qquad 2.10$$

$$v = \frac{1}{C}\int i\,dt \qquad 2.11$$

Inductor Current:

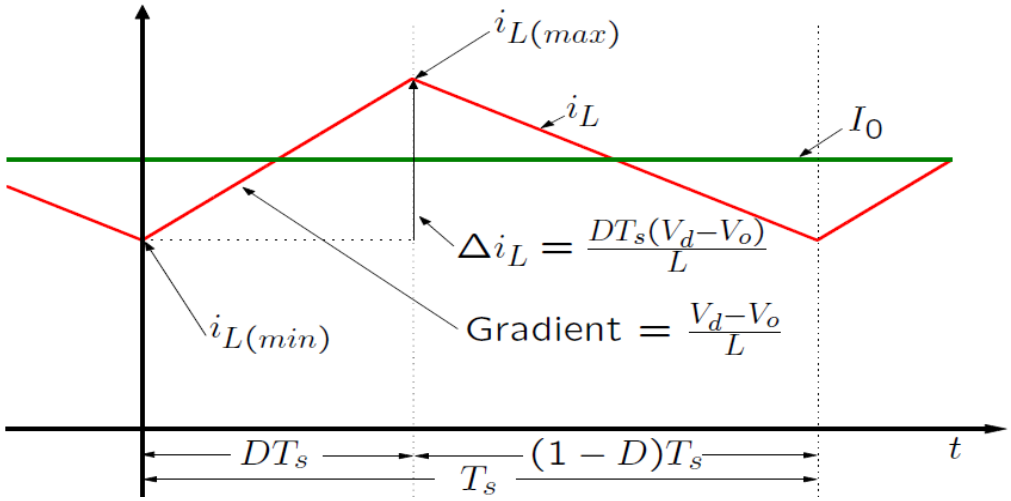

Figure 2.6: Inductor Current [8]

$$i_{L_{max}} = I_o + \frac{\Delta i_L}{2}$$
$$= I_o + \frac{DT_s(V_d - V_o)}{2L} \qquad 2.12$$

$$i_{L_{min}} = I_o - \frac{\Delta i_L}{2}$$
$$= I_o - \frac{DT_s(V_d - V_o)}{2L} \qquad 2.13$$

The buck uses the output capacitor and the inductor to store and transfer the energy from the input side of the circuitry to the load. A low-pass filter (LPF) is made up of the inductor (L1) and capacitor (C) to filter out the high frequency components [9]. Initially the current in the circuit is zero when the switch is open, the current will begin to increase when the switch is first closed and in response to the charging current the inline inductor will then start producing a voltage that is in opposite polarity across its terminals [6].

The Buck converter operates by switching on and off an input voltage to produce a lower output voltage. During the "on" time, the switch is closed, allowing current to flow from the input to the output inductor. The inductor stores energy during this process. In the "off" time, the switch opens, causing the inductor to release stored energy to the load. The duty cycle, determined by the ratio of on-time to the total switching period, regulates the output voltage. Figure 2.7 is a typical example of the inductor current and the output voltage.

Output Voltage Ripple

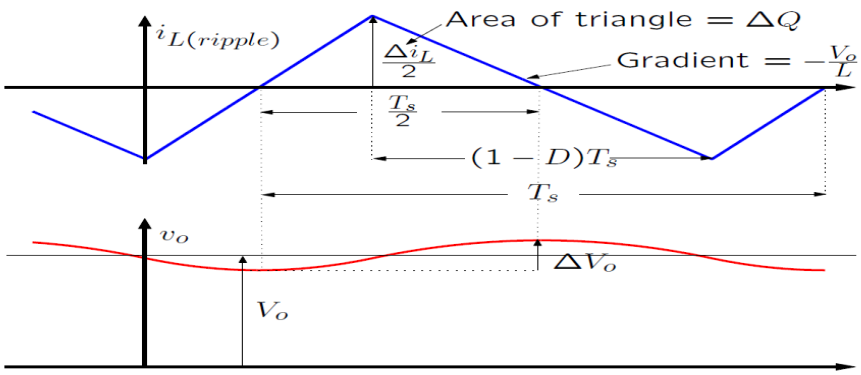

Figure 2.7: Output Ripple [8]

$$\Delta Q = \frac{1}{2} \cdot \frac{T_s}{2} \cdot \frac{\Delta i_L}{2}$$

$$= \frac{T_s \Delta i_L}{8} \qquad 2.14$$

2.3.1.1. Buck Converter Application Disadvantages and Challenges

The buck is an ever-present DC-DC converter that converts high DC voltage to lower DC voltage efficiently. The conversion is a trade-off between voltage and current, the converter drops the voltage while increasing the current as a give-and-take system. The buck converter can be designed and configured in such a way that the overall physical size is very small depending on the power requirements. The inductor and capacitor can be made very small by increasing the switching frequency. This is an advantage in terms of costs and physical size but it increases the switching losses.

For application where the delta between the input and output voltage at high currents can be challenging, these requires high duty cycle according to $V_o = V_{in}D$. Increasing the switching frequency to cater for a considerably small inductor and large enough capacitor can lead to inductor limitation such as current carrying capabilities. The option of changing the switching frequency to increase the period of the powers supply is limited by the Radar's pulse repetition interval as the power switching must be within one Pulse Repetition Interval (PRI).

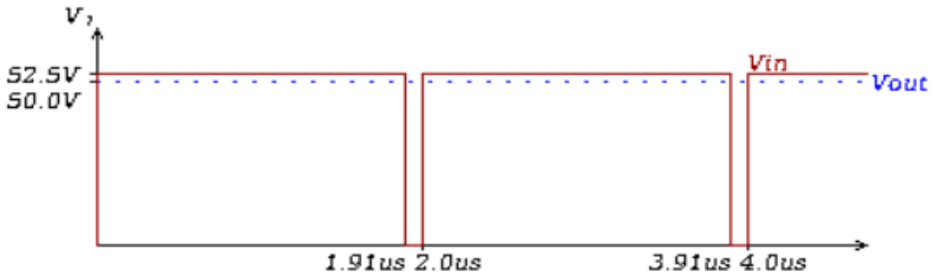

Figure 2.8: High Duty Cycle Simulated Switching time

As shown in the figure above, with the input and output voltage delta small, the transition of the MOSFET from ON to OFF and back to ON in as fast as 85ns. The control of such a short period is a challenge, this can be traded off with a lower switching frequency but that option will in-turn increase the inductor and capacitor size.

2.3.2. Boost Converter

A boost converter is also known as a step-up converter. The average output voltage is always greater than the input voltage. Typical operation is that when the switch is on, the diode is reversed biased as a result thus isolating the output stage. The input V_d provides power to the inductor L. When the switch SW is off, the output stage receives energy from the inductor and from the input as well. The output voltage V_o is defined by:

$$\frac{V_o}{V_d} = \frac{T_s}{t_{off}} = \frac{1}{1-D}$$

$$V_o = \frac{V_d}{1-D} \qquad 2.15$$

When the switch is on the inductor current flows through the switch and $i_{sw} = i_L$ and when the switch is off the inductor current flows through the diode and $i_D = i_L$.

Output voltage Ripple:

The average output voltage can be calculated as shown below. Assuming Constant output Current

$$\Delta V_o = \frac{\Delta Q}{C} = \frac{I_o\, DT_S}{C}$$

$$= \frac{\Delta V_o}{R}\frac{DT_s}{C} \qquad 2.16$$

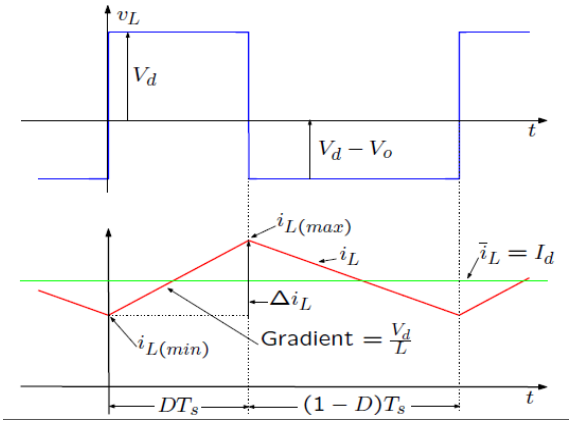

Figure 2.9: Output Ripple [8]

$$\Delta i_L = \frac{V_d}{L}\, DT_S \qquad 2.17$$

$$i_{L_{max}} = I_d + \frac{\Delta i_L}{2}$$

$$= I_d + \frac{DT_s V_d}{2L} \qquad 2.18$$

$$i_{L_{min}} = I_d - \frac{\Delta i_L}{2}$$

$$= I_d - \frac{DT_s V_d}{2L} \qquad 2.19$$

$$\Delta Q = I_o DT_S \qquad 2.20$$

2.3.2.1. Boost Converter Application Disadvantages and Challenges

The trade-off in the boost converter between current and voltage is that the increase in output voltage results in decrease in output current. This is because during the Switch ON time some of the current flows through the switch and the remaining current flows to the output. Given that the output voltage is increase by the rate at which the switch is turned ON and OFF, more and more current flows into the switch path dropping it more while increasing the output voltage.

From V = L di/dt, an increase in the inductor results in an increase in output voltage. Increase in switching frequency also result in an increase in the output voltage. The same challenge as the buck converter, the boost requires a fast and very short switching ON and OFF to get higher output voltage this can be a challenge to control the switch. The disadvantage regarding inductor in the boost configuration is that the increase in voltage is proportional to the increase of the inductor. Increasing the inductor results in a larger physical size. The same as in the buck converter, the option of changing the switching frequency to increase the period of the powers supply is limited by the Radar's pulse repetition interval as the power switching must be within the PRI.

2.3.3. Isolated switching power supplies

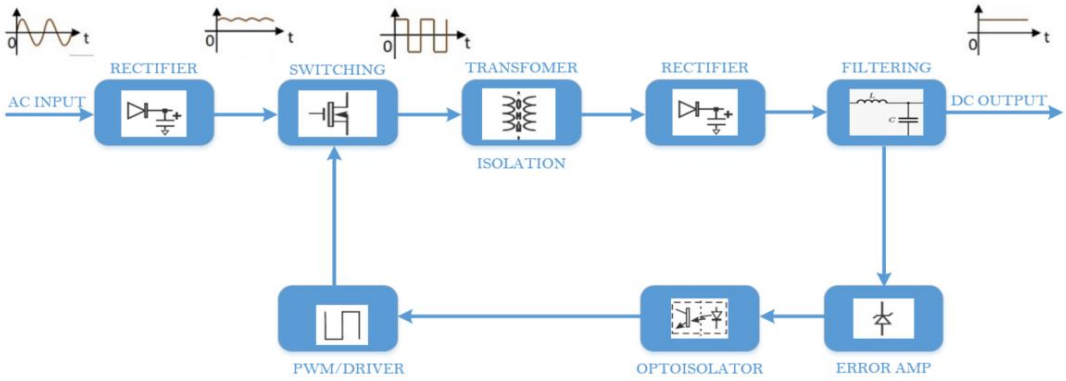

Figure 2.10: AC-DC Power stages with waveforms

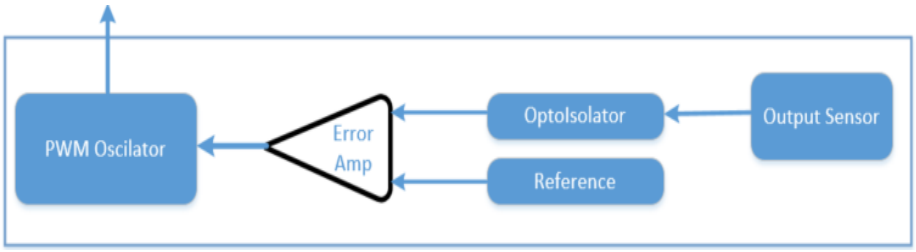

Figure 2.11: Control Unit

The isolated switching power supplies are basically derived from the basic switching power supply configurations. The isolation is achieved by means of a transformer. The mode of operation such as the give-and-take trade off remains the same. The advantage of the isolated configuration is the galvanic isolation between the input and the output side.

2.3.4. Fly-back Converter

The fly-back converter is derived from the buck boost converter. It is constructed of an isolation transformer with its primary winding connected to the source and an inline MOSFET back to the negative of the source. The secondary winding of the isolation transformer is connected with the diode D1 and a capacitor C in parallel with the load. The transformer in this configuration used to achieve isolation and energy storage [10]. The flyback converter is commonly used for power levels between 50-100W [11]. Fly-back converter is mostly attractive because of its simplicity and less components [12]. The operation of a fly-back is similar to that of the other SMPS, it is a combination of a series of ON and OFF [13].

$$\frac{V_{out}}{V_{in}} = \frac{D}{1-D} \qquad 2.\ 21$$

Where:

V_{out}: Output voltage across capacitor C1

V_{in}: Input source voltage

D: Duty cycle of switching pulse

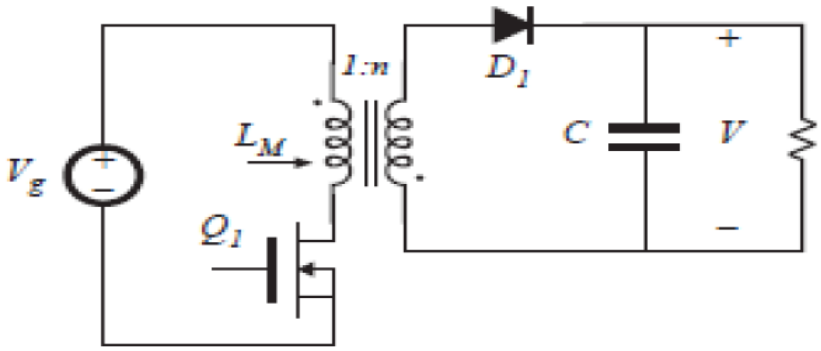

Figure 2.12: Flyback Converter [15]

2.3.4.1. Fly-back Converter Application Disadvantages and Challenges

The fly-back converter is basically a buck-boost chopper with an isolation transformer. This topology provides galvanic isolation between the input and the output. Fly-back converter can be configured for multiple outputs with a single control configuration, it has no inductor as the transformer acts as an inductor. Another advantage is that it has low voltage rating on the secondary side components making it easier to source components. It has fast transient response with an efficiency of about 75% to 80%.

As good as the advantage s are, the forward converter is for applications of about 50W, it comes with more EMI, more ripple current, more input and output capacitance and higher losses.

2.3.5. Forward Converter

Forward converters are part of the family of switched power supplies, they provide isolated and controlled dc voltage from an unregulated input dc input power supply [16]. Forward converters produce higher output power in rage of about 300W. The configuration of a forward converter comes with an output filtering that is not as simple as the other types of switching power supplies. Significance of a forward converter includes:

- Galvanic isolation between the input and the output.
- The transformer used in the forward converters has the flux waveform symmetrical to the positive and negative halves despite of the abrupt load variations which makes the transformer to operate below saturation [17].
- It makes use of filter inductor instead of transformer magnetizing inductance which makes its transformer less heavy.

2.3.5.1. Single switch Forward Converters

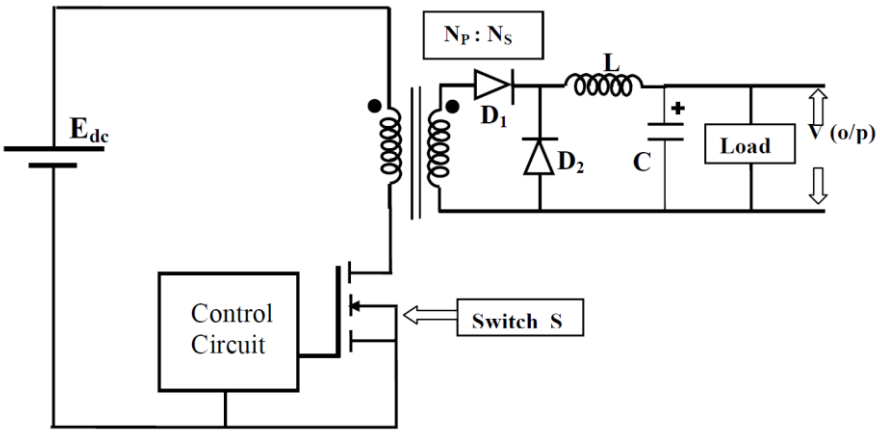

Figure 2.13: Single Switch Forward Converter [16]

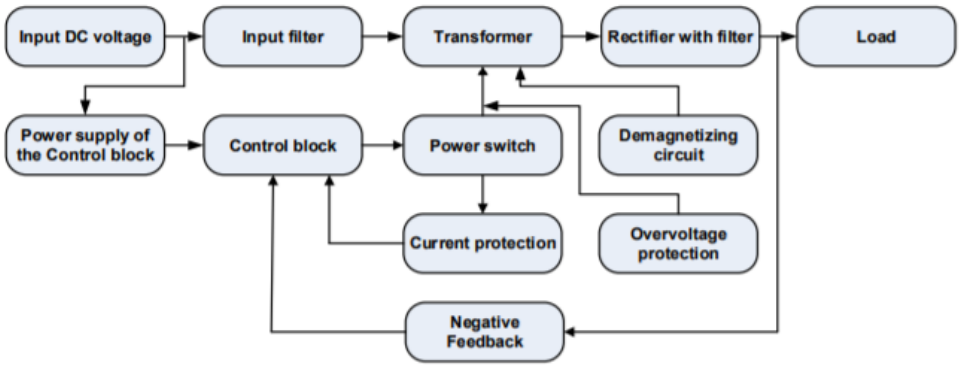

Figure 2.14: Structural Diagram of a single ended Forward Converter [18]

As shown in Figure 2.13, forward converters consist of a fast switching device that is connected to a control circuitry that controls the switching of the device, a transformer that is connected with the switching device in a series configuration on the primary side of the transformer, the secondary side of the transformer is connected with the filtering and rectification circuit of the converter.

When the MOSFET is on, D1 becomes biased and starts conducting inductor current which in turn increases during the on time of D1. When the MOSFET is then switched off, D2 then becomes biased and the inductor current then commutes to D2 and begins to decrease.in a case where the inductor current never decreases to zero during the off period, the converter is said to operate in continuous conduction mode.

Basically when switch S is turned ON, the input voltage is applied to the primary winding and a scaled voltage is induced to the secondary winding of the transformer. The scaling is specified by the turn's ratio of the transformer. D2 provides freewheeling path for this current. During the freewheeling, the filter inductor current starts dropping as it flows through the output but the large output filter capacitor maintains the output voltage closely constant.

Voltage across the secondary winding of the transformer is given by:

$$Vsec = \frac{NS}{NP} V \qquad 2.22$$

The instantaneous inductor voltage when switch S is ON is given by:

$$e_L(t) = \frac{NS}{Np} E_{dc} - V_o \qquad 2.23$$

The instantaneous inductor voltage when S is OFF is given by:

$$e_L(t) = -V_o \qquad 2.24$$

The Average output voltage is then given by:

$$V_o = D \frac{Ns}{Np} E_{dc} \qquad 2.25$$

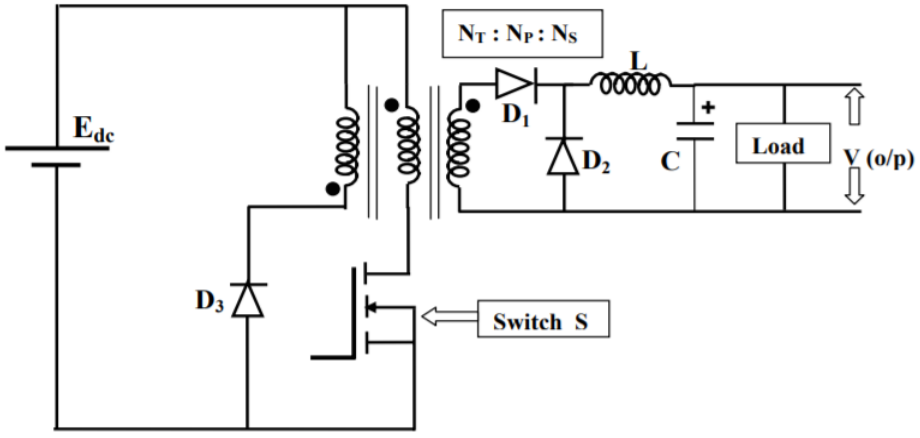

Figure 2.15: Practical Topology of a Forward Converter [15]

Different from the ideal topology, the practical configuration take into account the magnetizing current in the core of the transformer that is generated during the ON time of the switch S, the losses of the switch , the losses of the diode and the output filter.

Because of the energy stored in the core of the transformer, a third winding in series with a diode is employed. When both switch 'S' and 'D1' turn-off together, as discussed above, the magnetization energy will cause a current flow through the closely coupled tertiary winding and the diode 'D3'. The dot markings on the windings are to be observed. Current entering the dot through any of the magnetically coupled windings will produce magnetic flux in the same sense [16].

The decrease in the magnetizing current is expressed by:

$$\frac{N_T d\varphi_m}{dt} = -E_{dc} \qquad 2.26$$

As widely used as it is, it has a disadvantage of high voltage stress of the switch [19].

2.3.5.2. Two Switch Forward Converters

One of the advantages of the two switch forward converter over its single switch counterparts are the reduced switching noise and the lower voltage stress on the power semiconductor switch [20]. The severity of the voltage spark during the turn-off instance Is very little in the two switch topology[21]. This configuration is set up to provide a path for the leakage inductance to release all the stored energy to the input source.

The basic operation of a two switch forward converter shown in the figure above follows, both the fast switching transistors are turned on together allowing energy to be transferred to the primary winding of the transformer which in turn induce the energy into the secondary winding of the transformer, the forward rectifying diode then turns on allowing conduction transferring energy to the output filter and load.

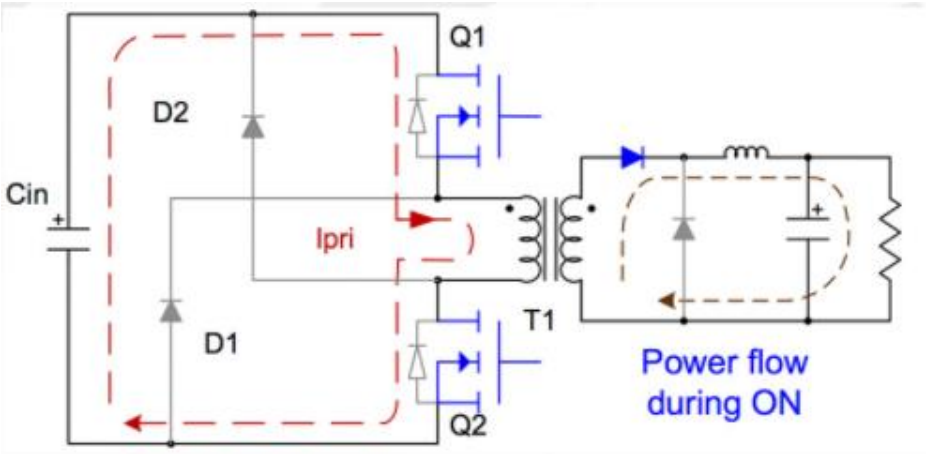

Figure 2.16: Two Switch On State [22]

When both switch Q1 and Q2 are switched off, the transformer magnetizing current flows through D1 and D2 which are now forward biased, the conduct until the magnetizing energy in the primary along with the energy stored in the leakage inductance is channelled back into the supply. The freewheeling diode conducts during the OFF time transferring the energy stored in the filter inductor into the load, the transformer reset occurs during this OFF time before the next ON time begins.

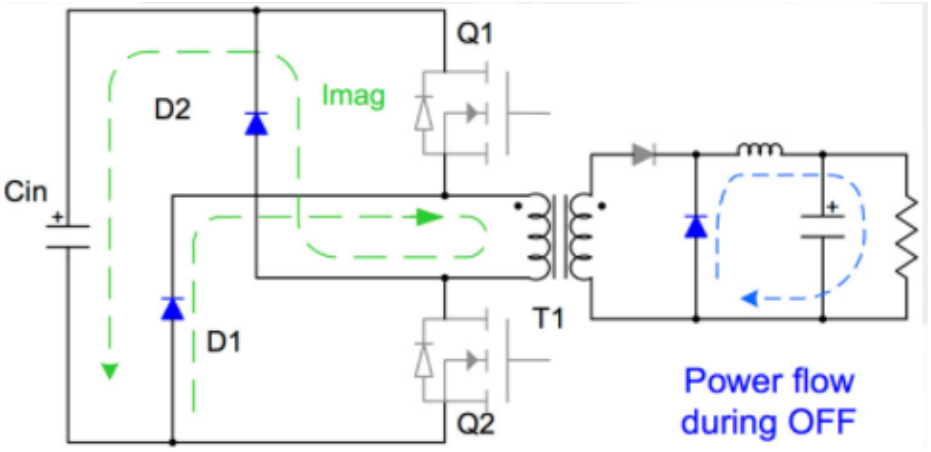

Figure 2.17: Two Switch OFF state [22]

2.3.5.3. Forward Converter Application Disadvantages and Challenges

The forward converter's mode of operation is derived from the buck converter. With all the advantage is that the buck converter has, the forward converter provides an isolated output from the input by means of a transformer. The forward converter also trades off voltage for current as a conversion factor. The forward converter has a single switch configuration and a two switch configuration, the two switch has higher power rating as it switch ON and OFF alternating the two switches instead of one switch.

As a result it low output current and voltage ripple as compared to the flyback topology. Another advantage of the two switch forward converter is that is doesn't require a snubber circuit and also has a low voltage stress across the switches and has low system power losses and noise.

As great as the advantages of the forward converter are, there are also a few setbacks. For the single switch configuration, the converter experiences high voltage stress across the switch, double the input voltage. It also is more expensive as compared to the buck due to the additional components, both the single switch and the two switch configuration.

The forward converter topology is best suitable for application where low output voltage and current ripple is required because of its low ripple capabilities and high current rating and low voltage stress across the switch in the two switch configuration.

2.3.6. Forward converter vs flyback converter

As we have discussed the advantages and the disadvantages of the isolated converters, forward and fly-back, the concluded comparison is as per table.

		Forward		Flyback	
		Traditional	Modern	Modern	Traditional
Decreasing Component Expense ↓	Power Transformer	1	1	1	1
	Controller IC	1	1	1	1
	FETs	2	4	2	1
	Output Inductor	1	1	1	0
	Signal Transformer	0	0	1	0
	Rectifier Diodes	2	0	0	1
	Output Capacitors	1	1	2	1
	TOTAL	8	8	8	5

Table 2.1: Forward vs Fly-back Converter [5]

Table 2.1 is a comparison in terms of components used in each specified topology configuration, forward and fly-back respectively.

	Forward	Flyback
Size (in^2)	3.2	2.6
Cost (normalized)	100%	90%
Efficiency (at 4 A_{OUT})	94.3%	92.8%
FET stress, pri (max)	90 V	146 V
FET stress, sec (max)	85 V	126 V

Table 2.2: Typical Example of Comparison

Table 2.2 compares the performance of the forward and the fly-back based on a 12V, 51W design and the stress across the switches in each design topology configuration.

2.4. Metal-oxide Semiconductor Field Effect Transistor

2.4.1. Metal-Oxide Semiconductor Field-Effect Transistor

A metal-oxide semiconductor field effect transistor is a voltage-controlled device that is widely used for switching and amplification purposes. It requires the continuation of a gate-source voltage within its operational range in order to be in its ON state and stay ON, removing or dropping the gate-source voltage below the threshold voltage with turn the MOSFET OFF. Current only flows during the transition from ON to OFF and from OFF to ON, thus when the gate capacitance is being charged and discharge respectively. The figure below shows a symbol of an N-Channel MOSFET. Metal-oxide field effect transistors are fast switching devices, being in the range of tens of nanoseconds to a few hundreds nanoseconds, depending on the device's characteristics [8] .

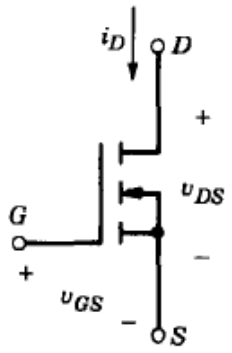

Figure 2.18: N-Channel MOSFET Symbol [8]

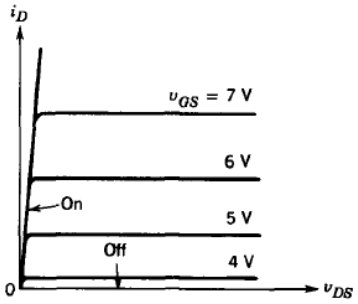

Figure 2.19: N-Channel MOSFET i-v Characteristics Graph [8]

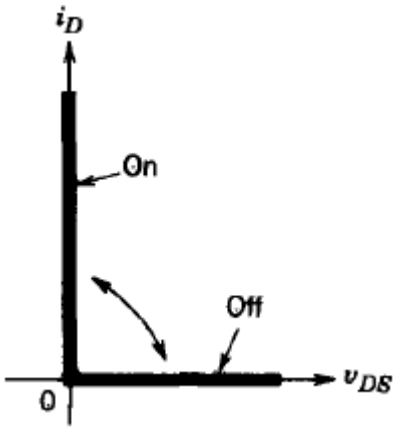

Figure 2.20: N-Channel MOSFET idealized Characteristics Curve [8]

MOSFET overcomes the disadvantages of FET such as high drain resistance, slower operation and moderate input impedance.

2.4.2. Classification of MOSFET

Metal-oxide field effect transistors are classified into two types based on their operation, Depletion mode of operation (D-MOSFET) and Enhancement mode (E-MOSFET). Their construction and material used further classify them into four different types.

- N-Channel Depletion mode MOSFET
- P-Channel Depletion mode MOSFET
- N- Channel; Enhancement mode MOSFET
- P-Channel Enhancement mode MOSFET

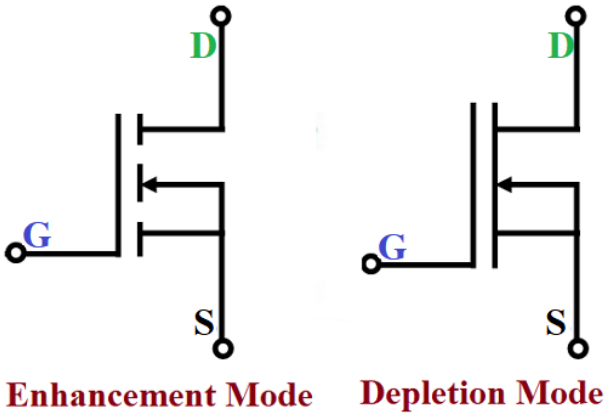

Figure2.21: NMOS Enhancement and Depletion Symbols

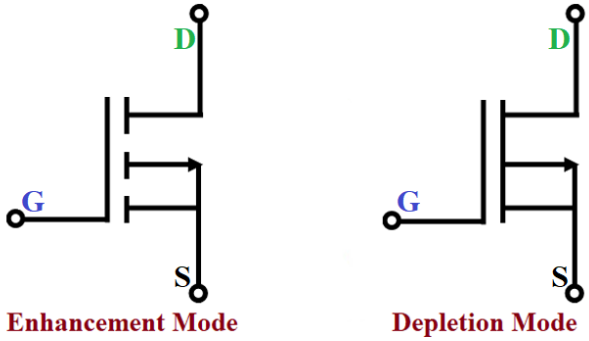

Figure 2.22: PMOS Enhancement and Depletion symbols

The difference between the N-channel and the P-channel is that the N-channel will stay in the OFF position until the minimum gate to source voltage is applied, making Drain and Source to connect. The P-channel is the opposite of the N-channel, it remains closed until the gate voltage is applied causing it to open, more like a normally open and a normally closed switch respectively.

E-MOSFET the gate voltage should always be positive while with the D-MOSFET the voltage can either be positive or negative and it never turns ON completely. E-MOSFET can only operate in the Enhancement mode while the D-MOSFET can operate in both Enhancement and depletion mode. Typically the Enhancement MOSFETs are used as a switch.

The sum of the on capacitor charging time and the actual rise time is the total time to switch the MOSFET on. The delay time is depended on the size of the capacitor and how much charge is required.

$$t_{off} = t_{d(off)} + t_f \quad 2.27$$

The total turn off time is the sum of the capacitor discharge time and the fall time, the discharging time is almost equal to the charging time.

The average gate current is given by:

$$I_{avg} = \frac{\Delta Q}{\Delta t} \quad 2.28$$

Drain current is given by:

$$I_D = \frac{V_{DD}}{R_{DS}} \quad 2.29$$

Where Q is the total charge of the MOSFET and t is the time required to charge it. The Δt is depended on the switching frequency, thus varying Fsw changes the average gate current.

Peak gate current is then given by:

$$I_{pk} = \frac{V_{GS}}{R_G} \quad 2.30$$

2.4.3. MOSFET Application Disadvantages and Challenges

Metal-oxide semiconductor field effect transistor are useful due to their input impedance being almost infinite and that gives them the capabilities to capture close to all input signals. Another advantage with MOSFETs is that they require close to no gate current in controlling the main load current when they are being compared to bipolar junction transistors. Their capability to operate with negative or negative voltage makes them efficient in design. With all the good features they have, MOSFET are still considered to have a shorter life span compared to other voltage controllable switches and they are also very susceptible to overload voltage.

For larger power applications, more charge is required to turn on the MOSFET because of the large physical area and as a result the switching speed is reduced, unless larger gate current is applied. MOSFET is more thermally stable due to its positive temperature co-efficient thus the increase in temperature during the ON time results in an increase in $R_{DS\,(ON)}$ and because of the on-resistance drop I_D also decreases and reduces the temperature of the MOSFET.

2.5. Capacitors

2.5.1. Super Capacitors

A Super capacitor is also referred to as ultracapacitor or EDLC (electric double layer capacitor). It is defined as a high capacity electromechanical capacitor with capacitance values much higher than other types of capacitors [24] and also has fast charge-discharge rate, high power density and long lifetime [25]. Supercapacitors work similar to the conventional capacitors, however supercapacitors have the capability to store more charge.

The capacitance is determined by the effective-area of the plates, the separation distance of the plates and the dielectric constant of the separating medium which is the same in the conventional capacitor [26]. The challenge with SC is that they have very low voltage rating, usually about 10V and lower. Voltage across a SC can be achieved by:

$$V_c = \frac{Q}{C} \qquad 2.31$$

Q is therefore the charge stored in the SC and C the capacitance of the SC. The Energy stored in the SC is then given by [27]:

$$E_C = \frac{1}{2} DV_c^2 \qquad 2.32$$

The unique feature of SC [28]:

- Extremely high volumetric efficiency, up to 100 times that of traditional capacitors.
- Very high energy density
- Ultra long life
- Fast charge and discharge capability with a large current rating.
- No need for current limiting protection.
- Maintenance free.
- Safer than batteries
- High temperature range

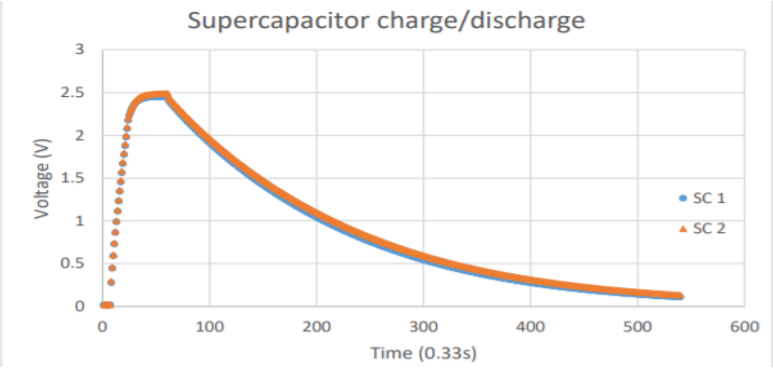

Figure 2.23: Typical charge and discharge curve of a supercapacitor [30]

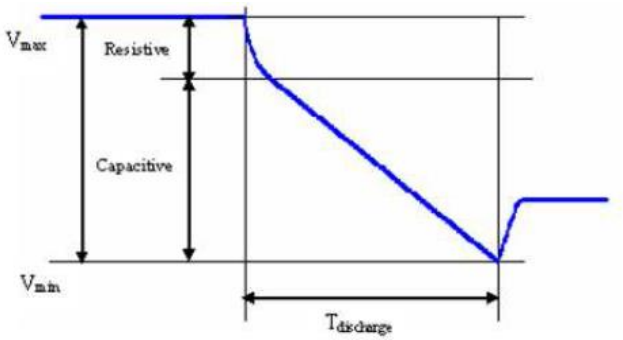

Figure 2.24: Supercapacitor Discharge profile [26]

2.5.2. Electrolytic capacitors

An aluminium electrolytic capacitor is made up of cathode aluminium foil, capacitor paper (electrolytic paper), electrolyte, and an aluminium oxide layer, which acts as the dielectric, formed on the anode foil surface [31]. The electrolytic paper and the foil are then wound into an element and then impregnated with electrolyte.

The relationship between the actual voltage and the effective capacitance is achieved by:

$$C_p = \frac{Q_p}{V_c} \qquad 2.33$$

Where C_p is the effective capacitance of the capacitor, Q_p is the charge and V_c is the measured voltage minus the voltage drop due to ESR [33].

Al-Cap is a widely used capacitor due to its high energy density and low cost but has a shorter lifespan as a result reduces reliability of systems [34]. An aluminium electrolytic capacitor provides a high ripple current capability together with a high reliability and an excellent price/performance ratio.

The capacitance of the capacitor is defined as:

$$C = \varepsilon_o . \varepsilon_r . \frac{A}{d} \qquad 2.34$$

Where:

C – Capacitance

ε_0 – Absolute permittivity

ε_r – Relative permittivity

A – Capacitor electrode surface area in m^2

D – Electrode spacing

The impedance of an aluminum electrolytic capacitor can be expressed as:

$$Z_c = ESR + jC_{cap} \qquad 2.35$$

$$= ESR + j\,w\,ESL - \frac{j}{wC}$$

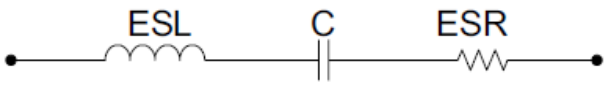

Figure 2.25: Equivalent circuit of an aluminium electrolytic capacitor [35]

$$ESR = \frac{DF}{2\,\pi\,fC} \qquad 2.\,36$$

In this application, the estimation of ESR intrinsic value of aluminum electrolytic capacitors used is of significance since they operate close to the resonance frequency [35]. An increased in ESR results in a significant increase in the alternate component of the output voltage, requiring a constant action of the control system.

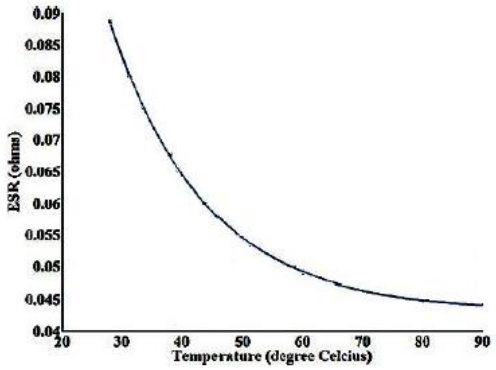

Figure 2.26: ESR Variation vs temperature [36]

The equivalent series resistance (ESR) is the resistive component of the equivalent series circuit. The ESR value depends on frequency and temperature and is related to the dissipation factor by the following equation.

$$ESR = \frac{tan\delta}{(\omega\,C_s)} \qquad 2.\,37$$

ESR Equivalent series resistance

tan δ Dissipation factor

CS Series capacitance

Since this capacitor are of a large capacitance per unit volume than the other types, this makes them of good choice and use in this application. Different from most capacitors, electrolytic capacitors have a voltage polarity requirement. This means that in the construction of the capacitor, the correct polarity is indicated on the housing of the capacitor by a stripe with minus signs and possibly arrowheads, denoting the adjacent terminal that should be more negative than the other. This is necessary because a reverse-bias voltage will destroy the center layer of dielectric material via electrochemical reduction

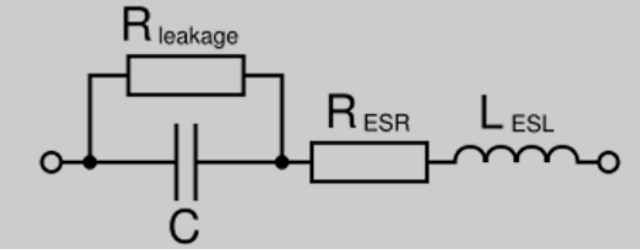

Figure 2.27: Equivalent Series Resistance

Where:

$R_{leakage}$ is the leakage resistance,

R_{ESR} is the equivalent series resistance,

L_{ESL} the equivalent series inductance

R_{ESR} must be as small as possible since it determines the loss power when the capacitor is used to smooth voltage. A parallel combination greatly contributes towards reducing the R_{ESR}. Loss power scales quadratically with the ripple current flowing through and linearly with R_{ESR}. Low ESR capacitors are imperative for high efficiencies in power supplies.

2.5.3. Capacitor Charging Current

The term ripple current is used to express the root-mean-square (RMS) value of the alternating current (AC) that flows through a device as a result of any pulsating or ripple voltage. Each family of capacitors comes with a range in ripple current that they can handle without degrading the performance of the capacitor. Power losses resulting from this ripple current induce self-heating of the capacitor. Ripple current results in higher dissipation in parasitic resistive portions of circuits like ESR of capacitors. The resulted dissipation is proportional to the current squared times resistance ($I^2 R_{ESR}$). And as a result, the RMS value of ripple current can be multiples of the RMS of the load current.

The maximum acceptable value of the ripple current depends on the ambient temperature, the equivalent series resistance (ESR) at the frequency of the AC signal, the thermal resistance, which is mainly determined by the surface area of the capacitor (which is the heat dissipation area) and the applied cooling. Moreover, it is restricted by the ripple current capability of the contact elements. This means that is also important to design the cooling system taking into account the optimum operating temperatures of the components.

The ripple current heats the capacitor and the maximum permitted ripple current is set by how much can be permitted and still meet the capacitor's load life specification. Too much temperature rise will cause the capacitor to exceed its maximum permitted core temperature and fail quickly, but operation close to the maximum permitted core temperature dramatically shortens expected life. The load life specifications for aluminium electrolytic capacitors operating at maximum permitted core temperature are typically 1000 to 10,000 hours.

2.5.4. Parallel Combination of Aluminium electrolytic Capacitors

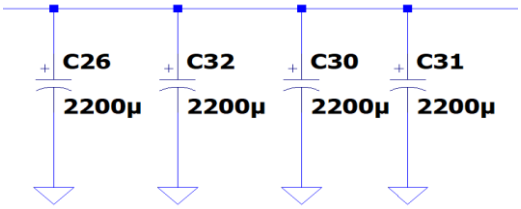

Figure 2.28: Energy Store Capacitor Connection

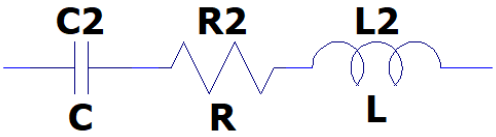

Figure 2.29: Energy Store Capacitor Internal Build up

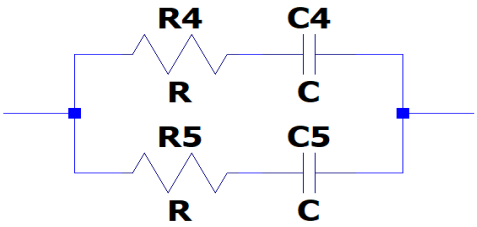

Figure 2.30: Energy Store Capacitors Parallel Combination

Figure 2.28 above is a representation of parallel combination of capacitors. With this configuration, comes with some advantages.

Figure 2.29 above is a representation of the internal build-up of a capacitor, consisting of the capacitance, some resistance and some inductance. The parallel combination adds up the capacitance and on the other hand reduces the resistance by creating a parallel resistor configuration. Figure x below is a representation of the configuration.

$$R_{total} = \frac{R_4 \, x \, R_5}{R_4 + R_5} \qquad 2.\,38$$

$$C_{total} = C_4 + C_5 \qquad 2.\,39$$

The capacitance will add up and the resistance will reduce since it is a parallel combination for both respectively. The above discussed configurations results in high current ripple handling capabilities, high reliability in a sense that failure of one capacitor doesn't results in a complete maximum worse case ripple current and reduces cost in terms of buying high value capacitance with high voltage compared to a combination of parallel capacitors.

The power losses and heat generated in the capacitor is driven by the formula

$$P_{ESR} = I^2 \, x \, R_{ESR} \qquad 2.\,40$$

Equation 43 above means that a reduced R_{ESR} results in lower power losses with the current being constant. As stated above, since the parallel configuration reduces the internal resistance of the capacitor resulting in lower power losses.

The parallel combination brings about a lot of advantages but also comes at a cost. The capabilities of having high current ripple reduces the life span of the capacitors and over time comes with reduces reliabilities.

2.6. Literature Review Conclusion

Based on the literature reviewed, the combination of a linear regulator and a switch mode power supply topologies proves to be the best approach toward the stated problem. The mitigation of the switching noise from coupling into the carrier signal to be transmitted can be suppressed via a precise control technique of the SMPS converter.

The best approach to prevent the switching signal to couple into the carrier signal is to ensure that just before every pulse the switching of the forward converter is turned OFF and switched ON again right after the pulse, this technique is to be modelled with precision and stability from pulse to pulse.

This integration of an SMPS into the power hold-up module should theoretically give an outcome that best translate the use of an SMPS into a hold-up module to improve efficiency and reduce the size of the hold-up module.

Chapter 3

Switch Mode Power Supply based Hold-up Module Evaluation and Design

In the switch mode supply family, the possibly options for a microwave power amplifier is directed towards the isolated topologies, thus the flyback converter and the forward converter. This chapter evaluates the application of the forward converter and compares the results with previous microwave power amplifier power supply with an analogue controller. The evaluation is done through simulation using LTSpice.

3.1. SMPS Controller

3.1.1. Single switch synchronous Forward Controller

LT1952-1 Features

- Synchronous Rectifier Control for High Efficiency
- Programmable Volt-Second Clamp
- Output Power Levels from 25W to 500W
- Low Current Start-Up
    - (LT1952: 460µA; VIN On/Off = 14.25V/8.75V)
    - (LT1952-1: 400µA; VIN On/Off = 7.75V/6.5V)
- True PWM Soft-Start
- Low Stress Short-Circuit Protection
- Precision 107mV Current Limit Threshold
- Adjustable Delay for Synchronous Timing
- Accurate Shutdown Threshold with Programmable Hysteresis
- Programmable Slope Compensation
- Programmable Leading-Edge Blanking
- Programmable Frequency (100kHz to 500kHz)
- Synchronizable to an external clock
- 2.5V External Reference
- Current Mode Control
- Small 16-Pin SSOP Package

Description

The LT1952-1 is a current mode PWM controllers optimized to control the forward converter topology, using one primary MOSFET. The LT1952-1 provides synchronous rectifier control, resulting in extremely high efficiency. A programmable Volt-Second clamp provides a safeguard for transformer reset that prevents saturation. This allows a single MOSFET on the primary side to reliably run at greater than 50% duty cycle for high MOSFET, transformer and rectifier utilization. The devices include soft-start for controlled exit from shutdown and undervoltage lockout.

A precision 107mV current limit threshold, independent of duty cycle, combines with soft start to provide hiccup short-circuit protection. The LT1952 is optimized for micropower bootstrap start-up from high input voltages. The LT1952-1 allows start-up from lower input voltages. Programmable slope compensation and leading-edge blanking allow optimization of loop bandwidth with a wide range of inductors and MOSFETs. Each device can be programmed over a 100kHz to 500kHz frequency range and the part can be synchronized to an external clock. The error amplifier is a true op amp, allowing a wide range of compensation networks. Other Suitable SMPS Controllers

- LTC1950
- LTC3752
- LTC3753

The above mentioned SMPS controllers are within the desired specification that can be configured and optimised to meet the HUM's specifications and they all have different limitations with their different configurations.

3.2. Proposed Forward Converter Configuration

With the identified potential controllers for this development, the LT1952-1 is deemed more suitable than the other controllers. It has a much less sophisticated configuration in modeling the power hold-up module and it is well within the capabilities required for the HUM.

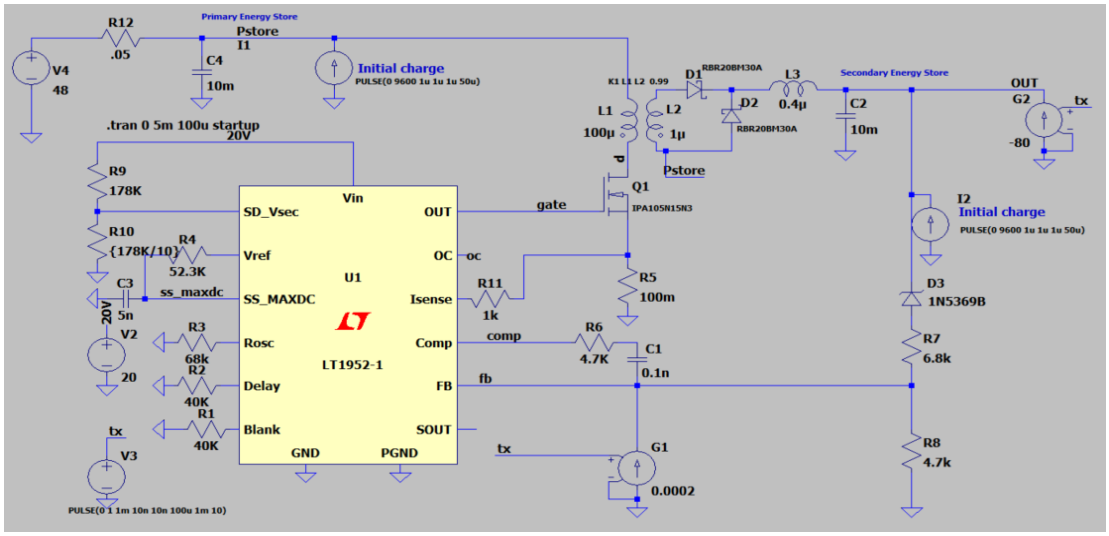

Figure 3. 1: Proposed Forward Converter Setup

3.3. Configuring a forward converter to meet requirements

The mode of operation is on two pulse repetition frequencies. The first step in setting up the simulation is identifying a switching controller that can do these frequencies. Switching frequency of the controller is another step in the frequency identification and selection.

Having a standard forward converter topology with the main source of power supplying all the power to the output stage proved to be inefficient. This is because to be able to produce current of about 10A at 50V requires a high duty cycle and that makes it almost impossible to find components that can do the regulation comfortably.

The DC-DC power supply shall charge the output capacitor bank to the same charge level from pulse to pulse, with a PRI of 142.29us at a 15% duty cycle, the pulse length is 21.34us. This leaves 120us to charge a 44mF capacitor bank. In this 120us recovery time, rise and fall time of the switch is to be catered for leaving very little time to charge the capacitor bank to the required level without pushing the MOSFET to an uncomfortable operating region.

The proposed evaluated configuration is in such a way that a bulk of the power to the output stage is provided for by the main power supply referred to as the vicor power supply, which is a 800W at 48V.

The simulation's primary focus is:

At PRF: 1.36 kHz

- Switching controller
- Input current ripple
- Output voltage stability
- Output voltage droop
- Heat analysis

3.3.1. Input Parameter of the SMPS based Hold-up module at 1.36 kHz pulse repetition frequency

3.3.1.1. Input Current Ripple

The input current ripple must be within the current ripple carrying capabilities of the capacitors in the input filter and inductors.

3.3.1.2. Input Current Ramp-up

The input current is to ramp up as the capacitor voltage ramps up to 50VDC. The ramp up is controlled and limited by the inrush current control circuitry. With the 1.36kHz PRF the maximum operating current is to be maintained at about 15A with a 1A safety net, thus operating at below 16A maximum.

3.3.1.3. Input Power Consumption

The input power consumption at PRF 1.36kHz is to be maintained at about input current of 15A max at 48VDC.

3.3.2. Output Parameters of the SMPS based Hold-up Module at 1.36 kHz pulse repetition frequency

This section of the requirements covers the 1.36kHz PRF based major requirements thus looking at the output voltage, voltage droop and the output current.

3.3.2.1. Output Voltage Stability and output voltage droop

The output of this power hold up module must as stable as best maintain the 50VDC with the same flatness after every pulse. This means that the output voltage regulation must be constant from pulse to pulse. 50VDC when the capacitors are charged subtract the droop during the pulse and then back to the 50VDC after the pulse. The voltage droop at 1.36kHz is to be set to 500mV max.

3.3.2.2. Output Inductor current

The output inductor is to charge up within the allowable charging time. This means that it must be at 0A during the pulse and start charging up right after the pulse. This is to be repeatable as a replica of each PRF.

3.3.2.3. Output Voltage Stability

The output of this power hold-up module must as stable as best maintain the 50VDC with the same flatness after every pulse. This means that the output voltage regulation must be constant from pulse to pulse. 50VDC when the capacitors are charged subtract the droop during the pulse and then back to the 50VDC after the pulse.

3.3.2.4. Output Inductor current

The output inductor is to charge up within the allowable charging time, the charging time is when the pulse is off and the main switching MOSFET is switching, inducing voltage to the secondary side of the transformer. This means that it must be at 0A during the pulse and start charging up right after the pulse. This is to be repeatable as a replica of each PRF.

3.3.3. Switch Mode Power Supply based Hold-up Module Evaluation Conclusion

With the above mentioned requirements and analysis done, the design of the above mentioned power hold up module is deemed to be feasible. Simulation will be dome and extensively analysed to assess and conclude on the switch mode based hold up module.

Design Specifications

This section details the specifications in which the HUM is designed upon. The approaches discussed and evaluated in chapter 3 are incorporated in the PCB design. The design setup is in such a way that it covers aspects from the PFC assembly, the HUM and military and industry compliance.

3.4. High Power Amplifier Assembly

3.4.1. Overview

The high power amplifier subsystem is built up of multiple power amplifiers combined to achieve the design requirement specified output power. Each of the power amplifier outputs are phase matched before fed into the high power combiner.

The power supply of each power amplifiers comprise of a power conditioning module along with a hold-up module. The power conditioning modules is responsible for the filtering and power factor correction of the main input power, it then provides the hold-up module with 48VDC. The hold-up module ensures that the pulsed load from the power amplifier is converted to a constant current.

3.4.2. Hold-up Module

The hold-up module shall maintains the specifications across the pre-set pulse repetition frequencies at a given duty cycle. This means that the switch mode controller shall stop the switching before each pulse is transmitted, and for the SMPS to stop switching the secondary storage capacitor bank shall be charge to the pre-set state of charge.

3.5. SMPS Based Hold-up module Requirements

The designed for power amplifier requires 50VDC and 12VDC supply voltages to operate the amplifier and the control logic respectively. The PA requires an average of about 9.6A typical and 16A maximum at a pulse width of 200us with a duty cycle of 13% and 20%, thus 73.85A and 80A pulsed current peak at 50VDC respectively. This design will be based on the Maximum of 16A average current and 80A pulsed current as calculated below.

3.6. External Interfaces

- Frequency
- Max output power level
- Input voltage
- HPA control

Given:

Duty cycle of the PA: 20%

Maximum PA average current: 16A

$$I_{Peak} = \frac{I_{DC}}{DC} \qquad 3.1$$

$$= \frac{16A}{20\%}$$

$$= 80A$$

3.7. Required output of the Hold-up module

Pulse length Limits

- Minimum 21us
- Maximum 110us

Pulse length design

- Maximum 110us

Input Power

- 48VDC regulated with a maximum average current of 15A.

Output Supply Voltage

- 50VDC from pulse-pulse

3.8. Detailed Operation and Design

Circuit Design of the Converter

In this chapter, the concept of operation and the design of the switch mode HUM will be discussed in detailed along with all the aspects of the power amplifier than needs to be catered for in the design.

3.8.1. Concept of operation

This Hold-up module is based on the LT3753 active clamp synchronous forward controller. The controller is a current mode PMW controller that is designed for active clamping forward converter topology. Active clamp reduces switch voltage stress on the main switching mosfet and increases efficiency but restricts permissible duty cycle.

The controller has a programmable volt-second clamp that can be programmed to provide a duty cycle guardrail. This is to protect the transformer from potential saturation damages. The IC contains a voltage error amplifier to allow a very simple non-isolated, fully regulated synchronous forward converter. This is by programming the feedback line connected to the controller to maintain the pre-set output voltage.

The controller has a wide range of protection features that includes programmable system input under voltage lockout (UVLO), programmable system input overvoltage lockout (OVLO), programmable overcurrent (OC) hiccup mode, and built-in thermal shutdown. Programmable slope compensation and switching frequency allow the use of a wide range of output inductor values and transformer sizes

With all the features of the LT3753, the hold-up module is configured in such a way that it successfully provides DC power to the pulsed microwave power amplifier in the kW range while maintaining the stability and efficiency. The primary energy store assists the main 48VDC input in charging the secondary energy store within the available charging time in the PRI based on PRF, but the charge is stored at a voltage lower than the required output voltage. The switch-mode controller has an isolated output port that is connected in series with the primary store to raise the voltage to that of the required output voltage.

3.8.1.1. Input Stage

Reverse Voltage Protection

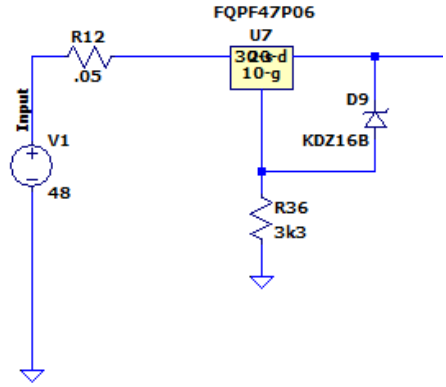

Figure 3. 2: Reverse Voltage Protection

Inrush Current and control circuitry

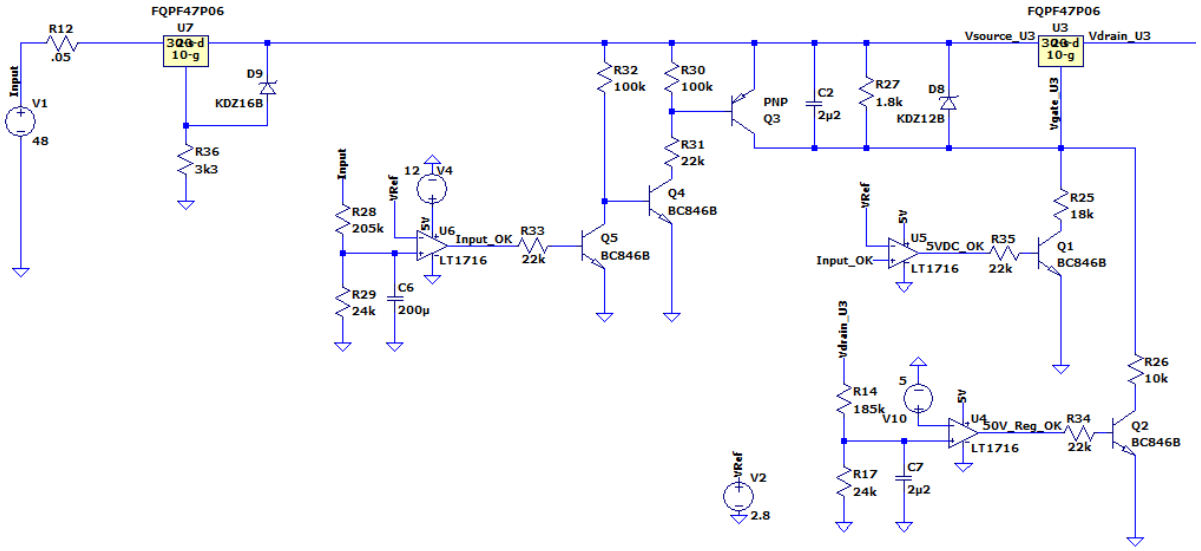

Figure 3. 3: Current Limiter and Control Circuitry

Initial states:

- U6 Rail-rail comparator is OFF
- Q5 transistor is OFF
- Q4 transistor is ON
- Q3 transistor is ON
- U3 MOSFET is OFF
- U5 rail-rail comparator is OFF
- Q1 transistor is OFF
- U4 rail-rail comparator is OFF
- Q2 transistor is OFF

Initially, the pnp transistor Q3 is conducting, making Vsource and Vgate equal. With 0Vgs the FET U3 is not conducting. After house keeping power conditioning is at steady-state, comparator U6 receives reference voltage and the input voltage via a resistor divider supplies the second input to the comparator which is higher than the non-inverting input thus switching ON the comparator U6 with output designator “Input _OK”. Input_OK supplies Vb to the transistor Q5, pulling down Vb of transistor Q4. By pulling down Vb of transistor Q4, Ve of pnp transistor Q3 becomes lower than Vc of the same Q3 which switches the transistor Q3 to a non-conducting state.

Input_OK is fed to comparator U5 and a reference voltage is also applied to U5 thus switching ON the output “5VDC_OK” which in turn provides Vb to transistor Q1. The transition of Q3 to non-conducting sets the programmed gate-source voltage. Once the threshold gate-source voltage of FET U3 is reached, current starts flowing through the FET U3 and Vdrain starts ramping up.

Once the drain voltage of FET U3 is above 45VDC and the delay capacitor C7 is charged, the inverting input and the reference voltage switches ON the comparator providing Vb to transistor Q2. With transistor Q2 switch ON, a R25 and R10 makes a parallel combination, this new resistor value then allows the gate-source voltage to move above -10VDC switching the FET U3 hard and allowing more current to flow through.

R27 and R25 are programming the voltage across the gate and the source of the mosfet U5 at the initial stage of gate-source. Varying R27 will then vary the amount of inrush current allowed through the mosfet on start-up and consequently the charging time.

The values of R27, R25 and R26 are calculated in such a way that the gate-to-source voltage of the FET U3iiiii is kept within the operating parameters of the FET. Below are calculations showing how the values are calculated.

$$V_{gate} = V_{Input}\left(\frac{R_B}{R_B+R_T}\right) \qquad 3.2$$

$$= 48\left(\frac{18x10^3}{18x10^3 +10x10^3}\right)$$

$$= 43.64V$$

$$= 48V - 43.64V$$

$$= 4.36V$$

$$V_{gate} = V_{Input}\left(\frac{R_B}{R_B+R_T}\right) \qquad 3.3$$

$$= 48\left(\frac{6.43x10^3}{6.43x10^3 +1.8x10^3}\right)$$

$$= 37.5V$$

$$= 48V - 37.5V$$

$$= 10.5V$$

With input voltage of 48V and selected operational value of FET at -10.5V, the gate voltage of the FET is calculated to be 37.5V to set Vgs to -10.5V. The required resistor combination is then worked out as:

$$V_{gate} = V_{Input}\left(\frac{R_B}{R_B+R_T}\right) \quad 3.4$$

$$V_{input}\ x\ R_B\ = V_{gate}(R_B + R_T)$$

$$R_B = \frac{V_{gate}\ x\ R_T}{V_{in} - V_{gate}}$$

$$= \frac{37.5V\ x\ 1.8x10^3}{48V-37.5V}$$

$$= 6.43k\Omega$$

The parallel combination of R25 and R26 must product 6.43kΩ. The product is calculated as follows:

$$R_X = \frac{R_1\ x\ R_2}{R_1 + R_2}) \quad 3.5$$

$$(R_1\ x\ R_2)\ = R_X(R_1 + R_2)$$

$$(18x10^3\ x\ R_2)\ = 6.43x10^3(18x10^3 + R_2)$$

$$R_2 = \frac{115.713x10^6}{18x10^3 - 6.43x10^3}$$

$$= 10k\Omega$$

To ensure that Vgs is maintained within the -20V operating region, a Zener diode is used to clamp it at 12VDC.

The gate-to-source at start-up during the current limiting is clamped to -4.36V allowing a constant initial charging current of about 2A . After the bulk initial charging of the capacitor primary and secondary energy store banks, the FET is then driven hard to allow the flow of just above the steady-state or operational input current thus at range -10.5VDC.

The LT3753 forward controller is capable of going well above 50 percent duty cycle for high switching frequency applications, transformer and rectifier utilization.

The comparator non-inverting inputs are calculated as follows:

Input Ok comparator

$$V_{comp\_in\_(+)} = V_{Input}\left(\frac{R_B}{R_B+R_T}\right) \qquad 3.6$$

$$= 48\left(\frac{24x10^3}{205x10^3 + 24x10^3}\right)$$

$$= 5.03V$$

Second Stage Current limiting comparator

$$V_{comp\_in\_(+)} = V_{Input}\left(\frac{R_B}{R_B+R_T}\right) \qquad 3.7$$

$$= 46\left(\frac{24x10^3}{185x10^3 + 24x10^3}\right)$$

$$= 5.28V$$

Input filter and primary energy storage bank

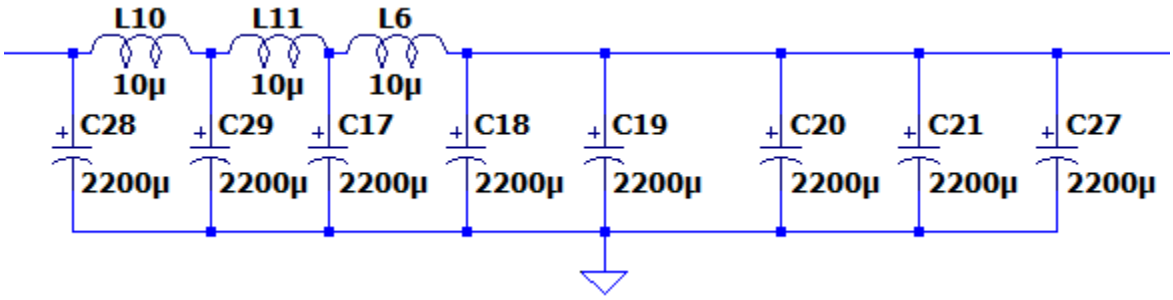

Figure 3. 4: Input Filter and Primary Energy Store

In order to filter out high frequency noise to the input supply and to the load (output), low pass filters must be added to the input and output circuits. Ideally signals above 50kHz should be attenuated. The inductor and capacitor cascade forms a filter with a cut-off frequency of about 39.18kHz as show in the calculation below. The filter used in this design is the Chebysheb PI Filter.

The filter capacitors are of dual purpose, thus forming part of the filter and primary energy storage. The configuration is in such a way that after every pulse, the primary energy store will provide energy for the power supply to fully charge up the secondary energy store within the off time of the load pulse.

This is achieved by determining the cut-off frequency according to:

$$fc = \frac{1}{2\pi\sqrt{LC}} \qquad 3.8$$

$$= \frac{1}{2\pi\ x\ \sqrt{30x10^{-9}\ x\ 2200x10^{-6}}}$$

$$= 39.18kHz$$

3.8.1.2. Transformer Selection

The transformer forms part of the energy transfer design that transfers energy from the primary/input stage to the secondary side of the converter and galvanically isolates the output circuit. The turns ratio is selected to top up about 2V to the input voltage (which is also an input to the rectifier at the secondary side) in order to maintain the 50VDC required by the power amplifier at the output stage.

Because the forward converter must accommodate the input voltage fluctuation, the forward converter must be designed to carter more than the required 2V. Therefore the selection of the transformer must be selected inline with that.

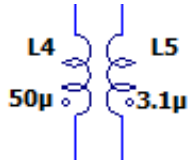

Figure 3. 5: Transformer

N = 1

Turns ration => 1 : t

$$t = \frac{\sqrt{Secondary\ winding\ inductance}}{\sqrt{Primary\ winding\ inductance}} \qquad 3.9$$

$$= \frac{\sqrt{3.1x10^{-6}}}{\sqrt{50x10\text{^}-6}}$$

$$= 0.24899 \approx 0.25$$

$$Turns\ Ration\ (N = n) = \frac{\sqrt{Primary\ inductance}}{\sqrt{Secondary\ inductance}} \qquad 3.10$$

$$= \frac{\sqrt{50x10^{-6}}}{\sqrt{3.1x10\text{^}-6}}$$

$$= 4.016 \approx 4$$

With input voltage at 48V, 2V volts must be regulated via the transformer. The output voltage of this configuration is given by:

$$V_{out} = V_{in}\ x\ n\ x\ D$$

Vin = 48VDC (Fixed)

Vout = 50VDC (Fixed)

n = 0.25 (Fixed by transformer selection)

D = Adaptive/Variable

Duty cycle can be varied to obtain the right output voltage. A variable resistor is used as Rivsec resistor to be able to adjust the Duty cycle. The output voltage can also be tuned by varying the feedback resistor configuration. Even though the controller can go up to 72% duty cycle, the transformer maintains its limitations. The active clamp switch control (Aout) contributes significantly in handling the residual flux of the transformer through the active clamping process.

To clamp the controller to 50 percent duty cycle, Rivsec must be as follows.

$$D_{vsec} = 0.725\ x\ \frac{R_{ivsec}}{51.1k}\ x\ \frac{1.25}{UVLO_{vsec}} \qquad 3.\ 11$$

$$R_{Ivsec} = \frac{D_{vsec}\ x\ 51.1k}{0.725\ x\ \frac{f_{osc}}{300}\ x\ \frac{1.25}{UVLO_{vsec}}}$$

$$= \frac{0.5\ x\ 51.1x10^{3}}{0.725\ x\ \frac{500}{300}\ x\ \frac{1.25}{1.69}}$$

$$= 28.58k\Omega$$

Duty cycle less than 50 percent

This design has the active clamp driven by the same controller driving the transfer of energy from primary to secondary side of the transformer. This active clamp configuration is not very much advanced. One of the challenges associated with the active clamp is the need for a precise duty clamp. Meaning that the duty cycle must be kept within specific limits. If not clamped to some maximum value, increased duty cycle can result in transformer saturation or additional voltage stress on the main switch which can be catastrophic to the converter as a whole. Another disadvantage has been the need for an advanced control technique to synchronize delay timing between the active clamp and main switch gate drive.

This design then clamps the duty cycle to about 50% to ensure that the transformer does not saturate resulting to damaging the transformer and the FETs functioning with it. Although the controller itself is capable of allowing well above 50% duty cycle, this configuration is in place as a safety measure.

3.8.1.3. Active clamping

Active clamping is defined as a protective function that acts as an absorber of the back-EMF generated during the switch-off of the low side of the switch. This function/configuration also eliminates the need for freewheeling diodes designed to return the generated back-EMF back into the power source.

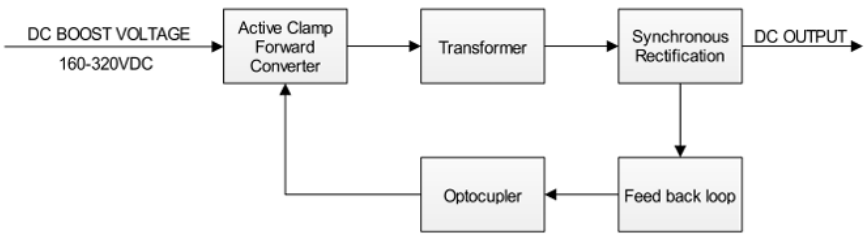

Figure 3. 6: Active Clamping

Traditionally, the Resistor-Capacitor-Diode (RCD) snubber circuit is used as a measure to maintain the stress on the semiconductors within the circuit to keep them within their safe operating limits, but the RCD comes with disadvantages as well. The introduction of active-clamp circuits overcome the shortcomings of the RCD clamp circuit. Active clamps not only recover the energy of the magnetizing inductance and leakage inductance, but they also suppress the voltage spike on the main switch MOSFET.

The concept is such that:

When the main switch is ON, energy is stored in the transformer's magnetic field, energising the primary winding thus inducing voltage to the secondary winding of the transformer.

When the main MOSFET is OFF, the energy stored in the transformer leakage inductance creates an inductive spike across the MOSFET.

To control and limit the spike, the active clamp MOSFET is switch ON shortly and or before the turn OFF of the main MOSFET.

With the active clamping operating, the energy stored in the leakage inductance is redirected to the clamping circuit and dissipated efficiently. Active clamp switches OFF and main MOSFET switches ON.

3.8.1.4. Synchronous Rectification

Synchronous rectifiers play a significant role in improving the efficiency of power converters, this is achieved by replacing diode rectifiers with MOSFETs. Synchronous rectification can be self-driven or controlled with an external controller, in this design we explore the self-driven synchronous rectification.

Choosing the suitable MOSFETs to use in a self-driven synchronous rectifier comes with a number of considerations. In a self-driven application, the MOSFET gate-to-source voltage is ideally derived directly from the transformer secondary. As a result, the gate drive voltage is not regulated but instead varies as a function of the voltage induced on the secondary side of the transformer since the gate of the rectifier FET is directly fed from the secondary side of the transformer

The configuration of having the synchronous rectifier in a self-driven SR implementation, thus the SRs are driven directly with the secondary voltage of the transformer result in the self-driven SR approach being very attractive since it is simple and requires a minimum number of components.

Synchronous rectification replaces the diodes with mosfets. Because mosfets are actively controlled, it makes the design more efficient. Mosfets has a low Rds_{on} they the act as resistors switched on and off in line with the circuit making them efficient compared to the use of diodes. Using a synchronous rectifier enables power losses to be minimised and efficiency levels to be improved.

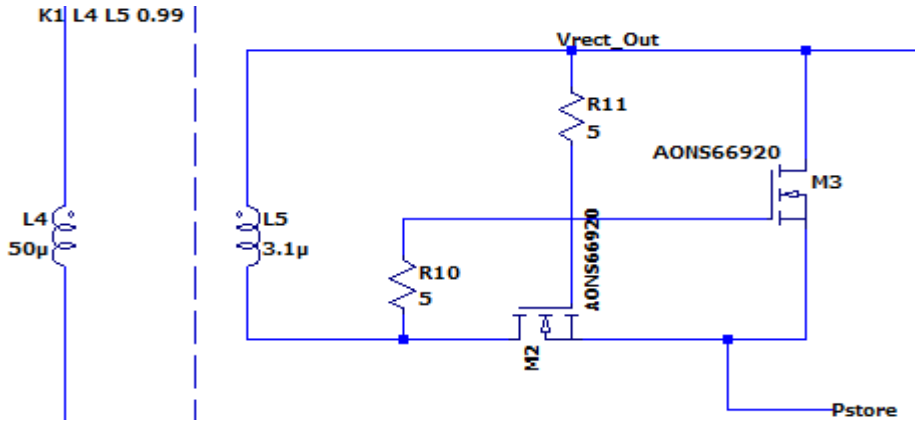

Figure 3. 7: Synchronous Rectifier

In Figure 3. 7 both the FETs are gate connected to their source pins, making it a simple configuration that allows the FET to be gate biased by the same voltage fed into the FET. This is the easier to implement configuration, as it does not call for more complicated biasing and timing circuitry. The two MOSFETs must be driven in a complimentary manner with a small dead time between their conduction intervals to avoid shoot–through. Figure 4. 24 shows the dead times in the simulations.

The way the synchronous rectification is setup, the synchronous FET operates in the third quadrant, this means that the current flows from the source to the drain. During the dead time periods, the inductor current flows through the lower FET's body diode. This body diode usually has a very slow reverse recovery characteristic that can adversely affect the converter's efficiency. An external Schottky diode can be placed in parallel with the low-side FET to shunt the body diode and prevent it from affecting the converter's performance.

In higher currents applications, a number of MOSFETs can be paralleled to handle higher output currents to increase the current carrying capabilities by sharing across the parallel combination of the FET's. Because the effective RDSON in this case is inversely proportional to the number of paralleled devices, conduction losses are reduced. Also, the RDSON has a positive temperature coefficient so the FETs will automatically tend to share current equally, facilitating optimal thermal distribution among the SR devices. This increases the capabilities to transfer heat from the components and the PCB which then directly improves the thermal performance of the converter.

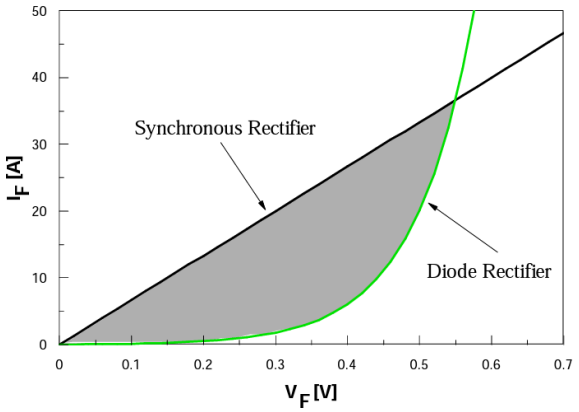

Figure 3. 8: Synchronous Rectifier Curve [Chapter 2 Document]

3.8.1.5. Output Stage

3.8.1.5.1. Output Voltage Programming

The controller has an internal error amplifier that generates a 1.25V as a reference to compare with the feedback voltage to be able to regulate the output voltage Vout to a constant pre-set voltage. With the configuration in the simulation circuit, the voltage to the voltage divider is in the order of 3.8V-4V. below is the calculation of the voltage fed into the output voltage divider configuration.

3.8V added with the voltage breakdown made up of the three zener diodes of 6.2V and 2 x 20V sums up to 50V output.

$$V_{OUT} = V_{Ref}\left(\frac{R_B}{R_T + R_B}\right) \qquad 3.\ 12$$

$$= 3.8\ \left(\frac{10x10^3}{19x10^3 + 10x10^3}\right)$$

$$= 1.31V$$

3.8.1.5.2. Switching frequency programming

The switching frequency for the LT3753 is programmed using a resistor, RT/R13, connected from analogue ground. The value of the resistor is calculated as follows.

$$R_t = 8.39\ x\ \frac{10^9}{f_{osc}}\ x\ \left(1 + \frac{(f_{osc} - 300x10^3)}{10^7}\right) \qquad 3.\ 13$$

$$R_t = 8.39\ x\ \frac{10^9}{500x10^3}\ x\ \left(1 + \frac{(500x10^3 - 300x10^3)}{10^7}\right)$$

$$= 13.992k\Omega$$

$$= 14k\Omega\ \ Selected$$

The table below is of pre-calculated values from the datasheet.

SWITCHING FREQUENCY (kHz)	R_T (kΩ)
100	82.5
150	53.6
200	39.2
250	30.9
300	24.9
350	21
400	18.2
450	15.8
500	14

Table 3. 1: Switching Frequency

$$C_{outBank} = \frac{T_{Longest\ Pulse} * I_{Max\ Pulse}}{V_{Max\ Droop}} \qquad 3.\ 14$$

$$= \frac{110x10^{-6} * 80}{500x10^{-3}}$$

$$= 17.6mF$$

3.8.1.5.3. Output

The output of the hold-up module is regulated through a synchronous rectifier built up of mosfet instead of a diode rectifier. Because the mosfets are actively controlled, it makes the design more efficient. The Mosfets have a low Rds_{on}, they act as resistors switched on and off in line with the circuit making them efficient compared to the use of diodes.

Each FET's gate is connected to the drain pin of the other FET, making it a simple configuration that allows the FET to be gate biased by the same voltage fed into the drain of the other FET. This is the easier to implement configuration, as it does not call for more complicated biasing and timing circuitry.

With the synchronous rectifier in place and the bulk energy not transferred through the transformer, the heat generated by the main switching FET (M1 in the circuit) as a sum of the switching and conduction losses drop drastically making the hold-up module more efficient.

3.8.2. Hold-Up Module Efficiency Analysis

The efficiency of the power hold-up module is defined by the power efficiency formula:

$$\eta = \frac{P_{OUT}}{P_{IN}} \qquad 3.\ 15$$

Where:

n is the efficiency

Pout is the average output power

PIN is the average input power

The detailed power efficiency analysis is done in 3.4.1.7 under efficiency.

3.8.3. Controller Description and configuration

The LT3753 controller is a current mode Pulse Width Modulator controller optimized for an active clamp forward converter topology, this controller allows up to 100V input operation. A programmable volt-second clamp allows primary switch duty cycles above 50% for high frequency switching configuration. The active clamp control feature reduces switch voltage stress and increases efficiency. A synchronous output is available for controlling secondary side synchronous rectification.

The controller comes with features such as short-circuit overcurrent protection, programmable soft-start and stop function, programmable switching frequency, programmable over voltage lockout and under voltage lockout as well as synchronizable to an external clock. The switch mode controller has built in accurate programmable volt-second clamp. When set above the natural duty cycle of the converter, it provides a duty cycle guardrail to limit primary switch reset voltage and prevent transformer saturation during load transients.

3.9. SMPS Evaluation and Design Conclusion

The analysis and design presented in this chapter confirm the feasibility of integrating an SMPS into the power hold-up module, yielding significant efficiency gains and a substantial reduction in HUM size. The chosen DC-DC converter incorporates features that enhance overall system performance.

Chapter 4

Simulations

4.1. Schematic simulation

The simulations of this proposed configuration is done using a simulation software LTspice. Using LTspice helps verify the calculated figures against the requirements specifications. With this tool it is possible to produce a relatively close representation of the input voltage, current with their ripple factors, the output voltages and currents along with their respective ripple factors, the capacitor charging current and the output voltage droop permitted in the design. Schematic simulated in Appendix 6.

Fundamental Parameter of the simulation

- Input Voltage: 48VDC
- Output Voltage: 50VDC
- PRF: 1.36kHz
- Duty Cycle: 15%

4.1.1. Pulse Repetition Frequency of 1.36kHz

Pulse Repetition Frequency refers to the number of pulses transmitted by the radar per unit time. PRF is one of the fundamental parameters of a radar and plays a very crucial role in determining the attributes and performance of the radar. This section details the simulations of the HUM at 1.36kHz PRF.

$$T = \frac{1}{f} \qquad 4.1$$

$$= \frac{1}{1.36x10^3}$$

$$= 735.29us$$

$$t_{on} = T\ x\ DC \qquad 4.2$$

$$= 735.29us\ x\ 15\%$$

$$= 110.29us$$

$$t_{off} = T - t_{on} \qquad 4.3$$

$$= 735.29us - 110.29us$$

$$= 625us$$

4.1.2. Start-up

Initially the charging current is set to current limit at a specific value which in this case is 2 amps. The capacitors will charge at this constant current until the voltage reaches 48V, then the MOSFET is driven hard allowing the operational current of about 15A to be drawn. With the selected MOSFET FQPF47P06, the gate-to-source voltage (Vgs) is negative when the gate voltage is below the source voltage. The MOSFET has a minimum voltage necessary to trigger the MOSFET, referred to as the threshold voltage. The drain-to-source voltage (V_{th}) by defined by the following formula:

$$V_{ds} = V_{gs} - V_{th} \qquad 4.4$$

For FQPF47P06 that is used for input inrush current, the threshold voltage is typically in the range of -2 to -4 volts.

4.1.3. Current limit Control

Figure 4. 4 (Red trace) is the inrush current control which is initially driven at about -5V to allow about 4.5A (4.5A set to reduce simulation run time during initial charging of the capacitors). Looking from top to bottom plot planes, below are the descriptions:

First Plot Plane (Top Plot Plane):

V(n017) – is the output of a resistor divider derived from Vin

V(vref) – is the reference voltage generated as part of the peripherals.

V(input_OK) – is the output of the comparator for input power good indication

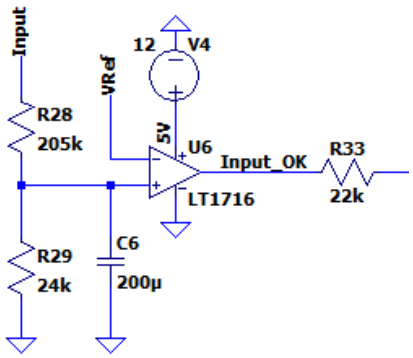

Figure 4. 1: Simulation - Input Power OK

Second From Top Plot Plane:

V(vref) – is the reference voltage generated as part of the peripherals.

V(input_OK) – is the output of the comparator for input power good indication fed from fist plot plane output as input to the second comparator.

V(5vdc_ok) – is the output of the comparator for 5vdc power ok.

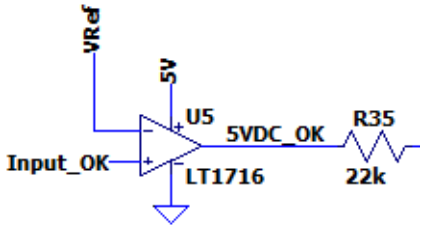

Figure 4. 2: Simulation - 5vdc ok

Third Plot Plane:

V(n025) – is the output of a resistor divider derived from the drain voltage of the current limiting FET.

V(n023) – is the reference voltage

V(50_reg_ok) – is the output of the comparator for 50vdc ok.

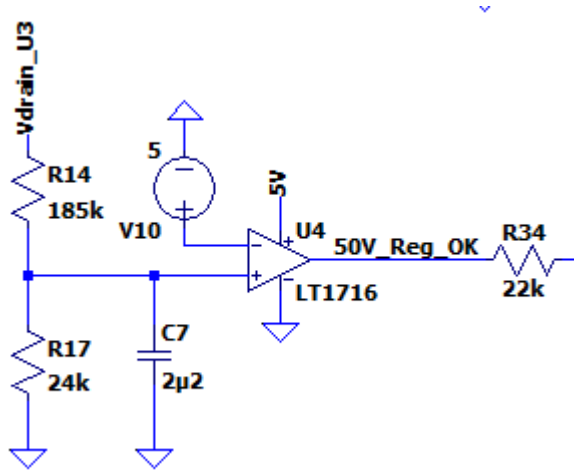

Figure 4. 3: Simulation - 50vdc ok

Fourth Plot Plane:

V(Vgate_U3, Vsource_U3) – is the gate to source voltage of the current limiting FET.

Firth Plot Plane:

I(R12) – is the input current od the HUM.

Bottom Plot Plane:

V(out) – is the output voltage of the HUM.

V(vdrain_u3) – is the drain voltage of the current limiting FET.

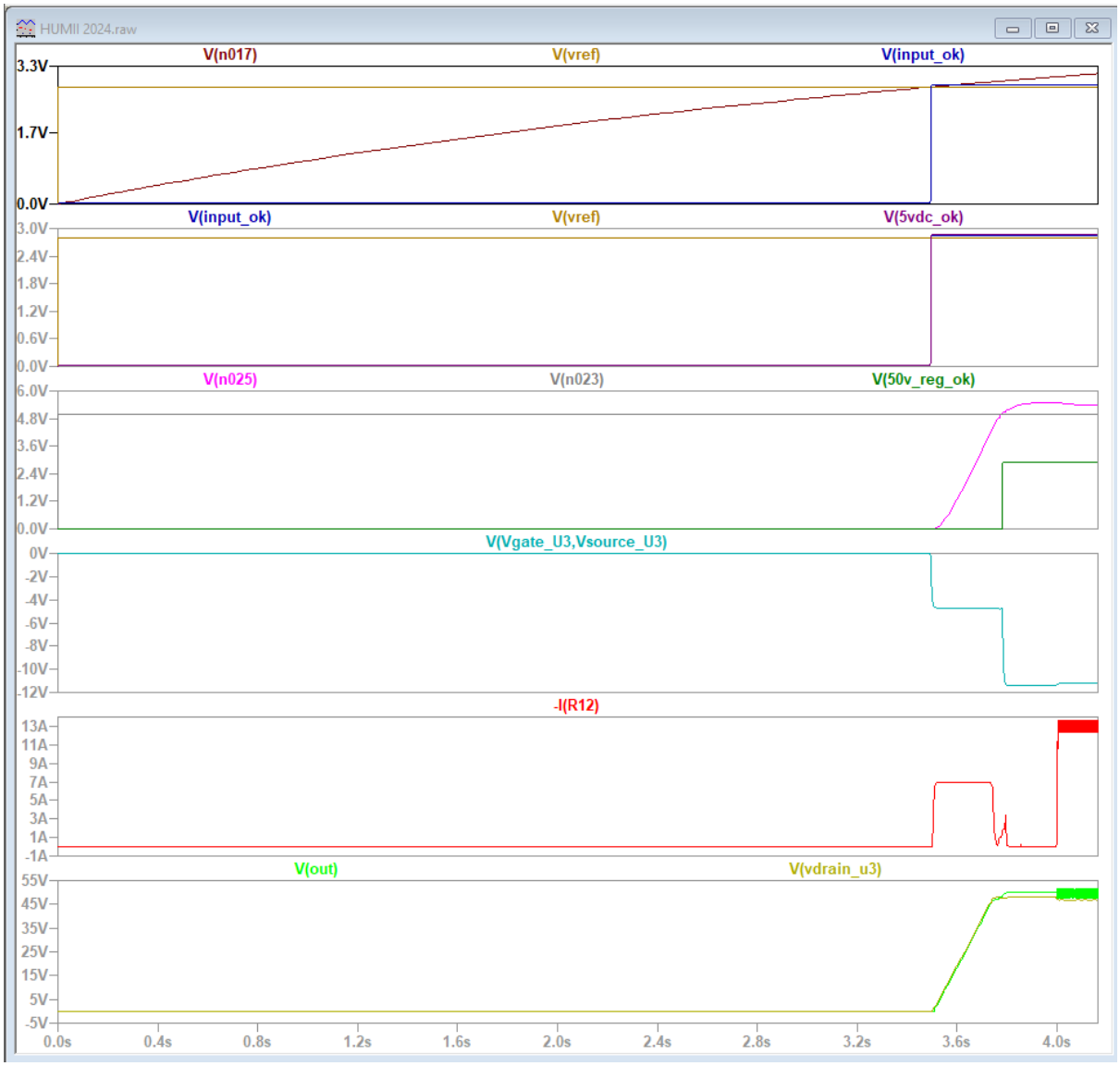

Figure 4. 4: Simulation - HUM Power Conditioning and control

4.1.4. Concept of Operation of the Current limit switch over

Looking at the plot presented in Figure 4. 4 above, it is seen that the HUM does not start the first stage of current limiting until the "input_ok" circuit shown in Figure 4. 1 is high. This rail being HIGH means that the input voltage is within the HUM's operating specifications. This HIGH is then fed into another comparator as an input along with a reference voltage which enables the current limiting by introducing a path to ground for the resistor divider setting up the gate to source voltage, the configuration is shown in Figure 4. 2.

Once the drain voltage of the current limiting FET reaches about 45VDC, the output of comparator shown in Figure 4. 3 triggers the second stage of the current liming which introduces a different resistor combination setting the gate to source voltage of the current limiting FET to about -10VDC. Figure 4. 4 above graphically shows the sequence of events from top to bottom.

4.1.5. Input current Ripple

Input ripple current basically refers to the oscillation of the current in the input components of the circuit, thus from the source through the filter components being the inductors and capacitors. Ripple current in a capacitor in this context refers to the alternating current component that flows through the capacitor. As indicated in the full datasheet of the selected capacitors, extract shown in Appendix 2 the rated ripple current is 5.2A. Figure 4. 5 below shows the measured current ripple at about 1.42A (IR31 – Red Trace) which is well within the range of the selected capacitors and influenced by the capacitance of the primary bank.

Figure 4. 6 below is the current experienced by C29 and due to the first order inductor, The delta between the capacitor rated current ripple and the simulated current ripple means that the capacitor will operate without being stressed and maintain proper operation and reliability.

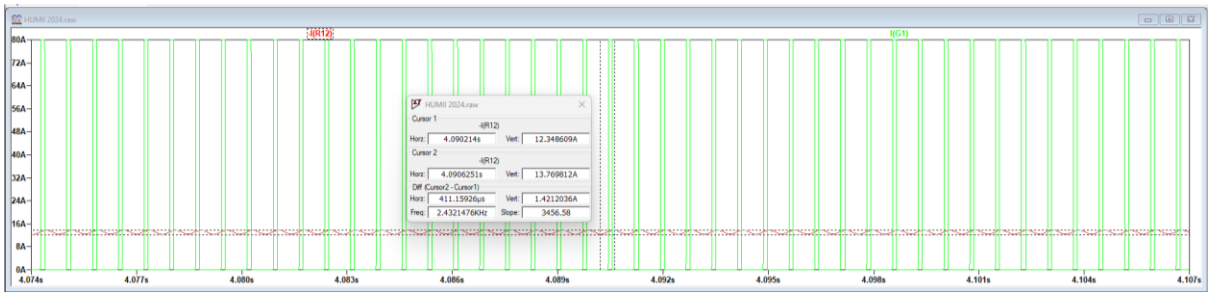

Figure 4. 5: Input Current with Transmit pulse

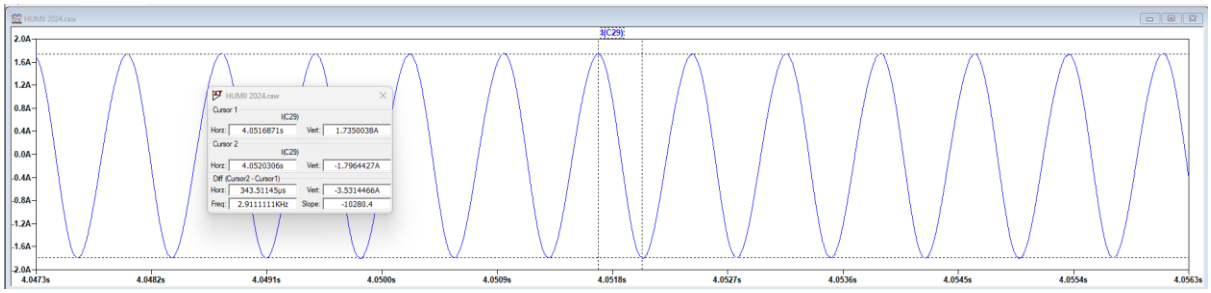

Figure 4. 6: Input Filter Capacitor Current Ripple

4.1.6. Power Losses

During the start-up process, the current limiting MOSFET experiences a fair amount of heat. The mathematical expressions are shown in section 3.8.1.4.

Figure 4. 7 *Traces*

- Top Plot
    - Synchronous rectifier M2
    - Synchronous rectifier M3
- Middle Plot
    - Main Switching FET M1
    - Active Clamp M4
- Bottom Plot
    - Current Limiting FET U3

Figure 4. 7: Input Power Losses

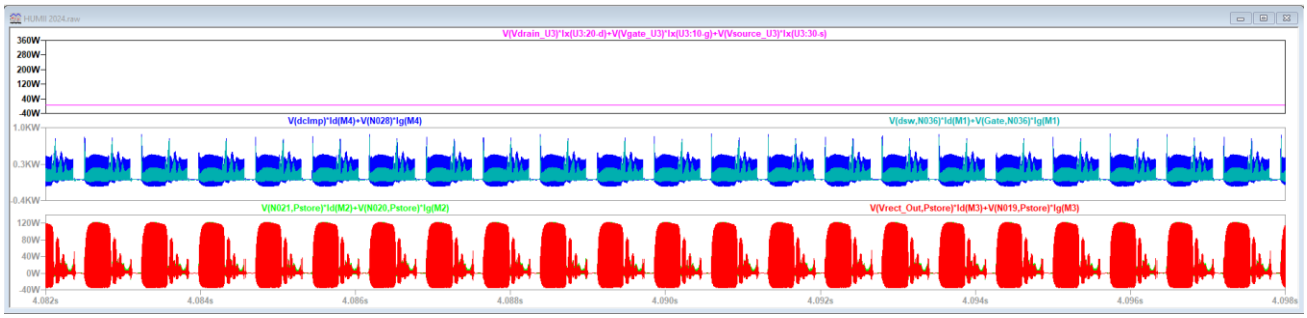

Figure 4. 8: Input Power Losses (Zoom in)

4.1.7. Steady State

In this state, the voltages and currents have stabilised. The HUM is at its state of equilibrium, maintaining an output voltage of 50VDC at the output bank from pulse to pulse. In steady-state, the input current is at an average in the order of 13A as seen in Figure 4. 10. Figure 4. 9 below shows the input voltage, feedback voltage (V_{OUT} program), Hum t xen voltage, output inductor current, input current and output voltage.

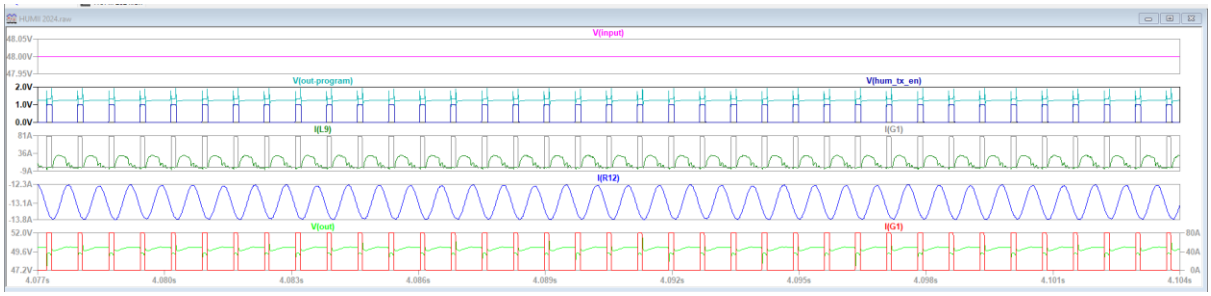

Figure 4. 9: Steady state wave forms

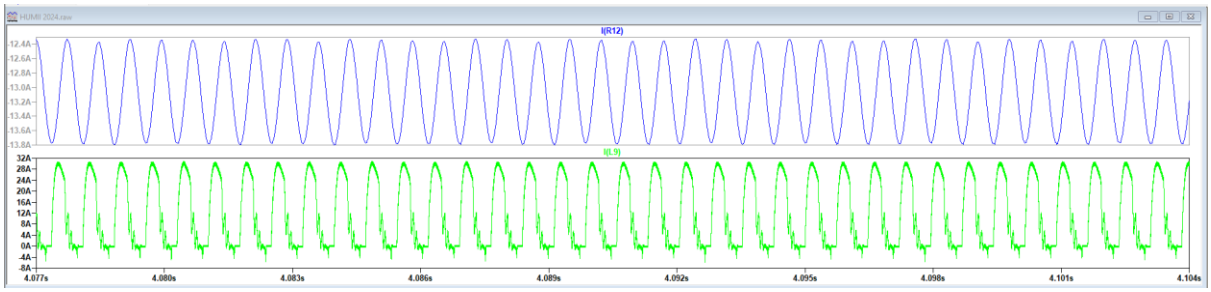

Figure 4. 10: Input and Output Current

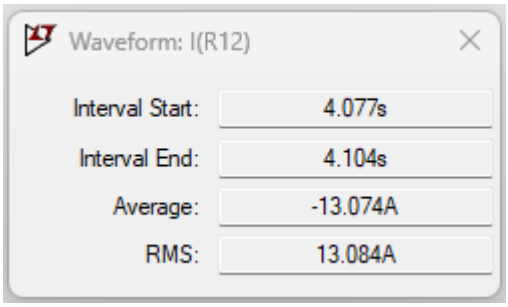

Figure 4. 11:Input Average current Consumption

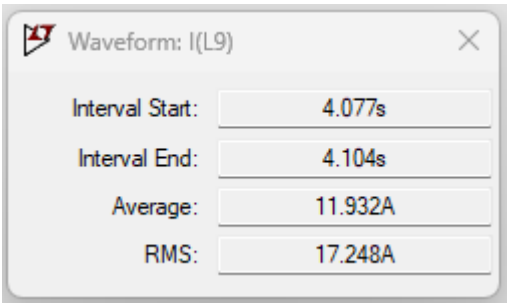

Figure 4. 12: Output Average Current Consumption

Figure 4. 11 and Figure 4. 12 above are the average current consumptions at steady state operation. Input at about 13A and output at about 11.93A.

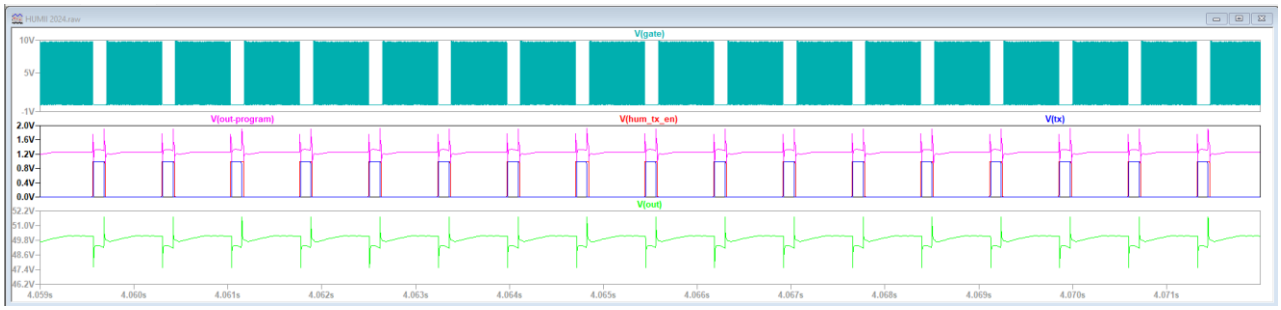

Figure 4. 13: Controller gate output, output voltage with transit pulse

Figure 4. 13 above shows the switching pulses of the controller gate along with the output voltage with its droop voltage along with the HUM tx enable and HUM tx. As explained in the concept of operation, the controller (Blue trace) must stop switching before the pulse starts and start switching again charging the capacitors bank.

4.1.8. Voltage Droop

Voltage droop is the pre-determined value that the output voltage can drop during the pulse. Figure 4. 14 shows the voltage droop at about 445.42mV from pulse to pulse while maintaining the 50VDC output before each pulse flatness.

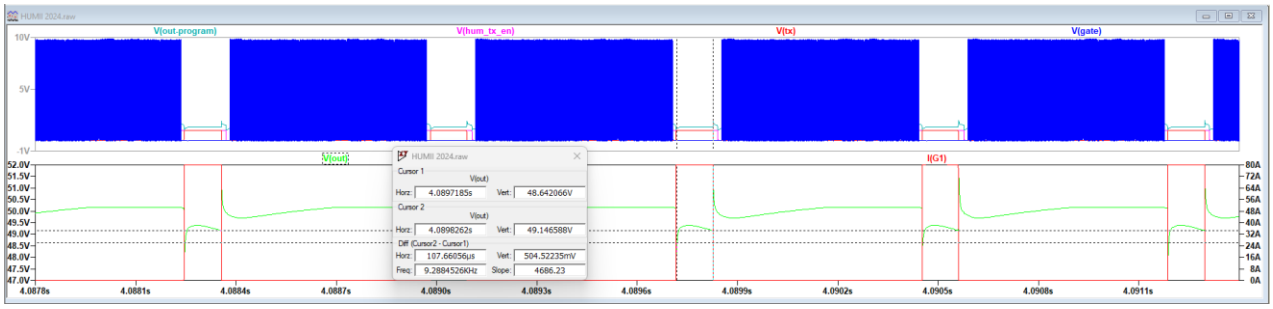

Figure 4. 14: Output Voltage Droop

4.1.9. Active Clamping MOSFET Voltage

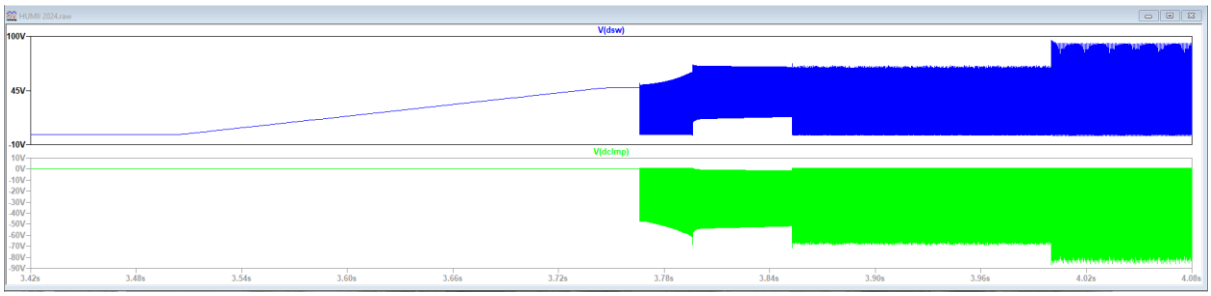

Figure 4. 15: Active Voltage Clamping and Main Switching MOSFET Voltages

Figure 4. 15 above shows the voltage of the main switching FET (M1) in blue trace and the green trace indicates the active clamp voltage (M4). The main switching FET (M4) with a maximum of about 90V and the active clamping voltage at about -80V suppressing voltage spike well below 100VDC. This is achieved by the A_{OUT} pin of the LT3753 forward controller.

4.1.10.HUM Ready and HUM Tx Enable Configuration

As discussed in the previous chapters, the SMPS must be switched off before every pulse to ensure that the switching does not crip into the pulse. This section will show how the two pulses that controls the SMPS.

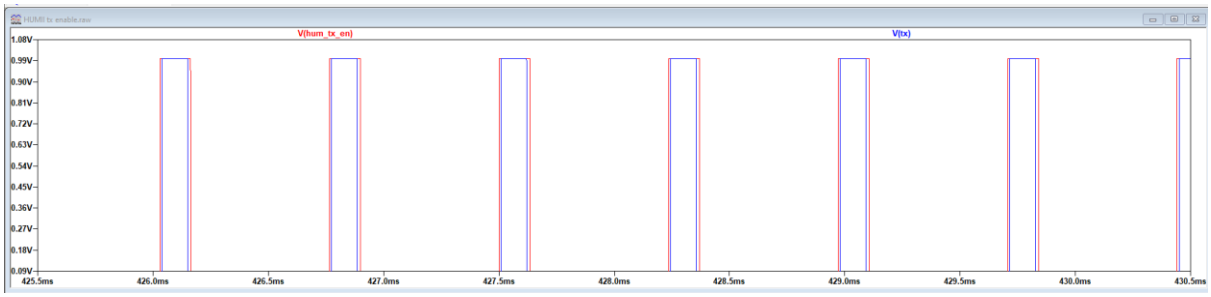

Figure 4. 16: HUM Ready and Tx

In Figure 4. 16 above, it is seen that the HUM enables which is the red trace goes HIGH first and then the transmit pulse which is the blue trace follows. The transit pulse goes HIGH and LOW inside the HUM enable pulse. The HUM enable pulse forces the SMPS to switch OFF by inducing a 1.25VDC into the feedback line of the forward controller. This ensures that the feedback that tells the forward controller that the output voltage is at 50VDC stays high throughout the transmit pulse.

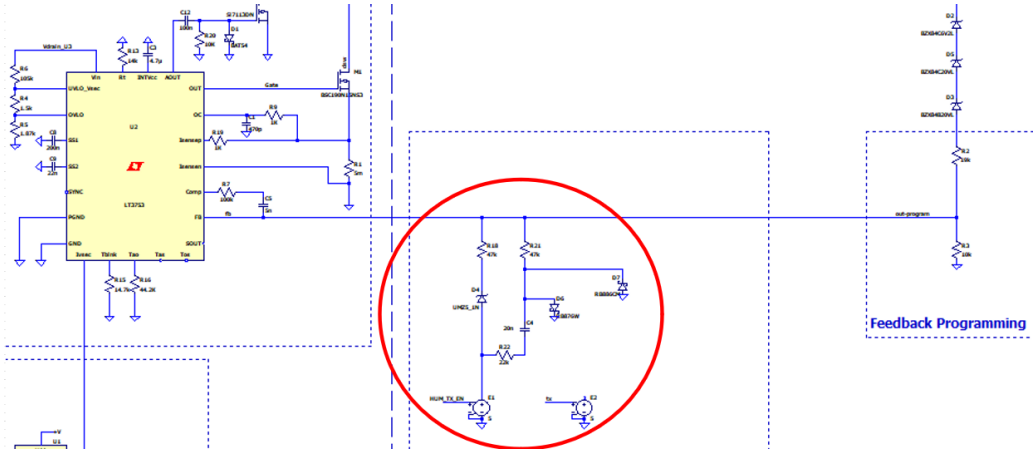

Figure 4. 17: HUM Ready Simulation circuit

4.1.11.Power Losses

After the initial charging of both the primary and the secondary store, the hold-up module goes into steady state mode. This means that it maintains the power consumption, thus maintaining 50VDC at about 11.93A Max peak current. Figure 4. 18 below shows the power consumption during this steady state operation. Green trace being the current limiting FET (U3), Grey trace the main switching FET (M1), Magenta trace being the active clamping FET (M4), Red (M2) and Cyan (M3) traces the synchronous rectifier FETs.

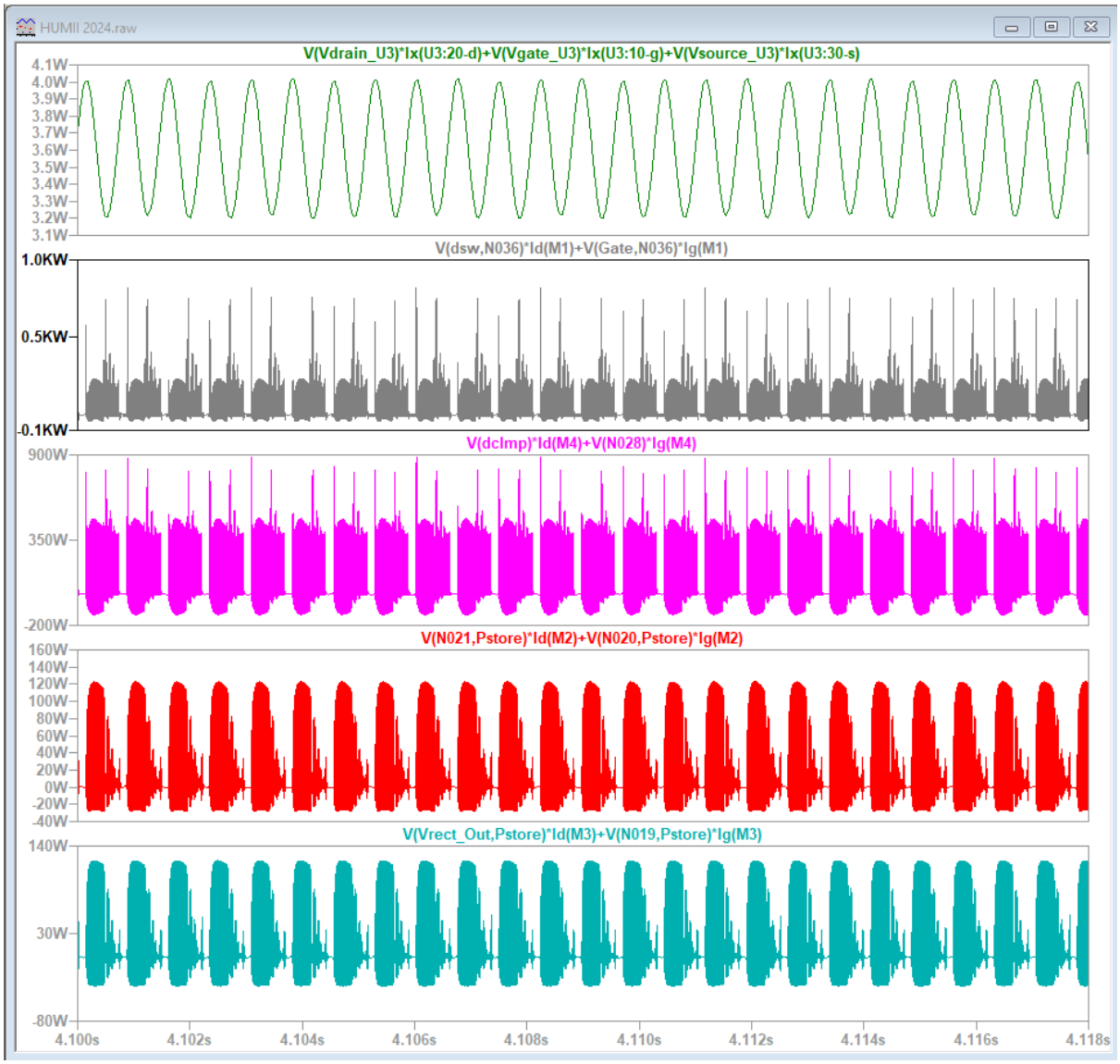

Figure 4. 18: Switching MOSFETs Power Dissipated in Steady-State

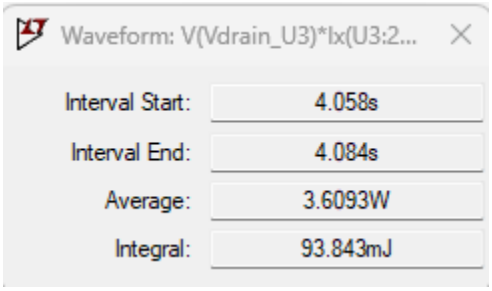

Figure 4. 19: U3 Power Losses

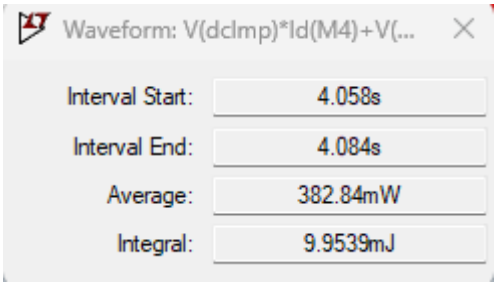

Figure 4. 20: M4 Power Losses

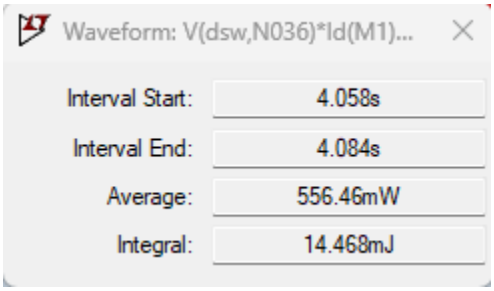

Figure 4. 21: M1 Power Losses

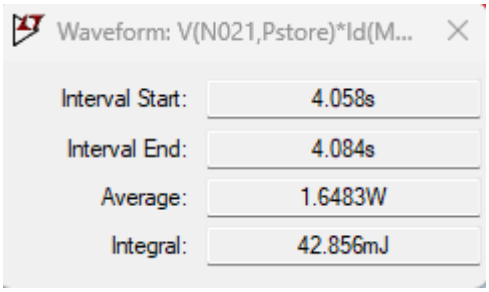

Figure 4. 22: M2 Power Losses

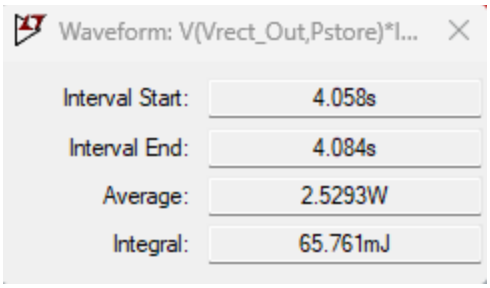

Figure 4. 23: M3 Power Losses

Figure 4. 19, Figure 4. 20, Figure 4. 21, Figure 4. 22 and Figure 4. 23 are the steady state power dissipation measurements of the MOSFETs, thus U3, M4, M1, M2 and M3 respectively. With the current limiting (U3) having the highest power dissipation of 3.6W and the active clamping FET (M4) with the lowest power dissipation of 382.84mW.

Current limiting MOSFET Power losses are given by

$$P_{losses} = I_D \; x \; R_{DS(on)} \qquad 4.5$$

$$= 11.99^2 \; x \; 21x10^{-3}$$

$$= 3W$$

The synchronous rectifier mosfets's power losses are derived from the following fomulas.

$$P_{Total\ Losses} = P_{cond} + P_{on} + P_{off} \qquad 4.6$$

Where;

$$P_{conduction} = I^2_{D_{RMS}(on)} \; x \; R_{DS(on)} \qquad 4.7$$

$$P_{on} = E_{on} \; x \; F_{sw} \qquad 4.8$$

$$E_{on} = \frac{1}{2} \; x \; I_{DS(on)} \; x \; V_{DD} \; x \; t_{on} \qquad 4.9$$

And

$$P_{off} = E_{off} \; x \; F_{sw} \qquad 4.10$$

$$E_{off} = \frac{1}{2} \; x \; I_{DS(off)} \; x \; V_{DD} \; x \; t_{off} \qquad 4.11$$

4.1.12.Rectification

Rectifier concept of operation

The two rectifier FETs are coupled to the secondary side of the transformer. They are dependent on the secondary voltage as gate driver with no additional FET driver circuitry or controller. The switching timing is controlled by the secondary voltage. The secondary voltage is dependent on the main switching FET M1, when M1 is switching voltage is induced on the secondary winding and rectification process starts.

M2 is on, M3 is off

Voltage corresponding to the winding ratio with the polarity symbol side of the secondary side winding n2 as plus voltage, is applied, current flows through the M2 to the inductor L9 and charges the output energy store.

$$\frac{n_2}{n_1} \, x \, V_{in} \qquad 4.\,12$$

M2 is off, M3 is off

The energy stored in the inductor L9 passes through the M3 body diodes

M2 is off, M3 is on

The energy stored in the L9 passes through the MOSFET part of the M3, and current flows.

M2 is off, M3 is off

The energy stored in the L9 flows through the body diodes of the M2 and M3, causing current to flow.

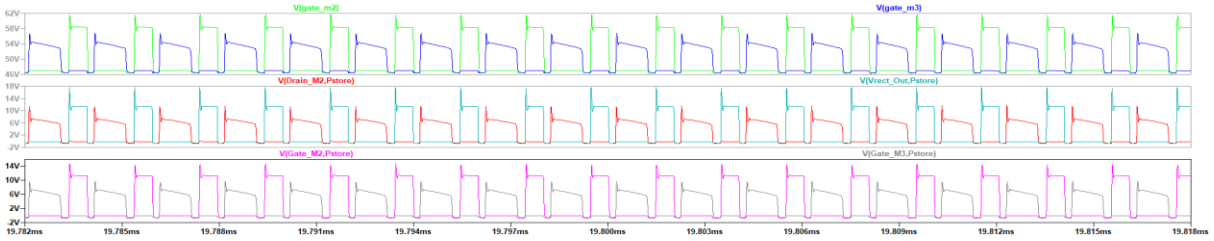

Figure 4. 24: Synchronous Rectifier Timing Graphs

Figure 4. 24 above shows the voltages of the synchronous rectification. The MOSFETs being M2 and M3 that forms part of the rectifier. The switching times are shows as seen in Figure 4. 24 along with the dead time in between the transitioning window. Top plot plane are the gate voltages, Middle plot plane is the drain to source voltages for both m2 and m3, and bottom plot plane are the gate to source voltages. V_{OUT} is made up of +/-48VDC Pstore plus the secondary induced voltage.

$$V_{OUT} = Pstore + (V_{in} \, x \, \frac{n_2}{n_1} \, x \, DC) - Vf \qquad 4.\,13$$

$$= 48 + (48 \, x \, 0.25 \, x \, 0.5) \text{ - } 1$$

$$= 53VDC$$

This is the highest it can go at maximum duty cycle. The calculation is done using maximum duty cycle being 50%. This includes the 0.5VDC-1VDC forward voltage of the MOSFETs rectifiers. The Duty Cycle changes as the controller is always working of optimising the converter by adapting the duty cycle.

4.1.13.Efficiency

The graphs in Figure 4. 25 below is the measure currents and voltage used to calculate the efficiency of the hold-up module. For input power I_{R31} is used with the input voltage 48VDC and for the output power I_{L9} is sued with the output voltage of 50VDC.

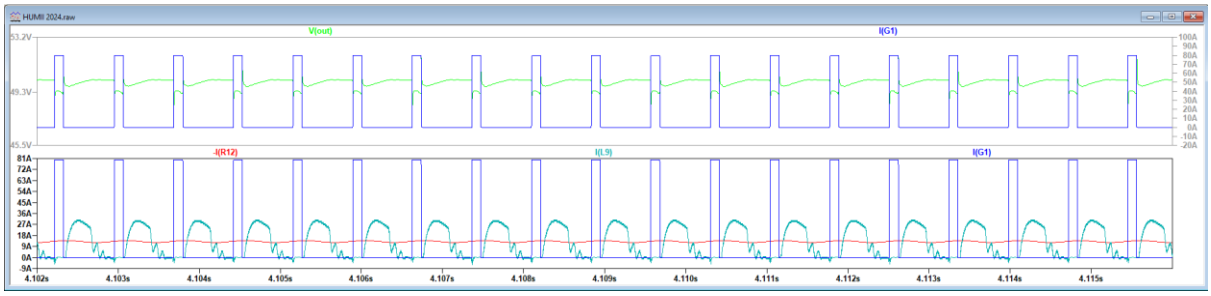

Figure 4. 25: Simulations - Efficiency

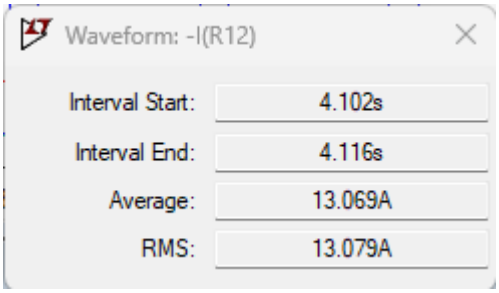

Figure 4. 26: Input Current - Average

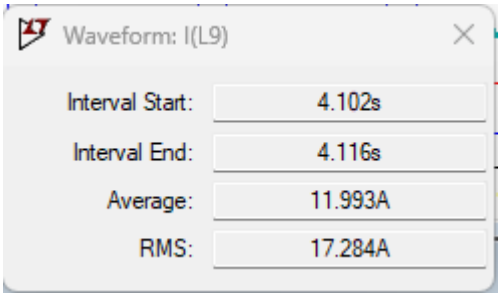

Figure 4. 27: Output Inductor Current - Average

Input Voltage: 48VDC

Output Voltage: 50VDC

$$\eta = \frac{P_{OUT}}{P_{IN}} \qquad 4.\ 14$$

$$P_{OUT} = V_{OUT}\ x\ I_{OUT} \qquad 4.\ 15$$

$$= 50\ x\ 11.993$$

$$= 599.65W$$

$$P_{IN} = V_{IN}\ x\ I_{IN} \qquad 4.\ 16$$

$$= 48\ x\ 13.069$$

$$= 627.312W$$

$$\eta = \frac{P_{OUT}}{P_{IN}} \qquad 4.\ 17$$

$$= \frac{599.65}{627.312}$$

$$= 0.9559\ or\ 95.59\%$$

4.2. Simulation Conclusion

The main objective of the thesis was to investigate the use of a switch mode power supply into the power hold-up module for radio frequency pulsed power amplifier application by introducing a switching controller into the design. One of the main objectives derived from the SMPS introduction was to improve the capability of the hold-up module to handle input power fluctuation while tightly regulating the output voltage, and to improve the efficiency of the power hold-up module, following reducing the physical size of the unit while reducing overall cost. The high-level design, detailed design, calculations and simulations proved the SMPS based power hold-up module to be feasible and within the targeted objectives and benefits.

The initial selection of the DC-DC converter or controller was the LT1952-1, which was evaluated and found to be lacking the active clamping function. The LT1952-1 without the active clamp function resulted in high drain voltage spikes on the primary side of the transformer. The LT3753 selection of an isolated model of a DC-DC power supply with some addition configuration to it proved to have successfully eliminate switching signals or noise into the pulse during the transmit pulse and clamped the voltage spikes well below 100VDC. This can be seen in Figure 4. 13 before the pulse starts, the switching controller completely stops switching and only starts again once the duration of the pulse has been completed. The stability of the output power is successfully demonstrated by observing the flatness of output voltage and the current thus maintaining the energy level in the energy store capacitors and can be seen in Figure 4. 14 V_{OUT} green trace.

The design and simulations of the SMPS based power hold-up module was able to successfully demonstrate reduced the power dissipation by a sound margin. This objective is achieved by introducing a synchronous rectifier which introduces the use of mosfets instead of schottky diodes, this introduction of the FETs reduces the forward voltage and because of the low drain-source on resistance the power dissipation becomes much lower. Figure 4. 19 up to Figure 4. 23 proves the improvements that comes about the FETs with the highest power dissipated being 3.6W and the lowest 382.84mW.

The simulated power hold-up module successfully reduced the size of the unit as the components used are of fairly small physical features.

Chapter 5

Hardware Design

This Chapter will discuss the PCB schematic design using Altium designer and will also outline the PCB layout procedure, as well as, the assembly of the PCB.

5.1. Schematic Design

The schematic design is developed from the simulation circuit diagram. The schematic design is a more detailed and evolved circuit design, taking into account all components required to make the simulated circuit work in the real world. This includes the additional design of DC regulator that will take care of the housekeeping voltage supplies, reference voltages and control voltages. Figure 5. 1, Figure 5. 2, Figure 5. 3, Figure 5. 4, Figure 5. 5 and Figure 5. 6 are the complete schematic of the HUM.

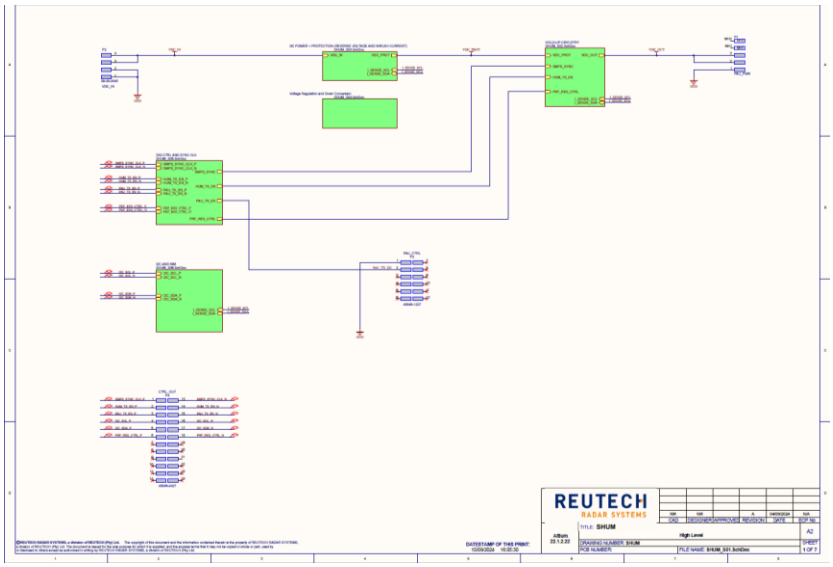

Figure 5. 1: Schematic - High Level Block Diagram

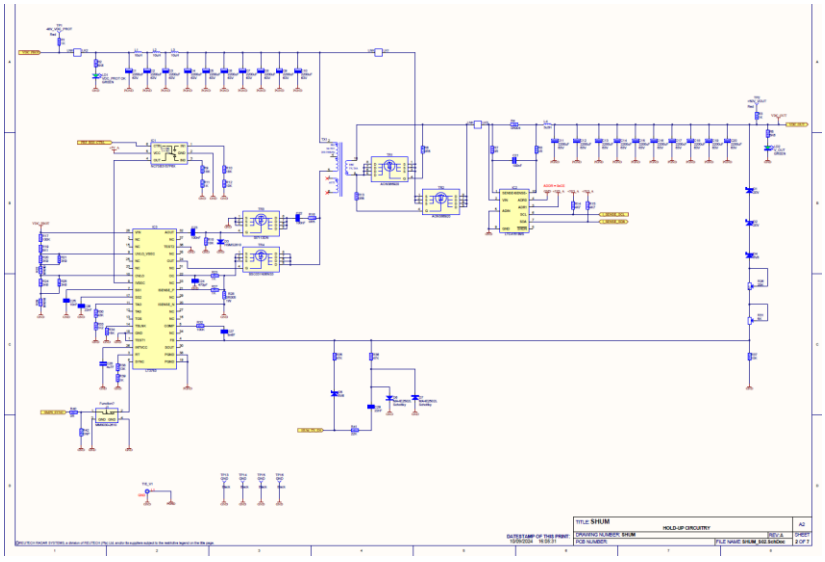

Figure 5. 2: Schematic - Hold-Up Circuitry

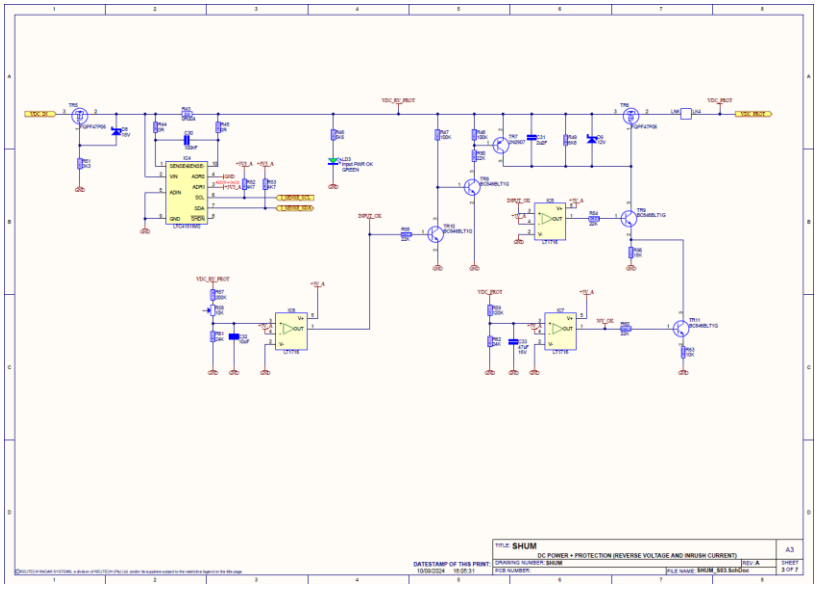

Figure 5. 3: Schematic - Reverse Voltage protection & Inrush Current Control

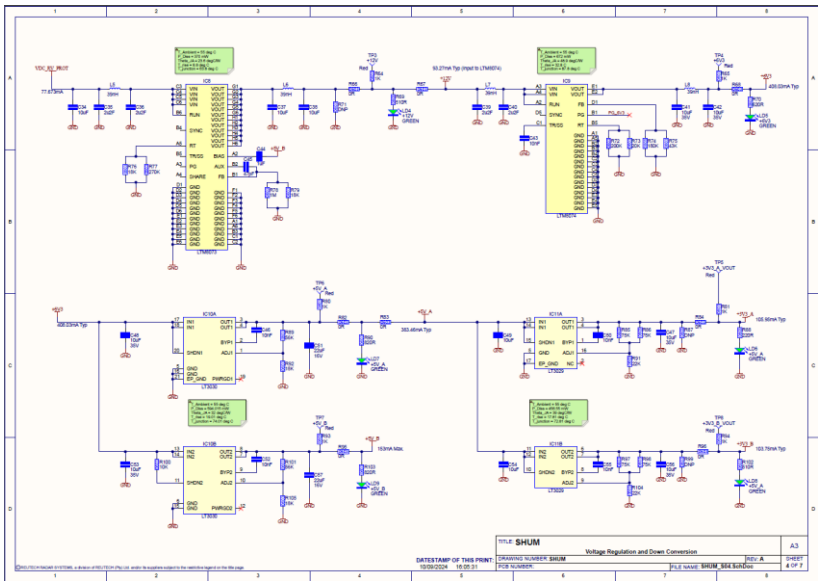

Figure 5. 4: Schematic - Voltage Regulation and Down Conversion (Peripherals)

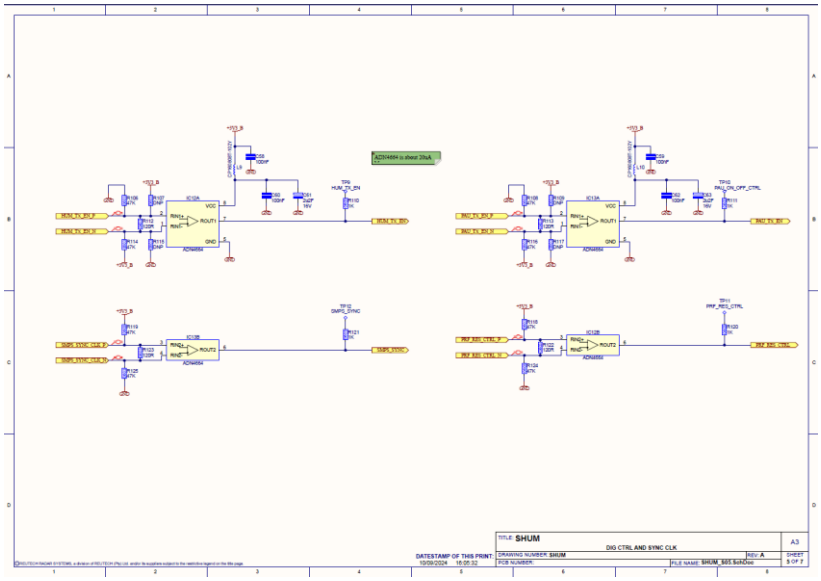

Figure 5. 5: Schematic - Dig Ctrl and Sync CLK

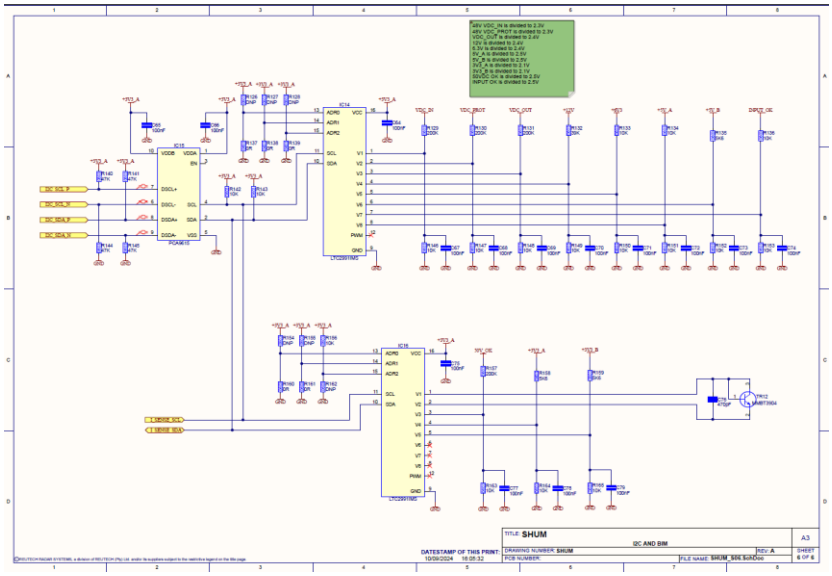

Figure 5. 6: Schematic - I2C and Built in Monitoring

5.2. PCB Layout and Routing

PCB layout, using Altium designer software is the next step of the PCB design. This section documents the PCB layout procedure, including the provisional layout, routing and manufacture.

5.2.1. Layout

Figure 5. 7 and Figure 5. 8 are the components layout of the HUM Top layer and Bottom later respectively. This is the first step in the PCB artwork.

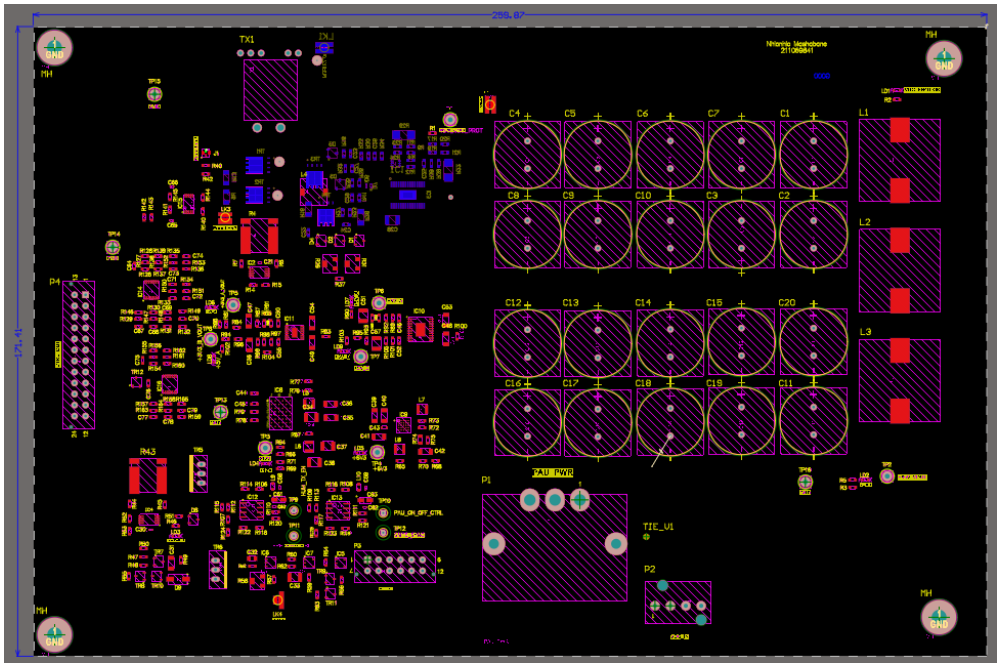

Figure 5. 7: PCB Layout - Top

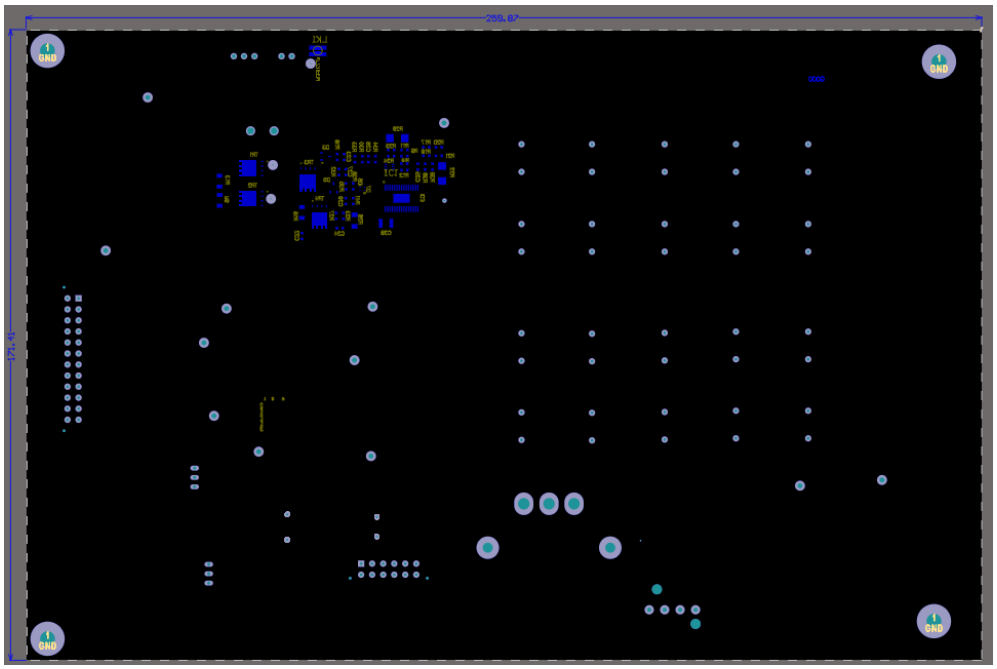

Figure 5. 8: PCB Layout - Bottom

5.2.2. Layout 3D

Figure 5. 9 and Figure 5. 10 presents the 3D view of the components placement, top layer and bottom layer respectively. All the ICs used it the design of the HUM including the peripheral voltages have a recommended placement configuration from their manufacturers, that recommendation is followed as close as possible in this design.

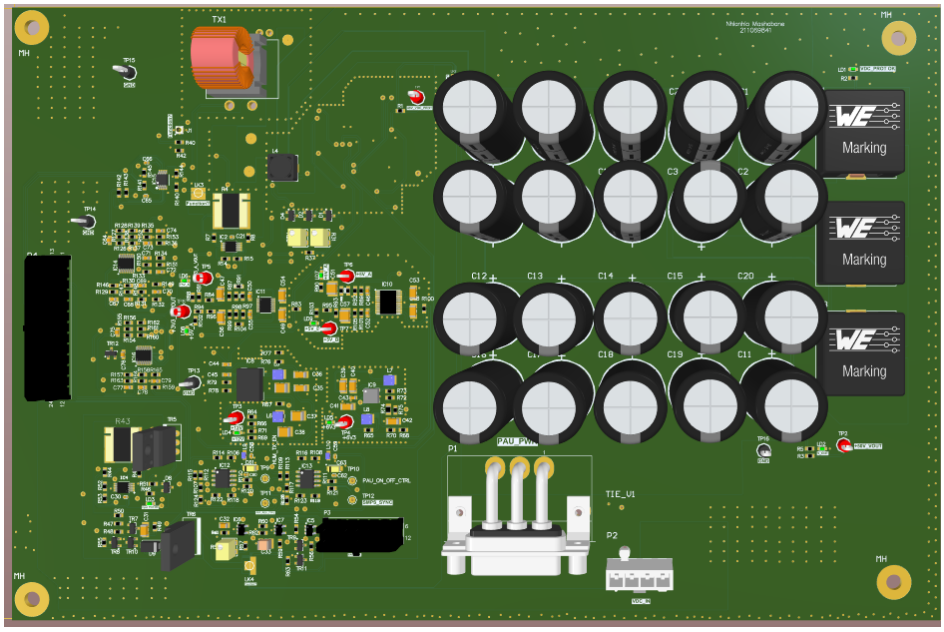

Figure 5. 9: PCB Layout - 3D Top View

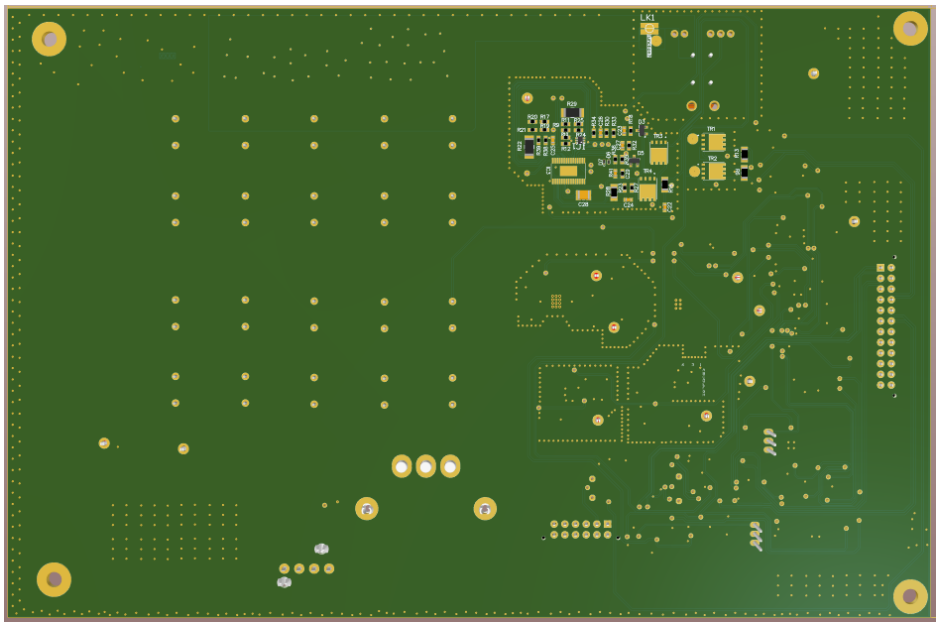

Figure 5. 10: PCB Layout - 3D Bottom

5.2.3. Routing

Figure 5. 11 and Figure 5. 12 shows the routing of the PCB, both top and bottom layers respectively. The tracks characteristics are determined by the type of signal flowing through. Thin track, vias and polygons are utilised to achieve the routing.

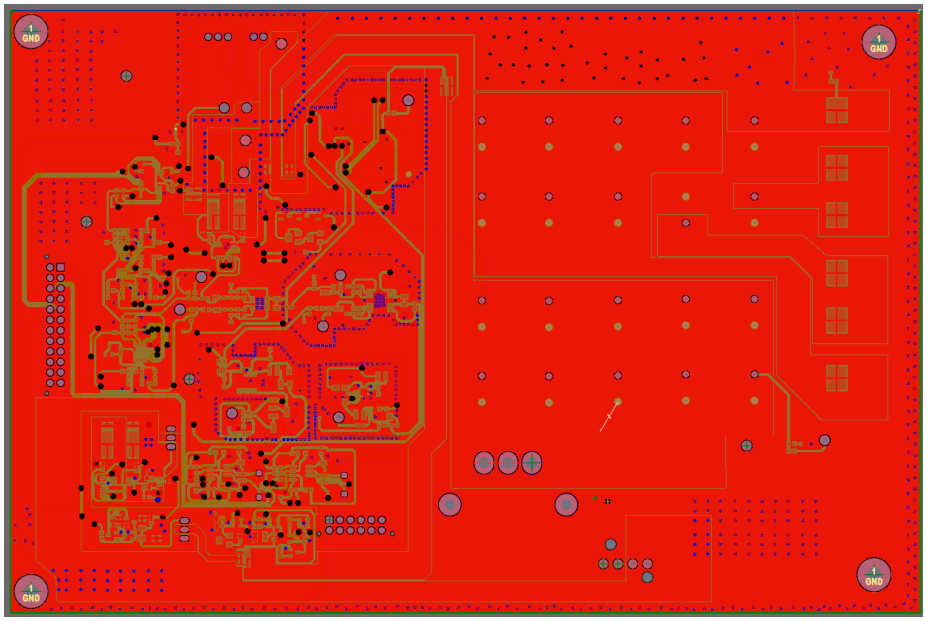

Figure 5. 11: PCB Routing - Top Layer

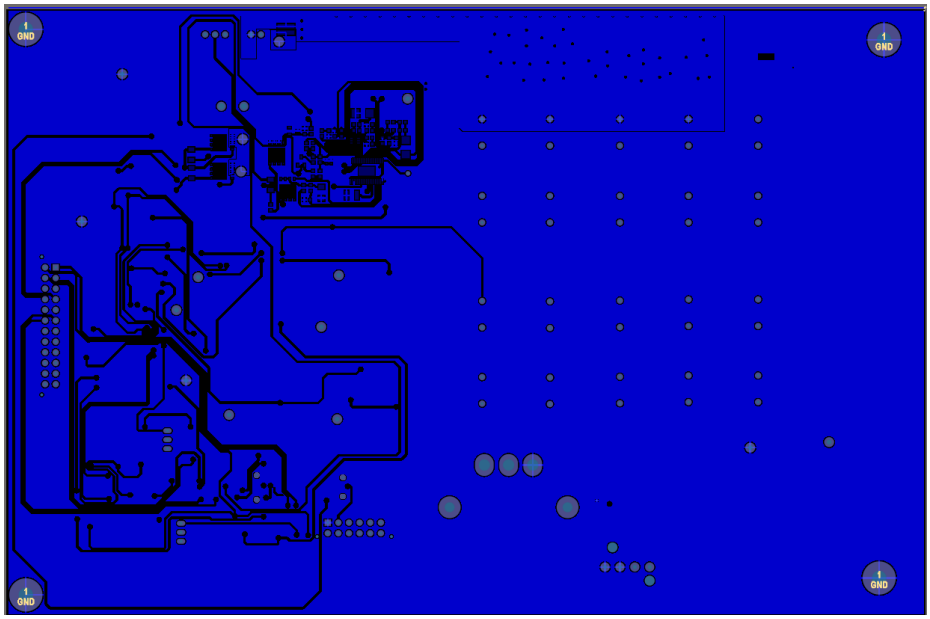

Figure 5. 12: PCB Routing - Bottom Layer

5.2.4. PCB Manufacturing

Using Altium designer, a datapack is generated and sent out to PCB manufactures for PCB manufacturing. For the prototype of the HUM the datapack was sent to JLCPCB, a Chinese manufacturing company. The manufactured PCBs can be seen Figure 5. 13 and Figure 5. 14 are the top and bottom view of the bare board.

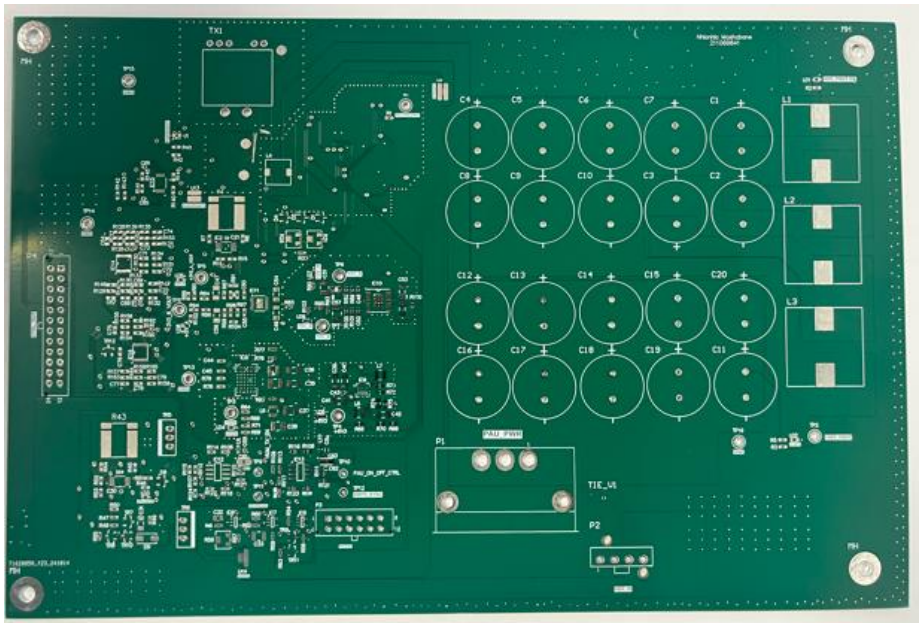

Figure 5. 13: Manufactured PCB - Bare Top

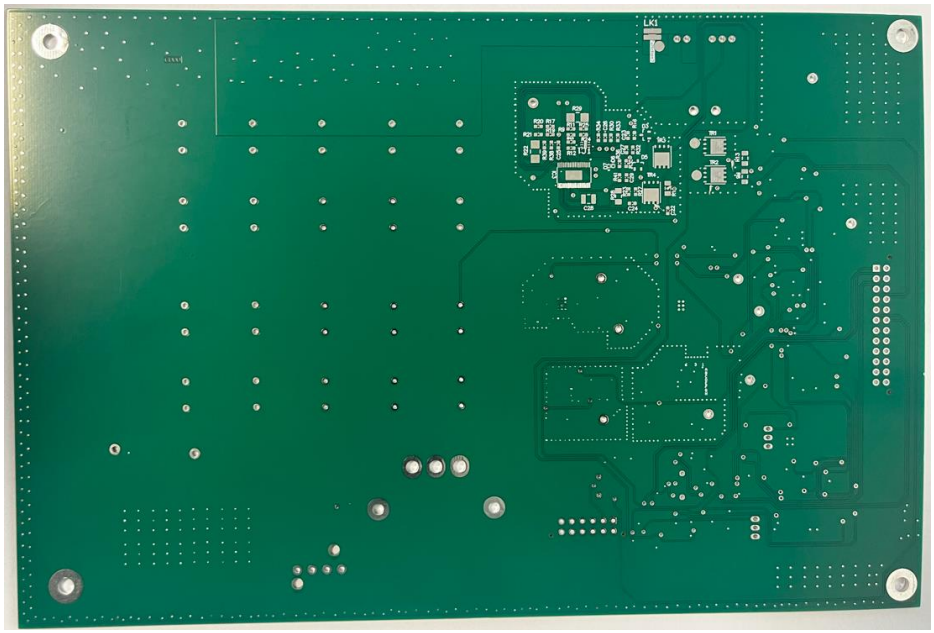

Figure 5. 14: Manufactured PCB - Bare Bottom

5.2.5. PCB Assembly

Figure 5. 15 and Figure 5. 16 presents the assembly drawing of the HUM, both top and bottom layer. This is used to populate and solder the components on the PCB.

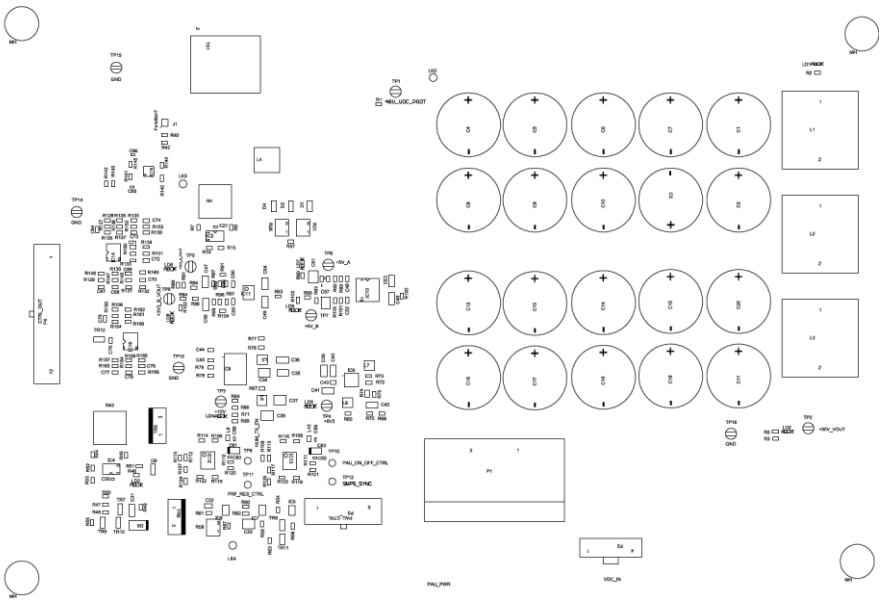

Figure 5. 15: PCB Assembly Drawing - Top

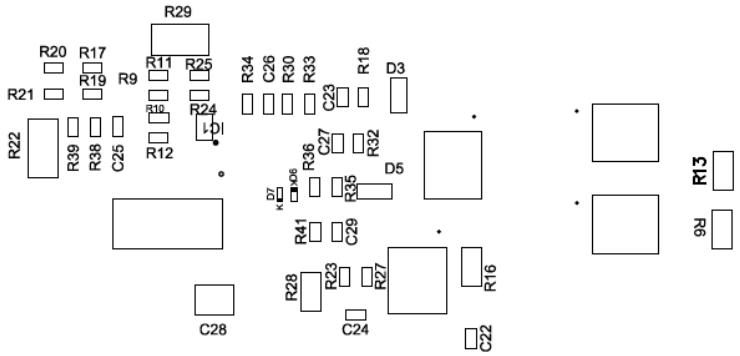

Figure 5. 16: PCB Assembly Drawing – Bottom

Figure 5. 17 and Figure 5. 18 show the PCB fully assembled. At this stage testing was already in progress hence the modification with wires on the board.

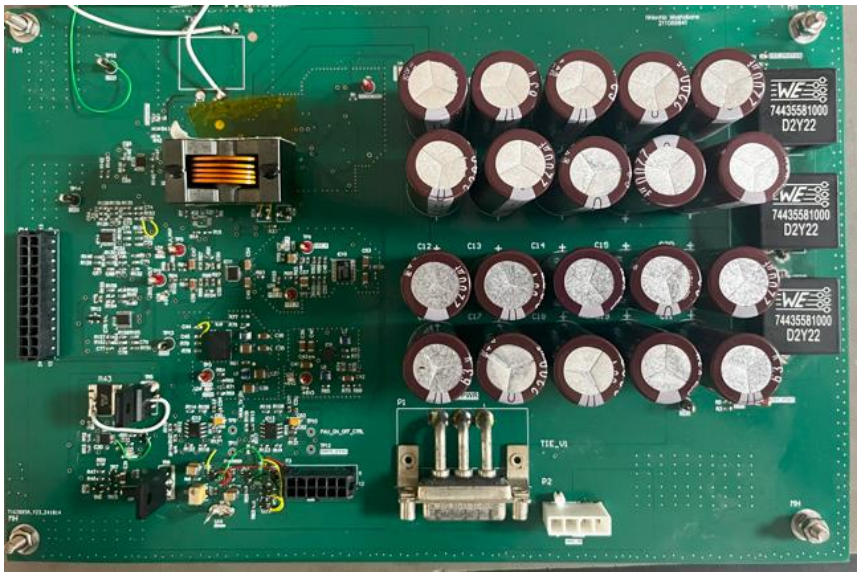

Figure 5. 17: Assembled PCB - Top

The bottom section shown in **Error! Reference source not found.** is the forward controller.

Figure 5. 18: Assembled PCB - Bottom

5.3. Experimental Evaluation

This chapter aim to answer the research questions, thus weather or not the goals have been achieved or not and why if they are not achieved. The answers to the research questions will be based on the simulated results as well as the measurements from the prototype. The research questions are as follows:

- How effective is using a Switch-mode based power supply in pulsed RF power Amplifiers?
    - An SMPS must be integrated with a linear regulator to top up 2VDC.
    - The configuration must maintain the output voltage of 50VDC.
- How efficient is using a Switch-mode based power supply in pulsed RF power Amplifiers?
    - The efficiency of the SMPS must be better than using a complete linear regulator-based system.
- Is the proposed configuration an optimal solution (the use of SMPS based HUM)?
    - The integration must allow an input voltage fluctuation while maintaining the output voltage.
    - The integrated unit must generate less heat.
- Is a forward converter the best solution?
    - The forward converter must introduce small size components.
- What technology can be used to nullify the switching noise of the SMPS circuitry?
    - The SMPS must be controlled - switched ON and OFF precisely.
- What are the overall benefits of SMPS over Linear controllers or analogue controllers?

5.3.1. Procedure

The SMPS based Hold-Up module discussed in this study is fed with an input of 48VDC and it has an integrated SMPS that regulates the delta from input to output voltage which in this case is 50VDC. The system must be capable of handling input voltage fluctuation while maintaining a tightly regulated output voltage.

A summarized test procedure is to inject an input voltage of 48VDC and measure a stable and well-regulated 50VDC. The HUM is to be loaded with a pulsed load drawing 80A peak with an average of about 12A. The significance of this study is to answer the question of integrating a linear regulator and a SMPS with full control of the SMPS.

5.3.2. Input vs Output Voltage

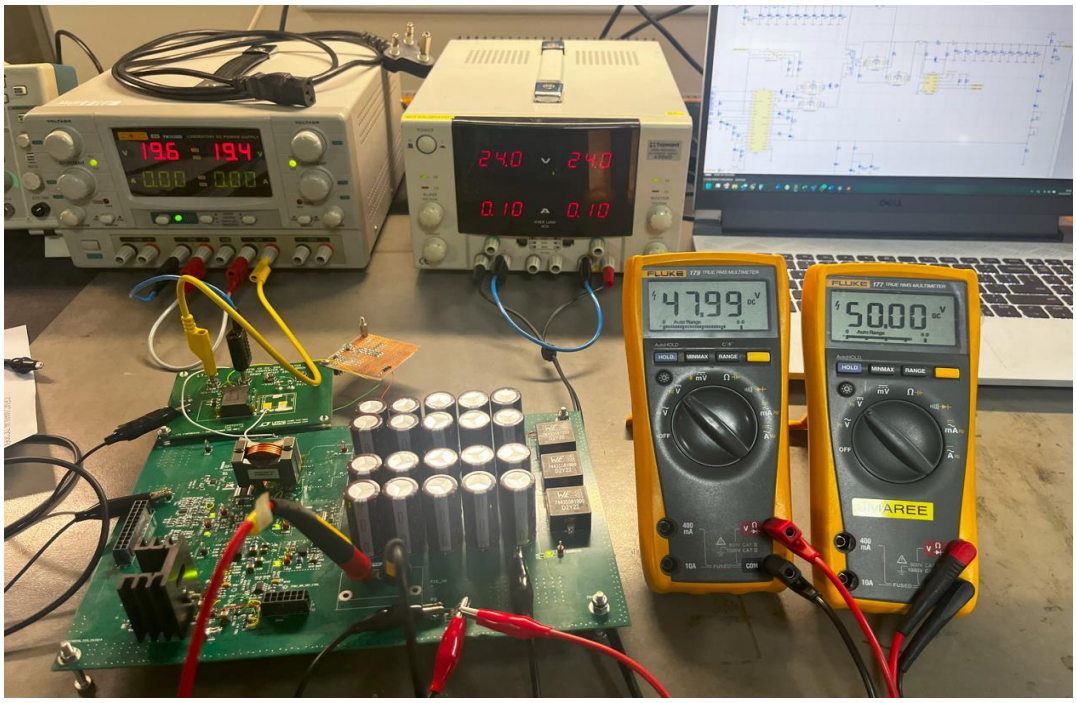

Figure 5. 19: Measurements - Input and Output Voltages

Figure 5. 19 above presents the input and output voltages regulated by the HUM. This means that the integration of the linear regulator and the SMPS is a success. To get to this stage, a lot of other HUM configuration is done and will be discussed in this study. Figure 5. 20 below is another setup during the testing showing measurements taken using an oscilloscope.

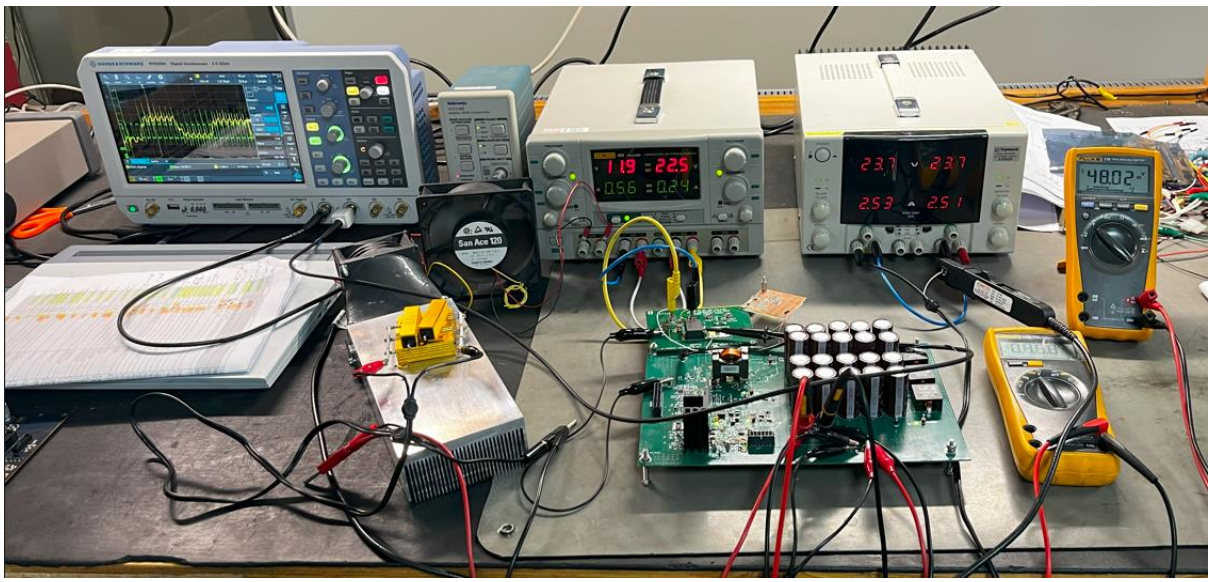

Figure 5. 20: Measurements

Figure 5. 21 below shows the HUM regulating a stable 50VDC with an input voltage of 46.63VDC. this is achieved by the adaptive duty cycle capability of the forward converter which allows the duty cycle to vary to compensate the input voltage drop.

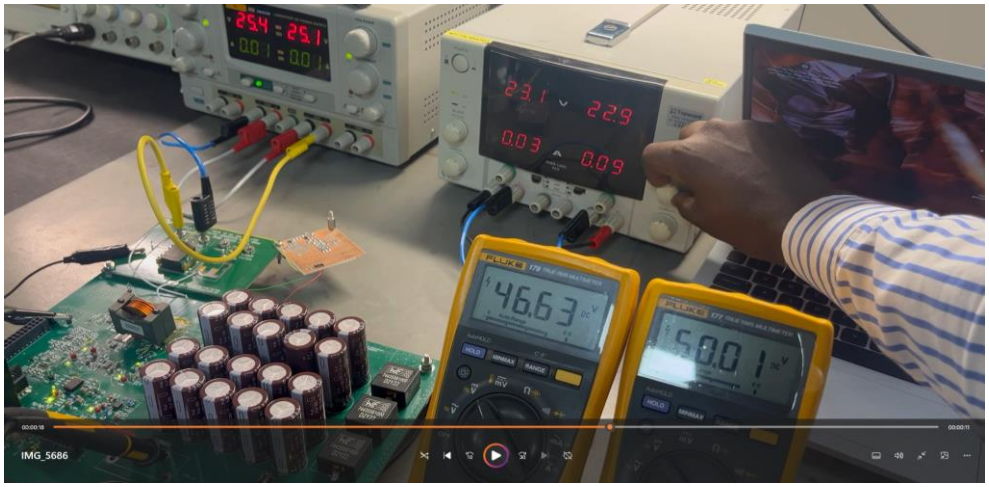

Figure 5. 21: Measurements - Reduced Input Voltage Test

5.3.3. Input Power OK

This section shows the sequence of ensuring that the input power to the hold-up module is present and within the set limits. After the dc-dc regulation of the onboard peripheral voltages is complete, the power conditioning sequencing begins. The peripheral voltages regulation is not discussed in detail in this study.

Ref voltage in xx below is a 3.3VDC line regulated by in the peripheral section of the design and is represented by the yellow trace in the ff. Vin in the figure below is generated from the input voltage of 48VDC via a resistor divider setup to drop it down to about 5VDC. Both the voltages are fed to a comparator and the output pf the comparator is used as Vb of a transistor that triggers the first stage of current limiting.

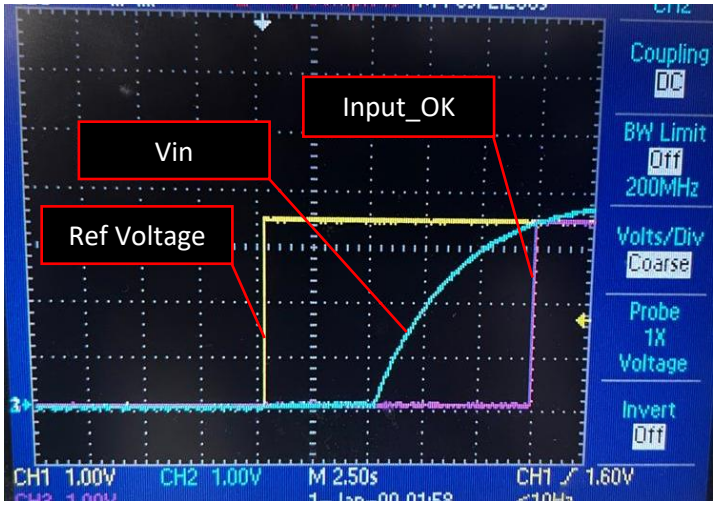

Figure 5. 22: Measurements - Input Voltage Okay & Current limiter trigger

5.3.4. Inrush Current control FET Gate to Source Configuration

Figure 5. 23 below shows the control of the current limiting mosfet. Two measurements, source voltage, gate voltage are taken and a MATH function is used to calculate and plot the gate to source voltage. Vsource is the blue trace, Vgate is the yellow trace and Vgate-source is the red trace.

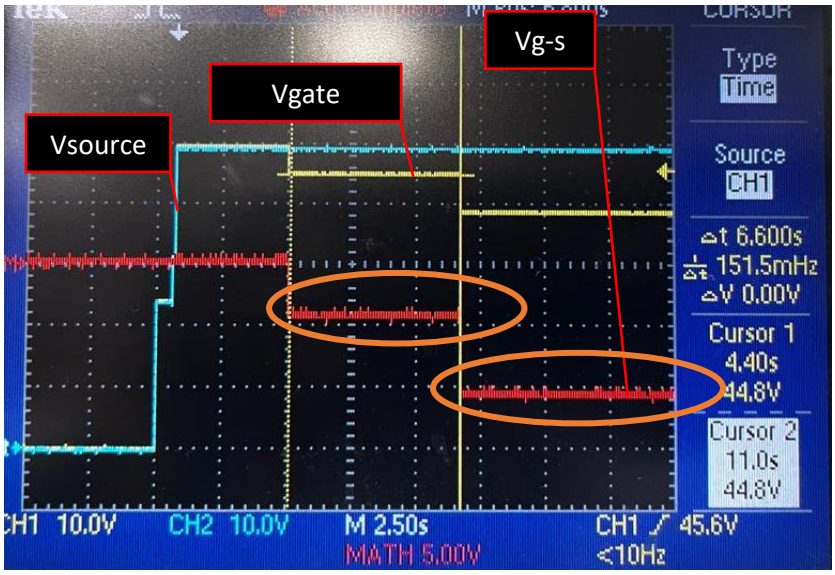

Figure 5. 23: Measurements - Inrush Current Control

5.3.5. Inrush Current Limiting Stage one Trigger

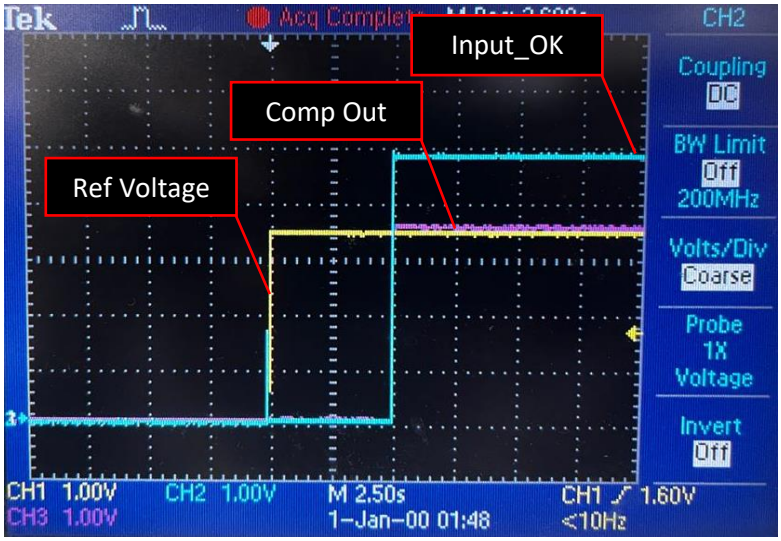

Figure 5. 24: Measurements - Inrush Current Stage one Trigger

In Figure 5. 24 above, reference voltage is the yellow trace, input ok is the blue trace and comp out is the purple trace. Ref voltage and input ok are the inputs to the comparator and the purple is the output. Input ok is fed from the first stage in Figure 5. 22, this comp out HIGH allows the first stage of current limiting. This is achieved by completing the gate to source resistor divider by supplying Vb to the transistor TR9 in the schematic diagram.

5.3.6. Inrush Current Limiting Second Stage Trigger

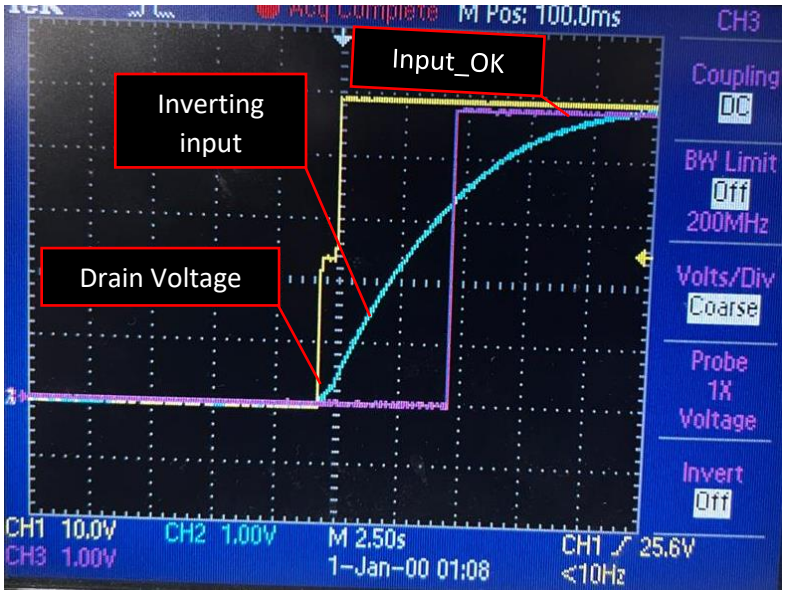

Figure 5. 25: Measurements - Inrush Current Second stage Trigger

In Figure 5. 25 above, the second stage of current limiting control graph is presented. Yellow trace is the drain voltage of the current limiting mosfet, blue trace is the output of the resistor divider as an inverting input to the comparator and purple trace is the output of the comparator. This is the logic that triggers the second stage of the current limiting sequence, setting gate to source voltage to -10.5VDC

5.3.7. Constant Charging Current

Figure 5. 26 below is the current limit graph, showing current capped at about 3Aand then ramping down. The capacitor banks are charged during the ramp up and the plateau at a constant current and then ramp down.

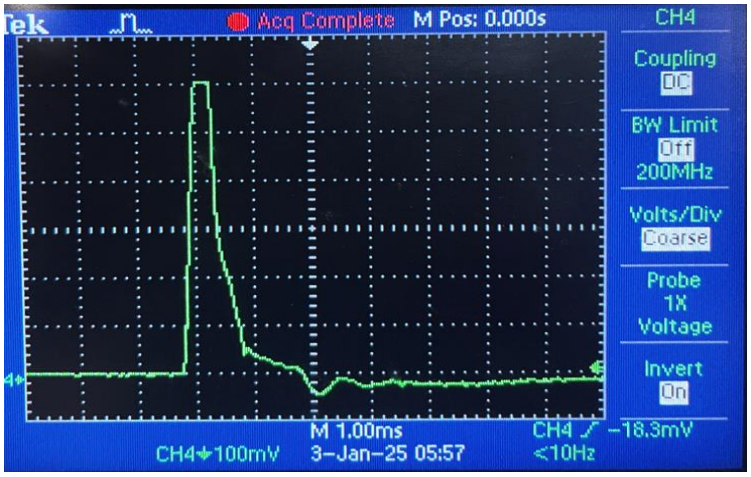

Figure 5. 26: Measurements - Input Current (Inrush)

5.3.8. Forward Controller Switching

Figure 5. 27: Measurements - Forward Controller Gate

The output of the forward converter switching is presented in Figure 5. 27 above. The forward converter switches from low duty cycle up to 50% as configured. The forward converter switches at a peak of about 11VDC.

5.3.9. Active Clamp Reset

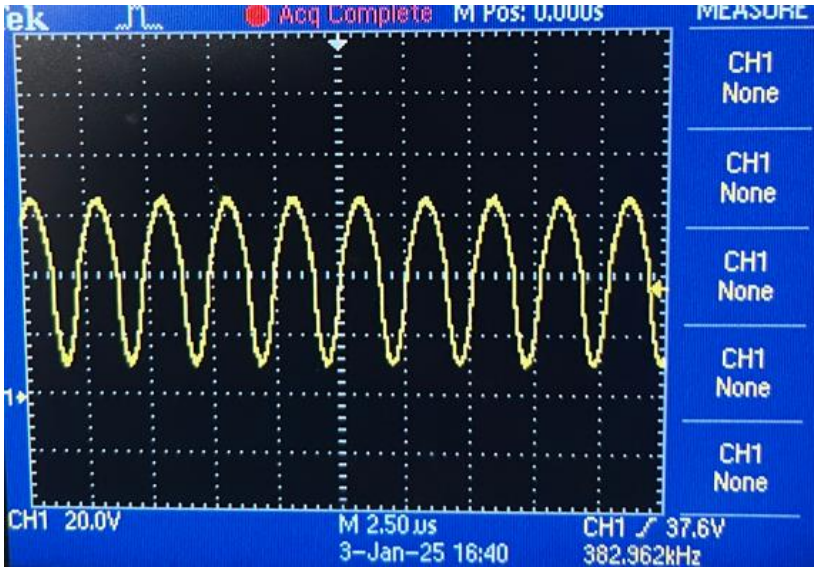

Figure 5. 28: Measurements - Transformer Voltage

Figure 5. 28 above show the drain voltage of the active clamping FET during the transformer demagnetizing. The controller is performing the clamping with a very small reset gap available.

5.3.10.Main switching FET vs Transformer primary winding

Figure 5. 29: Measurements - Transformer Primary voltage & Forward controller Switching

As seen in Figure 5. 29 above, the transformer voltage follows an inverse of the switching pulse when the main switching FET is switching, translating energy to the secondary side. The transformer goes back to demagnetising when the controller is not switching or translating energy to the secondary side.

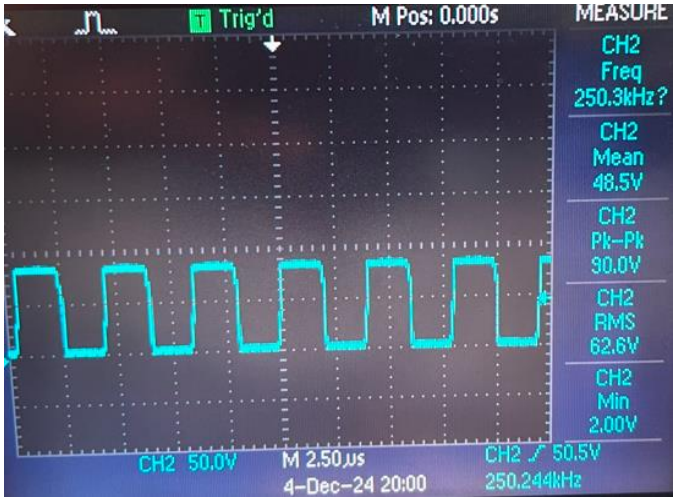

Figure 5. 30: Measurements - Transformer Secondary winding Voltage

Figure 5. 30 above is the secondary wing voltage during the switching period of the forward controller.

5.4. Hardware Conclusion

The prototype was evaluated to some degree, the results provided shows the successful integration of the SMPS into the HUM. The switch mode power supply tops up the required voltage to make up the 50VDC output voltage. The hold-up module meets the input fluctuation while maintaining the output requirement. The hold-up module does current limiting efficiently without generating a lot of heat on the current limiting FET.

Chapter 6

Conclusion and Recommendations

As demonstrated by the results shown in the hardware chapter and conclusion presented in 5.4, the testing of the HUM still needs more time and design optimisation. It is recommended that the test procedure is revisited to add more step-by-step procedure that will show more detail of each section in and around the HUM.

Develop a pulse test jig that will handle high current pulsed without melting soldering. This will allow the full potential testing of the hold-up module.

Re-design the PCB and make it a modular system, thus having:

- A motherboard
- Am inrush current control daughter board
- A daughter primary capacitor bank board
- A daughter controller board – in this case the forward controller
- A daughter secondary capacitor bank board
- A daughter control board
- A daughter BIM and Differential board.

This modular system will allow an easy method of developing and swapping out daughter boards without having to redesign the whole hold-up module, making the development of the SMPS based HUM efficient. The approach developed in this study may in future be used in more applications outside the power hold-up topology to further increase efficiency of other DC-DC converters in the isolated power supplies family.

6.1. PRF Design Exploration

This concept design is based on a 1.36kHz pulse repetition Frequency (PRF). This study has proven to be feasible at the 1.36kHz PRF, a future study going to higher PRF in the region of about 7kHz would be beneficial to the radar industry. The higher PRF presents about shorter OFF time between pulses, this brings the challenge of charging the energy up to the set voltage faster with higher peak current.

6.2. Synchronous Rectification Optimisation

The application of using synchronous rectification can further be investigated and compared between the self-driven configuration and having a circuitry that drives the gates of the MOSFETs. This investigation can be carried out to optimise the efficiency and operation of the synchronous rectifier.

6.3. Pulse and Switching Timing Optimisation

As presented in the design simulation chapter, the pulse fits in the OFF time of the main switching MOSFET giving the RF amplifier energy not influenced by the switching noise of the SMPS controller. The timing between the switching MOSFET going OFF and the pulse going high can be optimised by designing a circuitry that will delay the pulse after the controller has stopped switching. This would bring more control into positioning the pulse well within the OFF time of the controller and guarantee that the pulse will always be entered or place well within the OFF time of the controller at higher PRFs.

Chapter 7

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Appendix

Appendix 1: LT3753 Active Clamp Synchronous Forward Controller Datasheet Extract

Active Clamp Synchronous Forward Controller

FEATURES

- **Input Voltage Range: 8.5V to 100V**
- **Programmable Volt-Second Clamp**
- **High Efficiency Control: Active Clamp, Synchronous Rectification, Programmable Delays**
- Short-Circuit (Hiccup Mode) Overcurrent Protection
- Programmable Soft-Start/Stop
- Programmable OVLO and UVLO with Hysteresis
- Programmable Frequency (100kHz to 500kHz)
- Synchronizable to an External Clock

APPLICATIONS

- Industrial, Automotive and Military Systems
- 48V Telecommunication Isolated Power Supplies

DESCRIPTION

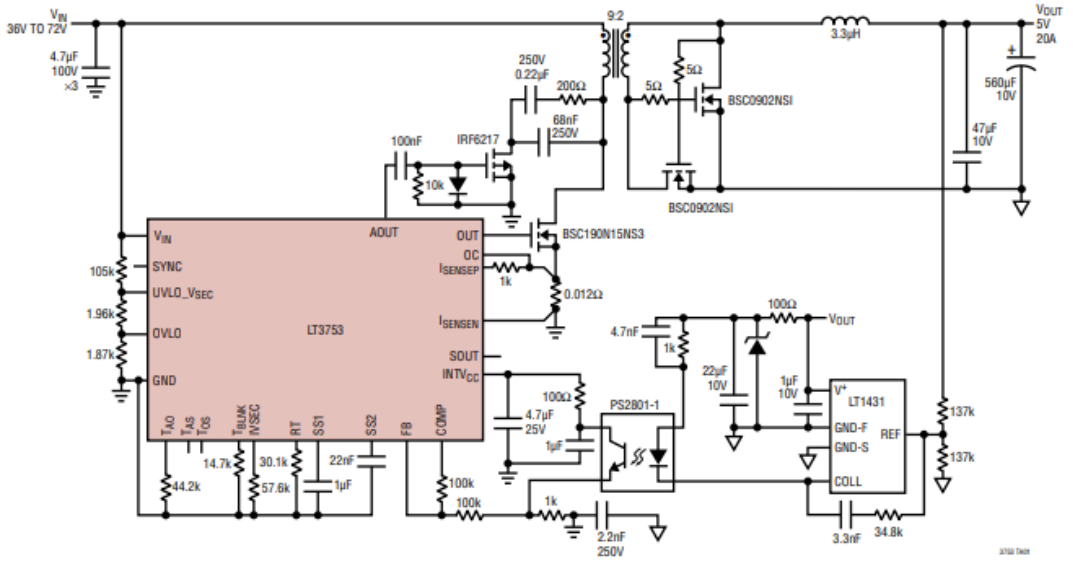
The LT®3753 is a current mode PWM controller optimized for an active clamp forward converter topology, allowing up to 100V input operation.

A programmable volt-second clamp allows primary switch duty cycles above 50% for high switch, transformer and rectifier utilization. Active clamp control reduces switch voltage stress and increases efficiency. A synchronous output is available for controlling secondary side synchronous rectification.

The LT3753 is available in a 38-lead plastic TSSOP package with missing pins for high voltage spacings.

TYPICAL APPLICATION

36V to 72V, 5V/20A Active Clamp Isolated Forward Converter



Rev. C

Forward Controller Pintouts

Out (Vgate)

The output on this pin is responsible to drive the main N-channel MOSFET. This pin is driven between 0V and INTVcc of the controller LT3753. This line is driven taking into account the value of the duty cycle at the time, the duty cycle adapts as the power requirement on the output side varies.

AOUT

The output on this pin is the clamped P-channel MOSFET drive signal, this pin controls the signal for external active clamp switch.

Comp

Error Amplifier Output. Allows various compensation networks for non-isolated applications.

GND (Pin 18):

Analog Signal Ground. Electrical connection exists inside the IC to the exposed pad (Pin 39).

PGND

The Power Grounds for the IC. The package has an exposed pad (Pin 39) underneath the IC which is the best path for heat out of the package. Pin 39 should be soldered to a continuous copper ground plane under the device to reduce die temperature and increase the power capability of the LT3753.Gnd

VCC

Input Supply Pin. Bypass with 1µF to ground.

SS1 (Pin 7)

Capacitor controls soft-start/stop of switching frequency and volt-second clamp. During soft-stop it also controls the COMP pin.

SS2 (Pin 17)

Capacitor controls soft-start of COMP pin. Alternatively, can connect to OPTO to communicate start of switching to secondary side. If unused, leave the pin open.

UVLO_VSEC (Pin 9)

A resistor divider from system input allows switch maximum duty cycle to vary inversely proportional with system input. This volt-second clamp prevents transformer saturation for duty cycles above 50%. Resistor divider ratio programs undervoltage lockout (UVLO) threshold. A 5µA pin current hysteresis allows programming of UVLO hysteresis. Pin below 0.4V reduces VIN currents to microamps.

OVLO (Pin 10)

A resistor divider from system input programs overvoltage lockout (OVLO) threshold. Fixed hysteresis included.

RT (Pin 3)

A resistor to ground programs switching frequency.

FB (Pin 4)

Error Amplifier Inverting Input.

NIPPON CHEMI-CON

MINIATURE ALUMINUM ELECTROLYTIC CAPACITORS

Long life, High ripple, 135℃

GPD New! Series

- Guaranteed short time at 150℃
- Downsized and high-ripple current version of GPA series
- For automobile modules and other high temperature applications
- Endurance with ripple current : 2,000 to 3,000 hours at 125℃ to 135℃
- Solvent resistant type (see PRECAUTIONS AND GUIDELINES)
- **RoHS Compliant**

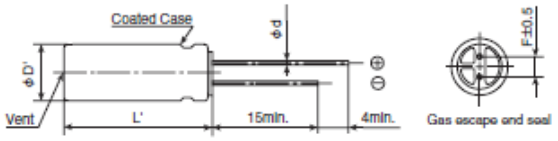
GPA P186 → Downsized Higher ripple current → GPD

◆SPECIFICATIONS

Items	Characteristics							
Category Temperature Range	−40 to +135℃							
Rated Voltage Range	25 to 100Vdc							
Capacitance Tolerance	±20% (M)							(at 20℃, 120Hz)
Leakage Current	I=0.03CV or 4μA, whichever is greater. Where, I : Max. leakage current (μA), C : Nominal capacitance (μF), V : Rated voltage (V)							(at 20℃, 1 minute)
Dissipation Factor (tanδ)	Rated voltage (Vdc)	25V	35V	50V	63V	80V	100V	
	tanδ (Max.)	0.14	0.12	0.10	0.10	0.08	0.08	
	When nominal capacitance exceeds 1,000μF, add 0.02 to the value above for each 1,000μF increase.							(at 20℃, 120Hz)
Low Temperature Characteristics (Max. Impedance Ratio)	Rated voltage (Vdc)	25V	35V	50V	63V	80V	100V	
	Z(−25℃)/Z(+20℃)	2	2	2	2	2	2	
	Z(−40℃)/Z(+20℃)	4	4	4	4	4	4	(at 120Hz)
Endurance 1	The following specifications shall be satisfied when the capacitors are restored to 20℃ after subjected to DC voltage with the rated ripple current is applied (the peak voltage shall not exceed the rated voltage) for the specified period of time at 125℃ or 135℃.							
	Time	125℃ 3,000hours 135℃ 25 to 50Vdc : 3,000hours 63 to 100Vdc : 2,000hours						
	Capacitance change	≤±30% of the initial value						
	D.F. (tanδ)	≤300% of the initial specified value						
	Leakage current	≤The initial specified value						
Endurance 2	The following specifications shall be satisfied when the capacitors are restored to 20℃ after the test condition that the rated voltage is applied for 100 hours at 150℃ and DC voltage with the rated ripple current is applied (the peak voltage shall not exceed the rated voltage) for the specified period of time at 125℃ or 135℃.							
	Time	125℃ 2,500hours 135℃ 25 to 50Vdc : 2,500hours 63 to 100Vdc : 1,500hours						
	Capacitance change	≤±30% of the initial value						
	D.F. (tanδ)	≤300% of the initial specified value						
	Leakage current	≤The initial specified value						
Shelf Life	The following specifications shall be satisfied when the capacitors are restored to 20℃ after exposing them for 1,000 hours at 125℃ without voltage applied. Before the measurement, the capacitor shall be preconditioned by applying voltage according to Item 4.1 of JIS C 5101-4.							
	Capacitance change	≤±30% of the initial value						
	D.F. (tanδ)	≤300% of the initial specified value						
	Leakage current	≤The initial specified value						

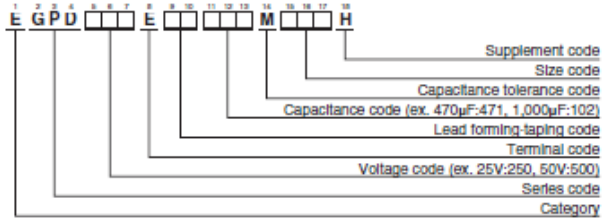
◆DIMENSIONS [mm]

●Terminal Code : E



φD	12.5	14.5	16	18
φd	0.6	0.8	0.8	0.8
F	5.0	7.5	7.5	7.5
φD'	φD+0.5max.			
L'	L+1.5max.			

◆PART NUMBERING SYSTEM



Please refer to "Product code guide (radial lead type)"

onsemi

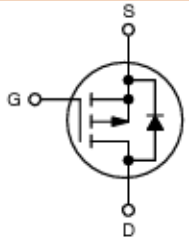
DATA SHEET
www.onsemi.com

MOSFET – P-Channel, QFET®

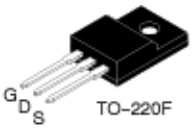
-60 V, -30 A, 26 mΩ

FQPF47P06, FQPF47P06YDTU

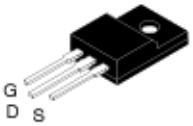
V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
−60 V	26 mΩ @ −10 V	−30 A



P−Channel MOSFET



TO−220 Fullpack, 3−Lead / TO−220F−3SG
CASE 221AT



TO−220−3LD LF
CASE 340BJ

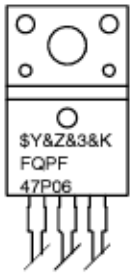
Description

This P−Channel enhancement mode power MOSFET is produced using **onsemi**'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on−state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- −30 A, −60 V, $R_{DS(on)}$ = 26 mΩ (Max.) @ V_{GS} = −10 V, I_D = −15 A
- Low Gate Charge (Typ. 84 nC)
- Low Crss (Typ. 320 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating

MARKING DIAGRAM



$Y	= **onsemi** Logo
&Z	= Assembly Plant Code
&3	= 3−Digit Plant Code
&K	= 2−Digits Lot Run Traceability Code
FQPF47P06	= Specific Device Code

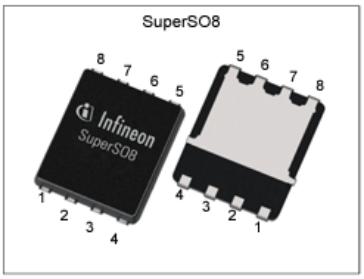
ORDERING INFORMATION

Device	Package	Shipping
FQPF47P06	TO−220−3 (Pb−Free)	1000 Units / Tube
FQPF47P06YDTU	TO−220−3 (Pb−Free)	800 Units / Tube

BSC0902NSI

MOSFET

OptiMOS™ Power-MOSFET, 30 V



Features

- Optimized SyncFET for high performance buck converter
- Integrated monolithic Schottky-like diode
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC[1)] for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

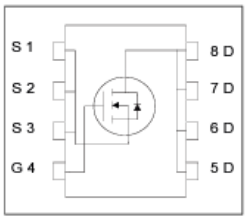


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	30	V
$R_{DS(on),max}$	2.8	mΩ
I_D	100	A
Q_{OSS}	17	nC
Q_G(0V..10V)	24	nC

Type / Ordering Code	Package	Marking	Related Links
BSC0902NSI	PG-TDSON-8	0902NSI	-

BSC190N15NS3 G

OptiMOS™3 Power-Transistor

Features

- N-channel, normal level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC[1)] for target application
- Ideal for high-frequency switching and synchronous rectification
- Halogen-free according to IEC61249-2-21

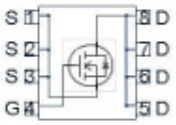
Product Summary

V_{DS}	150	V
$R_{DS(on),max}$	19	mΩ
I_D	50	A

RoHS

Halogen-Free

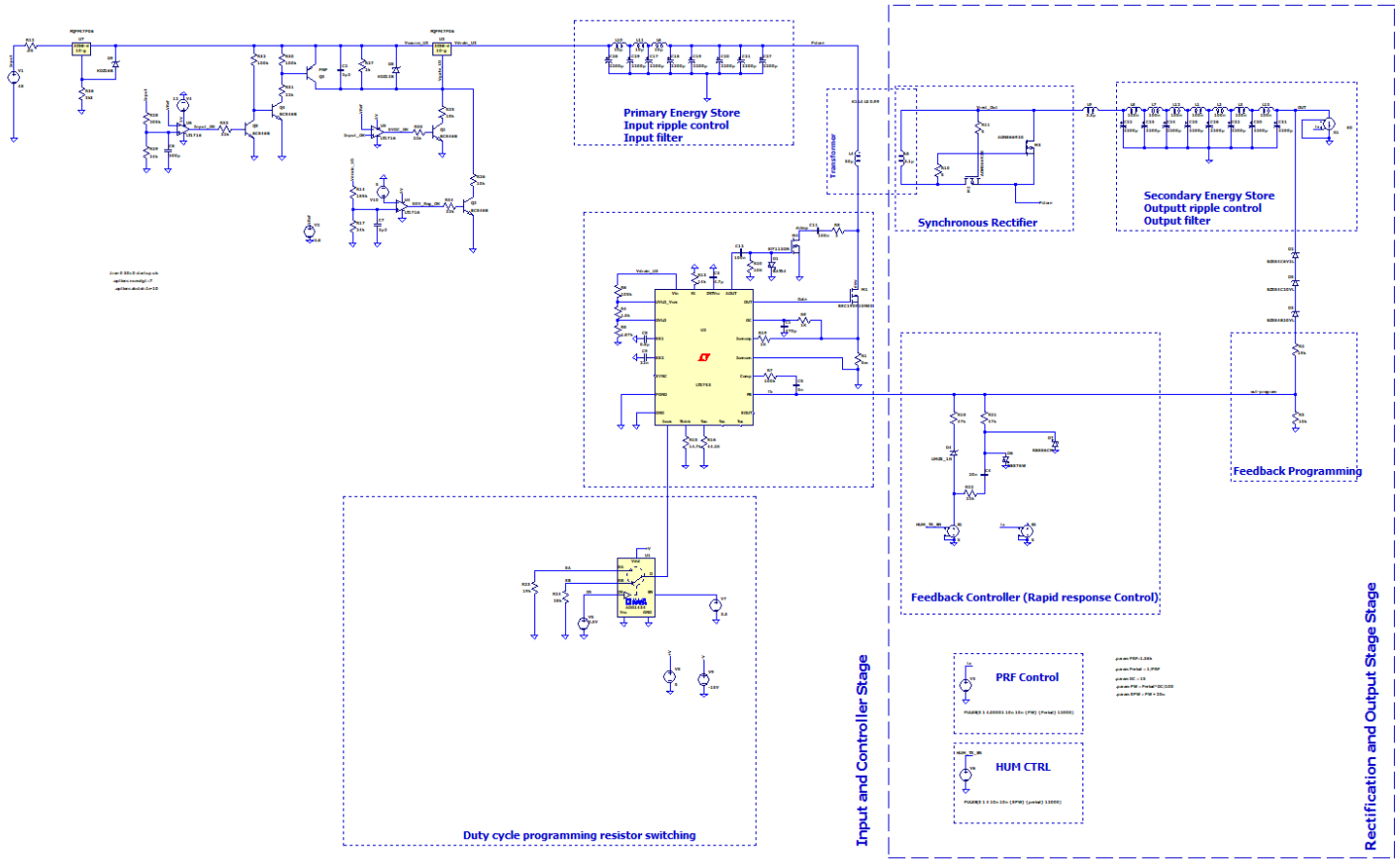
Type	BSC190N15NS3 G
	
Package	PG-TDSON-8
Marking	190N15NS



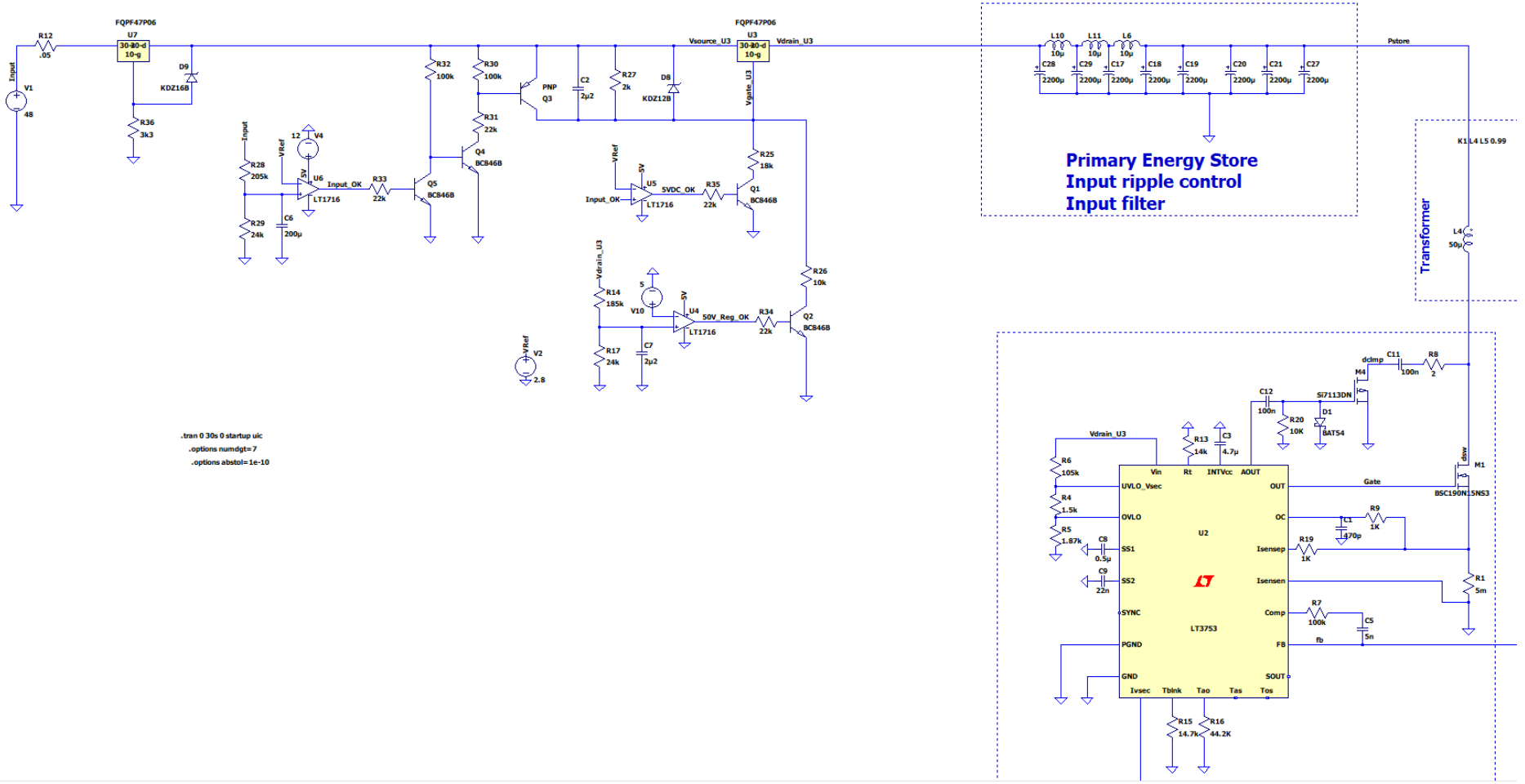
Maximum ratings, at T_j=25 °C, unless otherwise specified

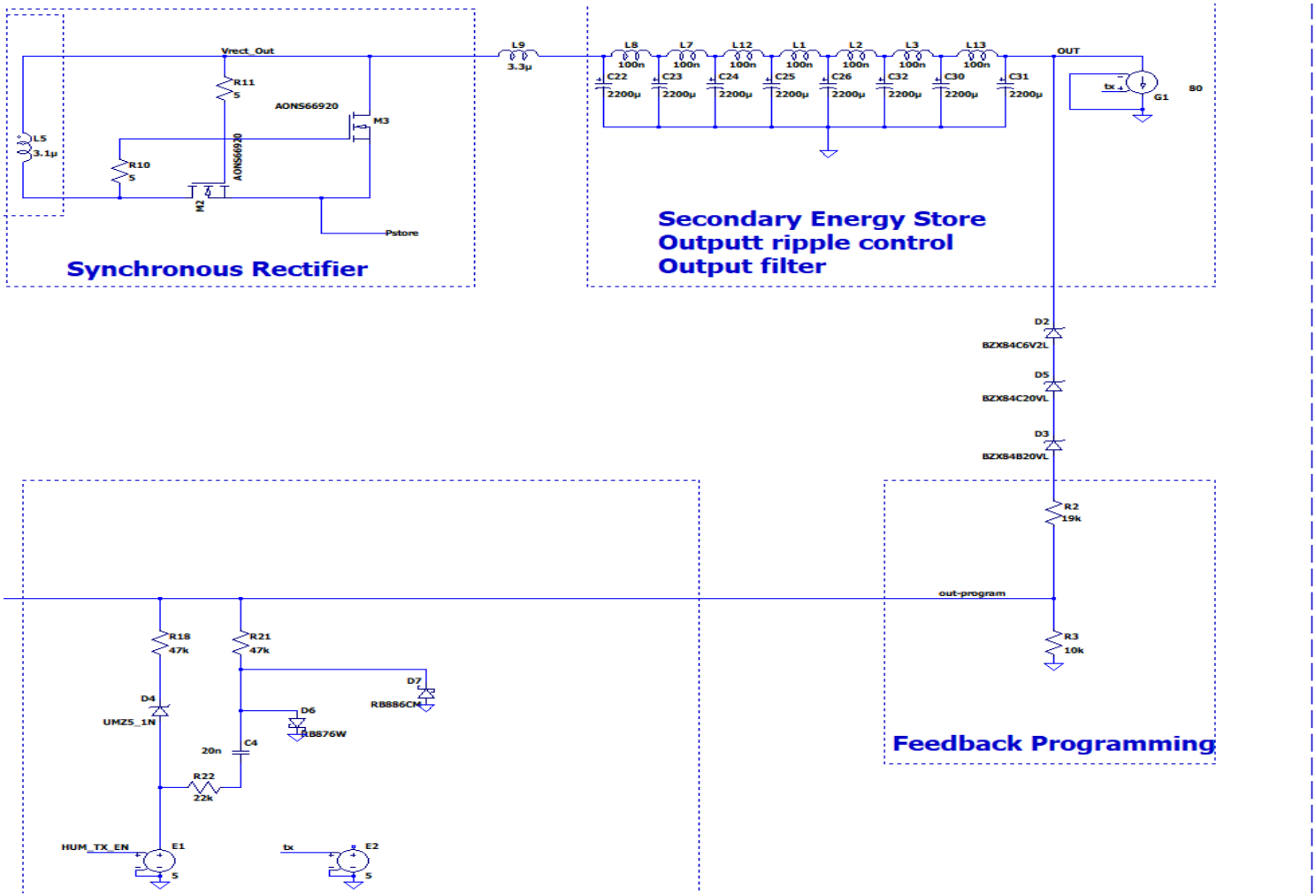
Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C	50	A
		T_C=100 °C	33	
Pulsed drain current[2)]	$I_{D,pulse}$	T_C=25 °C	200	
Avalanche energy, single pulse	E_{AS}	I_D=50 A, R_{GS}=25 Ω	170	mJ
Gate source voltage[3)]	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	125	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Appendix 6: Simulated Schematic Diagram



Appendix 7: Schematic Zoom In




Vrect_Out
R11
5
AONS66920
M3
L5
3.1µ
R10
5
AONS66920
M2
Pstore
Synchronous Rectifier
L9
3.3µ
L8
100n
L7
100n
L12
100n
L1
100n
L2
100n
L3
100n
L13
100n
C22
2200µ
C23
2200µ
C24
2200µ
C25
2200µ
C26
2200µ
C32
2200µ
C30
2200µ
C31
2200µ
OUT
tx
G1
80
Secondary Energy Store
Outputt ripple control
Output filter
D2
BZX84C6V2L
D5
BZX84C20VL
D3
BZX84B20VL
R2
19k
out-program
R3
10k
Feedback Programming
R18
47k
R21
47k
D7
RB886CN
D4
UMZ5_1N
D6
RB876W
20n
C4
R22
22k
HUM_TX_EN
E1
5
tx
E2
5