Cape Peninsula
University of Technology

# CHARACTERISATION OF RADIATION EFFECTS ON POWER SYSTEM COMPONENTS FOR CUBESATS

**by**

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## DECLARATION

I, Khader Destaing Mananga Bayimissa, declare that the contents of this thesis represent my own unaided work, and that the thesis has not previously been submitted for academic examination towards any qualification. Furthermore, it represents my own opinions and not necessarily those of the Cape Peninsula University of Technology.

**Signed** **Date**

## ABSTRACT

Front-end power converters for nanosatellite applications demand better performance in accurate reference tracking because of the wide-range input voltage of the solar panels. The very tight output voltage requirements demand a robust, reliable, and high-efficiency converter. The control of such a converter is very complex and time consuming to design. Two commonly used control modes are current and voltage control. The design and implementation of a voltage controller for DC–DC power converter is simpler but compared to current mode controller, does not do provide for overcurrent protection.

A single-ended primary inductance converter (SEPIC) was selected for this research work because of its ability to buck or boost the input voltage coupled with the ability to provide non-inverting polarity with respect to the input voltage. Parameter values for the converter studied are used to analyse and design both the voltage and the current mode controllers for the nanosatellite front-end power converter. Output voltage reference tracking with step and ramp changes in the input voltage is evaluated in terms of the time taken to reach steady-state after the induced disturbances and either the overshoot or undershoot of the output voltage reference. The design of analogue pulse width modulation (PWM) study was carried out in order to drive the metal-oxide-semiconductor field-effect transistor (MOSFET) switch. For the two controllers, changes in the reference output voltage in response to load changes are also studied.

An examination of the effects of solar radiation on the MOSFET switch was conducted; this switch is the main component of the front-end DC–DC power converter for a nanosatellite. At the more general level the examination also provided information on the response of the semiconductor technology in space application. The overall purpose of studying the MOSFET switch was to investigate the mechanisms that will facilitate its ability of switching ‘on’ and ‘off’ without failure as a result of solar radiation. The effects of solar radiation on MOSFET device in space, has resulted in more malfunctions of these devices in the past five years than over the preceding 40 years.

The modelling and simulation work was done using the National-Instrument-Multisim platform to analyse the analogue pulse width modulation, and laboratory virtual instrument engineering workbench (LABVIEW) was used to record data while running the radiation test on the circuit.

The design and implementation of the controllers was carried out using the SmartCtrl added module on the PSIM simulation platform. Results show that the current mode controller performed better than the voltage mode controller in terms of the reference tracking,

disturbance rejection and efficiency. Finally, a practical validation was carried out to confirm this research work.

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## LIST OF ABBREVIATIONS

| | |
|---|---|
| 1-U | 1 Unit nanosatellite 10 cm × 10 cm × 10 cm |
| 2-U | 2 Unit nanosatellite 20 cm × 10 cm × 10 cm |
| 3-U | 3 Unit nanosatellite 30 cm × 10 cm × 10 cm |
| AC | Alternative current |
| ALOS | Advanced land observing satellite |
| ATJ | Advanced triple junction |
| BJT | Bipolar junction transistor |
| CCM | Continuous conduction mode |
| CPUT | Cape Peninsula University of Technology |
| CRÈME | Cosmic ray effects on micro-electronics –commercial radiation test software |
| DC | Discontinuous current |
| DCM | Discontinuous conduction mode |
| DET | Direct energy transfer |
| DOD | Depth of discharge |
| EOC | End of charge |
| EPS | Electrical power supply |
| ESR | Equivalent series resistance |
| F'SATI | French South Africa Institute of Technology |
| GaAs | Gallium arsenide |
| GaN | Gallium nitride |
| GCR | Galactic cosmic rays |
| GEO | Geostationary earth orbit |
| GRAY | Derived unit of ionizing radiation dose |
| HEMT | High electron mobility transistor |
| IC | Integrated circuit |
| I-V | Current-voltage relation |
| LABVIEW | Laboratory virtual instrument engineering workbench –commercial test software |

| | |
|---|---|
| LEO | Low earth orbit |
| Li-Ion | Lithium-ion |
| Li-Po | Lithium-ion polymer |
| LET | Linear energy transfer |
| MEO | Medium earth orbit |
| MOSFET | Metal-oxide-semiconductor field-effect transistor |
| NMOSFET | Negative metal-oxide-semiconductor field-effect transistor |
| PMOSFET | Positive metal-oxide-semiconductor field-effect transistor |
| MPPT | Maximum power point tracking |
| NiCd | Nickel-Cadmium |
| NiMH | nickel-metal hydride |
| PCB | Printing circuit board |
| PV | Photovoltaic |
| PWM | Pulse width modulation |
| RAD | Deprecated unit of absorbed radiation dose |
| RMS | Root-mean-square |
| SAA | South Atlantic Anomaly |
| SEE | Single event effect |
| SEPIC | Single-ended primary inductance converter |
| Si | Silicon |
| SiC | Silicon carbide |
| SOC | State-of-charge |
| TID | Total ionizing dose |

## NOMENCLATURE

| | |
|---|---|
| $A$ | Amplifier gain ratio |
| $C$ | Speed of light [$2.9 \times 10^8$ m/s] |
| $C_{OX}$ | Oxide capacitance expressed per unit area |
| $D$ | Duty-cycle [%] |
| $E$ | Kinetic energy of particle [J] |
| $f$ | Frequency of light [Hz] |
| $h$ | Planck's constant |
| $I_{sc}$ | Short-circuit current [A] |
| $I_D$ | Drain current [A] |
| $I_{cell}$ | Cell current [A] |
| $I_{origin}$ | Origin current [A] |
| $I_{pv}$ | Photovoltaic output current [A] |
| $I_{ph}$ | Photovoltaic current [A] |
| $K$ | Constant whose value depends on the photovoltaic characteristic |
| $k_p$ | Proportional gain ratio |
| $L$ | Gate length [nm] |
| $m$ | Mass in motion [kg] |
| $m_0$ | Particle rest mass [kg] |
| $m_1$ | Slope of rising inductor current [A] |
| $m_2$ | Slope of falling inductor current [A] |
| $Q_{inv}$ | Inversion layer charge per unit area [C] |
| $R_{load}$ | Load resistor [Ω] |
| $t_r$ | Transit time [s] |

| | |
|---|---|
| $v$ | Velocity of the particle [$5 \times 10^{-8}$ m/s] |
| $V_{DS}$ | Drain-source voltage [V] |
| $V_{mpp}$ | Maximum power point voltage [V] |
| $V_p$ | Peak voltage [V] |
| $V_{pp}$ | Peak to peak voltage [V] |
| $V_o$ | Output voltage [V] |
| $V_{ref}$ | Reference voltage [V] |
| $W$ | Gate width [nm] |
| $X$ | Length of the material [m] |
| $\beta$ | Feedback factor |
| $e$ | Elementary charge [C] |
| $\epsilon$ | Electric field |
| $\Delta Io$ | Inductor current graph with distortion [A] |
| $\rho$ | Density of the material [kg/m$^3$] |
| $\Delta P$ | Change in power dissipation [W] |
| $\Delta N_{ot}$ | Change densities of oxide trapped charges [kg/m$^3$] |
| $\Delta N_{it}$ | Change densities of oxide interface states [kg/m$^3$] |
| $\Delta_S$ | Characteristic equation |
| $\mu$ | Mobility |

- **Research publications emanating for this thesis**

  **Mananga Bayimissa, K., Raji, A. & Marco, A**., 2015. *Performance Evaluation of Voltage and Current Control Mode Controller for SEPIC Converter in CubeSats Application.* Cape Town, Industrial Commercial Use of Energy (ICUE),pp.351-359.

  **Mananga Bayimissa, K., Raji, A. & Marco, A**., 2015. *Robust and Highly Efficient Wide-Input Range Power Converter for Space Application*. Cape Town, Domestic Use of Energy (DUE), pp. 209-214.

  **Mananga Bayimissa, K., Raji, A. & Marco, A**., 2015. *A Development of Maximum Power Point Tracking Based on DC–DC SEPIC Power Converter for Space Application.* Istanbul, Energy Technology (ENTECH), under reviews.

  **Mananga Bayimissa, K., Raji, A. & Marco, A**., 2015. *A Front-end DC–DC Power Converter for Space Application.* Istanbul, Energy Technology (ENTECH), under reviews.

# Chapter 1 : GENERAL CONCEPT OF THE STUDY

## 1.1 Background and introduction

Satellites are used for numerous purposes; the most common applications are communications, space weather, earth observation, navigation and research satellite. A satellite consists of different subsystems and is capable of carrying a payload, which are in most cases, electrical devices. Environmental conditions in space are more severe than on earth, mostly due to low residual pressure and solar radiation (Adams and Holmes 2004). Solar radiation can cause errors in the functioning of nanosatellite. Eventually components fail as the total radiation dose has grown large enough. Therefore, special care is needed when designing electrical devices to be used in a space system. One of the most essential subsystems on a spacecraft is the power system (Adams & Holmes, 2004; Hemmo, 2013).

The principal external energy source in space is solar radiation; and as such any spacecraft power system not using solar energy must therefore have its own source of energy. These sources may include fuel cells, nuclear, or chemical fuel. The available energy sources found onboard nanosatellite are photovoltaic (PV) solar cells and batteries (Bettex, 2010).

A spacecraft power system generally consists of primary power sources, secondary sources, power controllers, and a distribution system. Solar arrays are used as a primary power source in most spacecrafts when a long lifespan is required. Solar energy is a reliable power source as incoming solar radiation does not vary significantly when the satellite is above the earth atmosphere. Batteries are typically used as secondary power source to store and deliver the energy generated by solar arrays. Energy storage is necessary for the operation during orbital solar eclipse periods (Patel, 2005). The power system is responsible for distributing the power to the subsystems and payloads of the satellite (Hemmo, 2013). A simplified model of a typical electrical power supply is presented in Figure 1-1.

The harsh space environment contributes to the failure of the electronic system of a spacecraft (Figure 1-2). The aging and performance of electronic components are modified by radiation effects. The performance of spacecraft systems such as: electronic units, sensors power units, payload equipment, communication units, remote sensing instruments, data handling units, and propulsion units is dependent on the proper functioning of various electronic systems that are highly sensitive to space radiation (Coderre, 2006). In addition the payload of spacecraft invariably consists of sensitive electronic equipment which is similarly affected.

Space radiation can cause damage to electronic components or functional failure of the electronics. Proper procedures, processes and technologies need to be in place to ensure that space radiation is not a threat to the functionality and performance of electronics during operation (Dopart et al., 2012).

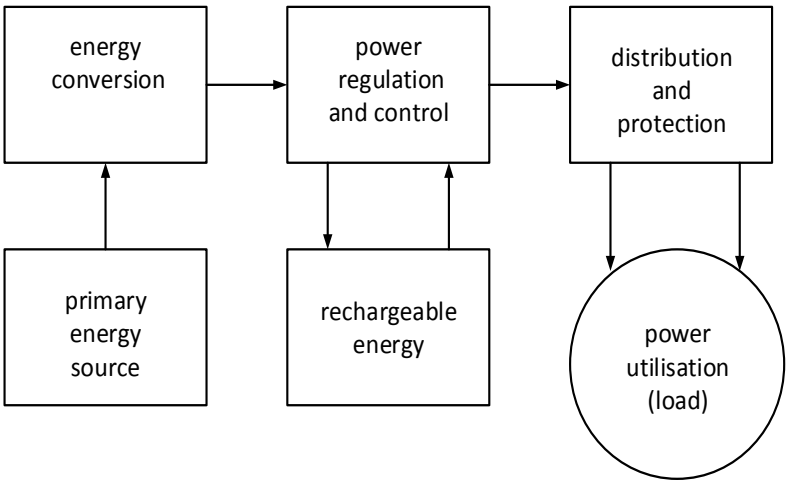


**Figure 1-1: A typical CubeSats electrical power system block diagram**

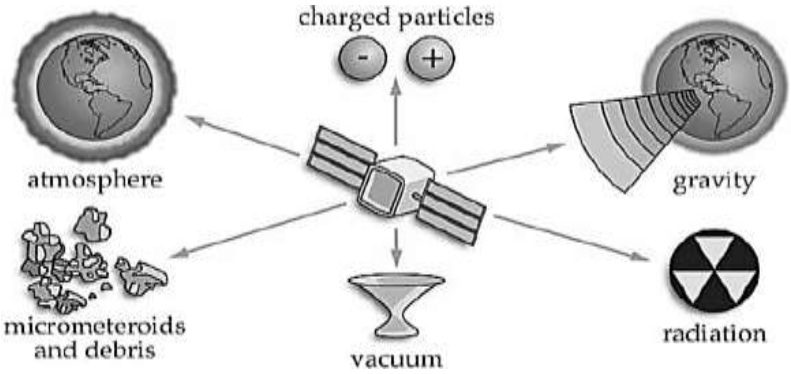


**Figure 1-2: Factors which act upon a spacecraft in the space environment (Coderre, 2006)**

Diodes rectifiers can be used to reduce the input voltage magnitude needed by the load, but using this method is inefficient. The use of voltage regulators is needed to efficiently provide a suitable reference voltage for the system.

In addition, the decreasing or increasing of the battery output voltage can produce many problem to the system if the there is no feedback control is provided to the system. There are five principal types of DC–DC switch mode power converters namely, buck, boost, buck-boost, CúK, and DC–DC SEPIC. The buck converter can only step down the voltage in a system, whereas the; boost converter can only step up the voltage and the buck-boost, CúK, and DC–DC SEPIC, can increase or decrease the voltage.

A buck or a boost converter can be used in many simple conversion networks where in accordance with the topology used, the voltage only be decrease or increase respectively. However, the required output voltage needed could be greater, less or equal the input voltage. The DC–DC buck-boost converter can be simpler the other DC–DC step up/down converter types to implement due to the single inductor and single capacitor it uses. However, this buck-boost converter has high current ripple input. This ripple produced the harmonics; the ripple is smoothed out by the use of the large capacitor or LC filter in network; therefore, the costs of the converter become high and inefficient due to the loss of energy. In fact the major problem of this converter is the response of the inverter output voltage to the utility.

The DC–DC CúK converter solves the inverting polarity of the output of the buck-boost and the high input ripple current by adding an extra inductor and capacitor in the circuit. However, CúK and buck-boost converters operation produce a large amount of electrical stress on electronics components. This could result the device failure or overheating in the network. The SEPIC solved the CúK and buck-boost problems.

### 1.2 Problem statement

One of the main challenges in space applications is to design a front-end DC–DC power converter capable of operating in the harsh environmental conditions of space. To solve these challenges, different techniques have been used to design a suitable converter; one of these techniques fault-tolerant hardware has been used in space systems for over the past couple of years to either ensure error-free operation, or to mask the error from the system. This research will investigate whether a robust front-end DC–DC power converter, using analogue pulse width modulation signal and voltage- and current-mode controls, will optimize the functionality in terms of weight, size and power challenges as presented by the nanosatellite standard.

### 1.3 Objectives of the research work

The specific objectives to meet the stated outcome of this research are listed as follows:

- Design a robust front-end DC–DC power converter according to nanosatellite specifications.
- Design an analogue pulse width modulation signal and determine if it is well suited for implementation in a front-end DC–DC power converter for a nanosatellite.
- Investigate the most common types of space radiation effect which adversely affecting the operation of the MOSFET switch in space.
- Investigate the different types of feedback control applied in nanosatellite technology.
- To provide criteria that facilitates the selection of appropriate electronic components suitable for space application.
- Produce simulated results from a front-end DC–DC power converter using appropriate software.
- Produce a framework for experiments to aid in the design of a front-end DC–DC power converter for a nanosatellite.
- Conduct tests to verify the correct response of a front-end DC–DC power converter module, while using voltage and current mode control as a proof of concept.

### 1.4 Research Methodology

A literature review was completed to establish extent of radiation space environment and its effects on switching MOSFET component within an electrical DC–DC power converter system. More research will be directed into the sensitive part of nanosatellite power system such as: the solar cells, maximum power tracking, the battery topology, and the mode of converting solar energy for the whole nanosatellite system. In order to establish to apply suitable technology to meet the design requirements of the front-end DC–DC power converter system, a high quality investigation needed to be done into DC–DC power converters technology. The investigation of solar radiation effect on the MOSFET switch is recorded while using LABVIEW.

Various DC–DC power converter topologies were investigated with regard to the modulation technique used and the implementation of feedback control. Tests will be done to determine the efficiency of the converter topologies considered.

This was followed by the design of specific sub-circuit of the nanosatellite power sub-system, simulating a sub-circuit, procurement of components, construction and testing of circuit and the overall simulations test of the entire network.

### 1.5 Delineation of study

This study focused on:

- the electrical power system of the nanosatellite, specifically on the front-end DC–DC power converter,
- the radiation effects during low-earth orbits and its effect on MOSFET switch,
- identification and evaluation of the components needed to implement the analogue pulse width modulation.

An engineering prototype of the power sub-system module was developed and tested at in the laboratory of CPUT and Ithemba-lab.

The power module was subjected to the different test scenarios, and the results were interpreted mostly based on the application scientific and engineering principles to explain the results obtained relating to nanosatellite technology, MOSFET technology. This approach will be applied to understanding the destructive impact of space weather changes on the front-end DC–DC power converter.

### 1.6 Literature study

This part is a well-established part of any research process and is mostly base on collecting the theoretical information about the nanosatellite power system, MOSFET technology, space radiation, photovoltaic cells, maximum power tracking, DC–DC power converters, compensation network, as well as the feedback control loops.

### 1.7 Simulation and Modelling

This section deals with the simulations of front-end DC–DC power converter module, which is based on mathematical equations representing the passive components values of the system constraints. The modelling techniques consist of capturing the system level requirements and the architectures of the design. To complete these simulations a PSIM platform model with its add-on SmartCtrl and NI Multisim National Instruments.

### 1.8 Thesis outline

This thesis consists of seven chapters and appendixes which are organised as described below:

- **Chapter 1**

  In this chapter the background and introduction to this research work is given. It presents an awareness of the problem investigated, the objective of the study, the problem statement, and the research methodology applied in this research work.

- **Chapter 2**

  Chapter 2 is focused on a review of the literature related to space radiations, as well the effects of solar radiation inside the spacecraft.

- **Chapter 3**

  This chapter deals with the power system literature study of the nanosatellite. The study specifically looks at a comparison of different type of batteries, photovoltaic cell technologies, as well on the different techniques of maximum power tracking available.

- **Chapter 4**

  The literature study for this chapter relates to DC–DC power converter topologies, feedback control loops and the slops compensation networks.

- **Chapter 5**

  This chapter is devoted to the design and simulation results of the front-end DC–DC power converter and the analogue pulse width modulation network.

- **Chapter 6**

  This chapter is dedicated for practical results discussion and validations of the system results.

- **Chapter 7**

  This chapter deals with a low-energy proton irradiation, and test validation of a MOSFET.

- **Chapter 8**

  Based on the results of work undertaken for this thesis, a conclusion is presented in this chapter. Also, flowing from the work undertaken, recommendations are made regarding possible future avenues of research

- **Appendices**

  In the appendixes the performance of control feedback of the front-end DC–DC power converter, the key diagrams obtained after modelling of the system are presented and datasheets.

# Chapter 2 : OVERVIEW OF SPACE RADIATION

## 2.1 Introduction

This chapter presents a literature study of space radiation. Firstly, the statistics on nanosatellite malfunctions will be presented. The different types of known radiation in space will be discussed, and the effects of radiation on electronic semiconductor materials will be presented. This is followed by an analysis, based on engineering concepts, of the radiation effects inside a nanosatellite which finds itself exposed to external radiation in a space environment. The last part of this chapter deals with power devices.

## 2.2 Nanosatellite statistics

Examining spacecraft status by launch year (Figure 2-1), two issues are apparent. From 2000 to 2012 there have been 122 CubeSat missions, and 12 of the 13 failed to achieve their missions initiated from 2002 to 2003, and only 5 of the first 36 survived launches and operated successfully. Secondly, it is instructive to note that the number of CubeSats failures each year has not diminished; from 2000 to 2006 an average of three missions launched each year fail to accomplish their objectives (Swartwout, 2013).

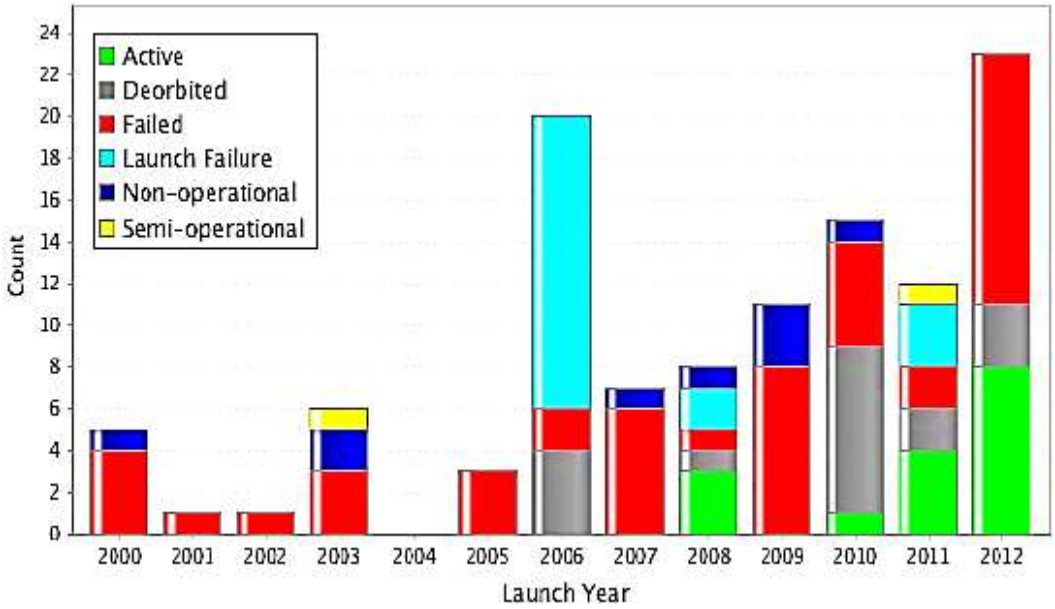


**Figure 2-1: CubeSats mission outcomes by launch year (Swartwout, 2013)**

The causes of mission failure were investigated and the results are depicted in Figure 2.2. As can be seen from the pie chart, nearly half (45%) of the failures were because the CubeSats could not be contacted after launching.

Such failures could have any number of causes, including power failure, communications failure, software lockup, radiation induced latch-up of electronics components, or mechanical failure due to launch loads (Swartwout, 2013).

Looking at the failure mechanisms it is apparent that the following three mechanisms make up almost half of all failures: more closely, a common thread was identified which accounts for almost half of all the failures: configuration or interface failure between communications hardware (27%), failure of the power subsystem (14%) and the flight processor (6%). Examples of such failure are listed below (Swartwout, 2013):

- Batteries and/or solar panels not connected properly to the power bus;
- Insufficient power generation to operate the transmitter at a level needed to close the link;
- Unrecoverable processor;
- Electronic circuitry failed due to space radiation effects

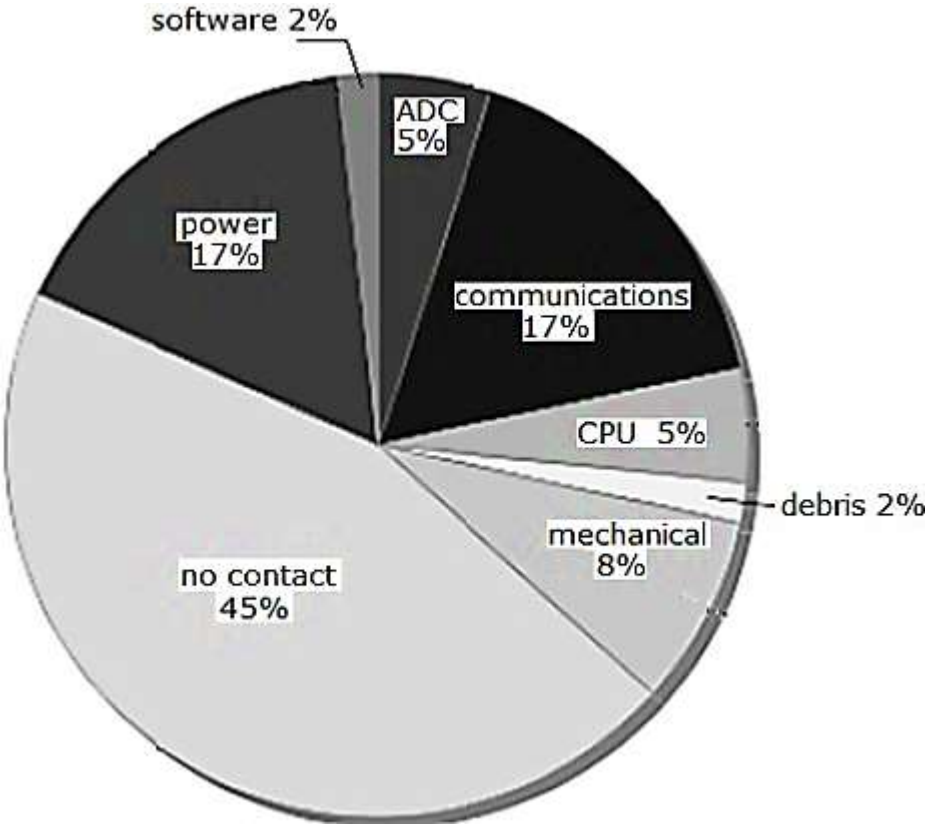


**Figure 2-2: Causes for CubeSats mission failure, 2000-2012 (Swartwout, 2013)**

## 2.3 Physical concepts

### 2.3.1 Energy

Kinetic energy represents the energy of motion. When the particles have rest mass, the Equations 1 and 2 are fundamental of kinetic energy is related to the mass and velocity can be given in the following:

relavistic: $E = (y - 1)mc^2,$ (1)

where: $y = \left[1 - \left(\frac{v}{c}\right)^2\right]^{-\frac{1}{2}}$

and: $E$ is the kinetic energy of particle

$m$ is the mass in motion

$c$ is the speed of light

Non-relavistic: $E = \frac{1}{2}m_0v^2$ (2)

where: $m_0$ is the particle rest mass

$v$ is the velocity of the particle

Equation 3 for the equivalent energy of a photon, which does not have a rest mass, is given by:

$$E = hf \quad (3)$$

where: $h$ is Planck's constant

$f$ is the frequency of light

Energy can be expressed in terms of joule or electron volt. An electron volt is a measure of energy gained by an electron moving through an electric potential difference of one volt (Amutkan, 2010). The relationship between the joule and an electron volt is given by:

$$1\ \text{eV} = 1.602\ X\ 10^{-19}\ \text{J} \quad (4)$$

### 2.3.2 Radiation dose

Radiation dose is a measure of deposited energy from an ion radiation per unit mass of a material. The dose is given by radiation absorbed dose because the energy deposition is dependent on the material. Unit of a dose can be written in terms of radiation absorbed dose rad or gray (Amutkan, 2010). The relationship between the Rad and Gray is shown below:

$$1\ \mathrm{Gy} = \frac{1\ \mathrm{J}}{\mathrm{kg}} = 100\ \mathrm{Rads} \tag{5}$$

### 2.3.3 Flux

Flux is the rate of flow of matter through a unit area, where matter could for instance be energy, photons, or radiation particles. In addition, for energy radiating from a particular source, the energy flux is usually given as the amount of energy flowing through a steradian per second; the units are $J \cdot sr^{-1}$ or $W \cdot s^{-1}$. However, when discussing the flow of particles, the unit of flux is given as the number of particle/$m^{-2}s^{-1}$ (Amutkan, 2010).

### 2.3.4 Linear energy transfer

Linear energy transfer (LET) is another way of quantifying the effect of ionizing radiation on electronic devices. LET is a measure of the energy transferred per unit length of absorbing material; it is defined as follow:

$$\mathrm{LET} = \frac{1}{\rho}\frac{dE}{dx} \tag{6}$$

where: $\rho$ is the density of the material
$E$ is the energy loss through the material
$x$ is the length of the material.

The unit of LET is $MeV \cdot g^{-1} \cdot cm^2$.

### 2.4 Low earth orbit (LEO)

Although Maini and Agrawal (2011), define LEO as orbits at altitudes between 150 km and 500 km above the surface of the earth, orbits of altitudes less than 1000 km above the surface of the earth are generally considered as LEO (Haduverdi & Baylakoglu, 2011). The advanced land observing satellite (ALOS) has collected data on space radiation in a Low earth orbit environment for minimum periods of solar activity between September 2006 and February 2011 (Koshiishi & Matsumoto, 2012).

Energies of around 10 MeV for protons and around 1 MeV for electrons were used to characterise the space radiation environment; above these energy levels the particles are most likely to penetrate the outer shell of a spacecraft.

Table 2.1 shows the simulated probability distribution of proton per energy range at 650 km altitude (Mayanbari & Kasesaz, 2011). This probability distribution is a good estimate of the population of different energetic protons in LEO; it shows that low energy protons are much more probable to find in LEO, Figure 2-3 shows the proton flux as a function of the energy spectra in LEO. It compares simulations to the data plotted on the CRÈME software, based on a database containing data from the 1970s to 2007 (Mayanbari & Kasesaz, 2011). It shows that there is a much higher flux of low energy protons in LEO.

**Table 2.1: Simulated probability of protons based on their energy spectra at 650 km altitude – Mayanbari and Kasesaz (2011)**

| Energy spectrum (MeV) | Probability |
|---|---|
| 1-10 | 0.882994 |
| 10-20 | 0.012832 |
| 20-30 | 0.008637 |
| 30-40 | 0.009249 |
| 40-50 | 0.008353 |
| 50-150 | 0.051168 |
| 150-250 | 0.016980 |
| 250-350 | 0.006103 |
| 350-400 | 0.003684 |

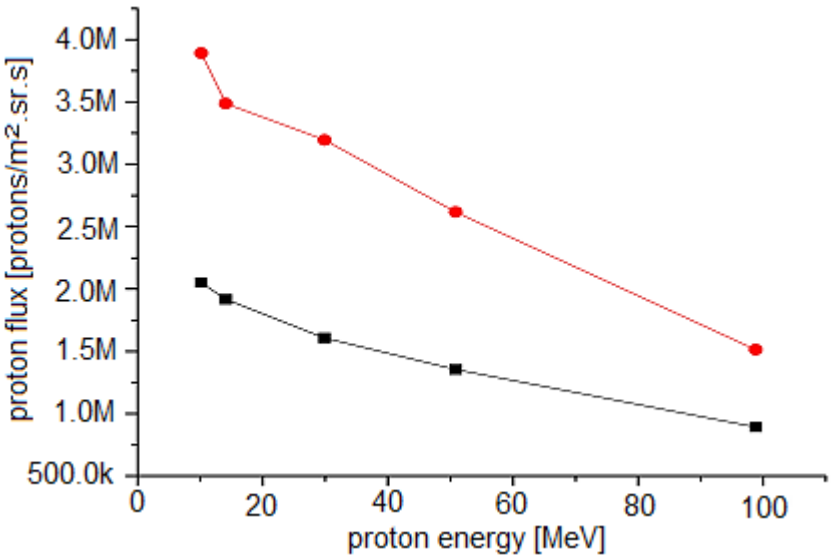


**Figure 2-3: Variation of proton flux with energy in LEO adapted and digitized from Mayanbari and Kasesaz (2011)**

### 2.5 Geostationary earth orbit

A Geostationary earth orbit (GEO) is an orbit that lies in the equator plane of the earth and is located at an altitude of 36000 km. Satellite missions in a GEO are exposed to outer radiation belts, solar flares and cosmic rays. In a GEO, satellites are exposed to a dose of about 10 krad/year; for typical 10 year mission, the total dose is 100 krad (Petkov, 2003; Amutkan, 2010).

### 2.6 Medium Earth Orbit

Medium earth orbit (MEO) is an orbit which has a range from 2000 to 36000 km altitude above the earth surface. Since a space system is mostly within the Van Allen belts in MEO it is harshly exposed to radiation. The MEO environment is highly affected by the solar cycle effects and the dose rate is in order of 100 krad/year (Petkov, 2003; Amutkan, 2010).

### 2.7 Space radiation environment

#### 2.7.1 Earth's geomagnetic field

The magnetic field on earth is generated within its core, through a combination of thermal movements, the earth's daily rotation, as well as by electrical forces within a core. These elements in combination form a dynamo that sustains a magnetic field which can be closely approximated by the field of giant dipole positioned near the center of the earth and inclined approximately 11.3$^{o}$ from the earth's spin axis. This magnetic field can be visualized (see

Figure 2-4) as magnetic field lines leaving one end of magnet, bending through the space, and re-entering the magnet at the other end.

The direction and strength of earth's magnetic field varies at different positions on the surface of the earth and it can be measured. The geomagnetic cavity generated by the earth's magnetic field is call magnetosphere. Over time the earth's magnetic field is slowly changing, reflecting the flow of thermal currents within the ion core (John, 2013).

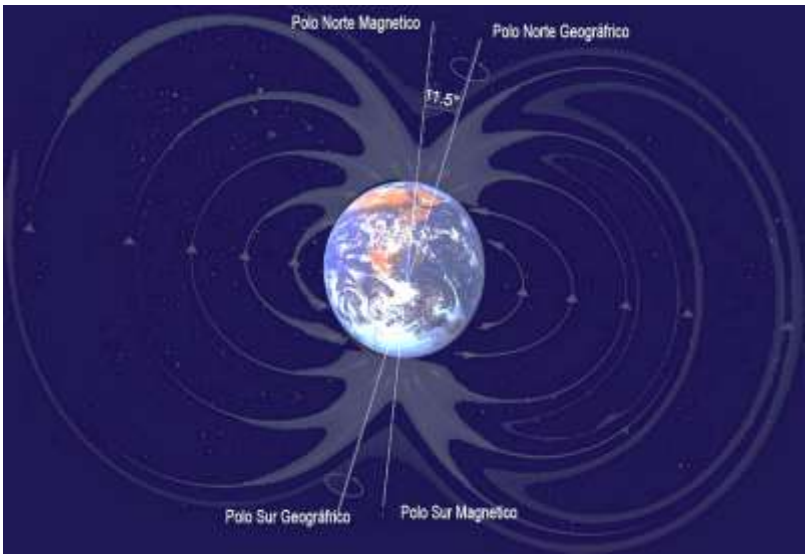


**Figure 2-4: Magnetic field of the earth's (Nave & Baseden, 1991)**

### 2.7.2 Trapped radiation environment

The earth's radiation environment is composed of different particles with varying energies; to a large extent radiation exposure depends on the location. The geomagnetic field lines trap charged particles such as electrons, protons, neutrons, alphas particles and some heavy ions; these particles gyrate spirally around the magnetic field lines and are reflected between ends of the magnetic flux lines, as shown in Figure 2-5 (Stassinopoulos & Raymond, 1988). Protons and electrons drift around the planet, with electrons moving to the east and protons moving to the west.

The motion of trapped particles forms bands of electrons and protons around the earth, and are responsible for the creation of two radiation belts, which are called the Van Allen radiation belts (Aksu, 2013). Figure 2-6 shows the earth's Van Allen belts formed by the earth's magnetosphere (Barnes & Selva, 1996).

The Van Allen belts were discovered in 1958 and are the result of the collision between solar winds and earth magnetic field. The solar wind is an electrically charged gas which blows from

the sun; the wind intensity varies with the sun's surface activity. The belts mainly consist of energetic protons and electrons with lesser percentage of heavy ions.

The inner belt is populated by high-energy (about 20–80 MeV) protons and medium energy (50–1000 keV) electrons and extends from an altitude of about 100 km to 6000 km in, while the outer belt is populated by high-energy electrons extending up to 60000 km in altitude (Garret, 1999). Regarding particles, the region between the Van Allen belts is by and large unpopulated.

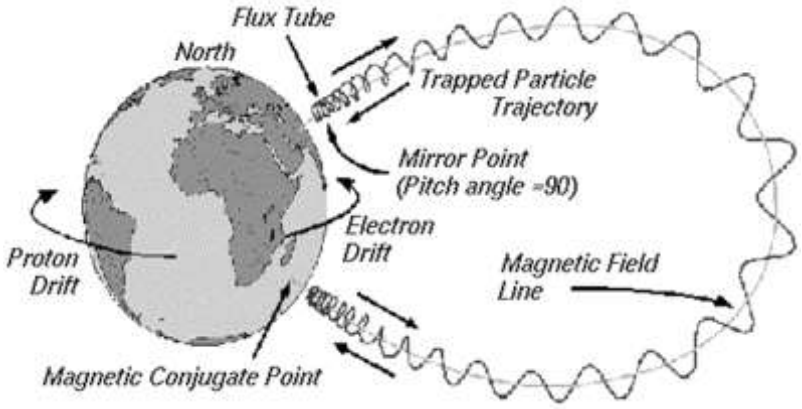


**Figure 2-5: Motion of trapped particles in earth's magnetosphere (Stasinopoulos & Raymond, 1988)**

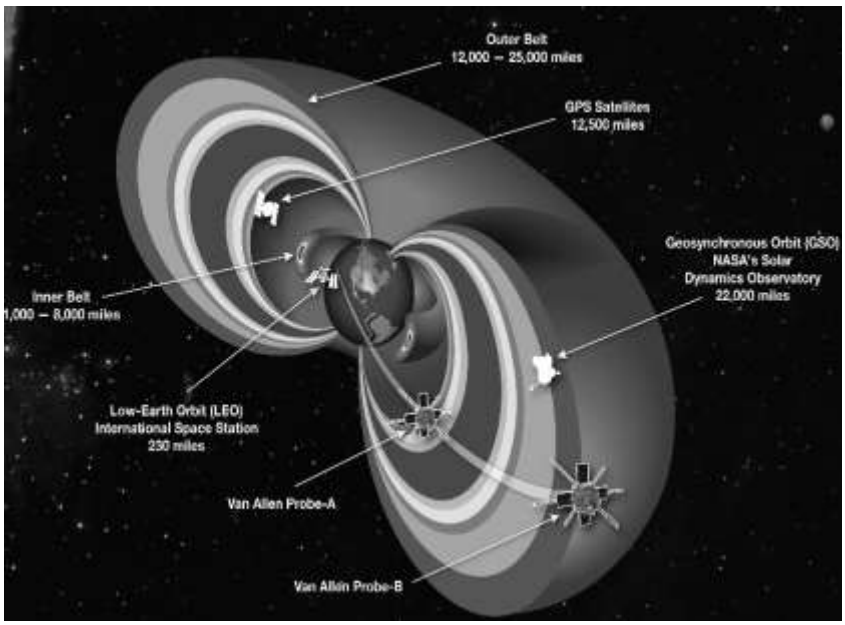


**Figure 2-6: The Van Allen belts (Aksu, 2013)**

### 2.7.3 South Atlantic Anomaly (SAA)

The centre of the earth's magnetic field is not at its geographical centre; geographical centre; neither do the magnetic poles coincide with the geographic poles. The Van Allen belts are closer to the earth on one side than on the other. They are closest to the South Atlantic area, which is known as South Atlantic Anomaly and has a relatively high, concentration of particles. This higher than usual concentration of particles creates a depression in magnetic field over the South Atlantic due to the charged particles which are trapped at a lower altitude at about 1000 km (Barth, 2004).

This result in a much higher flux of particles intersecting with a spacecraft passing through the anomaly, as compared to the other locations in the orbit; hence the operation of Low earth orbit (LEO) satellites can be affected (Hudson, 2008). Figure 2-7 shows the geographic location of the SAA; the proton flux increases at low altitudes over the South Atlantic Ocean.

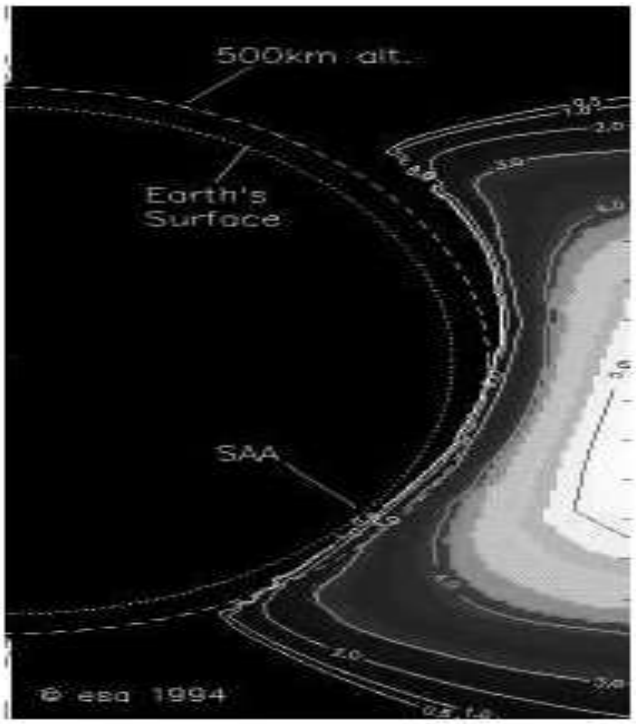


**Figure 2-7: South Atlantic Anomaly (Daly et al., 1996)**

### 2.7.4 Normal and worst case radiation environment

The complexity of defining the normal and worst-case radiation environment depends on many factors. The criticality levels of system components vary and hence it is difficult to predict single-event effects in those components.

Worst-case conditions are not applied to a system when it is not intended to work in worst-case radiation activities. The normal case radiation environment condition for a system requires that the system be able to handle the daily average; worst cases passes through the SAA, and heavy ions from background cosmic rays. On the other hand worst-case conditions are defined and applied while the system performs critical in a mission; the system must then operate at all times and no errors due to radiation are permitted (Label, 1996). Examples of the worst-case conditions are peak fluxes in the SAA and peal solar flare conditions.

### 2.8 Source of space radiation

The energy deposition in spacecraft materials, particularly electronic materials, may cause significant damage if not taken into account when designing a space mission (Ma & Dressender, 1989). In general, the ionizing radiation is made up of electromagnetic radiation such as: X-rays and Y-rays, and radiation caused by charged particles such as: electrons, protons, alpha particles and other heavier ions. Electromagnetic radiation which has a solar origin, origin, is not a significant source of ionization for the interior of a space vehicle, and thus has a minor effect on electronics systems (Corliss, 1968).

However, radiation due to charged particles has a significant effect and causes energy deposition inside space. Radiation in the space environment is classified as emanating from three main sources, namely: solar particles, geomagnetic trapped radiation near the earth orbit (Van Allen belts), and galactic cosmic rays (Corliss, 1968; Dopart et al., 2012). Cosmic rays consist of energetic electrons, protons, alpha particles and heavy ions from all the elements in the periodic table. Particles trapped by the magnetosphere include heavy ions, protons and electrons. Particles and their respective energy are shown in Table 2.2, (Barth et al., 2004).

#### 2.8.1 Trapped electrons and heavy ions

The main sources of radiation for earth-orbiting systems such as communication satellites, electrons and protons trapped in the earth's magnetosphere; as shown in Figure 2-5. The mapping of trapped heavy ions by satellite showed that these ions are not insufficiently energetic to penetrate a satellite; also the electrons are not known to induce transients (Label, 1996).

**Table 2.2: Energies of the particles in space radiation environment**

| Particle type | Maximum Energy |
|---|---|
| Trapped electrons | About 10 MeV |
| Solar Protons and Heavy Ions | About 100 MeV |
| Solar Protons | GeV |
| Solar Heavy Ions | GeV |
| Cosmic Rays | TeV |

### 2.8.2 Trapped protons

For the inner Van Allen belts, protons are the more important radiation components as compared to heavy ions. Protons can generate more transients in electronic devices because they can more easily penetrate a spacecraft and affect its electronic devices. Within the constraints of a spacecraft weight budget, it is difficult to provide against high energy protons. The population of trapped protons varies with the intensity of the solar cycle. It is important to consider the range of the trapped proton population to which a spacecraft can expect exposure, when designing for radiation mitigation (Label, 1996).

### 2.8.3 Galactic cosmic ray protons and heavy ions

Galactic cosmic rays (GCRs) are high-energy charged particles, which originate from outside the solar system. GCR consists of about 85% protons, 14% alpha particles and 1% heavy nuclei. Due to the highly energetic particles in GCRs, intense ionization is produced as they pass though the matter. The main radiation effect caused by the GCR is single-event effects in electronic circuits. Like proton shielding against these highly energetic particles is also difficult. The energy level of a galactic cosmic ray particle also varies with the ionization state of the particle. The distribution of GCR ions as function of kinetic energy is shown in Figure 2-8 (Label, 1996).

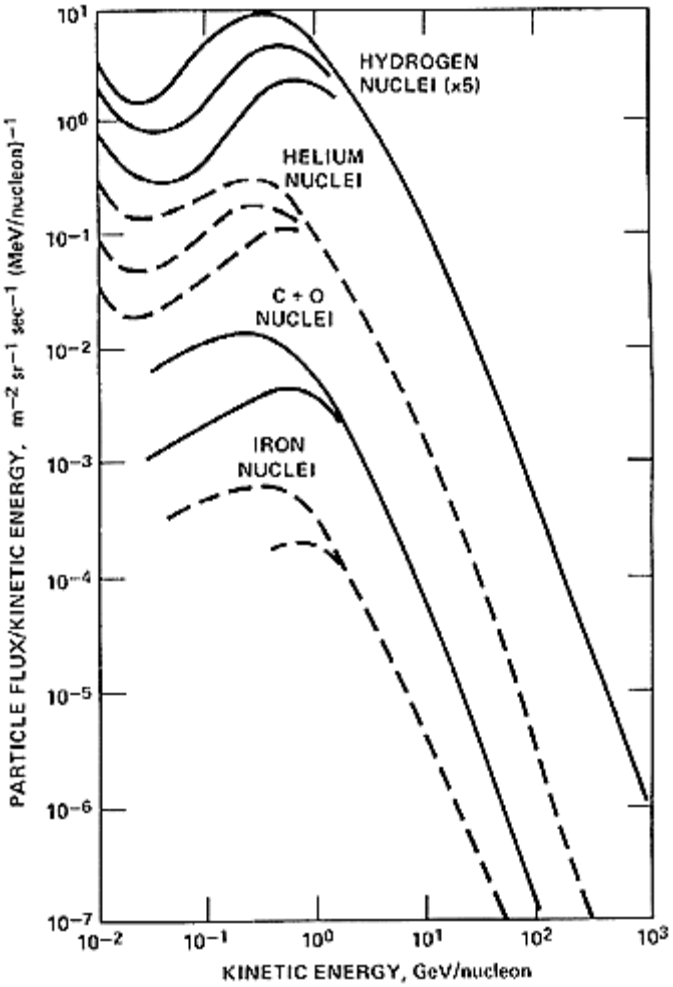


**Figure 2-8: Distribution of the energy levels of various galactic cosmic rays (Stassinopoulos & Raymond, 1988)**

### 2.8.4 Solar flare protons and heavy ions

Solar flares are one of the important sources of ionized radiation particles. Energetic protons, alpha particles and heavy ions are emitted in a solar flare. In the most solar flares, protons and alpha particles are in majority, while heavy ions make up only a small fraction of the emitted particles (Schwank et al., 2008). An average solar cycle is eleven years and can be divided into a relatively inactive four year period with a small number of solar flares occurring, and an active seven years period with several large number of solar flare events. Past and predicted solar cycles are shown in Figure 2-9, (Phillips, 2006). During the phase of decreased solar activity, maximum radiation from GCRs occurs and together with a few significant solar flare events; the solar flares may last from several hours to few days. Solar flare particles are attenuated by earth's magnetosphere (Label, 1996).

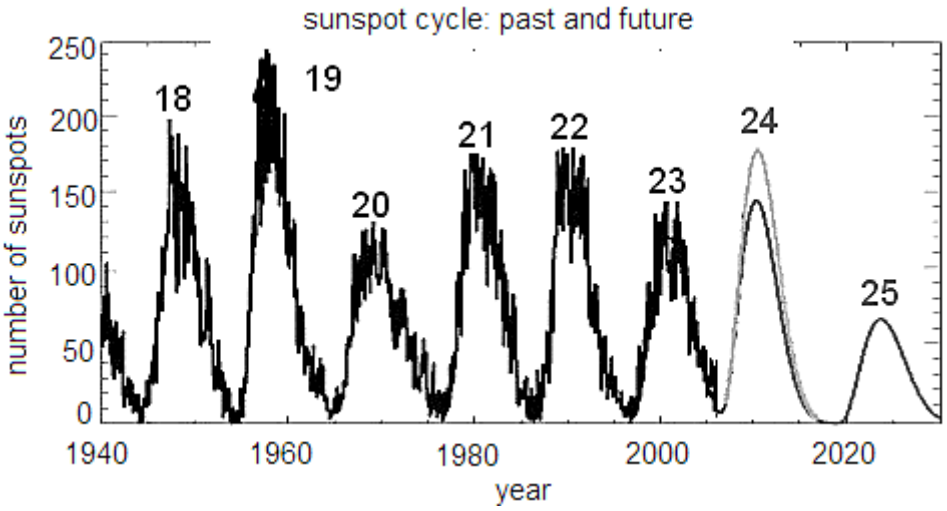


**Figure 2-9: Past and future solar cycles (Phillips, 2006)**

### 2.8.5 Displacement damage

Displacement damage is a non-ionizing damage generated by the displacement of individual atoms from their original position in a lattice structure; this damage is the result of the collision between an incoming particle and a lattice atom. Displacement damage is generated by protons, neutrons, and electrons with energy greater than 150 keV. The absence of an atom from its original position in the lattice structure due to the displacement of an atom results in a vacancy defect in the lattice, and if the displaced atom lodges on a non-lattice position, it is called an interstitial. The combination of a vacancy and an interstitial is known as closed pair or a Frenkel pair (Sayil, 2013).

## 2.9 Radiation effects on space systems

It is necessary to define the environmental effects on space systems before launch and to define the radiation levels within the space system. Basic principle mechanisms of space radiation effects and impacts on electronic systems are talk over in terms of single-event effects (SEEs) and total ionizing dose (Amutkan, 2010).

### 2.9.1 Single Event Effects

A single event effect is caused by striking a single energetic particle deposited along the track of a microelectronic device. As stated by Amutkan (2010), a single-event can be classified into three forms:

- A single-event upset is defined as a radiation-induce error in microelectronic circuits;
- A single-event latch up is the term used to describe a particular type of short circuit in an integrated circuit;
- A single-event burnout occurs when there is a high-current power transistor causes the device failure
- A single-event gate rupture is defined as the destructive rupture of a gate dielectric due to a high magnetic field generated by high-current.

### 2.9.2 Total Ionizing Dose (TID)

The total ionizing dose (TID) effect, due to trapped protons and electrons contained in radiation belts and protons emitted by solar flares, may result in device failure or biological damage to astronauts in space systems. The main dose source in Low earth orbits originates from protons and electrons, while at high altitudes in other words Geostationary earth orbits, the main dose source is from solar protons and electrons (Amutkan, 2010).

The total ionizing dose depends on altitude, inclination, and time. The calculation of the TID is carried out for the exact location of the space system. Total dose levels are calculated for all components, taking account of the shielding provided by the structure of the spacecraft. To evaluate the TID, a dose depth curve is consulted; this curve relates the dose received to the shielding thickness. The size of the shield is often not solid as the aluminium sphere. Dose depth curve is used to specify the spacecraft mission requirements for radiation assurance (Amutkan, 2010).

### 2.9.3 Effects of displacement damage on semiconductors

Displacement damage in semiconductor materials can significantly change their electrical and optical properties through the radiation-induce levels in the band-gap. The following are the five basic radiations-induce degradation effects as stated by (Srour, 2003):

- The generation of electron hole pairs, due to radiation
- The recombination of electron hole pairs
- Trapping of carriers
- Compensation of donors and acceptors
- Tunnelling of carriers

Displacement damage affects carrier lifetime, resistivity, and mobility. Carrier concentration inside semiconductors may cause failure of specific properties of electronic component, the electronics component characteristic to a failure, such as: transistors gain, junction leakage current, breakdown voltage and saturation voltage. The components most sensitive to the displacement damage are: linear bipolar transistors, phototransistors, and solar cells. This sensitivity is due to the majority carrier concentration reducing the lifespan of these components in space contrary to this; metal-oxide-semiconductor field-effect transistors are not sensitive to displacement damage because they are majority carrier devices and heavily doped (Barnes & Selva, 1996).

### 2.9.4 Displacement damage for solar cells

Protons and high-energy electrons can generate displacement damage to solar cells because the glass cover material used for solar cells is thin, providing ineffective shielding (Johnston, 2000).

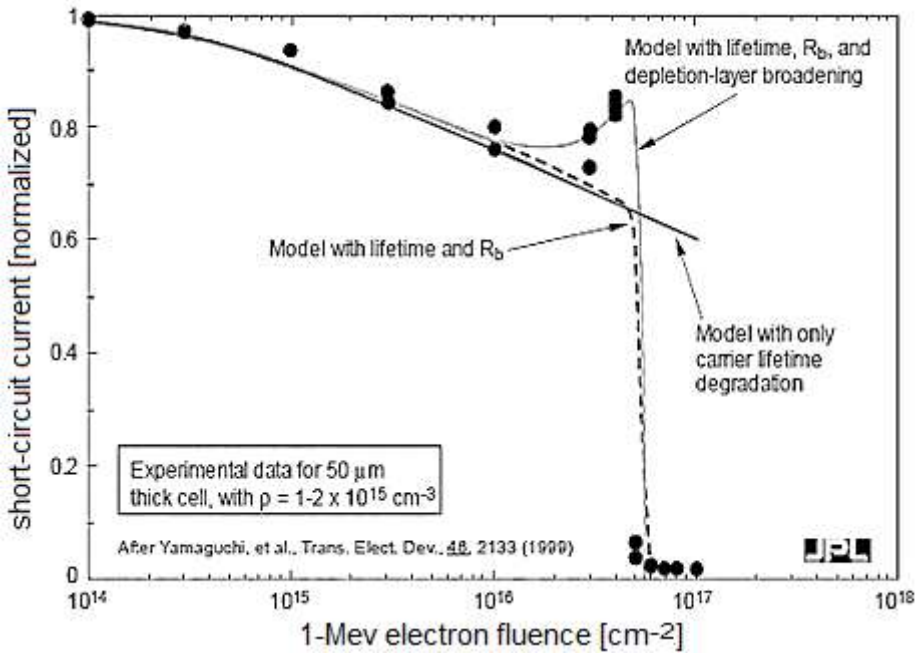


**Figure 2-10: Degradation of solar cells at high electron fluence (Yamaguchi et al., 1999)**

As per the model developed by Yamaguchi (1999), high electron fluence can generate catastrophic failure to solar cells due of carrier removal. Figure 2-10 show sharp decrease in $cm^{-2}$ short-circuit current at high electron fluence.

### 2.10 Radiation environment inside a spacecraft

Thus far, Up to this point the natural space radiation environment outside a spacecraft, has been explored the natural space radiation environment outside a spacecraft. To evaluate the effects of the natural space radiation environment on power system electronics component inside the spacecraft, the shielding must be taken into account. Shielding does not only modify the radiation environment inside a spacecraft by altering the energy and concentration of incoming particles; it can also create secondary particles as incoming particles pass through the shielding, such as bremsstrahlung in the form of X-rays, is emitted as energetic electrons decelerate in the shielding. For average shielding, the effects of shielding can be estimated by considering the energy loss of the particles as they pass through shielding (Adams, 1982).

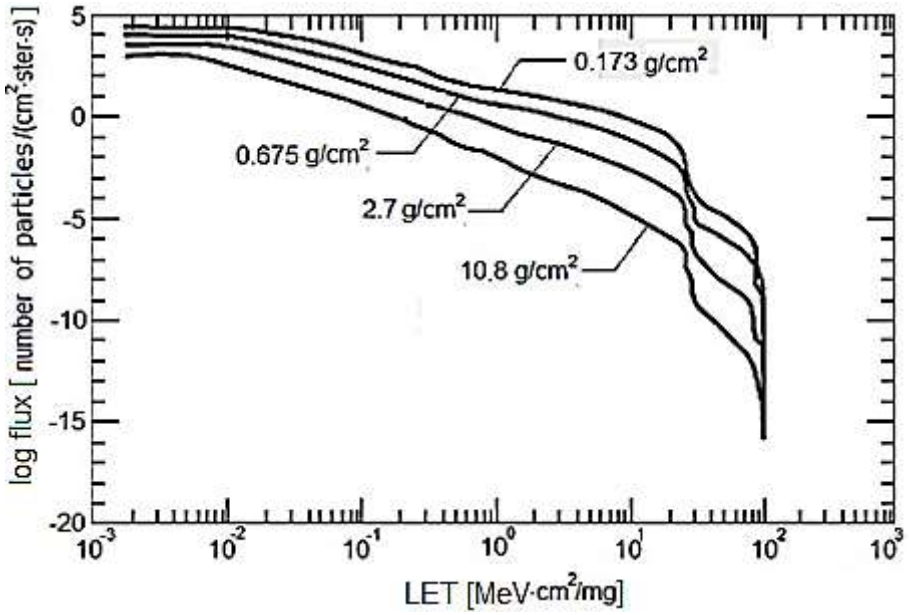


**Figure 2-11: Aluminium shielding effects on the attenuation of the flux from a large solar flare as a function of the LET of the incident particles (Adams, 2013)**

The amount of energy loss as a particle passes through shielding depends on the thickness of the material. Typical spacecraft shielding is in the range of 100 to 250 mils.

Figure 2-11 is a plot of the log of flux for a large solar flare versus linear energy transfer (LET) for an aluminium thickness ranging from 0.173 to 10.8 g/cm$^2$. Increasing the aluminium thickness, results in a decreased solar flare flux for particles with a relatively low energy level. However, the quantitative variation in flux with LET is relatively unaffected by the shielding for LETs above 30 MeV·cm$^2$/mg, increasing the shielding thickness from 0.17 g/cm$^2$ to 10.8 g/cm$^2$ reduces the intensity of the spectrum by five orders of magnitude (Adams, 2013). The effect of the thickness of the outer shell of a spacecraft the flux from galactic cosmic rays is shown in Figure 2-11; it takes more shielding to reduce the radiation intensity inside the spacecraft

as caused by galactic cosmic rays, to acceptable levels, than is the case for solar flare radiation.

When the outer wall of a spacecraft is made from aluminium with a thickness up to 10 g/cm$^2$, the LET spectrum is only slightly affect. By comparing Figure 2-11 and Figure 2-12, we conclude that spacecraft shielding can attenuate the low energy nuclei from a solar flare, however, it has fairly effect on the attenuation of nuclei in the galactic cosmic ray spectrum. Thus, for best practical thickness, additional shielding may prove effective against sensitive components of a solar flare environment, but it is relatively ineffective in reducing the galactic cosmic ray spectrum (Sexton, 1992).

Figure 2-13 is a plot of the contribution of proton, electrons and bremsstrahlung to the total dose received as function of aluminium thickness, after a period of 139 days as measured aboard the Explorer 55 spacecraft. The data were taken during a period of minimal solar activity. When the aluminium thickness is small, electrons and protons contribute to the total absorbed dose, while the contribution of bremsstrahlung is negligible. However, if the aluminium thickness is greater than 150 mils, only protons make a substantial contribution to the total dose; the contribution from electrons and bremsstrahlung becomes insignificant (Cliff et al., 1976).

Because of this, additional localized spot shielding near sensitive devices is sometimes used to reduce the total dose contribution from electron environments. However, increasing the shielding thickness from 100 to 250 mils of aluminium decreases the proton dose by less than a factor of two. Spot shielding is therefore less effective at mitigating the total absorbed dose in proton rich environment (Cliff et al., 1976).

Although these data are for specific satellite orbit, the trends indicated in Figure 2-13 are typical of those of other orbits (Cliff et al., 1976). To determine the total dose, one must include contributions from both electrons and proton. The dose rate may vary over a wide range; from $1\times10^{-6}$ to $0.5\times10^{-3}$ rad·s$^{-1}$ (Si) for a five year mission life. These dose rates correspond to a total dose range of less than 1 krad (Si) to more than 5 Mrad (Si).

For a Low earth orbit at a high inclination, 200 mils of aluminium shielding may limit the total proton dose to less than krad (Si) per year (Kaschmittr et al., 1996). In LEO and High inclination, the total doses results are several orders higher in magnitude. At altitudes corresponding to roughly 0.5 of the altitude of a geosynchronous orbit near worst case, the total dose that a device can receive inside a spacecraft with light shielding can approach 1 Mrad (Si) per year in a near-worst case situation (Stassinopoulos & Raymond, 1988).

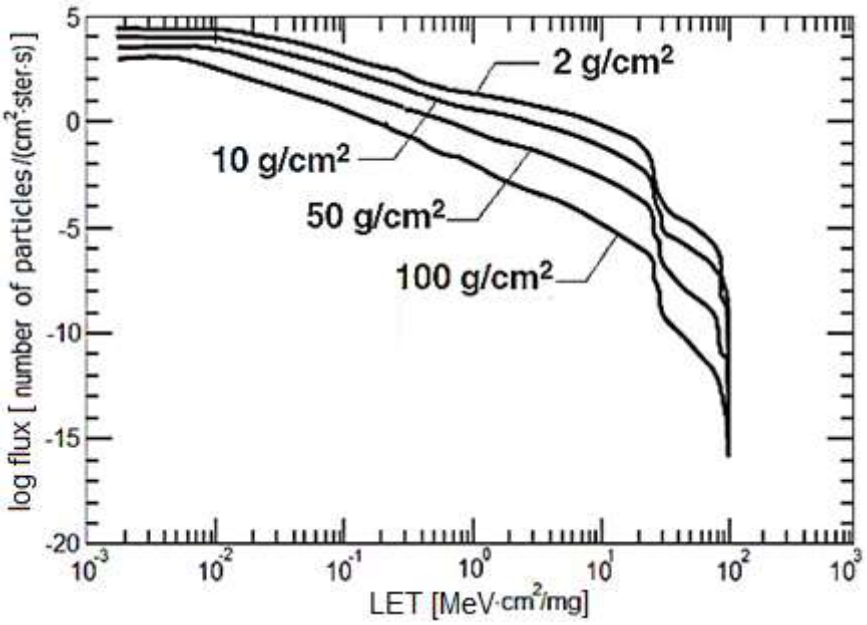


**Figure 2-12: Aluminium shielding effects on the attenuation of the flux from a galactic cosmic ray spectrum, as a function of the LET of incident particles (Adams, 2013)**

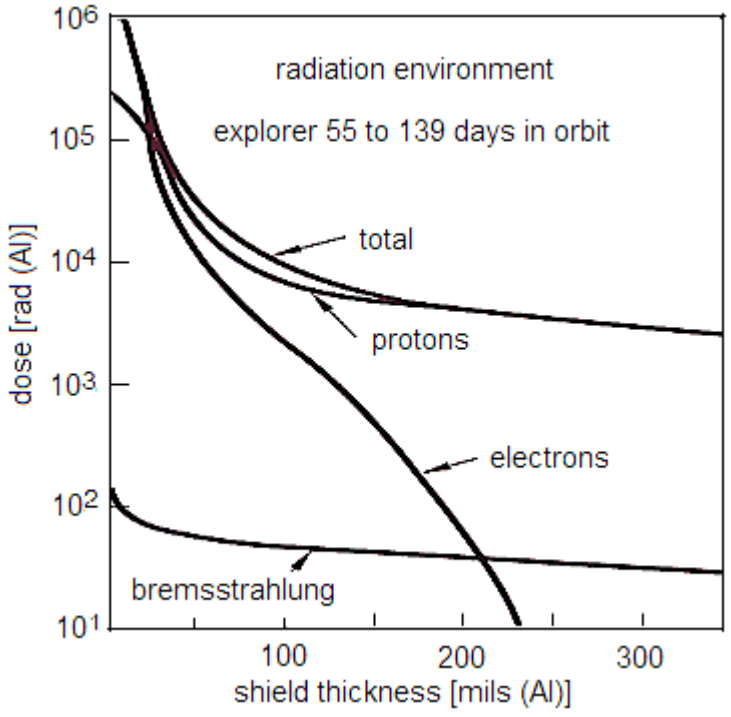


**Figure 2-13: Protons, electrons, and bremsstrahlung to total dose as a function of aliminium shielding (Cliff et al., 1976)**

### 2.10.1 Radiation effects on electronic devices

Photons and particles in a form of radiation may generate produce two types of effects on silicon components:

- Displacement damage;
- Ionizing effects.

According to Makozski (2006), radiation can modify the electrical parameters of a device, deteriorate its characteristics, and lead to the malfunction of the components or the whole system. Moreover, ionizing particles can produce photocurrents in active regions of the devices and provoke (single-event effects). The influence of the neutrons and protons radiation and their effects on silicon and silicon oxide, leading to the malfunctions in electrical components, as mentioned above, is set out in the Table 2.3 below.

High energy incident particles can interact with matter such as; silica and silicon. Mainly in three different ways (Napier et al., 2006);

- Ionization of the latter through the interaction with shell electrons,
- Nuclear reaction with the target nucleus,
- Displacement of atoms nucleus, assuming that the incident particle has enough energy.

**Table 2.3: Neutron and gamma radiation effects on silicon and silicon oxide (Makowski, 2006)**

| Radiation type | Energy range | Main type of interaction | Primary effects in Si and $SiO_2$ | Secondary effects in Si and $SiO_2$ |
|---|---|---|---|---|
| Photons | Low energy | Photoelectric effect | Ionizing phenomena | Displacement damage |
| | Medium energy | Compton effect | | |
| | High energy | Pair production | | |
| Neutrons | Low energy | Capture and nuclear reaction | Displacement damage | Ionizing phenomena |

The above-mentioned effects can be triggered by protons and electrons, all the phenomena can happen at the same time; such as the creation of the displacement damage may occur when an incident neutron collides with a nucleus, and a secondary effect is then initiated when this interaction produces a charged particle which causes ionization the material, assuming that the secondary particle has enough energy.

However, photons, neutrons, gamma radiation, high-energy particles, or charged particles have high-energy and thus the first predominates. High-energy and charged particles cause the ionizing dose effect to predominate (Grasser, 2014); therefore, only a small fraction of their energy is utilized for displacement damage.

On the other hand, the neutron particles are mainly responsible for displacement damage or displacement cascades; when a high-energy particle interacts with matter, some of energy is consumed by the ionizing process and the other part by displacement damage (Makowski, 2006). One can define stopping power, *S* of a particle as the rate of energy loss along the normalised path to the material density; see the Equation 7 below.

$$S = \frac{1}{\rho}\frac{dE}{dR} = NIEL + IEL \tag{7}$$

Where $\rho$ is the mass density of the interacting material; $\frac{dE}{dR}$ is the rate of energy loss along the path; $NIEL$ corresponds to non-ionizing energy loss and $IEL$ stand for ionizing energy loss; $NIEL$ is usually expressed as normalised effect of equivalent 1 MeV neutrons (Belousov, 2014).

### 2.10.2 Materials

Materials have to be lightweight and conduct electricity, since space radiation induces potential energy and charge accumulation in the satellite electronics. Different types lightweight conductive metals are commonly used for CubeSats structures. In this research the focus will be on aluminium. The California Polytechnic State University, San Luis Obispo (2009), writes a year report with updated the basic standard for CubeSats design and integration (CalPoly, 2013). They establish general rules governing materials, such as:

- No hazardous material shall be used in a CubeSat.
- All CubeSats should comply with the following requirements regarding out-gassing, total mass loss shall be less than 0.1%, and collection volatile condensable material shall be less than 0.1%.

Composite materials are made of two or more materials, with dissimilar physical and chemical properties. The main advantage of composites is that they can be designed for the requirements of a mission. Composite materials are usually made of a matrix material and a reinforcing material. The material used for the matrix is usually a cured resin that encapsulates a reinforcing material, usually carbon fibre.

Cyanate ester resin exhibits suitable performance characteristics for space applications due to low moisture absorption, low micro-cracking, and low out-gassing (KIZILÖREN, 2014).

### 2.10.3 Aluminium

Over the past 4 years aluminium has been the most common material used for the construction of small satellite missions. Aluminium offers reliability and lightweight support at a relatively low cost. It is thermally and electrically conductive, chemically resistant. In terms of strength, aluminium is equal to the other metals if reinforced at low temperatures (Texas, 2003). Table 2.4 and Table 2.5 show the characteristics of a few examples of different aluminium alloys used in previous satellite missions.

**Table 2.4: Aluminium structures used in the recent mission**

| Mission | Materials | Launch Date |
|---|---|---|
| EST-1 | Aluminium AW 6061-T6 and AW 7075 | 2013 |
| PROBA-V | Aluminium AA2024-T3 and Aluminium AA 7075-T7351 | 2013 |
| e-St@r | Aluminium 5005H16 | 2012 |
| Techedsat | Aluminium 6061 | 2012 |
| Hermes | Aluminium 7075-T73 | 2011 |

**Table 2.5: Properties of various aluminium types**

| Aluminium type | Density [g/cm$^3$] | Modulus of elasticity [Ga] | Fatigue strength [MPa] | Ultimate tensile strength [MPa] | Thermal conductivity [W/m.K] | Electrical resistance [Ω.cm] |
|---|---|---|---|---|---|---|
| 2024-T3 | 2.78 | 73 | 138 | 483 | 121 | $5.82 \times 10^{-6}$ |
| 7075-T73xx | 2.81 | 72 | 150 | 505 | 155 | $4.30 \times 10^{-6}$ |
| 5005-H16 | 2.70 | 69 | N/A | 180 | 205 | N/A |
| 6061 | 2.70 | 69 | 62.0 | 124 | 180 | $3.66 \times 10^{-6}$ |

### 2.10.3 Other Materials

- Titanium has positive attributes such as a high corrosion resistance, a low thermal expansion coefficient, as well as. However, it is it is complex to manufacture and is 60% heavier than aluminium (Cohen et al., 2014).
- Steel offers a low stiffness to density ratio, a large strength range, and good ductility. Unfortunately it is much too heavy; it has a density which is almost twice that of titanium (Cohen et al., 2014).
- Based on its high stiffness-to-mass ratio and its high thermal conductivity, beryllium appears to be a viable option. Although beryllium is lighter than aluminium, it is much more brittle, making it very expensive and time-consuming to machine. In addition beryllium, particles are toxic; driving manufacturing costs even higher (Cohen et al., 2014).

### 2.10.4 Interaction of radiation with materials

Semiconductor devices and integrated circuits of electronic systems used in nuclear power plants, spacecraft, high-energy physics experiments, advanced medical equipment, and in nuclear weapons, can potentially be exposed to extreme environments.

X-rays, gamma-rays, high-energy electrons, protons, neutrons, and cosmic ray ions all affected the operation of semiconductor electronics and lead to effects that may vary from graceful degradation of operating characteristics, to catastrophic failure (Cressler & A, 2013).

The total ionizing dose is the cumulative damage caused by ionizing radiation over the time of exposure. Ionizing radiation creates electron-hole pairs in the semiconductor and insulating materials used in devices, leading to transient effects and long term effects. These effects are produced by charge trapping in dielectrics that alter electric fields, setting up leakage paths, and changing threshold voltages (Gaylord & Ballantine, 2003).

Single-event effects result when a high-energy particles travel through a semiconductor leaving an ionized track behind. The movement and collection of this charge can cause effects ranging from a bit-flip, to latch-up, to catastrophic burnout (Peterson, 2011).The problem in which different types of radiation particles interact with materials and the effects of this interaction on electronic components may vary considerably. Dissimilar levels of radiation-induced degradation can be expected when a material is irradiated. The severity of irradiation will depend on the particle composition and fluence of the radiation, as well as the exposure duration to the radiation (Schwank et al., 2008).

### 2.11 Gamma ray and X-ray ionizing radiation interaction

X-rays and gamma-rays are used routinely for hardness assurance testing and process development. As X-rays or gamma rays collide with a material, they generate electron-hole pairs in the material by ionization. Because of high-energy of both gamma rays and X-rays, they can generate hundreds to thousands of electrons-hole pairs. With the net charge of X-ray or gamma ray exposure, it generates a photocurrent which affects the direct degradation of the dose rate and total dose in the electron-hole pair. Photons interact with a material through three different processes, namely; the fluorescent effect, the Compton-effect, and electron-hole pair formation (McLean & Oldham, 1987).

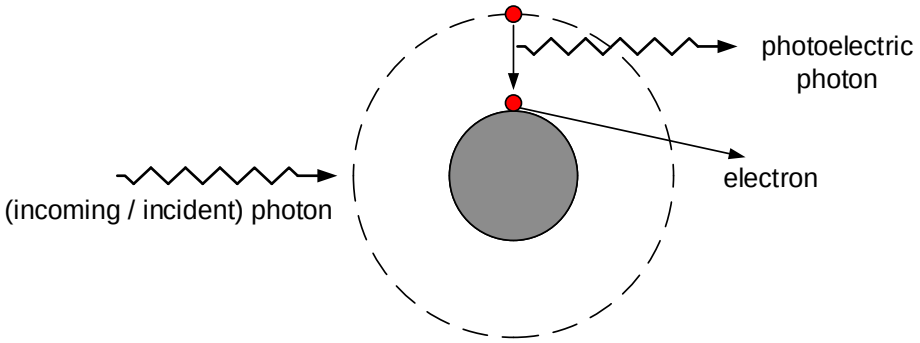


**Figure 2-14: Photon interaction with materials–photoelectric effect**

**(Schwank et al. 2008)**

Low-energy photons interact with materials predominately through the photoelectric effect. The photoelectric effect is illustrated in Figure 2-14. In this process, an incident photon excites an electron from an inner shell of a target atom, to an energy state high enough for it to be freed from the target atom. The incident photon is completely absorbed, thus photoelectric effect is emitted, and an electron in outer orbit of the atom will fall into the spot vacated by the electron causing a low-energy photon to be emitted. In general, the emitted low-energy photon does not have sufficient energy to create additional electron-hole pairs, but depending on energy of the incident photon, the emitted electrons can generate numerous additional electron-hole pairs (Schwank et al., 2008).

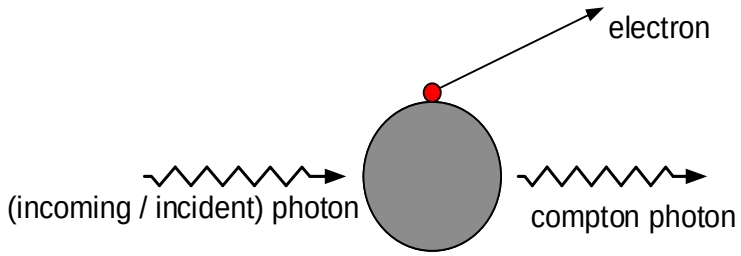


**Figure 2-15: Photon interaction with materials–Compton scattering**

**(Schwank et al., 2008)**

For higher energy photons, Compton scattering (shown in Figure 2-15.) will dominate over the photoelectric effect. In this process, as an incident photon collides with an atom, it transfers a fraction of its energy to an electron of the target atom, giving that electron sufficient energy to be dislodged from target atom. In the process of Compton scattering, a photon of lower energy is created which is free to interact with other target atoms.

Compton scattering can also create a free electron and ionized atom. Electron-hole pair formation occurs when the high energy photons collide with the target atom: the energy would typically be above 3 MeV (Muhammed & Zengin, 2012).

In pair production (shown in Figure 2.16), an incident photon collides with a target atom, creating an electron-positron pair. A positron has the same properties as an electron, except that the charge is positive; the incident photon is completely annihilated in pair production.

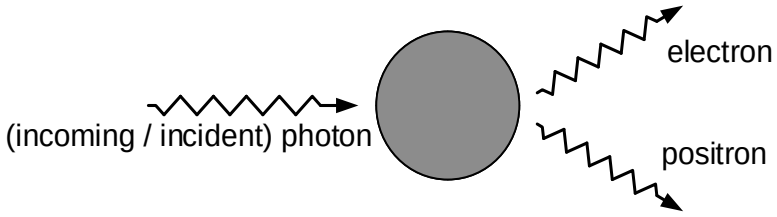


**Figure 2-16: Photon interaction with materials–pair production (Schwank et al., 2008)**

### 2.11.1 Cumulative effects

Exposure to radiation produces relatively stable, cumulative charges in device and circuit characteristics, which may result in parametric degradation or functional failure. The TID primarily impacts insulating layers, which may trap a bulk charge or develop interface traps at the contact plane with a semiconductor material. Non-ionizing energy losses result in displacement damage, and defects in the insulator and semiconductor region (Cressler & A, 2013).

In older technologies, these effects were well described by a spatially uniform representation of the cumulative amount of energy deposited. The accuracy of this description relies on the relatively large sizes of the devices, in relation to the average the energy deposited by individual particles or photons; or photons: current-day devices are much smaller (Cressler & A, 2013).

### 2.11.2 Transient effect

While the total dose hardness of commercial integrated circuits has generally improved in recent years, primarily because of reductions in gate oxide thicknesses and increases in doping densities, reduced device dimensions and the accompanying technological changes have resulted in increased sensitivity to transient radiation effects (Dodd, 2003).

Single event effects are a serious problem for electronics operated in space and they are becoming an issue for advanced technologies in avionics, and even at sea level. The charge deposited by a single ionizing particle can produce a wide range of effects. In general, the sensitivity of a technology to SEEs increases as device dimensions decrease and as circuit speed increases. These effects can be produced by direct ionization or by secondary particles resulting from nuclear reactions or elastic collisions (Dodd et al., 2004).

In a high dose rate environment, energy is generated relatively uniformly throughout the semiconductor device or integrated circuit. The resulting photocurrents produce effects that include rail span collapse, cell upset, and burnout of metal lines. Depending on system requirements, it may be possible to circumvent these effects by temporarily removing power (Massengill et al., 1986).

### 2.12 Power devices

When considering the power of the semiconductor devices, it must remember in mind that the device is essentially used as a switch. The goal is to develop an ideal switch, a switch which: has zero resistance when conducting, a zero leakage current (infinite resistance) when ‘off’, an ability to block an infinite voltage, switches instantaneously ‘on’ and ‘off’. The power switch is characterized by its ‘on’-state resistance, voltage drop, blocking voltage in the forward and reverse bias, leakage current when ‘off’, and the speed with which it can be turn ‘on’ and ‘off’ due to the intrinsic capacitance in the device (Cressler & A, 2013). To understand power devices for space application, a basic understanding of wide band-gap technologies is required. Accordingly, the two principal material systems, gallium nitride (GaN) and silicon carbide (SiC), will be briefly discussed in the next section.

#### 2.12.1 Wide band-gap

The energy required to excite a charge carrier from the valance band to the conduction band is a band-gap. The wide the band-gap of the material used in the power component, the more it becomes sensitive to radiation and heat; this heat causes the electric field to excite the carrier of the band-gap. The wider band-gaps of SiC and GaN; translate into a higher blocking voltage, lower conduction losses; lower switching losses, lower leakage current, and higher temperature operation. Additionally, the wide band contributes as well to the fast switching speed of SiC devices (Tang et al., 2010).

### 2.12.2 Gallium Nitride Power Device

Gallium nitride devices have been made on a variety of substrate implies a base or starting level in an effort to find the most suitable quality GaN substrates for use in devices. As a result, GaN devices can be built on silicon substrates, silicon carbide substrates, and on sapphire (Tang et al., 2010).

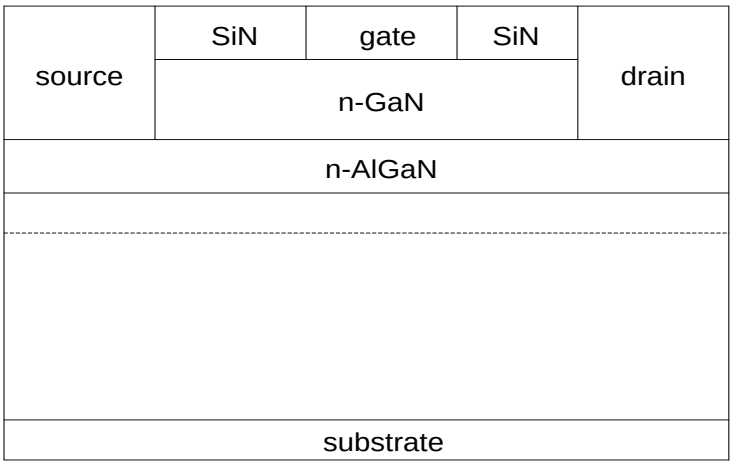


**Figure 2-17: Cross sectional structure of GaN high electron mobility transistor**

Another characteristic of a GaN device is that it is fixed in a lateral position in relation to unlike SiC power devices which are mounted vertically. The desirable carrier transport behaviours are achieved when a two-dimensional electron gas is formed in a quantum well within the device structure. This combination occurred in devices such as high electron mobility transistors (HEMTs), as shown in Figure 2-17. As a result, these devices do not possess the large blocking voltages found in vertical devices. The operating voltage range of GaN devices is from 200 V to 600 V (Zhang et al., 2001).

### 2.12.3 Silicon Carbide Power Devices

Silicon carbide power devices have received a substantial amount of attention from the research community recently. This material is potentially promising for high voltages, high-power density, and efficiency. With the improvement in the quality of wafer material being achieved by Cree and others, the density defects are steadily declining; as a result, devices with larger areas can be constructed. With this expanded size comes an increased current rating of the individual die. State-of-the-art for the largest area is about 1 cm x 1 cm, which corresponds to a 100 A die for power switching applications.

The continuous current rating is typically set at a current density of 100 A/cm$^2$ even though SiC could operate at higher current densities (Cressler & A, 2013).

### 2.12.4 Metal-oxide-semiconductor field-effect transistors (MOSFETs)

In general, the MOSFET is a workhorse device in electronics. In electronics, and is available as an n-type or a p-type. The n-type MOSFET consists of a source and a drain, two highly conductive n-type semiconductor regions, which are isolated from the p-type substrate by the reversed biased p-n diode. A metal or polycrystalline gate covers the region between source and drain. The gate is separated from the semiconductor by the oxide (Honda & Adams, 2005). The basic structure of the n-type MOSFET and the corresponding symbols is shown in Figure 2-18.

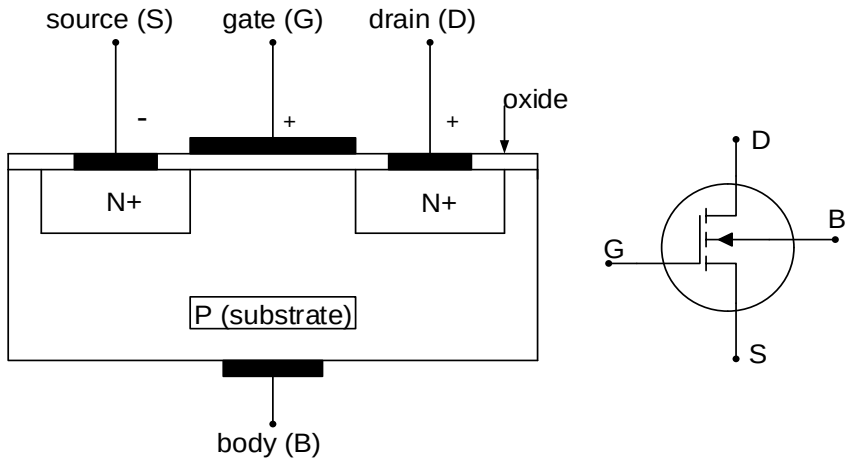


**Figure 2-18: Cross-section and circuit symbol of an n-type metal-oxide-semiconductor field-effect transistor (Honda & Adams, 2005)**

It can be seen on the figure above that the source and the drain regions are identical. Applying a voltage to the drain of the MOSFET, electrons are set free which link the drain and source pins (Zeghbroeck, 2011).

### 2.12.5 Structure and principle of operation

The plan view of the MOSFET is shown in Figure 2-19, where the gate length and gate width are indicated. Note that the gate length does not equal the physical dimension of the gate, but rather the distance between the drain and the source regions underneath the gate. The overlap of the gate onto the both the source region and the drain region, is required to ensure that the inversion layer forms a continuous conducting path between these two regions. Technically this overlap is made as small as possible in order to minimize the parasitic capacitance effect (Boulder, 2004).

The voltage applied to the gate, controls the flow of electrons from the source to drain. A positive voltage applied to the gate attracts electrons to the interface between the gate dielectric and the semiconductor. These electron forms a conducting channel called the inversion layer. No gate current is required to maintain the inversion layer at the interface since the gate oxide blocks any carrier flow. The result is that the applied gate voltage controls the current between the drain and the source (Zeghbroeck, 2011). Typical current versus voltage characteristics of a MOSFET can be seen in Figure 2-20.

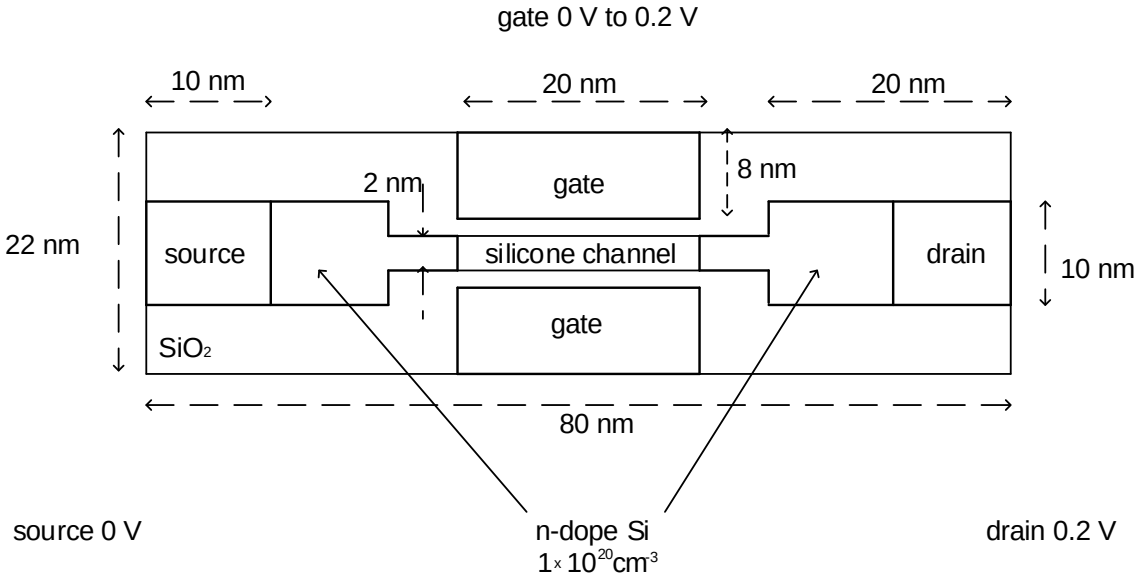


**Figure 2-19: Top view of a metal-oxide-semiconductor-field-effect-transistor re-draw (Honda & Adams, 2005)**

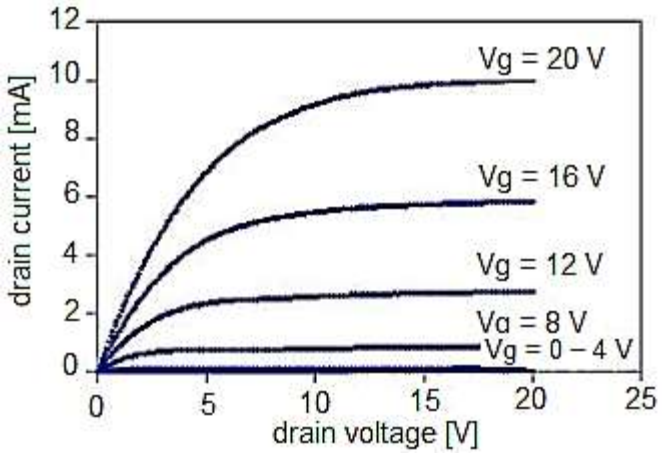


**Figure 2-20: I-V characteristics of a MOSFET (Zeghbroeck, 2011)**

### 2.12.6 Analysis of the metal-oxide-semiconductor field-effect transistors

There are three different models for the MOSFET to be analysed; the linear model, the quadratic model and the variable depletion layer model. The linear model correctly predicts the behavior of a MOSFET for small drain source voltages, where the MOSFET acts as a variable resistor. For the quadratic model, the voltage varies between the source and the drain along the channel; this model is often used notwithstanding that the variation of the depletion layer charge is ignored. The variable depletion layer model is more than the other two models, complex as it includes the variation of the depletion layer along the channel (Spirito et al., 2002).

### 2.12.7 Linear model of the MOSFET

The linear model describes the behaviour of a MOSFET biased with a small drain to source voltage. As the name suggests, in the linear model the MOSFET acts as a linear device. To be more specific, the MOSFET can be modelled as linear resistor with the resistance is modulated by the gate to source voltage. In this manner, the MOSFET may be used as a switch for analogue and digital signals, or as an analogue multiplier (Cabiluna et al., 2013).
The general expression for the drain current, $I_D$ is given by Equation 8, and equals the total charge in the inversion layer, divided by the time needed for the carrier to flow from the source to the drain:

$$I_D = -\frac{Q_{inv} W L}{t_r} \tag{8}$$

where $Q_{inv}$ the inversion layer charge per unit area
$W$ is the gate width
$L$ is the gate length and $t_r$ is the transit time

If the velocity of the carrier is constant between the source and the drain, the transit time is equals to:

$$t_r = \frac{L}{v} \tag{9}$$

Where: $v = \mu\epsilon = \mu\frac{V_{DS}}{L}$
$\mu$ is the mobility
$\epsilon$ is the electric field
$V_{DS}$ is a drain-source voltage

The constant velocity implies a constant electric field so that the field equals the drain-source voltage, divided by the gate length. This leads to the following expression for the drain current:

$$I_D = -\mu . Q_{inv} . \frac{W}{L} V_{DS} \tag{10}$$

We now assume that the charge density in the inversion layer is constant between source and drain.

$$Q_{inv} = -C_{OX}(V_{GS} - V_T), \qquad \text{for } V_{GS} > V_T \tag{11}$$

The inversion charge is zero if the gate voltage is lower than the threshold voltage. Replacing the inversion layer charge density in the expression for the drain current yields the linear model:

$$I_D = \mu C_{OX} \frac{W}{L}(V_{GS} - V_T)V_{DS}, \qquad for\ |V_{DS}| \ll (V_{GS} - V_T) \tag{12}$$

Note in the equation above, the capacitance is the gate oxide capacitance per unit area. Also, the drain current is zero if the gate-to-source voltage is less than the threshold voltage. The linear model is valid if the drain-to-source voltage is smaller than the gate-to-source voltage minus the threshold voltage. This insures the velocity, the electric field and the inversion layer charge density is indeed constant between the source and the drain (Boulder, 2004). An example of the linear current-versus-voltage (*I-V*) characteristics of a MOSFET is shown in Figure 2-21.

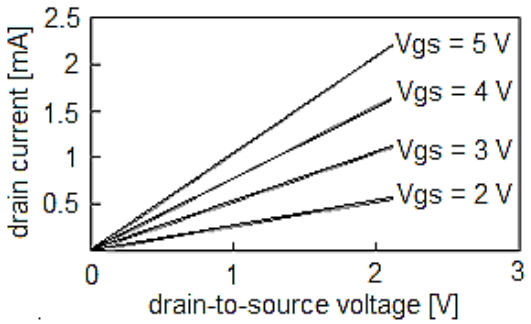


**Figure 2-21: Linear I-V characteristics of a MOSFET with $V_T$ = 1 V (Zeghbroeck, 2011)**

### 2.12.8 Quadratic model

The quadratic model uses the same approach as the linear model. This model allows the inversion layer charge to vary between the source and the drain. The derivation is based on the fact that the current is continuous throughout the channel (Boulder, 2004). Also, the current is related to the local channel voltage, $I > V_C$.

Consider a small section within the device (MOSFET) with a width $dy > I$ and channel voltage $V_C + V_S$ the linear equation describes in Equation 12 Applies:

$$I_D = \mu C_{OX} \frac{W}{dy} (V_G - V_S - V_C - V_T) dV_C \tag{13}$$

With the drain-to-source voltage being substituted by the channel voltage; The left-hand and right-hand sides of the equation could be integrated from the source to the drain, with y varying from 0 to the gate length (L), and the channel voltage varying from 0 to the drain-source voltage ($V_{DS}$) (Zeghbroeck, 2011).

$$\int_0^L I_D dy = \mu C_{OX} \frac{W}{dy} \int_0^{V_{DS}} (V_G - V_S - V_C - V_T) dV_C \tag{14}$$

With the drain current ($I_D$) constant, and the integration of Equation 15 yields:

$$I_D = \mu C_{OX} \frac{W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right], \qquad for\ V_{DS} < V_{GS} - V_T \tag{15}$$

Figure 2.22 below displays the typical current versus voltage characteristics of the MOSFET quadratic model; the relationship between the drain voltage and the drain current is given for differing gate-to-source voltages.

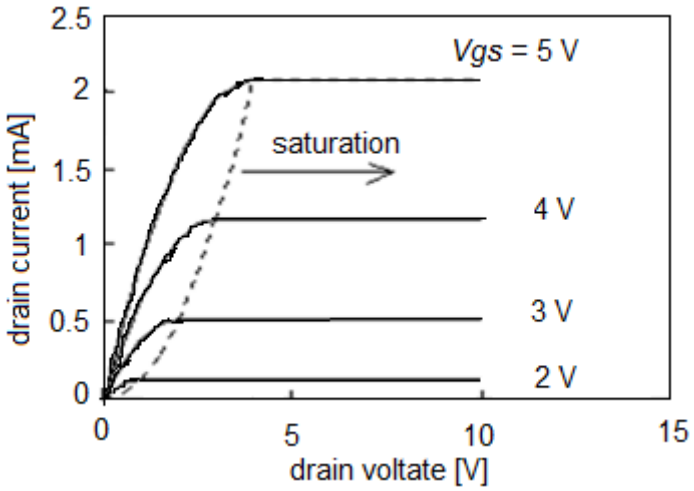


**Figure 2-22: Current to voltage characteristics of the quadratic model (Zeghbroeck, 2011)**

### 2.12.9 Variable depletion layer model

The variable depletion layer model includes the charge variation in the depletion layer between the source and the drain of the MOSFET (Boulder, 2004). This variation is cause by the voltage variation along the channel. The inversion layer charge is given by:

$$Q_{inv} = -C_{OX}(V_{GS} - V_T), \qquad for\ V_{GS} > V_T \tag{16}$$

Including the implicit dependence of the threshold voltage on the charge in the depletion region, thus:

$$V_T = V_{FB} + V_C + 2\phi_F + \frac{\sqrt{2\epsilon_S q N_a (2\phi_F + V_{SB} + V_C)}}{C_{OX}} \tag{17}$$

The difference between the voltage within the channel and the source voltage is the$V_C$. By applying the linear model to a small section with thickness $dy$, at a distance 'y' from the source Equation 18 can be derived; at 'y' the voltage equals $V_C + V_S$ while the voltage across that section equal$dV_C$. This result in the following expression for the drain current (Zeghbroeck, 2011):

$$I_D = \mu_n C_{OX} \frac{W}{dy}\left(V_{GS} - V_{FB} - 2\phi_F - V_C - \frac{\sqrt{2\epsilon_S q N_a (2\phi_F + V_{SB} + V_C)}}{C_{OX}}\right) dV_C \tag{18}$$

Integrating both sides from the source to the drain with 'y' varying from 0 to the gate length (L); and the channel voltage$V_C$varying from o to the drain-source voltage yields:

$$I_D = \frac{\mu_n C_{OX} W}{\boldsymbol{L}} \left( V_{GS} - V_{FB} - 2\phi_F - \frac{V_{DS}}{2} \right) V_{DS} - \frac{2}{3} \mu_n \frac{W}{L} \sqrt{2\epsilon_S q N_a} \left( (2\phi_F + V_{DB})^{3/2} - (2\phi_F + V_{SB})^{3/2} \right) \quad (19)$$

### 2.12.10 Degradation of the MOSFET parameters due to radiation

Ionizing radiation effects are responsible for the charge building-up at silica and interface. This charge build-up results in the alteration of a few important electronic parameters of the MOSFETs. The threshold voltage is one of the important parameters of a MOSFET and it is susceptible to mutation by ionizing radiation (Figure 2-23). Other parameters are affected by gamma radiation (Grasser, 2014; Makowski, 2006). As listed by Makozski (2006), listed them as follows:

- A decrease of transconductance,
- An increase of leakage currents,
- A reduction of drain-source breakdown voltage,
- A deterioration of noise parameters,
- A reduction in surface mobility,
- An increase of the surface recombination velocity.

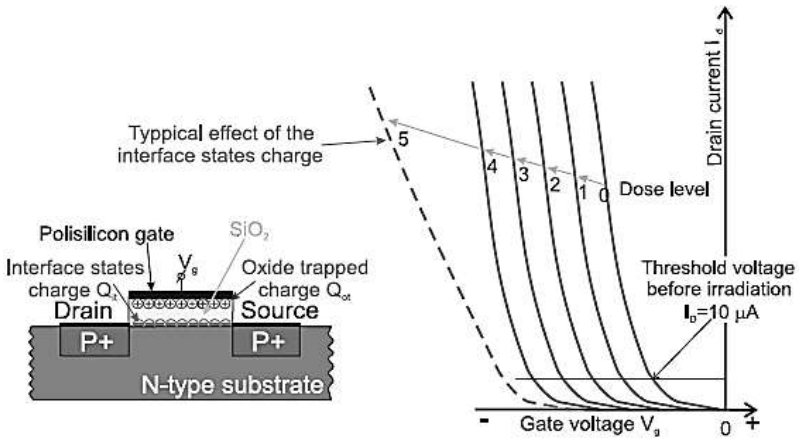


**Figure 2-23: Oxide and oxide-silicon trapped charges in NMOSFET along with the I(D ) and V(D) curves reflecting shifts in the threshold voltage (Adams & Holmes, 2004)**

### 2.12.11 Threshold voltage shift for the MOSFET

The change in the threshold voltage for the MOSFET substantially depends on electric field in the silicon oxide (Barnes et al., 1992; Makowski, 2006). Therefore, the biasing voltage of the transistor has a significant influence for generated and trapped charges; for example, the positively charged build up can be attracted to a negative biased gate electrode (see Figure 2-23and Figure 2-24). A charge generated by ionizing radiation results in a threshold voltage shift; this shift can be expressed as the sum of two voltage changes (Makowski, 2006) caused by the increase of charge in the silica, $Q_{ot}$ and the interface trapped charge, $Q_{it}$ Equation 20 below.

$$\Delta V_{th} = -e\frac{1}{C_{OX}}.\Delta N_{ot} \pm e\frac{1}{C_{OX}}.\Delta N_{it} \quad (20)$$

where $e$ is an elementary charge

$C_{OX}$ is an oxide capacitance expressed per unit area,

$\Delta N_{ot}$ and $\Delta N_{it}$ are densities of oxide trapped charges

and interface states, respectively

The voltage shift caused by the modification of interface states can be positive for PMOSFET and negative for NMOSFET. Charge trapped in PMOSFET oxide and threshold voltage shifts are exemplified in Figure 2-23; the threshold voltage shift towards the negative gate voltage in accordance with the absorbed dose.

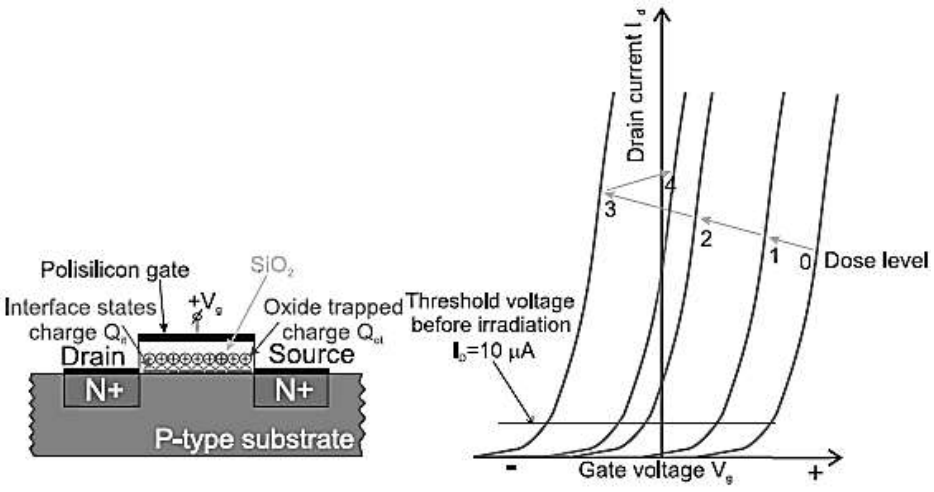


**Figure 2-24: Oxide-silicon trapped charges in PMOSFET along with the I(D ) and V(D) curves reflecting shifts in the threshold voltage (Adams & Holmes, 2004)**

## 2.13 Summary

This chapter presented the statistics of the status of the nanosatellite launched in the past 10 years. Different types of space orbit were mentioned, and a study of radiation sources and their effects inside the spacecraft was carried out. The modelling of the power devices in terms analogue, linear and quadratic model was highlighted in this chapter. The knowledge gained in this chapter leads to a better understanding the concepts of radiation effects in a space environment; and the functioning of electronic components used in the nanosatellite.

# Chapter 3 : OVERALL POWER CIRCUIT ARCHITECTURE

## 3.1 Introduction

This chapter discusses the literature study of the power system. Starting with the theoretical overview of photovoltaic cells; followed by modelling of photovoltaic cells. Also, online methods and offline methods of effecting maximum power point tracking techniques were investigated. Finally, a comparative study of the different battery technologies for nanosatellites, as well as direct energy transfer mechanisms, will be presented.

## 3.2 Photovoltaic cell technology

The conversion of electromagnetic sun radiation to electrical energy via the well-known photoelectric effect is termed a photovoltaic cell process. Photovoltaic cells may be configured in series or in parallel, increasing either the voltage or the current of the assemblage. An array is a group of multiple panels. The photovoltaic source has to be properly selected to provide a suitable electrical energy supply for charging batteries and meet: the power needs of all sub-systems during exposure to the sun; power form the batteries are sufficient to ensure that the satellite stays functional when it moves through the eclipse zone of its trajectory (Cupido, 2013).

There are many sources of electrical energy used on space applications such as, radio-isotope technology, nuclear power, fuel cells and solar dynamic power. However, in the case of nanosatellite, size and weight restrictions make photovoltaic cells the preferred renewable energy source (Maini & Agrawal, 2007; Cupido, 2013).

### 3.2.1 Theory of photovoltaic cell

The operation of photovoltaic cells is based on the photoelectric effect, and this effect happens when the photons of the electromagnetic radiation of the sun, strike a semiconductor material. These photons may reflect off surface of this material, and or they may be absorbed by the electrons in the crystal lattice of the material. Once the photons are absorbed and have energized the electrons in the crystal lattice structure of the material, these electrons can move about freely in the material ; prior to being energised the electrons were securely bound by covalent bonds (Maini & Agrawal, 2007).

The dislodged electrons leaving behind an electron hole; which could be filled by another electron of a close-by atom creating another electron hole. The electron-hole pairs move along the semiconductor material, driven by an electrostatic field created across the material or by

a gradient in the electrochemical composition. The movements of these electrons throughout the material produce a current that can be used to drive external loads (Cupido, 2013). The efficiency of the photovoltaic process decreases when the photons go straight through the crystal lattice. A comparison of the different photovoltaic cell technologies which are commercially available set out in Table 3.1.

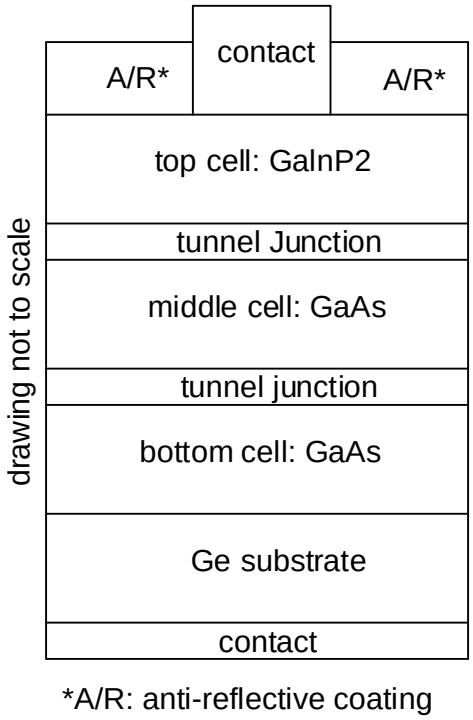


**Figure 3-1: Structure of generation triple junction photovoltaic cell (Spectrolab, 2010)**

Spectrolab and Emcore are manufacturers of photovoltaic cells such as Advanced Triple Junction (ATJ) and Next Triple Junction (UTJ) solar cells illustrated in Figure 3-1. It has a multiple layers of substrate, namely $GaInP_2$, GaAs and Ge, with two junctions between the different semiconductor materials. The different levels of substrate address the movement of photons straight though the photovoltaic cell by increasing the overall electron density of the photovoltaic cell, while the reflection of solar irradiance is prevented by anti-reflective coatings (Spectrolab, 2010).

**Table 3.1: Comparison of photovoltaic technologies (Spectrolab, 2010)**

| Company | Photovoltaic Description | Mass / unit area | Type | Min Efficiency | Dimension |
|---|---|---|---|---|---|
| Emcore | Triple-Junction Satellite Solar Cell | 84 mg/cm$^2$ | Germanium Triple Junction | 28.5% | 26.6 cm$^2$ x 140 µm (also custom available) |
| Emcore | Triple-Junction w/ Monolithic Diode | 84 mg/cm$^2$ | Germanium Triple Junction | 28.0% | 26.6 cm$^2$ x 140 µm (also custom available) |
| Emcore | Adv. Triple Junction (ATJ) | 84 mg/cm$^2$ | Germanium Triple Junction | 27.5% | 26.6 cm$^2$ x 140 µm (also custom available) |
| Emcore | Adv. Triple-Junction w/ Monolithic diode | 84 mg/cm$^2$ | Germanium Triple Junction | 27.0% | 27.5cm$^2$ x 140 µm (also custom available) |
| Spectrolab | Next Triple Junction (XTJ) Solar Cells | 84 mg/cm$^2$ | Germanium Triple Junction | 29.9% | Up To 60 cm$^2$ x 140 µm |
| Spectrolab | Ultra-Triple Junction (UTJ) Solar Cells | 84 mg/cm$^2$ | Germanium Triple Junction | 28.3% | Up to 32 cm$^2$ x 140 µm |
| Spectrolab | Improved Triple Junction (ITJ) Solar Cells | 84 mg/cm$^2$ | Germanium Triple Junction | 26.8% | Up to 31 cm$^2$ x 175 µm |

### 3.2.2 Model of photovoltaic cell

The photovoltaic cell can be modelled using the diagram depicted in Figure 3-2. The diagram is made of a current source ($I_{ph}$) used to represent the dislodging of electrons into the crystal lattice, the equivalent resistance of the photovoltaic cell is $R_s$ and $R_{sh}$ is a parallel shunt resistance. The source output current is directly proportional to the light coming from the cell (Barakati et al., 2009).

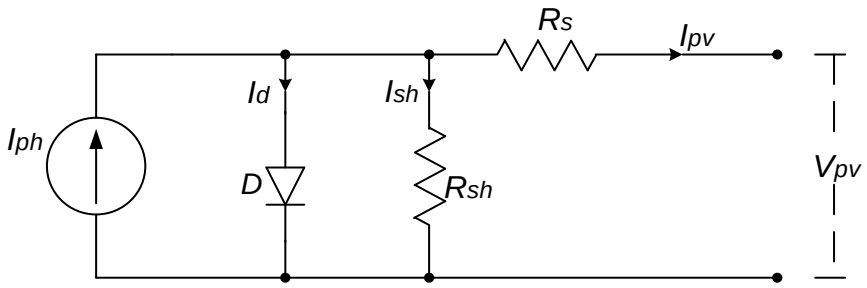


**Figure 3-2: Photovoltaic cell model**

$$I_{pv} = I_{ph} - I_d - I_{sh} \tag{21}$$

$$I_{pv} = I_{ph} - I_{sat}\, e^{\frac{q(V_O + I_{ph}R_s)}{nKT_{cell}N_s} - 1} - \left(\frac{V_o + I_{ph}R_s}{R_p}\right) \tag{22}$$

The photovoltaic cell data sheet of a particular commercial product may provide the information cell characteristics that can be visually displayed, using the suitable simulation software packages. The output current and voltage majorly depend on environmental temperature properties, and the illumination respectively. There are many manufacturers of photovoltaic cells, however, in this research work the focus will be on panel type MSX-64, marketed by SOLAREX (see Appendix C). The illustration of the photovoltaic cell variables (Figure 3-3) is an excerpt from the product data sheet of this panel (Figure 3-3).

By using different input parameters using PSIM software a characteristic graph of the MSX-64 panel was simulated, which was compared to a similar graph produced by the manufacturer. The result showed that, the output current of the photovoltaic cell is heavily dependent on the level of solar irradiance. It can be seen that the maximum current is achieved at the maximum solar irradiance; practically 1400 W/m$^2$ is taken to be representative of the level of irradiance that small satellite will experience in space environment, as illustrated in Figure 3-4. The current markedly reduces as the level of solar irradiance reduces; the photovoltaic output power will therefore tend to follow suit.

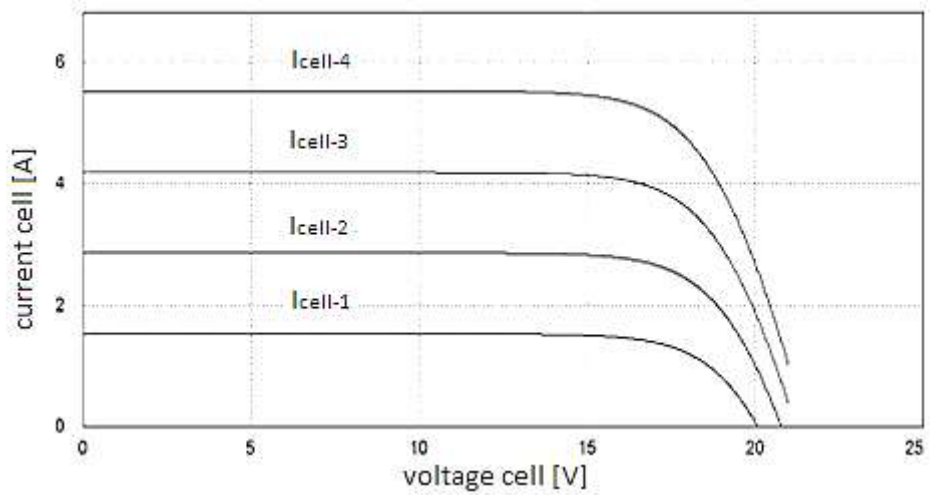


**Figure 3-3: Current and voltage characteristic at different irradiation values**

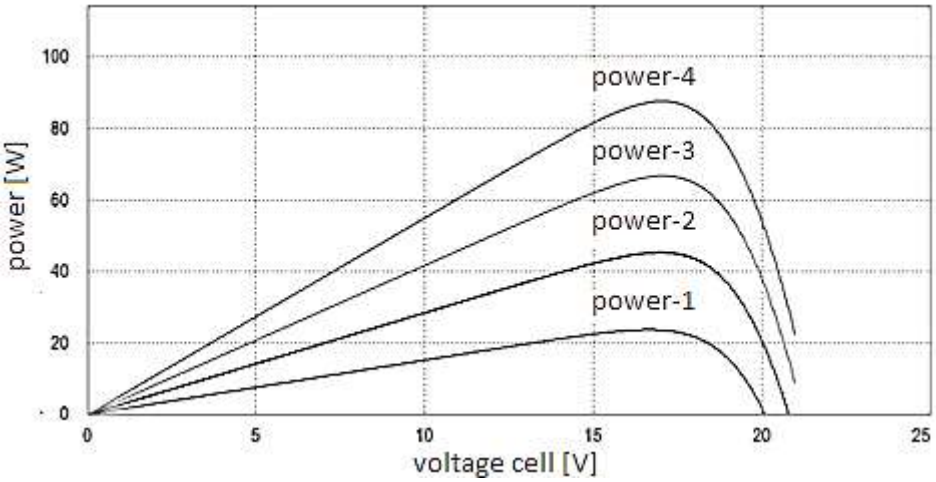


**Figure 3-4: Power and voltage characteristic at different irradiation values**

Regarding the space application for small satellites, the maximum voltage obtained at the different solar irradiance is 3. 92 V, highlighting that photovoltaic cells can be connected in parallel even when they are exposed to differing levels of solar irradiance. The changing temperature of space affects the output voltage and output power of the photovoltaic cell (Figure 3-5, Figure 3-6). Note that when the temperature of the photovoltaic cell increases, the output voltage and the power output decrease. This is a critical issue to mention as the temperature of the nanosatellite will be at the minimum value as soon as it faces the eclipse time and increase the maximum output power (Spectrolab, 2010).

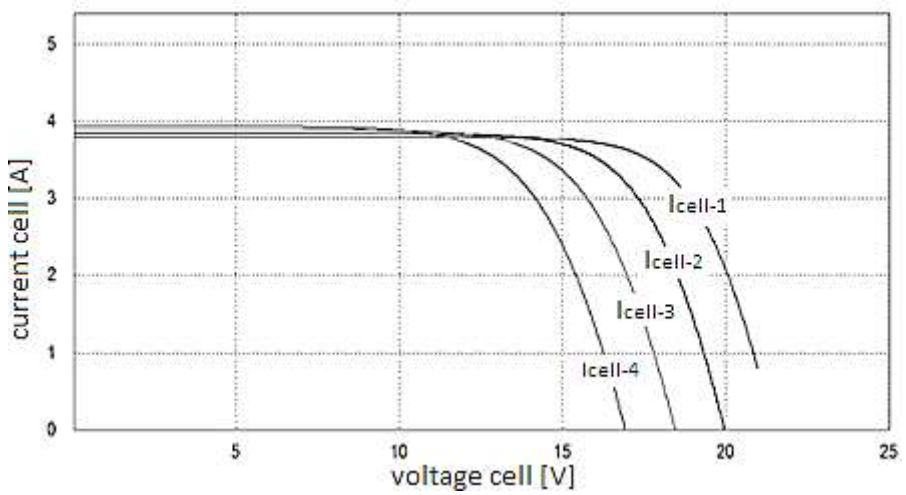


**Figure 3-5: current and voltage characteristic at different operating temperature**

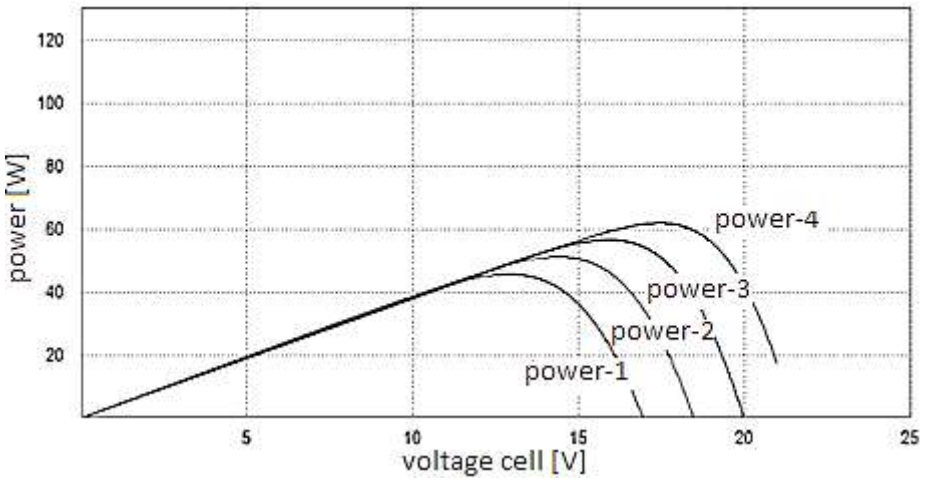


**Figure 3-6: Power and voltage characteristic at different operating temperature**

### 3.2.3 Another source of energy on spacecraft

Choosing a suitable battery technology to be used as a satellite power system is a critical point in the design procedure. The battery technology is selected in terms of weight, power limitations, and system size. To meet the standards for small-satellites, lithium-ion and Li-polymer battery technologies are rechargeable sources of choice; this is because of their small size, high volumetric energy densities, and high gravimetric energy densities (Cupido, 2013).

## 3.3 Comparison study of battery technologies

A comparative study of battery technologies is illustrated in Table 3.2; it is based on three battery technologies namely: lithium-ion (Li-Ion) and li-polymer (Li-Po), Nickel-Cadmium

(NiCd), and Nickel-Metal hydride (NiMH) batteries. It is shown that on the Table 3.2 below that the gravimeter and volumetric energy densities are higher for Li-Po batteries. Li-Ion batteries have a maximum 400 discharge cycles; this is on the assumption the depth of discharge (DOD) is 100%, which is not sensible as it drastically reduces the battery life cycle; the DOD is typically set at 20%. Battery capacity rating is commonly measured in milliampere-hour (mAh). In a small-satellite electrical power supply, the design of the power supply sub-system needs to be carefully considered. Because the power supply sub-system is the secondary power source of a small satellite, the calculation of the various currents and the overall number of cycles, have to be precisely known, so as to optimize battery lifespan (Cupido, 2013).

**Table 3.2: Comparison of battery technology (Cupido, 2013)**

| Type | NiCd | NiMH | Li-Ion, Li-Po |
|---|---|---|---|
| Nominal voltage [V] | 1.2 | 1.2 | 3.7 |
| Density of energy [W.h/L] | 140 | 180 | 200 |
| Density of energy [W.h/kg] | 39 | 57 | 83 |
| Maximum discharge current [C] | 20 | 4 | 2 |
| Charging time [min] | 15 | 30 | 60 |
| Thermal range for charging | 0 to +50 | 0 to +45 | 0 to +60 |
| Thermal range for discharge | -20 to +50 | -20 to +50 | 0 to +50 |
| Resistance against overcharging | Low | Low | Middle |
| Cathode material | NiOOH | NiOOH | LiPO |
| Anode material | Cd | Alloy | C |
| Max. number of cycles | 1000 | 500 | 400 |

To optimally charge the selected battery, a battery charger has to be chosen to fulfil the charging condition. The battery charger should take the chemical structure of the battery into account and must have the ability to detect the state-of-charge (SOC) of the battery.

Because of their different chemical structures, battery types like; Li-Ion, Ni-Cd, and Ni-MH, each require their unique charging regimen and to avoid their decreasing capacity, have to be fully discharged before the beginning of the charging process.

While lithium-ion batteries are being charged require application of constant current and constant voltage to reach a fully-charged state while having no issue regarding the memory effect (McLaren et al., 2008).

### 3.3.1 Lithium-Ion and Li-Polymer voltage Level

In the charging procedure, the charger must be able to identify the full-charged state. If not able to distinguish this condition (see Figure 3-7), the charger will keep on running a current through even after it has reached the fully-charge condition; in such a situation it is likely that damage to the battery will result (Cupido, 2013).

It can be seen that the Lithium-Ion battery loses its stability at a voltage above 4.3 V and also at a voltage lower than 2.0 V (see Figure 3-7); to enhance battery life, charging must be initiated between the upper charge voltage and the end voltage, which is between 4.2 V and 2.8 V on Figure 2.12. Starting the charging process outside the range mentioned above. Will decrease the capacity of the battery (Cupido, 2013), the protection circuit of a single Lithium-ion battery or multi-connected Lithium-ion batteries is built around MOSFETs. Can be implemented either in common source, common drain, n-channel series connected with negative electrode, or p-channel series connected with positive electrode conditional on the application. The operation of this protection circuit takes place when the voltage is into the unstable zones. The charging techniques applied to charge the lithium-ion and li-polymer batteries are the constant-voltage, and constant-current techniques (Liu & Jen-Hao, 2006).

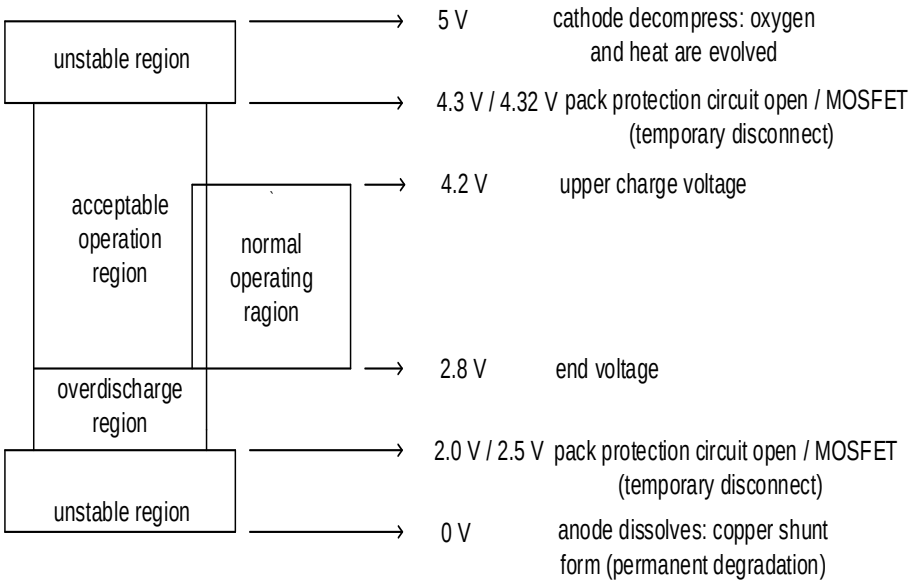


**Figure 3-7: Lithium-ion battery; regions of operation block diagram (Microchip, 2004)**

### 3.3.2 Direct energy transfer (DET)

The direct energy transfer networks are the shunt regulated networks into which extra energy generated by the photovoltaic arrays is off-loaded via the resistor banks. There are therefore, no active components online between the satellite load and the photovoltaic arrays. The depicted Figure 3-8 and Figure 3-9 show the direct energy transfer networks with a regulated and unregulated bus voltage (Patel, 2005).

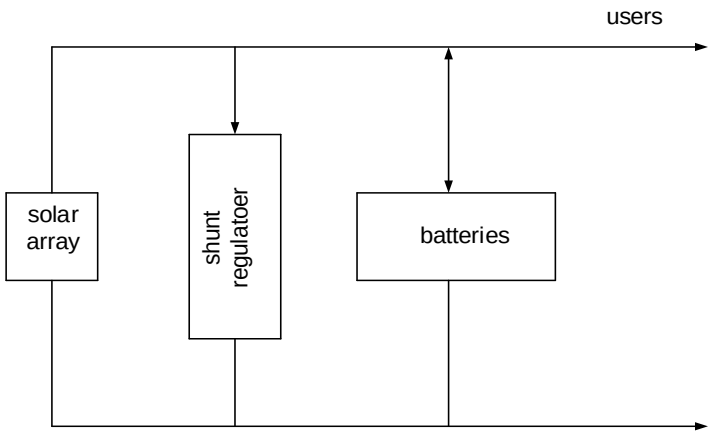


**Figure 3-8: Unregulated direct energy transfer (Cupido, 2013)**

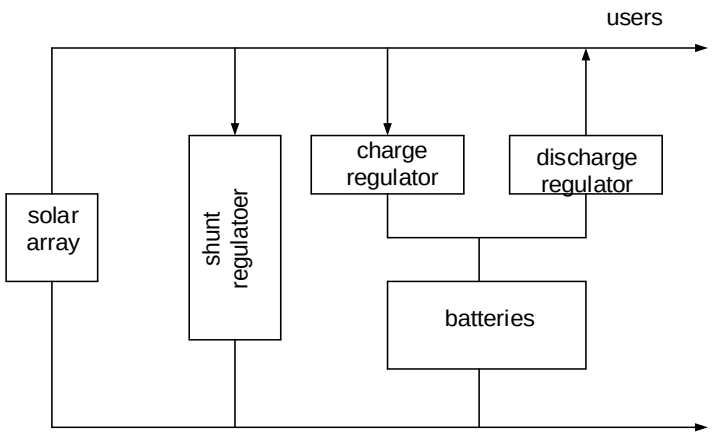


**Figure 3-9: Regulated direct energy transfer (Cupido, 2013)**

## 3.4 Maximum power point tracking (MPPT)

Maximum power point tracking is an electronics system which is implemented with the solar array modules in such a way that the modules produce the maximum power possible. MPPT is not a mechanical tracking network which physically orientates arrays to face the sun. MPPT is fully electronic system that changes the electrical characteristic of the cells, so that they are capable of yielding the maximum power possible under a given set of conditions. Adding the

power harvested from the modules, increases the battery current charge. Maximum power point tracking can be used in conjunction with a mechanical tracking system; note however, that two networks are totally different. The solar array is applied as a primary energy source. The DC–DC power converter is used to transfer the maximum power from the solar array to a load; also the MPPT controller tracks the maximum power of the system (see Figure 3-10) (Umesh & Preeti, 2013).

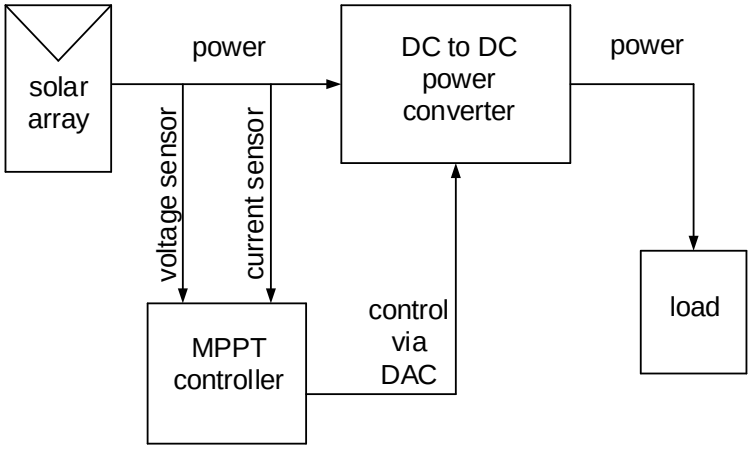


**Figure 3-10: Typical maximum power point tracking network block diagram**

### 3.4.1 Types of maximum power point tracking systems

A significant disadvantage of the photovoltaic networks is the relatively high cost required to produce energy, as compared to the traditional power generation systems. Even compared to renewable sources such as biomass electricity, the cost of photovoltaic network is high. To achieve high efficiency when delivering power to a load, it is crucial for the photovoltaic network to operate at its maximum capability; to affect this requires the implementation of maximum power point tracking. With regard to the space applications, a photovoltaic network is connected to a satellite via a DC–DC power converter. In order to gain the maximum power point tracking in photovoltaic networks, the voltage or current at the terminal can be selected in such a way the DC–DC power converter signal can be controlled.

To achieve maximum power point tracking, a large range of methods have been studied and implemented. These methods have been classified into three categories as stated by Reisi (2013):

- Online methods
- Offline methods and
- Hybrid methods.

### 3.4.2 Online methods

Applying the well-known model-free methods, the photovoltaic output voltage, or current is selected to produce control signals. The online methods discussed here are, incremental conductance method, the perturbation and observation method, as well as the extremum-seeking control method.

#### 3.4.2.1 Incremental conductance method

The incremental conductance method (Figure 3-11) determines the stable operating point by considering the operating point voltage at which the conductance is the same as the incremental conductance (Dorofte et al., 2005). This method has the ability to ascertain the relative distance to the maximum power point; it is able to track the maximum power point accurately during changing weather conditions, and compared to other methods, exhibits less oscillation around the maximum power point. This incremental conductance method does however, have drawbacks: the use of derivative operation in the method results in instability; also at low levels of insulation the differentiation process is demanding and subject to measurement noise which can cause undesired results (Babaa et al., 2014).

In the main, a fixed iteration step-size is used for the incremental conductance tracking method; this fixed step-size is governed by the accuracy and tracking speed required. Increasing the step-size improves the tracking speed; but, there is a decreased accuracy (Babaa et al., 2014). Similarly, a reduced step-size will improve accuracy; reducing the step-size will however, decrease the convergence speed of the method (Babaa et al., 2014).

#### 3.4.2.2 Perturbation and observation method

The perturbation and observation method (Figure 3-12) functions by adjusting the magnitude of the array terminal current, or voltage recurrently, and comparing the output power of the photovoltaic system with the output power measured at the preceding sample point. When the photovoltaic array operating voltage changes and the power increases, the control system amends the direct operating point of the photovoltaic system in the same direction; if this is not the case, the operating point will be adjusted the opposite way (Narendiran, 2013; Babaa et al., 2014).

The method carries on the operation at the same manner, so that at each perturbation point there is a precise value of current and voltage. The main benefit of this technique is the simplicity of the system; and that it achieves good results on condition that the solar irradiation conditions are relatively stable (Barakati et al., 2009). The operating point oscillates mildly around the maximum power point voltage when the system it operation at a steady state. This

is why the perturbation oscillation should be sufficiently low to permit the system achieving a steady state condition prior to the next perturbation (Babaa, et al., 2014). Additionally the step-size of the perturbation large enough so the controller is not materially influenced by measurement noise, and that a discernible change at the output of photovoltaic arrays is generated (Femia et al., 2005).

The major disadvantage of the perturbation and observation methods is poor efficiency at low irradiation. There are many solutions that have been suggested to improve efficiency at low radiation, such as: Cristinel (2005), suggests combining the constant voltage (CV) method with the perturbation and observation method, follow the maximum power point more closely at low and high solar irradiation conditions. In this method the duty-cycle is increased up to the point where the output voltage of the photovoltaic system is in the proximity of the open circuit voltage of the panel; this voltage is then applied in the starting conditions for the maximum power point tracker. This method examines the output current, and if the current is higher than a predetermined value, the algorithm causes the perturbation and observation method to be used; on the other hand, if it is lower, it defaults to the constant voltage method (Babaa et al., 2014).

Simulations Implementation have indicated that using this algorithm results in more energy being harvested from a photovoltaic panel than with the other methods; an efficiency range of 95% – 99%, over a wide irradiation range has been mentioned (Borup et al., 2005; Babaa et al., 2014).

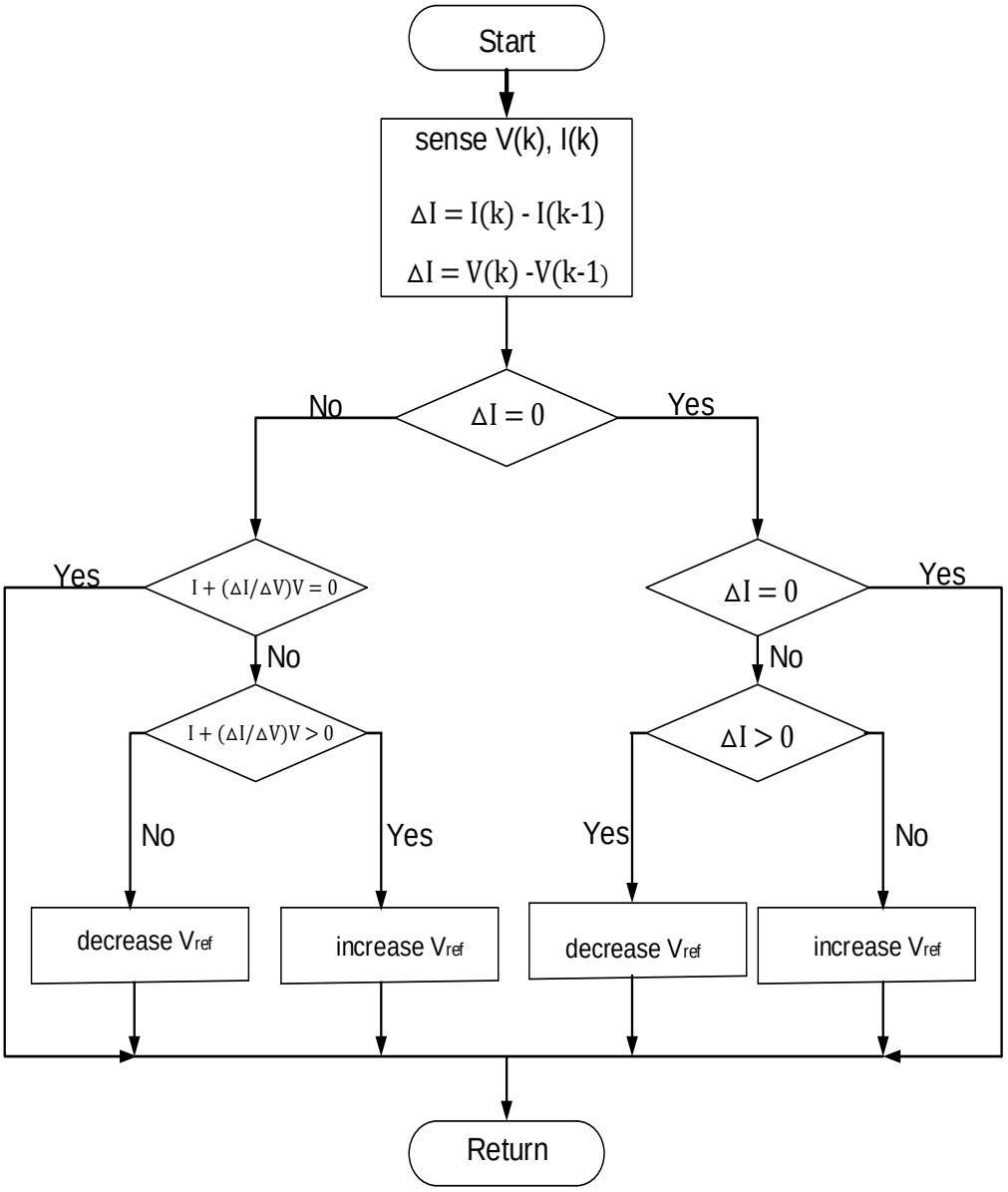


**Figure 3-11: Incremental conductance algorithm (Babaa et al., 2014).**

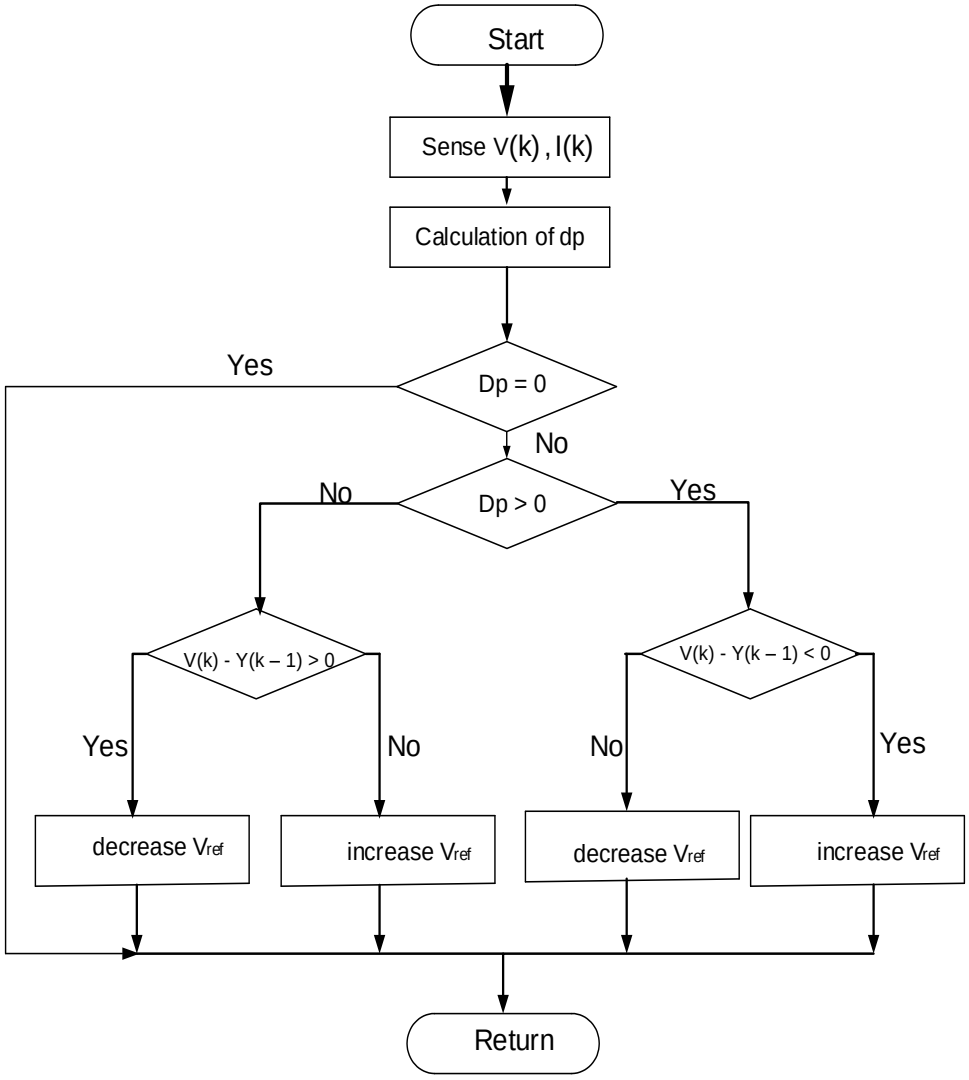


**Figure 3-12: Perturbation and observation algorithm (Babaa et al., 2014).**

### 3.4.2.3 Extremum-seeking control method

The usefulness extremum-seeking control was put forward by of Babaa (2014), who suggested that this method might be enhanced if singular perturbation and averaging were incorporated. This ideal real-time systematic procedure applies to a non-linear dynamic structure with adjustable feedback. Extremum-seeking control has found application in various fields; these include power reduction maximization of a flight, traction maximization in anti-lock braking for cars, autonomous vehicle target tracking, pressure-rise maximization of aero engine compressors, and fine adjustment of proportional integral derivative (PID) (Babaa et al., 2014). In terms of space applications, this method is used to track the maximum power point in photovoltaic systems (Bazzi & Krein, 2011).

Using the extremum-seeking control method which is self-optimizing, for controlling maximum power point tracking in a PV system, the aim is for the operating point of the photovoltaic system to rapidly follow the maximum power points, taking account of the uncertainties and disturbances from the PV panel and the external loads. The block diagram in Figure 3-13 below depicts the implementation of the extremum-seeking method with a photovoltaic network (Reisi et al., 2013).

Assume a small sinusoidal current represented by asin ($\omega t$), is added like a perturbation, to the original current ($I_{origin}$). This leads to the existence of a ripple power ($\triangle$P), where the amplitude and the phase depend on the position of the operating point relative to the maximum power point. As illustrated in Figure 3-13, the sinusoidal perturbation current is added to the original current, and used in the photovoltaic network. When the current ripple is in phase with the power output ripple, the power output fall to the left of the maximum power point, and the maximum power point current will be greater than the original current; therefore the controller has to vary the original current to improve the network (Babaa et al., 2014).

The ripple power in the output signal received by the MPPT controller is determined by the high-pass filter. Power is demodulated by multiplying it by sin ($\omega t$ -$\phi$). As a consequence, the signal is either negative or positive depending on the output curve power position. In order to achieve the maximum power point, the zeta is used with the integrator to change the original current. In the situation where the operating point is positioned at the maximum power point, the value of the ripple will be lower and the output power ripple frequency will be double the ripple current (Brunton et al., 2010).

There is a method similar to extremum-seeking control called ripple correlation control, which can perform the tracking of maximum power point by using a ripple in power. When a photovoltaic panel is connected to a switching DC–DC power converter, the switching techniques of the DC–DC power converter oblige the current and voltage ripple of a solar cell array. As a result, power from the solar cell array becomes the prone to ripple. For the ripple correlation control algorithm, correlation is implemented in terms of a current or voltage derivative connected to the photovoltaic array, which tries to reach the maximum power point by leading the gradient of the power to zero (Leyva & Alonso, 2006).

The extremum-seeking control has the two main advantages: firstly optimization is a concern in power maximization which is solved by dynamic techniques based on feedback control theory of the sinusoidal perturbation. The ability of the maximum power point is convergent, provided that the control algorithm is convergent.

Secondly, this approach does not need structured format or parameter to model the uncertainly. The disadvantage of an extremum-seeking control algorithm depends on the difficulties associated with its implementation, as well as the importance of knowing the signal relative to the low amplitude (Brunton et al., 2010).

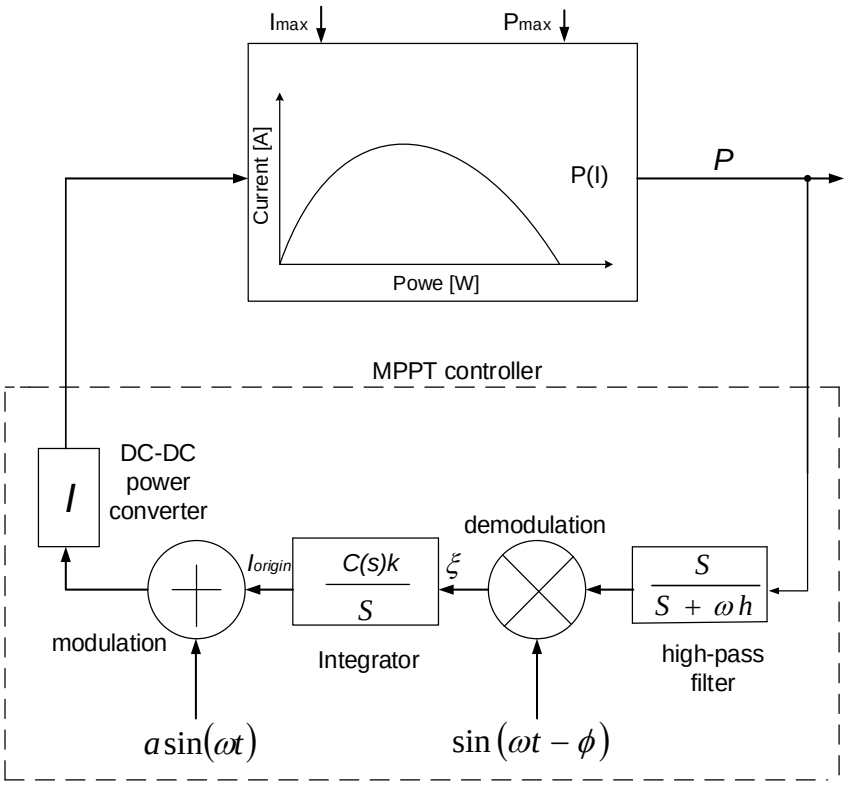


**Figure 3-13: Extremum-seeking MPPT controller with PV network (Brunton et al., 2010)**

### 3.4.3 Offline methods

Offline methods, or model-base methods as they are also known, generally respond to the actual values from the photovoltaic panel to produce appropriate control signals. Of these offline processes, the following are applied to photovoltaic systems: the short circuit current process; the open circuit voltage process; and the maximum power point tracking process which is based on artificial intelligence.

#### 3.4.3.1 Short circuit current techniques

These techniques; utilises the approximate straight-line relationship between the maximum power point current and the short circuit current of the photovoltaic array and is reflected in Equation 23 below:

$$I_{MPP} \approx KI_{sc} \quad (23)$$

where *K* has a constant value in the range

of 0.8 to 0.9

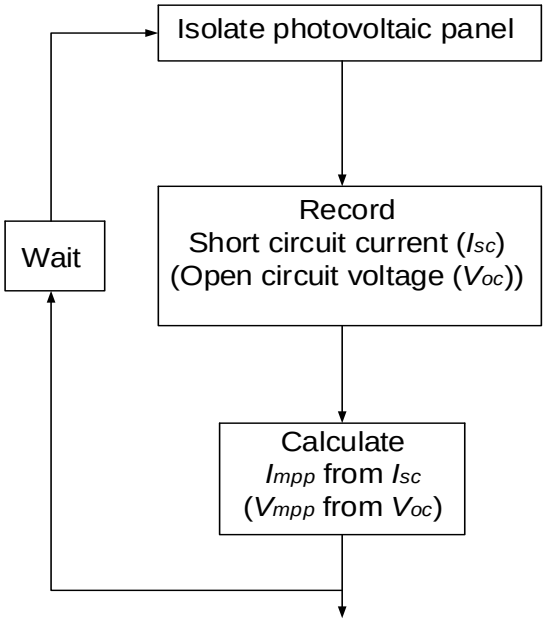


**Figure 3-14: Short circuit current techniques and open circuit voltage techniques**

The load has to be disconnected in order to determine the specific value of the short circuit current required. The short circuit technique is more accurate and efficient than the open circuit voltage technique (Reisi et al., 2013), and although it is practically simple to implement, and however, it is less cost effective. Using the DC–DC power converter, the switch can be used to close the circuit of the photovoltaic array (Noguchi et al., 2002; Reisi et al., 2013).

The short circuit current technique may fail to deliver the maximum power to the load for two reasons.

- First reason, the maximum power point could never be extracted by using Equation 23 above and
- The second reason is the temporary disconnection of the load while measuring the short circuit current. This method cannot be characterized as a true seeking maximum power point technique. However, the simplicity of this techniques and the ease with it can be applied to make it suitable for use as part of novel hybrid techniques (Reisi et al., 2013).

### 3.4.3.2 Open circuit voltage techniques

Another simple technique for the offline algorithms is the open circuit method (Figure 3-14); it is founded on the rough linear relationship between the maximum power point voltage and the open circuit voltage. This relationship holds true under differing environmental conditions, and is given by Equation 24 below:

$$V_{MPP} \approx KV_{OC} \tag{24}$$

where $K$ is a constant whose value depends on the photovoltaic characteristics

Based on the observations and experimental measurement the open circuit voltage and the maximum power point voltage under various environmental conditions; it is not possible to select an optimal value for $K$; however, a range of 0.73 – 0.80 has been reported for polycrystalline photovoltaic array modules (Salameh et al., 1991).

In spite of the relative ease of implementation and the low cost, this technique has two critical disadvantages. From the Equation 24 above, the voltage at the maximum power point is calculated at any open circuit voltage measured. At every intermediate stage where the maximum power point is tracked, the corresponding value of the maximum power point voltage is selected as a set point and is assumed to remain approximately the same throughout a wide range temperature and irradiance values (Brunton et al., 2010).

Firstly, the accuracy of tracking the maximum power point may not be properly implemented. Secondly, to measure the open circuit voltage requires periodic shedding load, which produces an undesirable effect on the network as well as further power losses. To obviate these losses, the use of a pilot cell has been applied to obtain the open circuit voltage. This pilot cell has to be carefully selected to characterize the PV array. To solve this problem of power losses resulting from load interruptions of the load, a straightforward approximate method can be applied. This application entails the measurement of temperature and solar irradiance, as well as an estimation of open circuit voltage, based on the model equations (Reisi et al., 2013).

### 3.4.3.3 Artificial intelligence techniques

Artificial intelligence techniques have become well-known as alternative ways to conventional algorithms, or as a key component of the integrating networks. They have been used to overcome the solution to various technical problem associated with maximum power point tracking. Artificial intelligence techniques have several disciplines such as artificial neural

networks, and fuzzy logic control. They have been successful used for finding the maximum power point (Reisi et al., 2013).

#### 3.4.3.4 Artificial neural network

The use of artificial neural networks in different fields has been increasing, because they offer the advantage of being able to process non-linear task. It is based on a learning process and does not have to be programmed. An artificial neural network is made up of three layers; an input layer, a hidden layer and an output layer. The nodes of an artificial neural network contain information and are inter-linked. Information exchanged between the nodes of different layers is scaled by the weighting attributed to a particular limit. As depicted in Figure 3-15 below, the inter-link between nodes '*i*' and '*j*' is weighted by a factor '$w_{ij}$'; the summation of all the input needs to be complete, and changed by the allocated weights (Syafaruddin, 2009).

It has been pointed out that the artificial neural network is techniques whereby an input is received data processes, and an output is delivered. The number of nodes and the setup of an artificial neural network may be change, depending on the designer. A typical variable input could be from a photovoltaic source and could comprise such parameters as temperature, rate of solar irradiance, short circuit current, and open circuit voltage. An artificial neural network output could be used to drive a DC–DC power converter, by selecting a suitable duty-cycle signal, or having an additional input controller to allow the photovoltaic network to operate optimally close to the maximum power point (Trishan & L, 2007).

In the shaded scenario, the artificial neural network is trained to predict the overall maximum power point voltage and power by using the PV characteristic curve under various exposure condition of the solar array.

The difference between the actual voltage and the predicted voltage of the solar array creates an error input for the maximum power point tracking controller to track the maximum power (Babaa et al., 2014).

The artificial neural network has two main topologies, which are the recurrent neural network (Figure 3-16) and the feed-forward neural network (Figure 3-17). The recurrent neural network depends on the dynamic response of the system; it has a feedback control loop which embodies short-term memory.

In a feed-forward neural network the input-output data is rigorously fed forward, creating the possibility of extending data to multiple layers, without feedback control loops. The link is from the input units to the output units with an identical layer or previous layers (Al-kazemi & Mohan, 2002).

In order to improve maximum power point tracking for a photovoltaic network under partial shading conditions, Syafaruddin (2009), suggested the an artificial neural network assembly together with fuzzy logic using a polar information controller to extract the maximum power. The artificial neurel network feed-forward has three layers which are trained under several partly shaded photovoltaic array to establish the optimum value of the photovoltaic voltage. These techniques has been compared to the perturbation and observation algorithm for differing patterns patterns over a set time frame. It has been proved that the tracking efficiency of this techniques is double that of perturbation and observation algorithm (Syafaruddin, 2009).

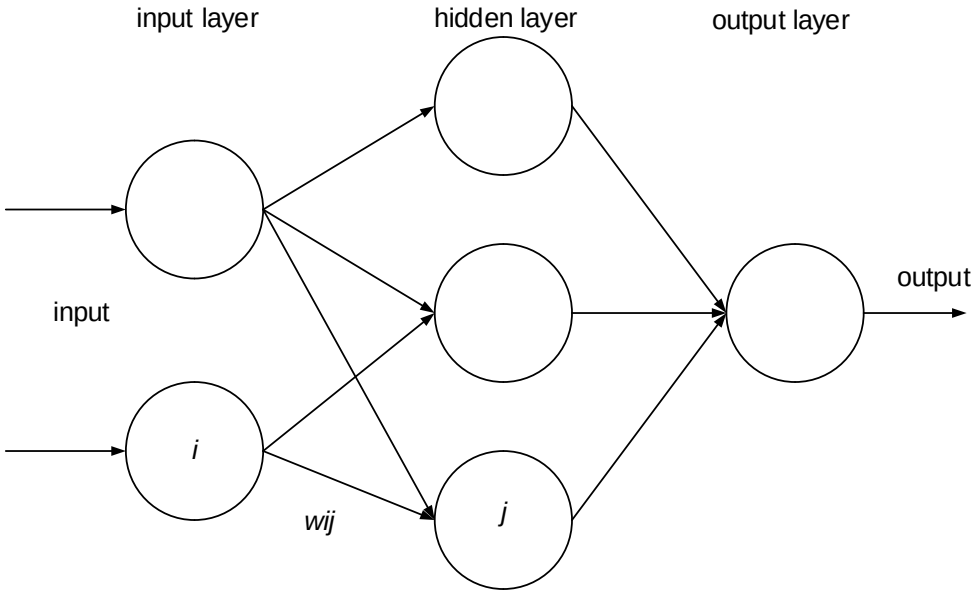


**Figure 3-15: Artificial neural network structure (Syafaruddin, 2009)**

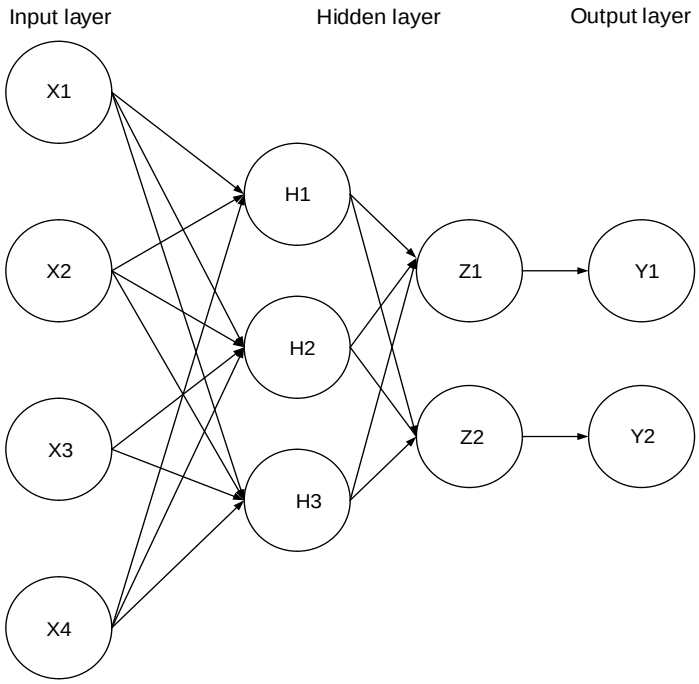


**Figure 3-16: Four input feed-forward neural network with two outputs**
**(Al-kazemi & Mohan, 2002)**

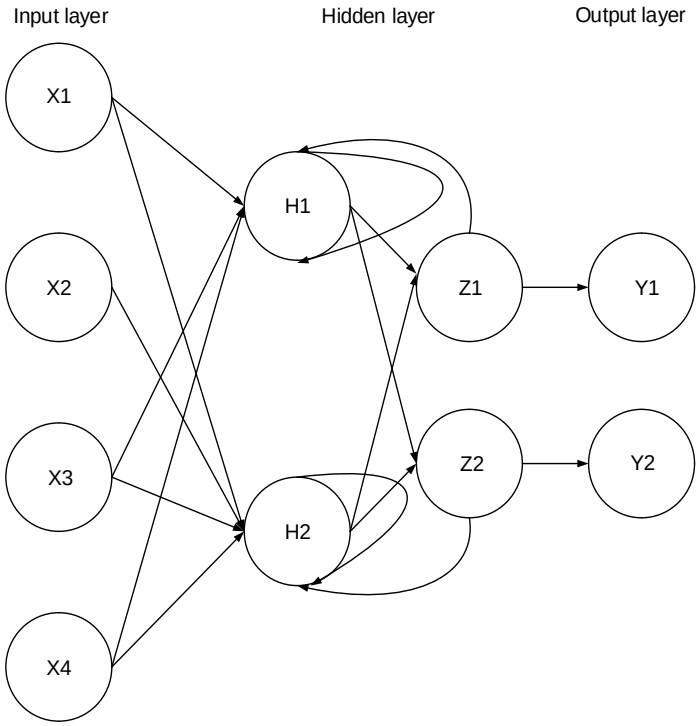


**Figure 3-17: Four input recurrent neural network with two outputs**
**(Al-kazemi & Mohan, 2002).**

### 3.4.3.5 Fuzzy logic control

The advent of microcontrollers has seen a rise in the application of fuzzy logic control over the last 20 years. It has the advantage of being able to process non-accurate input values, of mathematical models and is capable of data handling. Fuzzy logic control is made up of three different parts, namely: rule-based on look-up table, fuzzification, and defuzzification (Khaehintung et al., 2004).

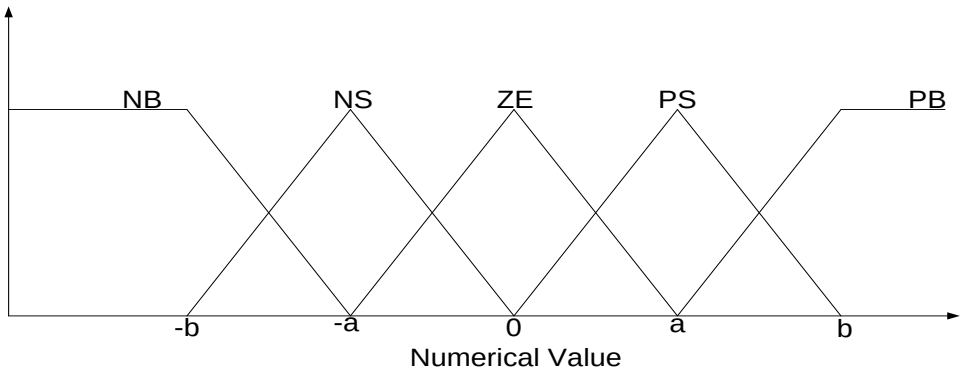


**Figure 3-18: Fuzzy logic control network**

In the fuzzification part, conversion of numerical input values to linguistic variables based on membership, takes place; this is illustrated in Figure 3-18.

In this scenario, five fuzzy steps are taken into consideration, for example: negative big (NB), negative small (NS), zero (ZE), positive small (PS), and positive big (PB). Patcharaprakiti (2002) stated that using seven fuzzy steps will be more accurate. In Figure 3-18 it is shown that from a to b, is the base interval of the numerical values (Veerachary et al., 2003).

The input to the fuzzy controller of an MPPT system is typically an error signal and a change in error. The user has the choice to how to compute the error and the change of error, change of power and the voltage vanishes at the maximum power point, uses the closest value required as illustrated in the Equation 25 below (Babaa et al., 2014).

$$E_n = \frac{P_n - P_{n-1}}{V_n - V_{n-1}} \tag{25}$$

and,

$$\Delta E_n = E_n - E_{n-1} \tag{26}$$

In the defuzzification part, the fuzzy logic controller output is converted from a linguistic value to a numerical value, taking account of the membership function. This supplies the analogue signal which will adjust the DC-DC power converter toward the maximum power point; maximum power point tracking fuzzy logic controllers have been proved their performance under changing atmospheric conditions. However, to achieve a significant result demands that the user applies appropriate knowledge and engineering control principles to select proper error computation and engagement with the rule-based table (Khaehintung et al., 2004).

### 3.5 Summary

In this chapter the theory behind photovoltaic cells employed as the first source of energy, was investigated. Additionally, a comparative of different types of batteries used as a secondary source of energy, was carried out. The different nanosatellite power system topologies such as MPPT, in parallel with a couple of MPPT methods, such as online and offline method and DET were investigated.

# Chapter 4 : DC–DC POWER CONVERTERS TOPOLOGIES

## 4.1 Introduction

Different types of regulators are presented. Feedback control loops, with specific reference to voltage and current mode controls, as well as slope compensation were studied. To counter perturbation and noise of the DC–DC power converter, compensation networks were studied.

## 4.2 Linear and switching voltage regulators

There is a big demand for switching and linear regulators in electronics applications. As stated by Mohan and Robbins (2003), the design of a voltage regulator has to meet at least one of following criteria:

- Regulated output load; the output voltage has to be kept constant in a specific tolerance for changes within a certain range in the input voltage.
- Isolation; electrically the output voltage can be isolated from the input voltage.
- Multiple output loads; there may be multiple output loads which can be differ in terms of voltage and current ratings; these the output load are isolated from others.

## 4.3 Linear voltage regulator

Every power supply used in electronics application has a basic building block linear regulator, and that linear regulator has the ability of producing a high quality output voltage suited to applications where a low power level is required (Czarkowski, 2001). These electronics devices in these kinds of power supply, act like an adjustable-resistor. The adjustable-resistor characteristic, limits the magnitude of output voltage of the linear regulator to a magnitude smaller than that of the input voltage. Electronic devices such as MOSFETs or BJTs in this region can cause a significant amount of power loss, making them impractical in many applications where a high level of power or efficiency is required (Mohan et al., 2003:178; Mutch, 2013).

## 4.4 Switching voltage regulators

In their operation, DC–DC converters widely use switching voltage regulators (Mohan et al., 2003:178; Mutch, 2013).These converters use power electronic semiconductor switches which can be in the ‘on’ or ‘off’ state; in these states power dissipation is low, voltage across the switch is low when there is a high current flowing, or there is a high voltage across the switch when a low current flows. Nowadays modern semiconductors switches can be switched

at a high frequency; compact designs using small filters and transformers (Mohan et al., 2003:178; Mutch, 2013).

DC–DC converters of the switch-mode type have an advantage over linear regulators that they are able to step-up or step-down a voltage depending on the topology used. There are various types of converters available can be used in switching mode power supplies such as: isolated and non-isolated converter topologies (Czarkowski, 2001).

Some of the non-isolated and isolated topologies are listed below:

- Buck converter
- Boost converter
- Buck-boost converter
- Single-ended primary inductance converter
- Zeta converter
- Charge-pump converter
- Flyback converter
- Forward converter

Regarding a nanosatellite platform, the common switching voltage regulators topologies used are: boost, buck, buck-boost, and single-ended primary inductance converter (Strain, 2010).

### 4.4.1 Switching voltage regulator, boost converter

A DC–DC boost converter produces an average output voltage greater than the input voltage. Figure 4-1 below shows a DC–DC boost converter with a pure resistive load; the boost converter consists of a DC input voltage source $V_{DC}$, a controlled switch MOSFET (*Q*), diode (*D*), inductor (*L*) and a filter capacitor (*C*) (Czarkowski, 2001).

When the switch is ‘on’ state, the output stage is isolated from the input due to the reverse bias of the diode (*D*), and the inductor (*L*) receives energy from the input voltage supply; in this time the filter capacitor, *C* provides current for the load. When the switch is ‘off’, the energy stored by the inductor as well as energy from the input supply is supplied to the output stage (Mohan et al., 2003:178; Mutch, 2013).

Applying Faraday’s law, the equations related to a boost converter can be determined. This leads to a DC voltage transfer function as given by Equation 27 and 28 (Czarkowski, 2001).

$$V_{DC}.DT = (V_O - V_{DC})(1 - D)T \tag{27}$$

$$\frac{V_O}{V_{DC}} = \frac{1}{1-D} \tag{28}$$

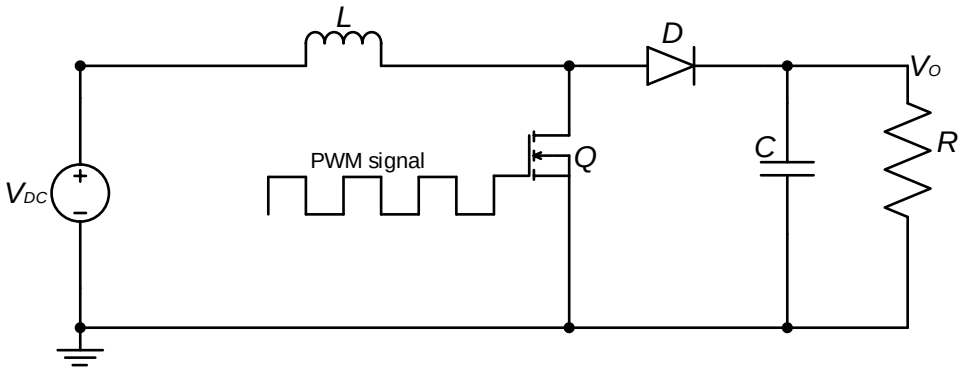


**Figure 4-1: Boost converter topology**

DC–DC boost converter operates in continuous-conduction mode under the condition where $L > L_b$. The inductor boundary value, $L_b$ can be determined by the Equation 29. The operation of the boost converter results in discontinuity of the output current to the *R-C* output stage. This discontinuous current requires the output filter capacitor found in the boost converter, to be larger than the one found in the buck converter. The larger filter capacitor is required to supply current to the load when the switch is 'on' state and the diode is reverse bias. The minimum value of capacitor that can be used to achieve a specific output ripple voltage needs to be larger than that calculated (using Equation 30) (Czarkowski, 2001).

Figure 4-2 illustrated the switching waveforms for an ideal DC–DC boost converter operating in continuous conduction mode.

$$L_b = \frac{(1-D)^2 D R_{load}}{2f} \tag{29}$$

$$C_{min} = \frac{DV_O}{V_r R_{load} f} \tag{30}$$

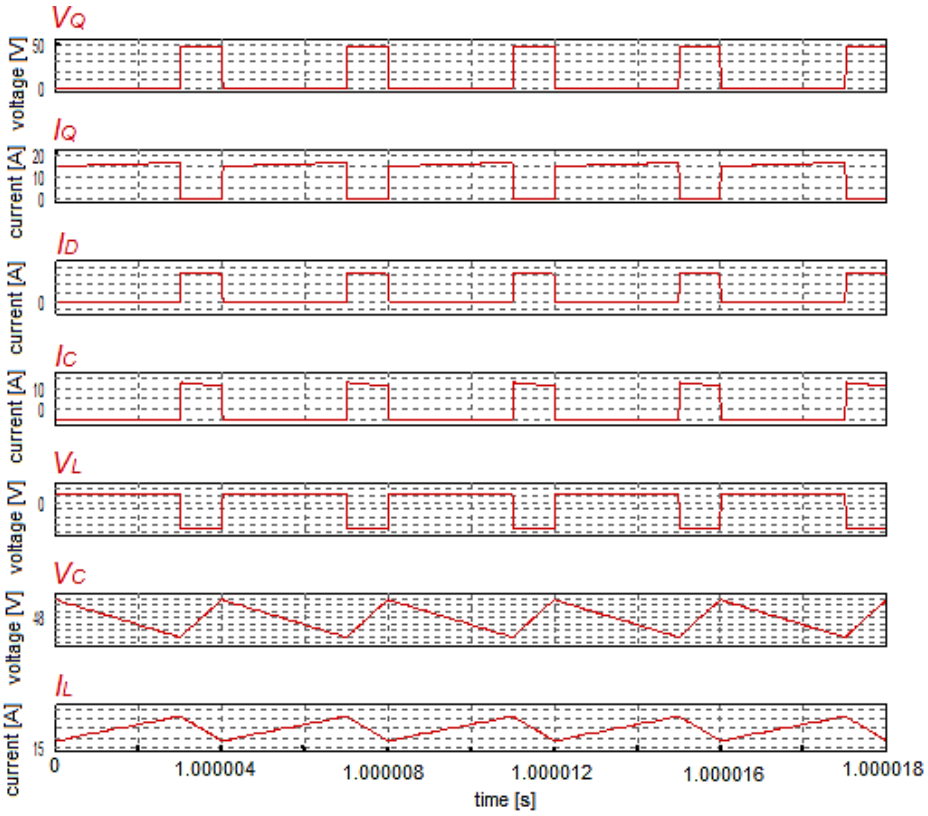


**Figure 4-2: DC–DC, boost converter ideal waveforms**

### 4.4.2 Switching voltage regulator, buck converter

The DC–DC buck converter produces an average output voltage lower than its input voltage. Figure 4-3 shown a DC–DC buck converter with a pure resistive load; it consists of a DC input voltage source, $V_{DC}$, a controlled switch (*Q*), a diode (*D*), a filter inductor (*L*) and a filter capacitor (*C*) (Czarkowski, 2001). The average output voltage can be calculated in terms of the switch duty-cycle as Equation 31 and Equation 32 shown below (Mohan et al., 2003:178; Mutch, 2013).

$$V_O = \frac{1}{T_S}\int_0^{T_S} v_O\,(t)\,dt = \frac{1}{T_S}\left(\int_0^{t_{on}} V_{dc}\,dt + \int_{t_{on}}^{T_S} 0\,dt\right) = \frac{t_{on}}{T_s}V_{dc} = DV_{dc} \qquad (31)$$

$$\frac{V_O}{V_{DC}} = D \qquad (32)$$

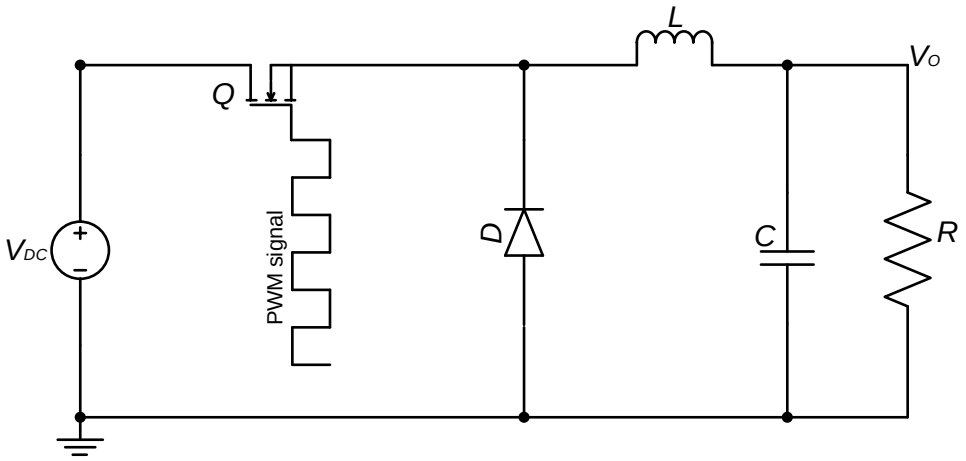


**Figure 4-3: Buck converter topology**

The DC–DC buck converter is operated in the continuous conduction mode (CCM) when the inductor current is never zero at any period of time. Figure 4-3 shows that when the switch (*Q*) is 'on' state, the diode (*D*) is in reverse bias. When the switch (*Q*) is 'off', the diode is in forward bias and conducts to support an uninterrupted current in the inductor. When the output current is low and the current of the inductor drops to zero, the converter is in discontinuous conduction mode (DCM). CCM is preferred as the semiconductor switches and passive components are better utilized resulting in a greater efficiency from the converter (Czarkowski, 2001).

The value of the inductance which determines between the boundary between CCM and DCM can be calculated from Equation 33, where *f* is the switching frequency of the switch and *R* is the load. For the value of $L > L_b$ the converter operates in the continuous conduction mode, and $L < L_b$ the converter operates in discontinuous conduction mode (Czarkowski, 2001).

$$L_b = \frac{(1-D)R_{load}}{2f} \tag{33}$$

The inductor current in CCM consists of a DC component, triangle AC, and the output current. Principally the AC current component flows through a filter capacitor as a capacitor current. This capacitor current causes a small voltage ripple in the DC output voltage. The filter capacitor needs to be large enough to limits the output ripple voltage; the Equation 34 shows the derive ripple voltage as a peak-peak voltage (Czarkowski, 2001).

$$C_{min} = \frac{(1-D)V_o}{8V_r L f^2} \tag{34}$$

Figure 4-4: illustrated the switching waveforms for an ideal DC–DC buck converter operating in continuous conduction mode.

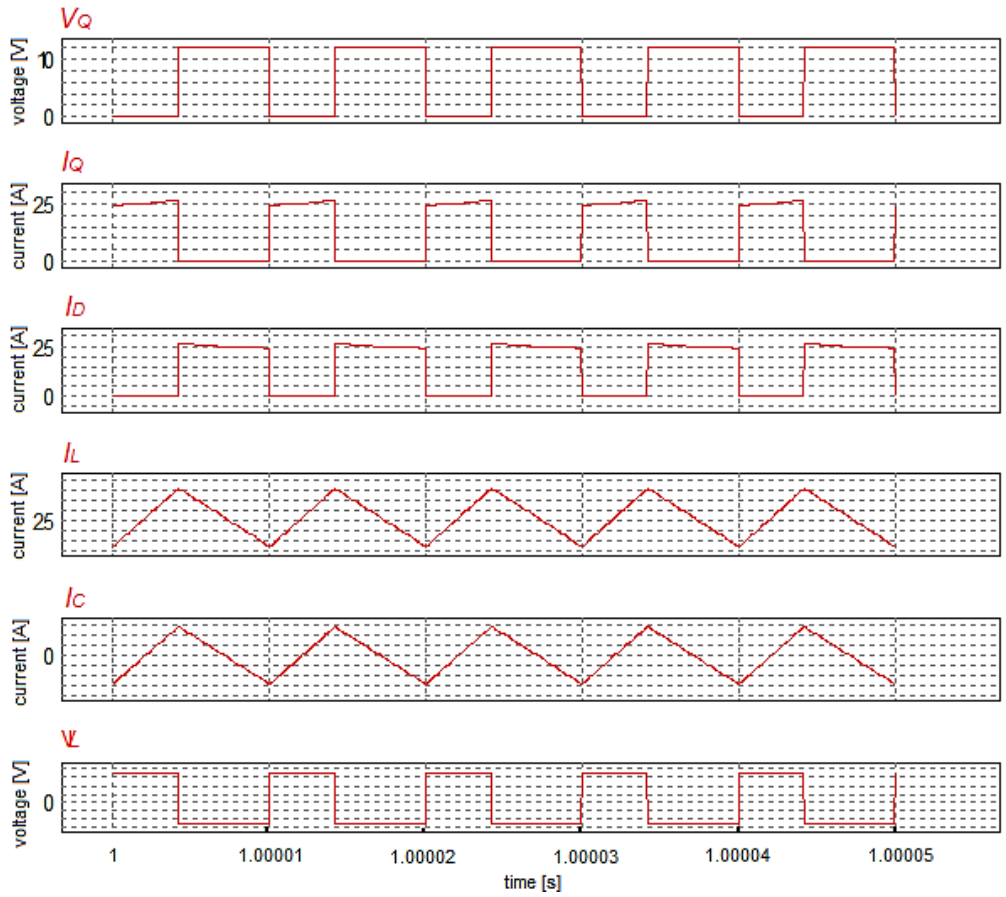


**Figure 4-4: DC–DC, buck converter ideal waveforms**

### 4.4.3 Switching voltage regulator, buck-boost converter

Regulated DC power supplies form the predominant use of buck-boost DC–DC converters; this is primarily because in these converters, a positive polarity input voltage with respect to the output voltage is wanted. The magnitude of the output voltage can be greater or less than the input voltage. In steady-state mode, the output to input ratio, shown by Equation 35 is the product of the conversion ratio the buck and conversion ratio of the boost converter. It is assumed that both buck and boost converters are operated at the same duty-cycle. A DC–DC buck-boost converter is illustrated in Figure 4-5 (Mohan et al., 2003:178; Mutch, 2013).

$$\frac{V_O}{V_{DC}} = D\frac{1}{1-D} \tag{35}$$

With the switch 'on', the inductor current increases and the diode (*D*) is in reverse bias. With the switch 'off', the diode provides a route for the flow of the inductor current. The specific value of the inductor can be calculated from Equation 36: the output stage structure of the DC–DC buck-boost converter is similar to that of the DC–DC boost converter.

$$L_b = \frac{(1-D)^2 D R_{load}}{2f} \tag{36}$$

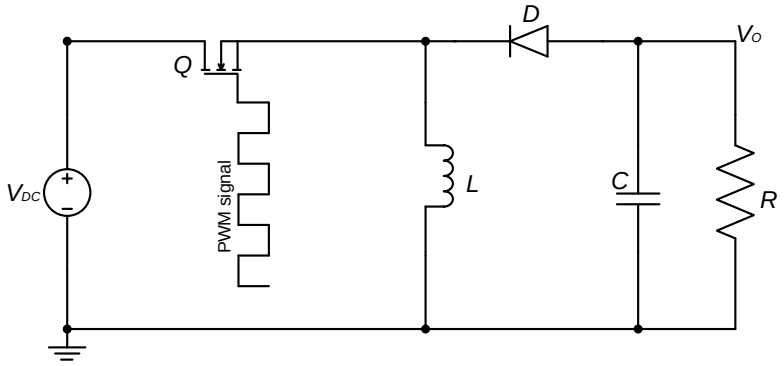


**Figure 4-5: Buck-boost converter topology**

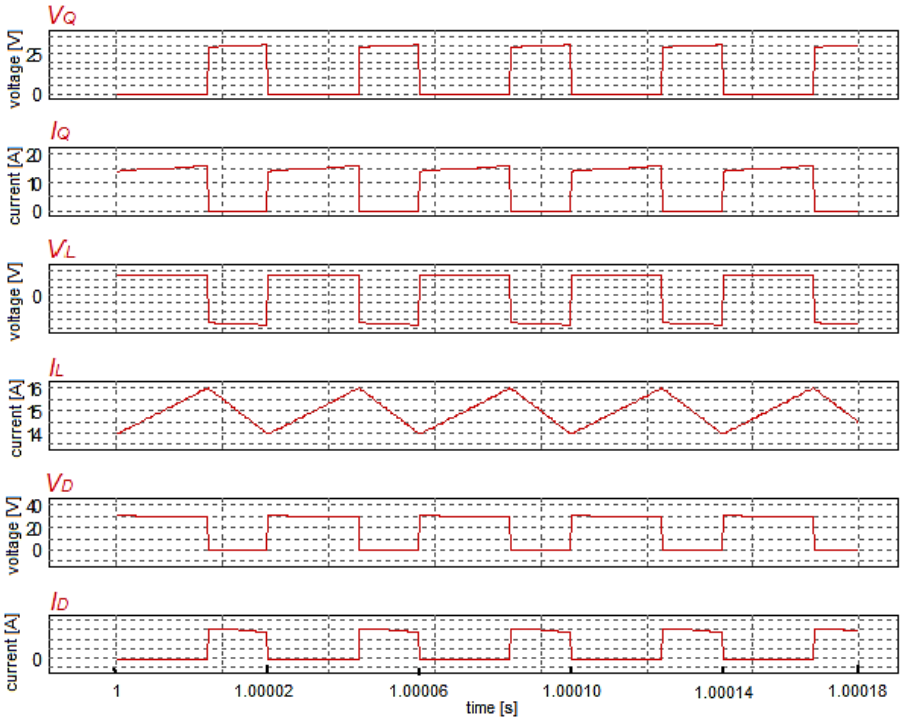


**Figure 4-6: DC–DC, buck-boost converter ideal waveforms**

### 4.4.4 Switching voltage regulator, single-ended primary inductance converter (SEPIC)

The single-ended primary inductance converter (SEPIC) is a DC–DC converter topology which regulated positive output voltage from an wide range of input voltage that varies from above to below the output voltage (Falin, 2008). The switch of a SEPIC is controlled by changing the duty-cycle; the use of a series capacitor couples the energy from input stage to the output stage. The SEPIC responds rapidly to short-circuit condition and when the switch is turned ‘off’ its acts in a true shutdown mode; its output drops to zero volt by following a hefty transient dump of charge (Fahmi, 2012; Subramanian & Manimaran, 2015). Figure 4-7 illustrates the completed SEPIC circuit, and in Figure 4-8 and Figure 4-9 the 'on' and 'off' states are respectively shown.

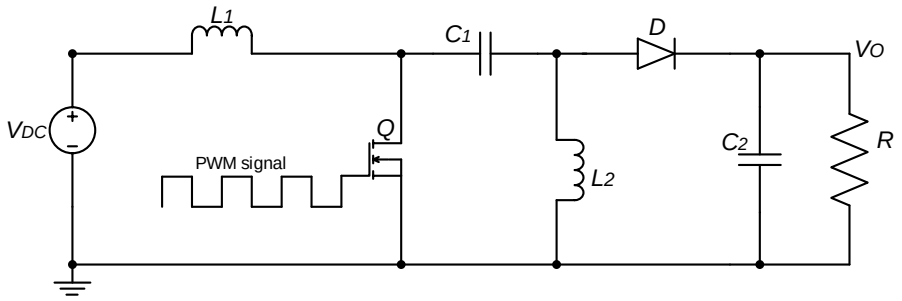


**Figure 4-7: SEPIC topology**

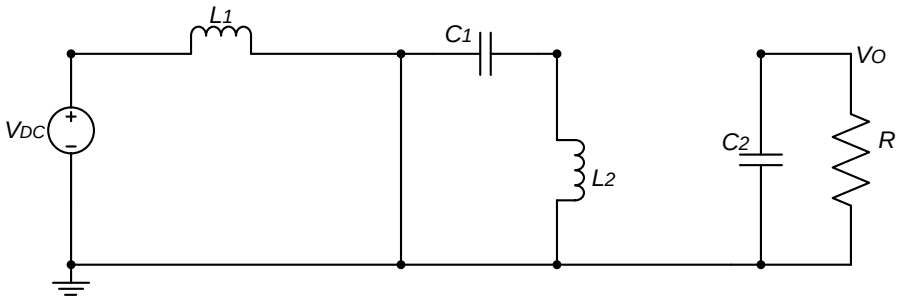


**Figure 4-8: SEPIC during on-state of the MOSFET**

The SEPIC is used in applications where the input voltage could be lower or higher than the output voltage of the regulator. SEPIC transfers energy between the capacitors and inductors during the switching operation; this process is done in order to convert from one voltage to another. The quantity of energy is controlled by the switch, which employs a transistor such as an IGBT, or a MOSFET. MOSFETs offer a wide range of advantages such as high input impedance which requires only a simple drive circuit, low voltage stress, as well as do not requiring any biasing resistors.

In addition, MOSFET switching can be controlled in voltage mode rather than a current mode (Subramanian & Manimaran, 2015).

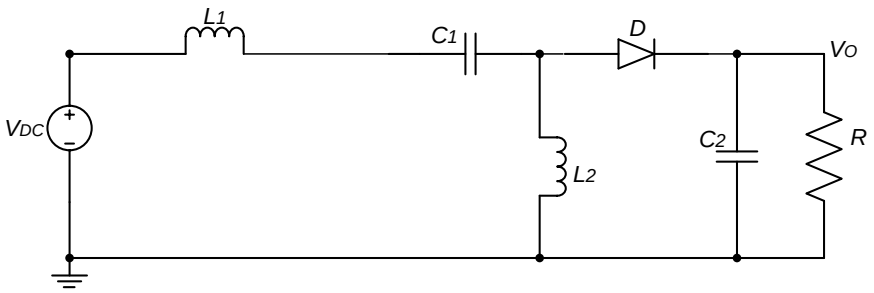


**Figure 4-9: SEPIC during off-state of the MOSFET**

### 4.4.5 Switching voltage regulator, SEPIC mathematical modelling

A mathematical model of a SEPIC is done by either an average method or a state space average method. Here state space average method is used to model a SEPIC. It is an approximation technique which allows approximation of the switching converter as a continuous linear system. A state space average method requires the effective filter corner frequency smaller to be than the switching frequency. The power stage of a clossed-loop system is a non-linear system (Hu et al., 2012).

Non-linear systems are difficult to model and also difficult to predicted, it is however, better to approximate the non-linear system to a linear system. To linearize the power stage of a DC–DC converter, a Bode plot can be used to determine for suitable compensation feedback in the loop for the desired steady-state and transient response (Padhi & Narain, 2013).

During switch on: $0 < t < dT$

$$\dot{X} = A_1 X + B_1 V_{in} \tag{37}$$

During switch off: $0 < t < (1 - d)T$

$$\dot{X} = A_2 X + B_1 \tag{38}$$

And the output voltage is:

$$V_o = CX + EV_{in} \tag{39}$$

To achieved an average description of the DC–DC converter circuit over the switching period, the equations corresponding to the two foregoing state spaces are time weighted and averaged, resulting in Equation 40:

$$\dot{X} = [A_1 d + A_2(1-D)]X + [B_1 d + B_2(1-D)]V_{in} \quad (40)$$

This equation shows that by controlling the duty-cycle of the switch, the output voltage can be higher than, lower than, or equal to the input voltage.

### 4.4.6 State space modelling for a conventional DC–DC SEPIC

The state space representation of a SEPIC has several advantages when compared to other mathematical models. A state space system has the ability to easily handle multiple inputs or outputs. The state variables for a SEPIC are considered to be currents ($I_{L1}$, $I_{L2}$) and voltages ($V_{C1}$, $V_{C2}$). When the switch is 'on', as illustrated in Figure 4.8, the state space equations for a SEPIC are:

During turned 'on' state as shown in Figure 4-8,

$$\begin{pmatrix} I_{L1} = -\dfrac{VDC}{L_1} \\ I_{L2} = \dfrac{V_{C1}}{L_2} \\ V_{C1} = -\dfrac{I_{L2}}{C_1} \\ V_{C2} = -\dfrac{V_{C2}}{RC_2} \end{pmatrix} \quad (41)$$

$$\frac{d}{dt}\begin{bmatrix} IL1 \\ IL2 \\ VC1 \\ VC2 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \dfrac{1}{L1} & 0 \\ 0 & \dfrac{-1}{C1} & 0 & 0 \\ 0 & 0 & 0 & \dfrac{-1}{RC2} \end{bmatrix}\begin{bmatrix} IL1 \\ IL2 \\ VC1 \\ VC2 \end{bmatrix} + \begin{bmatrix} \dfrac{-1}{L1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in} \quad (42)$$

Conversely, when the switch is 'off', as illustrated in Figure 4.9, the state space equations for a SEPIC are:

$$\frac{d}{dt}\begin{bmatrix} IL1 \\ IL2 \\ VC1 \\ VC2 \end{bmatrix} = \begin{bmatrix} 0 & 0 & \dfrac{-1}{L1} & \dfrac{-1}{L1} \\ 0 & 0 & 0 & \dfrac{-1}{L2} \\ \dfrac{1}{C1} & 0 & 0 & 0 \\ \dfrac{1}{C2} & \dfrac{1}{C2} & 0 & \dfrac{-1}{RC2} \end{bmatrix}\begin{bmatrix} IL1 \\ IL2 \\ VC1 \\ VC2 \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in} \quad (43)$$

$$\frac{d}{dt}\begin{bmatrix} IL1 \\ IL2 \\ VC1 \\ VC2 \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L1} & \frac{-1}{L1} \\ 0 & 0 & 0 & \frac{-1}{L2} \\ \frac{1}{C1} & 0 & 0 & 0 \\ \frac{1}{C2} & \frac{1}{C2} & 0 & \frac{-1}{RC2} \end{bmatrix} \begin{bmatrix} IL1 \\ IL2 \\ VC1 \\ VC2 \end{bmatrix} + \begin{bmatrix} \frac{VC1+VC-2VDC}{L1} \\ \frac{VC1+VC2}{L2} \\ \frac{-IL1-IL2}{C1} \\ \frac{-IL1-IL2}{C2} \end{bmatrix} Y + \begin{bmatrix} \frac{1}{L1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{DC} \quad (44)$$

$$\dot{X} = AX + BY + C \quad (45)$$

Where $Y$ is the status of the switches, and $X \; and \; \dot{X}$ are the state variables and their derivatives comprising the currents $I_{L1}$ and $I_{L2}$, and the voltages $V_{C1}$ and $V_{C2}$.

$$Y = \begin{pmatrix} 1 \rightarrow S \rightarrow ON \\ 0 \rightarrow S \rightarrow OFF \end{pmatrix} \quad (46)$$

### 4.5 Control loops and feedback

In general, DC–DC converters have a narrowly regulated output rail voltage. The regulated output rail voltage has to be stable during the input voltage and load current variations. Consider the converter to be used at a constant duty-cycle; the change in the input voltage of the converter would then result in a change of the output voltage due to a constant duty-cycle and a changing input voltage. Changes in the output load current may also result changes of the output voltage, as the switching losses in the switch and other components vary, dependently of the current variation (Zhang, 2010; Mutch, 2013).

With the use of a negative feedback, the duty-cycle of the switches can, where it is necessary to obtain a suitable output voltage from the DC–DC converter, can be automatically adjusted with a high level of accuracy despite changes in the output current and input voltage (Erickson & Maksimovie, 2004).

In the closed-loop feedback systems there are two most commonly used control methods for DC–DC converter namely: voltage-mode control and current-mode control (Czarkowski, 2001). Block diagrams illustrate these control methods: they were re-drawn from Czarkowski (2001:221) and can be seen in Figure 4-10 and Figure 4-11.

The implementation hardware of the voltage-mode control is simple, which is a major advantage. In a voltage-mode control scheme, the error amplifier produces a voltage difference; the control voltage from the output voltage and a reference voltage. The control voltage is compared to a constant-amplitude sawtooth (triangular waveform). This results in a PWM used to control the switches of the DC–DC converter.

The PWM duty-cycle directly depends on the control voltage. Voltage-mode control is able to provide good load regulation, however, line regulation is delayed as changes in the input voltage have to be observed at the output voltage before they can be corrected by this form of control (Czarkowski, 2001).

The inner control loop is added in the current mode control, feeding back a current signal from the inductor. This current signal is converted to an analogue voltage and compared to the control voltage as a replacement for the sawtooth (triangular waveform). By changing the sawtooth waveform used in voltage-mode control with a current signal, causes the DC–DC converter to take on some of the current source characteristics. The dynamic behavior of the converter is changed by this characteristic (Czarkowski, 2001).

Figure 4-10 illustrates a pratical application of voltage-mode control of a DC–DC converter where a fraction of output voltage is compared to the reference voltage.

The feedback loop from the converter output to the input, results in the controller trying to preserve equilibrium between α and the reference voltage ( Equation 47). the signal from the output feeds back to the inverting input of the comparator amplifier. The error amplifier frequency response is affected by a compensation network formed around the comparator amplifier (Figure 4-11). The componsation network is used to adjust the frequency response of the DC–DC converter in such a way that the converter is stablelised during a closed-loop operation (Basso, 2008).

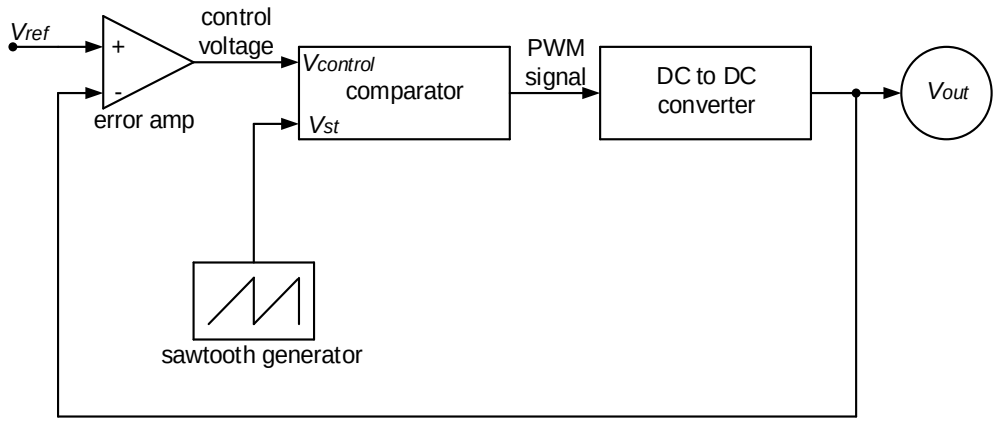


**Figure 4-10: DC–DC converter Voltage mode control**

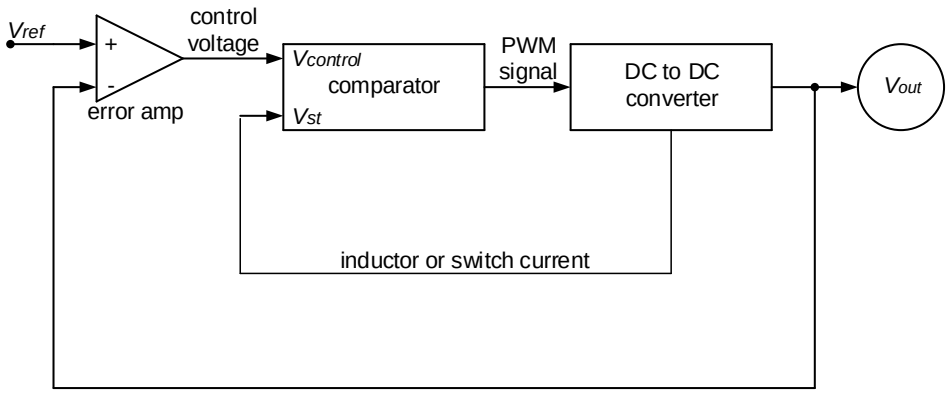


**Figure 4-11: DC–DC converter current-mode control**

$$V_{out} = \frac{V_{ref}}{\alpha} \tag{47}$$

A simplifier version of the converter seen in Figure 4-12 is shown in Figure 4-13 in which the loop gain of the system represented by the Equation 48 and 49 below:

$$G(s) = G_c(s)G_{PWM} \tag{48}$$

$$T(s) = H(s)G_cG_{PWM} \tag{49}$$

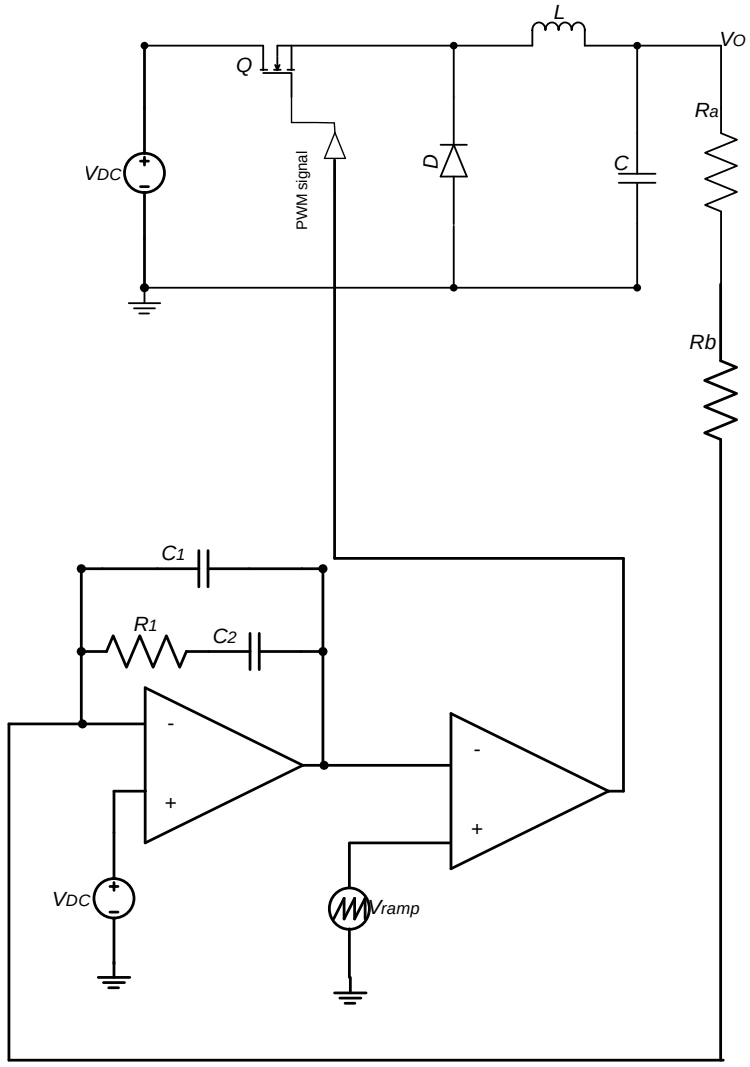


**Figure 4-12: Switch-mode power converter closed-loop mode (Basso, 2008)**

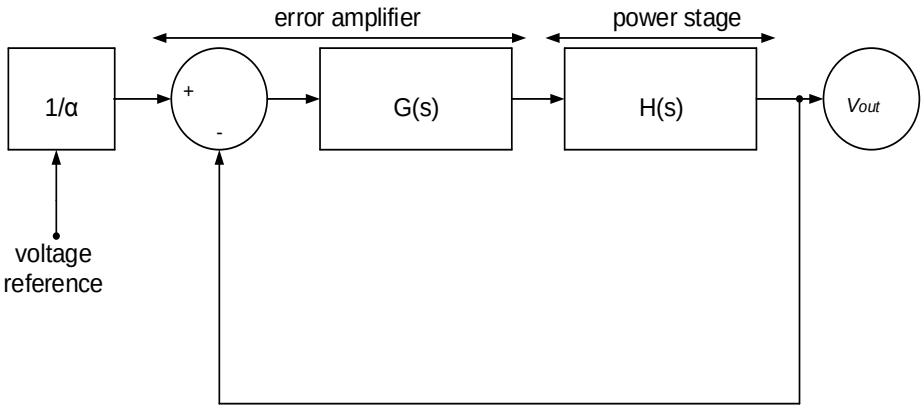


**Figure 4-13: Simplified representation of the switch-mode power converter functioning in closed-loop mode**

## 4.6 Challenges of loop design and objectives

The main goal of loop stability consists of two principal tasks. The first task is to determine what the type of plant transfer is, like its gain-phase Bode plot with all the characteristic of poles and zeros. The second task is to design a feedback compensator so that its zeros and poles are properly located with respect to the plant. Clearly, the transfer function is the product of G(s) and H(s). By calculating G(s), the design of H(s) can be accommodated that the combined gain is approaching to a straight line of slope which falls tenfold in gain every tenfold in frequency increase. That is the main criterion for loop stability of a DC–DC power converter, be it a current-mode control or voltage-mode control (Maniktala, 2012).

The plant transfer function of current-mode control differs substantially from that of voltage-mode control; however, they both result in the designed shape of G(s) x H(s) having a slope of -1. When the load and line variations occur, G(s) can be changed markedly in one control method as compared another (Maniktala, 2012).

## 4.7 Voltage mode control

In a voltage-mode control, the DC–DC converter output voltage is fed back to a pulse width modulation controller, and the duty-cycle is correspondingly adjusted. Figure 4-12 shows a DC–DC converter using voltage-mode has a single control loop. Stability of a control loop depends on considering the following during the design process: the small-transfer functions of the DC–DC converter power stage, the measurement of the voltage, and the gain of the PWM comparator. The control loop is stabilized by adding a compensation network (Van Rhyn, 2006). From Van Rhyn (2006) the advantages and disadvantage of a voltage mode control are listed below.

### 4.7.1 Advantages of voltage mode control

- The analysis of the feedback loop is easy, which simplifies the design of the compensation network.
- Large amplitude ramp waveform ensures good noise immunity.

### 4.7.2 Disadvantages of voltage mode control

- Slow response of the control loop to changes in the load current and line voltage; these changes are indirectly manifested as a change in the output voltage.
- A decrease in the input voltage range, resulting from the input voltages occurring in the small signal transfer function of the DC–DC converter power stage.
- Voltage mode control does not allow the control of the current in the system; however it used for current limiting, protecting the system under fault conditions.

## 4.8 Current mode control

### 4.8.1 Peak current mode control

A current mode control is a double loop control system (Figure 4-11). The inner loop controls the inductor current of the DC–DC converter. It provides the simplicity of the outer voltage control loop design, for better dynamics and improves the performance of a DC–DC converter. Practically, the peak method of current control in the inductor, works by comparing the up-slope of inductor current to the outer loop current level (Van Rhyn, 2006).

In general, the set current level is bigger than a current ramp, especially when the input voltage is low. The peak current mode control method is extremely susceptible to noise. When the output signal of a comparator goes high, a noise spike is produced; this could immediately turn the switch 'off', resulting in a sub-harmonic operating mode with greater ripple (Van Rhyn, 2006). Van Rhyn (2006), the advantages and disadvantage of a peak current mode control are listed below.

### 4.8.2 Advantages of peak current mode control

- The DC–DC converter will respond instantaneously to the changes in the input voltage; knowing that the inductor current increases with a slope of $\frac{V_{in}-V_{out}}{L_f}$, the input voltage change will yield the inductor current waveform measured. The delay allied to voltage-mode control due to input voltage changes, has been averted by peak current mode control.
- Minimizes the effect of the output filter inductor and decreases a transfer function of the output filter to a single pole, by using an error amplifier to control a current as opposed to a voltage.
- Sharing the load current if multiple DC–DC converters are used.

### 4.8.3 Disadvantages of peak current mode control

- Instability of the system at above a 50% duty-cycle, and therefore the need for slope compensation.
- Poor noise immunity of the system.
- Complexity analysis of the system due to the extra feedback loop added.

### 4.8.4 Average current mode control

Average current mode control solved the problem of instability and poor noise immunity by using a high-gain integrating current error amplifier (Van Rhyn, 2006). Average current mode control is identified by two feedback loops; an integrator in the inner loop to average the

observed current (Figure 4-14). The current to be controlled is picked up via a resistance and averaged. The voltage mode control loop provides a reference voltage to the integrator of the current amplifier of the inner loop. The signal output of the integrator is compared to a saw-tooth generator and the output of the comparator gives a signal which controls a switch (Raoufi & Moulay, 2004).

At the minimum current levels when a DC–DC converter operates on the boundary of continuous and discontinuous conduction mode, average current mode control tracks the current program with a high degree of accuracy (Van Rhyn, 2006). The average current mode control is an improved version of peak current mode control in terms of advantages as stated Raoufi & Moulay (2004) and Van Rhyn (2006).

### 4.8.5 Advantages of average current mode control

- Excellent noise immunity compared to a peak current mode control.
- With the adoption of an extra comparator to sense the current, the system is stable at the highest duty-cycle (>50%), and no slope compensation is needed.
- Average current mode tracks the current to a high degree of accuracy.

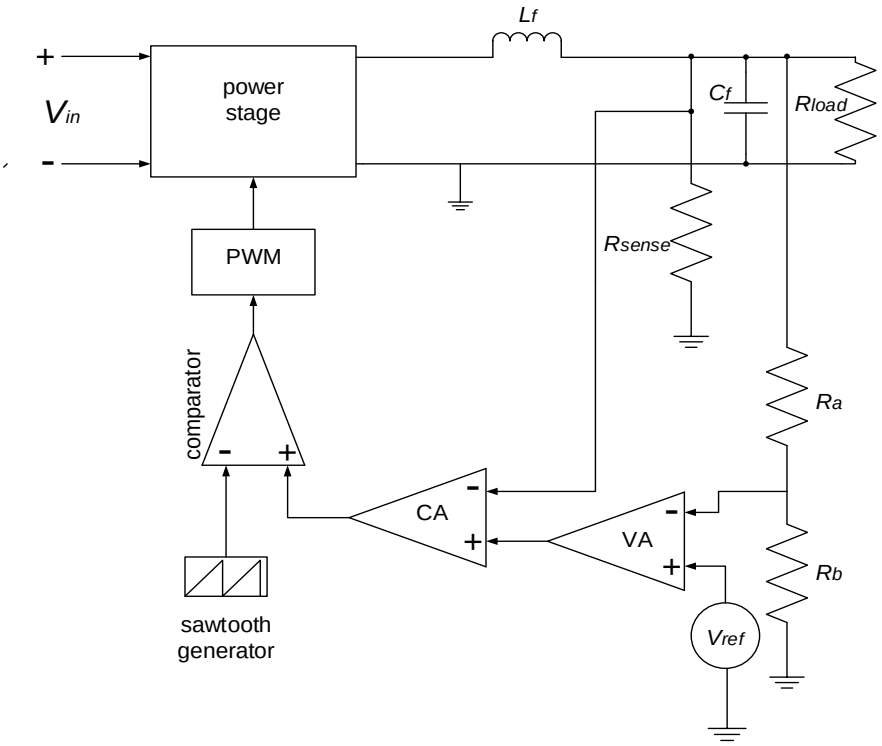


**Figure 4-14: Block diagram of an average current-mode control**

### 4.8.6 Hysteretic current-mode control

Hysteretic current mode control is the method where a switch-mode DC–DC converter has two or more inductors that need to be controlled. The operation of a switch mode DC–DC converter will be based on the theory of sliding mode control. Figure 4-15 depicts a circuit diagram of a hysteretic current-mode control with slope compensation using a DC–DC single ended primary inductor converter (Kavitha & Uma, 2011).

Consider a DC–DC SEPIC: the output voltage is the last target when it acts as a DC–DC buck (step-down) or a boost (step-up) converter; it is however not possible for a closed-loop system to achieve a stable oscillation of the switching function due to the output voltage has been chosen to be a direct control target. The sum of inductor current is selected plus slope compensation as a direct control target which may lead to a stability of switching operation; Equation 50 shows the switching function selected (Kavitha & Uma, 2011).

$$S = i_{L1} + i_{L2} - I_{ref} = 0 \tag{50}$$

This equation insures stable operation of the hysteretic current-mode control, because the switching function is defined, and minimizes the current error; additionally it follows the control law (Kavitha & Uma, 2011).

The switching current control law is:

$$U = \begin{cases} 1\,; & S < 0 \\ 0\,; & S > 0 \end{cases} \tag{51}$$

Here

$$U = \begin{cases} 1; & S < -\delta \\ 0; & S > \delta \end{cases} \tag{52}$$

Where delta ($\delta$) is a positive constant known as the width of hysteresis use to limit the switching frequency; the sum of inductor currents operates on the surface as depicted in Figure 4-16 below. The average state-space equations of the inductor currents and the capacitor voltage in terms of the control law are given in the Equation 53 below (Kavitha et al., 2008).

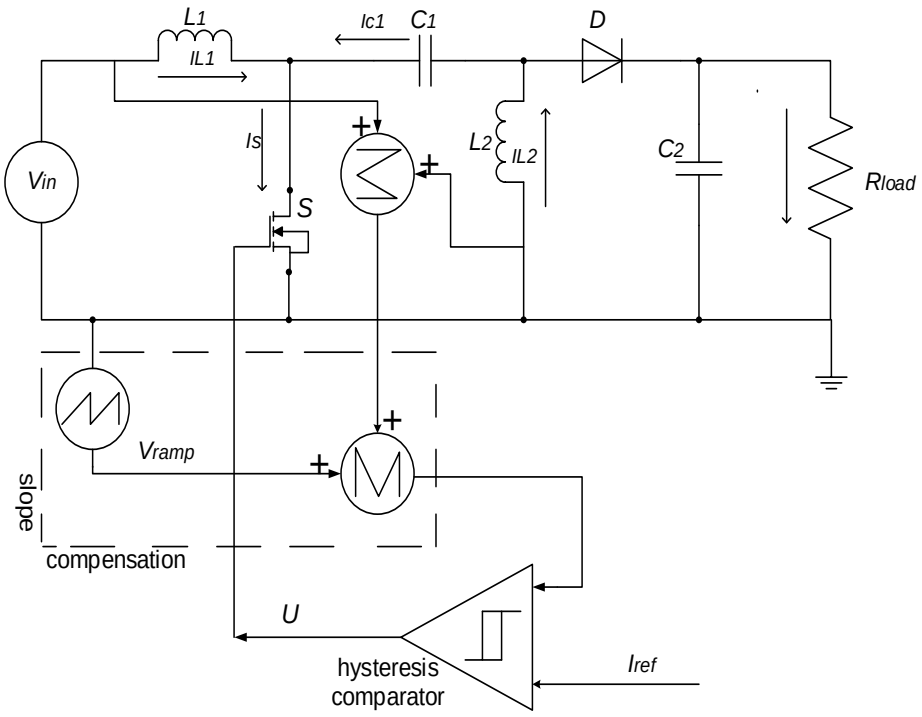


**Figure 4-15: Hysteretic current-mode control with slope compensation DC–DC SEPIC**

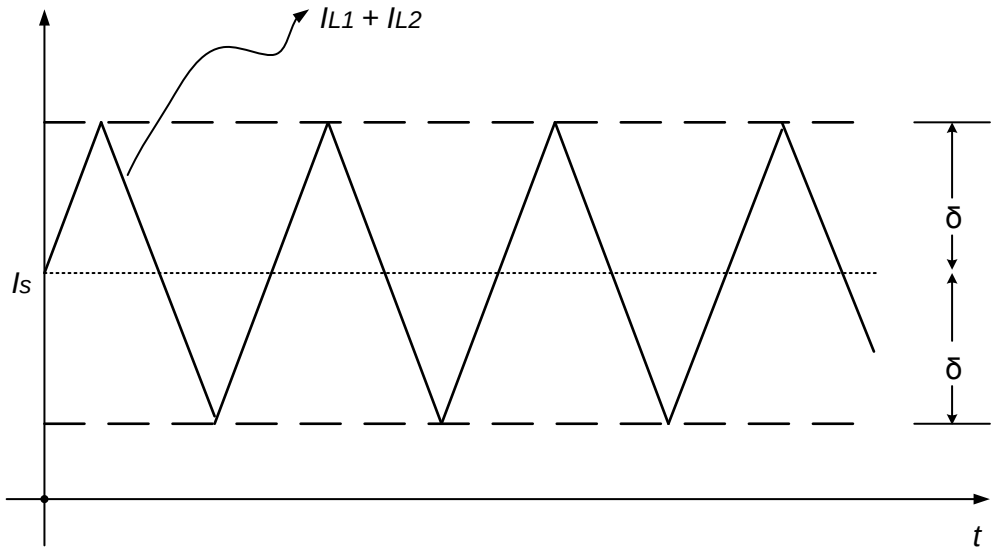


**Figure 4-16: Control signal waveform of the hysteretic current-mode control SEPIC**

$$\begin{pmatrix} \frac{di_{L1}}{dt} = -\frac{v_{C1}+v_{C2}}{L_1} + U\frac{(v_{C1}+v_{C2})}{L_1} + \frac{V_{in}}{L_1} \\ \frac{di_{L2}}{dt} = \frac{v_{C2}}{L_2} + U\frac{(v_{C1}+v_{C2})}{L_2} \\ \frac{dv_{C1}}{dt} = \frac{i_{L1}}{C_1} - U\frac{(i_{L1}+i_{L2})}{C_1} \\ \frac{dv_{C2}}{dt} = \frac{(i_{L1}+i_{L2})}{C_2} - \frac{v_{C2}}{RC_2} - U\frac{(i_{L1}+i_{L2})}{C_2} \end{pmatrix} \quad (53)$$

On the switching function;

$$\dot{S} = \dot{\iota_{L1}} + \dot{\iota_{L2}} = 0 \quad (54)$$

The equivalent control on the switching function is calculated using Equation 54 and Equation 55:

$$U_{eq} = \frac{(v_{C1}+v_{C2}-V_{in})L_2 + v_{c2}L_1}{(V_{C1}+V_{C2})(L_1+L_2)} \quad (55)$$

The equilibrium point is setting the partial derivatives of Equation 54 equal to zero:

$$\frac{di_{L1}}{dt} = \frac{di_{L2}}{dt} = \frac{dv_{C1}}{dt} = \frac{dv_{C2}}{dt} = 0 \quad (56)$$

Solving Equation 56, results in:

$$\begin{cases} \dot{\iota_{L1}} = \frac{\left[2RI_{ref} + V_{in} - \sqrt{4RI_{ref}V_{in} + (V_{in})^2}\right]}{2R} \\ \dot{\iota_{L2}} = \frac{\left[-V_{in} + \sqrt{4RI_{ref}V_{in} + (V_{in})^2}\right]}{2R} \\ \dot{v_{C1}} = V_{in} \\ \dot{v_{C2}} = \frac{\left[V_{in} + \sqrt{4RI_{ref}V_{in} + (V_{in})^2}\right]}{2} \end{cases} \quad (57)$$

With the standard function for switching, the fourth-order system is reduced to a third-order system. The dynamic equations stability analysis for the system in third-order is given by Equation 58;

$$\begin{cases} \dfrac{di_{L1}}{dt} = f_1(i_{L2}, v_{C1}, v_{C2}) = -\dfrac{v_{C2}}{L_2} + \dfrac{(v_{C1} + v_{C2} - V_{in})L_2 + v_{C2}L_1}{(L_1 + L_2)L_2} \\ \dfrac{dv_{C1}}{dt} = f_2(i_{L2}, v_{C1}, v_{C2}) = \dfrac{i_{L1}}{C_1} - \dfrac{(v_{C1} + v_{C2} - V_{in})L_2 + v_{C2}L_1}{(v_{C1} + v_{C2})(L_1 + L_2)C_2} I_{ref} \\ \dfrac{dv_{C2}}{dt} = f_3(i_{L2}, v_{C1}, v_{C2}) = -\dfrac{v_{C2}}{RC_2} + \dfrac{v_{C1}L_1 + V_{in}L_2}{(v_{C1} + v_{C2})(L_1 + L_2)C_2} I_{ref} \end{cases} \quad (58)$$

### 4.8.7 Stability analysis of hysteretic current-mode control

The stability of the DC–DC SEPIC using hysteretic current-mode control, can be analyzed by creating a Jacobian matrix, which can be derived from Equation 59. The Jacobian matrix, evaluated at the equilibrium point, is presented as:

$$J(X_e) = \begin{bmatrix} \dfrac{\partial f_1}{\partial i_{L2}} & \dfrac{\partial f_1}{\partial v_{C1}} & \dfrac{\partial f_1}{\partial v_{C2}} \\ \dfrac{\partial f_2}{\partial i_{L2}} & \dfrac{\partial f_2}{\partial v_{C1}} & \dfrac{\partial f_2}{\partial v_{C2}} \\ \dfrac{\partial f_3}{\partial i_{L2}} & \dfrac{\partial f_3}{\partial v_{C1}} & \dfrac{\partial f_3}{\partial v_{C2}} \end{bmatrix}_{(i_{L1}, i_{L2}, v_{C1}, v_{C2}) = (i_{\dot{L}1}, i_{\dot{L}2}, v_{\dot{C}1}, v_{\dot{C}2})} \quad (59)$$

The equilibrium point of the eigenvalues is calculated from:

$$det = [\lambda I - J(X_e)] = 0 \quad (60)$$

Then,

$$= \begin{bmatrix} 0 & \dfrac{1}{L_1 + L_2} & 0 \\ -\dfrac{1}{C_1} & \dfrac{L_1 v_{C2}^{\cdot} - L_2 V_{in}}{C_1(L_1 + L_2)(v_{C1}^{\cdot} + v_{C2}^{\cdot})^2} I_{ref} & \dfrac{L_1 v_{C1}^{\cdot} + L_2 V_{in}}{C_1(L_1 + L_2)(v_{C1}^{\cdot} + v_{C2}^{\cdot})^2} I_{ref} \\ 0 & \dfrac{L_1 v_{C2}^{\cdot} + L_2 V_{in}}{C_1(L_1 + L_2)(v_{C1}^{\cdot} + v_{C2}^{\cdot})^2} I_{ref} & -\dfrac{1}{RC_2} - \dfrac{L_1 v_{C2}^{\cdot} + L_2 V_{in}}{C_1(L_1 + L_2)(v_{C1}^{\cdot} + v_{C2}^{\cdot})^2} I_{ref} \end{bmatrix} \quad (61)$$

By increasing the values of the reference current (Table 4.1), the stability of the system is determined by the eigenvalues for each value of the reference current (from 5 A to 15 A). The hysteretic current-mode control system operates at a stable state up to a reference current of 14 A. Figure 4-17 and Figure 4-18 have shown how the eigenvalues increased for each value of the reference current; the real part decreases negatively; however, at the critical reference

current (15 A) the real part goes to zero and the operating point becomes unstable (He et al., 2010).

**Table 4.1: Eigenvalues for different values of reference current**

| $I_{ref}$ [A] | Eigenvalues | Results |
|---|---|---|
| 5 | -8469, -678 ± 21649i | stable |
| 6 | -8582, -602 ± 2164i | stable |
| 7 | -8675, -524 ± 21635i | stable |
| 10 | -8880, -296 ± 2161i | Stable |
| 12 | -8982, -149 ± 21588i | Stable |
| 14 | -9066, -892 ± 21569i | Stable |
| 15 | -9103, 61 ± 21557i | unstable |

It can be seen that the average current mode control is the best method to control the current and the voltage of a full-bridge DC–DC converter. It was decided that hysteretic current-mode control and voltage mode control would be sufficiently to prove the robustness and efficiency of the DC–DC converter feedback loop. A hysteretic current-mode control scheme was chosen because of the dynamic response of the converter, and the voltage mode control scheme was selected based on its simplicity and its slow response due to the line and load regulation been acceptable for this application. The performance of both schemes was tested subsequently by using PSIM add-on SmartCtrl.

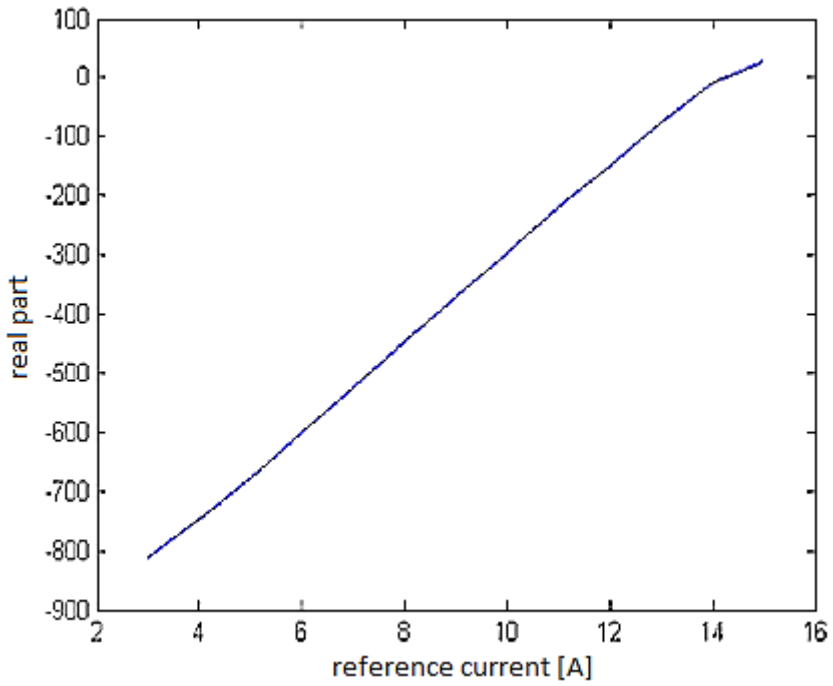


**Figure 4-17: Eigenvalues real part complex.**

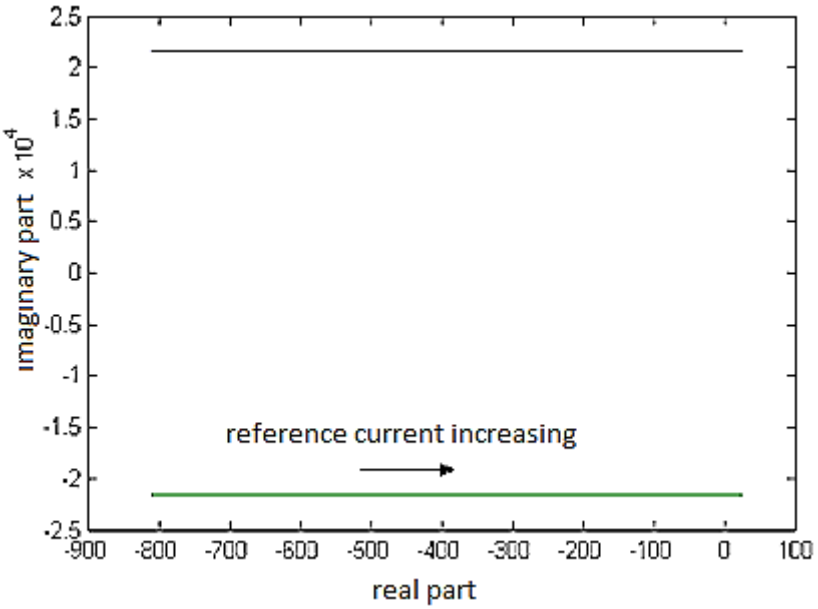


**Figure 4-18: Eigenvalues when Iref increased (loci complex)**

### 4.8.8 Slope compensation theory

The pulse width modulation function exists for current-mode control, except the ramp signal is created by monitoring the inductor current. This signal consists of two parts, namely: the AC current ripple, and the average value of the inductor current. The output signal of the current sensing amplifier is added to a voltage ramp signal through the resistor at the inverting input

signal of the pulse width modulation comparator. The ideal steady-state modulator gain for current-mode control can be adapted depending on whether the voltage ramp is proportional, or fixed, to a particular mix of the inductor current and bias current. Additional modification of the DC gain can be achieved when input and output signals are perturbed to generate the actual small-signal terms (Zhongjie et al., 2010).

However, despite small-signal modification of the ideal steady-state value, the concepts are still justifiable. Under specific working conditions, instability can result if there is a difference between the average inductor current and the DC value of the sampled indicator current. This type instability is known as sub-harmonic oscillation which exists when the ripple current of the inductor does not return to its initial magnitude for the following switching cycle (Zhongjie et al., 2010).

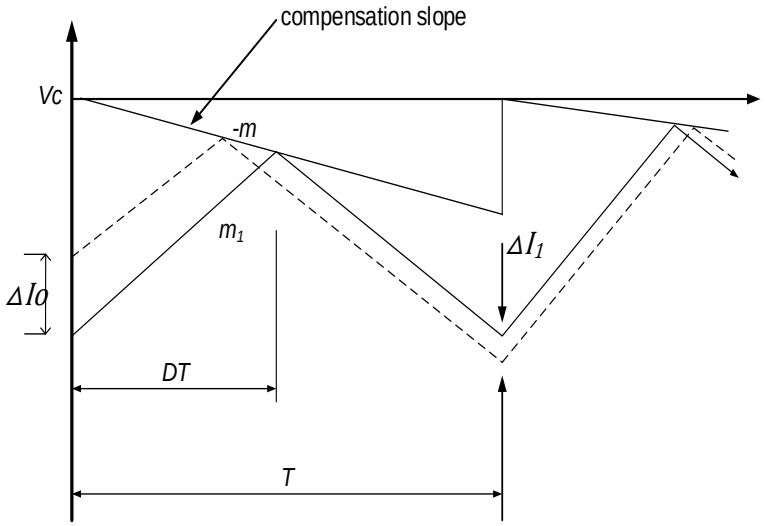


**Figure 4-19: Loop curve with slope compensation**

When alternating wide and narrow pulses at the switch are noted, it usually indicates the occurrence of sub-harmonic oscillation. An extra ramp (slope compensation) added to the current-sensing signal prevents this type of oscillation. To prevent subharmonic oscillation when PWM with duty-cycles in excess of 50% occur, the fixed frequency current-mode converters require slope compensation (Zhongjie et al., 2010).

The higher the duty-cycle is, the greater the slope compensation required. Figure 4-19 depicts the working principle of slope compensation. The output signal, $V_c$ of error amplifier; the inductor current graph with no distortion is represented by the solid line: the dotted line is the inductor current graph with distortion $\Delta Io$: D is the duty-cycle; T is the switching cycle;

$m_1$ is the slope of rising inductor current, $m_2$ is the slope of falling inductor current. If there is no slope compensation, $m_1$ and $m_2$ can be derived from the Equation 62 and 63 respectively (Zhongjie et al., 2010).

$$m_1 = \frac{V_{in} - V_{out}}{L} \tag{62}$$

$$m_2 = \frac{V_{out}}{L} \tag{63}$$

In continuous conduction mode (CCM),

$$\frac{m_2}{m_1} = -\frac{D}{1 - D'} \tag{64}$$

$$\Delta I_1 = \Delta I_0 \frac{m_2}{m_1} \tag{65}$$

From Equation 62, it can be seen that if the duty-cycle is less than 50%, $\Delta I_1$ is attenuated periodically and the system loop is conclusive, however if the duty-cycle is larger than 50%, $\Delta I_1$ increases periodically, the system loop is aborted and the loop is unstable. Therefore slope compensation is introduced to stabilize the loop (Zhongjie et al., 2010).

### 4.9 Compensation network

A switched-mode power converter requires a compensation network circuit for improved stability. A compensation network provides a closed-loop control system with an appropriate phase margin at the selected crossover frequency point, and a high DC gain. There are many ways to implement a compensation network circuit for use in improving the stability of a DC–DC power converter. These compensation circuits work by assembling poles and zeros into the closed-loop system response of a DC–DC converter; its decreases or increases the phase and the gain of the closed-loop system response. A phase boost is required at the crossover frequency in order to obtain a usable phase margin (Basso, 2008).

The type of compensation network circuits discussed here are those stated by Basso (2008), namely: Type 1 compensation, Type 2 compensation, Type 2a and Type 2b compensation, and Type 3 compensation. And had been re-simulated by using LTSpice software package, the circuit uses are an operational amplifier with 60 dB open-loop voltage gain.

### 4.9.1 Type 1 Compensation network (Active Integrator)

Type 1 Compensation network circuit is shown in Figure 4-20, is a basic active integrator circuit with a transfer function as given in Equation 66 (Basso, 2008).

$$G_c(s) = \frac{1}{sR_1C_1} \tag{66}$$

A compensation Type 1 gain is given at the rate of -20 dB/decade while the phase plot stays flat at 90º because of the inverting configuration of the operational amplifier which has a phase shift of -180º; also, the pole at the origin brings an additional -90º. This equates to a phase shift of 270º or +90º, as illustrated in Figure 4-21 (Basso, 2008).

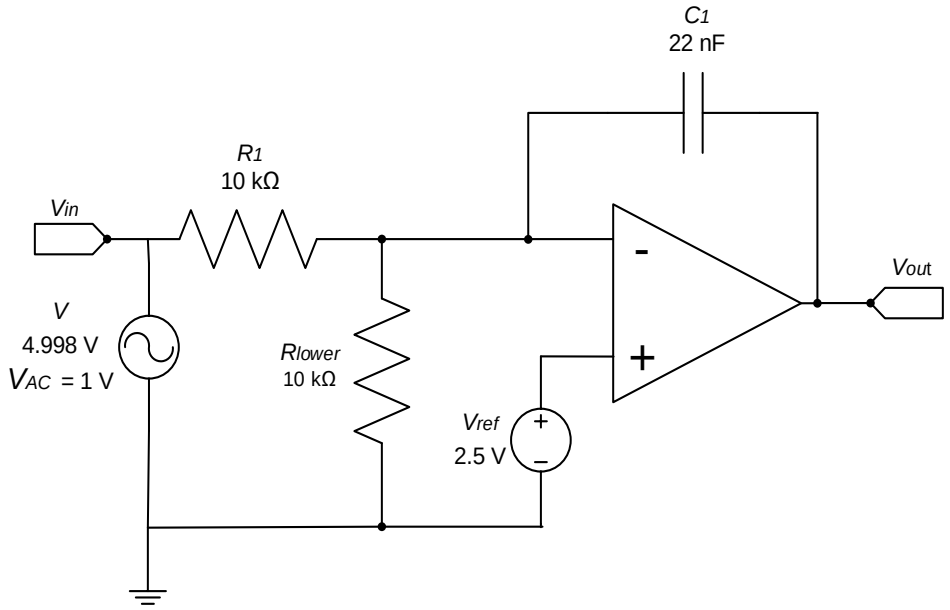


**Figure 4-20: Type 1 Compensation amplifier circuit diagram**

The open-loop gain DC simulation of this type of amplifier configuration has a fixed gain, when $C_1$ (i6867 s) acts like an open circuit; this fixes the gain rate at a value of 60 dB.

Regarding the AC input voltage (Figure 4-20): as the frequency increases the dynamic impedance of $C_1$ decreases, and the closed-loop gain of the amplifier drops at the rate of -20 dB/decade. A voltage divided network ($R_1$ and $R_{lower}$) allows selecting the suitable output voltage as required for a switch-mode power converter (Basso, 2008).

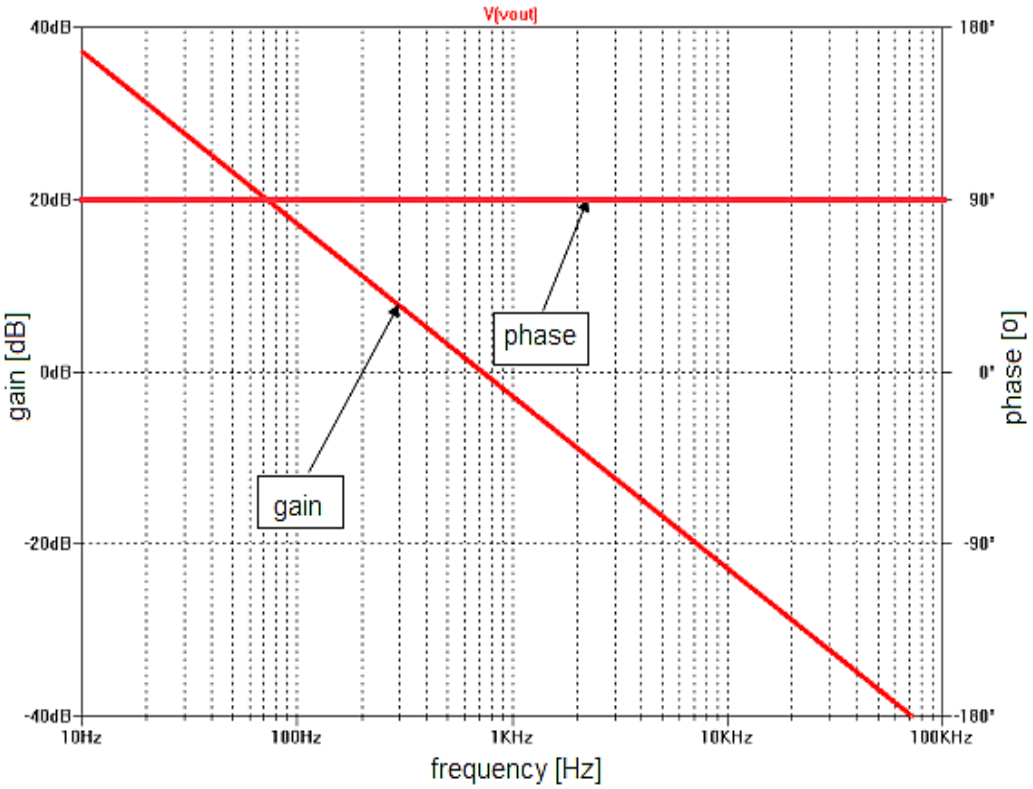


**Figure 4-21: Type 1 Compensation Bode plot amplifier**

### 4.9.2 Type 2 Compensation network (Zero-Pole Pair)

Type 2 Compensation consists of a zero-pole pair and an integrator, and could be used to increase the phase margin of a closed-loop system at crossover frequency, if needed. A Type 2 Compensation amplifier can be seen in Figure 4-22, and the related Bode plot is presented in Figure 4-23. A derived transfer function of this type of compensation is given in the Equation 67 (Basso, 2008).

$$G_c(s) = \frac{1 + sR_2C_1}{sR_1(C_1 + C_2)\left(1 + sR_1\frac{C_1C_2}{C_1 + C_2}\right)} \tag{67}$$

By using the Equation 67 above, the zero and poles can be determined.

$$\omega_Z = \frac{1}{R_2C_1} \tag{68}$$

$$\omega_{p1} = \frac{1}{R_1(C_1 + C_2)} \tag{69}$$

$$\omega_{p2} = \frac{1}{R_2\left(\frac{C_1 C_2}{C_1 + C_2}\right)} \tag{70}$$

If $C_2 << C_1$ the Equation 70 can be written as follows:

$$\omega_{p2} = \frac{1}{R_2 C_2} \tag{71}$$

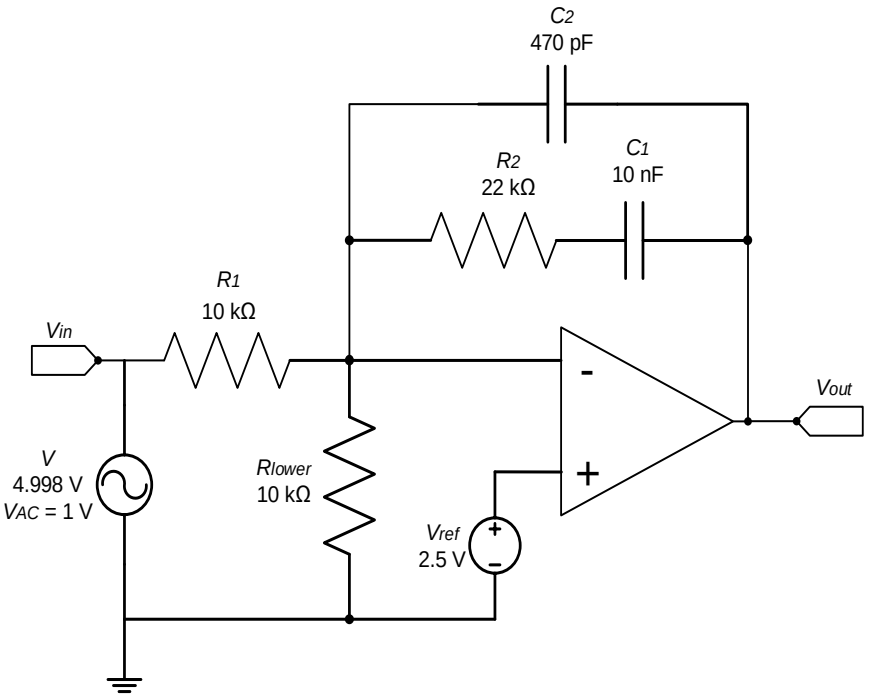


**Figure 4-22: Type 2 Compensation amplifier circuit diagram.**

The distance between the zero and pole positions, determines the quantity of the phase boost that can be delivered by this kind of compensation network.

An increase in phase, phase boost, occurs between the zero-pole pair. The geometric mean value of the peak boost is located between zero and pole (Basso, 2008).

Similarly to a Type 1, the amplifier configuration produces an open loop gain when implementing the DC analysis. The pole origin is defined by Equation 69. The pole causes the gain to roll off at a slope of -1 or -20 dB/decade from the origin, as the frequency increases. The zero effect is illustrated in Figure 4-23 at roughly 1 kHz.

The zero keeps acting as the frequency increases, up to the final pole start position to affect the gain and phase of the system. The final pole position effectively counteracts the previous

zero, bringing the phase down to 90º; and the gain of the slope is -20 dB/decade. The effect of the end pole is illustrated at 10 kHz in Figure 4-23 (Basso, 2008).

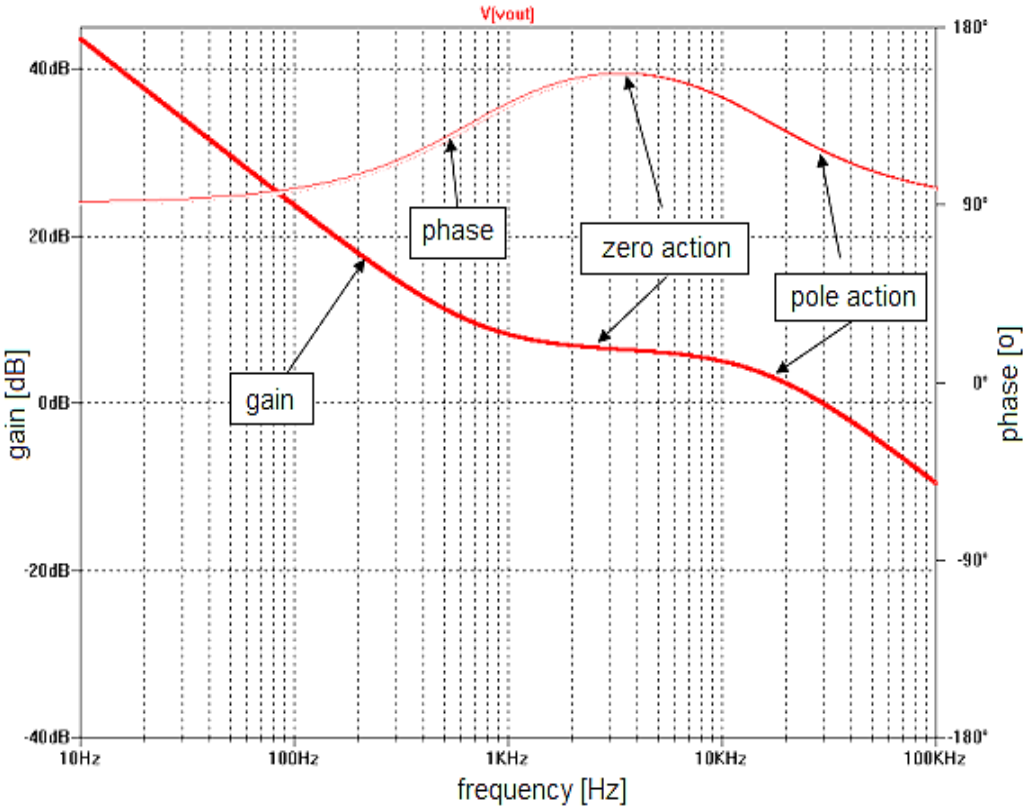


**Figure 4-23: Type 2 Compensation Bode plot amplifier**

### 4.9.3 Type 2a Compensation network (origin pole plus a zero)

The Type 2a Compensation network amplifier is the same as the Type 2 Compensation networks, except that the Type 2a has no $C_2$ capacitor (Figure 4-24); this omission eliminates the high frequency pole associated with Type 2 compensation. Equation 72 shows a transfer function of a Type 2a Compensation network, with the zero and pole given respectively by Equation 73 and Equation 74 (Basso, 2008).

$$G_c(s) = \frac{1 + sR_2C_1}{sR_1C_1} \tag{72}$$

$$\omega_z = \frac{1}{R_2C_1} \tag{73}$$

$$\omega_p = \frac{1}{R_1C_1} \tag{74}$$

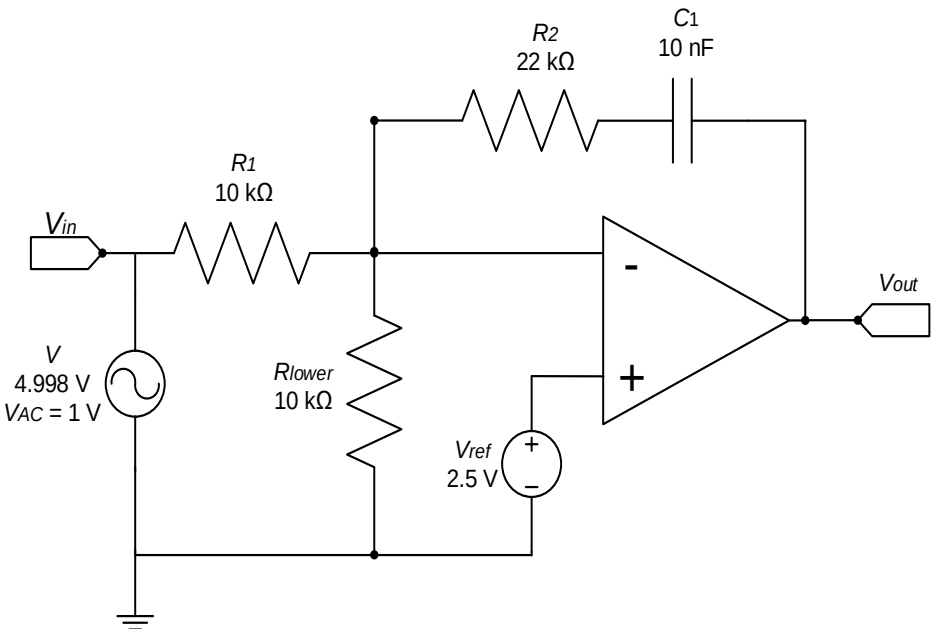


**Figure 4-24: Type 2a Compensation amplifier circuit diagram**

Implementing Type 1 and 2 compensation network amplifiers, the DC response results in an open loop gain the operational amplifier. This compensation network type is merely a modified model of Type 2 Compensation where capacitor $C_2$ has been omitted. By removing $C_2$, the high frequency pole is no longer exists and the system exhibited a pole at the origin and a zero (Basso, 2008).

The pole at the origin causes a slope of -20 dB/decade between the origin and the zero with a phase shift of 90$^o$ (Figure 4-25). Increasing of the frequency affects the response of the amplifier at the starting zero; this causes the slope of the gain to increase to 0 dB/decade, and the phase boost to go through 90$^o$ resulting in a phase of 180$^o$ (Basso, 2008).

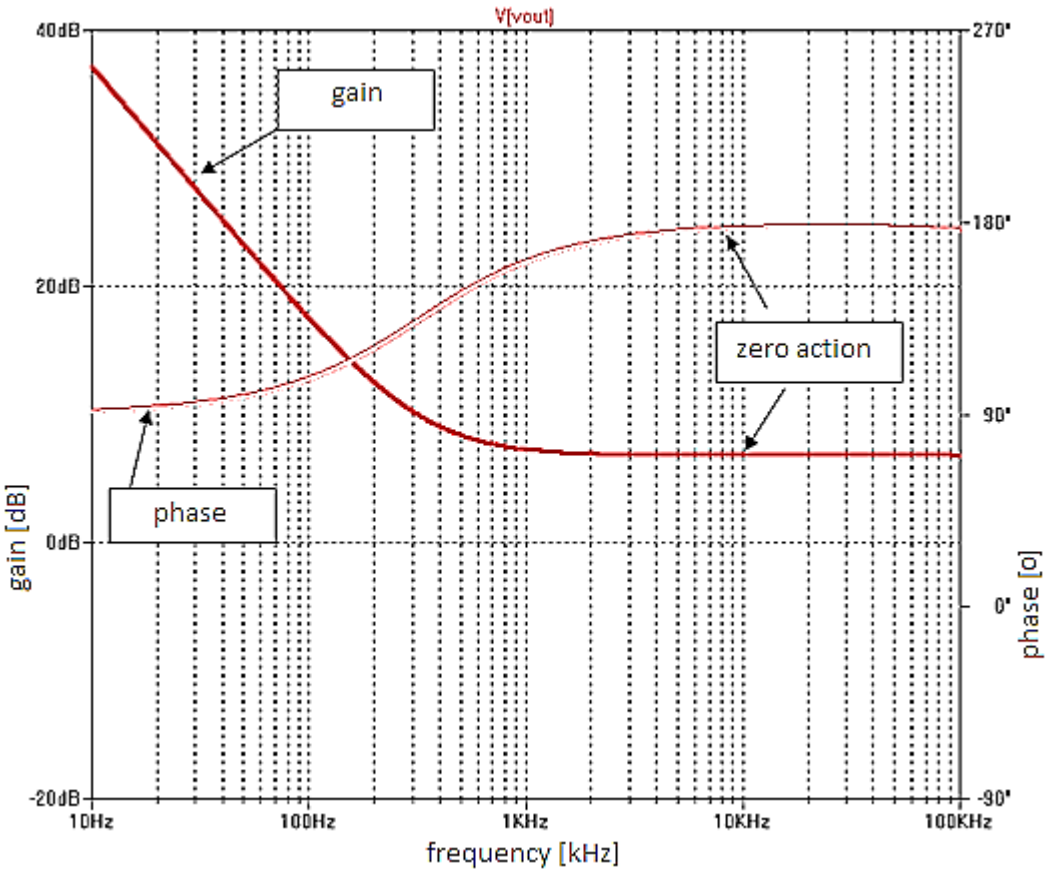


**Figure 4-25: Type 2a Compensation Bode plot amplifier**

### 4.9.4 Type 2b Compensation network (proportional plus a pole)

Figure 4-26; illustrated the Type 2b Compensation network amplifier, this type of amplifier produces a flat gain, governed by $R_1$ and $R_2$. This flat gain changes when then the pole imposed by $C_1$ becomes effective, as can be seen on the Bode plot in Figure 4-27. The transfer function of Type 2b Compensation network amplifier is depicted by Equation 75 and the pole location is defined by Equation 76 (Basso, 2008).

$$G_c = \frac{R_2}{R_1}\frac{1}{1 + sR_2C_1} \tag{75}$$

$$\omega_P = \frac{1}{R_2C_1} \tag{76}$$

As mentioned, the gain of this type of compensation network amplifier remains flat from the origin frequency domain, until the pole starts to affect the response of the amplifier. The gain decreases at a slope of -20 dB and the phase changes from 0º to 180º due the pole.

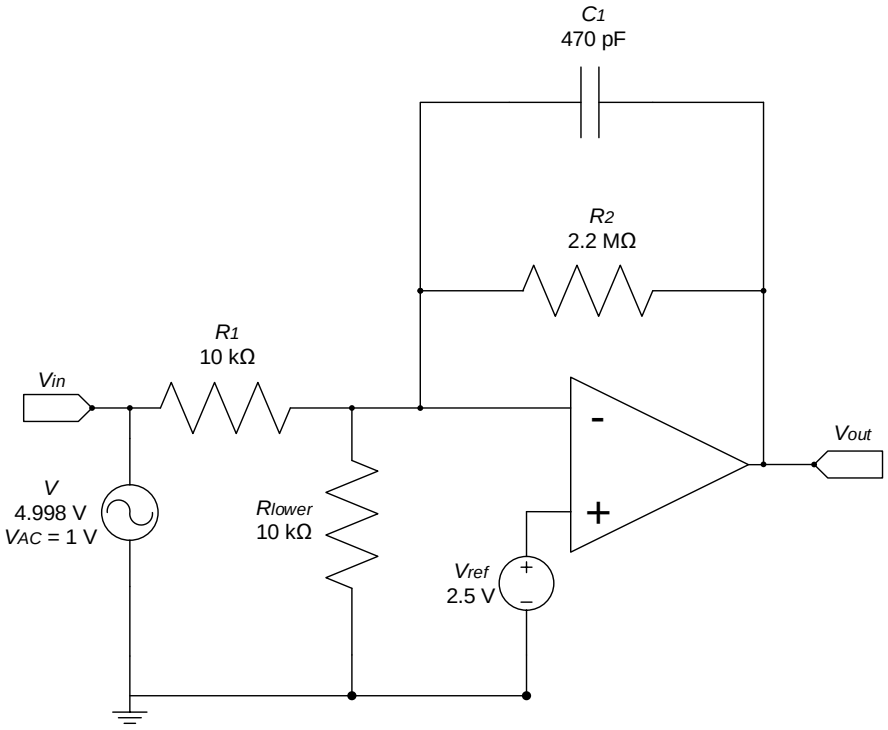


**Figure 4-26: Type 2b Compensation amplifier circuit diagram**

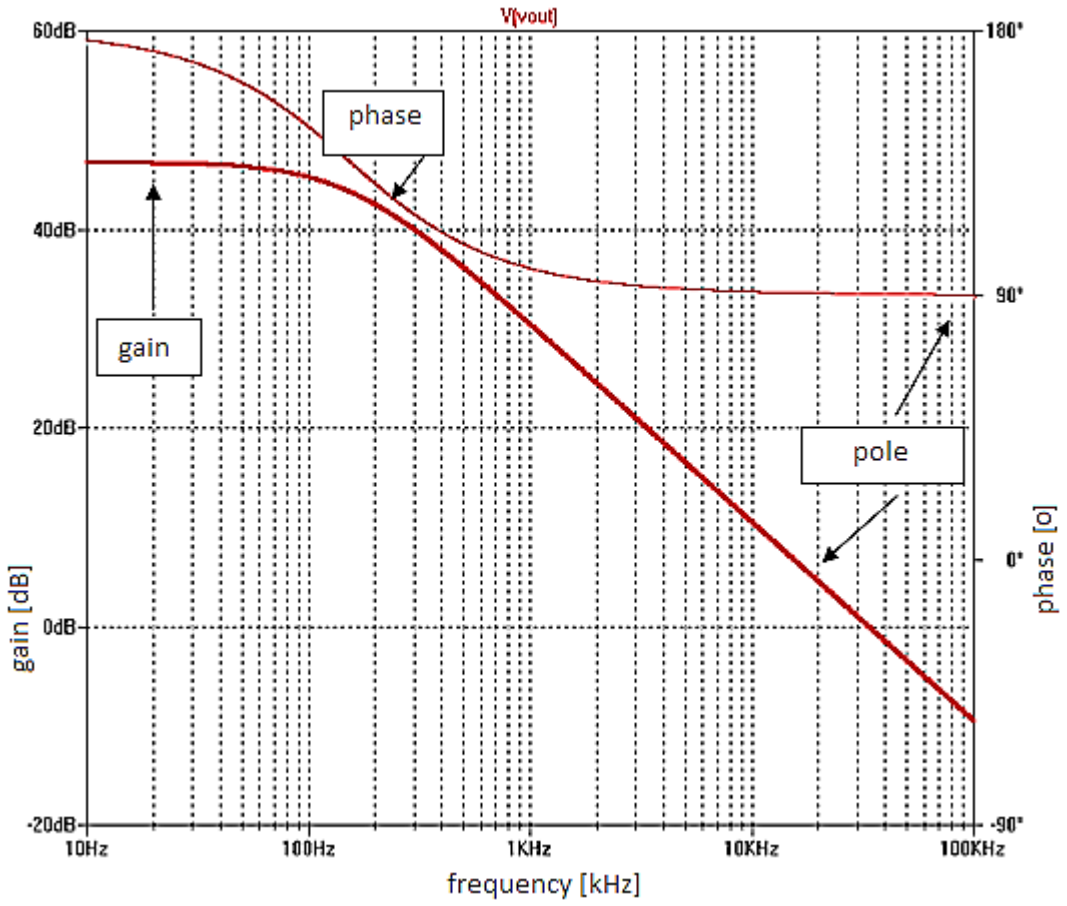


**Figure 4-27: Type 2b Compensation Bode plot amplifier**

### 4.9.5 Type 3 Compensation network (origin pole plus town coincident zero-pole pairs)

Type 3 Compensation network amplifiers are suitable where a substantial phase boost is required, such as in the case of a switch-mode converter operating in constant conduction mode (CCM) and a second-order response when operating in voltage mode (Basso, 2008).

The response of Type 3 amplifier consists of a pole at the origin and two coincident zero-pole pairs. A Type 3 configuration can be seen in Figure 4-28 and the corresponding Bode plot is illustrated in Figure 4-29. The derive transfer function of Type 3 Compensation is given by Equation 77, and assuming $C_2$<<$C_1$, and $R_3$<<$R_1$, the poles and zero are derived in Equation 78 to Equation 82 assuming $C_2$<<$C_1$, and $R_3$<<$R_1$ (Basso, 2008).

$$G_c(s) = \frac{sR_2C_1 + 1}{sR_1(C_1 + C_2)\left(1 + sR_2\frac{C_1C_2}{C_1 + C_2}\right)}\frac{sC_3(R_1 + R_3) + 1}{(sR_3C_3 + 1)} \qquad (77)$$

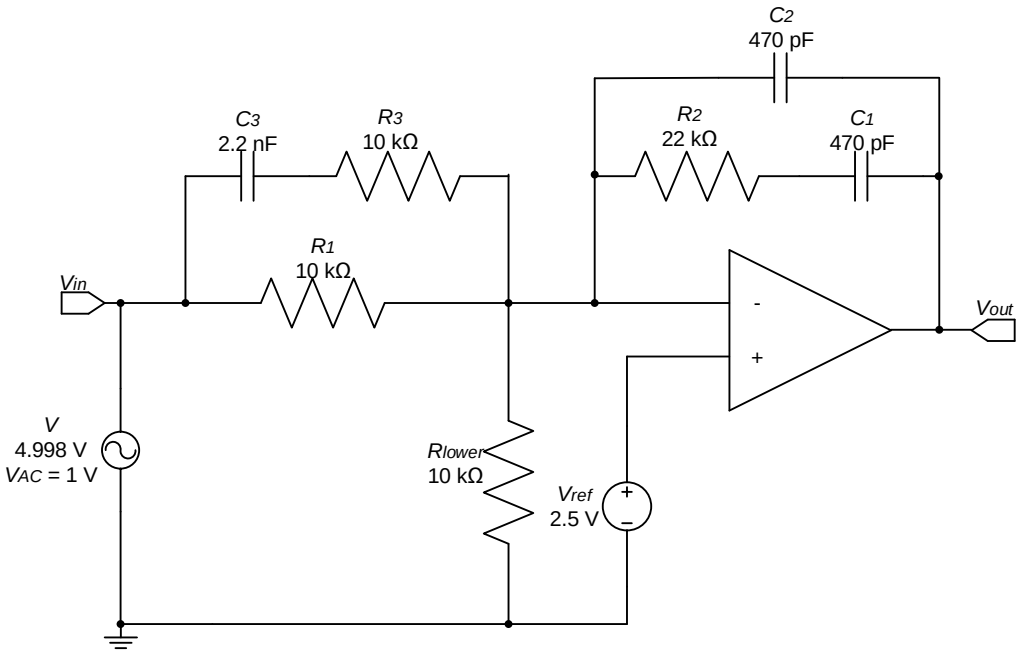


**Figure 4-28: Type 3 Compensation amplifier circuit diagram**

$$\omega_{z1} = \frac{1}{R_2 C_1} \tag{78}$$

$$\omega_{z2} = \frac{1}{R_1 C_3} \tag{79}$$

$$\omega_{PO} = \frac{1}{R_1 C_1} \tag{80}$$

$$\omega_{P1} = \frac{1}{R_3 C_3} \tag{81}$$

$$\omega_{P2} = \frac{1}{R_2 C_2} \tag{82}$$

As seen for Type 1, 2 and 2a compensation networks; the DC gain of Type 3 amplifier is an open loop gain of the operational amplifier. Regarding an AC response, this amplifier has a 20 dB/decade slope from the origin through the double zero (Basso, 2008).

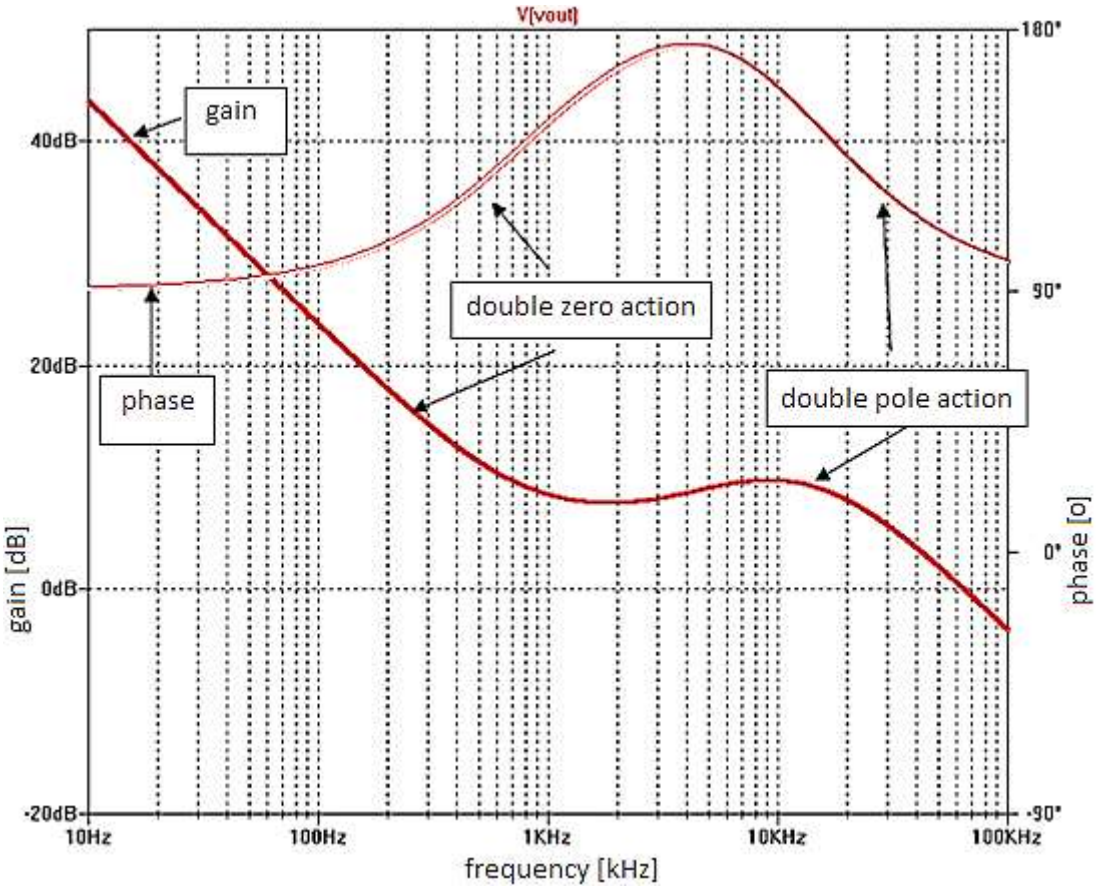


**Figure 4-29: Type 3 Compensation Bode plot amplifier**

As the double zero action starts to act, the response of the amplifier increases both in the frequency slope, as well as the gain, this results in a slope gain of +20 dB/decade. The double zero pair also introduces a phase boost. As the frequency increases; the double pole begins to react on the amplifier response causing the slope of the gain to go back to -20 dB/decade and the phase to drop back by 90$^{o}$ (Basso, 2008).

### 4.10 Summary

In this chapter the DC–DC power converter topologies were investigated as well as the control aspects required to maintain a stable system. Additionally, the importance of mathematical modelling and state-space modelling of the DC–DC SEPIC were investigated.

# Chapter 5 : DESIGN AND SIMULATIONS

## 5.1 Overview of the design solution and simulations

This section gives a detailed description of the design procedure to reach the project goal (an electrical power supply subsystem) more specifically a DC–DC converter (SEPIC), and analogue pulse width modulation. A brief overview of the proposed solution is discussed, taking into consideration the implementation of the analogue pulse width modulation, and PI controller design. The section also provides the simulation (Multisim, Psim) results for the above mentioned subsystems.

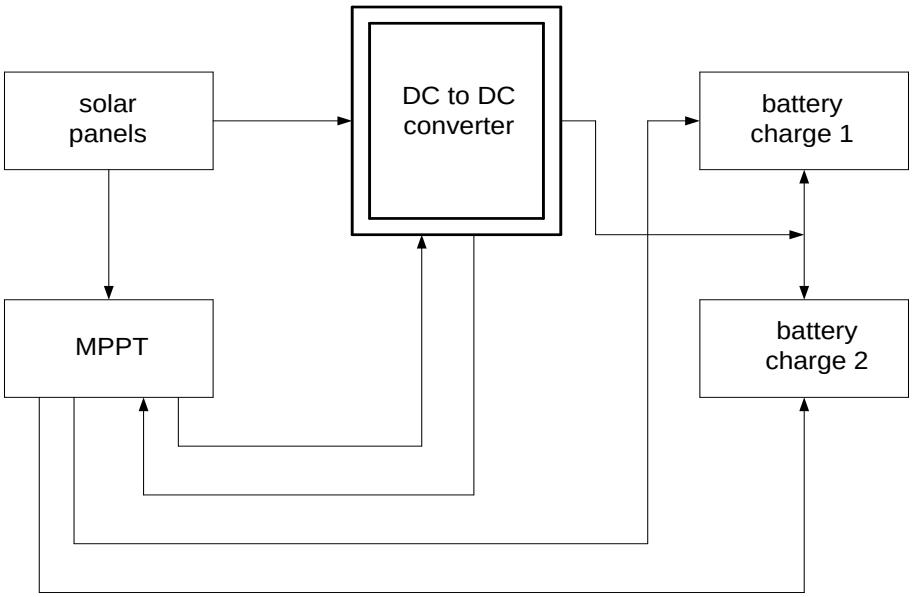


**Figure 5-1: Proposed structure of the design**

Figure 5-1 provides an overview of the structure of the design. It consists of the solar panels, MPPT, control batteries, and the DC–DC converter. In this project the study will be limited to the design of the DC–DC converter (SEPIC) with analogue pulse width modulation, and a PI controller (Figure 5-2); this subsystem will receive its input from a solar panel, and deliver its output to charge a battery pack.

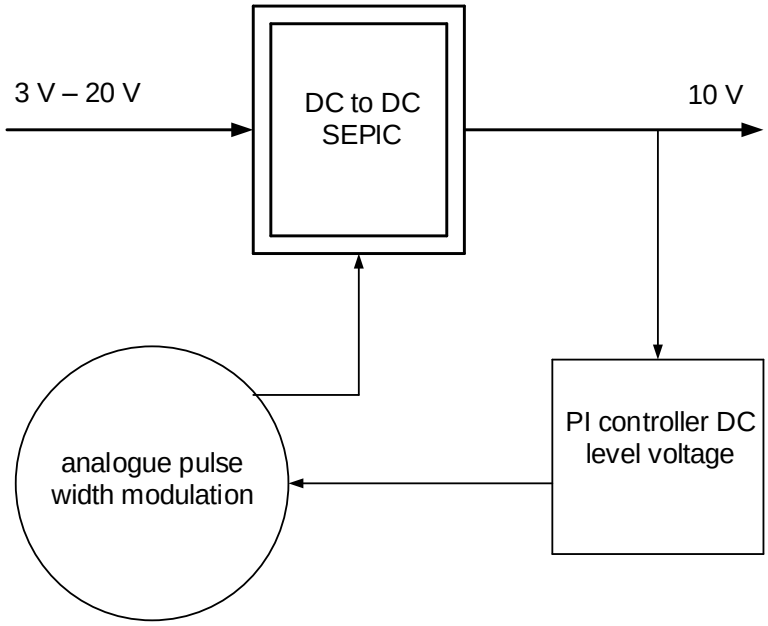


**Figure 5-2: SEPIC, analogue PWM, and PI controller block diagram**

### 5.2 Analogue pulse width modulation

Pulse width modulation signals consist of two main components that define its behaviour; the duty-cycle and the frequency. With reliability and flexibility as the target, the design of the analogue pulse width modulation will be as shown in Figure 5-3:

Figure 5.3 provides an overall view of the proposed analogue pulse width modulation. This figure is composed of:

- An oscillator block, where the frequency will be generated;
- An integrator block where the signal from the oscillator is integrated and produces a negative triangular wave form;
- An inverting amplifier; and
- The pulse width modulation which produces a square wave output voltage by comparing the triangular signal and the constant DC voltage (PI controlled signal).

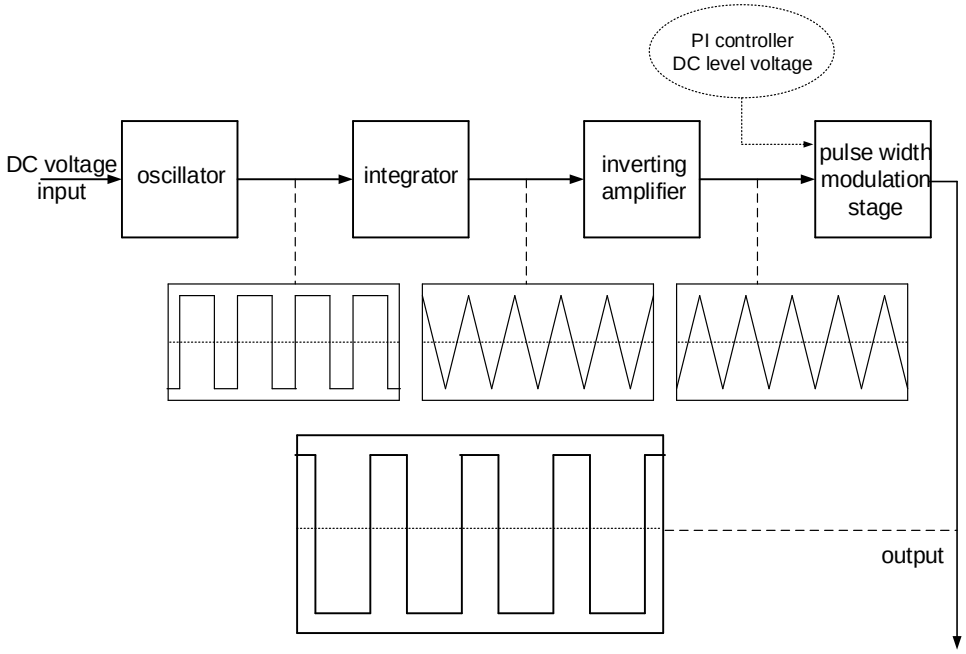


**Figure 5-3: Proposed analogue pulse width module design solution**

### 5.3 Oscillator

An oscillator is a positive feedback control system which generates a self-sustained output without requiring an input signal. Figure 5-4 provides a block diagram of an oscillator and the definition of the oscillator terms (Haile & Lepkowski, 2004) as well as the equation described.

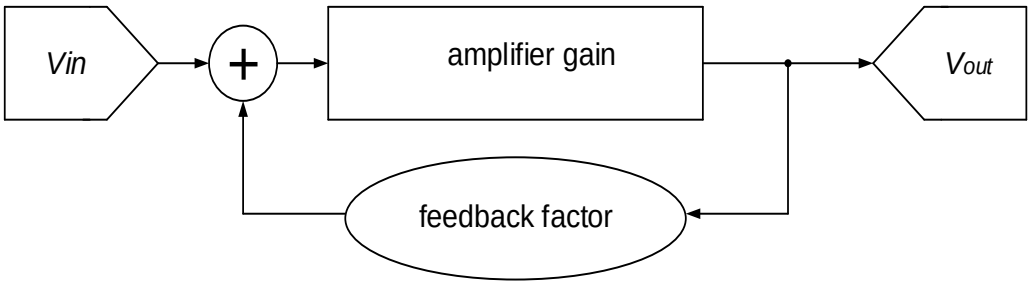


**Figure 5-4: Oscillator block diagram**

$$T_S = \frac{V_{out}}{V_{in}} = \frac{A}{1 - A\beta} = \frac{A}{1 - LG} = \frac{A}{\Delta_S} \tag{82}$$

Where $A$ is the amplifier gain, and $\beta$ feedback factor

$\Delta_S$= characteristic equation if $V_{IN}$ =0, then $T_{(S)}$ = ∞ when

$\Delta_S$= 0.

### 5.4 Relaxation oscillator

The comparator was chosen and configured as a relaxation oscillator, to provide a simple and inexpensive clock output (Figure 5-5). The capacitor is charged at a rate of $0.69RC$; it discharges at the same rate and therefore the period is $1.38RC$. $R_1$ may be different value than other resistors in the circuit (Brown, 2005).

The relaxation oscillator attributes are:

- Low cost solution,
- Single comparator circuit,
- Square wave output, and
- Frequency = 1/ (1.386 x $R_1$ x $C_1$) Hz.

A simplified design procedure has been proposed for selecting the resistors and capacitor $C_1$. The relaxation oscillator design equations may be simplified by selecting the trip point voltages of the comparator circuit to be equal to $\frac{1}{3}V_c$ and $\frac{2}{3}V_c$ ; this achieved making the values of $R_2, R_3$ and $R_4$ equal.

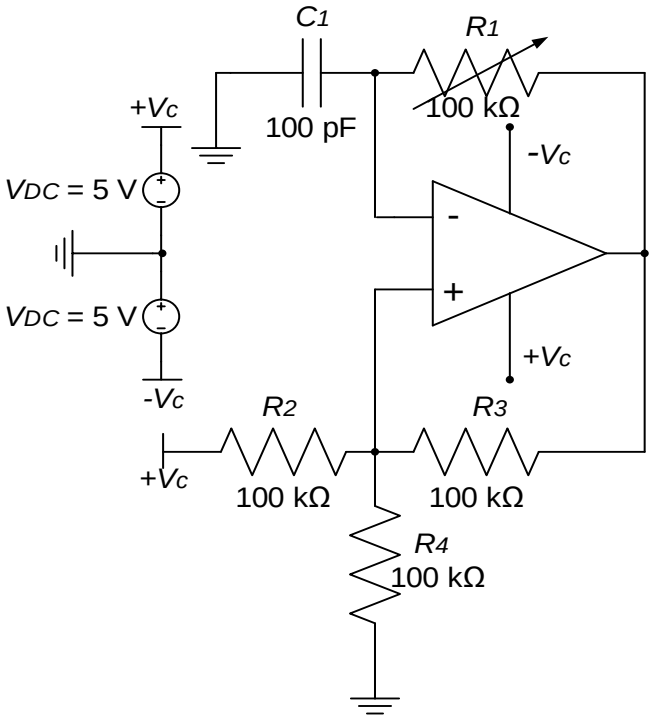


**Figure 5-5: A relaxation oscillator configuration**

Simulating of $\frac{1}{3}V_c$ and $\frac{2}{3}V_c$ from the comparator, results in a voltage waveform at the node-point between $C_1$ and $R_1$, which is depicted in Figure 5-6; Figure 5-7 displays the output voltage of the relaxation oscillator.

### 5.6 Integrator

As its name indicates, the integrator is an operational amplifier circuit that performs a mathematical operation; it is a frequency to voltage converter. It causes the output to respond to changes in the input voltage over time because the operational-amplifier integrator produces an output voltage which is proportional to the integral of the input voltage (Storr, 2015). Equation 84 below indicates the relationship between the output voltage and the integrated input.

$$V_O = -\frac{1}{R_1 C_F}\int_0^T (V_{in}dt + C) \tag{83}$$

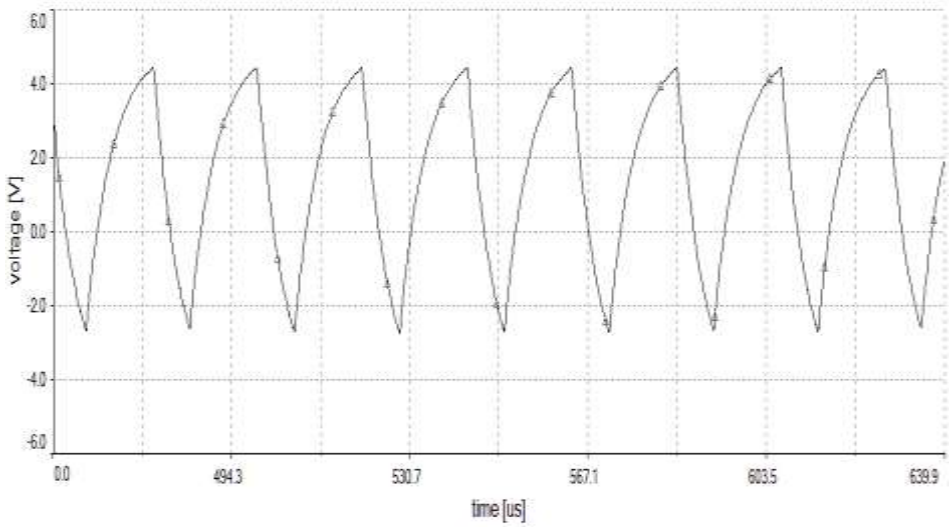


**Figure 5-6: Node-point voltage between $C_1$ and $R_1$**

Normally, only $C_2$ is used as feedback; however to avoid an error voltage at the output, a resistor, $R_5$ is connected across the feedback capacitor $C_2$ (Figure 5-8).

Thus $R_5$ limits low frequency gain and hence minimizes the variations in the output voltage. Roll-off and stability problems may be practically eliminated by the use of an $R_5$ resistor in this manner. Figure 5-9 shows how the input voltage square wave has been integrated into a triangular waveform with a negative voltage level.

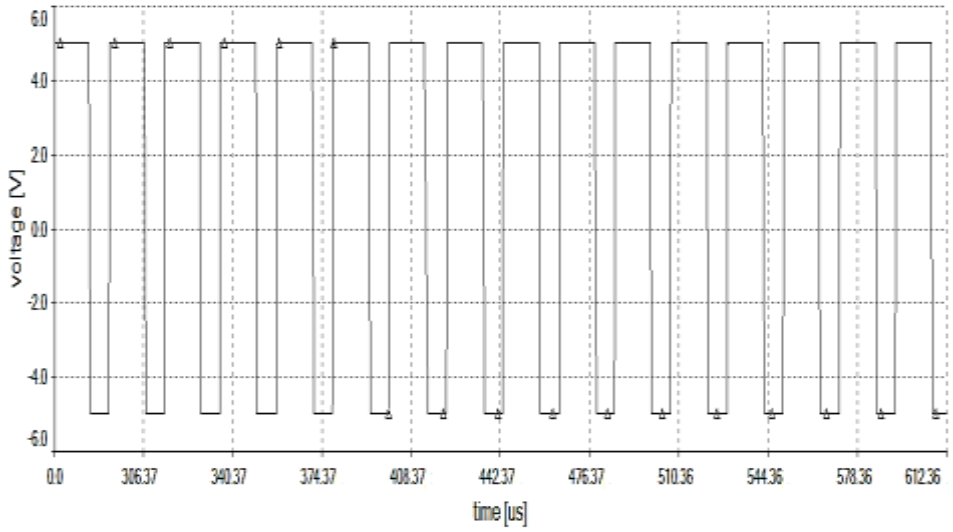


**Figure 5-7: Output voltage of the relaxation oscillator**

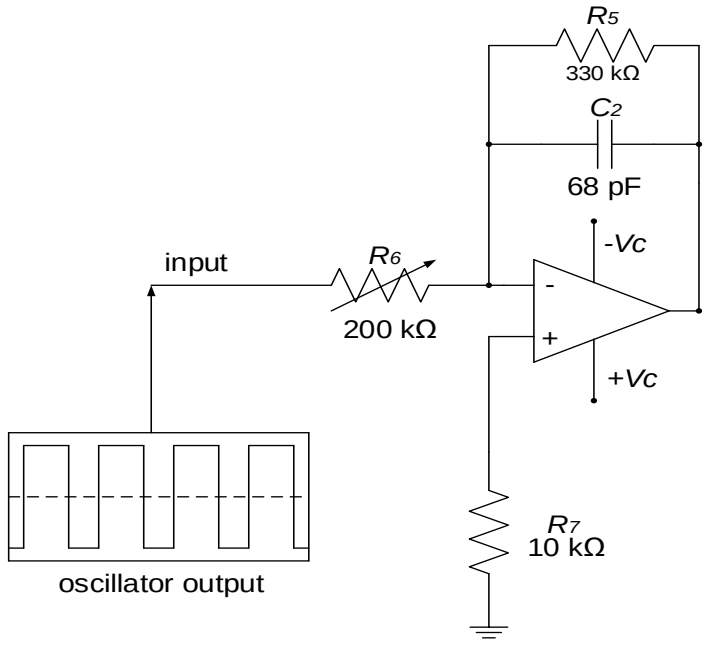


**Figure 5-8: Integrator circuit with a feedback resistor across $C_2$**

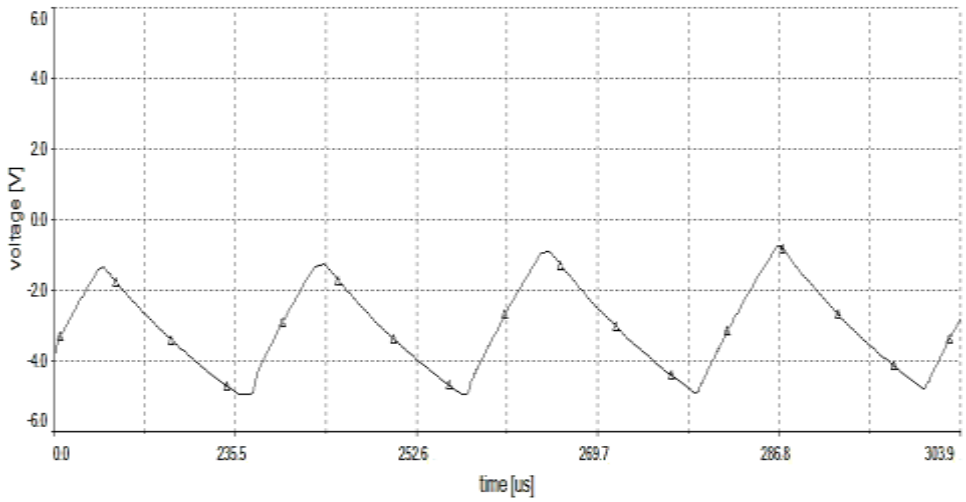


**Figure 5-9: Output voltage of the integrator**

## 5.6 Inverting amplifier

The inverting amplifier is provided to invert the negative output signal from the integrator with a gain of 1. Figure 5-10 illustrates the inverting amplifier circuit diagram. Figure 5-11 displays the output voltage waveform from the inverting amplifier, with this output having a gain of unity.

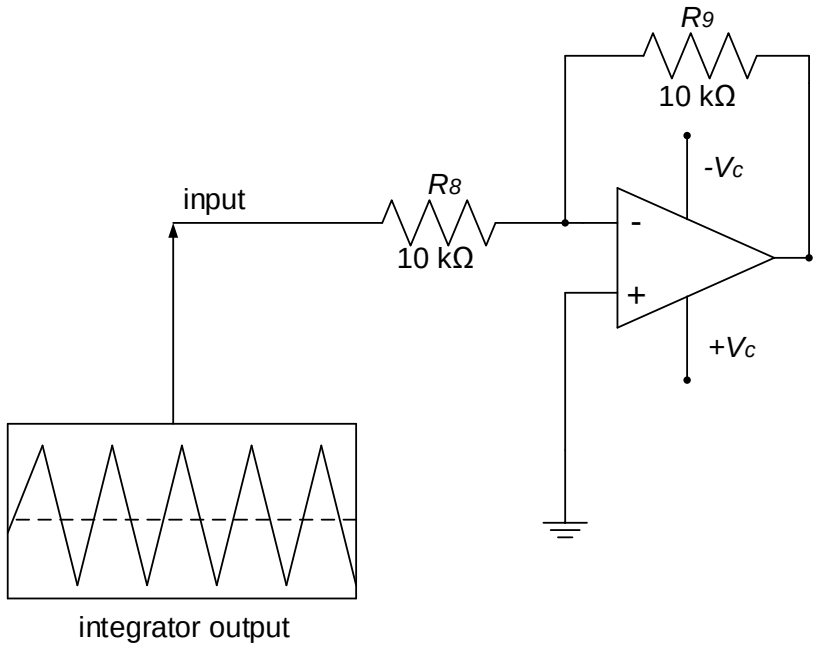


**Figure 5-10: Unity gain inverting amplifier**

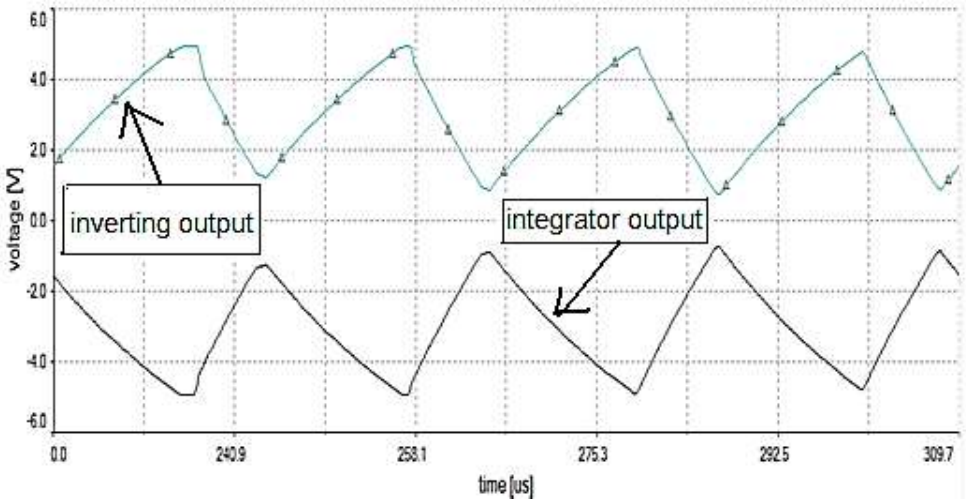


**Figure 5-11: Output voltage signal of the integrator which, after processing by the inverting amplifier, has a gain of unity**

### 5.7 Pulse width modulation stage (duty-cycle)

Pulse width modulation, is a technique applied to control the quantity of power delivered to a load without any power dissipation in the load driver; the output pulse width varies and is dependent on the input signal (Talulah, 2004). It is one the important concepts in the field of analogue electronics. Pulse width modulation can implement by various methods, such as:

- The digital method,
- The discrete IC method,
- The analogue method, and
- The on-board microcontroller method.

In the case of this study, an analogue method is implemented using discrete components.

#### 5.7.1 Analogue method pulse width modulation

The inverting triangular output signal which is compared with the PI controller DC level input (see Figure 5-13). The reference voltage (PI controller DC level) is generated by comparing the two signals from a simple voltage-divide; the reference voltage and the inverting triangular produces the PWM signal (see Figure 5-14) which is connected to MOSFET switch. DC level signal from the PI controller can vary between the maximum and the minimum voltage of the triangle; the higher the DC level of the PI controller, the wider the PWM pulses are.

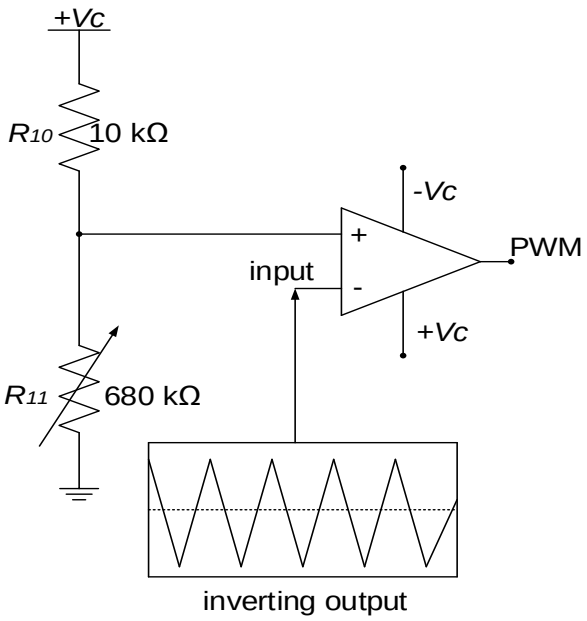


**Figure 5-12: Analogue PWM generator circuit**

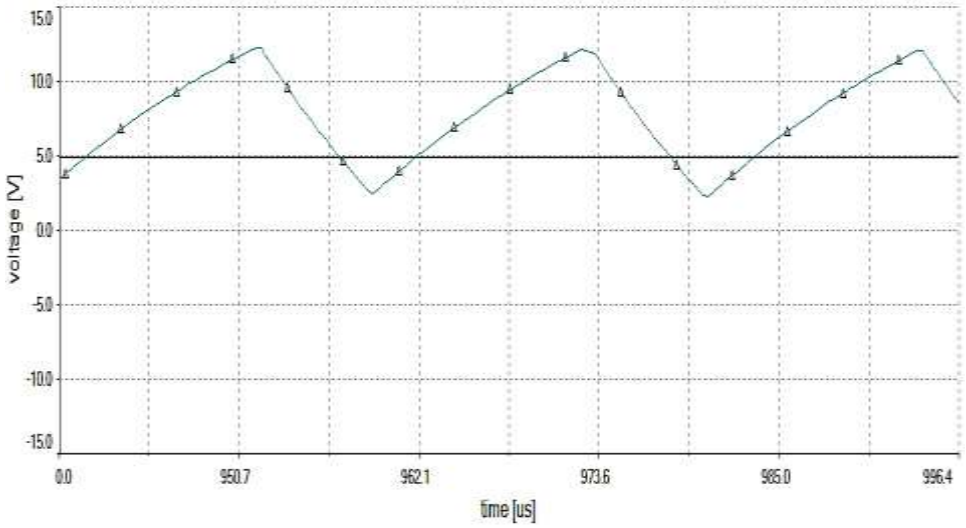


**Figure 5-13: Triangular and the PI controller DC level input**

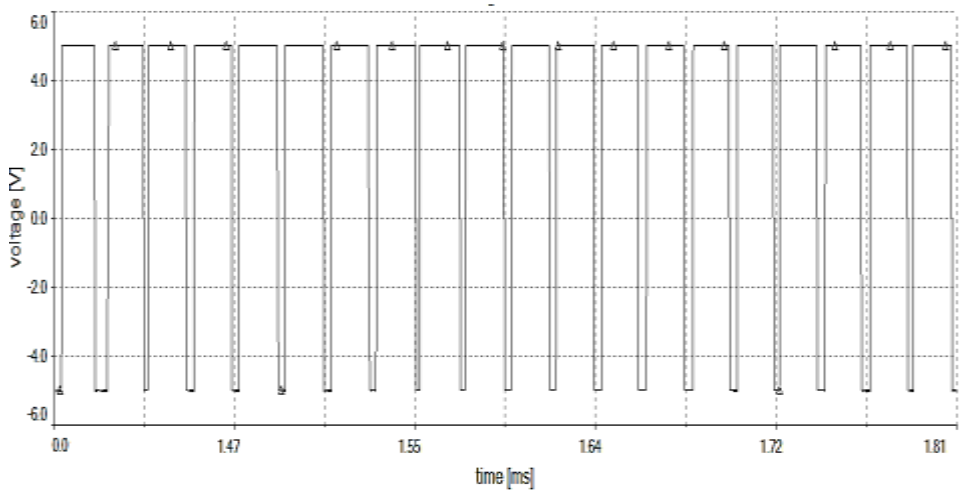


**Figure 5-14: Pulse width modulation output level**

### 5.7.2 PI controller DC level design

Currently, PI control is the most commonly used linear control application in industry. Linear PI controllers are designed for DC–DC converter topology; they utilize common frequency response techniques and are founded on the small signal model of the converter (Joseph et at., 2011). The PI control method offers numerous advantages over the PID control technique; these advantages include: robustness, good dynamic response, reduced steady-state error, load variation and simple implementation (Venkatanarayanan & Saravanan, 2014).

Optimising the stability of the SEPIC is effected by ensuring the correct operation and working conditions at any stage; PI control is a more feasible approach presenting to a better alternative for the control of a switching power converter.

The principal advantage of PI control schemes is that they are not susceptible to system parameter variations; such variations would lead to unpredictable dynamics (and static responses (Subramanian & Manimaran, 2015).

There are a number of ways of modelling the controller, such as: state space model, the K-method transfer function model, and Bode plot model. In the case of this study, a Bode plot model method was implemented to achieve the appropriate loop gain, the crossover frequency**,** and phase margin.

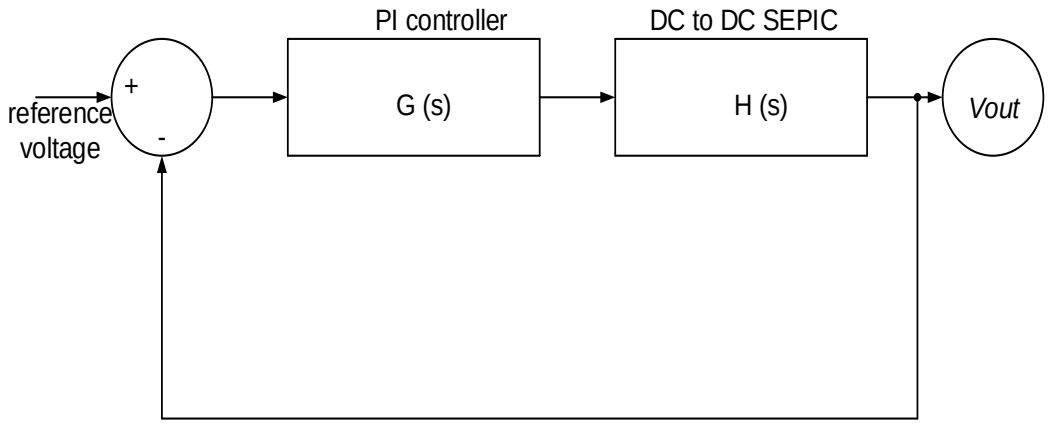


**Figure 5-15: Block diagram of the DC-DC SEPIC with PI controller**

Figure 5-15 above shows the Closed-loop of a DC–DC SEPIC with a PI controller. A large DC gain is implemented to minimise the steady-state errors when a P controller is used. Combining the proportional and integral functions will eliminate forced oscillations and steady-state errors. The integral term has a negative effect on the response speed and the overall stability of the system. SmartCtrl software, an add-on of the PSIM package, was used to simulate the PI controller and find a suitable solution. The main goal was to choose a nominal input voltage value, and to tune the controller by adjusting the loop transfer function to the ideal gain versus the desired frequency response (Figure 5-16).

To obtain satisfactory overshoot and stability margins, the bandwidth (crossover frequency) should be chosen between 10 and 20% of the switching frequency of the SEPIC, and the phase margin from $45^0$ to $60^0$. By running an AC-sweep analysis on a SEPIC using PSIM software, the loop gain, the phase of the converter (as illustrated in the Figure 5-17), and the loop transfer function file were exported to the smart-control platform.

Once a transfer function file has been exported, the implementation of a voltage mode controlled design can easily be performed. The procedure involves choosing single loop the sensor type, which in this study is a voltage divider together a PI controller. Table 5.1 and Table 5.2 show the resulting values of the input/output data for the selected PI controller; a schematic of the final PI controller arrived at is given in Figure 5-18.

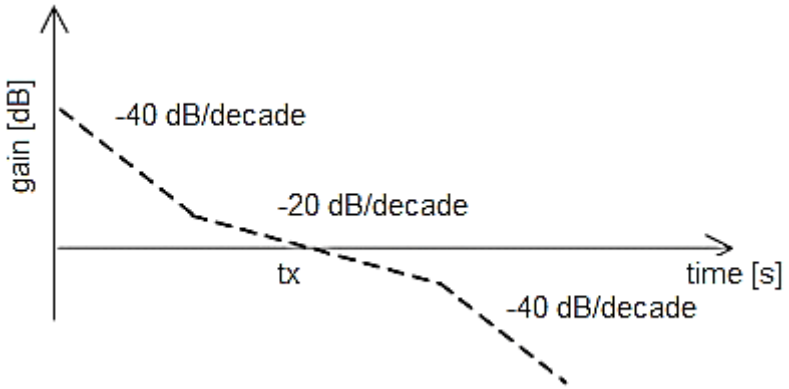


**Figure 5-16: Ideal gain versus frequency profile**

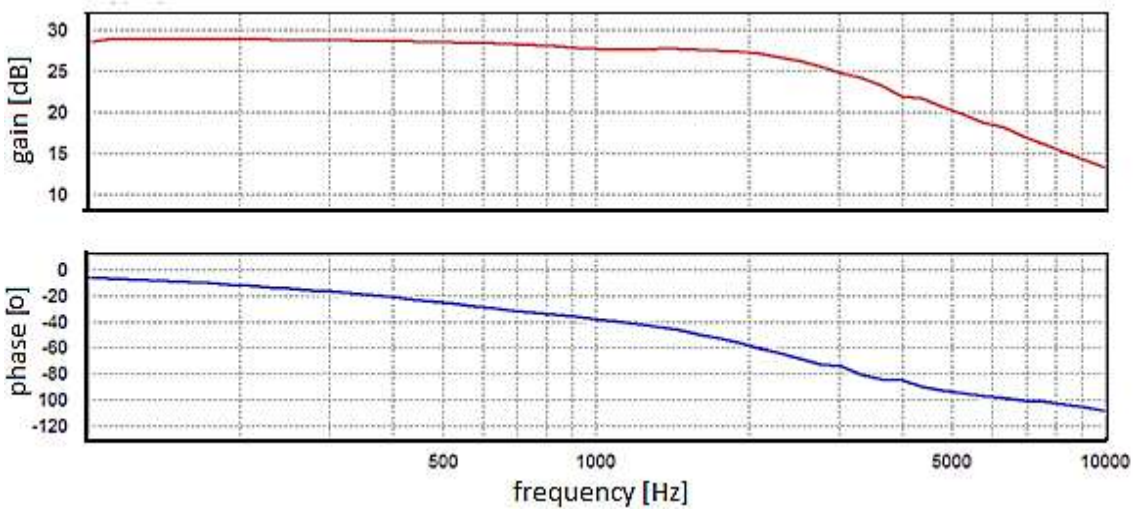


**Figure 5-17: Voltage control Bode plot, gain, and phase graph versus frequency profile**

**Table 5.1: Voltage controlled; PI controller results values of input data**

| Single-loop | | | Sensor | | | Regulator | |
|---|---|---|---|---|---|---|---|
| **Name** | **Values** | | **Name** | **Values** | | **Name** | **Values** |
| Frequency | 100 – 10 kHz | | Voltage divider | | | PI controller | |
| Cross frequency | 1.91646 kHz | | $V_{ref}$ / $V_o$ | 0.1 | | $G_{mod}$ | 0.4 |
| Phase margin (º) | 60 | | | | | $R_{11}$ [Ω] | 10000 |
| | | | | | | $V_p$ [V] | 3 |
| | | | | | | $T_r$ [s] | $3.2x10^{-6}$ |

**Table 5.2: Voltage controlled: PI controller results values of output data**

| Regulator (Analog) | | | Sensor | | | Loop performance parameters | |
|---|---|---|---|---|---|---|---|
| **Name** | **Values** | | **Name** | **Values** | | **Name** | **Values** |
| $K_p$ | 478.021 m | | $R_a$ [kΩ] | 4.5 | | PhF [Hz] | Out of F |
| $K_{int}$ | 41.4511 u | | $R_b$ [Ω] | 500 | | GM [dB] | … |
| $R_2$ [kΩ] | 4.7802 | | $P_a$ [mW] | 18 | | Atte [dB] | -26.41 |
| $C_2$ [nF] | 8.6714 | | $P_b$ [mW] | 2 | | | |
| $F_z$ [kHz] | 3.8396 | | | | | | |
| $F_i$ [kHz] | 1.8354 | | | | | | |
| $b_2$ [$s^2$] | 0 | | | | | | |
| $b_1$ [s] | $4.1451\times10^{-5}$ | | | | | | |
| $b_0$ | 1 | | | | | | |
| $a_3$ [$s^3$] | 0 | | | | | | |
| $a_2$ [$s^2$] | 0 | | | | | | |
| $a_1$ [s] | $8.6714\times10^{-5}$ | | | | | | |
| $a_0$ | 0 | | | | | | |

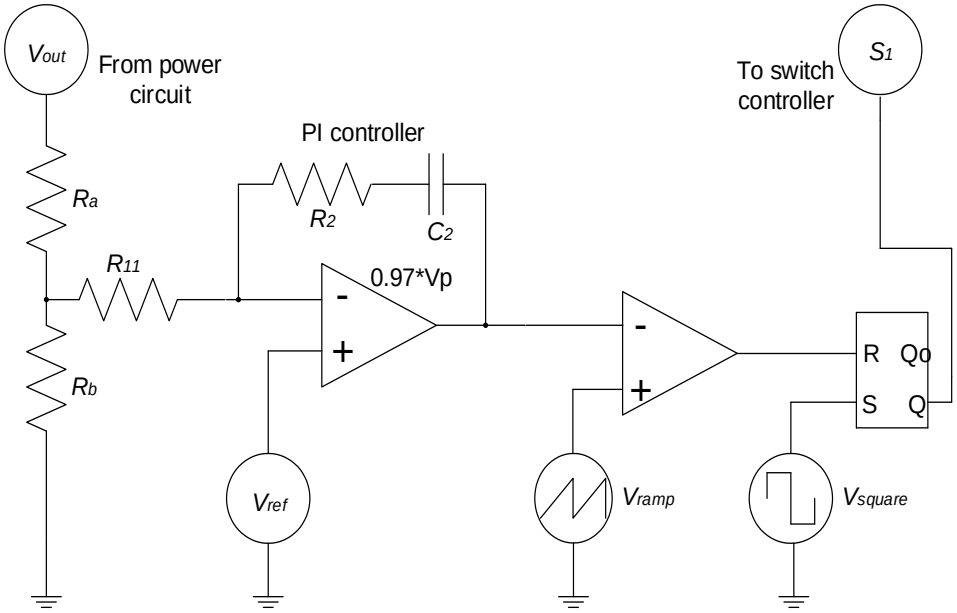


**Figure 5-18: Voltage controlled: PI controller schematic diagram**

## 5.8 SEPIC design

The single-ended primary inductance converter is designed to achieve the lower or the higher positive output voltage. The SEPIC illustrated in Figure 4-7 incorporates two inductors, which can be mounted on the same core; additionally, the same voltage is applied to each of the inductors throughout the switching cycle (Gu & Zhang, 2008). In terms of cost, using a coupled inductor requires less space on the printing circuit board (PCB), than the two independent inductors. Capacitor $C_1$ provides the isolation between the input, and output, providing protection by shorting the load. Figure 4-8 and Figure 4-9 illustrate the SEPIC current flow.

### 5.9 Design consideration

The Table 5.3 is the given data of proposed SEPIC.

**Table 5.3: SEPIC parameters data**

| Name | Values |
|---|---|
| Input voltage | 3 V – 20 V |
| Power | 8 W |
| Frequency | 250 kHz |
| Output voltage | 10 V |

- **Input / output currents**

  Assuming 100% efficiency:

$$I_{in\,(max)} = \frac{P_c}{V_{in\,(max)}} = 0.4\ \text{A} \tag{84}$$

$$I_{in\,(min)} = \frac{P_c}{V_{in\,(min)}} = 2.667\ \text{A} \tag{85}$$

$$I_{out} = \frac{P_c}{V_{out}} = 0.8\ \text{A} \tag{86}$$

  The SEPIC needs to be designed so that is capable of handling the maximum current flowing during the ‘on’ and ‘off’ states

- **Duty-cycle**

  Consider the SEPIC operating in the continuous conduction mode (CCM), the expression of the duty-cycle is then given by:

$$D = \frac{V_{out} + V_d}{V_{in} + V_{out} + V_d} \tag{87}$$

  $V_d$ is the forward voltage drop of the diode (0.0136 mV). The minimum and maximum duty-cycle are calculated below.

$$D_{max} = \frac{V_{out} + V_d}{V_{in\,(min)} + V_{out} + V_d} = 0.7694 \cong 77.0\% \tag{88}$$

$$D_{min} = \frac{V_{out} + V_d}{V_{in(max)} + V_{out} + V_d} = 0.3336 \cong 33\% \quad (89)$$

- **Inductor selection**

The best way of determining the inductance, is to allow the peak-to-peak ripple current to be approximately 40% of the maximum input current at the minimum input voltage. The current ripple is given by:

$$\Delta I_l = 40\% I_{in} = I_{out} \frac{V_{out}}{V_{in(min)}} 40\% = 1.06666 \text{ A} \quad (90)$$

And the inductor values are calculated from:

$$L_1 = L_2 = \frac{V_{in(min)}}{\Delta I_l f_{sw}} D_{max} = 8.6566 \text{ µH} \quad (91)$$

To avoid the inductor saturation, the peaks currents need to calculated.

$$I_{l1(peak)} = I_{out} \frac{V_{out} + V_d}{V_{in(min)}} \left(1 + \frac{0.4}{2}\right) = 3.2044 \text{ A} \quad (92)$$

$$I_{l2(peak)} = I_{out} \left(1 + \frac{0.4}{2}\right) = 0.96 \text{ A} \quad (93)$$

- **Coupling capacitor**

The coupling capacitor value of the SEPIC depends on the root-mean-square current, which is given by:

$$I_{C1(rms)} = I_{out} \times \sqrt{\frac{V_{out} + V_d}{V_{in(min)}}} = 1.4616 \text{ A} \quad (94)$$

Also the SEPIC has to be rated for a large root-mean-square current relative to the output power. This property makes the SEPIC better suited to lower power applications where the root-mean-square (RMS) current through the capacitor is relatively small.

Care has to be taken with the voltage rating of the coupling capacitor, which has to be greater than the maximum input voltage; the coupling capacitor, $C_1$ specified in this study was a 10 $\mu$F tantalum or ceramic.

- **Input capacitor (optional)**

  As a boost converter, the SEPIC has an inductor at the input. This inductor ensures that input capacitor is subjected to low amplitude ripple currents. The root-mean-square current in the input capacitor is given by:

$$I_{cin(rms)} = \frac{\Delta I_l}{\sqrt{12}} = 0.3079 \text{ A} \tag{95}$$

  Although the input capacitor is not so critical in a SEPIC application, the input capacitor should be capable of handling the root-mean-square current.

- **Output capacitor**

  When the switch in a SEPIC is turned ‘on’, the inductor is charges and the output current is supplied by the output capacitor. As a coupling capacitor, the output capacitor has to able to handle the maximum root-mean-square current.

$$I_{c1(rms)} = I_{C2(rms)} = 1.4616 \text{ A} \tag{96}$$

  It is assumed that half of the ripple is caused by the equivalent series resistance (ESR) and that other half is caused by the magnitude of capacitance. Hence:

$$ESR \leq \frac{V_{ripple} \times 0.5}{I_{l1(peak)} + I_{l2(peak)}} = 0.0240 \ \Omega \tag{98}$$

$$C_{out} \geq \frac{I_{out} \times D_{max}}{V_{ripple} \times 0.5 \times f_{sw}} = 24.6231 \ \mu\text{F} \tag{99}$$

  It is assumed that the peak-to-peak ripple voltage is 2% of the output voltage;

- **Output diode**

  The output diode has to be selected so that it can handle the peak current and the reverse voltage. In a SEPIC the diode peak current is equal to the switch peak current. The minimum peak reverse voltage that the diode must able to handle is:

$$V_{rd1} = V_{in(\max)} + V_{out(max)} = 30 \text{ V} \tag{97}$$

Like for the boost converter, the average diode current must be equal to the output current. The power dissipation within the diode is equal to the forward voltage drop of the diode, multiplied by the output current. Schottky diodes were recommended in order to minimize efficiency losses.

- **Power switch**

The peak current of the switch is:

$$I_{sw(peak)} = I_{l1(peak)} + I_{l2(peak)} = 4.1644 \text{ A} \quad (98)$$

And the RMS current is:

$$I_{sw(rms)} = I_{out} \times \sqrt{\frac{\left(V_{out} + V_{in\,(min)} + V_d\right) \times (V_{out} + V_d)}{{V_{in(min)}}^2}} = 3.0441 \text{ A} \quad (99)$$

$$P_{sw} = {I_{sw(rms)}}^2 \times R_{DS(on)} \times D_{max} + \left(V_{in(min)} + V_{out}\right) \times I_{sw(peak)} \times \frac{Q_{GD} \times f_{sw}}{I_G} \quad (100)$$

$$= 0.8127 \text{ W}$$

### 5.10 SEPIC simulation results

The proposed topology of the SEPIC was verified by analysing the simulation results from the open-loop and Closed-loop model. For the Closed-loop model, the PI controller parameters were calculated using the SmartCtrl add-on module of the PSIM package, and the Bode-plot technique.

#### 5.10.1 SEPIC open-loop model simulations

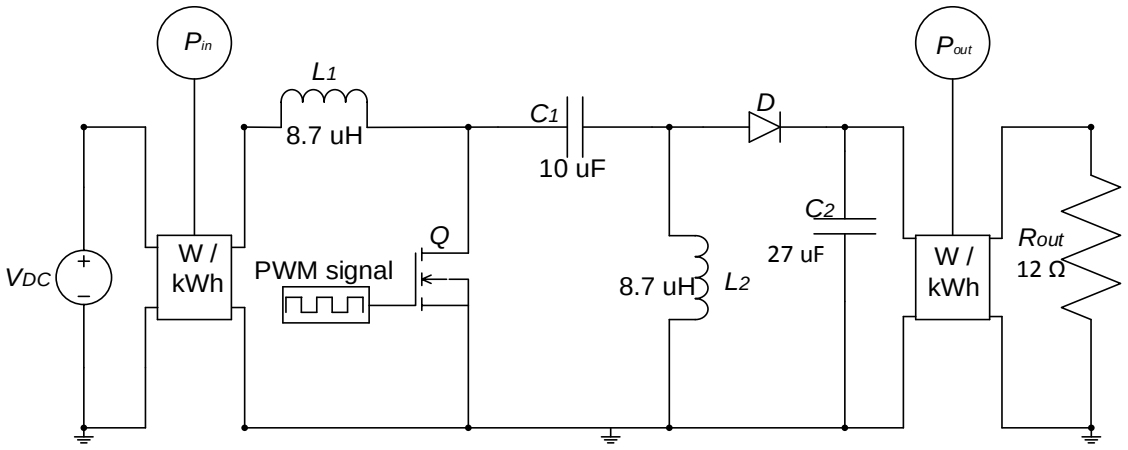


**Figure 5-19: PSIM model for the open-loop SEPIC circuit**

Figure 5-19 illustrates the proposed open-loop SEPIC circuit. Since an input voltage range of 3 V to 20 V is required, care has to be taken to limit the output voltage while running the open-loop simulation test. Figure 5-20 shows the graph of the output voltage when an input voltage of 3 V is applied, in this case, the SEPIC acts as a boost converter (step-up).

Additionally, for the input voltage of 3 V, the output current and the efficiency waveforms were computed. Figure 5-21 and Figure 5-22 respectively show the output current, and the efficiency achieved during the open-loop simulation.

When an input voltage of 20 V is applied, a SEPIC acts like a buck converter (step-down), and the desired maximum output voltage of 10 V is exceeded. With the input voltage of 20 V; the output current (Figure 5-23) and output voltage (Figure 5-25) increase due to the step change of the input voltage from 3 V to 20 V. In Figure 5-24, it can be seen that the SEPIC efficiency decreased to 86.5%, as compared to an efficiency of 96.8% for the case of an input voltage of 3 V, as illustrated in Figure 5-22. And accounted the overshoot at the settle time of 0.17 s to 0.24 s in this region with a designer of the open loop. Parasitic resistance of the inductors and MOSFET can cause the increased of voltage and current in the output.

To obtain a solution to the problem of an increasing output voltage, output current and decreasing efficiency, the PI controller was designed incorporating voltage mode control and peak current mode control (hysteresis), keeping the output voltage stable at 10 V maximum.

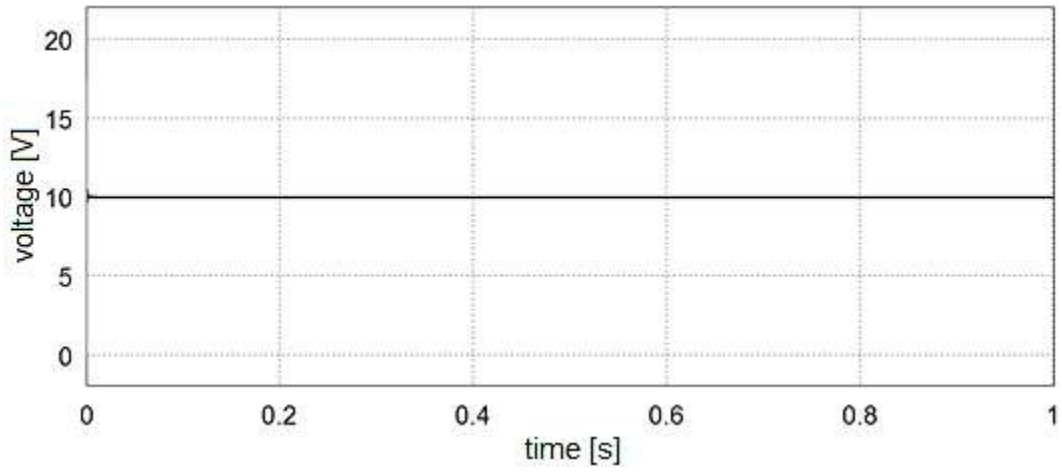


**Figure 5-20: Output voltage graph at 3 V input, maximum duty-cycle**

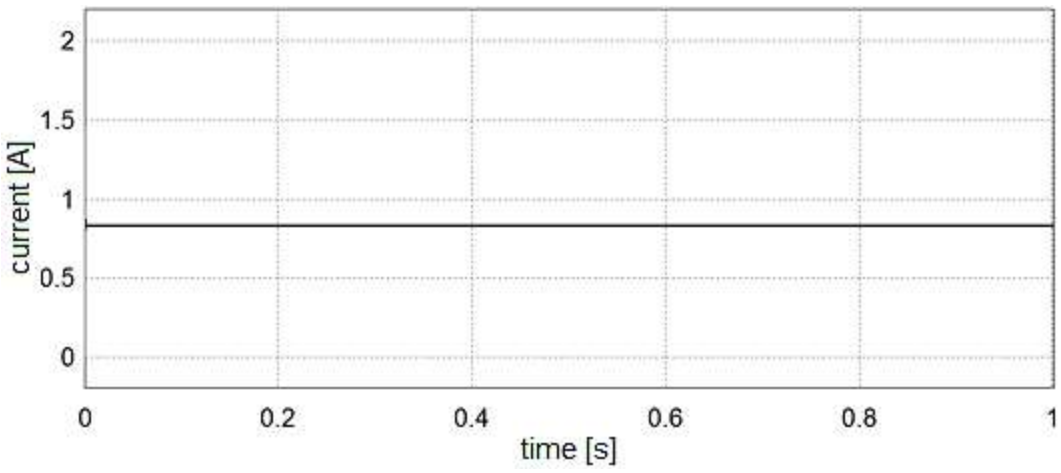


**Figure 5-21: Output current graph at 3 V input, maximum duty-cycle**

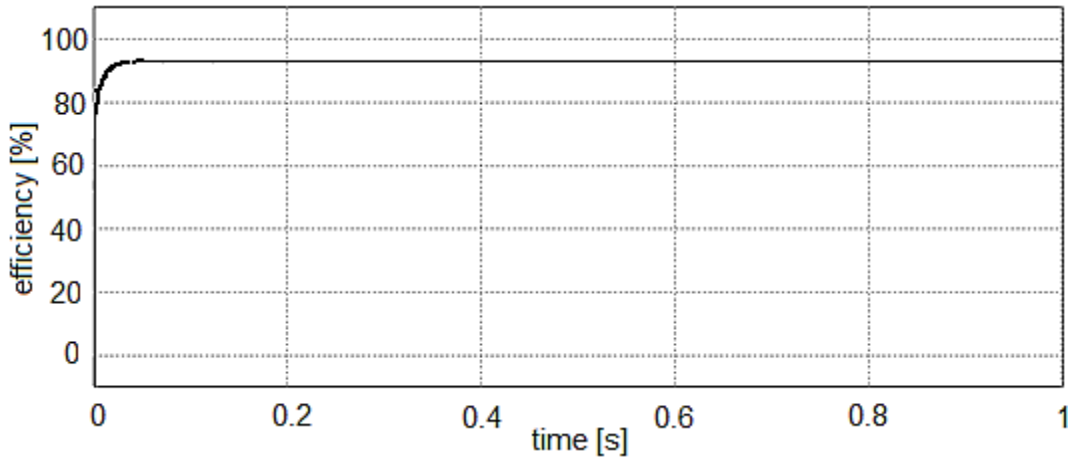


**Figure 5-22: Efficiency graph at 3 V input, maximum duty-cycle**

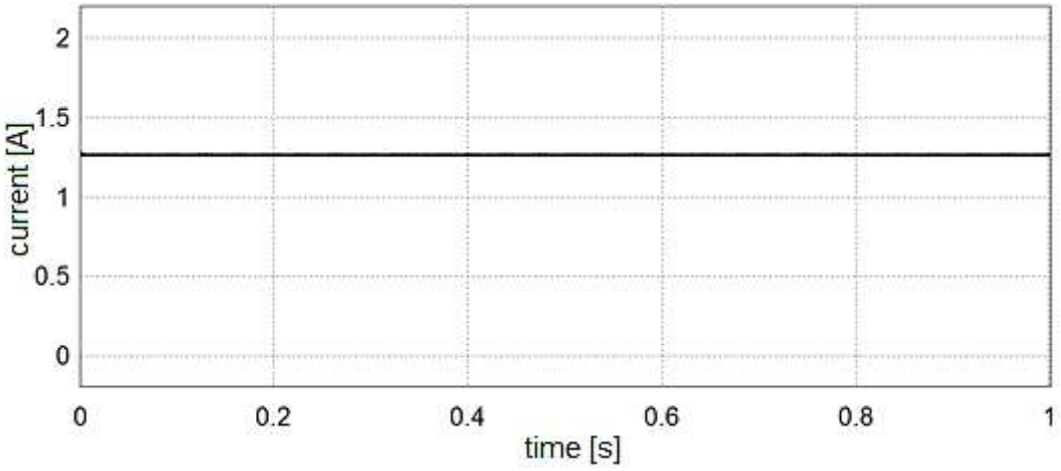


**Figure 5-23: Output current graph at 20 V input, minimum duty-cycle**

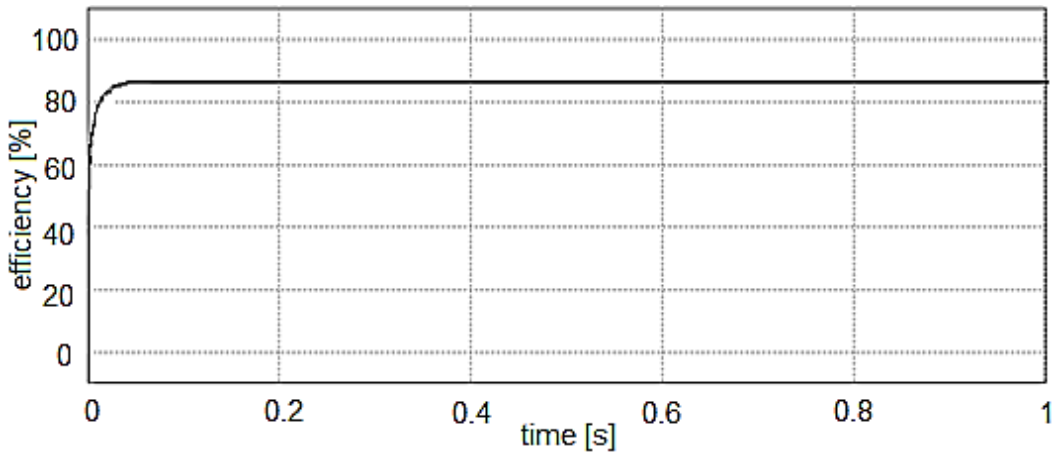


**Figure 5-24: Efficiency graph at 20 V input, minimum duty-cycle**

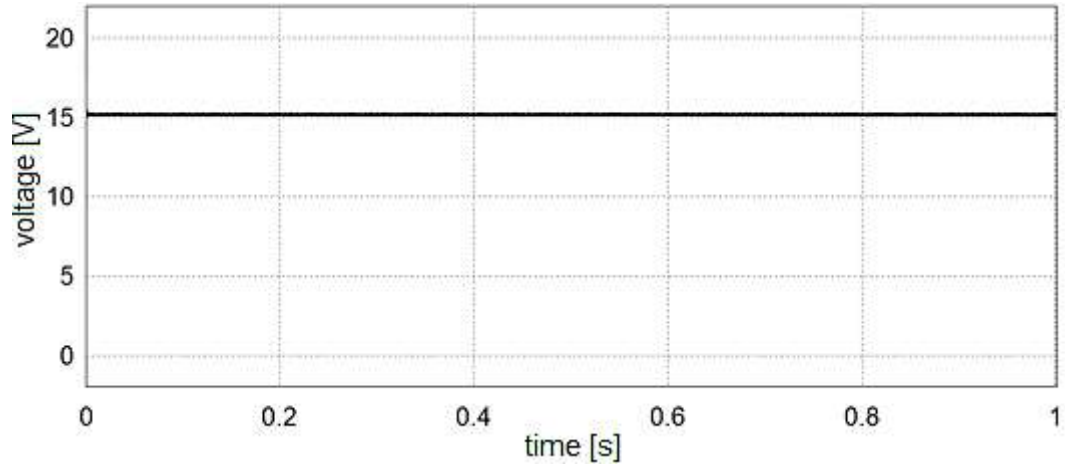


**Figure 5-25: Output voltage graph at 20 V input, maximum duty-cycle**

### 5.10.2 SEPIC voltage-mode controlled simulations (closed loop)

The Closed-loop model was implemented because it provides better transient and steady-state responses of the system. The PI controller is connected to the power circuit to form a complete Closed-loop system, using the voltage-mode control model. This is illustrated in Figure 5-26.

The nominal input voltage (11.5 V) was achieved by applying the average method to the input voltage range, which allowed the calculation and tuning of the nominal duty-cycle. Figure 5-27 shows the output voltage when the PI controller is connected; there insignificants undershoot and overshoot at the beginning of cycle (Figure 5-27, Figure 5-28). The efficiency (Figure 5-29) and the output current (Figure 5-28) are displayed for a comparison with the open-loop scenario at the maximum input voltage.

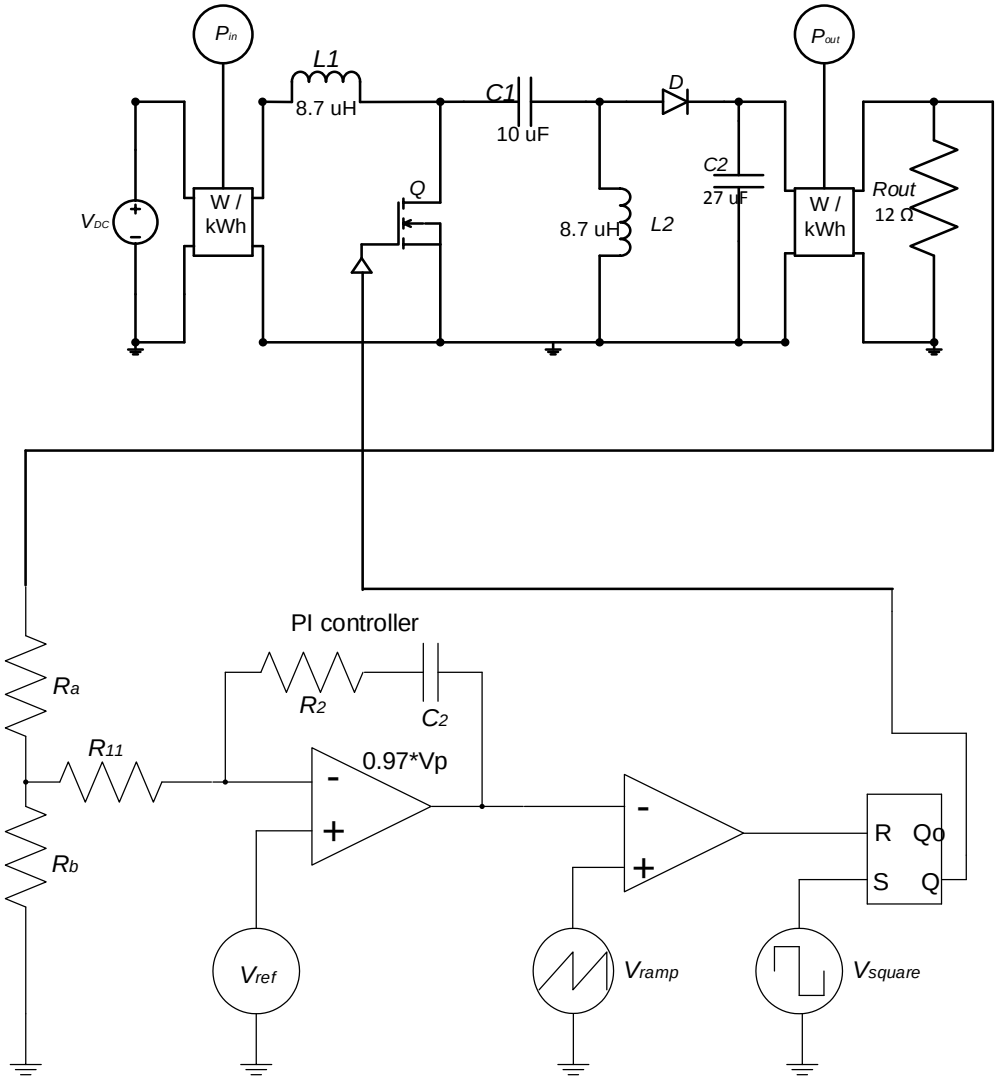


**Figure 5-26: PSIM model for the Closed-loop SEPIC circuit**

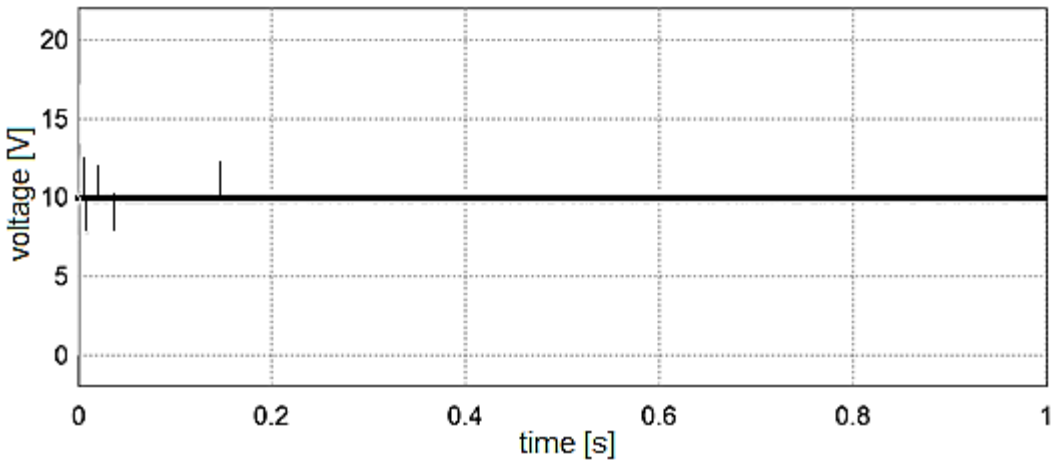


**Figure 5-27: Output voltage graph at 20 V input, nominal duty-cycle**

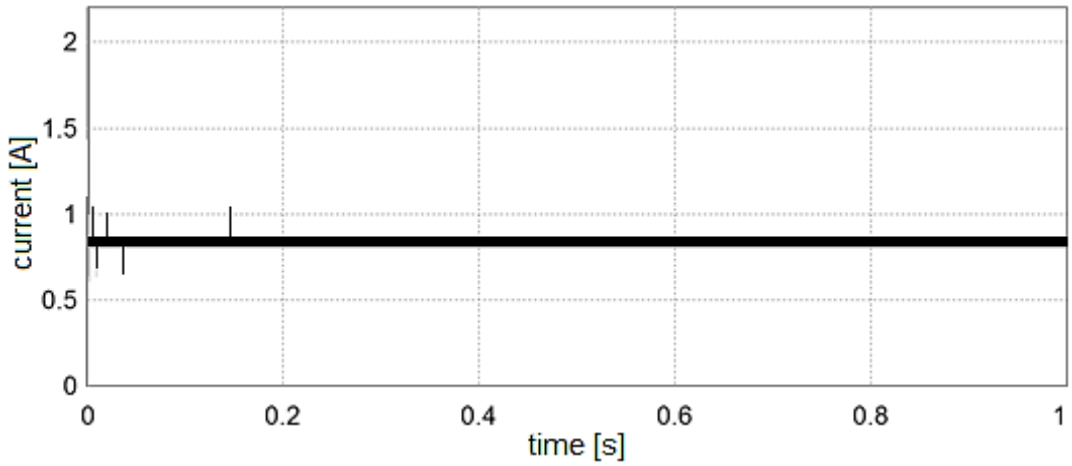


**Figure 5-28: Output current graph at 20 V input, nominal duty-cycle**

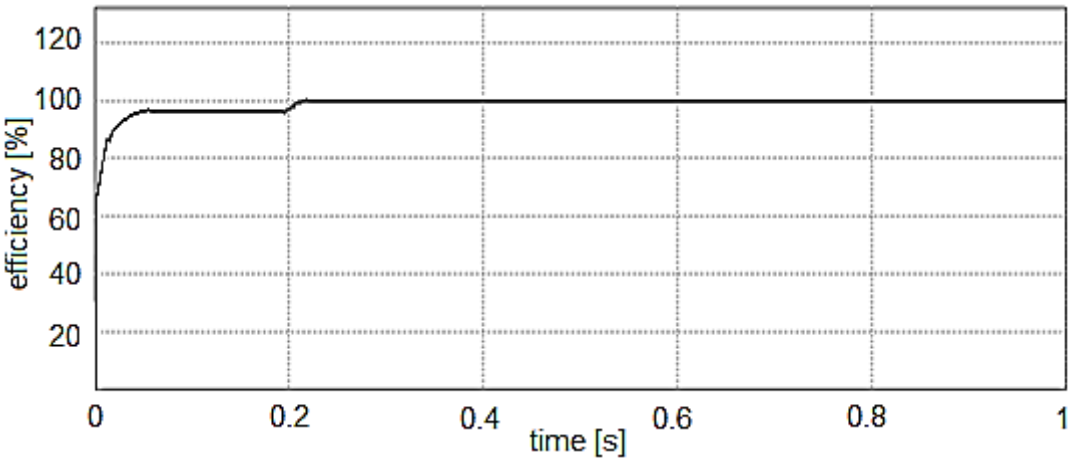


**Figure 5-29: Efficiency graph at 20 V input, nominal duty-cycle**

It can be seen from the output voltage, that the output current becomes stable at the desired values of the nominal input voltage. Moreover, Table 5.4 shows how robust and dynamic a SEPIC is, by its ability to keep the output voltage under the maximum allowed value of 10 V under load, over the full range input voltages from 3 V to 20 V.

Further simulations have been done; a controlled voltage which controlled a piecewise linear source, was applied to the input of the SEPIC. It can be seen that the output voltage has the maximum value of 10 V, however there is a neglible overshoot and a transient effect between 0.1 s to 0.3 s; this is illustrated in Figure 5-30.The Tables in Appendix A present the performance of the SEPIC using a voltage-mode controlled closed-loop, while decreasing and increasing the load resistance load resistance value; with a decreasing load value and the fixed input voltage (3 V or 20 V), the output power increase.

However, the output power decreases with an increasing load resistance value. Performing the load changes for voltage-mode control scheme, the scale of the output currents and output voltages in the Figures was increased by a factor of 30 for better reading of data; this was also done for the current-mode control, which is discussed later. In Figure 5-30 it is shown that the output voltage response has an overshoot of 30 V at time of 0.3 s, before going back to the desired steady-state value desired (10 V).

Depicted in Figure 5-31 below, is the output voltage response with a step change output current at an input voltage of 3 V; it shows that at the higher output current, the output voltage exhibits a uniform noise level from 0.05 – 0.2 s, 0.3 – 0.4 s, and 0.5 s to 0.6 s; thereafter it falls back to the desired steady-state value.

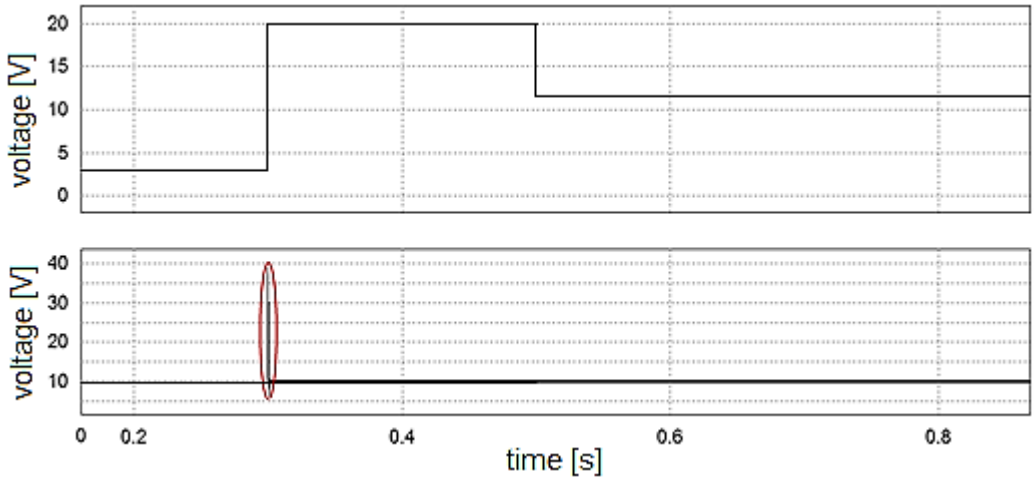


**Figure 5-30: Voltage-mode control, output voltage response with a step change input voltage**

At the nominal input voltage (Figure 5-32) and in the time interval 0.08 s to 0.2 s, the output voltage response of a voltage-mode control has a uniform noise level due to the high step change of the output current. In Figure 5-33, the output voltage response to a step change output current at the maximum input voltage (20 V) is depicted. It can be seen that in the interval of 0.1 s to 0.2 s, the output voltage produced an inform noise level at the maximum output current.

**Table 5.4: Data recorded for a SEPIC using voltage-mode controlled**

| Input data | | | Output data | | | Relations | |
|---|---|---|---|---|---|---|---|
| Voltage [V] | Current [A] | Power [W] | Voltage [V] | Current [A] | Power [W] | Efficiency [%] | Duty-cycle [%] |
| 3 | 2.205 | 8.177 | 9.759 | 0.815 | 7.884 | 96.368 | 76.51 |
| 5 | 0.997 | 8.559 | 10.035 | 0.838 | 8.189 | 95.677 | 66.77 |
| 7 | 0.292 | 8.401 | 10.027 | 0.838 | 8.178 | 97.346 | 58.92 |
| 9 | 0.128 | 8.534 | 10.019 | 0.837 | 8.180 | 95.852 | 52.71 |
| 11.5 | 0.217 | 8.348 | 10.015 | 0.837 | 8.180 | 97.988 | 46.58 |
| 13 | 0.226 | 8.367 | 10.021 | 0.837 | 8.181 | 97.777 | 43.56 |
| 16 | 0.236 | 8.378 | 10.016 | 0.837 | 8.354 | 99.713 | 38.53 |
| 19 | 0.225 | 8.315 | 10.011 | 0.836 | 8.182 | 98.401 | 34.54 |
| 20 | 0.216 | 8.279 | 10.011 | 0.836 | 8.183 | 98.840 | 33.39 |

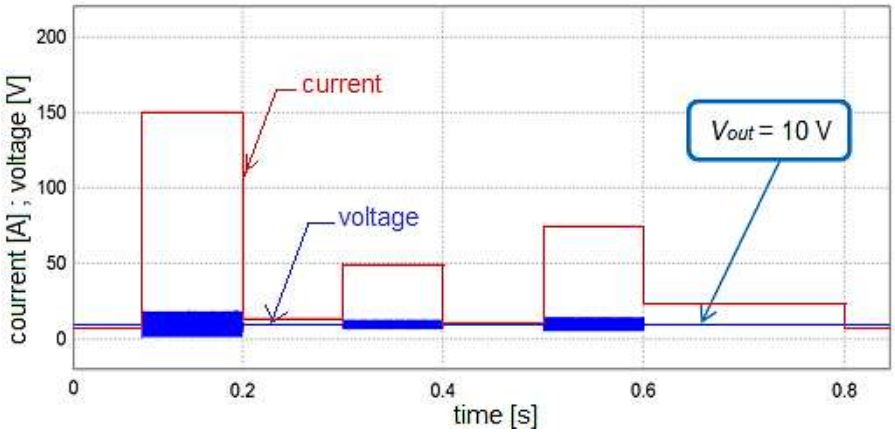


**Figure 5-31: Voltage-mode control, output voltage response and step change output current with an input voltage of 3 V**

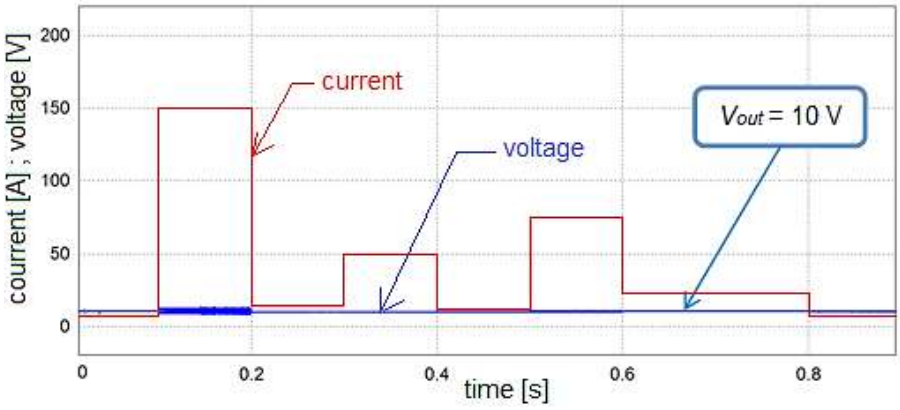


**Figure 5-32: Voltage-mode control, output voltage response and step change output current with an 11.5 V nominal input voltage**

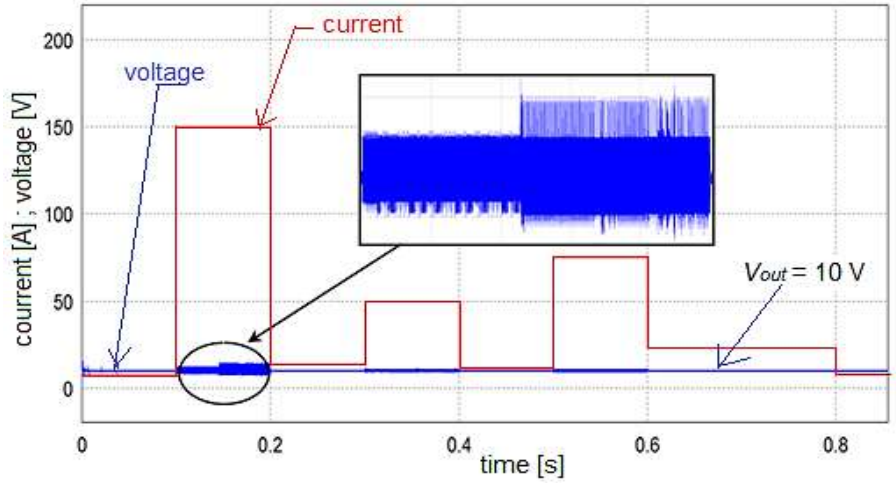


**Figure 5-33: Voltage mode control, output voltage response and step change output current with a 20 V input voltage**

### 5.10.3 SEPIC current mode controlled simulations (closed-loop)

A circuit diagram of a current-mode controlled SEPIC topology is shown in Figure 4-15. The implementation current controlled topology of this type from other DC–DC topologies such as: buck, boost, and buck-boost. Because this topology uses two inductors, the peak current control signal (reference current) is chosen as the sum of the inductor currents, hence:

$$I = I_{L1} + I_{L2} \tag{101}$$

With of a duty-cycle greater 0.5, slope compensation is taken into consideration to provide a better response to the output voltage of the SEPIC. An AC-sweep was performed to obtain the loop transfer function of the system, which results in the voltage gain and the phase angle

plot shown in Figure 5-34. The same step-by-step procedure as mentioned in Chapter 4, was applied to design the PI controller, using the PSIM add-on module, SmartCtrl.

To determine a suitable reference voltage and control current, an appropriate output voltage sensor must be selected. For this study, a voltage divider was embedded in the regulator and an unattenuated PI regulator was selected. Figure 5-35 shows the complete circuit diagram of a SEPIC with the current-mode controller connected. The components of the PI control circuit are calculated automatically by the simulation software (Table 5.5).

Several test simulations were done to evaluate the performance of the proposed SEPIC combined with peak current-mode controller. These simulations included: assessment of the output voltage using an input voltage of 3 V (Figure 5-36) and 20 V (Figure 5-37), as well as the using an input voltage control with a piecewise linear source, and a piecewise triangle source.

For current-mode control, the output voltage resulting when there is a step-change in the input voltage is illustrated in Figure 5.38. It can be seen that the output voltage was obtained throughout the step change, there is however, a 0.1V overshoot at 0.3 seconds. There is a disturbance of the steady-state, and an overshoot which can be neglected. The recording data of the SEPIC using peak current-mode control is shown in the Table 5.6. With an input voltage of 16 V the converter performed at 100% efficiency.

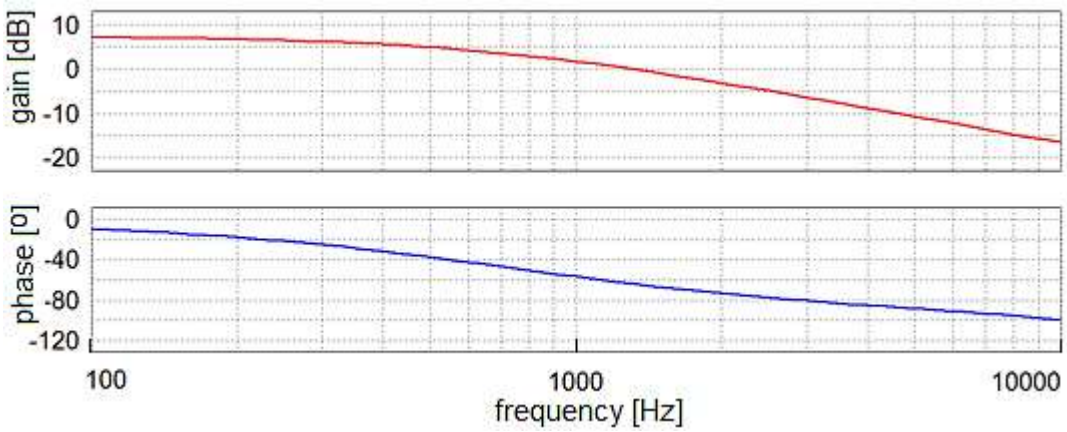


**Figure 5-34: Current mode control Bode plot, gain and phase graph versus frequency**

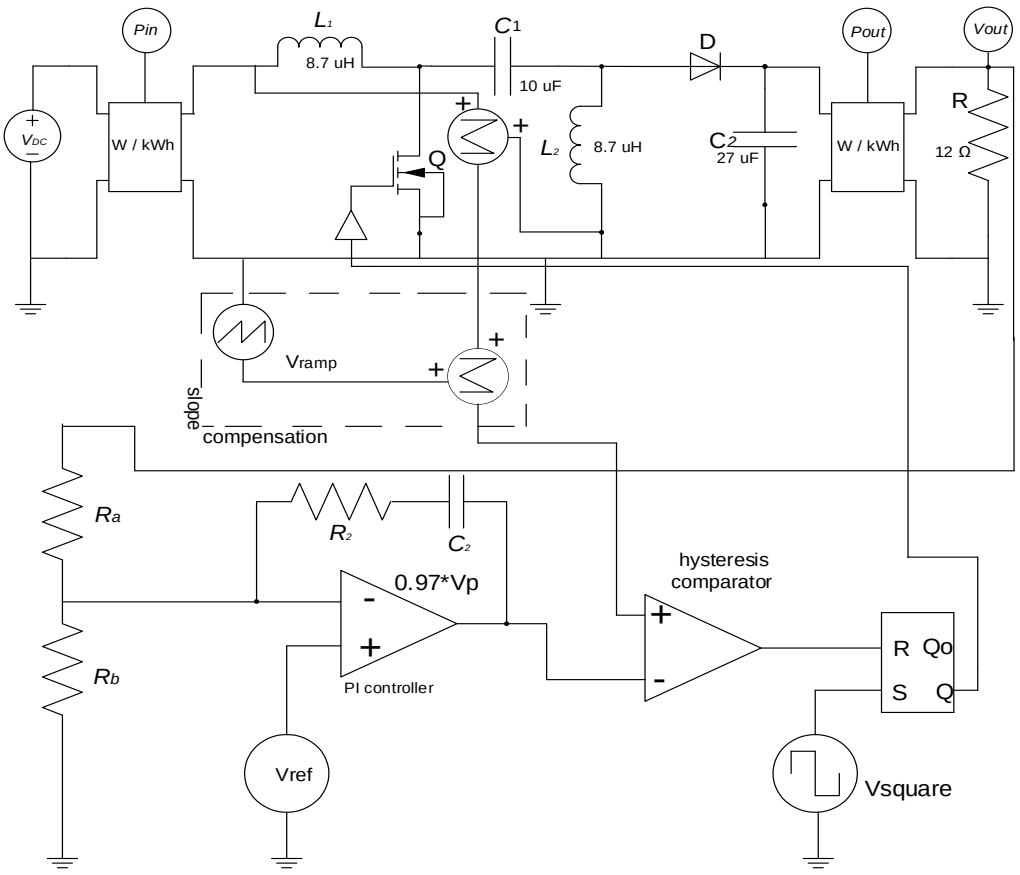


**Figure 5-35: Closed-loop SEPIC with a peak current-mode control**

**Table 5.5: PI control components values**

| **Critical components values** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **voltages [V]** | | **Resistance [kΩ]** | | **capacitor [pF]** | | **frequency [kHz] / Ramp** | |
| $V_p$ | 3 | $R_2$ | 227.952 | $C_2$ | 365.8 | $F_{sw}$ | 250 |
| $V_v$ | 1 | $R_{11}$ | 10 | | | $D_{ramp}$ | 0.8 |
| $V_{pp}$ | 2 | $R_{ar}$ | 10 | | | | |
| $V_{ref}$ | 5 | | | | | | |

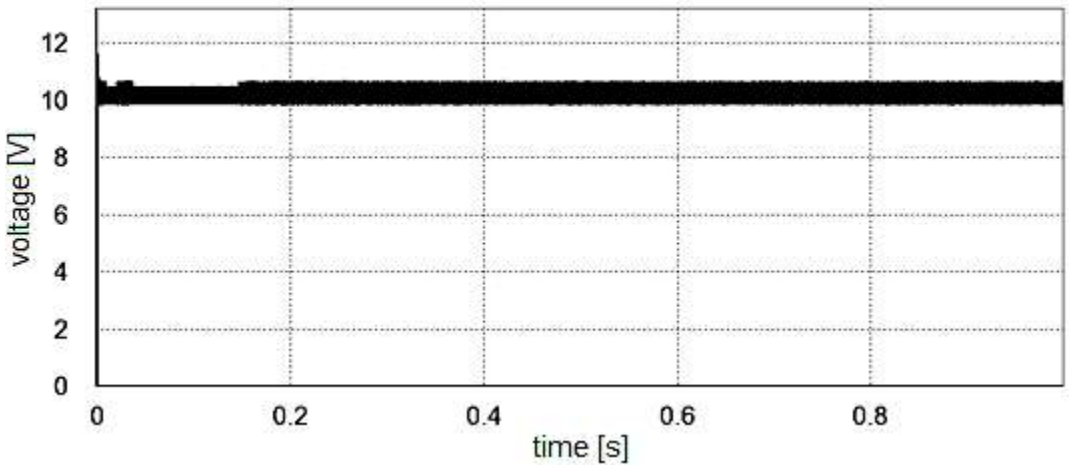


**Figure 5-36: Output voltage of the SEPIC using peak current-mode control at an input voltage of 20 V**

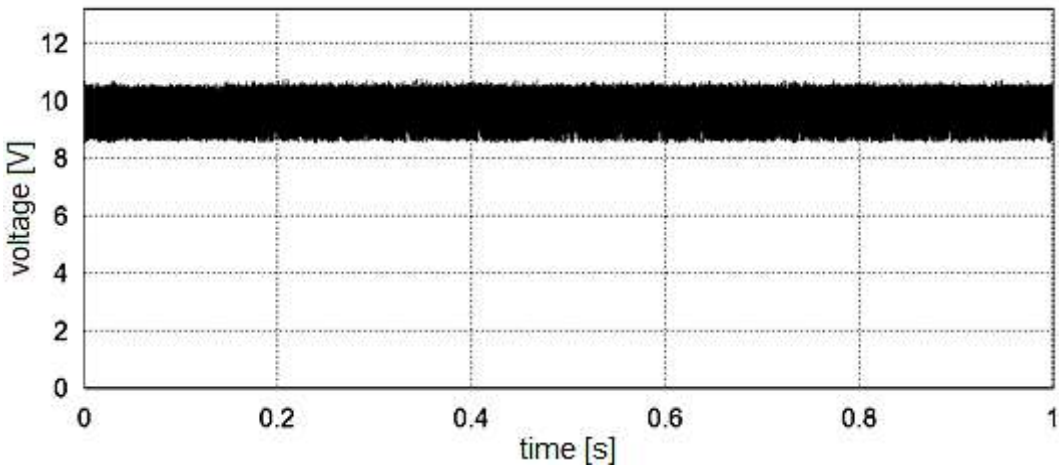


**Figure 5-37: Output voltage of the SEPIC using peak current-mode control at an input voltage 3 V**

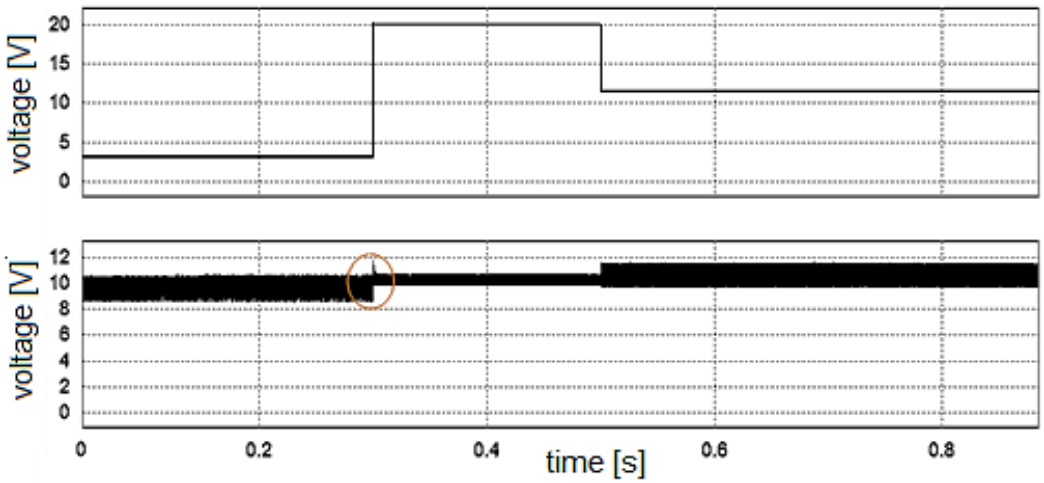


**Figure 5-38: Current-mode control: output voltage response with a step change in the input voltage**

In Figure 5-39 below it is shown that when the load resistor decreases, the output current increases; this results in the current-mode control stabilizing the output voltage at the desired value (10 V). As depicted in, this phenomenon occurred during time intervals 0.05 – 0.2 s, 0.3 – 0.4 s, and 0.5 – 0.6 s.

The controller has been designed using a nominal voltage value; Figure 5-40 below shows the stability of the output voltage (10 V) over a load current step change, when using a fixed nominal input voltage. At the maximum input voltage (20 V), the output voltage produced the an inform noise level when the output load current was increased to 150 A over the interval 0.05 s to 0.2 s; however the average output voltage value remained at 10 V, as depicted in Figure 5-41.

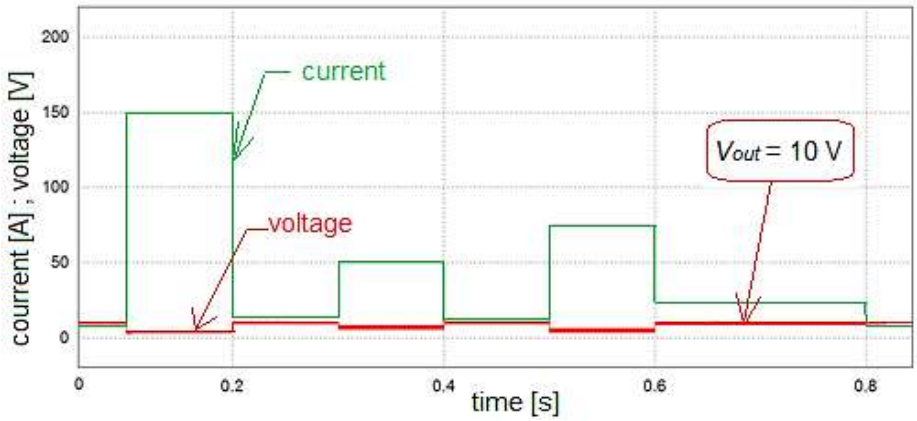


**Figure 5-39: Current-mode control: output voltage response and step change output current with an input voltage of 3 V**

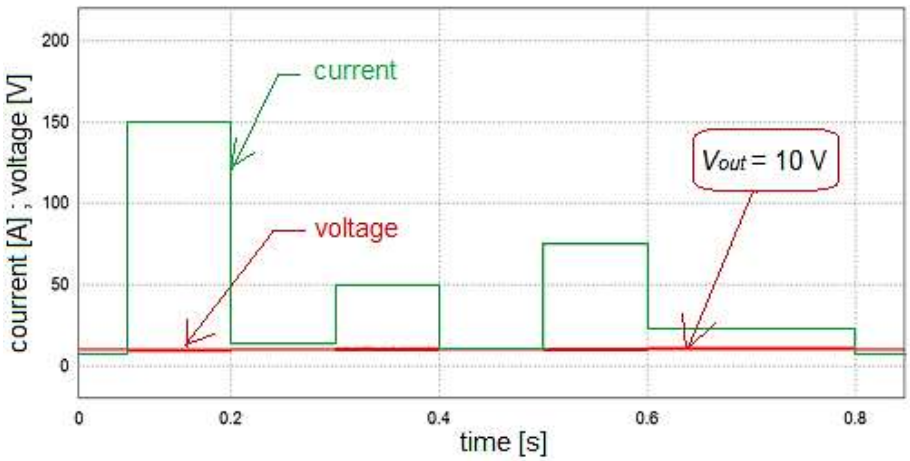


**Figure 5-40: Current-mode control: output voltage response and step change output current with an input voltage 11.5 V**

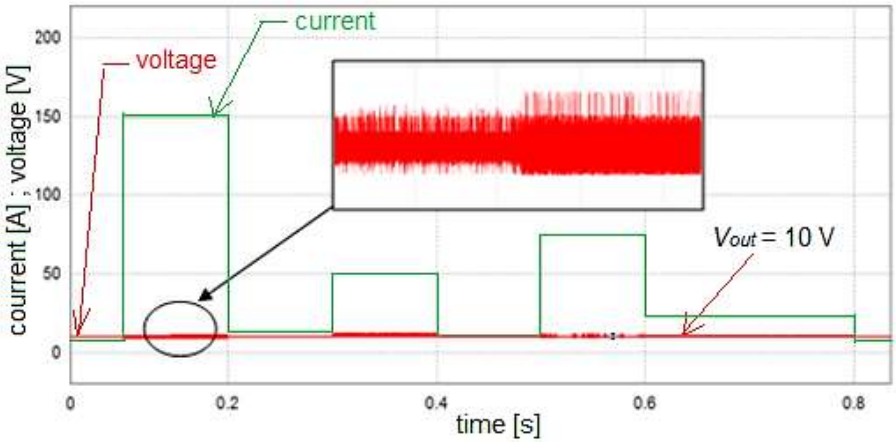


**Figure 5-41: Current-mode control: output voltage response and step change output current with an input voltage of 20 V**

**Table 5.6: Data recorded for a SEPIC using current-mode controlled.**

| Input data | | | Output data | | | Relations | |
|---|---|---|---|---|---|---|---|
| Voltage [V] | Current [A] | Power [W] | Voltage [V] | Current [A] | Power [W] | Efficiency [%] | Duty-cycle [%] |
| 3 | 2.707 | 7.951 | 9.705 | 0.809 | 7.708 | 96.943 | 76.387 |
| 5 | 1.723 | 8.449 | 9.921 | 0.827 | 8.051 | 95.289 | 66.490 |
| 7 | 1.315 | 9.014 | 10.017 | 0.848 | 8.448 | 93.720 | 58.865 |
| 9 | 0.998 | 8.796 | 10.285 | 0.858 | 8.644 | 98.272 | 53.331 |
| 11.5 | 0.816 | 9.184 | 10.481 | 0.873 | 8.986 | 97.844 | 47.682 |
| 13 | 0.707 | 9.198 | 10.298 | 0.859 | 8.858 | 96.304 | 44.201 |
| 16 | 0.566 | 8.417 | 10.151 | 0.847 | 8.417 | 100.00 | 38.817 |
| 19 | 0.477 | 8.867 | 10.219 | 0.852 | 8.530 | 96.199 | 34.974 |
| 20 | 0.453 | 8.867 | 10.184 | 0.849 | 8.470 | 95.523 | 33.739 |

## 5.11 Summary

In this chapter the design and simulation of a front-end DC–DC power converter for a nanosatellite, was carried out. Additionally, an analogue PWM signal was investigated. The different control techniques of DC–DC power converter namely, voltage- and current-mode control, were investigated.

# Chapter 6 : TEST RESULTS AND VALIDATIONS

## 6.1 Overview

The following chapter discusses the various test results obtain in order to validate the functioning of the front-end DC–DC power converter (SEPIC) for space application. Preliminary results involved the validation of analog pulse width modulation, which comprised: validating the output voltage using different input voltages, a load changing test which was done to verify the robustness of the front-end DC–DC power converter, and establishing the efficiency of the system by applying a control loop in the system. Voltage-mode control and current-mode control were used to stabilize the output voltage at the required values.

Once the results of the abovementioned tests were, an integrated network test was done. Among the testing equipment used were: a digital multi-meter, a DSO-X 2002A oscilloscope, two N2863B low-cost passive probes with attenuation 10:1 and an impedance of 10 MΩ, and a bread-board project which was tested to avoid short circuits and malfunctions of the system. Tests were conducted independently on each stage and the results were compared to an expected outcome. For this, each stage was constructed on a bread-board as a stand-alone assembly and tested when subjected to expected simulated inputs.

## 6.2 Analog PWM validation test

Analog pulse width modulation (see Figure 6-1) was validated using different stages namely: the relaxation oscillator stage, which creates the system frequency and produces the square wave signal as its output — this is depicted in Figure 6-2 and it was measured at node A, indicated in Figure 6-1 ; the sawtooth generator stage, which is used to convert the square wave from oscillator output and produce a triangular signal — this is illustrated in Figure 6-3 and was measured at node B as shown Figure 6-1 ; and finally the inverting stage, was introduced to obtain the positive sawtooth required to overlap with a DC level control signal — see Figure 6-4, which was measured at node C in Figure 6-1, and Figure 6-5 which was measured at nodes C and B in Figure 6-1. The sawtooth waveform is need to produce the required duty-cycle — this is shown in Figure 6-6 and was measured at node D in Figure 6-1. The 33.51% minimum duty cycle (see Figure 6-7 as measured at node E in Figure 6-1), and 77.38% maximum duty-cycle( see Figure 6-8 as measured at node E in Figure 6-1) were achieved to ensure better functioning of the MOSFET switch of the DC–DC power converter.

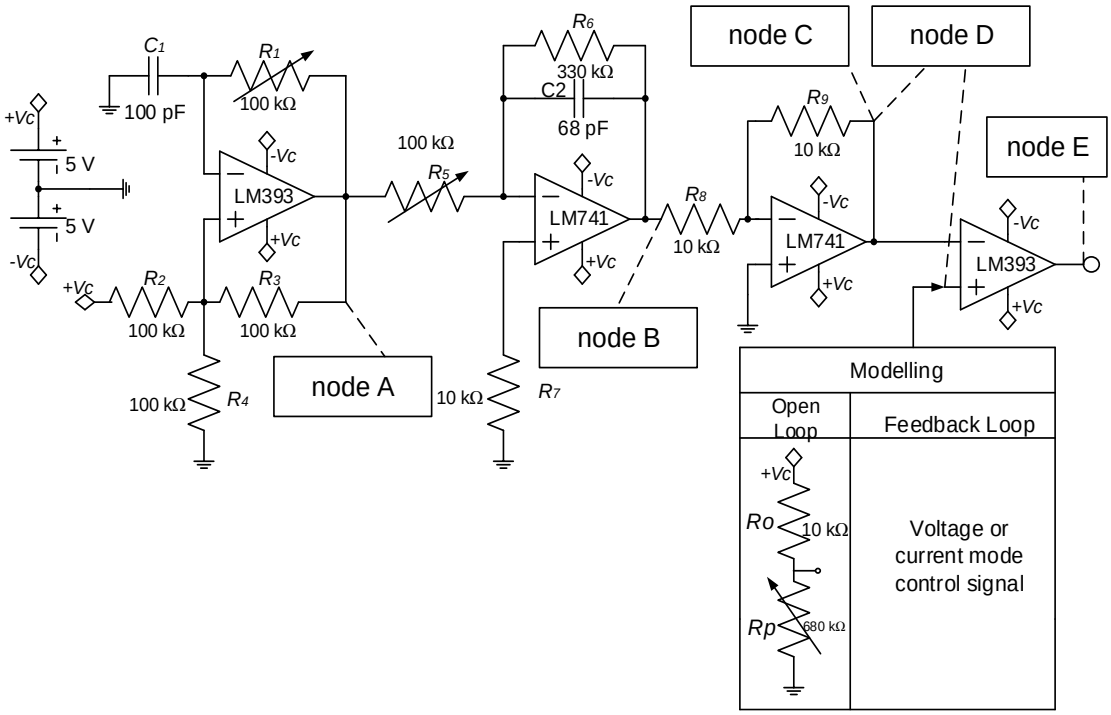


**Figure 6-1: Analogue PWM circuit**

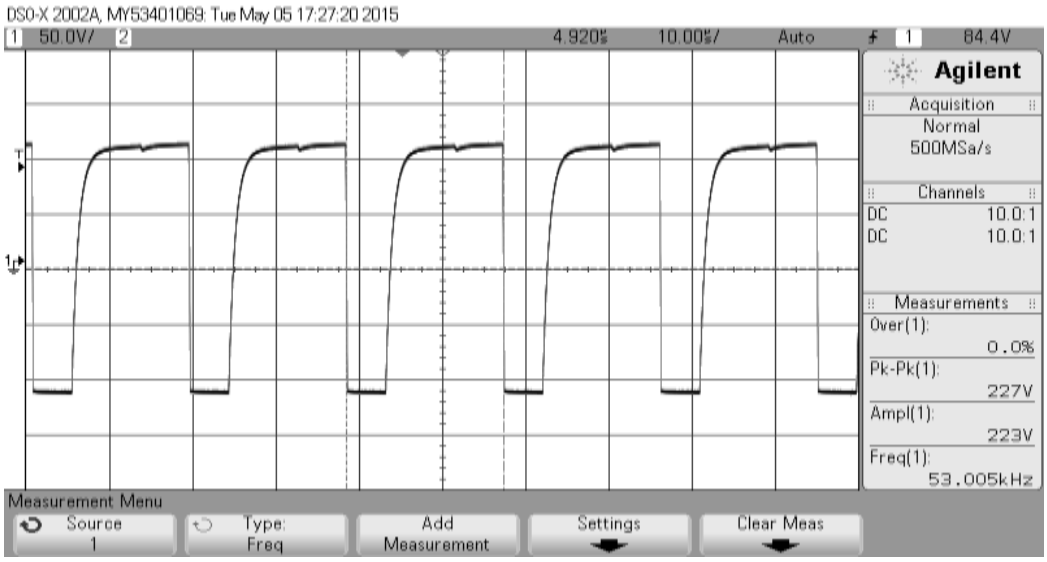


**Figure 6-2 : Relaxation oscillator test validation as measured at node A in Figure 6-1**

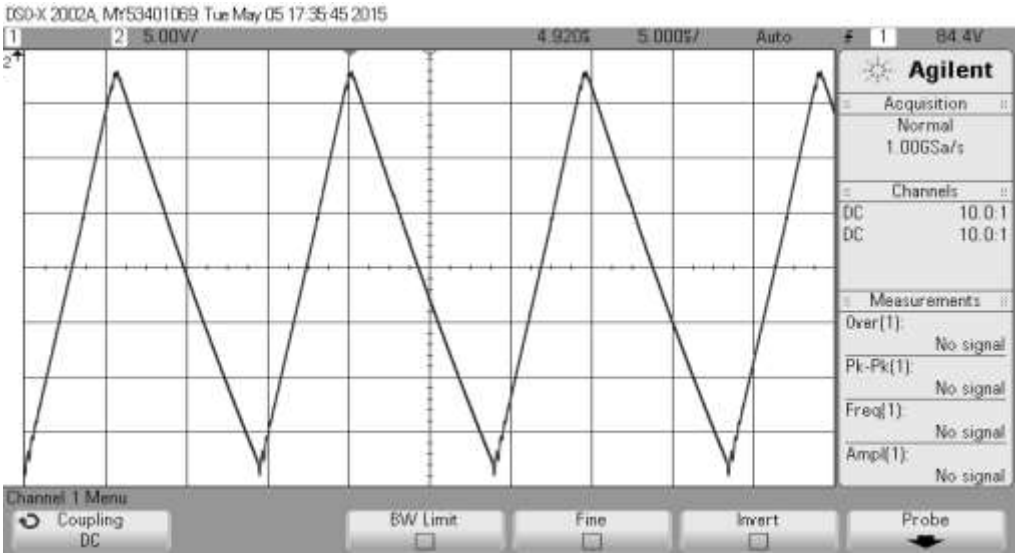


**Figure 6-3: Sawtooth generator test validation as measured at node B in Figure 6-1**

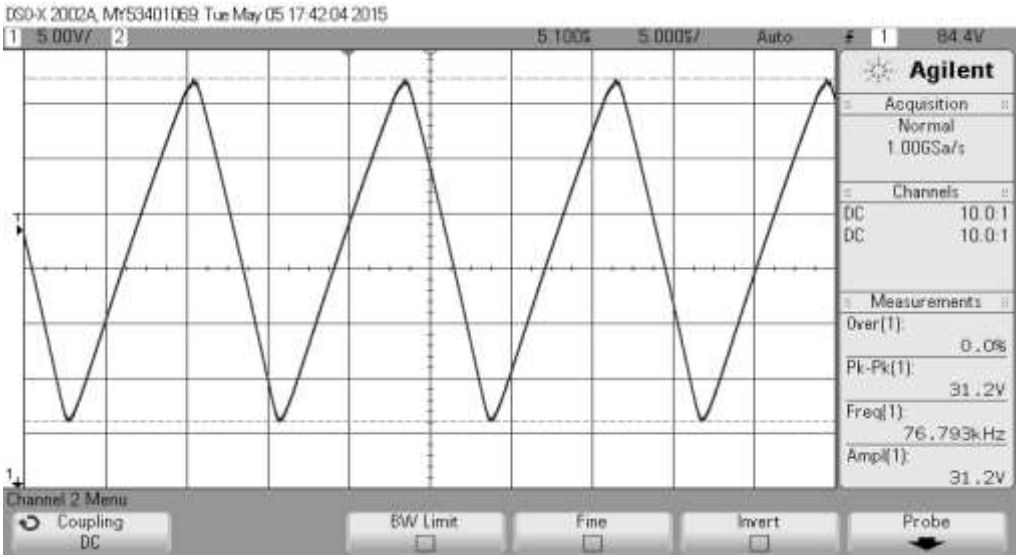


**Figure 6-4: Inverting sawtooth test validation as measured at node C in Figure 6-1**

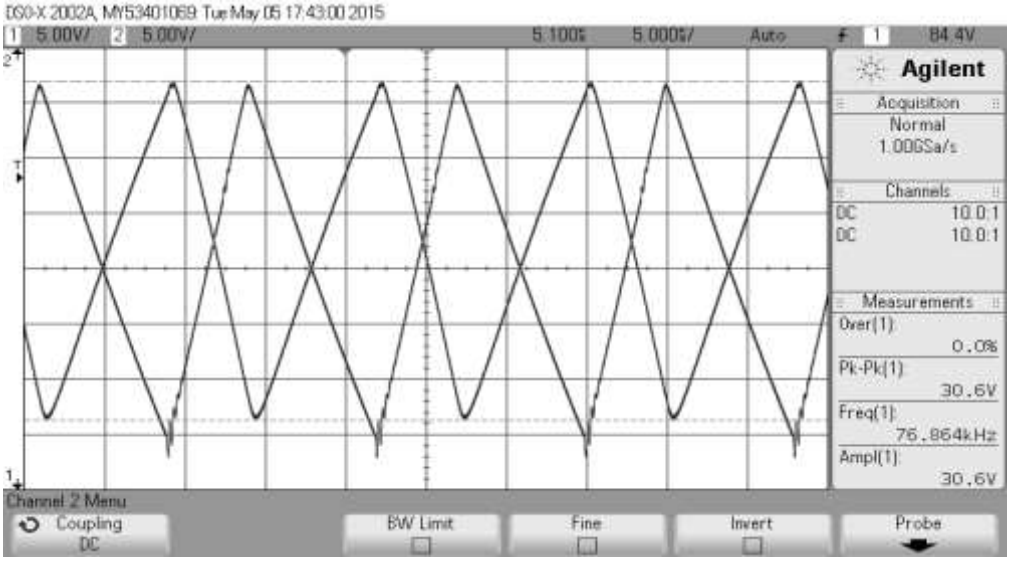


**Figure 6-5: Original sawtooth generator versus inverting sawtooth generator test validation as measured at node B and C in Figure 6-1**

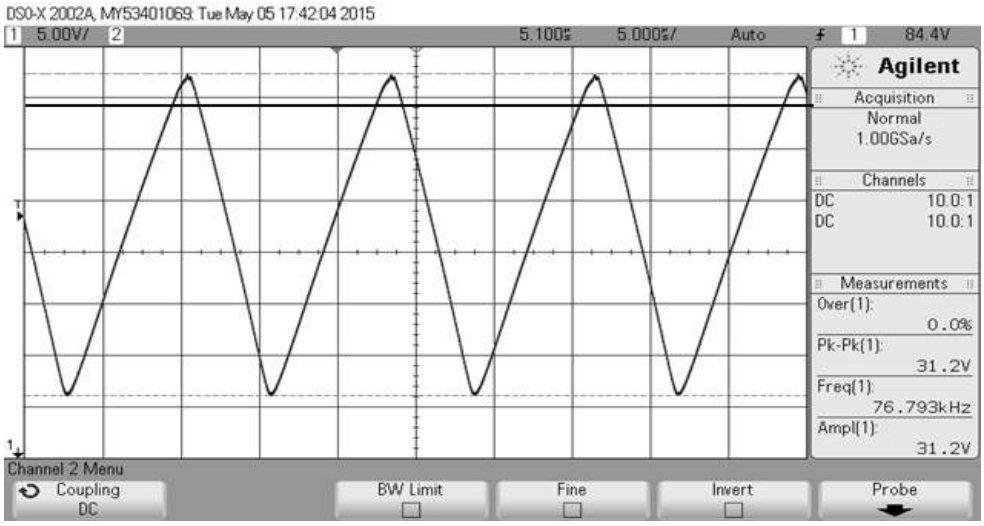


**Figure 6-6: DC level control signal and inverting sawtooth signal test validation as measured at node D in Figure 6-1**

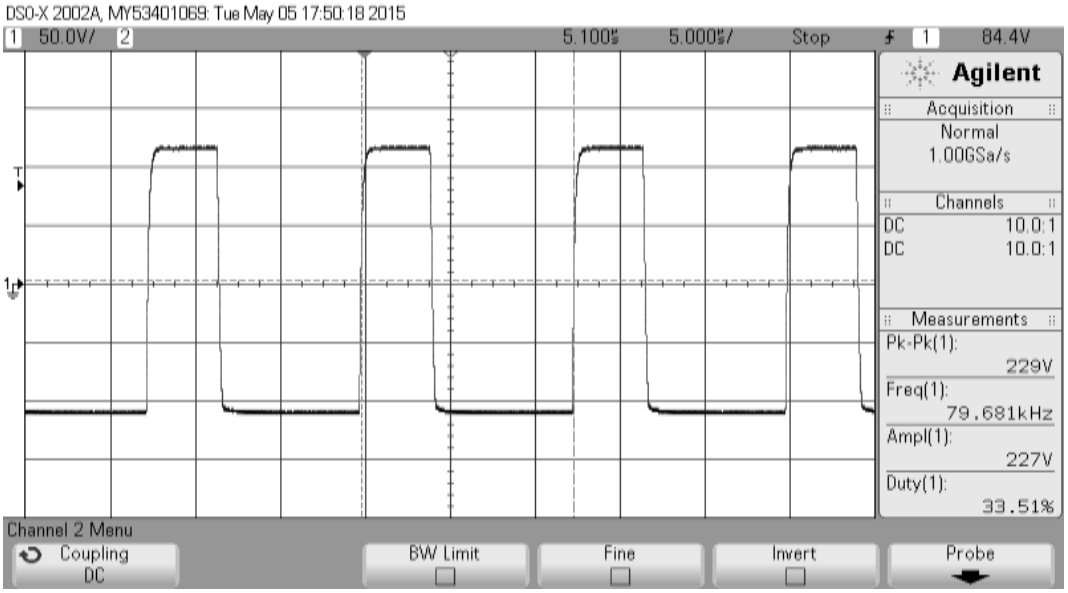


**Figure 6-7: Minimum duty-cycle test validation as measured at node E in Figure 6-1**

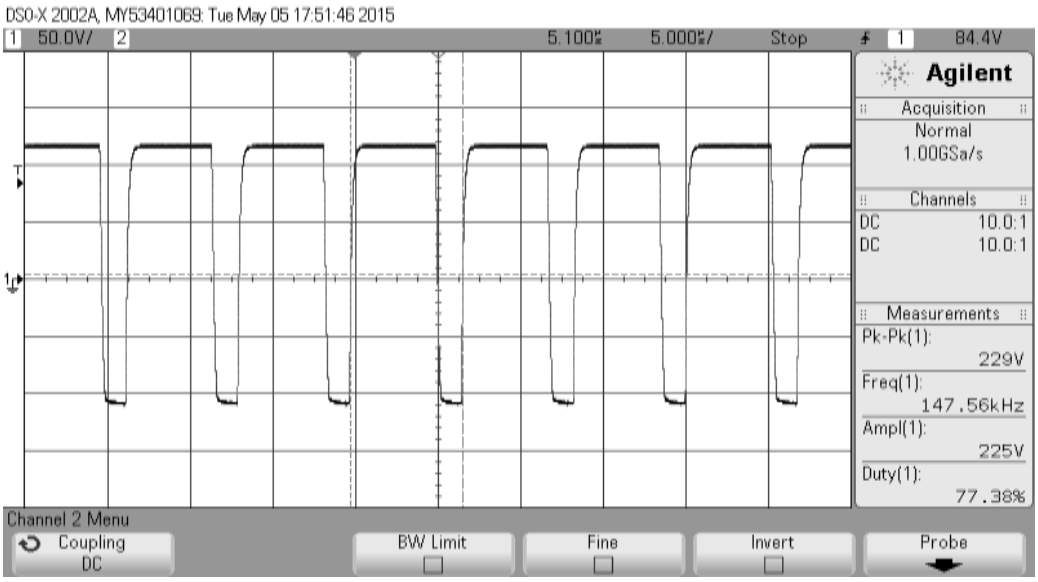


**Figure 6-8: Maximum duty-cycle test validation as measured at node E in Figure 6-1**

### 6.3 Power circuit validation

An analog PWM signal was connected to the switch of the power circuit, after which several tests were done to confirm the dynamic response of the front-end DC–DC power converter. After analysing the experimental results obtained from the front-end converter, three different control techniques were applied. Readings of the parameters listed in Chapter 5, were taken from the DC–DC power converter circuit under the following conditions:

- Open loop controller (without a feedback)
- Closed-loop controller (with a feedback, voltage control and current control)

#### 6.3.1 Open loop power circuit validation

The expected results from the proposed DC–DC power converter were experimentally verified using the open loop model and Closed-loop models. The resulting experimental open loop output voltage of 9.92 V from the DC–DC power converter when applying a 3 V input voltage and at the maximum duty-cycle can be seen in Figure 6-9; this output voltage was in accordance with the design requirements stipulated in Chapter 5. Undershoot and overshoot happened over a short period of time before a steady-state value was reached.


**Figure 6-9: Output voltage: open-loop condition test validation with an input voltage of 3 V**

### 6.3.2 Closed-loop power circuit validation

To better assess the functionality of the DC–DC power converter, the Closed-loop experiment was done using the two different control loops, mentioned above; this was done to better assess the functionality of the DC–-DC power converter. It was incorporated to provide better transient and steady state responses of the system, as well as better dynamics. The PI controller loop was connected to the power circuit to form the completed Closed-loop network as depicted in Chapter 5, using voltage and current mode control models.

Figure 6-10 shows a stable output voltage of 10.36 V which resulted when 20 V input voltage using voltage-mode control also, when assessing the current-mode control two simulated runs using the output voltage were done with a different input voltages (3 V, 20 V) — this is illustrated in Figure 6-11 and Figure 6-12. It was confirmed that with current mode control there is a lower noise level response than is the case for voltage mode control.

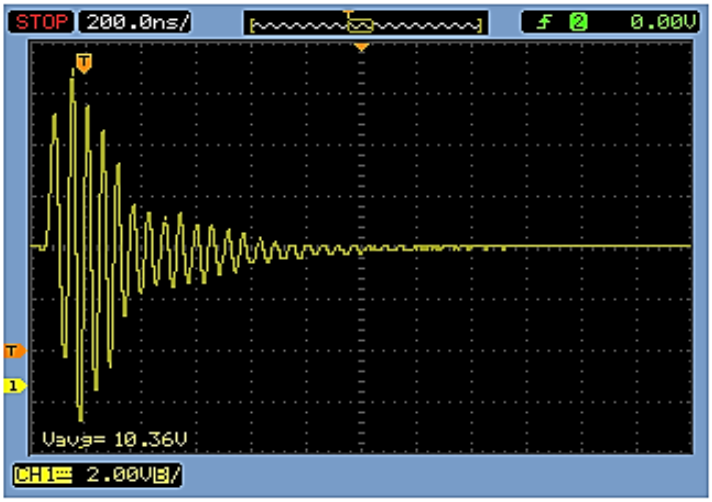


**Figure 6-10: Output voltage: voltage-mode control condition test validation with an input voltage of 20 V**

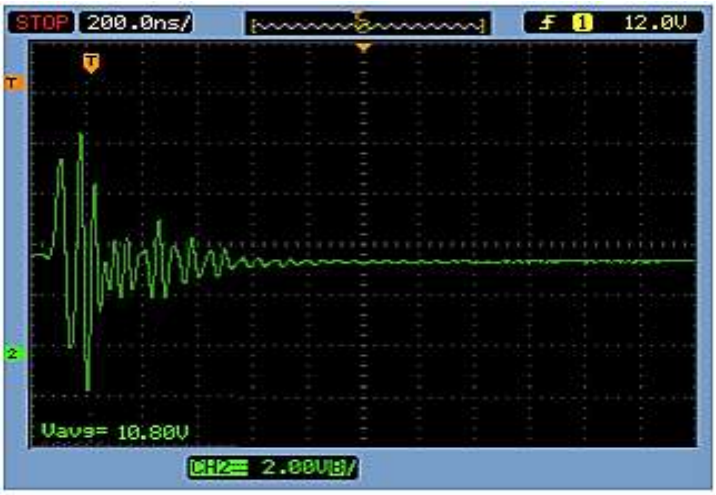


**Figure 6-11: Output voltage: current-mode control condition test validation with an input voltage of 3 V**

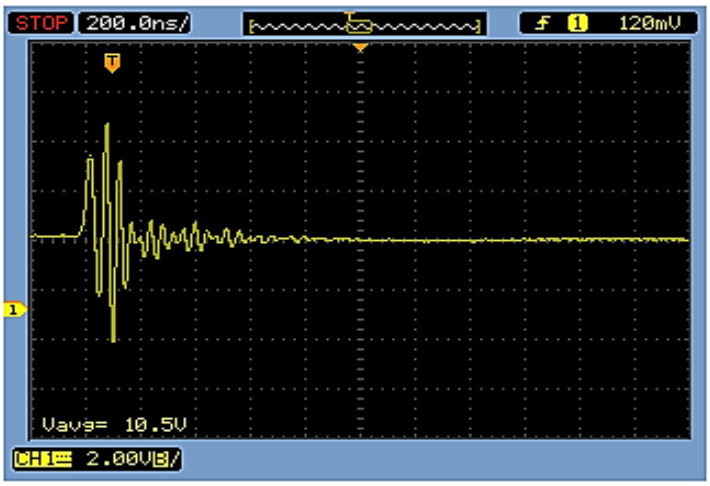


**Figure 6-12: Output voltage: current-mode control condition test validation with an input voltage of 20 V**

Load test validation was concluded by decreasing, and increasing the load of the DC–DC power converter. To assist with changing the applied load during the experiments, a dumping resistor was used. Figure 6-13 and Figure 6-14 illustrate the output voltage response of the converter while increasing and decreasing the load, for respectively voltage and current mode control. It can be seen the response with current-mode control is better than the response with voltage-mode control.


**Figure 6-13: Output voltage: voltage-mode control increase and decrease test validation with fixed input voltage**

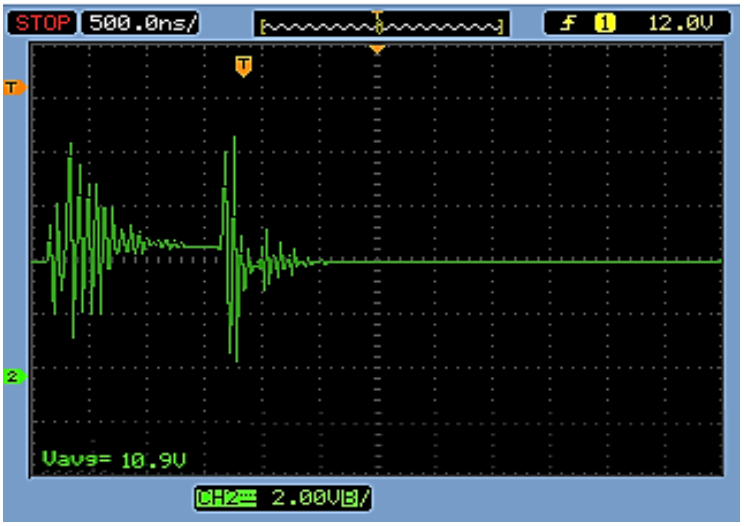


**Figure 6-14: Output voltage: current-mode control increase and decrease test validation with fixed input voltage**

### 6.3.3 Efficiency power circuit validation

The efficiency test validation was calculated by taking the solar activity in the space into consideration. Amongst these considerations are the satellite spin in orbit, the power is distributed in the system in the 24 hours that the panels face the sun, and after 24 hours the batteries take over the distribution of power in the system. In the experiment electricity from the grid replaced solar panels as the electricity source.

The efficiency was determined as follows:  the input current was measured with a multimeter, and this value is multiplied by the prevailing input voltage (between 3 V and 20 V), which yielded the input power; to obtain the output power, divide the output voltage squared was divided by the 12 Ω resistance of the load — the output power divided by the input power, expressed as a percentages then gives the efficiency for a particular set of circumstances. This efficiency test validation was done in both voltage- and current-mode control. Figure 6-15 shows the result of efficiency test verification using current-mode control techniques; it reached 90%. However, by using the voltage-mode control the efficiency is about 95%; this is depicted in Figure 6-16. The current-mode control efficiency is low than voltage-mode control, due to the uncontrolled switching frequency.

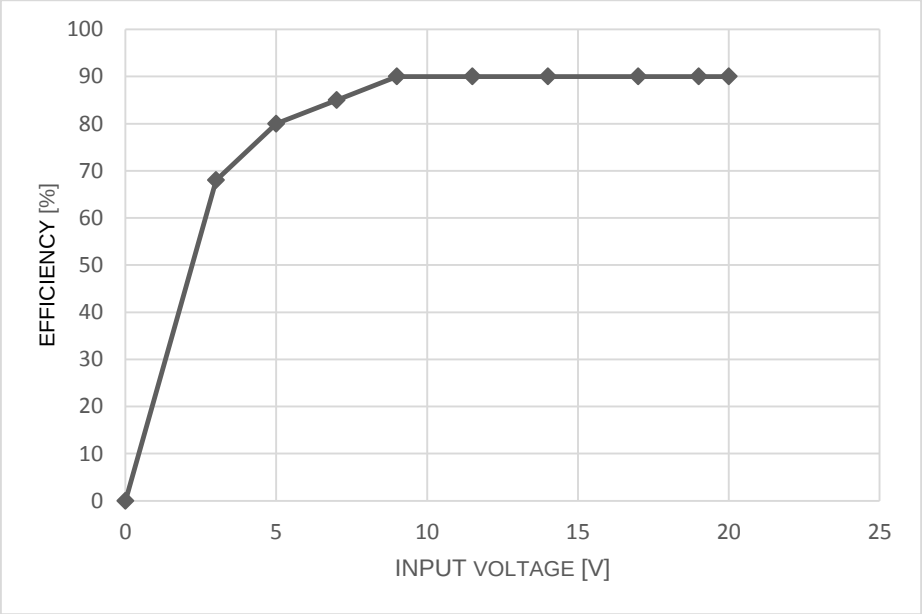


**Figure 6-15: Current-mode control: efficiency test validation**

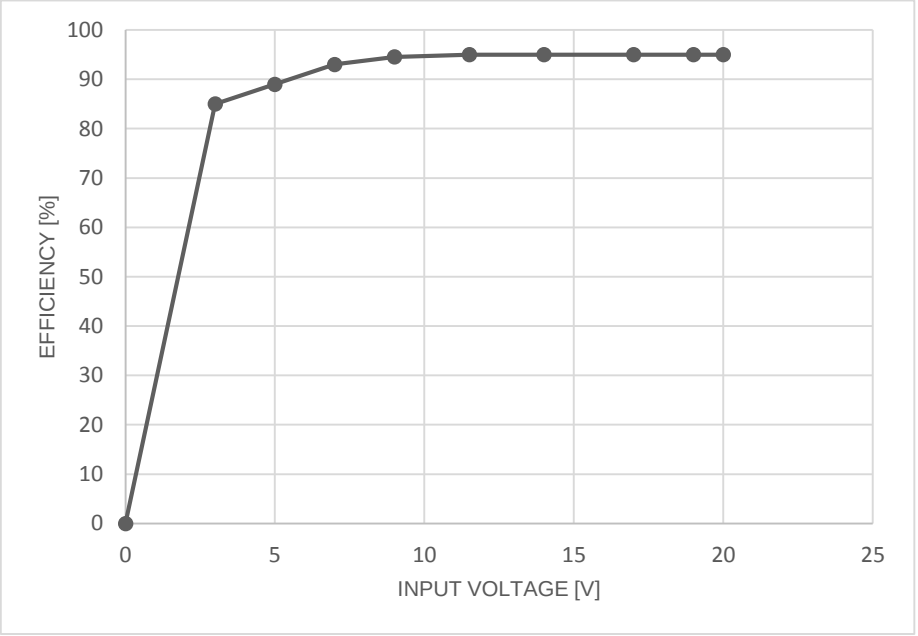


**Figure 6-16: Voltage-mode control: efficiency test validation**

## 6.4 Summary

In this chapter the front-end DC–DC power converter were investigated, as well as the analogue PWM signal aspects required to drive a MOSFET. Additionally, the summary comparison of front-end DC–DC power converter between the manufacturers namely; GomSpace, Clyde Space and this project research is shown on Table 6.1.

**Table 6.1: Comparative study**

| **Front-end DC–DC power converter electrical characteristics** | | | | | |
|---|---|---|---|---|---|
| **Manufactures** | **Switching frequency [kHz]** | **Input voltage [V]** | **Converter power [W]** | **Output voltage [V]** | **Efficiency [%]** |
| **Clyde Space** | 245 to 250 | 10 to 25 | 8 | 10 | 97 |
| **Project research** | 50 to 250 | 3 to 20 | 8 | 9.977 | 90.23–96.02 |
| **GomSpace** | 200 to 250 | 9 to 22 | 8 | 10 | 92 |

# Chapter 7 : LOW-ENERGY TEST IRRADIATION OF A MOSFET COMPONENT FOR SPACE APPLICATION

## 7.1 Introduction

The rapid development of modern technology has opened up the possibility to strive for an emerging class of nanosatellite mission with a predictable lifespan. One of the key factors which determines the lifespan of a nanosatellite, is the total radiation dose received by the spacecraft. As the total dose increases there is a general degradation in the power available on the nanosatellite; more specifically, there is degradation in the performance of components such as the photovoltaic cells, maximum power point tracking, the altitude system control, and telecommunications. This chapter investigates the effects of low energy protons on MOSFETs within a front-end power converter more specifically a SEPIC, as used in nanosatellite applications.

## 7.2 Description

The following procedures will be implemented:

- The MOSFET casing will be entirely thinned to 2 µm or less.
- The MOSFET, mounted on its 2 cm by 2 cm board (see Figure 7-1), will be the only component in the vacuum chamber.
- The MOSFET will be connected to the rest of its test circuit via the existing connector within the vacuum chamber.
- The MOSFET will be irradiated while the test circuit is operational (live).

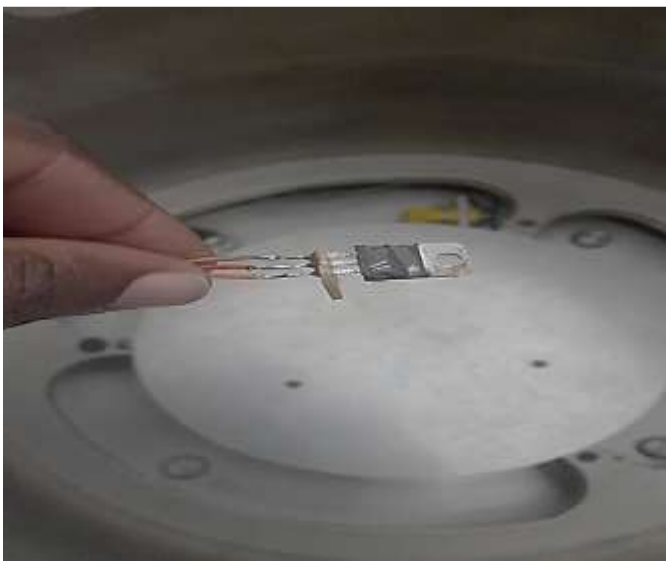

**Figure 7-1: MOSFET mounted on 4 cm$^2$ board**

### 7.3 Requirements

- 4 MeV protons,
- A beam diameter of 6 mm,
- The lowest stable current available (20 mA),
- The maximum fluence will be $1 \times 10^{15}$ protons/cm$^2$,
- A GW-INSTEK single variable power supply (0V–30V) to provide the power in the circuit,
- Laboratory virtual instrument engineering workbench (LABVIEW) software was used to create the interface between the beam chamber and the user,
- A Toptronic digital multimeter (T48), used for the continuity testing of the circuit, and to measure the output voltage of the circuit during the live test,
- Matlab software was used to plot data obtained from the experimental.

Stopping and Range of Ions in Matter' because it is a software package and this is how it is described (SRIM) simulation was used to shows the range of protons in set of epoxy; epoxy is the most popular integrated circuit (IC) encapsulate used in microelectronics. A flux value of $1\times10^{11}$ particle/sq.cm/s was calculated using the SRIM platform (see Figure 7-2); this reading was a function of the fluence and radiation exposure

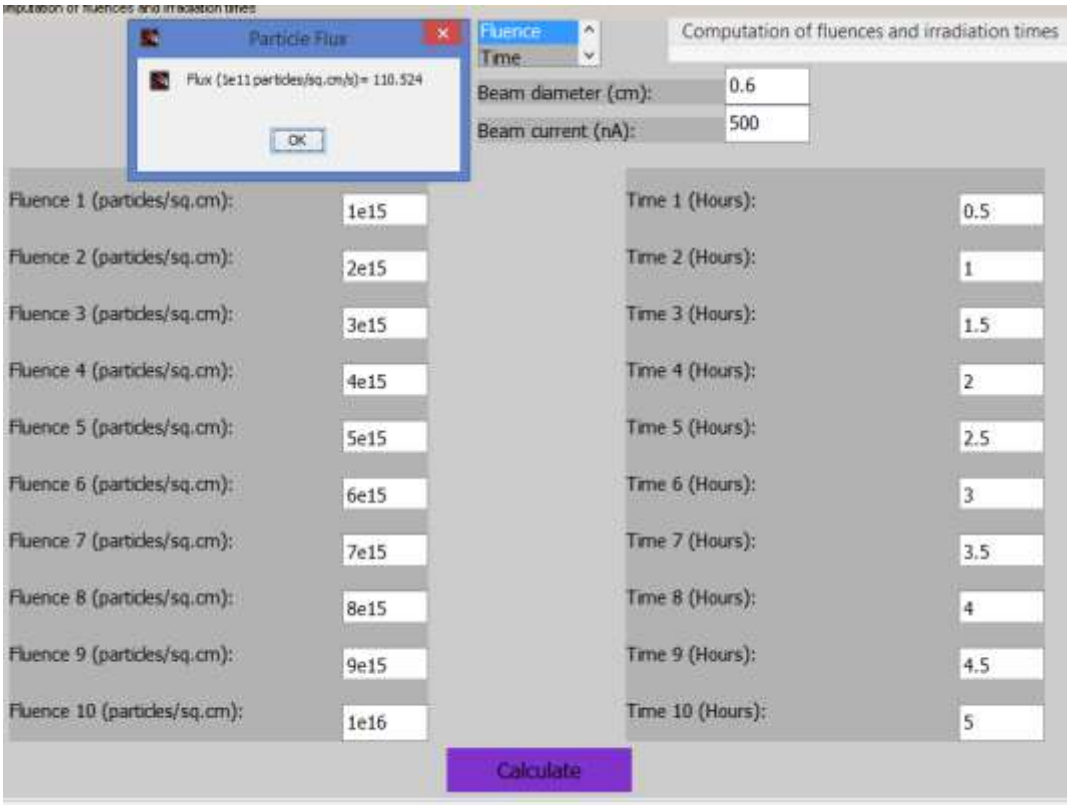


**Figure 7-2: Flux value calculation using the SRIM platform**

### 7.4 Step-by-step practical concept of the proton irradiation of a MOSFET

As mentioned in Chapter 2, MOSFETs are among the most sensitive of all semiconductors to radiation. Ionizing radiation in particular, can cause major changes, even after a relatively low-dose. In this research work, the radiation effects on a MOSFET device (see Appendix D) was determined by the level of the protons accumulated during the live test. The changes in electrical characteristics as a result of proton irradiation are principally influenced by the gate structure.

From the point of view of MOSFET device operation, the nature of the displacement damage produced by neutrons and high-energy protons is essentially the same, except that total dose effects should be taken into account. However, it should be noted that low-energy protons (4 MeV) cause 8.5 times more damage to MOSFET devices than do neutrons, whereas high-energy protons of 60 MeV are only about 1.8 times more damaging. Figure 7-4 illustrates the flow process of proton irradiation system.

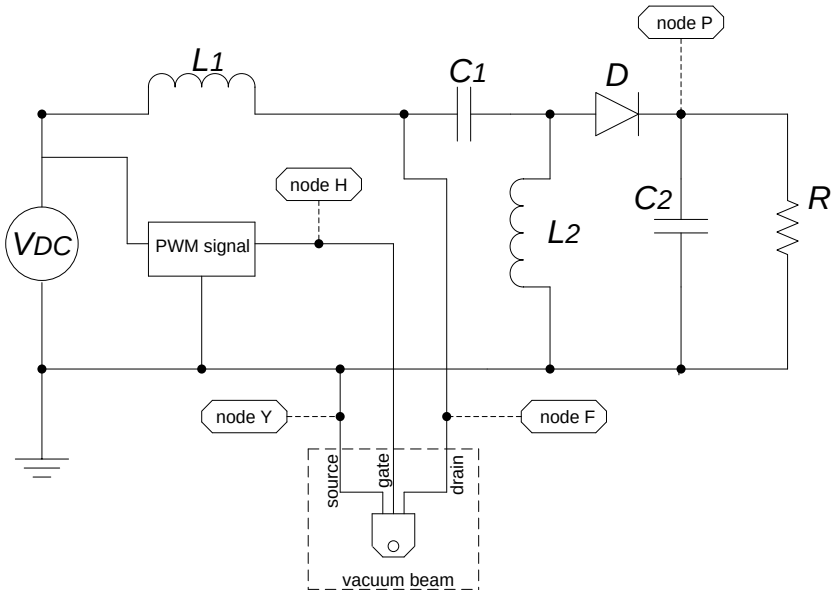


**Figure 7-3: MOSFET device set-up in the vacuum beam connected with SEPIC**

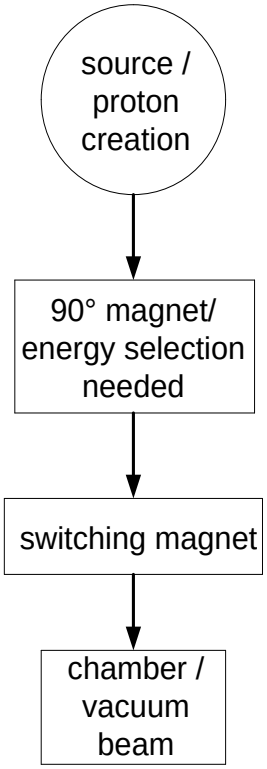


**Figure 7-4: Flow diagram of the proton irradiation process**

A commercial off-the-shelf MOSFET (STP60NF06FP) was selected for testing, together with the rest of a SEPIC. During the live experiment different voltages were recorded using LABVIEW platform; these voltages namely: the drain voltage ($V_F$), the gate voltage ($V_H$), the source voltage ($V_Y$), and the output voltage ($V_P$) of the SEPIC, as pointed out in Figure 7-3. The MOSFET device lasted for 30 minutes during the live experiment, and failed due to the heat generated by the proton beam inside the vacuum chamber. Figure 7-5 below illustrates the drain voltage recorded, there was a undershoot voltage at the beginning of the graph. Before the end time, the drain voltage decreased to about $10^{-3}$ V showing the failure of the MOSFET.

The square block view shown in Figure 7-5 depicts the unstable gate voltage of the MOSFET, is due to the protons bombardment during the live experiment. The source voltage of the MOSFET was connected to the ground of the circuit; theoretically the voltage measured at that point was 0 V. With regard to the gate voltage however, there were significant variations, ending with the voltage oscillating between -1 V and just over 4 V, with the MOSFET eventually failing at 4,3 V — see Figure 7-6. The output voltage of the SEPIC was recorded during the live experimental, and an average value of 10 V was noted. It is shown in Figure 7-7, that at the start of the experiment, an undershoot of the output voltage occurred before the required stable value achieved.

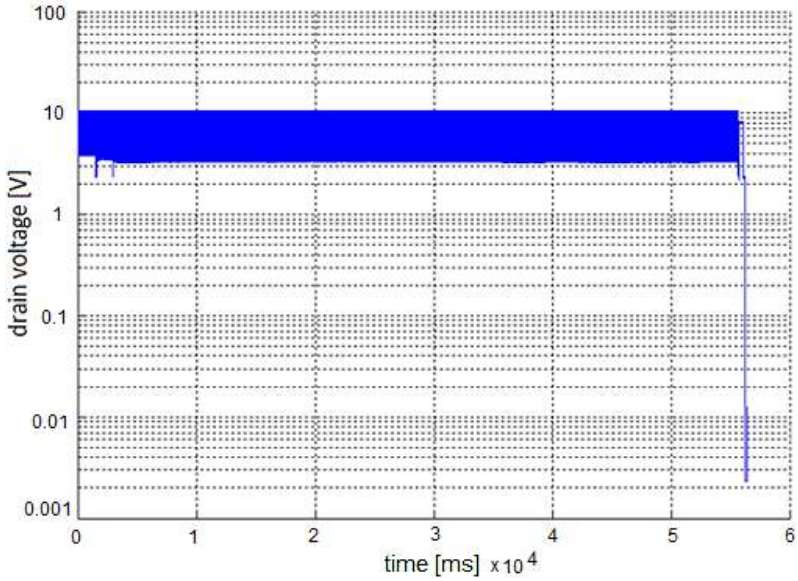


**Figure 7-5: Drain voltage recorded at node F (Figure 7-3) during the live test**

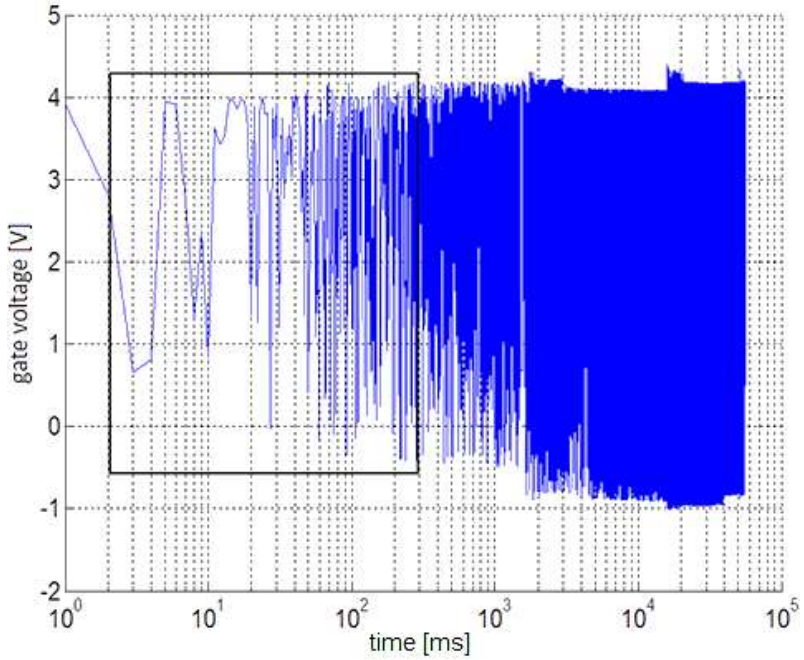


**Figure 7-6: Gate voltage recorded at node H (see Figure 7-3) during the live test**

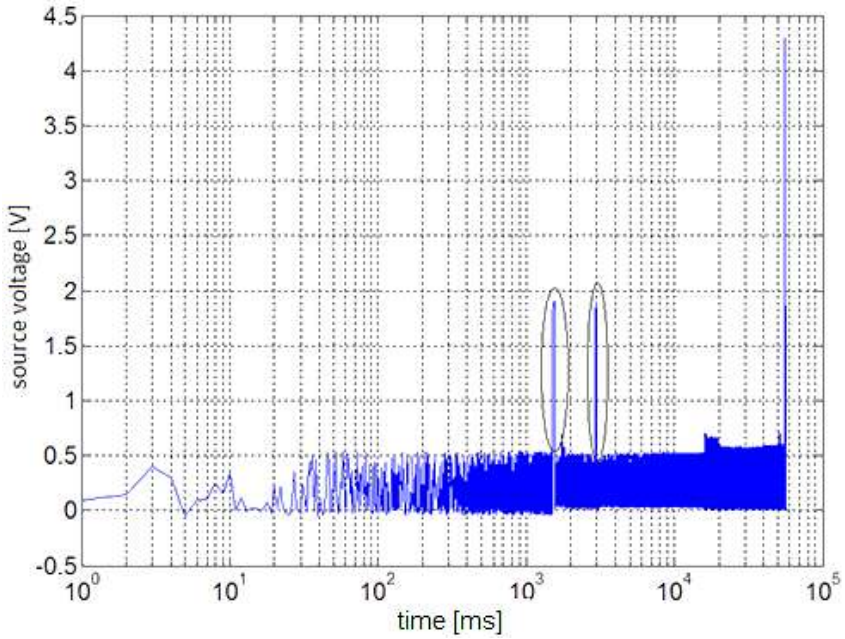


**Figure 7-7: Source voltage recorded at node Y (see Figure 7-3) during the live test**

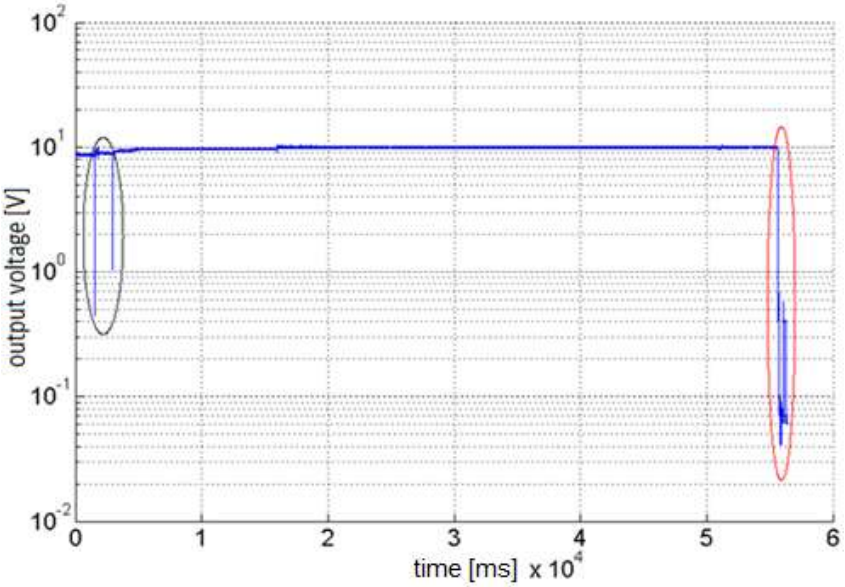


**Figure 7-8: Output voltage recorded at node P (see Figure 7-3) during the live test**

## 7.5 Summary

This chapter dealt with the practical evaluation of low-energy protons irradiation of a MOSFET. As mentioned, different types of data were record on the MOSFET pins using LAVIEW, and the step-step proton irradiation process was established. The knowledge gained in this chapter provided a good understanding of the radiation testing of the electronic components used in nanosatellites.

# Chapter 8 : CONCLUSION AND RECOMMENDATIONS FOR FURTHER STUDY

## 8.1 Introduction

The principal purpose of the project was to design and build a front-end DC–DC power converter using analogue pulse width modulation techniques, and test the functionality of this converter against established nanosatellite mission standards. Additionally radiation effects were investigated to determine whether they could possibly cause malfunction in the switching components of the MOSFET. Achieving these aims will widen the knowledge base of the F'SATI unit at CPUT in the area of the power systems, specifically in the field of DC–DC power converters. To complete this research, a literature study of different aspects of a nanosatellite front-end DC–DC power converter was done. After the completion of the literature study an original engineering model was designed and built. The requirements for the original model were determined through the research work covered in Chapter 4. The requirements were subsequently finalized in Chapter 5 with the development of the design considerations.

As discussed, the space environment is a harsh place for a nanosatellite and its electronic components. Radiation effects could cause malfunctioning of electronic components due to the total dose irradiance, single-event upset, single event latch-up, and displacement damage. Along with the trapped particles, these issues were addressed and discussed in the literature study. This damage could possibly cause the current and voltage changes in the photovoltaic cells. A nanosatellite is expected to work in a temperature range of -40$^{o}$C to 85$^{o}$C and where the thin atmosphere is considered to be a vacuum. Out-gassing of electronic components may occur in this vacuum, and it heightens the thermal problem affecting heat transfer limits.

## 8.2 Photovoltaic cells findings

Photovoltaic cells were studied as the primary energy source for the nanosatellite. From the literature study it was apparent that there are many problem factors that affect the amount of energy that can be extracted from a photovoltaic cell. The variable power source of photovoltaic cells results in a non-linear output of voltage and current. For of this research work, a variable power supply was used to simulate the energy output from a photovoltaic source.

Batteries are considered as a secondary source of energy for the nanosatellite. Batteries store energy for peak power demand and distribute the power during eclipse times.

- The battery type recommended for a nanosatellite mission is Li-Ion which, unlike NiMH batteries, has a high energy density and sustained load capabilities; the boundaries of operating voltage of Li-Ion and Li-Po batteries are also discussed.
- The literature study regarding the Li-Ion batteries established their operating temperature range as $0^{o}$C to $45^{o}$C during charging and indicated the maximum and minimum voltage that must be adhered to for optimal life span of the batteries.

Regarding this research work, a dummy resistor was used as the load; this was necessary to verify the load functionality of the front-end DC–DC power converter of the nanosatellite.

### 8.3 DC–DC power converter findings

DC–DC power converter control techniques required an extremely careful study, particularly in the domain of voltage- and current-mode control. Feedback and loop stability were discussed in terms of the voltage and current required for battery charging from the front-end DC–DC power converter. The stability of the front-end DC-DC power converter and compensation for better response frequencies of the system were discussed; this was done in order to improve the stability and gain required for transient response of the close loop system. Different types of compensation network for the front-end DC–DC power converter were discussed.

- To support the wide range input voltages from the photovoltaic cells, the front-end DC-DC power converter was required to be a SEPIC.
- The practical efficiency of the DC–DC SEPIC was 90.23% with the wide input range voltage from 3 V to 20 V, using voltage-mode control techniques; using the current-mode control under full load condition the efficiency was 96%.
- This was compared to the 8W DC–DC SEPIC marketed by GomSpace. This manufacturer claims an efficiency 92% from their DC–DC SEPIC based on voltage-mode control techniques. Manufacturer Clyde Space manufacture claims a 97% efficiency for their DC–DC SEPIC based on the current-mode control techniques, with a wide input voltage range and working at under full load conditions.

The front-end DC–DC power converter performed adequately though its efficiencies could be improved. The front-end DC–DC power converter effectively harnessed the maximum power from the input voltage and will charge batteries and power the load of a nanosatellite system.

### 8.4 MOSFET low-energy irradiation findings

An emerging class of nanosatellite mission requires assured operational lifetime and rapid development of modern technology. The research work describes a careful commercial off-

the-shelf approach to component selection and testing to meet the needs of space mission. Without careful attention, a nanosatellite lifespan may be cut short by space radiation effects.

The low-energy proton testing done on the MOSFET allows simultaneous exploration of different testes; namely: total dose, displacement damage of the MOSFET, as well as the single-even effects. The approach of low-energy proton irradiation MOSFET for a particular radiation environment was completed by using a vacuum chamber. The current was set at 20 mA, and the MOSFET was connected to the DC–DC SEPIC power converter; while bombarding the proton to the MOSFET with a flux value of $1\times10^{11}$ particle/sq.cm/s, the data recorded showing the behaviour of MOSFET were displayed in Chapter 7.

- The MOSFET failed after 30 minutes of intensive bombarding of protons.

This approach will allow in the near future researchers to build and test reliable and successful space components from modern commercial off-the-shelf component that will meet the radiation requirements.

### 8.5 Further study

Following on from this research, there are several aspects that warrant further investigation; among these are the following:

- More research can be done into the control techniques of DC–DC power converter as this may improve transient and frequency response of the front-end DC–DC SEPIC mode of control.
- Coupled inductors can be used with a DC–DC SEPIC to reduce the physical footprint of the converter.
- The improvement in efficiency would be more noticeable with the use of DC–DC synchronous SEPIC.
- Various radiation tests can be completed namely: TID test, SEEs, X-ray, gamma ray. These tests can be performed on the different components of the front-end DC–DC SEPIC.
- A digital PWM signal can be implemented using a field-programming gate array board.
- This design can be implemented using surface mounted components on a printed board circuit to reduce the physical size of the front-end DC–DC SEPIC, and to minimize the noise signal that is superimposed on the various output and control signals.

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## 8.7 APPENDICES

## APPENDIX A

Data recorded of changing load with a fixed input voltage using voltage mode controlled.

**Table 8.1: A1, Increasing and decreasing load test at a 3 V input voltage**

| **Load data** | **Input data** | | | **Output data** | | | **Relations** | |
|---|---|---|---|---|---|---|---|---|
| Resistance [Ω] | Voltage [V] | Current [A] | Power [W] | Voltage [V] | Current [A] | Power [W] | Efficiency [%] | Duty-cycle [%] |
| 12 | 3 | 2.727 | 8.010 | 9.713 | 0.811 | 7.718 | 96.354 | 76.402 |
| 18 | 3 | 1.853 | 5.442 | 9.718 | 0.542 | 5.157 | 94.763 | 76.411 |
| 22 | 3 | 1.534 | 4.508 | 9.720 | 0.444 | 4.224 | 93.700 | 76.415 |
| 25 | 3 | 1.363 | 4.003 | 9.721 | 0.391 | 3.720 | 92.930 | 76.417 |
| 28 | 3 | 1.228 | 3.606 | 9.722 | 0.349 | 3.324 | 92.179 | 76.418 |
| 30 | 3 | 1.153 | 3.386 | 9.722 | 0.326 | 3.104 | 91.672 | 76.419 |
| 6 | 3 | 5.345 | 15.700 | 9.699 | 1.618 | 15.371 | 97.905 | 76.376 |
| 4 | 3 | 7.955 | 23.369 | 9.684 | 2.423 | 22.979 | 98.331 | 76.348 |
| 3 | 3 | 10.558 | 31.016 | 9.669 | 3.225 | 30.541 | 98.468 | 76.320 |
| 2.5 | 3 | 12.635 | 37.117 | 9.657 | 3.865 | 36.557 | 98.491 | 76.298 |
| 2 | 3 | 15.742 | 46.243 | 9.639 | 4.822 | 45.527 | 98.452 | 76.264 |

**Table 8.2: A2, Increasing and decreasing load test at a 20 V input voltage**

| Load data | Input data | | | Output data | | | Relations | |
|---|---|---|---|---|---|---|---|---|
| Resistance [Ω] | Voltage [V] | Current [A] | Power [W] | Voltage [V] | Current [A] | Power [W] | Efficiency [%] | Duty-cycle [%] |
| 12 | 20 | 0.423 | 8.279 | 10.011 | 0.836 | 8.183 | 98.840 | 33.331 |
| 18 | 20 | 0.282 | 5.529 | 9.999 | 0.558 | 5.462 | 98.789 | 33.331 |
| 22 | 20 | 0.232 | 4.538 | 10.000 | 0.457 | 4.476 | 98.634 | 33.333 |
| 25 | 20 | 0.204 | 3.989 | 10.000 | 0.403 | 3.938 | 98.722 | 33.333 |
| 28 | 20 | 0.182 | 3.565 | 10.000 | 0.359 | 3.519 | 98.709 | 33.333 |
| 30 | 20 | 0.169 | 3.329 | 10.000 | 0.335 | 3.286 | 98.708 | 33.333 |
| 6 | 20 | 0.758 | 14.806 | 9.999 | 1.502 | 14.697 | 99.264 | 33.331 |
| 4 | 20 | 1.008 | 19.644 | 10.000 | 2.002 | 19.528 | 99.409 | 33.333 |
| 3 | 20 | 1.177 | 22.844 | 9.999 | 2.336 | 22.735 | 99.523 | 33.331 |
| 2.5 | 20 | 1.262 | 24.362 | 9.999 | 2.502 | 24.254 | 99.557 | 33.331 |
| 2 | 20 | 1.304 | 25.036 | 10.000 | 2.585 | 24.927 | 99.567 | 33.333 |

## APPENDIX B

Data recorded of changing load with a fixed input voltage using current mode controlled

**Table 8.3: B1, Increasing and decreasing load test at a 20 V input voltage**

| **Load data** | **Input data** | | | **Output data** | | | **Relations** | |
|---|---|---|---|---|---|---|---|---|
| Resistance [Ω] | Voltage [V] | Current [A] | Power [W] | Voltage [V] | Current [A] | Power [W] | Efficiency [%] | Duty-cycle [%] |
| 12 | 20 | 0.453 | 8.867 | 10.184 | 0.849 | 8.470 | 95.523 | 33.739 |
| 6 | 20 | 0.931 | 18.235 | 10.036 | 1.727 | 17.562 | 96.309 | 33.413 |
| 4 | 20 | 1.332 | 26.089 | 10.069 | 2.517 | 24.838 | 95.205 | 33.486 |
| 3 | 20 | 1.795 | 35.157 | 10.214 | 3.405 | 34.114 | 97.033 | 33.806 |
| 2.5 | 20 | 2.120 | 45.524 | 10.187 | 4.075 | 40.729 | 89.671 | 33.746 |
| 2 | 20 | 2.492 | 48.813 | 9.872 | 4.936 | 47.808 | 97.941 | 33.048 |
| 18 | 20 | 0.301 | 5.899 | 10.019 | 0.567 | 5.666 | 96.050 | 33.376 |
| 22 | 20 | 0.245 | 4.789 | 10.239 | 0.466 | 4.673 | 97.578 | 33.860 |
| 25 | 20 | 0.217 | 4.250 | 10.225 | 0.409 | 4.102 | 96.518 | 33.829 |
| 28 | 20 | 0.193 | 3.784 | 10.243 | 0.366 | 3.676 | 97.146 | 33.869 |
| 30 | 20 | 0.180 | 3.526 | 10.246 | 0.342 | 3.433 | 97.363 | 33.876 |

**Table 8.4: B2, Increasing and decreasing load test at a 3 V input voltage**

| Load data | Input data | | | Output data | | | Relations | |
|---|---|---|---|---|---|---|---|---|
| Resistance [Ω] | Voltage [V] | Current [A] | Power [W] | Voltage [V] | Current [A] | Power [W] | Efficiency [%] | Duty-cycle [%] |
| 12 | 3 | 2.707 | 7.951 | 9.705 | 0.809 | 7.708 | 96.943 | 76.387 |
| 18 | 3 | 1.898 | 5.577 | 9.944 | 0.553 | 5.390 | 96.647 | 76.823 |
| 22 | 3 | 1.558 | 4.577 | 9.932 | 0.452 | 4.401 | 96.155 | 76.802 |
| 25 | 3 | 1.367 | 4.018 | 9.942 | 0.398 | 3.881 | 96.590 | 76.819 |
| 28 | 3 | 1.240 | 3.644 | 9.987 | 0.357 | 3.496 | 95.938 | 76.899 |
| 30 | 3 | 1.162 | 3.414 | 9.992 | 0.334 | 3.266 | 95.665 | 76.908 |
| 6 | 3 | 5.345 | 15.700 | 9.699 | 1.618 | 15.371 | 97.905 | 76.376 |
| 4 | 3 | 7.955 | 23.369 | 9.684 | 2.423 | 22.979 | 98.331 | 76.348 |
| 3 | 3 | 10.558 | 31.016 | 9.669 | 3.225 | 30.541 | 98.468 | 76.320 |
| 2.5 | 3 | 12.635 | 37.117 | 9.657 | 3.865 | 36.557 | 98.491 | 76.298 |
| 2 | 3 | 15.742 | 46.243 | 9.639 | 4.822 | 45.527 | 98.452 | 76.264 |

## APPENDIX C

Data sheet from SOLAREX

# MSX-60 and MSX-64 Photovoltaic Modules

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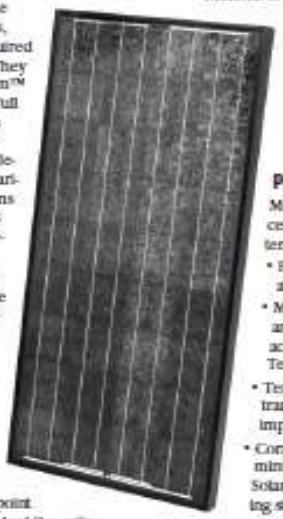
SOLAREX

The MSX-64 and -60 are among the most powerful of Solarex's Megamodule™ series, a product line which is the culmination of nearly three decades of extensive research in polycrystalline silicon photovoltaics. With over 3 amperes of current at peak power, these modules offer the most cost-effective package in the industry, and charge batteries efficiently in virtually any climate.

These modules may be used in single-module arrays or deployed in multiple-module arrays, wired in series/parallel combinations as required to meet current and voltage requirements. They are engineered under Solarex's IntegraSystem™ system integration concept, which ensures full compatibility with other Solarex subsystems and components (support hardware, regulators, etc.) and easy system assembly. As single-module arrays, they may be mounted on a variety of surfaces using optional kits or by means of user-fabricated support hardware. Solarex also offers hardware for supporting multiple-module arrays.



These modules are well-suited for virtually all applications where photovoltaics are a feasible energy source, including telecommunications systems, pumping and irrigation, cathodic protection, remote villages and clinics, and aids to navigation.

### Individually Tested, Labeled and Warranted

As part of the final inspection procedure, every MSX module is tested in a solar simulator and labeled with its actual output—voltage, current, and power at maximum power point ($P_{max}$)—at Standard Test Conditions and Standard Operating Conditions. Furthermore, the MSX-64 and -60 are covered by our industry-leading limited warranty, which guarantees:

- that no module will generate less than its guaranteed minimum $P_{max}$ when purchased;
- at least 80% of the guaranteed minimum $P_{max}$ for twenty years.

Contact Solarex's Marketing Department for full terms and limitations of this unparalleled warranty.

### Reliable and Versatile

The Megamodule series has proved its reliability at thousands of installations in every climate on Earth. Among the features that contribute to its versatility:

***Dual Voltage Capability***

These modules consist of 36 polycrystalline silicon solar cells electrically configured as two series strings of 18 cells each. The strings terminate in the junction box on the module back. Shipped in 12V configuration, modules may easily be switched to 6V configuration in the field by moving leads in the junction box. This design also allows installation of bypass diodes on 18-cell strings, which can improve reliability and performance in systems with nominal voltage 24V and above.

***High-Capacity Multifunction Junction Box***

The size of the junction box (25 cubic inches, 411cc) and its six-terminal connection block allow most system array connections to be made right in the J-box. The box also can accommodate bypass or blocking diodes or a small regulator, which can save the expense and labor of additional boxes. The box is raintight (IP54 rated) and accepts 1/2" nominal or PG13.5 conduit or cable fittings. The standard terminals accept wire as large as AWG #10 (6mm²); an optional terminal block accepts wire up to AWG #4 (25mm²).

### Proven Materials and Construction

Megamodule materials reflect Solarex's quarter-century of experience with solar modules and systems installed in virtually every climate on Earth.

- Polycrystalline silicon solar cells: efficient, attractive, stable.
- Modules are rugged and weatherproof: cell strings are laminated between sheets of ethylene vinyl acetate (EVA) and tempered glass with a durable Tedlar backsheet.
- Tempered glass superstrate is highly light-transmissive (low iron content), stable, and impact-resistant.
- Corrosion-resistant, bronze-anodized extruded aluminum frame is strong, attractive, compatible with Solarex mounting hardware and most other mounting structures.

### Options

- Blocking and bypass diodes
- Solarstat™ charge regulator
- Protective aluminum backplate

*More than 20 years ago, Solarex made the first polycrystalline silicon solar cell, advancing photovoltaics beyond the first-generation monocrystalline technology developed for electronics. Developed specifically for photovoltaics, polycrystalline silicon is used in Solarex's Mega™ series to provide a wide range of attractive, efficient modules. They require substantially less energy to manufacture and generate substantially more energy per rated watt than other crystalline silicon modules.*

630 Solarex Court, Frederick, MD 21703 USA • PHONE (301) 698-4200 • FAX (301) 698-4201 • www.solarex.com • info@solarex.com

## Safety Approved

MSX-60 and -64 modules are listed by Underwriter's Laboratories for electrical and fire safety (Class C fire rating), certified by TUV Rheinland as Class II equipment, and approved by Factory Mutual Research for application in NEC Class 1, Division 2, Group C & D hazardous locations.

## Quality Certified

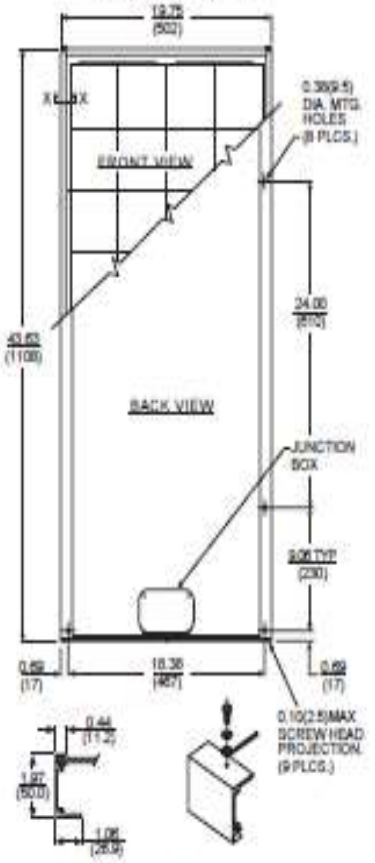
These modules are manufactured in our ISO 9001-certified factories to demanding specifications, and comply with IEC 1215, IEEE 1262 and CEC 505 test requirements, including:

- repetitive cycling between -40°C and 85°C at 85% relative humidity;
- simulated impact of one-inch (25mm) hail at terminal velocity;
- 2700 VDC frame/cell string isolation test;
- a "damp heat" test, consisting of 1000 hours of exposure to 85°C and 85% relative humidity;
- a "hot-spot" test, which determines a module's ability to tolerate localized shadowing (which can cause reverse-biased operation and localized heating);
- simulated wind loading of 125 mph (200 kph).

## Mechanical Characteristics

**Weight:** 15.9 pounds (7.2 kg)

**Dimensions:** Dimensions in brackets are in millimeters
Unbracketed dimensions are in inches
Overall tolerances ±1/8" (3mm)




## Typical Electrical Characteristics[1]

| | MSX-64 | MSX-60 |
|---|---|---|
| Maximum power ($P_{max}$) | 64W | 60W |
| Voltage @ $P_{max}$ ($V_{mp}$) | 17.1V | 17.1V |
| Current @ $P_{max}$ ($I_{mp}$) | 3.66A | 3.5A |
| Guaranteed minimum $P_{max}$ | 62W | 58W |
| Short-circuit current ($I_{sc}$) | 4.0A | 3.8A |
| Open-circuit voltage ($V_{oc}$) | 21.2V | 21.1V |
| Temperature coefficient of open-circuit voltage | ....-(80±10)mV/°C.... | |
| Temperature coefficient of short-circuit current | ....(0.065±0.015)%/°C.. | |
| Temperature coefficient of power | ....-(0.5±0.05)%/°C.... | |
| NOCT[2] | ..... 47±2°C ..... | |

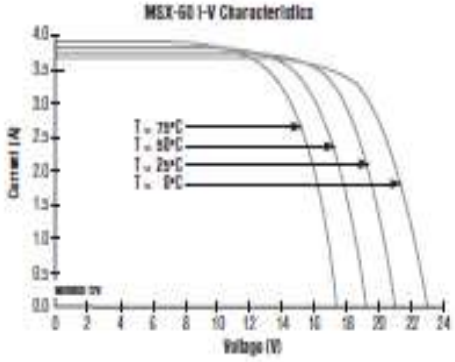
**NOTES:**

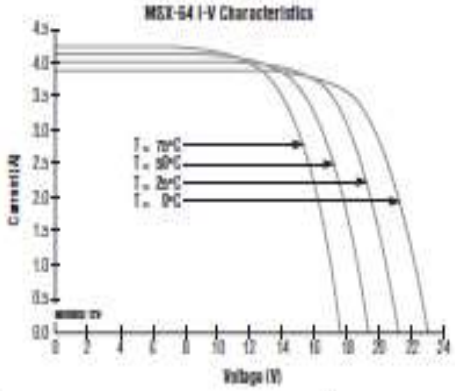
(1) These modules are tested, labeled and shipped in 12V configuration. These data represent the performance of typical 12V modules as measured at their output terminals, and do not include the effect of such additional equipment as diodes and cabling. The data are based on measurements made in a solar simulator at Standard Test Conditions (STC), which are:

- Illumination of 1 kW/m$^2$ (1 sun) at spectral distribution of AM 1.5;
- cell temperature of 25°C or as otherwise specified (on curves).

Operating characteristics in sunlight may differ slightly. To determine the characteristics of modules in 6V configuration, divide the 12V voltage characteristics by 2 and multiply current characteristics by 2. Power values are unchanged.

(2) Under most climatic conditions, the cells in a module operate hotter than the ambient temperature. NOCT (Nominal Operating Cell Temperature) is an indicator of this temperature differential, and is the cell temperature under Standard Operating Conditions: ambient temperature of 20°C, solar irradiation of 0.8 kW/m$^2$, and wind speed of 1 m/s.

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## VARIABLES AFFECTING PERFORMANCE

The performance of typical MEGA SX-64 and -60 modules is described by the I-V curves and electrical characteristics table on the next page. Each module's actual, tested output characteristics are printed on its label.

The current and power output of photovoltaic modules are approximately proportional to illumination intensity. At a given intensity, a module's output current and operating voltage are determined by the characteristics of the load. If that load is a battery, the battery's internal impedance will dictate the module's operating voltage. An I-V curve is simply all of a module's possible operating points (voltage/current combinations) at a given cell temperature and light intensity. Increases in cell temperature increase current but decrease voltage.

## TYPICAL ELECTRICAL CHARACTERISTICS(1)

| | 12 VOLT CONFIGURATION(2) MSX-64 | MSX-60 |
|---|---|---|
| Typical peak power ($P_p$) | 64W | 60W |
| Voltage @ peak power ($V_{pp}$) | 17.5V | 17.1V |
| Current @ peak power ($I_{pp}$) | 3.66A | 3.5A |
| Guaranteed minimum peak power | 62W | 58W |
| Short-circuit current ($I_{sc}$) | 4.0A | 3.8A |
| Open-circuit voltage ($V_{oc}$) | 21.5V | 21.1V |
| Temperature coefficient of open-circuit voltage | .....–(80±10)mV/°C..... | |
| Temperature coefficient of short-circuit current | ....(0.065±0.015)%/°C... | |
| Approximate effect of temperature on power | .....–(0.5±0.05)%/°C.... | |
| NOCT(3) | ..... 49°C ..... | |

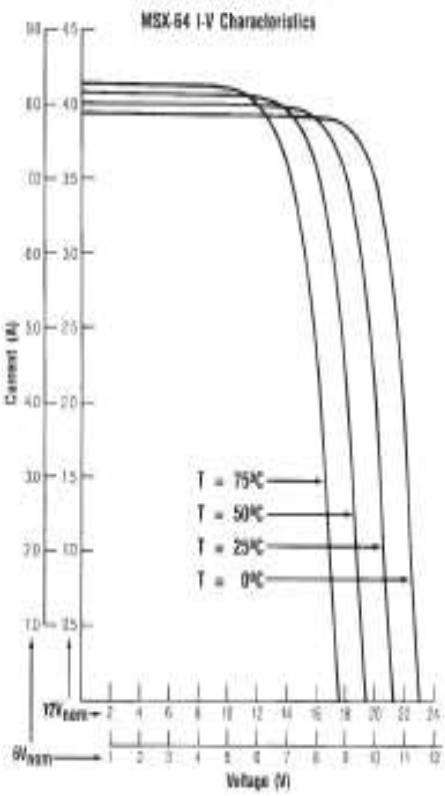
Notes:

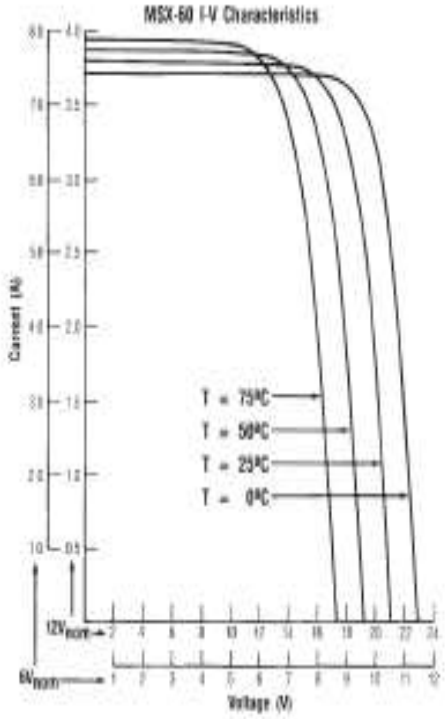
(1) These data represent the performance of typical modules as measured at their output terminals, and do not include the effect of such additional equipment as diodes and cabling. The data are based on measurements made at Standard Test Conditions (STC), which are:
- Illumination of 1 kW/m² (1 sun) at spectral distribution of AM 1.5
- Cell temperature of 25°C or as otherwise specified (on curves).

(2) Electrical characteristics of modules wired in the nominal 6V configuration may be found by using the 6V scales on the I-V curves. For more exact values, divide the 12V voltage characteristics in the table by 2 and multiply the 12V current characteristics by 2. Power values are unchanged.

(3) Under nearly all climatic conditions, the solar cells in an operating module are hotter than the ambient temperature, a fact which must be considered when reading module data. NOCT (Nominal Operating Cell Temperature) is an indication of this temperature rise, and is the cell temperature under Standard Operating Conditions: ambient temperature of 20°C, solar irradiation of 0.8 kW/m², and average wind speed of 1 m/s.

## I-V CHARACTERISTICS



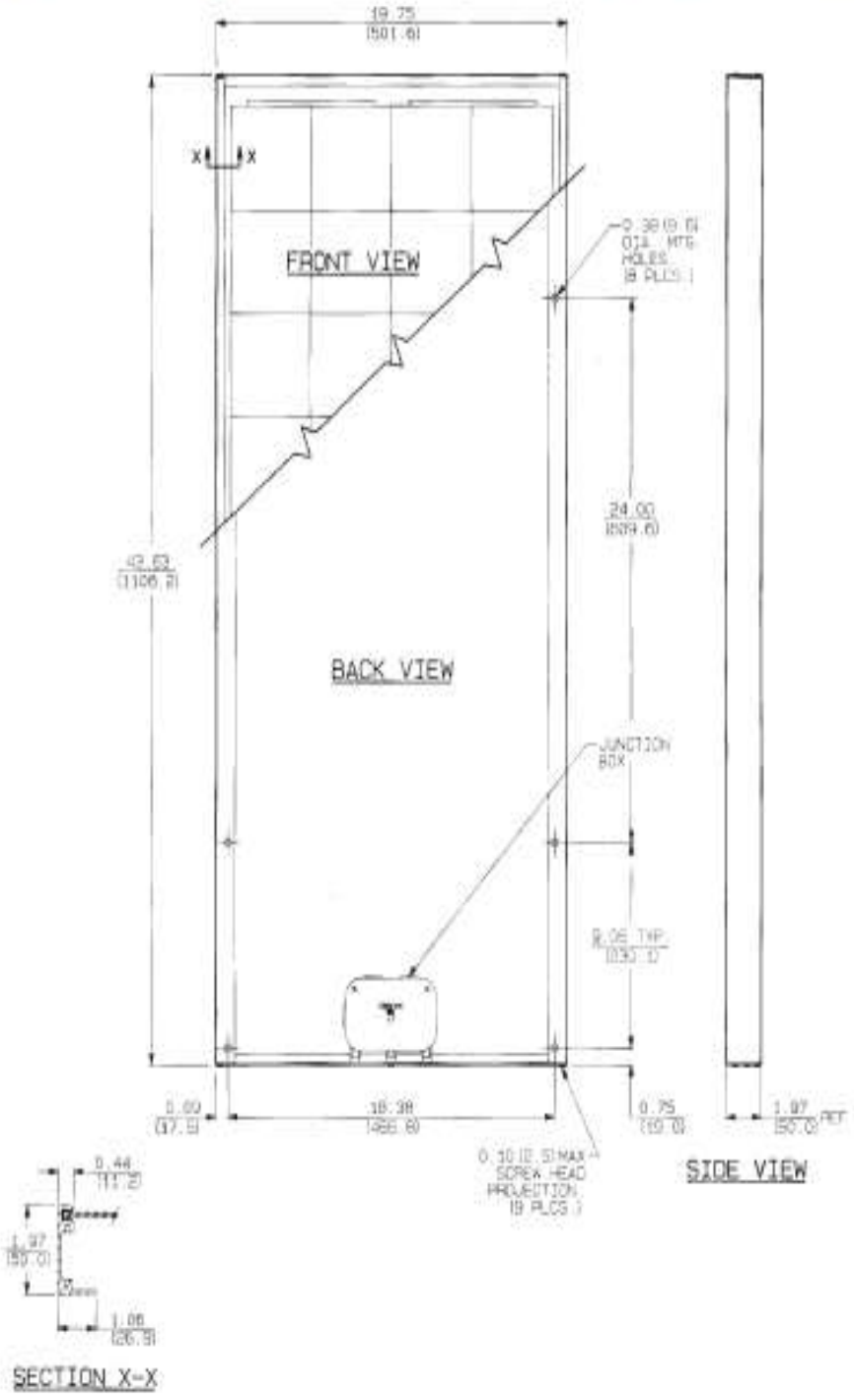



## MECHANICAL CHARACTERISTICS

**MEGA** SX-64 and -60 are mechanically identical, differing only in electrical output.

**Weight:** 15.9 pounds (7.2 kg)

**Dimensions:** Dimensions in brackets are in millimeters
Unbracketed dimensions are in inches



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## APPENDIX D

MOSFET datasheet

# STP60NF06FP

N-channel 60V - 0.014Ω - 30A TO-220FP
STripFET II™ Power MOSFET

### General features

| Type | $V_{DSS}$ | $R_{DS(on)}$ | $I_D$ |
|---|---|---|---|
| STP60NF06FP | 60V | <0.016Ω | 30A |

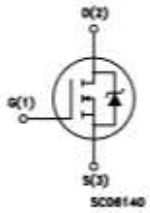
- Exceptional dv/dt capability
- 100% avalanche tested
- Application oriented characterization

TO-220FP

### Description

This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer application. It is also intended for any application with low gate charge drive requirements.

### Internal schematic diagram




### Applications

- Switching application

### Order code

| Part number | Marking | Package | Packaging |
|---|---|---|---|
| STP60NF06FP | P60NF06 | TO-220FP | Tube |

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2 Electrical characteristics . . . . . 4

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# 1 Electrical ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage ($V_{GS}$ = 0) | 60 | V |
| $V_{GS}$ | Gate- source voltage | ±20 | V |
| $I_D$ | Drain current (continuos) at $T_C$ = 25°C | 30 | A |
| $I_D$ | Drain current (continuos) at $T_C$ = 100°C | 21 | A |
| $I_{DM}$ (1) | Drain current (pulsed) | 120 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25°C | 30 | W |
| | Derating factor | 0.2 | W/°C |
| dv/dt (2) | Peak diode recovery voltage slope | 4 | V/ns |
| $V_{ISO}$ | Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s; Tc= 25°C) | 2500 | V |
| $T_{stg}$ | Storage temperature | – 55 to 175 | °C |
| $T_j$ | Max. operating junction temperature | | |

1. Pulse width limited by safe operating area
2. $I_{SD}$ ≤60A, di/dt ≤400 A/µs, $V_{DD}$ ≤24V, Tj ≤$T_{jmax}$

Table 2. Thermal data

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case max | 5 | °C/W |
| $R_{thj\text{-}a}$ | Thermal resistance junction-ambient max | 62.5 | °C/W |
| $T_l$ | Maximum load temperature for soldering purpose | 300 | °C |

Table 3. Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AS}$ | Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max) | 30 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting Tj=25°C, Id=Ias, Vdd=30V) | 370 | mJ |

# 2 Electrical characteristics

($T_{CASE}$=25°C unless otherwise specified)

**Table 4. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source Breakdown voltage | $I_D$ = 250 µA, $V_{GS}$ = 0 | 60 | | | V |
| $I_{DSS}$ | Zero gate voltage Drain current ($V_{GS}$ = 0) | $V_{DS}$ = Max rating<br>$V_{DS}$=Max rating, $T_C$=125°C | | | 1<br>10 | µA<br>µA |
| $I_{GSS}$ | Gate-body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ±20V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA | 2 | | 4 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS}$ = 10V, $I_D$ = 30A | | 0.014 | 0.016 | Ω |

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (1) | Forward transconductance | $V_{DS}$ = 15V, $I_D$=30A | | 50 | | S |
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 25V, f = 1 MHz, $V_{GS}$ = 0 | | 1810 | | pF |
| $C_{oss}$ | Output capacitance | | | 360 | | pF |
| $C_{rss}$ | Reverse transfer capacitance | | | 125 | | pF |
| $Q_g$ | Total gate charge | $V_{DD}$ = 48V, $I_D$ = 60A, $V_{GS}$ = 10V *(see Figure 12)* | | 49 | 66 | nC |
| $Q_{gs}$ | Gate-source charge | | | 18 | | nC |
| $Q_{gd}$ | Gate-drain charge | | | 14 | | nC |

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$<br>$t_r$ | Turn-on delay time<br>Rise time | $V_{DD}$ = 30V, $I_D$ = 30A<br>$R_G$ = 4.7Ω $V_{GS}$ = 10V *(see Figure 13)* | | 16<br>108 | | ns<br>ns |
| $t_{d(off)}$<br>$t_f$ | Turn-off-delay time<br>Fall time | $V_{DD}$ = 30V, $I_D$ = 30A,<br>$R_G$ = 4.7Ω, $V_{GS}$ =10V *(see Figure 13)* | | 43<br>20 | | ns<br>ns |

Table 7. Source drain diode

| Symbol | Parameter | Test conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | | | 30 | A |
| $I_{SDM}$ (1) | Source-drain current (pulsed) | | | | 120 | A |
| $V_{SD}$ (2) | Forward on voltage | $I_{SD}$ = 60A, $V_{GS}$ = 0 | | | 1.3 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 60A, $V_{DD}$=25V di/dt = 100A/µs, Tj = 150°C *(see Figure 13)* | | 75 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | | 182 | | nC |
| $I_{RRM}$ | Reverse recovery current | | | 5 | | A |

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

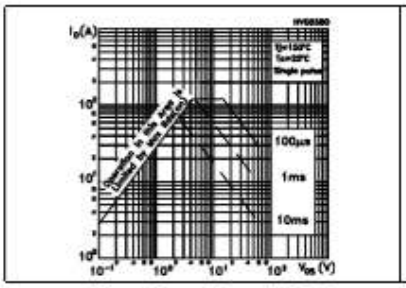



Figure 2. Thermal impedance

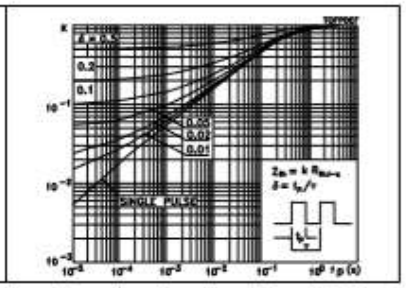



Figure 3. Output characteristics

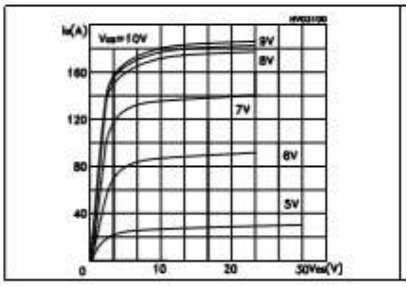



Figure 4. Transfer characteristics

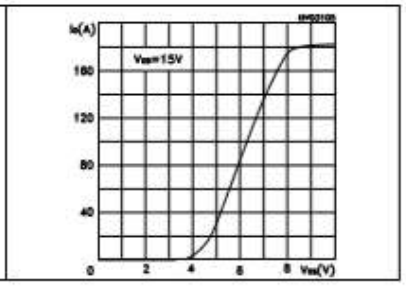



Figure 5. Source-drain diode forward characteristics

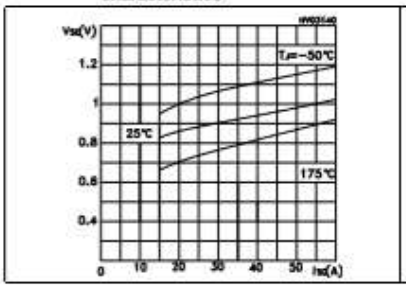



Figure 6. Static drain-source on resistance

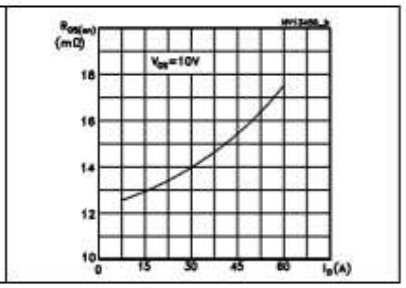


Figure 7. Gate charge vs gate-source voltage

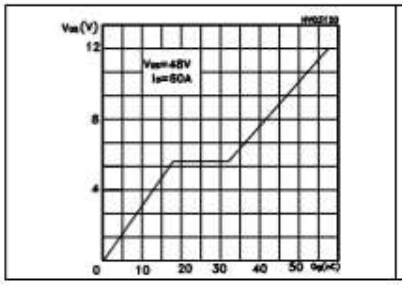



Figure 8. Capacitance variations

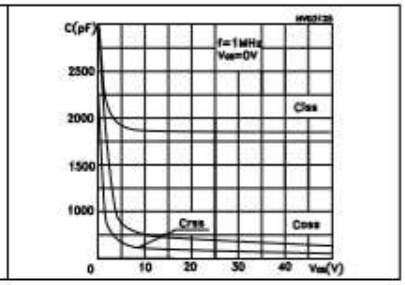



Figure 9. Normalized gate threshold voltage vs temperature

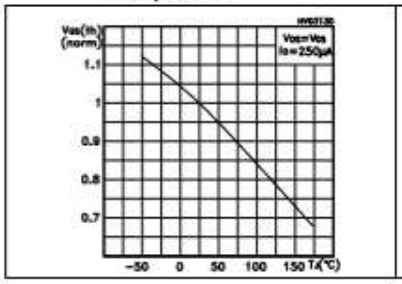
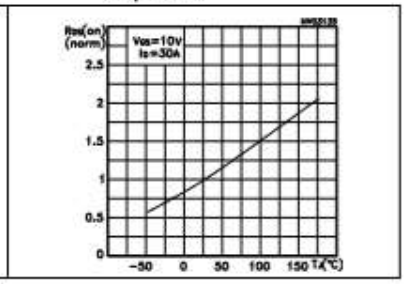



Figure 10. Normalized on resistance vs temperature



# 3 Test circuit

Figure 11. Switching times test circuit for resistive load

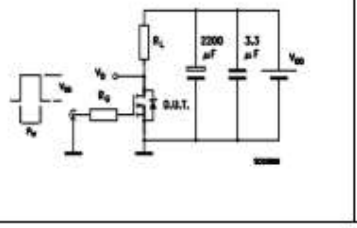


Figure 12. Gate charge test circuit

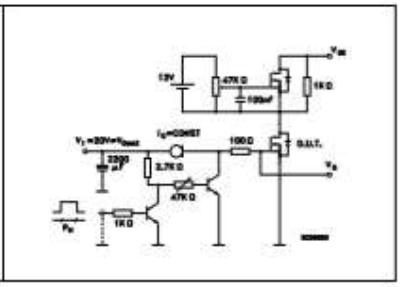


Figure 13. Test circuit for inductive load switching and diode recovery times

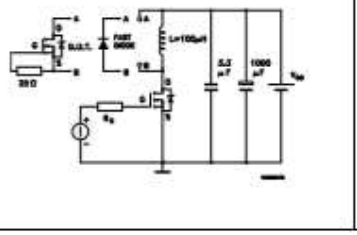


Figure 14. Unclamped Inductive load test circuit

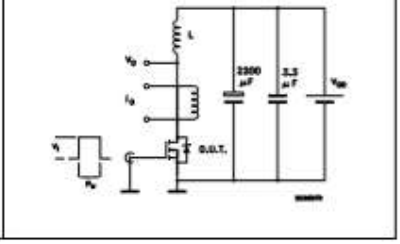


Figure 15. Unclamped inductive waveform

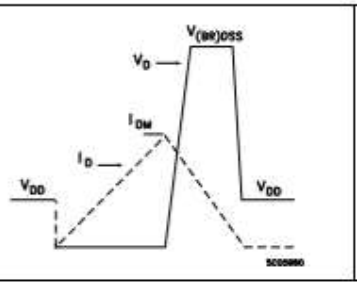
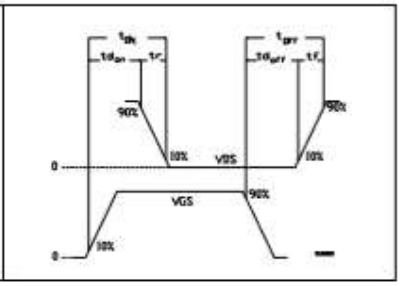



Figure 16. Switching time waveform



# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

## TO-220FP MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 4.4 | | 4.6 | 0.173 | | 0.181 |
| B | 2.5 | | 2.7 | 0.098 | | 0.106 |
| D | 2.5 | | 2.75 | 0.098 | | 0.108 |
| E | 0.45 | | 0.7 | 0.017 | | 0.027 |
| F | 0.75 | | 1 | 0.030 | | 0.039 |
| F1 | 1.15 | | 1.7 | 0.045 | | 0.067 |
| F2 | 1.15 | | 1.7 | 0.045 | | 0.067 |
| G | 4.95 | | 5.2 | 0.195 | | 0.204 |
| G1 | 2.4 | | 2.7 | 0.094 | | 0.106 |
| H | 10 | | 10.4 | 0.393 | | 0.409 |
| L2 | | 16 | | | 0.630 | |
| L3 | 28.6 | | 30.6 | 1.126 | | 1.204 |
| L4 | 9.8 | | 10.6 | .0385 | | 0.417 |
| L5 | 2.9 | | 3.6 | 0.114 | | 0.141 |
| L6 | 15.9 | | 16.4 | 0.626 | | 0.645 |
| L7 | 9 | | 9.3 | 0.354 | | 0.366 |
| Ø | 3 | | 3.2 | 0.118 | | 0.126 |