IEC 61850 STANDARD-BASED GOOSE MESSAGE APPLICATION FOR A SHUNT CAPACITOR BANK PROTECTION

By

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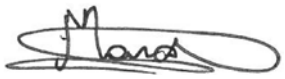
Declaration

I, **Manduleli Alfred Mquqwana**, declare that the contents of the thesis represent my own unaided work, and that the thesis has not previously been submitted for academic examination towards any qualification. Furthermore, it represents my own opinions and not necessarily those of the Cape Peninsula University of Technology.



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Signature

Date

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I wish to thank the following people:

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Dedication

The thesis is dedicated to my late mother **Nontombizangoku No-Income Mquqwana** and the entire family. Further dedication goes to my children, **Oyena Imitha Mquqwana**, **Sibahle Amila Mquqwana**, **Aqhama Imbo Mquqwana** and **Iyana Gumata.**

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Glossary of terms

Capacitor a device used to store an electric charge, consisting of one or more pairs of conductors separated by an insulator.

Capacitor Bank is a grouping of several capacitors units of the connected in, either, series, parallel or combination to provide the required rating.

Capacitor Unit is a grouping of capacitors, either connected in series, parallel or a combination to provide a required rating.

Delay is a waiting time implemented before taking an action.

Differential protection is protection scheme whereby voltage measurements, such as bus bar and capacitor tap, are continuously compared against each other. Should the difference be above a certain threshold, an action is taken, be it tripping the breaker or sending an alarm to SCADA system.

Distribution Management System is a collection of applications designed to monitor and control the entire distribution network efficiently and reliably. It acts as a decision support system to assist the control room and field operating personnel to monitor and control the electric distribution system.

Energy Management System is a system of computer-aided tools used by operators of electric utility grids to monitor, control, and optimize the performance of the generation and/or transmission system.

GOOSE messages are messages “published” by a device via Ethernet multicast such that they can be “subscribed” to by any number of other devices on the network and these are retransmitted in case of lost packets or devices coming online which need the current state.

Graphical User Interface is a type of user interface that allows users to interact with electronic devices through graphical icons and visual indicators such as typed command labels or text navigation.
Hardware in the loop is a technique that is used in the development and test of complex real-time embedded systems.

High Voltage Alternating Current system is high voltage three phase alternating current transmission lines which are 132kV and above.

High-Voltage Direct Current system is an electric power transmission system that uses direct current for the bulk transmission of electrical power, in contrast with the more common alternating current (AC) systems.

Human Machine Interface is the part of the machine that handles the Human-machine interaction. Membrane Switches, Rubber Keypads and Touchscreens are examples of the Human Machine Interface, which we can see and touch.

IEC 61850 Standard is an international standard defining communication protocols for intelligent electronic devices at electrical substations developed by IEC TC57.

Intelligent Electronic Device is a term used in the electric power industry to describe microprocessor-based controllers of power system equipment, such as relays, circuit breakers, transformers and capacitor banks.

LAN is a group of computers and devices that share a communications line or wireless link to a server within the same geographical area.

Local Area Network is a computer network that interconnects computers within a limited area such as a home, school, computer laboratory, or office building using a suitable communication medium.

Over voltage is a state in an electric power system whereby voltage measurement is more than a safe, normal operating value defined for a particular power system network, off which in most cases, is 1.1 time the rated voltage.

Overcurrent is an electric current in excess of that which is normal, safe, or allowed for in a particular circuit.

Pickup is a threshold value configured on the protection relay which, if reached or exceeded, an action such, trip or alarm issue is taken after the delay time has elapsed.
Programmable Logic Controller is a digital computer used for automation of electromechanical processes, such as control of machinery on factory assembly line.

Protection relay is an intelligent electronic device used to trip a circuit breaker based on the protection algorithms applied.

Real Time Digital Simulator provides power systems simulation technology for fast, reliable, accurate and cost-effective study of power systems with complex High Voltage Alternating Current (HVAC) and High Voltage Direct Current (HVDC) networks. RTDS is a fully digital electromagnetic transient power system simulator that operates in real time.

Remote Terminal Unit is a microprocessor-controlled electronic device that interfaces objects in the physical world to a distributed control system or SCADA (Supervisory Control and Data Acquisition) system by transmitting telemetry data to a master system, and by using messages from the master supervisory system to control connected objects.

Supervisory Control and Data Acquisition is a system operating with coded signals over communication channels and to provide control for remote equipment. The supervisory system may be combined with a data acquisition system by adding the use of coded signals over communication channels to acquire information about the status of the remote equipment for display/recording functions.

System-based testing is testing of a complete and fully integrated system either from local and/or remote location.

Test injection device is a device capable of injecting secondary scaled measurements to devices such as protection relays for testing purposes.

Transmission Control Protocol/Internet Protocol provides end-to-end connectivity specifies how data should be formatted, addressed, transmitted, routed and received at the destination.

Under voltage is a state in an electric power system whereby voltage measurement is less than a normal operating value defined for a particular power system network. This value, in most cases, is 0.9 times the rated voltage network voltage.

Virtual Local Area Network (Virtual LAN) is a subnetwork which can group together collections of devices on separate physical local area networks (LANs).

Wide Area Network is a telecommunications network that links across metropolitan, regional, national or international boundaries using communications medium and telecommunication lines.

Nomenclature

27P1	–	Under voltage Level 1
27P2	–	Under voltage Level 2
50P1	–	Overcurrent Level 1
50P2	–	Overcurrent Level 2
50P3	–	Overcurrent Level 3
59P1	–	Over voltage Level 1
59P2	–	Over voltage Level 2
87AP	–	Alarm Pickup
87ATP	–	Trip Phase A Pickup
87ATPD	–	Trip Phase A Delayed Pickup
87BTP	–	Trip Phase B Pickup
87BTPD	–	Trip Phase B Delayed Pickup
87CTP	–	Trip Phase C Pickup
87CTPD	–	Trip Phase C Delayed Pickup
87HP	–	High Pickup
87TP	–	Trip Pickup
87TP1P	–	Trip Pickup greater than 0
87TP2P	–	Trip Pickup less than or equal to 0
87TPD	–	Delayed Trip Pickup
87TPDO	–	Trip Dropout Delay
87TPEN	–	Trip Enable
87TPPU	–	Trip Pickup Delay
A87PDIF1	–	Instantaneous Differential Voltage – Alarm
AA87PDIF1	–	Instantaneous Differential Voltage – Alarm Above Tap
AEP	–	American National Standards Institute
ANSI	–	American Electric Power
BA87PDIF1	–	Instantaneous Differential Voltage – Alarm Below Tap
BRCB	–	Buffered Report Control Blocks
CBA	–	Capacitor Bank Assistant
CBP	–	Capacitor Bank Protection
CMC	–	Calibration and Measurement Capability
CID	–	Configured IED Description

CT	–	Current Transformer
DA	–	Distribution Automation
DMT	–	Definite Minimum Time
DMS	–	Distribution Management System
DNP3	–	Distributed Network Protocol Version 3.0
DO	–	Data Object
ESS	–	Energy Storage Systems
FACTS	–	Flexible Alternating Current Transmission Systems
FTP	–	File Transfer Protocol
FDIR	–	Fault Detection, Isolation and Restoration
GOOSE	–	Generic Object Oriented Substation Event
GPS	–	Global Position System
GSSE	–	Generic Substation Status Event
H87PDIF1	–	Instantaneous Differential Voltage – High set
HMI	–	Human Machine Interface
HV	–	High Voltage
IEC	–	International Electrotechnical Commission
IED	–	Intelligent Electronic Device
IEEE	–	Institute of Electrical and Electronic Engineers
LVC	–	Low Voltage Capacitor
MAC	–	Media Access Control
MMS	–	Message Manufacturing Specification
MV	–	Medium Voltage
NTP	–	Network Time Protocol
O1P1PTOV1	–	Over voltage Element 1, Level 1
O1P2PTOV1	–	Over voltage Element 1, Level 2
OSI	–	Open System Interconnect
PC	–	Personal Computer
PCC	–	Point of Common Coupling
PMU	–	Phasor Measurement Unit
POTT	–	Permissive Overreach Transfer Trip
PTP	–	Precision Time Protocol
RMS	–	Root Mean Square
RTAC	–	Real Time Automation Controller

RTDS	– Real Time Digital Simulator
RTU	– Remote Terminal Unit
SAS	– Substation Automation System
SBT	– System-based Testing
SCADA	– Supervisory Control and Data Acquisition
SCB	– Shunt Capacitor Banks
SCL	– Substation Configuration Language
SCD	– Substation Configuration Description
SEL	– Schweitzer Engineering Laboratories
STATCOM	– Static Synchronous Compensators
SVC	– Static Var Compensators
T87PDIF1	– Instantaneous Differential Voltage – Trip
TCP/IP	– Transmission Control Protocol/Internet Protocol
TRIPPTRC1	– Bank General Trip Asserted
TRIPPTRC2	– Bank General Trip Asserted
TVA	– Tennessee Valley Authority
U1P1PTUV1	– Under voltage Element 1, Level 1
U1P2PTUV1	– Under voltage Element 1, Level 2
UCA	– Utility Communications Architecture
URCB	– Unbuffered Report Control Block
VLAN	– Virtual Local Area Network
VT	– Voltage Transformer
WG1TPIOC7	– Instantaneous Zero-sequence Overcurrent Level 1
WG2TPIOC8	– Instantaneous Zero-sequence Overcurrent Level 2
WG3TPIOC9	– Instantaneous Zero-sequence Overcurrent Level 3
WP1TPIOC1	– Instantaneous Phase Overcurrent Level 1
WP2TPIOC2	– Instantaneous Phase Overcurrent Level 2
WP3TPIOC3	– Instantaneous Phase Overcurrent Level 3

List of Symbols

C_{capi} - Annual cost of capacitor bank including installation, maintenance, etc.

C_{eLS} - Number of capacitor elements on the left hand side string

C_{eRS} - Number of capacitor elements on the right hand side string

C_{losses} - Annual cost of losses

C_{max} - Voltage correction factor for maximum short circuit currents

$C_{volviol}$ - Fictitious cost used for voltage violations

$I"_{B1}$ - Initial symmetrical short circuit current at the feeder connection Bus 1

I_{cap} - Nominal capacitor bank current

I_{rcap} - Rated capacitor bank current at voltage and reactive power rating

I_{str} - Nominal string current

PTR_{bus} - Bus VT ratio

PTR_{tap} - Tap VT ratio

S_{erat} - Rated element power

S_{erat} - Rated element power

S_{rT} - Rated apparent power of the transformer

T_{cost} - Total annual network cost

U_{NB1} - Nominal system voltage at the connection point Bus 1

U_{kr} - Short circuit voltage at rated current in percentage

U_n - Rated voltage of the capacitor bank

U_{rT} - Rated voltage of the transformer

V_{bsec} - Secondary voltage of the bus VT

V_{bus} - Bus voltage

V_e - Nominal element voltage

V_{eop} - Nominal operational element voltage as a percentage

V_{erat} - Rated element voltage

V_{erat} - Rated element voltage

V_{tap} - Tap voltage

V_{tsec} - Secondary voltage of the tap VT

Z_{B1max} - Impedance measured at Bus 1 from the source feeder

Z_T - Impedance of the transformer

Z_{TAeq} - Total equivalent impedance above tap

Z_{TAeq} - Total equivalent impedance above the tap

Z_{eq} - Element equivalent impedance

Z_{eq} - Rated element impedance

t_r - Rated transformation of the transformer

ε_0 - Permittivity of free space

ε_r - Relative permittivity of the dielectric between the plates

ΔV - Potential difference

A - Area

C - Capacitance

Q - Reactive power

d - Distance between plates

dV - Voltage deviation

k - Compensation factor

Abstract

Capacitor banks play an important function in power systems, helping to enhance voltage profiles, reduce power system losses, correct power factor, and release system capacity. It is consequently critical that they are successfully and efficiently safeguarded through the use of quick and dependable protection solutions. When capacitor banks fail, they cause maintenance concerns, making it difficult to identify broken units/elements and time consuming for specialists, perhaps resulting in voltage control issues or the loss of any of the above-mentioned benefits. As a result, the goal of the research is to use the dedicated voltage differential protection function to identify the unit or element failure within the capacitor bank. The failure of capacitor elements either above or below the tap results in differential voltages detected and these differential voltages are calculated for each element failure to determine protection settings for alarm and trip conditions. To determine the fault location either above or below the tap, the sign of the detected differential voltages is used, with a positive sign indicating the fault is below the tap while a negative sign indicates the fault above the tap. These voltages are monitored per phase and this minimizes fault-finding times as the fault location is identified during fault reporting.

The voltage differential protection scheme is used as the main protection of the shunt capacitor bank for faults within the capacitor bank, while for backup protection against external faults, overcurrent and over/under voltage protection schemes are used. A simulation of the network on DIGSILENT software package is performed in order to test backup protection schemes for faults outside the shunt capacitor bank installation.

Two modes of operation are considered: i) Alarm, which is activated when a few capacitor bank elements fail but the bank can still be operated for a short period of time, and ii) Trip, which is activated when differential voltages detected result in the capacitor bank operating in an unsafe manner, requiring the bank to be disconnected from the power system network. The use of system-based testing for shunt capacitor bank voltage differential protection function testing is explored.

A lab-scale test bench is setup to test the implementation of shunt capacitor bank protection for both main and backup protections. The protection settings calculated are applied to a SEL 487V protection relay and the network under study is simulated in the RelaySimTest software package for system-based testing functionality which does not only test steady state conditions but transient state conditions also. A local area network is setup which consists of the SEL 487V protection relay, SEL 3555 RTAC, SIEMENS

RUGGEDCOM RSG2288 network switch, SEL 2488 GPS clock, OMICRON CMC 256 plus and CMC 356 units, and RelaySimTest software.

To test the voltage differential function, two Calibration and Measurement Capability (CMCs) test injection devices, representing bus bar and capacitor bank tap voltages, are employed to link the VZ and VY channels of the SEL487V protection relay. Using GPS signals from SEL satellite clock SEL 2488, the two CMCs are synced in the RelaySimTest program. RelaySimTest simulates capacitor element failures scenario by closing the circuit breaker across the bank element/s, causing an impedance shift and thus influencing voltage. For a shunt capacitor bank with three logical nodes defined, i) A87PDIF1 (alarm mode) and ii) T87PDIF1 (trip mode), iii) H87PDIF1 (high set), the IEC 61850 GOOSE messaging application is explored. The A87PDIF1 Logical Node is further divided into two Logical Nodes for fault location identification, i) AA87PDIF1 for faults above the tap and ii) BA87PDIF1 for faults below the tap and these are monitored per phase.

The lab-scale simulation results are analysed and proved that the protection schemes implemented using the system-based testing methods prove to be very useful for testing steady state and transient conditions. The system-based testing of the protection scheme and its simulation results are close as possible to real life conditions at site.

IED Scout is used to analyse the IEC 61850 GOOSE simulation results. For SCADA HMI applications, Manufacturing Message Specification (MMS) is also utilized to collect data from the protection relay utilizing Buffered Report Control Block (BRCB) and Unbuffered Report Control Block (URCB) subscribed by the substation gateway SEL 3555 RTAC device. SEL AcSELerator Diagram Builder software is used to develop the HMI which is loaded into the RTAC device for online viewing of alarms, events and measurements.

The research provides insight into shunt capacitor bank protection and the implementation of the IEC 61850 standard. The project outcomes assist industry specialists to better understand and implement voltage differential protection schemes for shunt capacitor banks while also introducing system-based testing methods to the industry, which provide advantages over conventional testing methods.

Key words: Capacitor Banks, Capacitor Bank Protection, IEC 61850, Reactive Power Compensation, Voltage Differential Protection, Current Unbalance Protection, System-based Testing.

1. CHAPTER ONE: INTRODUCTION

1.1 Introduction

Electric power utilities are experiencing losses in their power system network. There are power losses on the network due to the nature of the network, device design tolerances, and distances between sources and loads. These power losses are caused by voltage drops, low power factor, higher reactive power, and poor voltage regulation on the network, which results in electric power utilities being penalized for poor supply quality. The current literature review studied the answer to the problem and determined that strategically placing capacitor banks on the network would improve supply quality. The existing review of the literature focuses on the best location of capacitor banks. The inquiry of the placement of capacitor banks on primary distribution feeders began in the mid-1950s (Du et al, 2012). The installation of capacitor banks on distribution networks improves voltage regulation, reduces power loss, compensates for reactive power, and corrects power factor, most of which minimizes operating costs.

Because of the benefits indicated, capacitor banks have become key components of the power system network, and as such, they must be adequately secured against faults within the bank that might cause damage as a whole and/or the bank, as well as against system faults. There are two types of capacitor bank installations: series connected and parallel or shunt connected. Series capacitors are commonly used to increase network stability in circuits with high X/R ratio and long transmission lines. These series-connected capacitor banks require more sophisticated protection than the shunt capacitor banks. The study focuses on shunt capacitor bank protection techniques.

The research analyzes the usage of shunt capacitor banks, their protection and settings calculations, protection settings testing using the most recent available tools, IEC 61850 standard implementation, and so on. A lab test bench configuration is constructed for a protection simulation investigation. The lab-scale configuration includes a SEL-487V protection relay, a SEL RTAC gateway, OMICRON CMC 256 plus and CMC 356 units, network switches, and full engineering configuration software tools. The next section provides information about the problem being investigated.

1.2 Awareness of the problem

On power system networks, capacitor banks play a critical role in power quality and the safety of sensitive client equipment connected to the network. There are various shunt capacitor bank topologies and connections. These are classified according to whether they are start connected or delta connected, grounded or ungrounded, directly grounded or capacitively grounded. The listed configurations can be combined in a variety of ways. According to Brunelo et al. (2003), there are four types of capacitor banks, which are discussed next.

A) Externally fused where individual fuse that is externally mounted between the capacitor unit and the capacitor bus.
B) Internally fused with each capacitor element having its own fuse.
C) Fuseless with similar configuration as externally fused but with no fuses with series and parallel connected groups.
D) Unfussed series connected units usually applied in voltage networks less than 34.5 kV.

Fuseless capacitor banks are investigated further in the thesis since they are (1) less expensive than both fused options and (2) take up less room because they are more compact than both fused options. The unfussed option is typically utilized in distribution systems with voltages less than 34.5 kV, hence it was not chosen for the thesis because the network under consideration has a voltage of 144.9 kV. The degree of intricacy of the protection methods is determined by the type of capacitor bank employed and the bank connection used. Regardless of the bank configuration or type of bank utilized, the capacitor bank must be effectively safeguarded from system and bank faults that may cause harm, as well as system faults caused by the bank. Bank protection for faults within the capacitor bank and system protection for problems outside the bank installation are the two types of shunt capacitor bank protection. According to IEEE Guide for the Protection of Shunt Capacitor Banks, IEEE Std C37.99™, the following are some of the protection techniques used to protect shunt capacitor banks against system stress or failures.

I) External Arching
II) Over/undervoltage
III) Overcurrent

For testing reasons, the research only covers over/undervoltage and overcurrent protection. The IEEE Guide for the Protection of Shunt Capacitor Banks, IEEE Std C37.99-2012 included some bank protection strategies based on imbalance protection approach, which are listed.

i) Phase voltage differential
ii) Neutral voltage differential
iii) Phase current unbalance
iv) Neutral current unbalance

The study only focuses at phase voltage differential protection. Faster communication networks were necessary with the introduction of microprocessor-based relays that replaced electromechanical relays. These microprocessor-based relays included communications modules that allowed them to share data using protocols such as RS232, RS483, and others. Further advancements were achieved, and IEC TC57 was created. IEC 61850 standard was established to meet protection, control, monitoring, recording, and other requirements (Apostolov 2006). According to Adamiak and Mackiewicz (2009), the standard was created by IEC TC57 Working Groups 10, 11, and 12 on the basis of Utility Communications Architecture (UCA). Apostolov (2006) also described the IEC 61850 standard's several communication types, including client-server, peer-to-peer, unicast, and multicast. Skendzic and Gumza (2006) discussed the need for real-time Ethernet solutions to meet the communications requirements of the IEC 61850 standard's following real-time applications: Generic Substation State Event (GSSE), Generic Object Oriented Station Event (GOOSE), and IEC 61850 Part 9 - 1 and 2 for sampled analog values over serial unidirectional point to point links and sampled analog values over VLAN/priority-tagged Ethernet networks, respectively.

The study work examines various logical nodes applicable to capacitor bank protection utilizing the selected protection methodology, which are discussed in the implementation part.

1.3 Problem statement

Capacitor banks are a vital component of a power system network and, as such, require intelligent, fast, and dependable protection from internal and external failures. It is also assumed that the capacitor bank would always be available when the system requires it. As a result, a dependable, speedy, and intelligent protection system that would generate alerts for notice of individual element failures within the bank and isolate the bank when operating limitations were exceeded is requirements.

Problem statement: To solve the voltage stress and reactive power compensation problem on the power system network using shunt capacitor banks, and to repair the capacitor bank before catastrophic failures, the project introduced a rapid and reliable voltage differential protection solution based on the IEC 61850 standard-based GOOSE messaging application.

1.4 Research aim and objectives

1.4.1 Aim:

To create a quick and dependable protection mechanism for shunt capacitor banks, as well as to provide voltage regulation and reactive power assistance to the power system. The lab-scale test bench is built, protection configuration settings are built, and the IEC 61850 GOOSE message application-based voltage differential protection scheme for shunt capacitor banks is tested and analysed.

1.4.2 **Objectives**:

1. To conduct a literature review on various capacitor bank protection strategies, as well as to implement the IEC 61850 standard and system-based testing methodology.
2. To create a capacitor bank protection system-based on the IEC 61850 standard.
3. To build a simulation of a power system network using software such as DIGSILENT Power Factory and RelaySimTest.
4. To setup and test primary and backup protection configuration options for shunt capacitor banks.

5. To build a lab scale test bench utilizing SEL-487V relays, SEL RTACs, network switches, and other components.
6. To carry out a system-based simulation research with thoroughly considered test scenarios.
7. Analyze and compare simulation results to a standard benchmark model.

1.5 Motivation for research project

The crucial nature of capacitor banks in power system networks, as well as the necessity for intelligent, fast, and reliable protection needs, motivated the research. As power systems and communications networks improve the protective approaches. To explore the implementation of the IEC 61850 standard on capacitor bank protection and develop a system-based testing method for lab scale implementation. The sole constraint is the simulation accuracies. This method of testing simulates a real-life situation in which the device is utilized on a proficient network.

1.6 Hypothesis

The developed approach for capacitor bank protection based on the IEC 61850 standard and an automated system-based testing methodology, is explored and executed on a lab scale environment, with simulation results analysed.

1.7 Delimitation of research

The developed approach for capacitor bank protection is applied on a lab scale level using the IEC 61850 standard and an automated system-based testing methodology. The research focuses on imbalance protection methods, specifically phase voltage differential. For comparison purposes, this thesis presents a number of capacitor bank protection methods at a greater extent. The following are the factors that will be taken into account during the research:

1. Protection method for phase voltage differentials.
2. Protection against overcurrent and undervoltage.
3. RelaySimTest was used to perform system-based testing.
4. 66 kV, 144.9 kV, and 33 kV are the voltage levels in the network system.

5. The IEC 61850 standard specifies how to use GOOSE and MMS applications for SCBs.
6. DIGSILENT software used for fault study simulation work.
7. The Capacitor Bank Assistant software in SEL quickset is limited to tap voltage of 10 kV while the reactive voltage is 0.999 MVar.
8. The project utilized centre tapped capacitor bank configuration.

1.8 Assumptions

In order to address the research challenge, certain assumptions had to be made, which are given next.

1. The steady state and transient state conditions are both taken into account.
2. The simulation tools create a situation that is as close to real life as feasible.
3. The mathematical models and calculations used are as accurate as feasible.
4. The hardware utilized is entirely compatible with the IEC 61850 standard and its implementation.
5. Hardwired signals are slower than IEC 61850 GOOSE communications.

1.9 Research design and methodology

The goal of this study is to use the GOOSE messaging application and system-based testing methods to construct a capacitor bank protection mechanism based on the IEC 61850 standard. In order to ensure that the research's goal is realized, the following procedures were used.

1.9.1 Literature review

A review of existing publications is conducted to assess relevant applications, benefits and drawbacks, desired changes, and general comparisons. These papers will be assessed against a set of criteria in order to make comparisons and draw conclusions.

1.9.2 Unbalance protection scheme

Unbalance prevention, specifically phase voltage differential protection, is chosen among the many capacitor bank protection techniques available. The SEL-487V protection relay, CMC test injection devices, and OMIRCON RelaySimTest software are used to further investigate this technique in a lab-scale implementation environment.

1.9.3 Simulation study

The DIGSILENT Power Factory and RelaylSimTest software packages are used to simulate the power system network under investigation. Power Factory simulation studies are used to assess steady state conditions and to create and test overcurrent and over/undervoltage protection for capacitor banks. For system-based testing, the same network is emulated using the RelaySimTest software package.

1.9.4 Lab-scale implementation

The developed capacitor bank protection method is implemented and evaluated in a laboratory environment, as shown in Figure 1.1. A LAN with an Internet Protocol (IP) address range of 192.168.1.0/24 has been established, with all devices as shown in the diagram being assigned an IP address in this range. On the engineering computer, the power system network is simulated using the RelaySimTest software package. A Global Positioning System (GPS) clock server is used to keep track of all hardware and software, ensuring that everything is in sync. CMC injection test sets are used to inject the measurements (bus bar and capacitor bank tap voltages) seen on the simulated network into the protection relay. Depending on the protection settings, the protection relay will either continue to operate normally, send an alarm to SCADA, or send a trip signal. The IEC 61850 standard is used to communicate, namely Generic Object Oriented Substation Event (GOOSE) communication and Manufacturing Message Specification communication (MMS). The SEL AcSELerator Diagram Builder program is used to create a Human Machine Interface (HMI) for monitoring the capacitor bank protection system and viewing alerts and events provided by the protection relay.

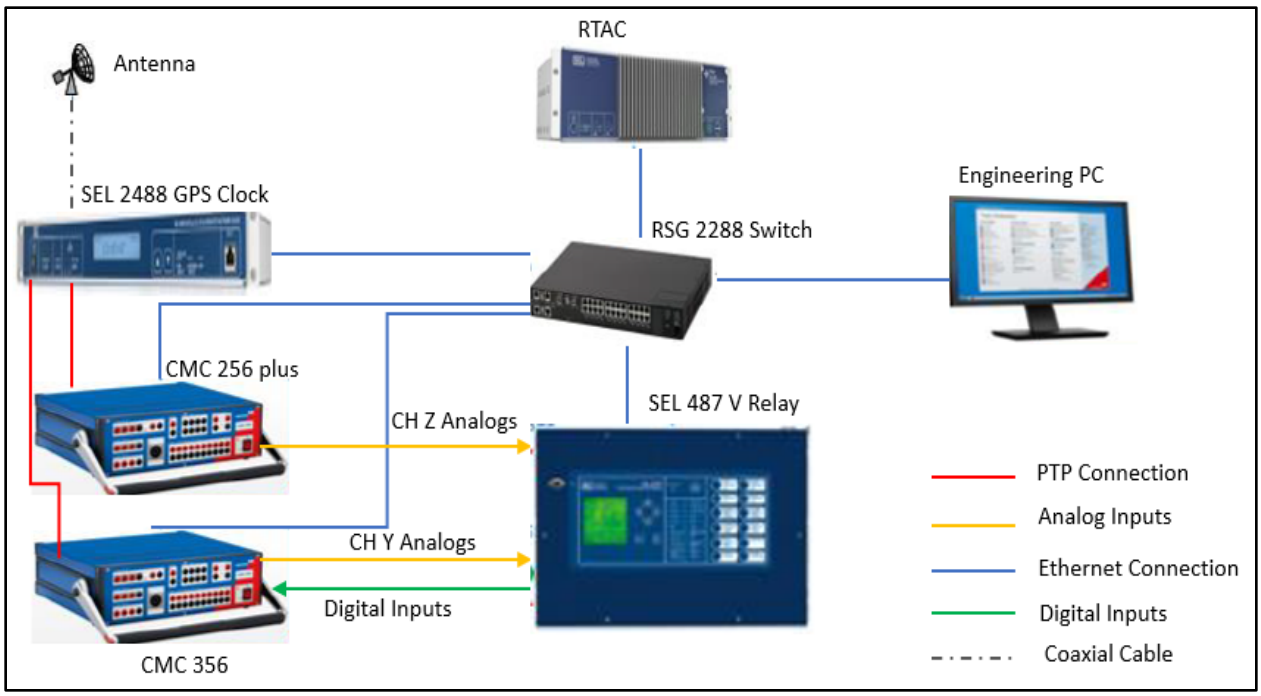

Figure 1.1. Lab-scale implementation

1.9.5 Data analysis

The data collected from all the processes followed during the research work is compared and analysed in order to draw conclusions and provide direction for future work.

1.10 Thesis chapters

The thesis is divided into seven chapters and four appendices.

1.10.1 Chapter one

The chapter begins with an overview of the research goal, objectives, motivation, delimitation, assumptions, and research methodology.

1.10.2 Chapter two

The background theory for reactive power compensation techniques, the IEC 61850 standard, and system-based testing methods are covered in this chapter. Review of

capacitor bank protection literature, implementation of the IEC 61850 standard for capacitor bank protection, and system-based testing procedures are also included.

1.10.3 Chapter three

The chapter details a simulation study that used DIGSILENT Power Factory to identify backup overcurrent protection settings for the shut capacitor banks, which included load flow and short-circuit tests. The simulation findings are analyzed and compared to earlier research.

1.10.4 Chapter four

The voltage differential primary protection scheme for shunt capacitor banks is discussed in this chapter, as well as the calculation technique for obtaining the voltage differential protection setting.

1.10.5 Chapter five

The lab scale implementation setup for both hardwired and software applications used in the research activity is described in this chapter.

1.10.6 Chapter six

This section of the thesis presents the results of the lab-scale setup implementation and simulation results.

1.10.7 Chapter seven

The chapter discusses the main protection, as well as coming to conclusions and identifying a need for further research.

1.10.8 Appendix A.1

The DIGSILENT simulation short circuit calculation process and simulation results are provided in the appendix A.1.

1.10.9 Appendix A.2

The appendix A.2 covers the fundamentals of capacitor bank theory calculations and how they are used to derive the capacitor element and capacitor unit impedances.

1.10.10 Appendix A.3

The calculation process for shunt capacitor bank voltage differential protection settings is provided in the appendix A.3.

1.10.11 Appendix A.4

The OMICRON RelaySimTest report for system-based testing technique is included in the appendix A.4.

1.10.11 Appendix A.5

The appendix provides some of SEL 487 V relay summary of commands.

1.10.12 Appendix A.6

The appendix provides group 1 settings of SEL 487V protection relay using commands as provided in appendix A.6.

1.11 Conclusion

The significance of shunt capacitor banks in the power system has been demonstrated, and as a result, the unit requires quick and reliable protection to assure the bank's availability. A process for calculating capacitor bank protection settings is described in the study effort, as well as a system-based testing methodology. The chapter begins with an overview of the research goal, objectives, motivation, delimitation, assumptions, and methods.

The following chapter discusses a literature study on capacitor bank protection, reactive power compensation with shunt capacitor banks, and a review on system-based testing.

2. CHAPTER TWO: LITERATURE REVIEW

2.1 Introduction

Shunt capacitor banks are critical components of the electrical power system because they offer reactive power to the network. The benefits of placing shunt capacitor banks in an electrical power system include improved voltage profiles, power factor correction, reduced electrical power losses, and improved line capacity factor. As a result, it is critical that such an important component of the network is protected using fast and dependable protection approaches. The chapter includes a study and review of IEEE standards and articles on capacitor bank protection theories and substation automation.

The chapter is divided into five sections, as seen in Figure 2.1. Section 2.1 is the chapter introduction, Section 2.2 is background theory, Section 2.3 is an overall literature search, and Section 2.4 provides summary of literature review, whereas Section 2.5 includes a discussion and conclusion.

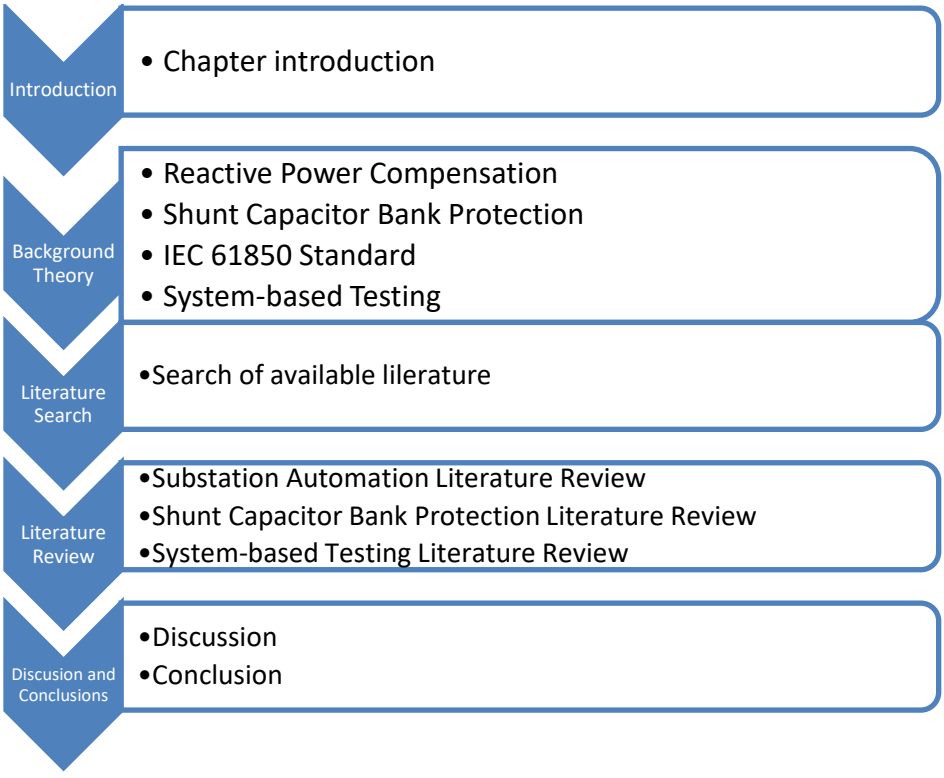

Figure 2.1. Chapter 2 flow diagram

The next section provides background theory to reactive power compensation techniques, namely shunt capacitor bank installation, as well as the IEC 61850 standard and system-based testing procedures.

2.2 Background theory

Heat dissipation on power line conductors and other electrical components, as well as other non-technical factors, cause power losses in electrical power systems. There are two types of power losses: technical and non-technical power losses. Technical power losses, also known as I^2R losses, are produced by heat dissipation on conductors, whereas non-technical power losses are caused by difficulties outside of the power system, such as electricity theft, non-payment, and so on. The study only looks at technical power losses. Different methods are in place to reduce technical power losses in electrical power systems. Power is transported over long distances at high voltages, which helps to reduce technical losses because there is less current flowing on the line due to the high voltage levels. Among the different loss reduction solutions available are network reconfiguration, network re-conductoring, distribution transformer position and sizing, automatic voltage booster, reactive power compensation, and aerial bunched cables (Kour and Sharma, 2013).

Figure 2.2 depicts a typical electrical power system network in which power is generated at low voltages ranging from 10kV to 33kV (Generation), these voltages are then stepped up to 765 kV where power can be transmitted over long distances (Transmission), and finally stepped down to voltage levels ranging from 66kV to customer levels as required (Distribution).

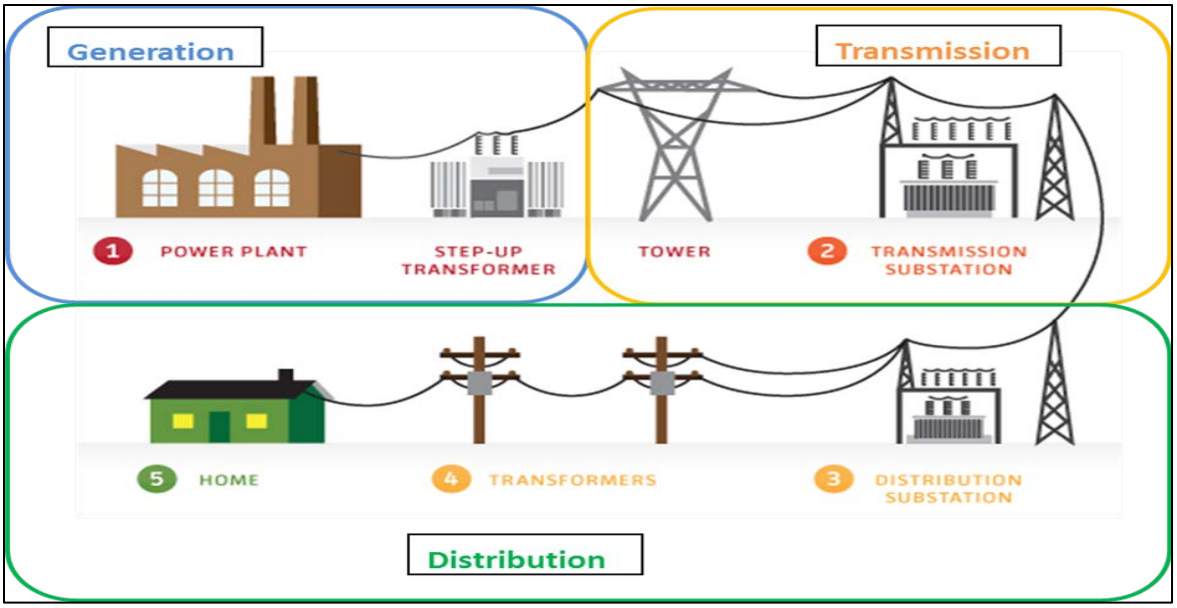

Figure 2.2. Typical electrical power system

The next section discusses reactive power compensation strategies, with a focus on shunt capacitor bank installation.

2.2.1 Reactive power compensation

Figure 2.3 shows Pudney's (2012) usage of a beer analogy to demonstrate the idea of reactive power on electrical power networks. The cup capacity reflects the system's kVA (apparent power), the froth represents kVar (reactive power), and the actual beer content represents kW (real/active power). Shunt and series capacitor banks, FACTS (Flexible and AC Transmission Systems), SVC (Static Var Compensators), STATCOMs (Static Synchronous Compensators), and other reactive power compensation systems are available. All of these strategies give the necessary reactive power to the system, which aids in the reduction of power system losses, the improvement of voltage profile, power factor correction, and the growth of system capacity.

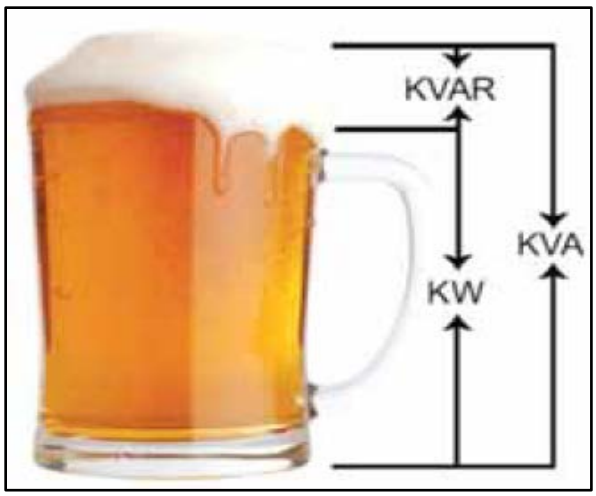

Figure 2.3. Beer analogy for reactive power (Pudney, 2012)

The analysis takes into account the installation of a shunt capacitor bank in the power system network. These units require fast and dependable protection to guarantee that they continue to offer the system with the benefits it requires while also supplying a consistent supply. The next section discusses capacitor bank protection strategy.

2.2.2 Shunt capacitor bank protection philosophies

As stated in the preceding subsection, humans must be safeguarded from injury, and the equipment placed must be protected from damage, while quality and continuity of supply must be maintained. The capacitor bank protection concept takes into account two scenarios: power system protection and capacitor bank protection. The study focuses primarily on the latter. For shunt capacitor banks, several protection theories such as voltage differential, current unbalance, overcurrent, and so on are employed. The study only looks at voltage differential and current unbalance protection strategies. Table 2.1, drawn from IEEE standard C37.99-2000, shows the circumstances that are safeguarded against within the capacitor bank using a protective philosophy known as bank protection.

Table 2.1. Capacitor bank protection, IEEE standard C37.99-2012

Bank protection		
Condition	**Type of protection**	**Remarks**
Faulted capacitor element.	External or internal fuse for fused banks; weld, which occurs at the failure, for banks without fuses.	Fuses should be fast to coordinate with fast unbalance relay settings, but should not operate during switching or external faults.
Fault from capacitor elements to case, bushing failure, faulty connection in capacitor unit.	Fuse for externally fused capacitor; unbalance protection for internally fused banks or banks without fuses.	For externally fused capacitor banks, fuses should be fast to coordinate with fast unbalance relay settings, but should not operate during switching or external faults. For internally fused banks or banks without fuses, the unbalance protection should be fast to avoid case rupture, but should not operate during switching or external faults.
Fault in capacitor bank other than in unit (arcing fault in bank).	Unbalance protection. Relay should have a band-pass filter for the fundamental current or voltage for security.	Unbalance protection should be fast to minimize damage to other units during a major fault. See 7.1.4.
Continuous overvoltage on capacitor elements or units due to faulted elements or fuse operations within the bank.	Unbalance protection. Relay should have a band-pass filter for the fundamental current or voltage for security.	Bank should be tripped for voltages > 110% of rated voltage or as recommended by manufacturer on healthy capacitor units. An alarm may be added for 5% unbalance or one unit out. (In some critical applications an alarm with delayed tripping above 110% of rated voltage is used; see 7.1.4.)
Rack-to-rack flashover in two series group phase-over-phase single wye banks.	Phase overcurrent or negative sequence relay; unbalance current for wye-wye capacitor banks.	Fast operation is required to minimize damage. See 7.1.4 and 7.1.5.

The sections referred to in the Table, 7.1.4 and 7.1.5 discuss about capacitor unbalance protection which is the main protection and protection against rack faults. IEEE Guide for the Protection of Shunt Capacitor Banks, IEEE standard C37.99-2000, lists four types of shunt capacitor bank connections that influence the choice of protection system to be utilized, as follows:

a) Each capacitor unit is individually fused and externally fused.
b) Internally fused means that each element is fused within the capacitor unit.
c) Fuseless, using capacitor units linked in series strings between the line and neutral (or between line terminals).
d) Unfussed using capacitor units coupled in a variety of series and parallel configurations.

As previously indicated, the research is limited to fuseless capacitor banks. Figure 2.4 from IEEE standard C37.99-2000 depicts various forms of capacitor bank connections. The standard defines the following drawings: a) Delta, b) Grounded wye, c) Ungrounded wye, d) Ungrounded double wye (neutrals may or may not be tied), and e) Grounded double wye. Delta linked capacitor banks are typically found on distribution systems and are made up of a single series set of capacitors rated at line to line voltage. Grounded wye capacitor banks are made up of groups of series and parallel linked capacitor units that provide lightning surges with a low impedance path to ground. Zero-sequence currents and third harmonic currents are not permitted in unground wye capacitor banks. However, the study only looks at the Grounded wye topology.

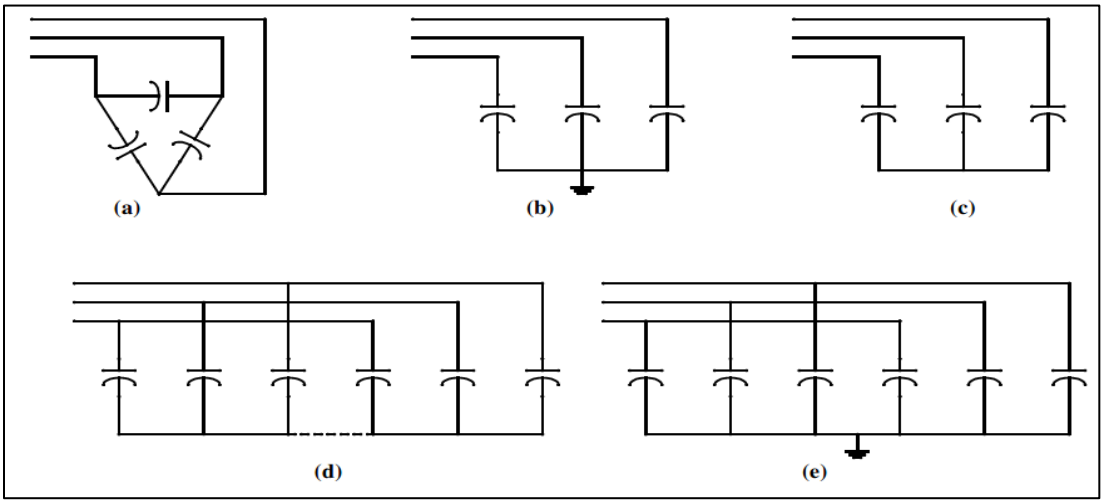

Figure 2.4. Various types of capacitor bank connections, IEEE standard C37.99-2000

The following are some of the constraints that should not be exceeded while guaranteeing continued operation during system contingency, as specified by IEEE standard C37.99-2000:

a) rated terminal root-mean-square (rms) voltage of 110 percent
b) 100-110 percent rated reactive power at rated sinusoidal voltage and frequency, and so on.

The protection scheme that is to be developed should ensure that the following limits are followed and should serve as the foundation of the protection logic. Voltage differential and current unbalance are covered in the sections that follow.

2.2.3 SCB protection using voltage differential scheme

The voltage differential protection (87V) principle compares the voltages on the bus bar and at the tap point. To account for any intolerances, a compensation factor is utilized. The protection mechanism works for both grounded and ungrounded capacitor banks. Figures 2.5 and 2.6 from the SEL487V instruction manual depict a typical use of voltage differential protection for grounded and ungrounded capacitor banks.

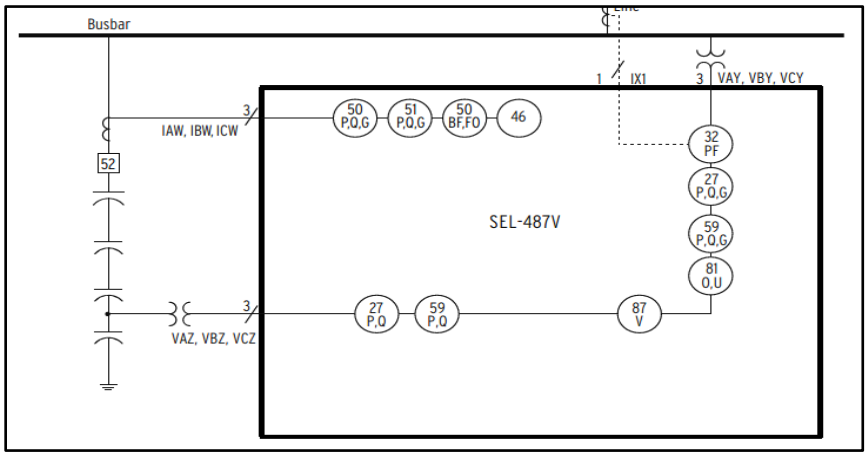

Figure 2.5. A typical application of phase voltage differential protection, SEL-487V Relay Instruction Manual

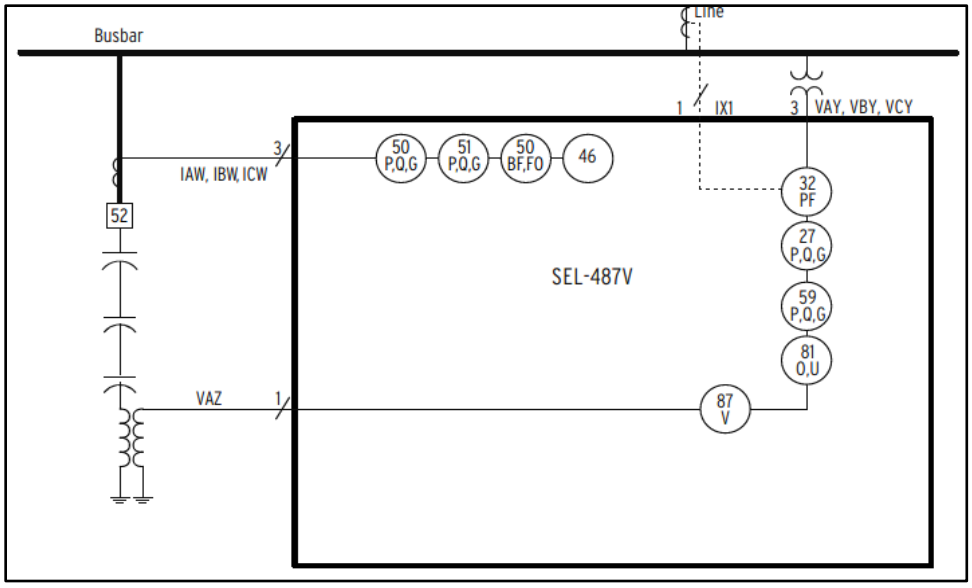

Figure 2.6. A typical application of neutral voltage differential protection, SEL-487V Relay Instruction Manual

Figure 2.5 depicts a phase differential voltage protection (87 V) scheme in which bus bar voltage is compared to tap voltage. Voltage channel Y represents bus bar voltage, while voltage channel Z represents capacitor bank tap voltage, as illustrated in the diagram. There are two current channels as well: X for bus bar currents and W for capacitor bank currents. Figure 2.6 depicts a neutral voltage differential protection technique in which the bus bar voltage is compared to the neutral voltage measured at the capacitor bank neutral connection. Other backup protection schemes shown in the typical drawings include definite time overcurrent (50/P/Q/G) for phase, negative sequence, and zero-sequence faults, inverse time overcurrent (50/P/Q/G) for phase, negative sequence, and zero-sequence faults, under voltage (27/P/Q/G), over voltage (59/P/Q/G), and so on. The following section discusses current imbalance protection systems.

2.2.4 SCB protection using current unbalance scheme

Current imbalance protection, similar to voltage differential protection, use comparative philosophy by comparing currents originating from each side of the capacitor bank at the neutral point. The protection method generally protects against arcing faults inside the capacitor bank and detects changes caused by a capacitor element or unit failure. Current unbalance protection can be performed in two ways: neutral current unbalance (60N) and phase current unbalance (60P), and it can be used on both grounded and ungrounded capacitor banks. Figures 2.7 and 2.8, courtesy of the SEL487V instruction manual, depict common applications for phase current unbalance and neutral current unbalance protection methods. Backup protection schemes such as definite time overcurrent (50/P/Q/G) for phase, negative sequence, and zero-sequence faults, inverse time overcurrent (50/P/Q/G) for phase, negative sequence, and zero-sequence faults, under voltage (27/P/Q/G), over voltage (59/P/Q/G), and so on are shown in the typical drawings.

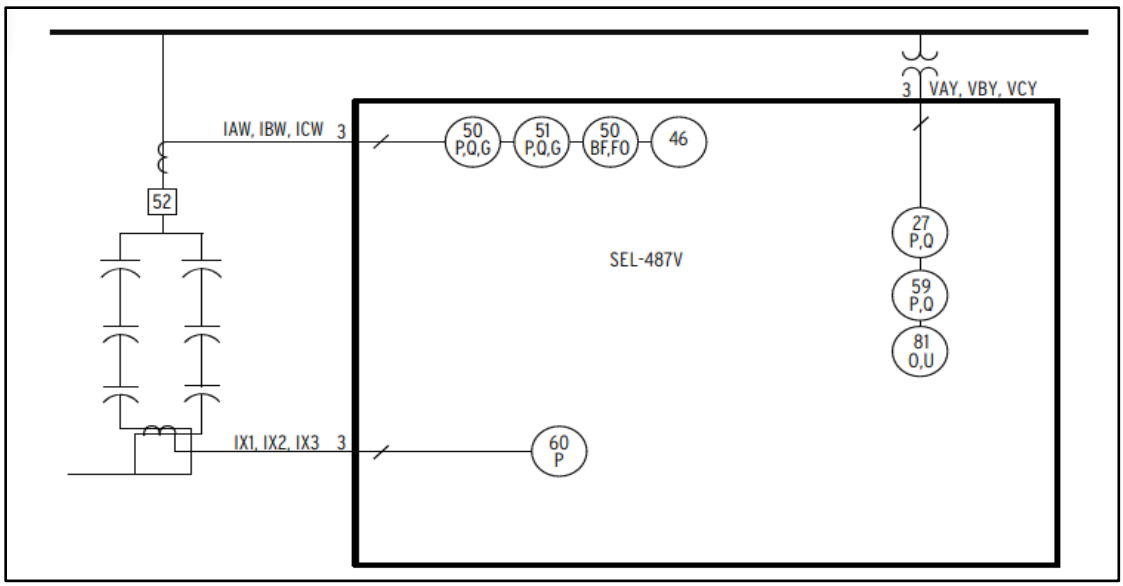

Figure 2.7. A typical application of phase current unbalance protection, SEL-487V Relay Instruction Manual

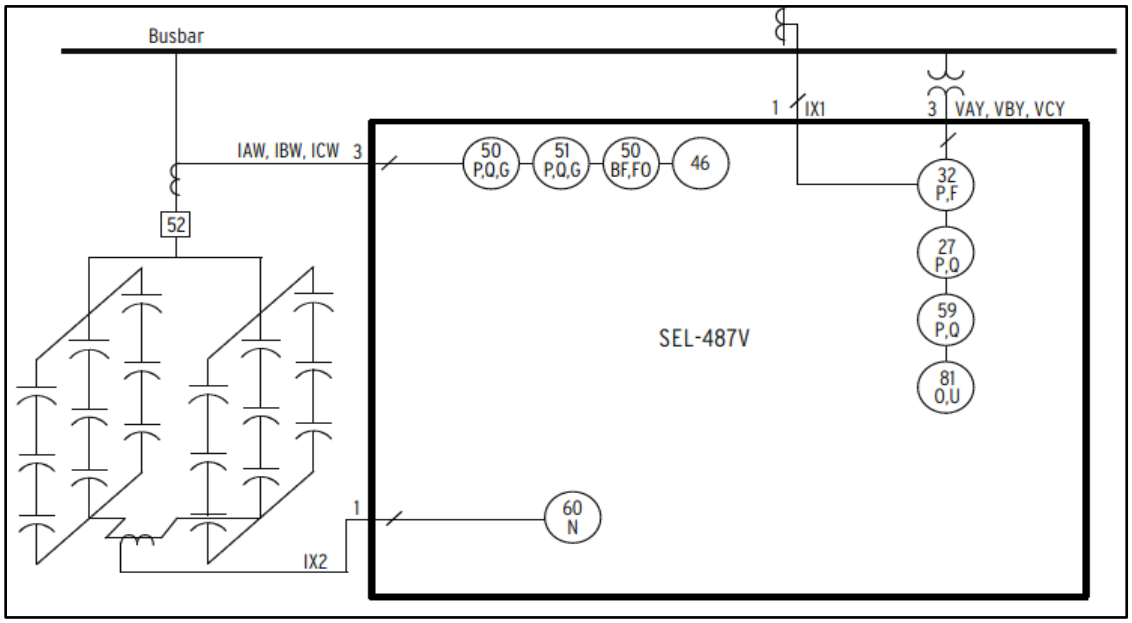

Figure 2.8. A typical application of neutral current unbalance protection, SEL-487V Relay Instruction Manual

In keeping with current substation design techniques, the next subsection examines substation automation and how it is/can be implemented for shunt capacitor banks. The following section gives background on the IEC 61850 standard and its evolution.

2.2.5 IEC 61850 communication standard

The IEC 61850 standard was created to improve communication and lower the cost of substation wiring. Figure 2.9 depicts the progression of substation designs from the formerly hardwired, signal-by-signal, to the protection devices displayed in the far-left frame to the contemporary designs of Ethernet-based substations, also known as digital substations, shown on the far right. The majority of the work and expense came from hardwiring signals from the protection devices to the control room. The more recent substations have been digitalized, with communication interfaces placed in the HV yard and fiber optic cables flowing to the control center.

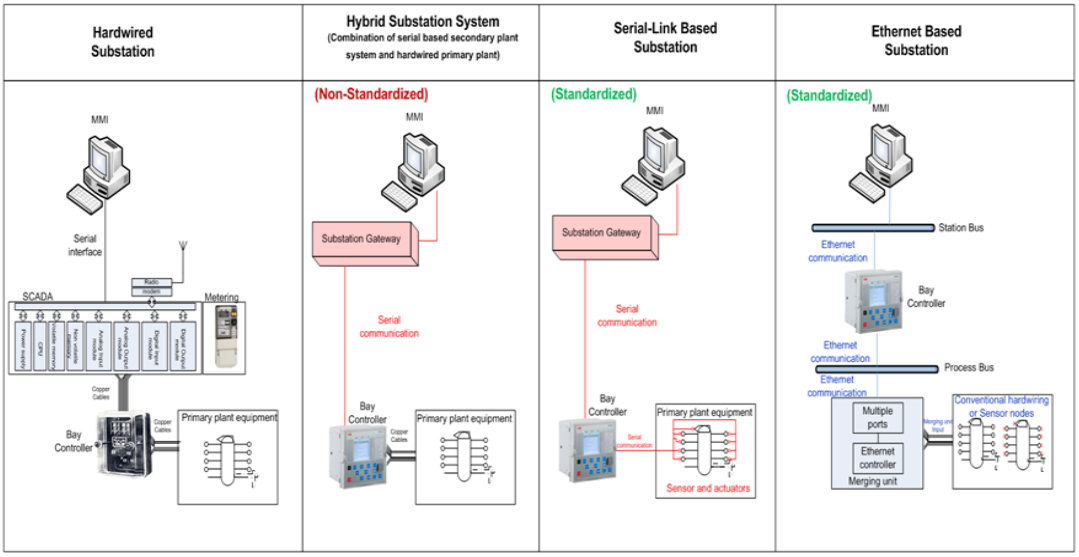

Figure 2.9. Substation migration design

These hardwired substations still exist today, however refurbishment operations are being undertaken to try to modernize them where possible. The following are some of the drawbacks of having these substations:

- There is no addressability: the separate feeds are hardwired, with labels at either end of the cable serving as the only form of addressing.
- There is no data connection among the feeds.
- The majority of the expense for setting up such a system is invested in cable and personnel expenditures.

- The system is difficult to scale.
- There is no substation automation: the system is hardwired, and communication between devices at the same level in the hierarchy is not possible.

In the 1990s, microprocessor-based relays were developed to replace electromechanical relays. These relays had communication modules that allowed them to share information using point-to-point communication protocols such as RS232, RS485, and so on, as illustrated in Figure 2.9, second frame from the left (Hybrid substations). One problem of this method was that it was not standardized, thus suppliers devised solutions that only worked with their devices. The progress of communications continued, and serial-based communications were developed. The solution is depicted in Figure 2.9, frame 3. The following are some of the drawbacks of this solution:

- Speed limitation: the maximum speed on an RS232 link is ±14.5kbps
- Costs: RS485/RS422 to RS232 converters are often required.
- Restricted in terms of scalability
- Only physical layer standard specified
- Data communication is not standardized
- Only Unicast (Point to point) measurement communication
- No interface to conventional transformers defined.

With these drawbacks in mind, the research for better alternatives persisted. This resulted in the creation of Ethernet-based substation communications systems. The IEC 61850 standard was created with the primary goal of standardization in order to enable interoperability amongst intelligent electronic devices (IEDs) offered by various vendors.

The standard is divided into different parts as shown.

- Part 1: Introduction and overview
- Part 2: Glossary
- Part 3: General requirements
- Part 4: System and project management
- Part 5: Communication requirements for functions and device models
- Part 6: Configuration description language for communication in electrical substations related to IEDs

- Part 7-1: Basic communication structure for substation and feeder equipment – Principles and models
- Part 7-2: Basic communication structure for substation and feeder equipment – Abstract Communication Service Interface (ACSI)
- Part 7-3: Basic communication structure for substation and feeder equipment – Common data classes
- Part 7-4: Basic communication structure for substation and feeder equipment – Compatible logical node classes and data classes
- Part 8-1: Specific Communication Service Mapping (SCSM) – Mappings to MMS (ISO/IEC 9506-1 and ISO/IEC 9506-2) and to ISO/IEC 8802-3
- Part 9-1: Specific Communication Service Mapping (SCSM) – Sampled values over serial unidirectional multidrop point to point link
- Part 9-2: Specific Communication Service Mapping (SCSM) – Sampled values over ISO/IEC 8802-3
- Part 10: Conformance testing

The IEC 61850 standard specifies logical interfaces between the various components of a substation automation system as shown in Figure 2.10. These interfaces are described next:

- IF1: protection-data exchange between bay and station level.
- IF2: protection-data exchange between bay level and remote protection
- IF3: data exchange within bay level.
- IF4: CT and VT instantaneous data exchange (especially samples) between process and bay level.
- IF5: control-data exchange between process and bay level.
- IF6: control-data exchange between bay and station level.
- IF7: data exchange between substation (level) and a remote engineer's workplace.
- IF8: direct data exchange between the bays especially for fast functions such as interlocking.
- IF9: data exchange within station level.
- IF10: control-data exchange between substation (devices) and a remote control center

The standard defines three levels as shown Figure 2.10,

- Station Level
- Bay/Unit Level
- Process Level

The substation automation components at the same level or at different levels of the hierarchy are then linked together by the various interfaces.

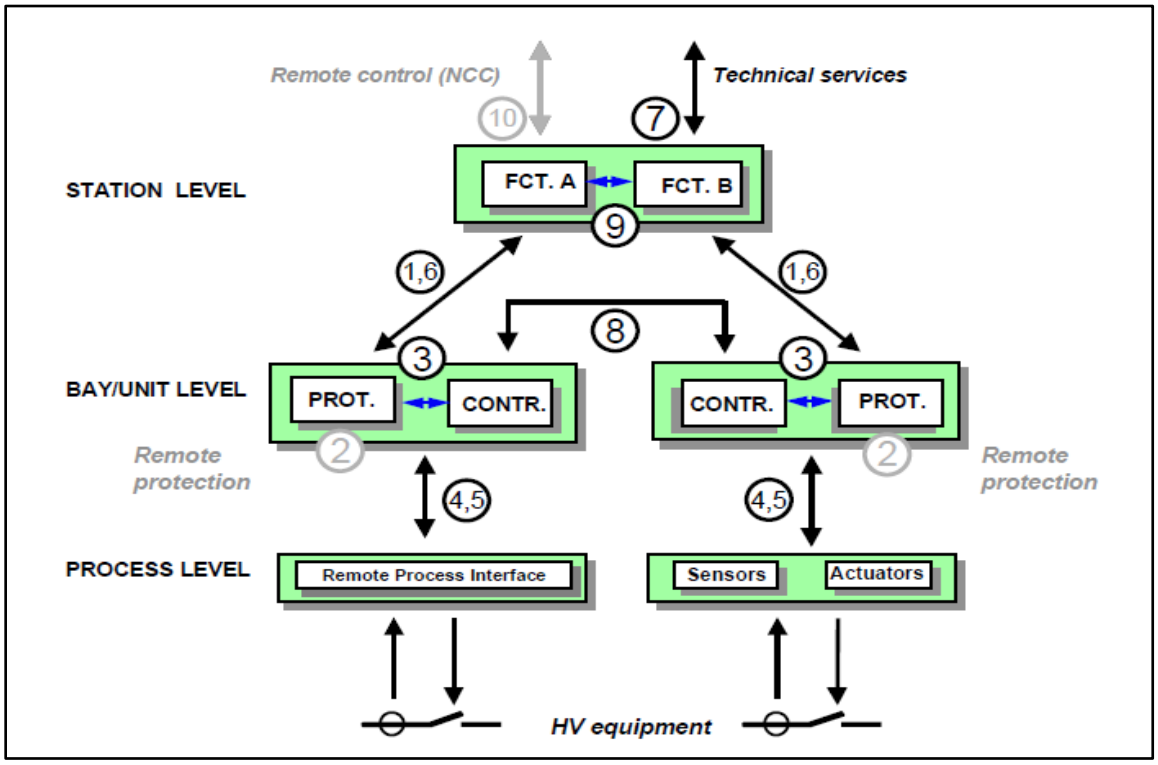

Figure 2.10. Interface model of a substation automation system

The station level, also known as the "station bus," connects all of the IEDs to one another as well as to the human machine interface (HMI) via interfaces 1, 3, 6, 7, and 8. In a client/server architecture, the IEDs connect with the Station level devices via the messaging services offered by the Manufacture Message Specification (MMS) protocol. The publisher/subscriber communication services are used for inter-IED communication on interface 3. Interfaces 4 and 5 connect process-level or "process bus" equipment to Bay-level equipment and vice versa. Through publisher/subscriber communication

services, the process level transmits raw power system information from switchyard source devices to the Bay Level.

Figure 2.11 depicts how the IEC 61850 standard is mapped to the Manufacturing Message Specification in terms of message types, as detailed in IEC 61850 part 8-1 of the standard. The message types are as follows: Type 1 for fast messages, Type 1A for Trips, Type 2 for medium speed messages, Type 3 for low speed messages, Type 4 for raw data messages, Type 5 for file transfer functions, and Type 6 for time synchronization messages as stated in the standard. GOOSE employs Type 1 and 1A messages, as indicated in the screenshot, whereas Client/Server mappings for MMS use Type 2, 3, and 5 messages.

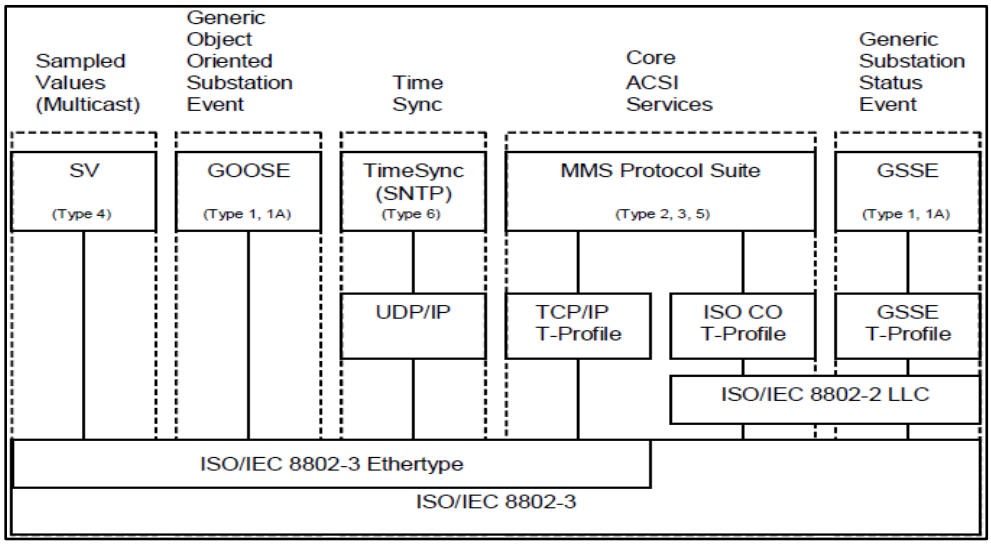

Figure 2.11. IEC 61850 standard mappings to MMS

The following section discusses the history of system-based testing methods as well as the benefits of utilizing them over traditional testing methods.

2.2.6 System-based testing

Injection test sets with system steady state are used in traditional techniques of testing protective relays. According to Skrbinjek and Cialla (2015), traditional techniques of testing single relays yield restricted results in terms of functionality, stability, and safety. Traditional methods of testing distributed systems required at least one staff member for each end station to synchronize by communicating over the phone. Because only steady

state testing is undertaken, this type of testing did not give accurate results. These constraints demanded the development of enhanced testing methods as well as the provision for future power system requirements. For this purpose, system-based testing was created.

OMICRON created RelaySimTest software to meet this demand and provide the flexibility of testing distributed systems in both steady and transient modes. Each device to be tested must be linked to the injection test set, and the test sets must be time synchronized through GPS clock. System-based testing provides for the testing of the entire system or a component of the system for steady-state and transient conditions, as well as the analysis of the impact fault conditions encountered by one device have on the rest of the network's devices. RelaySimTest enables the creation of automated test scenarios that are as near to a real-world situation as feasible.

Skrbinjek and Cialla's distributed system is seen in Figure 2.12 (2015). Five dispersed test stations make up the power system network. To guarantee that all devices are time synchronized, each station has a CMC injection test set and a GPS synchronizing device. All five devices are tested using a single computer that is linked to other CMC devices via the internet/communications media. The configuration enables testing of the entire system at the same time, with findings available quickly.

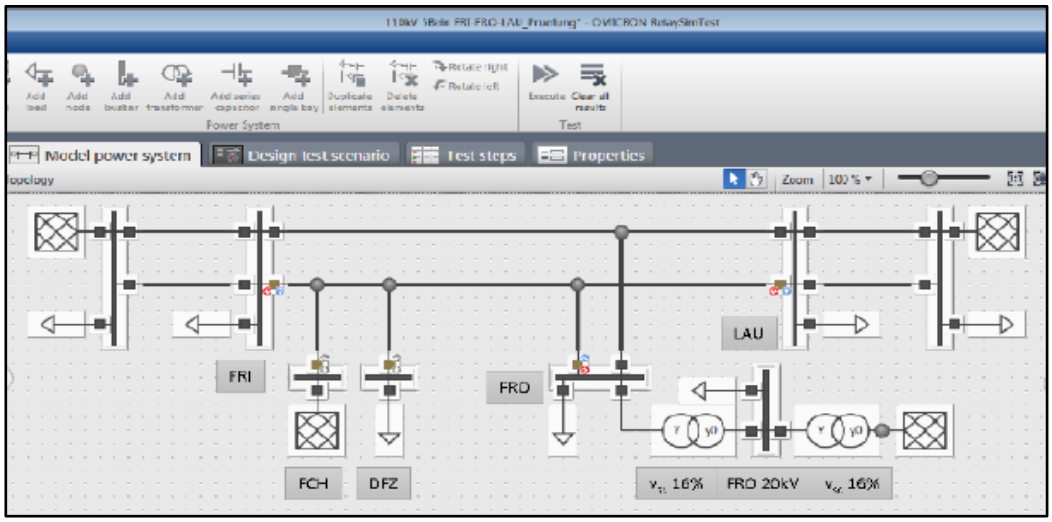

Figure 2.12. OMICRON RelaySimTest setup: Skrbinjek & Cialla (2015)

Different sorts of literature material, such as papers, journals, books, industry manuals, standards, and internet articles, were employed in the research, and these are detailed in the following section.

2.3 Literature search

To help with study on the capacitor bank protection challenge, existing literature was consulted. Figure 2.13 depicts a curve of 101 publications reviewed between 1978 and 2021. The papers were chosen for their contributions in the areas of reactive power compensation employing capacitor banks, capacitor bank protection strategies, substation automation development and implementation, and system-based testing.

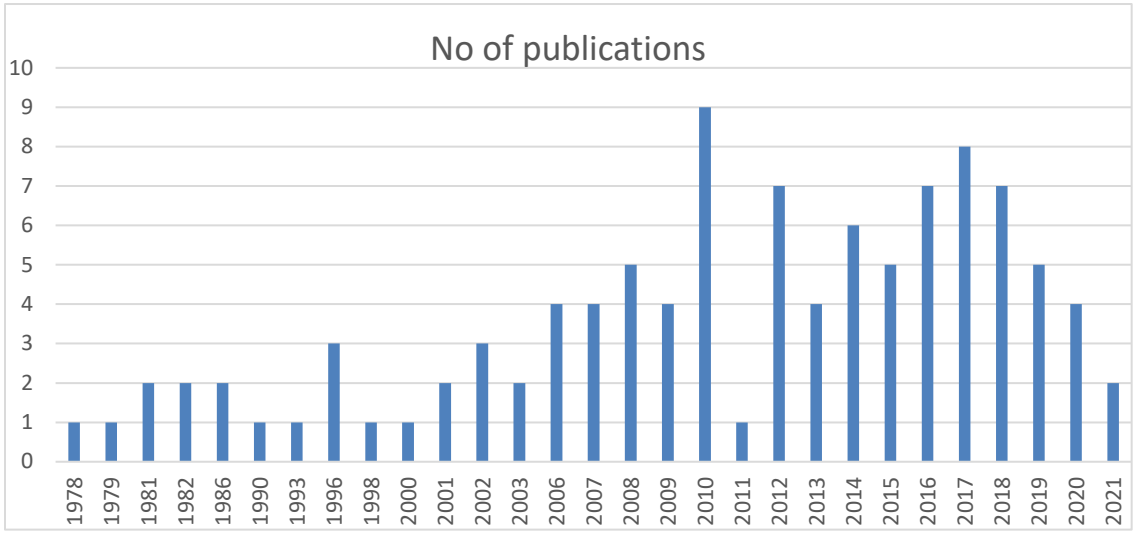

Figure 2.13. Number of publications per year

One hundred and one publications have been examined from 1978 to October 2021, as shown in the graph in Figure 2.13. During the literature search, the following key phrases were used: reactive power compensation, capacitor bank protection, substation automation, IEC 61850, capacitors, GOOSE communication, and so on. Based on these key terms, a broad review of the papers was conducted, with the review divided into three sections, as indicated next: i) Section 2.4 Substation Automation System (SAS), ii) 2.5 Capacitor Bank Protection (CBP), and iii) section 2.6 System-based Testing (SBT). Figure 2.14 shows the number of papers reviewed for each review category, with SAS having 12 publications, CBP having 17 while SBT having 10 publications and others 62 publications.

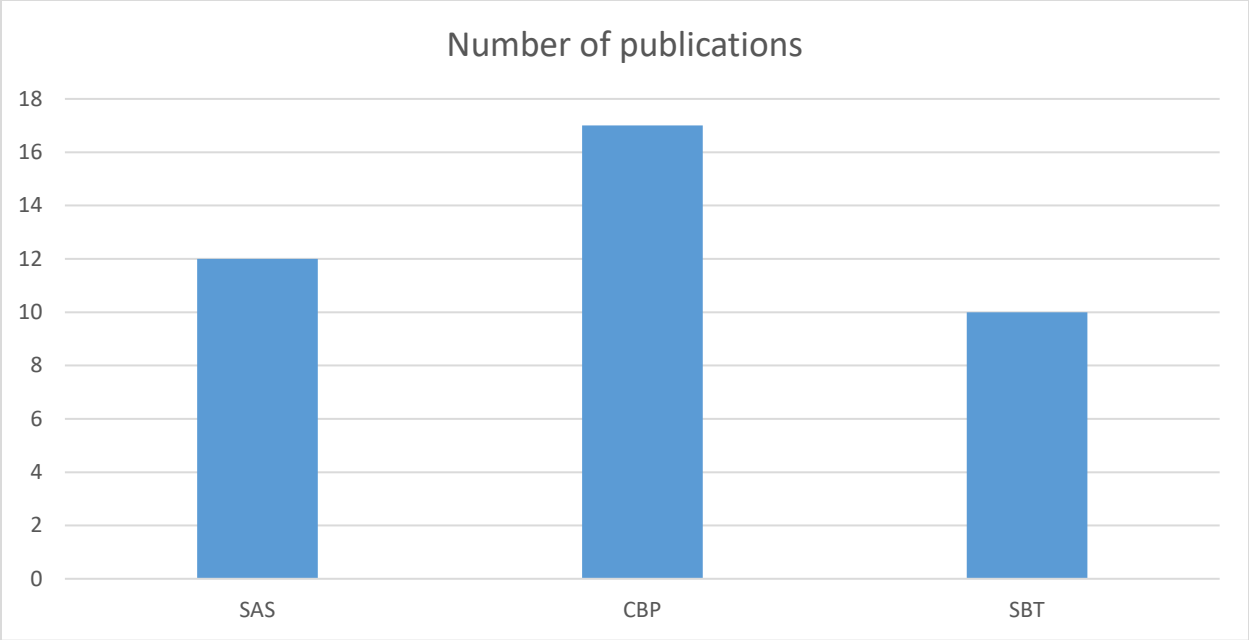

Figure 2.14. Number of publications reviewed in each review category

The section that follows describes the substation automation review and the impact these articles contributed to the study work.

2.4 Substation automation literature review

As stated in Table 2.2 a number of studies were assessed and compared using the aforementioned criteria. Apostolov (2006) published a study in which he explained the various communications and performance requirements of the IEC 61850 standard. The report went into great detail about numerous substation functions related to station, bay, and process levels as outlined by the standard. Skendzic and Gumza (2006) presented a paper on how real-time Ethernet can be used to improve substation automation. The article describes the influence of increased Ethernet communications on performance in terms of the standard's communication requirements, as well as presenting examples of implementations in important processes. Janssen and Apostolov (2008) discussed the various components of IEC 61850 communications networks and substation automation systems, as well as the impact on substation design and operation.

The paper also focuses on to cover the benefits of implementing the IEC 61850 standard, as well as how it influences new substation design and integration with existing traditional substations, including merging units. McGinn et al. (2009) examined the practical applications of the IEC 61850 standard, as well as the cost reductions associated with the use of less copper wires in substation designs. Part 9-2 of the standard was the subject of the report, with the usage of fiber optic cables replacing copper cable cabling from substation high voltage equipment to control buildings. Adamiak and Mackiewicz (2009) offered a high-level summary of the IEC 61850 standard. They also provided a brief history of how the standard was created, which was based on the Utility Communications Architecture (UCA) released in 1988. According to the authors, IECTC57 Working Groups 10, 11, and 12 used the UCA standard as the foundation for developing IEC 61850 Communication Networks and Systems in Substations.

Apostolov and Vandiver (2010) presented their work on distance protection methods, their functional hierarchy, and testing methodology. The article emphasized the usage of logical nodes for distance protection and the benefits of using the IEC 61850 standard in general. Ouellette et al. (2010) presented their work detailing how IEDs react to anomalous IEC 61850 communications and how these abnormal messages can be replicated using the Real Time Digital Simulator (RTDS).

Although different manufacturers interpret and implement the standard differently, the study effort helps end users understand the answer a certain device from a specific manufacturer provides. Apostolov (2010) discussed the IEC 61850 standard part 9-2 process bus and the implementation that guarantees compatibility between different vendor devices. Mohagheghi et al. (2011) presented work on the application of the Distribution Automation standard (DA). The authors demonstrated how the standard was used to tackle the problem of distribution automation, including Fault Detection, Isolation, and Restoration (FDIR), Feeder Reconfiguration, Volt/Var Optimization, Microgrid Management, Demand Response, and so on. Mascarella et al. (2015) examined a wind farm control strategy that employs a slow-active reactive power controller to regulate steady-state voltage and a fast-acting active power controller for an embedded energy storage system to reduce voltage flicker. The solution was evaluated utilizing RTDS for wind turbine and distribution feeder simulation, a digital controller for control loops, and IEC 61850 GOOSE messaging for communications.

Krishnamurthy and Baningobera (2019) presented their research on transformer deferential and overcurrent protection techniques based on IEC 61850 harmonic blocking. The authors examined and implemented the harmonic blocking function SEL487E relay during inrush currents, sending the block signal to the overcurrent backup relay (SEL751A) through GOOSE messaging to ensure it did not trip under these situations. Krishnamurthy et al. (2020) also reported research on capacitor bank safety based on the IEC 61850 standard. The capacitor bank protection philosophy used SEL487V relays and was tested with CMC 256 plus and OMICRON RelaySimTest software, which provided system-based testing. It has been discovered that using IEC 61850 GOOSE messaging instead of hardwired signals resulted in speedier communications.

The following part presents discussion points from the peer-reviewed published articles on substation automation systems.

2.4.1 Review discussion on substation automation

The IEC 61850 standard is always evolving and improving since its first creation and applications. A large number of researchers have conducted study on the various applications of the standard. Some of the topics covered are communications requirements, the impact of the standard on new substation design, the integration of new designs with traditional substation designs, the benefits of the standard's implementation, and so on. The standard's application in distribution automation systems, distance protection schemes, transformer differential protection schemes, overcurrent protection, harmonic blocking schemes, capacitor bank voltage differentials protection schemes, and other areas. Some of the research is done through discussion, while others are done through lab testing. All of the study work highlighted and demonstrated the benefits of using the IEC 61850 standard over traditional hardwired solutions, such as cost savings, interoperability between different vendor equipment, and so on.

The following section provides an overview of capacitor bank protection.

Table 2.2. Review summary on substation automation

SUBSTATION AUTOMATION				
Author	**Aim**	**Application**	**Hardware/Software used**	**Achievements**
Apostolov (2006).	The paper discussed different communications related to IEC 61850 standard and performance requirements of various substation functions.	General review and discussion of IEC61850 standard	Not Applicable	Clearly discussed communications and performance requirements of the standard
Skendzic & Gumza (2006).	The paper provides an overview of the Ethernet standards and investigates their impact on substation system automation and protection.	Review and discussion of real-time Ethernet and its usefulness and application in substation protection and control	Not Applicable	Clearly demonstrated the advantages and importance of reliable communications in substation protection and control environment with the use of examples
Janssen & Apostolov (2008).	The paper describes different components of IEC 61850 communication networks and substation automation systems affecting design and operation of the substations	Review and discussion the standard has on new designs and including interfacing with existing conventional substations	Not Applicable	Provides advantages of implementing IEC 61850 standard and how affects the design of new substations as well as interfacing with existing substations
McGinn, Adamiak & Goraj (2009).	A Practical IEC 61850 process bus based architecture which eliminates excessive use of copper cables is discussed in the paper	The application of IEC 61850 part 9-2 of the standard in order to replace copper wiring with fibre optic cables which results in cost reduction	Merging Units	Demonstrated that use of part 9-2 of the standard result into cost saving, improved safety, reliability, scalability, etc.
Adamiak, Baigent & Mackiewicz (2009).	The paper looks at the needs of next generation communication systems and provides an overview of the IEC	Not applicable	Not Applicable	The authors managed to provide an overview of the standard and the future direction of the IEC61850 technology

	61850 protocol and how it meets these needs.			
Apostolov & Vandiver (2010).	The paper discusses distance protection functionality and the hierarchy in the functionality and how these can be tested	Distance protection	Merging Units	Testing of distance protection functionality
Ouellette, Desjardine & Forsyth (2010).	The purpose of the paper is to show how IEC 61850 compliant IEDs react to abnormal IEC 61850 data and how to create these conditions using Real Time Digital Simulator (RTDS)	Testing different IED response to normal and abnormal messages	Real Time Digital Simulator	Testing the IEDs response to normal and abnormal states of the power systems utilizing application of the IEC 61850 GOOSE messages and RTDS interface
Apostolov, A. (2010).	The paper discusses the Process Bus as defined in IEC 61850 9-2 and the implementation that ensures interoperability between different vendor IEDs	Process Bus Sampled Values	Merging Units	Discussed how interoperability between different vendor IEDs and testing procedure
Mohagheghi, Tournier, Stoupis, Guise, Coste, Andersen & Dall (2011).	The paper provides some concrete examples on how IEC 61850 can be employed in the context of distribution automation applications, and what measures need to be taken to enable it to efficiently respond to some of the emerging technologies in DA systems	Not applicable	Not Applicable	Provides an example of IEC61850 application for capacitor bank protection and control
Mascarella, Chlela, Joos & Venne (2015).	This paper investigates a wind farm control scheme employing a slow-acting reactive power controller to regulate the steady-state voltage at the point of common coupling (PCC) and a fast-acting active power controller, streaming from an embedded energy storage system	Not applicable	OPAL-RT real-time digital simulator and it's software	The control strategy resulted in up to 83% reduction in the short-term flicker level

	(ESS) to mitigate flicker at the wind turbine terminals			
Krishnamurthy & Baningobera (2019).	To developed harmonic blocking scheme for transformer which uses element (87HB) of the transformer differential relay (SEL487E) to send an IEC61850 GOOSE-based harmonic blocking signal to the backup overcurrent relay (SEL751A) to inhibit from tripping during the transformer magnetizing inrush current conditions.	Transformer Differential Protection	SEL487E, SEL751A, CMC 356, Acselerator QuickSet, Acselerator Architect	Developed a harmonic blocking scheme with IEC61850 GOOSE application
Krishnamurthy, Jones & Mquqwana (2020).	The aim is to identify either the unit or element fails within the capacitor bank using the dedicated voltage differential protection function	Voltage Differential Protection	SEL487V, CMC 356, Acselerator QuickSet, Acselerator Architect	System-based testing method introduced and lab-scale simulation results provides early warning and location of fault on capacitor elements/units

2.5 Capacitor bank protection literature review

Table 2.3 shows an overview of the literature on capacitor bank protection methods and standards discussed in this section. Zulaski (1982) released a study on the ANSI/IEEE Standard C37.99-1980 standard review. The paper investigated several combinations published in the standard, such as current unbalance and voltage differential approaches for grounded and ungrounded capacitor bank units. Andrei and colleagues (1996) explored the design and operation of bridging capacitor banks. The research looked at both the control and protection of capacitor banks using imbalance protection. The protection scheme uses internally fused capacitor units, and the protection must be graded in accordance with the fuse. Dhillon (1998) reported work on fuseless capacitor bank protection. The study covered internally and externally fused capacitor banks, as well as the reasons why fuseless capacitor banks were chosen. Two protection mechanisms, current imbalance and voltage differential, as well as capacitor bank control strategies, have been examined.

Bishop and Chaudhary (2001) provided a paper on the principles of protected relaying of grounded and ungrounded Y-connected shunt capacitor banks. The authors explored imbalanced protection strategies, presenting benefits and drawbacks before recommending the usage of impedance-based protection solutions. They also discussed the advantages and disadvantages of impedance-based protection solutions. Fendrick et al. (2002) continued their research on impedance-based protection strategies for fuseless capacitor banks. By measuring impedance on series strings, the approach provides total bank protection and can detect strings with an alert or trip state based on the typical preset impedance. Lee et al. (2003) proposed a new innovative protection mechanism based on modified impedance protection. The proposed approach utilised impedance relay, and the test results demonstrated significant advantages over conventional impedance methods.

Amberg and Young (2010) published an application guide that demonstrates how to configure the SEL-487V for a fuseless bank application utilizing voltage differential. The guide provided a quick overview of capacitor bank protection and the IEEE standard. It then went on to demonstrate how the settings computation should be carried out, as well as the subsequent implementation on the SEL-487V relay. Smith (2010) gave calculations for capacitor bank protection parameters for both grounded and ungrounded capacitor banks. On both the bank and the system, protection strategies such as phase overcurrent,

negative sequence overcurrent, and overvoltage were investigated. Calculations for both current imbalance and voltage differential protection methods for warning and tripping settings were also shown in the article. Dos Santos et al. (2012) presented a work that used Rogowski coils to provide capacitor bank protection. The authors highlighted the benefits of employing these coils, stating that they produce low voltage outputs that do not increase when the conductor is disconnected. In the case of current unbalance, the proposed technique proved to be more successful than employing standard current transformers (CTs).

Ellis et al. (2012) reported work done for American Electric Power (AEP) that included design considerations of H configuration of grounded fuseless capacitor banks as well as details of the protective mechanism used. They advocated the use of imbalance protection, which would detect element failures and reduce the error margin difficulties that standard protection schemes encounter. Frye et al. (2012) discussed work done for the Tennessee Valley Authority (TVA) on the development of an application standard for capacitor bank protection and control. The TVA standard proposed has two IEDs for bus and bank protection, a single programmable logic controller (PLC) for control and operation, and up to six IEDs for individual capacitor stacks. The implementation was tested satisfactorily on the TVA 161 kV network.

Moxley et al. (2012) provided a paper that discussed the protection mechanisms used for grounded and ungrounded bank connections, as well as additional bank connections such as C-Type filter banks, capacitively grounded, and so on. The authors elaborated on the application, sensitivity, and speed of the chosen protection systems. The study discusses both current imbalance and voltage differential prevention systems. Wang et al. (2016) published a paper in which they discussed a protection strategy designed to identify internal problems in capacitor and filter banks that typically use the H configuration type. The goal, as with the other protection techniques outlined earlier, was to detect element failures and identify their location, provide a warning if the operational restrictions were not exceeded, and trip the bank if the operational constraints were exceeded.

A work on fault location on double wye connected shunt capacitor banks was discussed by Jouybari-Moghaddam et al. (2017). They demonstrated an improved neutral current unbalance protection algorithm for detecting and locating faulty parts on grounded and

ungrounded shunt capacitor banks. The proposed method was validated using PSCAD and MATLAB simulations for both internally fused and fuseless shunt capacitor banks. Jouybari-Moghaddam et al. (2018) continued their research and published a study on the development of a novel approach based on Superimposed Reactance (SR). To calculate the amount of SR, the suggested method makes use of already known measurements of the imbalance protection function. This was utilized in both internally fused and fuseless shunt capacitor banks and allows for wye grounding, wye grounding via a low ratio current transformer, and wye grounding via a capacitor at the neutral point. PSCAD and MATLAB simulation tools were used to test the newly proposed protection techniques.

Vandiver (2018) gave a presentation on capacitor bank protection and control techniques. The author talked about two operational band widths, narrow and wide bands, as well as protection methods such imbalance protection, phase overcurrent, negative sequence overcurrent, undervoltage, and so on. Krishnamurthy et al. (2020) presented a paper on shunt capacitor bank protection utilizing a voltage differential protection system. The protection strategy was tested on a lab test bench with a SEL-487V relay, an OMICRON CMC 256 plus, and the OMICRON RelaySimTest program. The hardwired trip and alarm signals were compared to the IEC 61850 GOOSE messaging solution. In terms of response and dependability, it was demonstrated that GOOSE surpasses hardwired solutions.

The following part presents discussion points from the peer-reviewed published publications on shunt capacitor bank protection methods.

Table 2.3. Review summary on capacitor bank protection

CAPACITOR BANK PROTECTION					
Author	**Aim**	**Protection Method**	**Bank Configuration**	**Software/Hardware**	**Achievements**
Zulaski (1982).	The purpose of the paper is to review some of the highlights of the guide for protection of capacitor banks to familiarize the industry with the scope and usefulness of this new document, and to invite considered discussion for the purpose of improving this guide in the future	Unbalance Protection, Voltage Differential	Grounded wye-wye and ungrounded wye	Not Applicable	The paper covered the highlights of the IEEE guide for protection of capacitor banks
Andrei, Kaushik & Reinaker (1996).	The paper discusses design and operation aspects related to the installation of a bridge capacitor bank in a substation	Unbalance Protection	H-Bridge, fused capacitor, grounded wye	Not Applicable	The bridge capacitor bank assembly was tested with an automatic switching control scheme and unbalance protection scheme was tested with good results
Dhillon (1998).	The paper reviews existing shunt capacitor bank technologies, discusses the advantages and disadvantages of the different capacitor technologies, and details the reasons why Pacific Gas and Electric Co. (PG&E) is implementing fuseless capacitor technology on all new shunt capacitor designs in their 115 and 230 kV system	Current unbalance and voltage differential	Grounded and ungrounded wye, fuseless, internally and externally fused	Not Applicable	The paper provided an overview discussion on different methods of capacitor bank protection methods for different bank configurations

Bishop, Day, & Chaudhary (2001).	The paper will focus on protective relaying philosophies of grounded and ungrounded Y-connected shunt capacitor banks, which are commonly applied on industrial and utility power systems	Unbalance Protection	Grounded and ungrounded wye	Not Applicable	The paper has presented an overview of capacitor bank protection schemes, discussing the variety of techniques that can be applied to detect unbalances due to failure of individual capacitor units in the bank
Fendrick, Day, Fender & McCall (2002).	The paper describes a novel application of the impedance method to provide complete bank protection by measuring the impedance of each series string of the capacitor bank	Impedance protection	Fuseless, grounded wye	Not Applicable	The paper has described the main features and advantages of a new scheme to protect multi-string fuseless capacitor banks.
Lee, Narayanan, Maffetone & Didsayabutra (2003).	The paper proposed a novel approach to the protection of the capacitor banks which modifies the impedance relay scheme to achieve the capacitor bank protection function with reliability	Impedance relay algorithm	Ungrounded Y	EMTP, C++ programming language	The proposed protection scheme successfully implemented a modified impedance relay algorithm that is more reliable
Amberg & Young (2010).	The application guide shows how to set the SEL-487V for a fuseless bank application using voltage differential	Voltage Differential Protection	Fuseless, grounded wye	SEL-487V, Acselerator QuickSet	The guide shows how the configuration of the relay is achieved for voltage differential protection of capacitor banks
Smith (2010).	The paper discusses methods of determining capacitor bank protection settings	Unbalance Protection	Grounded and ungrounded wye, fuseless, internally and externally fused	Not Applicable	The paper showed different mathematical approaches to different bank configurations for determining protection settings

Dos Santos, Lourenço, Martins, Monteiro & Kojovic, (2012).	The paper presents novel solutions for protection of capacitor banks using Rogowski coils as currents sensors	Current Unbalance	Grounded wye-wye	Rogowski coil current sensors	Verification of the scheme performance characteristics was performed as final verification that the system preserved its full performance characteristics after completing high power and impulse-current tests.
Ellis, Meisner & Thakur (2012).	The paper discusses the fundamentals of the design criteria (electrical and physical configurations) for H Configuration Grounded Fuseless Shunt Cap Bank and provides details about the development of an innovative Protective Relaying Schemes which accurately detects and identifies capacitor elements/units failures on each diagonal quadrant of each phase of Shunt Capacitor Banks	Imbalance protection scheme	H-Bridge, fuseless capacitor, grounded wye	Not Applicable	The innovative methods outlined in this paper show how the advancements in digital relays provide an opportunity for Relay Engineers to design more effective imbalance protection schemes for large Shunt Capacitor Banks in accurately detecting and tracking capacitor elements failures in each diagonal/phase and solving offsetting element failures issues of traditional protective relaying schemes
Frye, Hicks & Price (2012).	The paper will discuss in detail the capacitor bank protection and control scheme and its implementation and testing on a new configurable substation IED,	Phase voltage unbalance, phase and ground overcurrent	-	Programmable Logic Controller, Protection IED	The authors have been able to meet its design objectives of combining protection and control requirements into a

	which incorporates the all the necessary protection and logic control functions				minimum number of boxes
Moxley, Pope & Allen (2012).	The paper discusses the application, sensitivity, and speed of the applied protection schemes.	Current unbalance	Fuseless, grounded wye, double H	Not Applicable	The authors have discussed in detail the capacitor bank protection scheme applications and the importance of fast response
Wang, Ibrahim, Gajić & Saha (2016).	The paper describes a solution of a protection algorithm intended to detect internal element failures for large capacitor and filter banks	Unbalance Protection	Externally and internally fused,	Not Applicable	The method has been implemented based on unbalance detection considering tracing the unbalance current variations and tracking the change in the current-to-current phase angle measurements
Jouybari-Moghaddam, Sidhu, Parikh & Voloh (2017).	This paper elaborates on fault location for a common configuration in high-voltage SCBs, which is the double wye connection (Y-Y)	Neutral current unbalance	Externally fused, grounded and ungrounded double wye	PSCAD, MATLAB	A comprehensive investigation on fault location in double wye shunt capacitor banks with neutral unbalance protection was performed
Jouybari-Moghaddam, Sidhu, Voloh & Zadeh (2018).	The paper presents a new method using indicating quantity Superimposed Reactance (SR) to locate capacitor elements failures in Shunt Capacitor Banks	Superimposed Reactance	Externally fused, grounded and ungrounded wye	PSCAD, MATLAB, LABVIEW	A discriminating principle called Superimposed Reactance (SR) that has the following functionalities for both grounded and ungrounded wye-

					connected SCBs was presented
Vandiver (2018).	This paper discussed capacitor bank protection and control scheme including its implementation and testing on a configurable and scalable substation IED that incorporates all the necessary advanced protection and logic control functions	Unbalance Protection, Phase overcurrent, Negative sequence overcurrent, Earth fault, Under voltage, Breaker Failure	Fuseless, grounded wye	Not Applicable	The paper covered the fundamental protection elements used in typical capacitor bank applications, although there are many possible cap bank configurations, the principles for cap bank protection are the same
Krishnamurthy, Jones & Mquqwana (2020).	The aim of the paper is to identify either the unit or element fails within the capacitor bank using the dedicated voltage differential protection function	Voltage Differential Protection	Fuseless, grounded wye	Acselerator QuickSet, Architect, CMC 356, SEL-487V, RelaySimTest, PSCAD, MATLAB	The research work implemented lab-scale test bench setup for system-based voltage differential main protection and overload backup protection for shunt capacitor banks

2.5.1 Review discussion on shunt capacitor bank protection

A capacitor bank is a critical component of the electrical system that requires fast and dependable protection. The ANSI/IEEE Standard C37.99-1980 serves as the foundation for capacitor bank protection, and several researchers have written articles examining and describing the standard's use. The standard specifies rules and limits to be followed when constructing capacitor bank protection systems, such as 110 percent of nominal voltage that should not be exceeded, 135 percent continuous of nominal current that should not be exceeded, and so on. Different capacitor bank protection techniques, such as voltage differential protection, current imbalance prevention, and so on, are explored for various combinations of capacitor banks, such as directly grounded, capacitively grounded, ungrounded, and so on. Externally fused banks, internally fused banks, fuseless banks, and unfused banks are examples of capacitor bank designs. Some of the published research work was implemented on a real-world power system network, some on a lab scale, while yet others provide theoretical discussion. All of the published literature that was evaluated gave insight into the capacitor bank protection challenge and emphasized the significance of fast and reliable protection requirements in order to assure high bank availability. The following section provides a review of system-based testing approaches.

2.6 System-based testing

Skrbinjek and Cialla (2015) demonstrated a procedure for testing and verifying a protection system and a signal transmission system using distributed testing and a time-synchronized approach. The demonstration made use of RelaySimTest software for power system simulation, CMGPS for time synchronization, and CMC injection test sets. Geiger (2016) submitted a paper offering a testing technique for any distribution automation system that considerably saves testing time while verifying correct scheme operation through the usage of the auto reclose function in RelaySimTest software. Cowhey (2016) discussed a study that covers utilities' end-to-end testing approach. For complicated extra high voltage systems, the approach is shifting away from traditional steady state methods and toward system-based methodologies.

Fink (2017) published an application note describing the simulation of transformation ratio and phase shift in transformer testing using RelaySimTest software and a transformer differential protection method. Garcia and Baumeister (2017) published an application

note on how to use RelaySimTest software to test directional distance protection used as transformer backup protection.

Rud et al. (2017) presented work on many elements of system-based testing. Using the RelaySimTest software, the researchers investigated distance protection and line differential protection. Fink (2019) submitted an application note showing how to evaluate directional, transient, and intermittent ground faults using RelaySimTest. Pritchard (2019) published a paper in which he discussed a safe, simple, and rapid testing approach for distance protection relays. RelaySimTest is covered in the article Permissive Overreach Transfer Trip (POTT) with the usage of OMICRON's system-based testing tools.

Tagabe (2020) discussed the advantages of utilizing system-based testing methodologies for distributed systems over traditional testing methods. Krishnamurthy et al. (2020) presented research on system-based voltage differential protection testing for shunt capacitor banks. They also compared a hardwired solution for signals to the IEC 61850 GOOSE messaging service in the article. They were able to demonstrate that the GOOSE message is faster and more reliable than a hardwired alternative. Table 2.4 depicts the authors as previously described, as well as a comparison of the published material.

Table 2.4. Review summary on system-based testing

SYSTEM-BASED TESTING					
Author	**Aim**	**Protection Method**	**Bank Configuration**	**Software/Hardware**	**Achievements**
Skrbinjek & Cialla (2015).	To show how protection system and signal transmission system can be tested and verified using distributed testing and time synchronised approach.	Line Protection	N/A	CMC 256, RelaySimTest, DANEO 400, CMGPS 588	The successful testing of the protection system using system-based testing with RelaySimTest. The application made it possible to test the complete network from 5 different ends (with distributed injection devices on all 5 ends) synchronised via CMGPS device and communicating via MPLS and internet).
Geiger (2016).	This paper suggests a method for testing of any distribution automation network that will significantly reduce testing time while covering parameters which can influence a correct operation of the scheme.	Auto recloser	N/A	Recloser, RelaySimTest, CMGPS 588, CMC	The procedure successfully demonstrated the use of RelaySimTest to test distributed communication based automated distribution schemes
Cowhey (2016).	The paper describes a utilities approach to end to end testing, from traditional steady state methods to the evolution of system-based testing to test a complex extra high voltage (EHV) over line protection scheme, and outlines the test methods used and the issues identified.	Line Protection	N/A	RelaySimTest	The successful demonstration end to end system-based methodology over conventional end to end test methods.

Fink (2017).	The application note describes how a simulation the transformation ratio and phase shift in the transformer could be done in an easy and comfortable way using RelaySimTest.	Transformer Differential Protection	N/A	RelaySimTest	Successful demonstration of how the set up can be done on RelaySimTest as well as scenarios tested
Garcia & Baumeister (2017).	The application note describes how to test directional distance protection when it is used as a backup protection for a power transformer.	Distance Protection	N/A	RelaySimTest	Succesful demostration of how the set up for distance protection as transformer backup protection can be done on RelaySimTest as well as scenarios tested
Rud, Kyosev & Fong (2017).	The paper discusses all aspects of this system-based testing, from planning and execution to resolution of issues.	Distance Protection, Line Differential Protection	N/A	RelaySimTest	System-based Testing proved to be valuable in evaluating the performance of line protection systems at EPCOR. Through the simulation testing is useful to discover relay setting errors as well as relay algorithm errors.
Fink (2019).	The application note describes how to test the directional, transient and intermitting ground fault determination function of protection relays for insulated or compensated networks using RelaySimTest.	Directional	N/A	RelaySimTest	The successful demonstration end to end system-based methodology over conventional end to end test methods.
Pritchard (2019).	The article presents testing methodology for distance protection relays that is safe, simple and quick	Permissive Overreach Transfer Tripping	N/A	RelaySimTest	The use of RelaySimTest software was demonstrated and provided system-based testing solution to protection problem.

Tagabe (2020).	The article presents advantages using system-based testing methods for distributed systems over conventional methods utilizing RelaySimTest	N/A	N/A	RelaySimTest	The article highlighted the advantages system-based testing to test distributed systems over the conventional methods.
Krishnamurthy, Jones & Mquqwana (2020).	The aim of the paper is to identify either the unit or element fails within the capacitor bank using the dedicated voltage differential protection function	Voltage Differential Protection	Fuseless, grounded wye	Acselerator QuickSet, Architect, CMC 356, SEL-487V, RelaySimTest, PSCAD, MATLAB	The research work implemented lab-scale test bench setup for system-based voltage differential main protection and overload backup protection for shunt capacitor banks

The following part contains discussion points from the reviewed published articles on system-based testing methods.

2.7 Overall literature review discussion

The significance of capacitor banks in the power system network is explored, and their protection is even more critical since fast and reliable protection is necessary. The evaluated articles gave insight into various capacitor bank protection strategies for various capacitor bank configurations, the use of the IEC 61850 standard and how it is implemented on capacitor bank protection, and newly developed system-based testing methods.

The researched publications provide insight into existing capacitor bank protection approaches and how they have been used to solve capacitor protection problems. Various protection approaches, including as impedance protection, imbalance protection, superimposed reactance, voltage differential, and so on, are used to provide primary protection for shunt capacitor banks.

The IEC 61850 Standard for substation automation is examined to assess its application and advantages over traditional hardwired techniques, which are costly and difficult to change designs. Publications on system-based testing methods are analyzed to determine their implementation and advantages over traditional test methods. The data aided in the research to discover how a voltage differential protection scheme can be implemented using the most recent available technologies and techniques, such as the IEC 61850 Standard and system-based testing methods.

2.8 Conclusion

Losses in electrical power systems are classified as technical and nontechnical losses. Non-technical losses are caused by tempering with meters, theft, and so on, whereas technical losses are caused by energy dissipated in conductors, system equipment, magnetic losses in transformers, and so on. The chapter examined methods for lowering technical power losses, notably reactive power compensation employing shunt capacitor banks. Shunt capacitor bank installation is crucial to the system and must be done strategically in terms of placement, size, and function. The chapter covers an overview of capacitors and their role in power systems, as well as bank configuration and protection strategies. Substation automation systems, capacitor protection theory and applications, capacitor bank settings calculations and testing, and other papers were reviewed. These published papers were categorized and reviewed as such.

The following chapter discusses backup protection utilizing overcurrent and over/under voltage protection techniques, as well as simulation experiments using DIGSILENT software.

Technical power losses, more specifically reactive power compensation with shunt capacitor banks Shunt capacitor bank installation is crucial to the system and must be done strategically in terms of placement, size, and function. The chapter covers an overview of capacitors and their role in power systems, as well as bank configuration and protection strategies. Substation automation systems, capacitor protection theory and applications, capacitor bank settings calculations and testing, and other papers were reviewed. These published papers were categorized into 1) Protection schemes for capacitor banks 2) IEC61850 standard applications for capacitor bank protection and 3) System-based testing method to test the shunt capacitor bank protection configurations are reviewed in detail.

3. CHAPTER THREE: CAPACITOR BANK SIMULATION AND PROTECTION STUDIES

3.1 Introduction

The chapter describes the base case power system network and its parameters, as well as a simulation study in DIGSILENT Power Factory software. The fault currents are then estimated at various network fault locations. The relay settings are then calculated based on the fault level estimates and the network's normal operating conditions. To protect capacitor banks, the DIGSILENT software version of the SEL 751A relay overcurrent protection relay is used, and the calculated fault current settings are used to configure the protection relay, and simulation results are used to confirm relay operation speed and reliability of the protection scheme.

Capacitor bank protection consists of two components: bank protection and system protection. The latter is covered in depth in this chapter and is utilized as a backup protection, specifically overcurrent protection. The chapter describes the simulation studies, protective settings calculations, and testing the protection functions on DIGSILENT Power Factory.

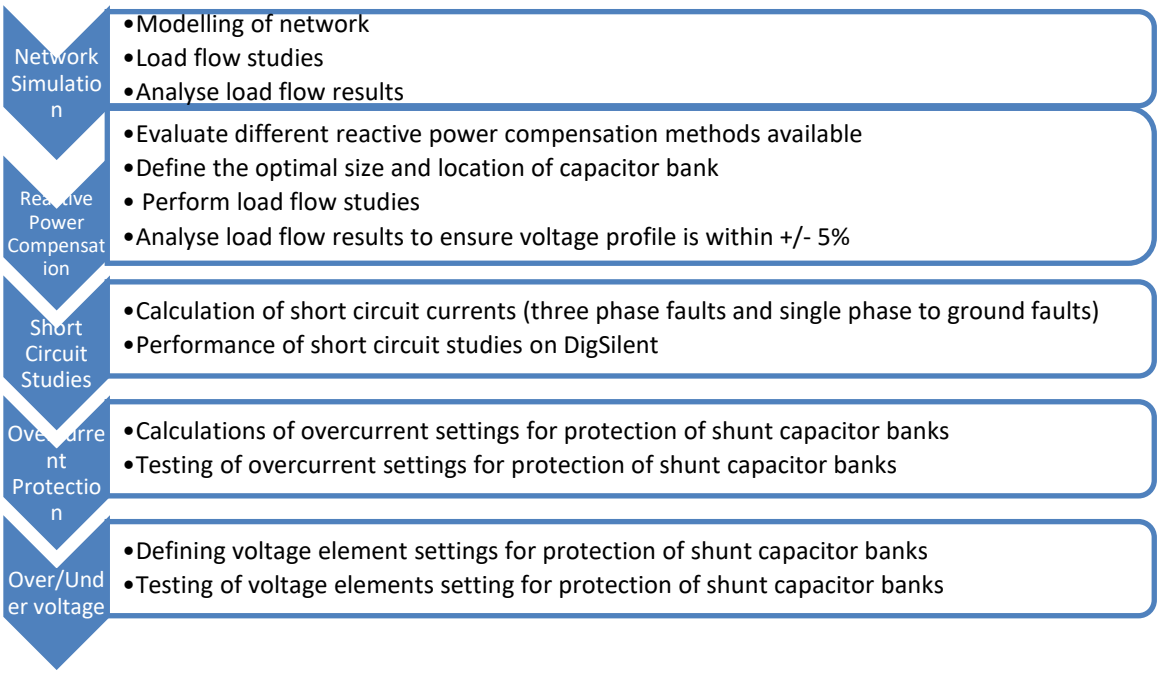

Figure 3.1. Chapter 3 flow diagram

Figure 3.1 depicts the flow diagram for the chapter, which is divided into five sections. Section 3.2 goes through electrical network modelling, load flow investigations, and reactive power correction in DIGSILENT Power Factory software. Section 3.3 discusses short circuit investigations, followed by Section 3.4, which discusses protection setting calculations. Sections 3.5 and 3.6, respectively, present the simulation outputs, discussions, and conclusions.

3.2 Modelling of electrical system networks

The section describes the presented electrical power system as well as the modelling performed on the software package. The network is depicted as a single line diagram in the following section.

3.2.1 Single line diagram of the network

The electrical network is a four-bus network with the supply represented by the external grid and has two transformers, one overhead line and two loads. The network has three standard voltage levels, 66 kV on the source side, 144.9 kV sub-transmission level and the 33 kV the distribution level.
DIGSILENT is used to model the network, and load flow experiments are carried out. The load flow results are used to determine the network's regular functionality. It is well known that the system does not always operate under normal settings; abnormal, transient conditions are also encountered. During these abnormal conditions, the system, equipment, and, most importantly, personnel must all be kept safe. This is why protection devices are used, and as a result, suitable protection settings must be determined. Short circuit studies are performed to establish fault levels at various network sites, and the results are utilized to define protection device settings and proper equipment ratings.

Figure 3.2 depicts a single line diagram of the network that has been modelled and studied. The data for the electrical components of the system depicted in the diagram are given in the next sections.

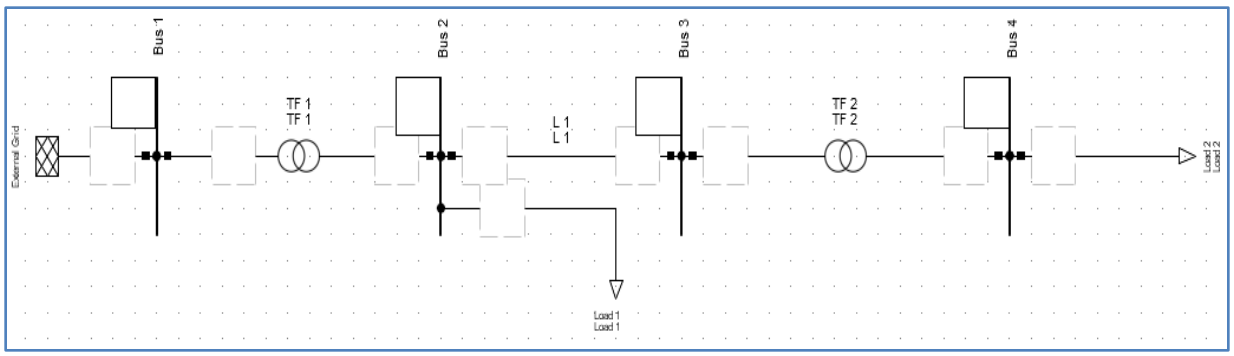

Figure 3.2. Single line diagram

3.2.2 Network data

The section displays the network data of the sample network 66/144.9kV for all of the electrical components of the system depicted in Figure 3.2. To conduct load flow studies, all network data for all equipment must be established on the system model in DIGSILENT software. Once the data has been entered into the software, load flow calculations can begin. Load flow calculations are used to calculate any two of the four following quantities: voltage V, voltage angle, active power P, and reactive Q. Two of these quantities are known at each node, while the other two must be estimated. This is what load flow studies are for. The network data to be setup on each component of the software is shown in Table 3.1. The following subsection discusses the load flow results from the DIGSILENT software program.

Table 3.1. Network data

External Grid		**Line**		**Transformer 2**	
Bus Type	Slack Bus	Rated Voltage	144.9 kV	Type	2 winding
Angle	0	Rated Current	1 kA	Rating	80 MVA
Voltage Set point	1 pu	AC Resistance (1,2)	0.2376 Ω/km	Voltage	144.9/33 kV
Short Circuit VDE/IEC	1000 MVA max	Reactance (1,2)	0.3465 Ω/km	Impedance	7.5%
		AC Resistance (0)	0.2546 Ω/km	Copper Losses	5.5 kW
	800 MVA min	Reactance (0)	0.3245 Ω/km	Vector group	YN/YN
Transformer 1		Length	18.56 km		
Type	2 winding			**Load 2**	
Rating	150 MVA	**Load 1**		Type	Balanced
Voltage	66/144.9 kV	Type	Balanced	Active Power	55.96 MW
Impedance	6.0%	Active Power	53.62 MW	Reactive Power	21.74 Mvar
Copper Losses	4.5 kW	Reactive Power	23.86 Mvar		
Vector group	YN/YN	Voltage	1 pu	Voltage	1 pu

3.2.3 Load flow results

After completing network configuration and modelling on the DIGSILENT software package, load flow experiments can be performed. This section summarizes the findings of the network's load flow investigations. The findings of load flow experiments are shown in Figure 3.3, as seen on the DIGSILENT software single line overview graphic. The data show that transformers 1 and 2 are loaded at 82.8 percent and 80.3 percent, respectively. The voltages on the bus bars are as follows: 1 p.u. on Bus 1, 0.98 p.u. on bus 2, 0.96 p.u. on bus 3, and 0.93 p.u. on bus 4, with a line loading of 85.4 percent. Figure 3.3 shows that both the transformers and the line are overloaded, as indicated by the orange colour.

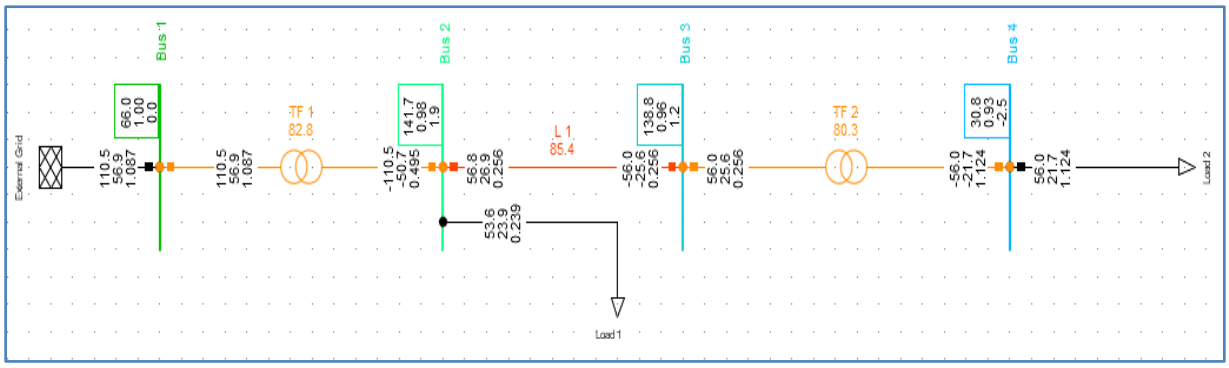

Figure 3.3. Load flow results

The data given in Figure 3.3 is also shown in a table format in Table 3.2. The table displays the grid summary report, which includes both active and reactive power losses. The active power loss is 0.82 MW, the reactive power loss is 10.89 MVar, and the load power factor is 0.91. Overloading on the network necessitates action, otherwise the equipment's lifespan will be severely shortened. According to the data in Table 3.2, the loads are very inductive and demand a large amount of reactive power from the grid, which is the reason of the high current flowing in the network from the grid. The total active power drawn from the grid is also shown as 108.40 MW, whereas the reactive power is 58.49 MVar (including line and transformer losses).

Table 3.2. Grid summary report without capacitor bank

Load Flow Calculation				Grid Summary
AC Load Flow, unbalanced, 3-phase (ABC)		Automatic Model Adaptation for Convergence		No
Automatic tap adjustment of transformers	No	Max. Acceptable Load Flow Error		
Consider reactive power limits	No	Bus Equations(HV)		1.00 kVA
		Model Equations		0.10 %

Grid: Grid	System Stage: Grid	Study Case: Study Case	Annex: / 1

Grid: Grid	Summary								
No. of Substations	0	No. of Busbars	4	No. of Terminals	0	No. of Lines	1		
No. of 2-w Trfs.	2	No. of 3-w Trfs.	0	No. of syn. Machines	0	No. of asyn.Machines	0		
No. of Loads	2	No. of Shunts/Filters	1	No. of SVS	0				
Generation	=	0.00	MW	0.00	Mvar	0.00	MVA		
External Infeed	=	100.44	MW	45.55	Mvar	110.29	MVA		
Inter Grid Flow	=	0.00	MW	0.00	Mvar				
Load P(U)	=	99.58	MW	35.60	Mvar	105.75	MVA		
Load P(Un)	=	99.58	MW	35.60	Mvar	105.75	MVA		
Load P(Un-U)	=	0.00	MW	0.00	Mvar				
Motor Load	=	0.00	MW	0.00	Mvar	0.00	MVA		
Grid Losses	=	0.86	MW	9.95	Mvar				
Line Charging	=			0.00	Mvar				
Compensation ind.	=			0.00	Mvar				
Compensation cap.	=			0.00	Mvar				
Installed Capacity	=	0.00	MW						
Spinning Reserve	=	0.00	MW						
Total Power Factor:									
Generation	=	0.00	[-]						
Load/Motor	=	0.94 / 0.00	[-]						

As seen in Table 3.3, the voltages on bus 4 are dropping below the standards' criteria by -/+ 5%. As the conductor temperatures rise due to the high currents flowing in the network from the grid, more power losses (active and reactive power) are experienced. bus 1 has a voltage of 1 p.u., bus 2 has a voltage of 0.978 p.u., bus 3 has a voltage of 0.958 p.u., and bus 4 has a voltage of 0.934 p.u. According to the data in the Table, bus 3 is on the border line, while bus 4 is below the threshold, and customer voltage sensitive equipment may be impacted, and penalties may be levied.

As demonstrated by the load flow data, intervention methods are required to remedy network faults, and these are discussed further below in the reactive power compensation section.

Table 3.3. The network's voltage profile

		DIgSILENT PowerFactory 2020 SP1	Project:	
			Date: 11/23/2021	

Load Flow Calculation		Complete System Report: Substations, Voltage Profiles, Grid Interchange	
AC Load Flow, unbalanced, 3-phase (ABC)		Automatic Model Adaptation for Convergence	No
Automatic tap adjustment of transformers	No	Max. Acceptable Load Flow Error	
Consider reactive power limits	No	Bus Equations(HV)	1.00 kVA
		Model Equations	0.10 %

Grid: Grid	System Stage: Grid	Study Case: Study Case	Annex: / 4

	rtd.V [kV]	Bus - voltage [p.u.]	[kV]	[deg]	Voltage - Deviation [%] −10	−5	0	+5	+10
Bus 1									
	66.00	1.000	66.00	-0.00					
Bus 2									
	144.90	0.983	142.38	-2.34					
Bus 3									
	144.90	0.962	139.41	-3.06					
Bus 4									
	33.00	0.939	30.98	-6.38					

3.2.4 Reactive power compensation methods

There are a few alternatives available for improving the voltage profile on the network. Network reconfiguration, network re-conductoring, distribution transformer position and sizing, automatic voltage booster, reactive power compensation, and aerial bunched cables are among the solutions that can be adopted, according to Kour and Sharma, 2013. A network upgrade that increases the ratings of electrical components such as lines and transformers can be utilized to help with network overloading.

This solution would be prohibitively expensive because transformers are notoriously expensive and have lengthy lead periods, hence it will not be investigated. The reactive power compensation methods are further classified as Static Var Compensators (SVC), Static Synchronous Compensators (STATCOM), capacitor bank installation, and so on. The capacitor bank option is the least expensive and easiest to install, and it will be investigated further. Capacitor banks can be deployed either in series on long transmission lines to help enhance load capacity or in parallel to help boost the voltage profile, improve power factor, and reduce power losses. Because the load flow results suggest that the voltage profile is quite bad and requires intervention, as well as overloading of electrical components on the network, a shunt capacitor bank is selected to help with these difficulties.

There are numerous approaches that have been utilized since the start of the project to identify the appropriate capacitor bank size, number, and position. These approaches, according to Ng et al. 2000, are categorised as follows:

i. Analytical Methods
ii. Numerical Programming Methods
iii. Heuristic Methods
iv. Artificial Intelligence Methods

DIGSILENT software performs an Optimal Capacitor Placement computation to determine the capacitor size from a list of available capacitor sizes. The calculating formula utilized by the software is presented next.

$$T_{cost} = C_{losses} + \sum_{i=1}^{m} C_{capi} + \sum_{i=1}^{n} C_{volviol} \quad 3.1$$

Whereby,

T_{cost} Total annual network cost
C_{losses} Annual cost of losses, i.e. I^2R losses
C_{capi} Annual cost capacitor bank including installation, maintenance, etc.
$C_{volviol}$ Fictitious cost used for voltage violations

Table 3.4 shows the list of available capacitor bank sizes. As shown in the table, capacitor bank sizes and costs were chosen at random based on cost data from renewable projects in South Africa. The annual cost of supplying, installing, and maintaining an 18 MVar capacitor bank is ZAR 540 000, ZAR 660 000 for a 22 MVar, ZAR 840 000 for a 28 MVar, ZAR 1 650 000 for a 55 MVar, and ZAR 2 400 000 for an 80 MVar. The optimal capacitor placement analysis is performed to identify the lowest cost while still meeting the specified network voltage levels.

Table 3.4. List of capacitor banks

	Ignored	Q per Step Mvar	Switchable	Max.Step	Technology	Cost ZAR/a
1	☐	18.	☐	1	Three-phase	540000.
2	☐	22.	☐	1	Three-phase	660000.
3	☐	28.	☐	1	Three-phase	840000.
4	☐	55.	☐	1	Three-phase	1650000
▶ 5	☐	80.	☐	1	Three-phase	2400000

The calculation results for the optimal capacitor placement research are shown in Table 3.4. It should be noted that the feeder selection was limited to high-voltage terminals (144.9 kV section). The results demonstrate that, of the possible capacitor banks listed in Table 3.4, a 22 MVar capacitor bank installed on bus 3 is chosen as the ideal capacitor bank size based on the annual savings, as shown in Table 3.5. The study used voltage limitations of +/- 5% of nominal and a maximum capacitor bank of 100 MVar for installation. The results reveal that the cost of power losses per year before the optimization process was ZAR 7 623 339.10, whereas the cost after the optimization process was ZAR 6 090 898.36, resulting in a cost savings of ZAR 1 532 440.74 per year. Subtracting the cost of supplying, installing, and maintaining a 22 MVar capacitor bank results in a first-year savings of ZAR 872 440.74.

Table 3.6 compares the calculation results for an 18 MVar and 28 MVar capacitor bank using formula 3.1 to the results of Table 3.5. There is a minor variance in the cost savings section, with the installation of a 22 MVar capacitor bank yielding larger savings than the other two capacitor bank sizes. The Table demonstrates that the supply, installation, and maintenance of 18 and 28 MVar capacitor banks cost ZAR 852 459.66 and ZAR 782 167.39, respectively, which is less than the savings offered by a 22 MVar capacitor bank.

Table 3.5. Results of optimal capacitor placement

		DIgSILENT PowerFactory 2020 SP1B	Project: Date: 6/2/2020
Network Representation	Balanced, positive sequence	Constraints	
Time period under consideration	1 year	Upper Voltage Limit	1.05 p.u.
		Lower Voltage Limit	0.95 p.u.
Energy Costs		Limit Reactive Power of all Capacitors	No
Take from External Grid	No	Maximum	100.00 Mvar
Energy Cost	1.06 ZAR/kWh		

Costs		Reactive power of installed capacitors	
Before Optimisation		Before Optimisation	0.00 Mvar
Power Losses	7623339.10 ZAR	New Capacitors	22.00 Mvar
Voltage Violations	0.00 ZAR	After Optimisation	22.00 Mvar
Total	7623339.10 ZAR		
After Optimisation			
Power Losses	6090898.36 ZAR		
Voltage Violations	0.00 ZAR		
Costs of new capacitors	660000.00 ZAR		
Total	6750898.36 ZAR		
Saved Costs			
Power Losses	1532440.74 ZAR		
Voltage Violations	0.00 ZAR		
Total	872440.74 ZAR		

New Capacitors	Busbar	Technology	Station	Costs	Phases	Vector Group	Un [kV]	Capacitor
Shunt/Filter 1	Bus 3	ABC		660000.00 ZAR/a	abc	D	144.90	22.00 Mvar

New Capacitors	Busbar	Technology	Station	Load Level	Act.Step	Max.Step
Shunt/Filter 1	Bus 3	ABC				
				Load Level 100 %	1	1

Table 3.6. Comparisons of savings with different capacitor bank size

Bank Size (Mvar)	P loss before optimization	P loss after optimization	Total cost savings
18	7 623 339.10 ZAR	6 230 879.44 ZAR	852 459.66 ZAR
22	7 623 339.10 ZAR	6 090 898.36 ZAR	872 440.74 ZAR
28	7 623 339.10 ZAR	6 001 171.71 ZAR	782 167.39 ZAR

The simulation results are shown in the table after the installation of a 22 MVar capacitor bank, which improved the voltage profile to within the acceptable standard limits. When comparing Tables 3.3 and 3.7, it is clear that the voltage on bus 3 grew from 0.96 p.u. to 0.97 p.u., whereas the voltage on bus 4 increased from 0.93 p.u. to 0.95 p.u. Figure 3.4 depicts the usual operating conditions of the network covered in this chapter when there is no overloading.

Table 3.7. Voltage profile with a capacitor bank

			DIgSILENT PowerFactory 2020 SP1	Project:	Date: 11/23/2021

Load Flow Calculation — Complete System Report: Substations, Voltage Profiles, Grid Interchange

AC Load Flow, unbalanced, 3-phase (ABC)		Automatic Model Adaptation for Convergence	No
Automatic tap adjustment of transformers	No	Max. Acceptable Load Flow Error	
Consider reactive power limits	No	Bus Equations (HV)	1.00 kVA
		Model Equations	0.10 %

Grid: Grid — System Stage: Grid — Study Case: Study Case — Annex: / 4

	rtd.V [kV]	Bus - voltage [p.u.]	[kV]	[deg]	Voltage - Deviation [%] −10 −5 0 +5 +10
Bus 1					
	66.00	1.000	66.00	-0.00	
Bus 2					
	144.90	0.991	143.63	-2.32	
Bus 3					
	144.90	0.978	141.65	-3.27	
Bus 4					
	33.00	0.955	31.50	-6.49	

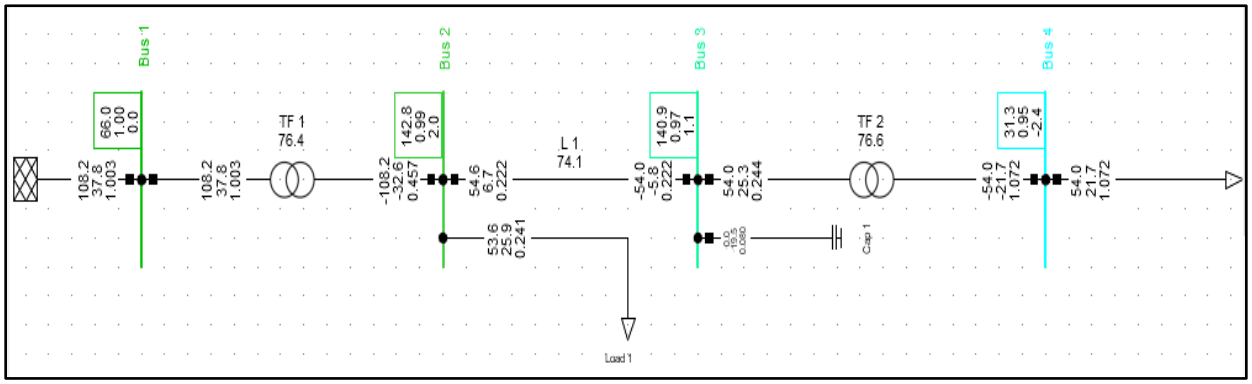

Figure 3.4. Load flow results with capacitor bank

The grid summary report after the installation of the 22 MVar capacitor bank on bus 3 is shown in Table 3.8. The table shows that both active and reactive power losses have decreased. Active power losses fell from 0.82 MW to 0.66 MW, while reactive power fell from 10.89 MVar to 9.74 MVar. This reduction helps in reducing overloading on electrical components.

Table 3.8. Grid summary report with a capacitor bank

Load Flow Calculation				Grid Summary
AC Load Flow, unbalanced, 3-phase (ABC)		Automatic Model Adaptation for Convergence		No
Automatic tap adjustment of transformers	No	Max. Acceptable Load Flow Error		
Consider reactive power limits	No	Bus Equations(HV)		1.00 kVA
		Model Equations		0.10 %

Grid: Grid	System Stage: Grid	Study Case: Study Case	Annex: / 1

Grid: Grid	Summary								
No. of Substations	0	No. of Busbars	4	No. of Terminals	0	No. of Lines	1		
No. of 2-w Trfs.	2	No. of 3-w Trfs.	0	No. of syn. Machines	0	No. of asyn.Machines	0		
No. of Loads	2	No. of Shunts/Filters	1	No. of SVS	0				
Generation	=	0.00	MW	0.00	Mvar	0.00	MVA		
External Infeed	=	100.28	MW	23.93	Mvar	103.09	MVA		
Inter Grid Flow	=	0.00	MW	0.00	Mvar				
Load P(U)	=	99.58	MW	35.60	Mvar	105.75	MVA		
Load P(Un)	=	99.58	MW	35.60	Mvar	105.75	MVA		
Load P(Un-U)	=	0.00	MW	0.00	Mvar				
Motor Load	=	0.00	MW	0.00	Mvar	0.00	MVA		
Grid Losses	=	0.70	MW	8.97	Mvar				
Line Charging	=			0.00	Mvar				
Compensation ind.	=			0.00	Mvar				
Compensation cap.	=			-20.64	Mvar				
Installed Capacity	=	0.00	MW						
Spinning Reserve	=	0.00	MW						
Total Power Factor:									
Generation	=	0.00	[-]						
Load/Motor	=	0.94 / 0.00	[-]						

Figure 3.5 depicts the voltage and current waveforms at bus 3, with graph 2 indicating the voltage waveform and graph 1 indicating the capacitor bank current waveform. Because the load flow results showed an RMS voltage of 140.90 kV (0.97 p.u.), the graph shows a peak value of 199.132 kV, which equals to an RMS voltage of 140.8 kV. Graph 1 also indicates a peak value of 119 A, which corresponds to an RMS value of 84.13 A, which is extremely close to the load flow values. These are the network's typical operating conditions, with no interruptions.

Table 3.9 shows a comprehensive system report created by the DIGSILENT software package for the load flow results with voltage profiles and grid interchange chosen. The report displays power exchange, both incoming and outgoing, by network voltage level, beginning with the lowest voltage level and progressing to the highest voltage level, as well as total power exchange. A negative indication shows entering or injected power into the bus bar, whereas a positive sign indicates power leaving the bus bar.

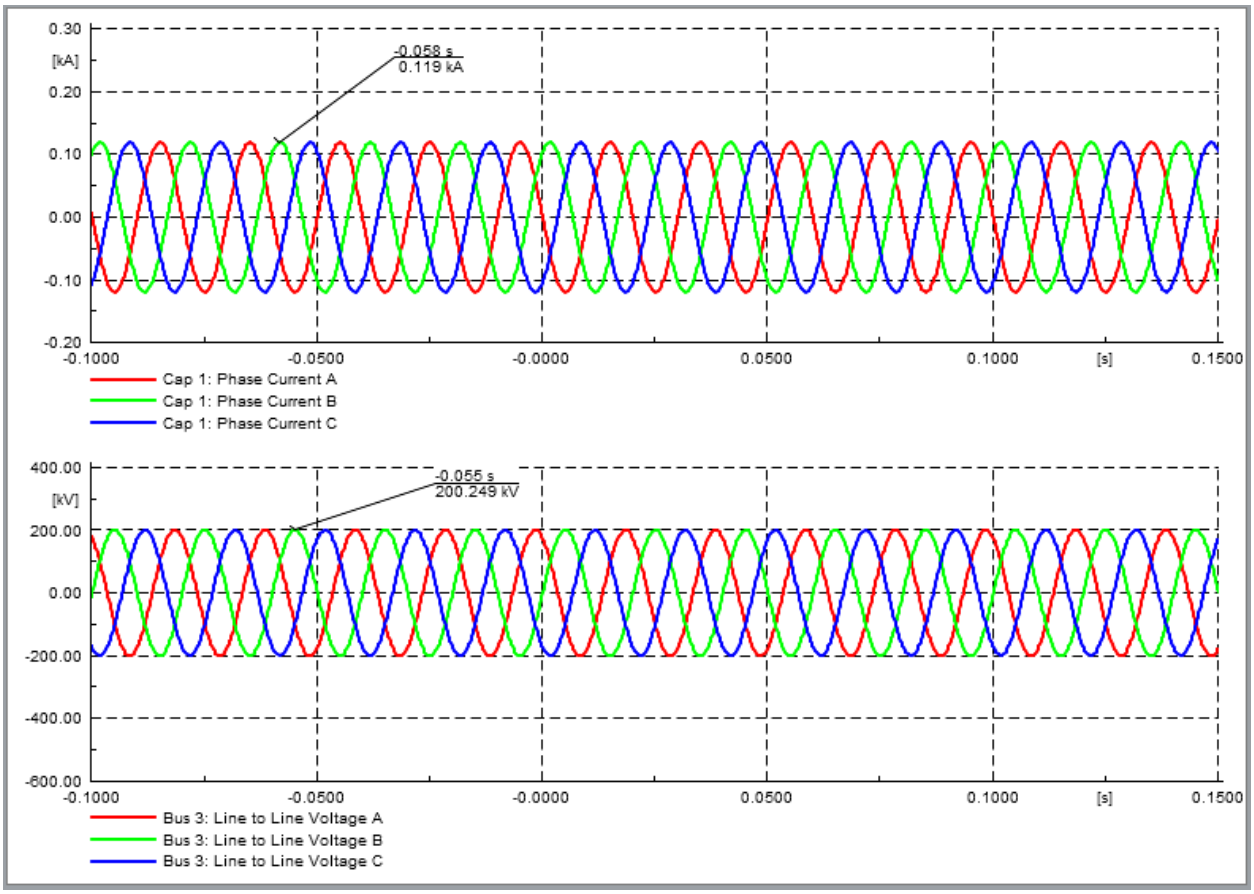

Figure 3.5. Voltage and current waveforms

The 33 kV segment has incoming and outgoing power of +/- 55.96 MW and +/- 21.74 MVar, with load losses of 3.74 MW. The incoming input of 110.29 MW and 34.87 MVar is shown in the 66 kV network section. The 144.9 kV has a load power requirement of 53.62 MW and 23.86 MVar, with the capacitor bank injecting 20.84 MVar into the bus and line losses of 0.7 MW and 1.02 MVar. The 144.9 kV segment is connected via two transformers, as depicted on the network diagram, 66/144.9 kV as transformer 1 and 144.9/33 kV as transformer 2. This is also stated in the study, with the power exchange for the 33 kV interchange being 55.96 MW and 25.48 MVar, and the power exchange for the 66 kV interchange being -110.28 MW and -29.52 MVar. In these voltage levels, the active and power losses are as discussed. According to the report, the total load requirements are 109.58 MW and 45.60 MVar, with the capacitor bank supplying 20.84 MVar. The total external power drawn is 110.29 MW and 34.87 MVar, with total power losses of 0.71 MW and 10.11 MVar.

Table 3.9. Report on the entire system

Grid: Grid	System Stage: Grid	Study Case: Study Case	Annex: / 1

Volt. Level [kV]	Generation [MW]/ [Mvar]	Motor Load [MW]/ [Mvar]	Load [MW]/ [Mvar]	Compen-sation [MW]/ [Mvar]	External Infeed [MW]/ [Mvar]	Interchange to	Power Interchange [MW]/ [Mvar]	Total Losses [MW]/ [Mvar]	Load Losses [MW]/ [Mvar]	No load Losses [MW]/ [Mvar]
33.00	0.00	0.00	55.96	0.00	0.00			0.00	0.00	0.00
	0.00	0.00	21.74	0.00	0.00			0.00	0.00	0.00
						144.90 kV	-55.96	0.00	0.00	0.00
							-21.74	3.71	3.71	0.00
66.00	0.00	0.00	0.00	0.00	100.28			0.00	0.00	0.00
	0.00	0.00	0.00	0.00	23.93			0.00	0.00	0.00
						144.90 kV	100.28	0.00	0.00	0.00
							23.93	4.25	4.25	0.00
144.90	0.00	0.00	43.62	0.00	0.00			0.69	0.69	0.00
	0.00	0.00	13.86	-20.64	0.00			1.01	1.01	0.00
						33.00 kV	55.96	0.00	0.00	0.00
							25.45	3.71	3.71	0.00
						66.00 kV	-100.28	0.00	0.00	0.00
							-19.68	4.25	4.25	0.00
Total:	0.00	0.00	99.58	0.00	100.28		0.00	0.70	0.70	0.00
	0.00	0.00	35.60	-20.64	23.93		0.00	8.97	8.97	0.00

Total System Summary	Study Case: Study Case	Annex: / 2

	Generation [MW]/ [Mvar]	Motor Load [MW]/ [Mvar]	Load [MW]/ [Mvar]	Compen-sation [MW]/ [Mvar]	External Infeed [MW]/ [Mvar]	Inter Area Flow [MW]/ [Mvar]	Total Losses [MW]/ [Mvar]	Load Losses [MW]/ [Mvar]	No load Losses [MW]/ [Mvar]
\ax12497\Capacitor Bank Project\Network Model\Network Data\Grid									
	0.00	0.00	99.58	0.00	100.28	0.00	0.70	0.70	0.00
	0.00	0.00	35.60	-20.64	23.93	0.00	8.97	8.97	0.00
Total:									
	0.00	0.00	99.58	0.00	100.28		0.70	0.70	0.00
	0.00	0.00	35.60	-20.64	23.93		8.97	8.97	0.00

The previous sections discussed simulation and network modelling, as well as reactive power compensation strategies for improving voltage profiles in order to produce a stable network. The next part goes over short circuit current calculations and simulations with the IEC6009 standard.

3.3 Short circuit simulations and calculations

The section covers a method for computing short circuit currents in a network, as well as simulation with the DIGSILENT software package.

3.3.1 Short circuit calculations

The goal of this section is to cover different ways for calculating short circuit current. The purpose of performing these calculations is twofold: the planning stage, in which equipment ratings and other parameters are determined, and the operations stage, in

which short circuit limits must be determined when network reconfiguration occurs, as well as verification of protection settings, among other things, to ensure that they are not exceeded.

Two fundamentally different methodologies are employed when undertaking short circuit current studies for both planning and operations purposes. Estimates are used for planning studies because the system operating conditions are not yet understood. The strategy of placing an equivalent voltage source at the fault location is used for this purpose. In general, two standards are commonly used and accepted: IEC 909 (VDE 0102) and its revised version, IEC 60909. The approach is independent of system load flow, is based on nominal system dimensions, and employs correction factors for voltages and impedances. The method yields prudent results.

The network operating circumstances are well understood for short circuit calculations during the operations stage. In comparison to the other approaches stated, the superposition method, also known as the complete method, is employed and produces accurate findings. Using the findings of load flow studies, the approach determines short circuit currents based on existing network operating circumstances. The graphs in Figure 3.6 depict short circuit currents as a function of time, courtesy of the IEC6090 standard.

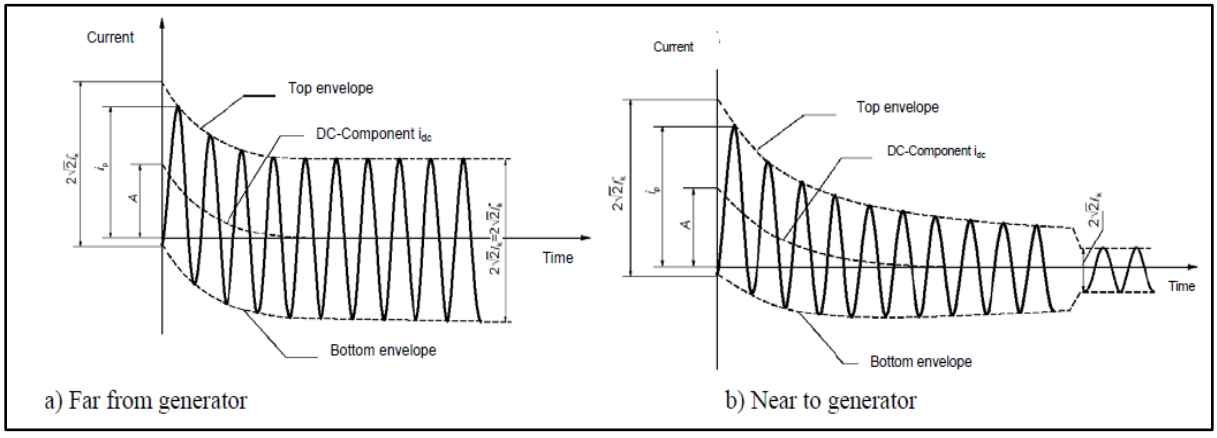

Figure 3.6. Short circuit currents as a function of time

Further, as shown in Figure 3.6, short circuit currents measured near the generator are different from those measured far from the generator. The IEC 60909 standard computes two parameters,

- Maximum short circuit current to determine electrical equipment rating.
- Minimum short circuit currents for use in determining the foundation of protection devices settings.

The following process as per IEC 60909 standard is followed.

- Calculate the equivalent short circuit impedances for all network equipment. Convert all impedances to the reference voltage level.
- Calculation of short circuit currents at various locations for various fault types, particularly three-phase and single-phase to ground short circuits.

Three phase, two phase, two phase to ground, and single phase to ground short circuits are the most prevalent faults considered. Only three phase and single phase to ground faults are examined in this study as the others are a combination of these faults.

The following calculations are based on the network diagram in Figure 3.4 as well as the data in Table 3.1, which includes the capacitor bank of 22 MVar. The procedure outlined is based on the IEC 60909 standard.

3.3.2 Three phase short circuit calculations

Figure 3.7 depicts an equivalent impedance diagram of a network for positive sequence components, in which all electrical components are represented by equivalent impedances. Appendix A.1 contains the formulae and computations for these impedances, as well as the fault current calculations.

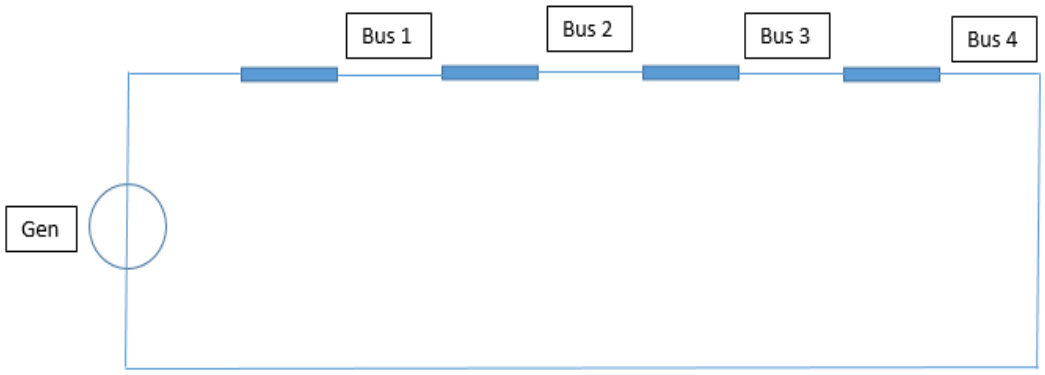

Figure 3.7. Positive sequence equivalent impedance diagram

The following subsection analyzes ground-related defects in the same manner as this section.

3.3.3 Calculations for ground-related short circuits

Ground related short circuit currents are calculated using the same method as three phase short circuit currents. The only distinction is that zero-sequence impedances are taken into account rather than positive/negative sequence values. The formulae differ slightly, but the method is the identical, and they, as well as the fault current calculations, are shown in Appendix A.1.

The calculating process stated in the IEC60909 standard was followed, and the same will be accomplished in the following part utilizing a software program.

3.3.4 Short circuit simulations

The DIGSILENT software tool is used to perform short circuit simulation investigations, and the findings are exhibited and discussed in this part. As shown in Figure 3.8, balanced three phase short circuit faults are used in all four bus terminals. The short circuit simulation studies are carried out in accordance with the IEC 60909 standard, as shown in Table 3.10, with maximum fault levels at all bus terminals. The maximum short current data aid in determining equipment ratings. The study was also carried out to identify the minimal short circuit currents, as shown in Table 3.11. The calculation findings aid in determining the foundation for network protection settings.

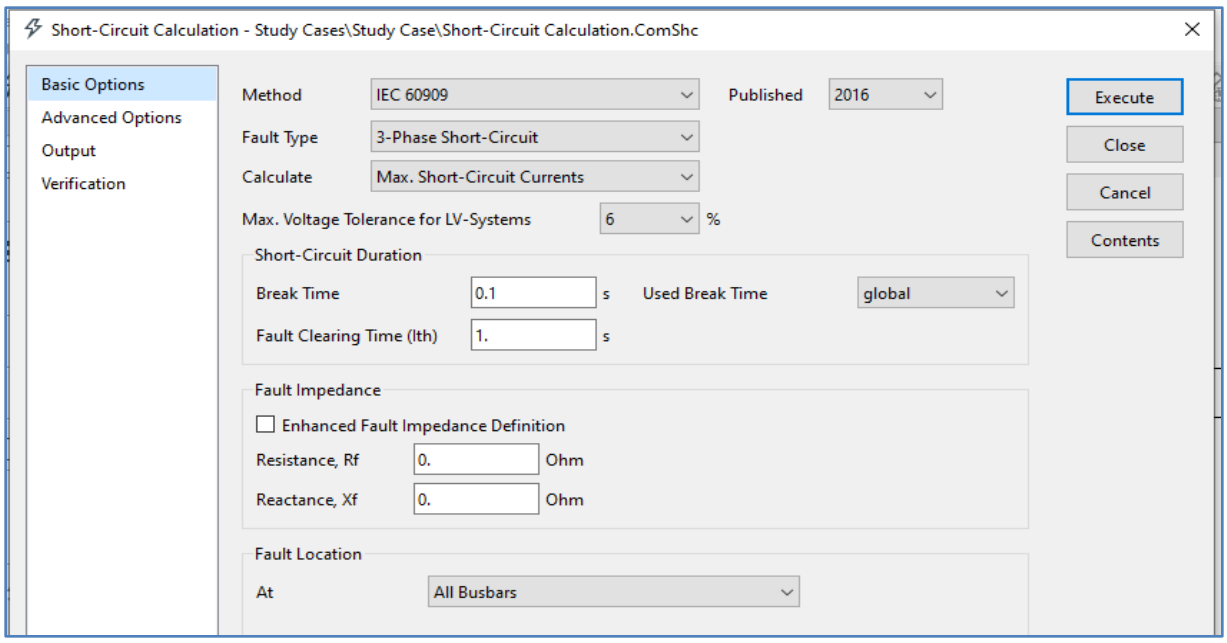

Figure 3.8. Use of three phase short circuits at bus 3

The external grid complex power rating is 1 000 MVA, as shown in Table 3.10, with a short circuit rating of 8.75 kA. As shown in Figure 3.8, the information is typically provided by the network (grid) provider and is specified on the application software. The arrangement accommodates both maximum and minimum short circuit current levels.

Table 3.10. Three phase maximum short circuit currents

							DIgSILENT PowerFactory 2020 SP1	Project:				
								Date: 5/15/2020				
Fault Locations with Feeders												
Short-Circuit Calculation / Method : IEC 60909						3-Phase Short-Circuit		/ Max. Short-Circuit Currents				
Asynchronous Motors		Grid Identification				Short-Circuit Duration						
Always Considered		Automatic				Break Time		0.10 s				
						Fault Clearing Time (Ith)		1.00 s				
Decaying Aperiodic Component (idc)		Conductor Temperature				Voltage factor c						
Using Method	B	User Defined	No			Standard defined table						
Grid: Grid		System Stage: Grid						Annex:	/ 1			
	rtd.V. [kV]	Voltage [kV]	[deg]	c-Factor	Sk" [MVA]		Ik" [kA]	[deg]	ip [kA]	Ib [kA]	Sb [MVA]	Ik [kA]	Ith [kA]
Bus 1	66.00	0.00	0.00	1.10	1000.00	MVA	8.75	-84.29	21.60	8.75	1000.00	8.75	8.90
TF 1	Bus 2				0.00	MVA	0.00	0.00	0.00				
External Grid					1000.00	MVA	8.75	-84.29	21.60				
Bus 2	144.90	0.00	0.00	1.10	732.35	MVA	2.92	-85.81	7.46	2.92	732.35	2.92	2.99
TF 1	Bus 1				732.35	MVA	2.92	94.19	7.46				
L 1	Bus 3				0.00	MVA	0.00	0.00	0.00				
Bus 3	144.90	0.00	0.00	1.10	600.30	MVA	2.39	-79.95	5.40	2.39	600.30	2.39	2.41
TF 2	Bus 4				0.00	MVA	0.00	0.00	0.00				
L 1	Bus 2				600.30	MVA	2.39	100.05	5.40				
Cap 1					0.00	MVA	0.00	0.00	0.00				
Bus 4	33.00	0.00	0.00	1.10	398.48	MVA	6.97	-83.33	16.86	6.97	398.48	6.97	7.07
TF 2	Bus 3				398.48	MVA	6.97	96.67	16.86				

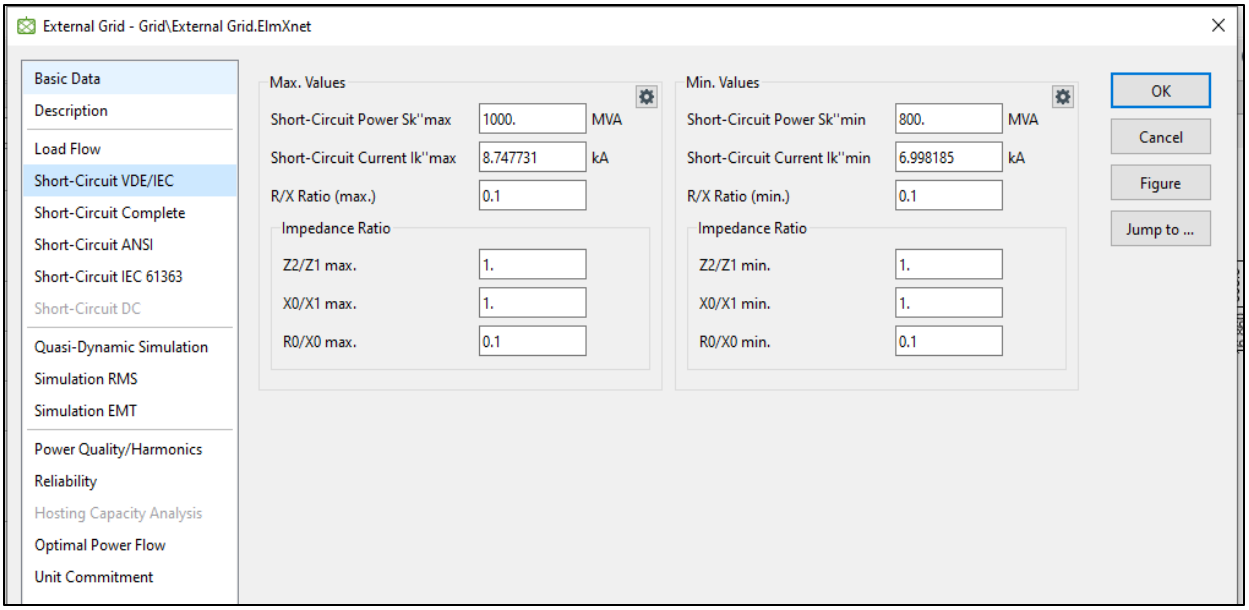

Figure 3.9. External grid short circuit rating

Table 3.11. Three phase minimum short circuit currents

			DIgSILENT PowerFactory 2020 SP1	Project:	
				Date: 5/15/2020	

Fault Locations with Feeders
Short-Circuit Calculation / Method : IEC 60909 — 3-Phase Short-Circuit / Min. Short-Circuit Currents

Asynchronous Motors	Grid Identification	Short-Circuit Duration
Always Considered	Automatic	Break Time 0.10 s
		Fault Clearing Time (Ith) 1.00 s
Decaying Aperiodic Component (idc)	Conductor Temperature	Voltage factor c
Using Method B	User Defined No	Standard defined table

Grid: Grid — System Stage: Grid — Annex: / 1

	rtd.V. [kV]	Voltage [kV]	[deg]	c-Factor	Sk" [MVA]	Ik" [kA]	[deg]	ip [kA]	Ib [kA]	Sb [MVA]	Ik [kA]	Ith [kA]
Bus 1	66.00	0.00	0.00	1.00	800.00 MVA	7.00 kA	-84.29	17.28 kA	7.00	800.00	7.00	7.12
TF 1	Bus 2				0.00 MVA	0.00 kA	0.00	0.00 kA				
External Grid					800.00 MVA	7.00 kA	-84.29	17.28 kA				
Bus 2	144.90	0.00	0.00	1.00	606.61 MVA	2.42 kA	-85.67	6.16 kA	2.42	606.61	2.42	2.47
TF 1	Bus 1				606.61 MVA	2.42 kA	94.33	6.16 kA				
L 1	Bus 3				0.00 MVA	0.00 kA	0.00	0.00 kA				
Bus 3	144.90	0.00	0.00	1.00	503.08 MVA	2.00 kA	-78.83	4.43 kA	2.00	503.08	2.00	2.02
TF 2	Bus 4				0.00 MVA	0.00 kA	0.00	0.00 kA				
L 1	Bus 2				503.08 MVA	2.00 kA	101.17	4.43 kA				
Cap 1					0.00 MVA	0.00 kA	0.00	0.00 kA				
Bus 4	33.00	0.00	0.00	1.00	343.26 MVA	6.01 kA	-82.39	14.24 kA	6.01	343.26	6.01	6.08
TF 2	Bus 3				343.26 MVA	6.01 kA	97.61	14.24 kA				

Tables 3.10 and 3.11 show the maximum and minimum short circuit currents for three phase faults on all bus terminals, respectively. The same analysis was performed for ground faults, which are important in this study because the equipment under

consideration is a grounded shunt capacitor bank. Tables 3.12 and 3.13 show the maximum and minimum short circuit currents for single phase to ground faults on all bus terminals, respectively.

After the short circuit investigations were completed, protection studies were carried out to calculate and test the capacitor bank system protection settings. The details of the computation procedure and testing are covered in the following sections.

Table 3.12. Maximum single-phase to ground short circuit currents

						DIgSILENT PowerFactory 2020 SP1	Project:							
							Date: 5/18/2020							
Fault Locations with Feeders														
Short-Circuit Calculation / Method : IEC 60909							Single Phase to Ground / Max. Short-Circuit Currents							
Asynchronous Motors			Grid Identification				Short-Circuit Duration							
Always Considered			Automatic				Break Time				0.10 s			
							Fault Clearing Time (Ith)				1.00 s			
			Conductor Temperature				Voltage factor c							
			User Defined		No		Standard defined table							
Grid: Grid			System Stage: Grid							Annex:		/ 1		
		rtd.V. [kV]	Voltage [kV]	[deg]	c-Factor		Sk" [MVA]	Ik" [kA]	[deg]	ip [kA]	Ib [kA]	Sb [MVA]	EFF [-]	
Bus 1	A	66.00	0.00	0.00	1.10		333.33 MVA	8.75 kA	-84.29	21.60 kA	8.75	333.33	0.00	
	B		41.92	-120.00			0.00 MVA	0.00 kA	0.00	0.00 kA	0.00	0.00	1.00	
	C		41.92	120.00			0.00 MVA	0.00 kA	0.00	0.00 kA	0.00	0.00	1.00	
TF 1			Bus 2			A	0.00 MVA	0.00 kA	0.00	0.00 kA				
						B	0.00 MVA	0.00 kA	0.00	0.00 kA				
						C	0.00 MVA	0.00 kA	0.00	0.00 kA				
External Grid						A	333.33 MVA	8.75 kA	-84.29	21.60 kA				
						B	0.00 MVA	0.00 kA	0.00	0.00 kA				
						C	0.00 MVA	0.00 kA	0.00	0.00 kA				
Bus 2	A	144.90	0.00	0.00	1.10		28.51 MVA	0.34 kA	-89.48	1.09 kA	0.34	28.51	0.00	
	B		150.56	-147.73			0.00 MVA	0.00 kA	0.00	0.00 kA	0.00	0.00	1.64	
	C		149.83	148.18			0.00 MVA	0.00 kA	0.00	0.00 kA	0.00	0.00	1.63	
TF 1			Bus 1			A	35.77 MVA	0.43 kA	90.42	1.09 kA				
						B	7.26 MVA	0.09 kA	90.03	0.22 kA				
						C	7.26 MVA	0.09 kA	90.03	0.22 kA				
L 1			Bus 3			A	7.26 MVA	0.09 kA	-89.97	0.00 kA				
						B	7.26 MVA	0.09 kA	-89.97	0.00 kA				
						C	7.26 MVA	0.09 kA	-89.97	0.00 kA				
Load 1						A	0.00 MVA	0.00 kA	0.00	0.00 kA				
						B	0.00 MVA	0.00 kA	0.00	0.00 kA				
						C	0.00 MVA	0.00 kA	0.00	0.00 kA				
Bus 3	A	144.90	0.00	0.00	1.10		27.54 MVA	0.33 kA	-88.07	0.93 kA	0.33	27.54	0.00	
	B		149.63	-147.00			0.00 MVA	0.00 kA	0.00	0.00 kA	0.00	0.00	1.63	
	C		147.71	148.17			0.00 MVA	0.00 kA	0.00	0.00 kA	0.00	0.00	1.61	
TF 2			Bus 4			A	0.09 MVA	0.00 kA	90.82	0.00 kA				
						B	0.09 MVA	0.00 kA	90.82	0.00 kA				
						C	0.09 MVA	0.00 kA	90.82	0.00 kA				
L 1			Bus 2			A	34.65 MVA	0.41 kA	91.70	0.93 kA				
						B	7.11 MVA	0.09 kA	90.82	0.19 kA				
						C	7.11 MVA	0.09 kA	90.82	0.19 kA				

Cap 1					A	7.20 MVA	0.09 kA	-89.18	0.00 kA				
					B	7.20 MVA	0.09 kA	-89.18	0.00 kA				
					C	7.20 MVA	0.09 kA	-89.18	0.00 kA				
Bus 4	A	33.00	0.00	0.00	1.10	14.04 MVA	0.74 kA	-89.02	1.78 kA	0.74	14.04	0.00	
	B		34.53	-147.85		0.00 MVA	0.00 kA	0.00	0.00 kA	0.00	0.00	1.65	
	C		34.29	148.48		0.00 MVA	0.00 kA	0.00	0.00 kA	0.00	0.00	1.64	
TF 2	Bus 3				A	14.04 MVA	0.74 kA	90.98	1.78 kA				
					B	0.00 MVA	0.00 kA	0.00	0.00 kA				
					C	0.00 MVA	0.00 kA	0.00	0.00 kA				
Load 2					A	0.00 MVA	0.00 kA	0.00	0.00 kA				
					B	0.00 MVA	0.00 kA	0.00	0.00 kA				
					C	0.00 MVA	0.00 kA	0.00	0.00 kA				

Table 3.13. Minimum single phase to ground short circuit currents

						DIgSILENT PowerFactory 2020 SP1	Project: Date: 5/18/2020						
Fault Locations with Feeders													
Short-Circuit Calculation / Method : IEC 60909							Single Phase to Ground / Min. Short-Circuit Currents						
Asynchronous Motors					Grid Identification				Short-Circuit Duration				
Always Considered					Automatic				Break Time		0.10 s		
									Fault Clearing Time (Ith)		1.00 s		
					Conductor Temperature				Voltage factor c				
					User Defined	No			Standard defined table				
Grid: Grid			System Stage: Grid						Annex:		/ 1		
		rtd.V. [kV]	Voltage [kV]	[deg]	c-Factor	Sk" [MVA]	Ik" [kA]	[deg]	ip [kA]	Ib [kA]	Sb [MVA]	EFF [-]	
Bus 1	A	66.00	0.00	0.00	1.00	266.67 MVA	7.00 kA	-84.29	17.28 kA	7.00	266.67	0.00	
	B		38.11	-120.00		0.00 MVA	0.00 kA	0.00	0.00 kA	0.00	0.00	1.00	
	C		38.11	120.00		0.00 MVA	0.00 kA	0.00	0.00 kA	0.00	0.00	1.00	
TF 1	Bus 2				A	0.00 MVA	0.00 kA	0.00	0.00 kA				
					B	0.00 MVA	0.00 kA	0.00	0.00 kA				
					C	0.00 MVA	0.00 kA	0.00	0.00 kA				
External Grid					A	266.67 MVA	7.00 kA	-84.29	17.28 kA				
					B	0.00 MVA	0.00 kA	0.00	0.00 kA				
					C	0.00 MVA	0.00 kA	0.00	0.00 kA				
Bus 2	A	144.90	0.00	0.00	1.00	26.09 MVA	0.31 kA	-89.39	0.99 kA	0.31	26.09	0.00	
	B		136.06	-147.48		0.00 MVA	0.00 kA	0.00	0.00 kA	0.00	0.00	1.63	
	C		135.31	147.98		0.00 MVA	0.00 kA	0.00	0.00 kA	0.00	0.00	1.62	
TF 1	Bus 1				A	32.63 MVA	0.39 kA	90.49	0.99 kA				
					B	6.54 MVA	0.08 kA	90.01	0.20 kA				
					C	6.54 MVA	0.08 kA	90.01	0.20 kA				
L 1	Bus 3				A	6.54 MVA	0.08 kA	-89.99	0.00 kA				
					B	6.54 MVA	0.08 kA	-89.99	0.00 kA				
					C	6.54 MVA	0.08 kA	-89.99	0.00 kA				
Load 1					A	0.00 MVA	0.00 kA	0.00	0.00 kA				
					B	0.00 MVA	0.00 kA	0.00	0.00 kA				
					C	0.00 MVA	0.00 kA	0.00	0.00 kA				
Cap 1					A	6.49 MVA	0.08 kA	-89.03	0.00 kA				
					B	6.49 MVA	0.08 kA	-89.03	0.00 kA				
					C	6.49 MVA	0.08 kA	-89.03	0.00 kA				
Bus 4	A	33.00	0.00	0.00	1.00	12.80 MVA	0.67 kA	-88.81	1.59 kA	0.67	12.80	0.00	
	B		31.31	-147.68		0.00 MVA	0.00 kA	0.00	0.00 kA	0.00	0.00	1.64	
	C		31.06	148.43		0.00 MVA	0.00 kA	0.00	0.00 kA	0.00	0.00	1.63	
TF 2	Bus 3				A	12.80 MVA	0.67 kA	91.19	1.59 kA				
					B	0.00 MVA	0.00 kA	0.00	0.00 kA				
					C	0.00 MVA	0.00 kA	0.00	0.00 kA				
Load 2					A	0.00 MVA	0.00 kA	0.00	0.00 kA				
					B	0.00 MVA	0.00 kA	0.00	0.00 kA				
					C	0.00 MVA	0.00 kA	0.00	0.00 kA				

Both hand calculations and software methods were used to accomplish short circuit calculations. These results are used to calculate protection settings, which will be described further next.

3.4 Protection settings calculations

This section of the chapter elaborates through the mathematical method used to calculate backup protection settings. As a backup, overcurrent protection for all ground related faults with zero-sequence components and over/under voltage protection for three phase short circuits are used. The two protection techniques are utilized for system protection, whereas bank protection (protection within the capacitor bank) is covered in Chapter 5. Following that is a discussion on overcurrent protection.

3.4.1 Voltage differential protection

Since a voltage differential protection algorithm is not supported by the DIGSILENT simulation program. DIGSILENT vendor may develop a voltage differential algorithm for the SEL 487V relay as part of their future effort. Meanwhile, the project work consists of lab-scale implementation, testing, and modelling of the voltage differential system using a SEL487V relay and an Omicron test injection device, as described in Chapter 5 which provides engineering and configuration of lab scale setup and Chapter 6 which discusses test results of the lab scale implementation. As a result, this section of the project only includes the backup protection configuration settings and simulation results for overcurrent, overvoltage, and undervoltage protection functions.

3.4.2 Overcurrent protection

The mathematical method used is based on recommendations from other scholars. The voltage on bus 3 is 0.97 p.u. (140.9 kV) with a current of 80 A and injecting 19.5 MVar during typical operating conditions, as determined by load flow results. The following formula can be used to calculate the capacitor bank's current rating:

$$I_{rcap} = \frac{Q_r}{\sqrt{3}\, x\, U_n} \qquad 3.2$$

Whereby,

I_{rcap} Rated capacitor bank current at voltage and reactive power rating

Q_r Rated reactive power of the capacitor bank

U_n Rated voltage of the capacitor bank

Equation 3.2 calculation yields,

$I_{rcap} = \frac{22000000}{\sqrt{3}\, x\, 144900}$ = 87.66 A = 88 A

As previously noted, the capacitor bank is injecting 80 A into the network, which is standard network operation. As a result, the capacitor bank current injected into the network will be used to calculate the overcurrent protection scheme's protection parameters.

Overcurrent Stage 1 Element = 1.2 x I_{norm}

Whereby,

I_{norm} Capacitor bank current during normal operating conditions

The 1.2 is to ensure that the relay does not trip on overload.

Therefore,

Stage 1 (50 P1) = 1.2 x 80 = 96 A (primary)

Overcurrent Stage 2 Element (50 P2) = 1.35 x I_{norm}

Stage 2 = 1.35 x 88 = 108 A (primary)

Overcurrent Stage 3 Element = 3 x Stage 2

Stage 3 = 3 x 119 = 324 A (primary)

The diagrams of the protection flow chart and decision-making are shown in Figure 3.10. It should be noted in the diagram that both the capacitor bank current and the bus voltage are continuously checked to ensure that no thresholds are exceeded. The flow chart diagram demonstrates that there are no threshold deviations on both current and voltage, indicating that the system is operating normally. If a violation occurs, a check of which violation happened is performed, and the corresponding delay is applied, which may result in a breaker trip or the delay being reset.

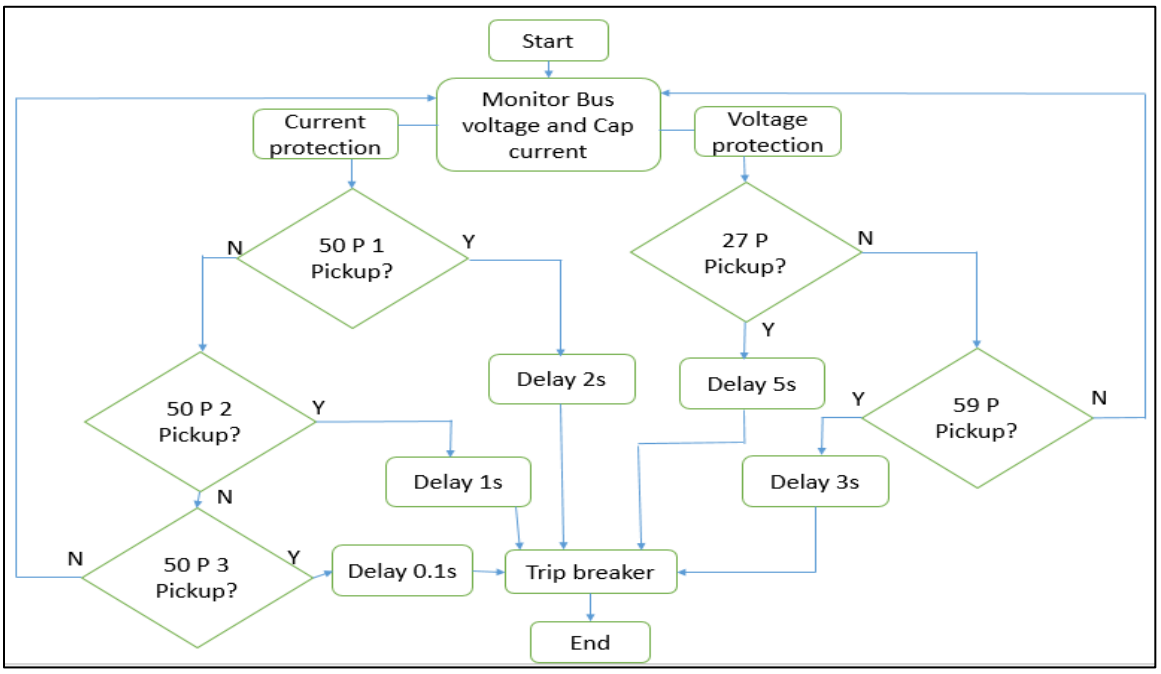

Figure 3.10. Flowchart of the procedure of configuring capacitor bank protection relays

The estimated current values above are to be used to the DIGSILENT software package's relay simulation model. For this purpose, a Schweitzer Engineering Laboratories (SEL) 751-A feeder protection relay model with a secondary CT rating of 1 A is used. The CT ratio of the current transformer installed on the feeder is 100/1.

Figure 3.11 depicts the relay model and settings configuration on the software package.

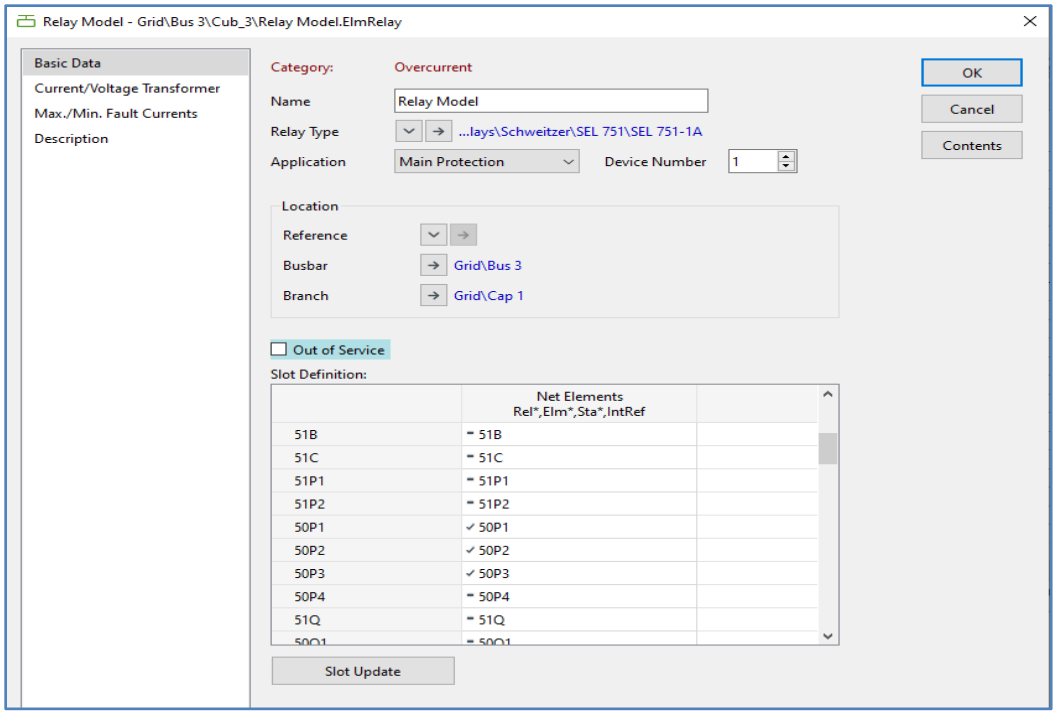

Figure 3.11. Overcurrent relay model for SEL751-A feeder protection relay

The settings described are then transformed to secondary values.

Stage 1 = 96 x 0.01 = 0.96

Stage 2 = 108 x 0.01 = 1.08

Stage 3 = 324 x 0.01 = 3.24

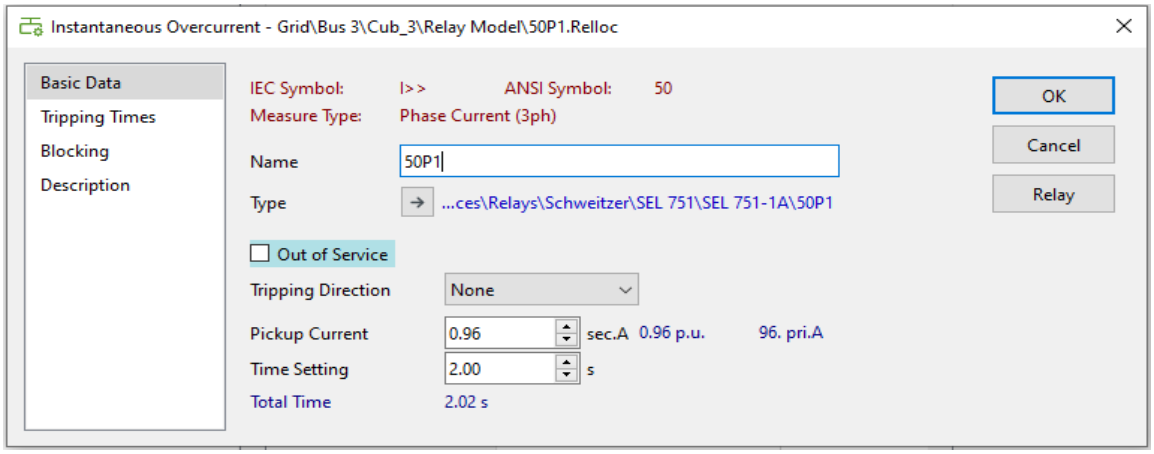

Figure 3.12. Configuration of overcurrent protection elements

The configuration of overcurrent elements on the application software is shown in Figure 3.12. The times associated with the calculated pickup currents are as follows and are presented in Table 3.14.

0.96 pickup = 2 seconds delay

1.08 pickup = 1 second delay

3.24 pickup = 0.1 seconds delays (100 millisecond)

Table 3.14. Overcurrent element settings

	Protection Devi...	Location	Branch	Manufacturer	Model	Stage (Phase)	Current [pri.A]	Current [sec.A]	Current [p.u.]	Time	Characteristic	Directional
▸ 1	Relay Model	Bus 3		Schweitzer	SEL 751-1A	50P1	96	0.96	0.96	2.00	Definite	None
						50P2	108	1.08	1.08	1.00	Definite	None
						50P3	324	3.24	3.24	0.10	Definite	None

Table 3.15. The protection functions report stage 1 tripping

```
----------------------------------------------------------------------------------------------------
|              |                                                   |   DIgSILENT   | Project:        |
|              |                                                   | PowerFactory  |-----------------
|              |                                                   |   2020 SP1B   | Date:  6/20/2020 |
----------------------------------------------------------------------------------------------------
----------------------------------------------------------------------------------------------------
| Relays Detailed                                                                                   |
| Short-Circuit Calculation / Method : IEC 60909         Single Phase to Ground  / Max. Short-Circuit Currents |
----------------------------------------------------------------------------------------------------
| Asynchronous Motors              | Grid Identification              | Short-Circuit Duration          |
|    Always Considered             |    Automatic                     |    Break Time              0.10 s |
|                                  |                                  |    Fault Clearing Time (Ith) 1.00 s |
|                                  | Conductor Temperature            | Voltage factor c                |
|                                  |    User Defined          No      |    Standard defined table       |
|                                  |                                  |                                 |
----------------------------------------------------------------------------------------------------
----------------------------------------------------------------------------------------------------
| Grid: Grid           System Stage: Grid       | Study Case: Study Case        | Annex:          / 1 |
----------------------------------------------------------------------------------------------------
----------------------------------------------------------------------------------------------------
| Relay Model                    Relay Type : SEL 751-1A                                            |
|  Ct     : CT 1                 Location   : Busbar     : Bus 3        /       Ratio      : 100A/1A |
|                                             Branch     : Cap 1                Connection : Y      |
|                                                        :                                          |
|  CoreCt: CT 1                  Location   : Busbar     : Bus 3        /       Ratio      : 100A/1A |
|                                             Branch     : Cap 1                Connection : Y      |
|                                                        :                                          |
|  Vt     : VT 1                 Location   : Busbar     : Bus 3        /       Ratio      : 144900V/100V |
|                                             Branch     :                                 :   - Y   |
|  50P1     : 50P1             ( IEC: I>>  ANSI: 50   )   Tripping Current    [pri.A]    Tripping Time |
|    Pickup Current  :  0.960 sec.A    96.00 pri.A   0.960 p.u.   A :   1.014   101.42    2.020 s   |
|    Time Setting    :  2.000 s                                  B :   1.014   101.42              |
|    Total Time      :  2.020 s                                  C :   1.014   101.42              |
|  50P2     : 50P2             ( IEC: I>>  ANSI: 50   )   Tripping Current    [pri.A]    Tripping Time |
|    Pickup Current  :  1.080 sec.A   108.00 pri.A   1.080 p.u.   A :   1.014   101.42    9999.999 s |
|    Time Setting    :  1.000 s                                  B :   1.014   101.42              |
|    Total Time      :  1.020 s                                  C :   1.014   101.42              |
| Grid: Grid           System Stage: Grid       | Study Case: Study Case        | Annex:          / 2 |
----------------------------------------------------------------------------------------------------
----------------------------------------------------------------------------------------------------
|  50P3     : 50P3             ( IEC: I>>  ANSI: 50   )   Tripping Current    [pri.A]    Tripping Time |
|    Pickup Current  :  3.240 sec.A   324.00 pri.A   3.240 p.u.   A :   1.014   101.42    9999.999 s |
|    Time Setting    :  0.100 s                                  B :   1.014   101.42              |
|    Total Time      :  0.120 s                                  C :   1.014   101.42              |
|  Logic      : Logic                                                            :                 |
|    Breaker          Cubicle      Branch          Busbar        / Substation    Fault Clearing Time |
|                                                                /                                  |
|  Closing Logiclosing Logic                      :                               :                 |
|    Breaker          Cubicle      Branch          Busbar        / Substation    Fault Clearing Time |
|                                                                /                                  |
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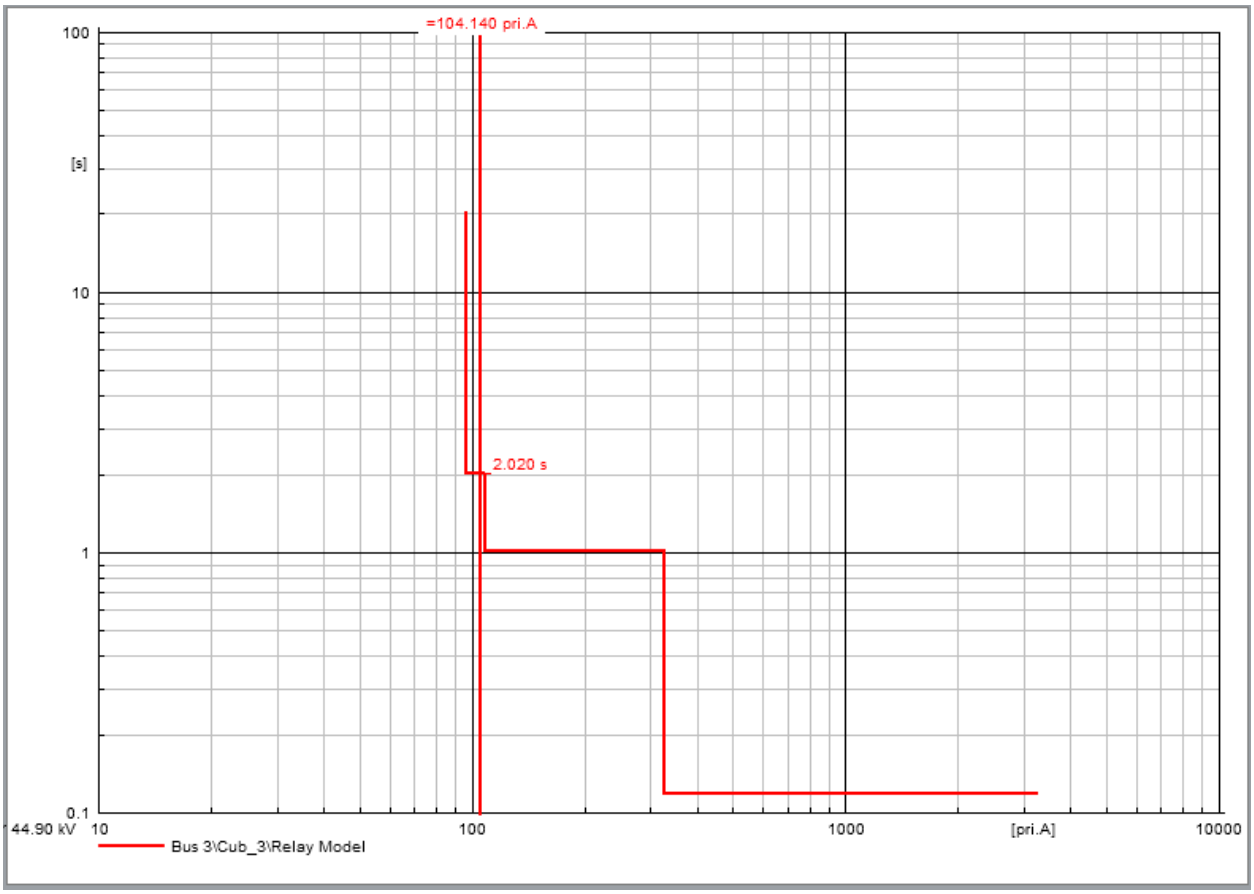

Figure 3.13. Stage 1 element tripping

Table 3.14 depicts the various levels of overcurrent protection (stage 1, stage 2 and stage 3). As previously stated, various faults at various locations were used to test all protection levels and their tripping times. A fault that led to 101 A is indicated in Figure 3.13, a primary current was recorded, the stage 1 element was picked up, and the breaker tripped after 2.020 seconds. This is consistent with the settings made to the relay model, and the relay is functioning properly according to the setup.

Table 3.15 displays a protection functions report with relay tripping times. It can be seen that just the first stage element takes up and sends out a trip signal. The report displays relay settings such as CT ratio, stage 1 to 3 element settings, appropriate time delays, and so on.

Figure 3.14 shows simulations of voltage and current waveforms using a short circuit that triggered the stage 2 element. The current waveform shows that the peak value climbed

to almost double the nominal value and that a delay of just over 1 second was applied before the breaker tripped. This is triggered by a single phase to ground fault on bus 3, which picked up the stage 2 element, causing the relay to trip and all breaker poles to open after 1.052 seconds, as illustrated in Figure 3.15. The figure is known as the Definite Minimum Time (DMT) Overcurrent curve, and it just monitors the pickup value and applies a fixed time delay after which a trip is sent. Figure 3.16 depicts the network as a single line with the capacitor bank breaker open after the problem occurred.

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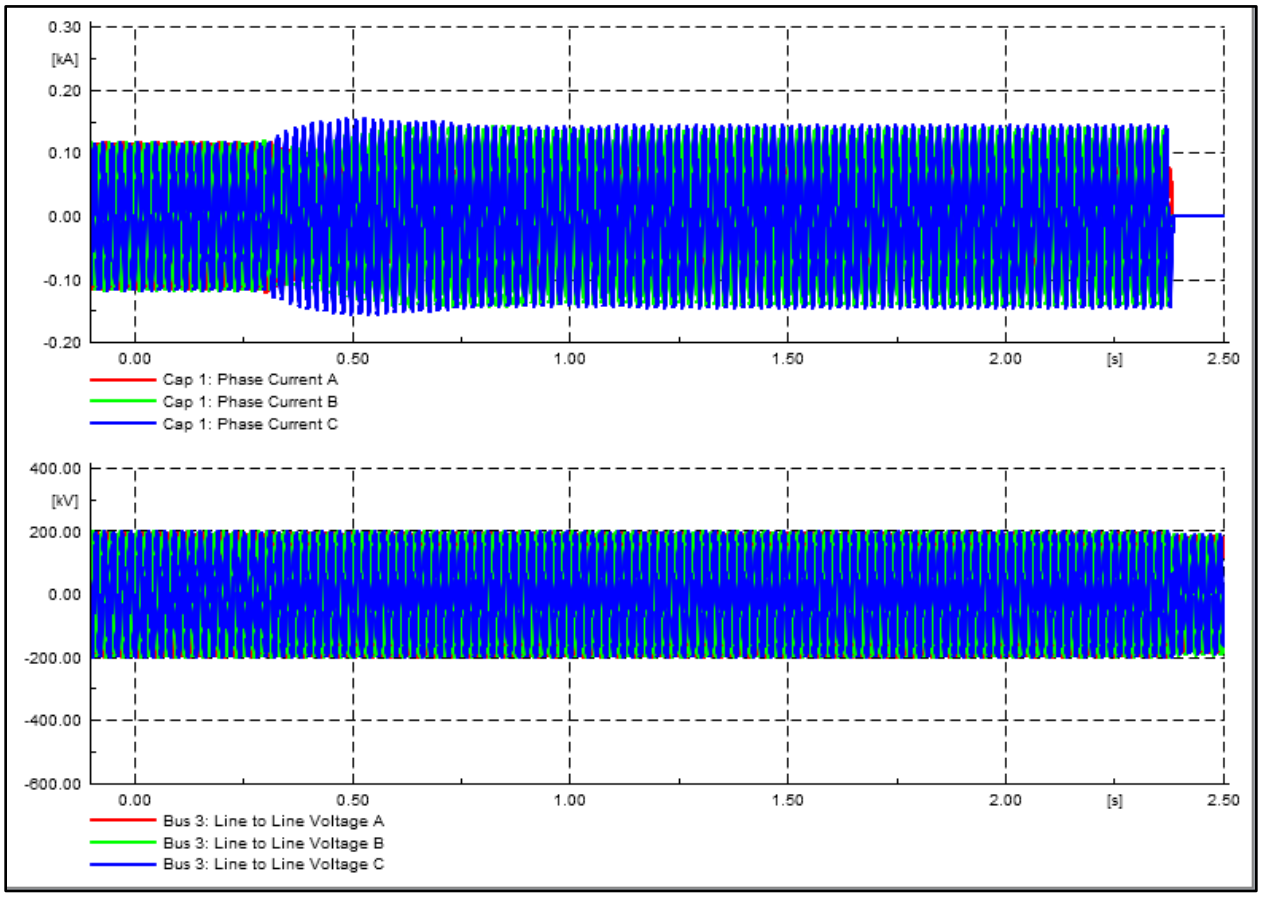

Figure 3.14. Single phase voltage and current waveforms to ground fault on bus 3

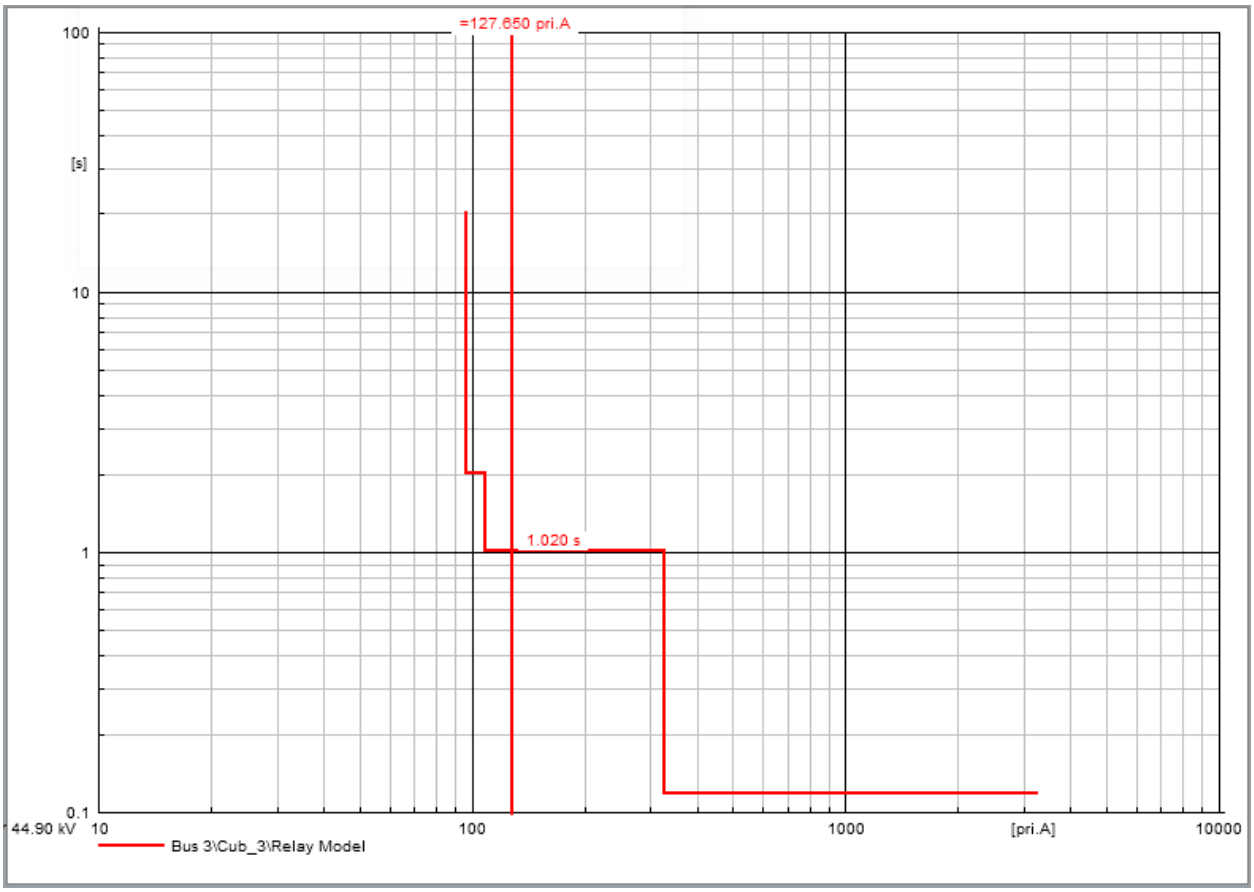

Figure 3.15. Stage 2 element tripping

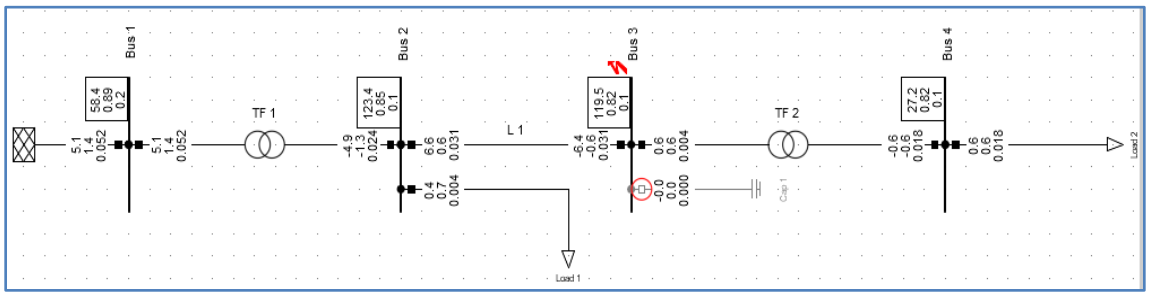

Figure 3.16. Single line representation with the capacitor bank breaker open

As shown in Table 3.16, a protection settings report is generated. When the measured current exceeds 115 A, both stage 1 and stage 2 elements pick up; however, the stage 2 element provides a trip signal before the stage 1 element, causing the breaker to trip in 1.020 seconds.

Table 3.16. The protection functions report stage 2 tripping

		DIgSILENT PowerFactory 2020 SP1B	Project: Date: 6/20/2020

Relays Detailed			
Short-Circuit Calculation / Method : IEC 60909		Single Phase to Ground	/ Max. Short-Circuit Currents
Asynchronous Motors	Grid Identification	Short-Circuit Duration	
Always Considered	Automatic	Break Time	0.10 s
		Fault Clearing Time (Ith)	1.00 s
	Conductor Temperature	Voltage factor c	
	User Defined No	Standard defined table	

Grid: Grid	System Stage: Grid	Study Case: Study Case	Annex: / 1

Relay Model	Relay Type : SEL 751-1A							
Ct : CT 1	Location : Busbar	: Bus 3	/		Ratio	: 100A/1A		
	Branch	: Cap 1			Connection	: Y		
		:						
CoreCt: CT 1	Location : Busbar	: Bus 3	/		Ratio	: 100A/1A		
	Branch	: Cap 1			Connection	: Y		
		:						
Vt : VT 1	Location : Busbar	: Bus 3	/		Ratio	: 144900V/100V		
	Branch	:				: - Y		
50P1 : 50P1	(IEC: I>>	ANSI: 50)	Tripping Current		[pri.A]	Tripping Time		
Pickup Current :	0.960 sec.A	96.00 pri.A	0.960 p.u.	A :	1.277	127.65	2.020 s	
Time Setting :	2.000 s			B :	1.277	127.65		
Total Time :	2.020 s			C :	1.277	127.65		
50P2 : 50P2	(IEC: I>>	ANSI: 50)	Tripping Current		[pri.A]	Tripping Time		
Pickup Current :	1.080 sec.A	108.00 pri.A	1.080 p.u.	A :	1.277	127.65	1.020 s	
Time Setting :	1.000 s			B :	1.277	127.65		
Total Time :	1.020 s			C :	1.277	127.65		

Grid: Grid	System Stage: Grid	Study Case: Study Case	Annex: / 2

50P3 : 50P3	(IEC: I>>	ANSI: 50)	Tripping Current		[pri.A]	Tripping Time		
Pickup Current :	3.240 sec.A	324.00 pri.A	3.240 p.u.	A :	1.277	127.65	9999.999 s	
Time Setting :	0.100 s			B :	1.277	127.65		
Total Time :	0.120 s			C :	1.277	127.65		
Logic : Logic						:		
Breaker	Cubicle	Branch	Busbar	/ Substation		Fault Clearing Time		
				/				
Closing Logiclosing Logic		:				:		
Breaker	Cubicle	Branch	Busbar	/ Substation		Fault Clearing Time		
				/				

Figure 3.17 depicts a fault simulation that results in a stage 3 element picking up at a measured current of 364 A and a breaker tripping after 120 milliseconds. According to the DMT curve, the breaker trips after 120 milliseconds. The protective functions report for stage 3 element simulation is also generated and is shown in Table 3.17. When element 3 trips, all elements pick up, however the stage 3 element sends a trip signal before the stage 1 and stage 2 elements, causing the breaker to trip in 120 milliseconds.

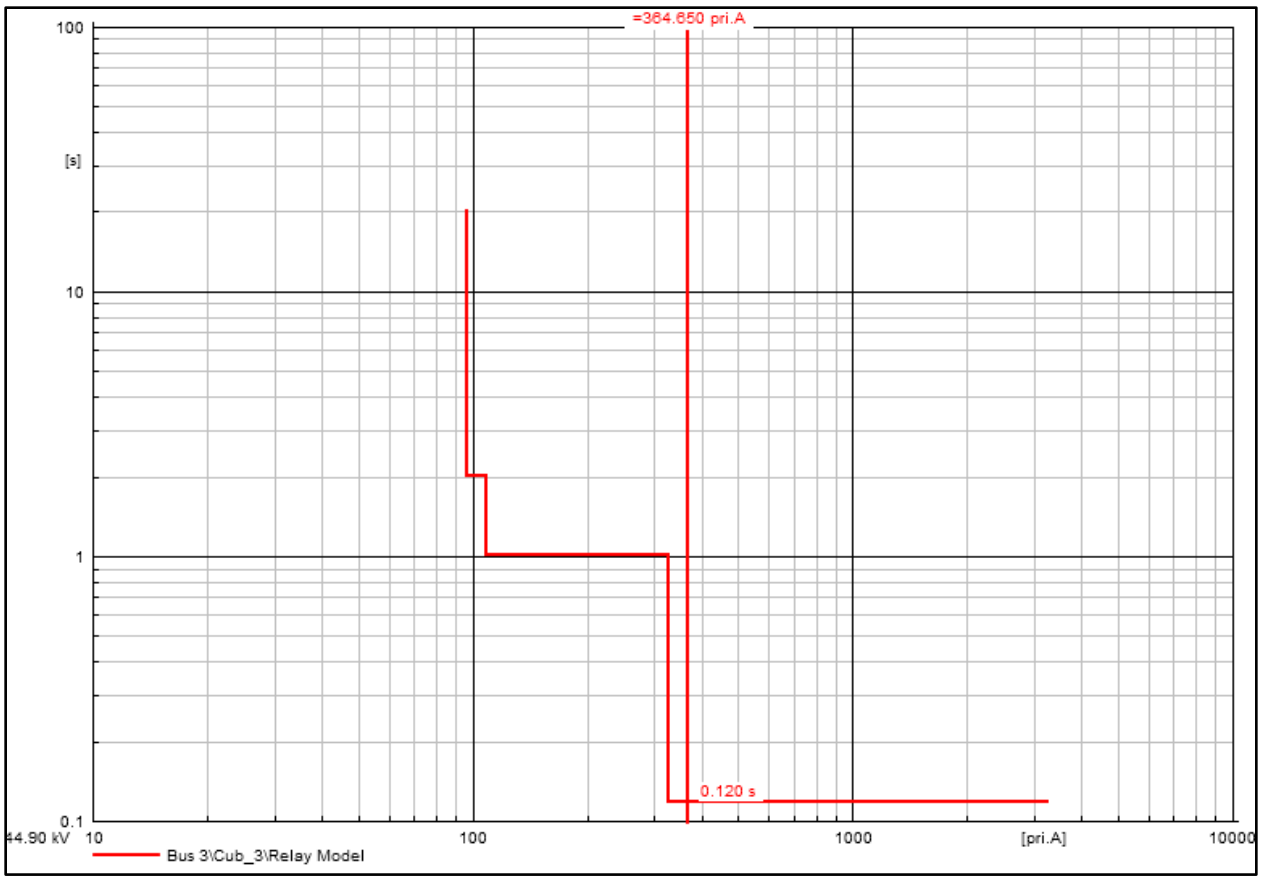

Figure 3.17. Stage 3 element tripping

Table 3.17. The protection functions report stage 3 tripping

						DIgSILENT PowerFactory 2020 SP1B	Project:		
							Date: 6/20/2020		
Relays Detailed									
Short-Circuit Calculation / Method : IEC 60909						Single Phase to Ground	/ Max. Short-Circuit Currents		
Asynchronous Motors		Grid Identification				Short-Circuit Duration			
Always Considered		Automatic				Break Time		0.10 s	
						Fault Clearing Time (Ith)		1.00 s	
		Conductor Temperature				Voltage factor c			
		User Defined		No		Standard defined table			
Grid: Grid	System Stage: Grid				Study Case: Study Case		Annex:		/ 1
Relay Model		Relay Type : SEL 751-1A							
Ct : CT 1		Location : Busbar	: Bus 3		/		Ratio	: 100A/1A	
		Branch	: Cap 1				Connection	: Y	
			:						
CoreCt: CT 1		Location : Busbar	: Bus 3		/		Ratio	: 100A/1A	
		Branch	: Cap 1				Connection	: Y	
			:						
Vt : VT 1		Location : Busbar	: Bus 3		/		Ratio	: 144900V/100V	
		Branch	:					: - Y	
50P1 : 50P1		(IEC: I>> ANSI: 50)			Tripping Current	[pri.A]		Tripping Time	
Pickup Current :	0.960 sec.A	96.00 pri.A	0.960 p.u.		A :	3.644	364.45	2.020 s	
Time Setting :	2.000 s				B :	3.644	364.45		
Total Time :	2.020 s				C :	3.644	364.45		
50P2 : 50P2		(IEC: I>> ANSI: 50)			Tripping Current	[pri.A]		Tripping Time	
Pickup Current :	1.080 sec.A	108.00 pri.A	1.080 p.u.		A :	3.644	364.45	1.020 s	
Time Setting :	1.000 s				B :	3.644	364.45		
Total Time :	1.020 s				C :	3.644	364.45		

Grid: Grid	System Stage: Grid	Study Case: Study Case	Annex: / 2

50P3 : 50P3	(IEC: I>> ANSI: 50)		Tripping Current	[pri.A]	Tripping Time	
Pickup Current :	3.240 sec.A	324.00 pri.A 3.240 p.u.	A :	3.644	364.45	0.120 s
Time Setting :	0.100 s		B :	3.644	364.45	
Total Time :	0.120 s		C :	3.644	364.45	
Logic : Logic					:	
Breaker	Cubicle	Branch	Busbar	/ Substation /	Fault Clearing Time	
Closing Logiclosing Logic		:			:	
Breaker	Cubicle	Branch	Busbar	/ Substation /	Fault Clearing Time	

All of the overcurrent settings have been tested and have performed as expected. It should be noticed that the faults that tripped the relay are all ground faults. For grounded capacitor banks, phase overcurrent prevention does not cover errors with non-zero-sequence components. The next section discusses an extra protection system for three phase faults or other failures that do not have zero-sequence components.

3.4.3 Over/Under voltage protection

Capacitor bank overcurrent protection is insufficient since it does not cover all or the majority of network problems. Voltage-related protection systems are advised as an extra safeguard against nonzero-sequence component defects. The under-voltage element will care for short circuits that cause voltages to decrease to less than a pre-set value, whilst the over-voltage element will safeguard the capacitor bank or the system from extreme overvoltages on the system. Figure 3.19 depicts a three-phase short circuit applied to bus 4, resulting in a voltage drop of 54.1 kV on Bus 3.

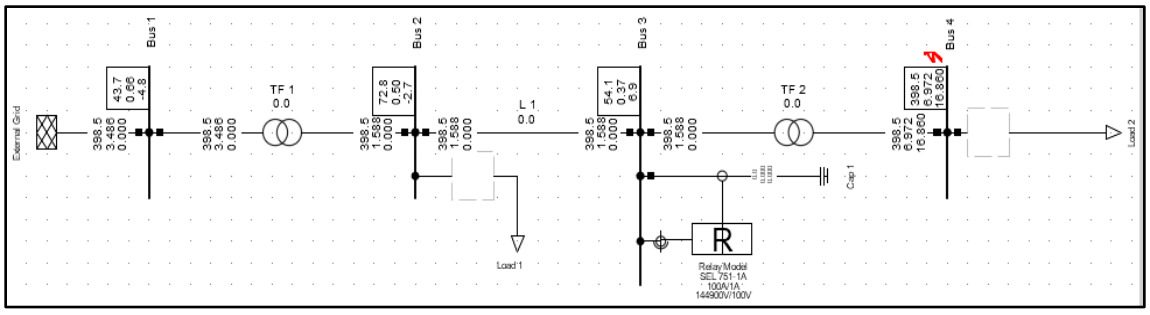

Figure 3.18. Bus 4 is experiencing a three-phase fault.

Table 3.18 displays the protection functions report, which demonstrates that no elements are tripping because no zero-sequence component is involved.

Table 3.18. The protection functions report with no element tripping

```
------------------------------------------------------------------------------------------------------------------------------
|               |                                                           |   DIgSILENT  | Project:                      |
|               |                                                           | PowerFactory |-------------------------------
|               |                                                           |    2020 SP1B | Date:  6/20/2020              |
------------------------------------------------------------------------------------------------------------------------------
------------------------------------------------------------------------------------------------------------------------------
| Relays Detailed                                                                                                            |
| Short-Circuit Calculation / Method : IEC 60909                            3-Phase Short-Circuit    / Max. Short-Circuit Currents |
------------------------------------------------------------------------------------------------------------------------------
| Asynchronous Motors                  | Grid Identification                   | Short-Circuit Duration                         |
|    Always Considered                 |    Automatic                          |    Break Time                        0.10 s    |
|                                      |                                       |    Fault Clearing Time (Ith)         1.00 s    |
| Decaying Aperiodic Component (idc)   | Conductor Temperature                 | Voltage factor c                               |
|    Using Method               B      |    User Defined          No           |    Standard defined table                      |
|                                      |                                       |                                                |
------------------------------------------------------------------------------------------------------------------------------
------------------------------------------------------------------------------------------------------------------------------
| Grid: Grid               System Stage: Grid          | Study Case: Study Case              | Annex:                   / 1  |
------------------------------------------------------------------------------------------------------------------------------
------------------------------------------------------------------------------------------------------------------------------
| Relay Model                       Relay Type : SEL 751-1A                                                                  |
|   Ct    : CT 1                    Location   : Busbar      : Bus 3         /                Ratio      : 100A/1A          |
|                                                Branch      : Cap 1                           Connection : Y                |
|                                                            :                                                               |
|   CoreCt: CT 1                    Location   : Busbar      : Bus 3         /                Ratio      : 100A/1A          |
|                                                Branch      : Cap 1                           Connection : Y                |
|                                                            :                                                               |
|   Vt    : VT 1                    Location   : Busbar      : Bus 3         /                Ratio      : 144900V/100V     |
|                                                Branch      :                                            :   - Y           |
|   50P1    : 50P1                  ( IEC: I>>   ANSI: 50   )     Tripping Current      [pri.A]        Tripping Time       |
|     Pickup Current  :  0.960 sec.A     96.00 pri.A   0.960 p.u.    A :    0.000         0.00           9999.999 s         |
|     Time Setting    :  2.000 s                                     B :    0.000         0.00                              |
|     Total Time      :  2.020 s                                     C :    0.000         0.00                              |
|   50P2    : 50P2                  ( IEC: I>>   ANSI: 50   )     Tripping Current      [pri.A]        Tripping Time       |
|     Pickup Current  :  1.080 sec.A    108.00 pri.A   1.080 p.u.    A :    0.000         0.00           9999.999 s         |
|     Time Setting    :  1.000 s                                     B :    0.000         0.00                              |
|     Total Time      :  1.020 s                                     C :    0.000         0.00                              |
| Grid: Grid               System Stage: Grid          | Study Case: Study Case              | Annex:                   / 2  |
------------------------------------------------------------------------------------------------------------------------------
------------------------------------------------------------------------------------------------------------------------------
|   50P3    : 50P3                  ( IEC: I>>   ANSI: 50   )     Tripping Current      [pri.A]        Tripping Time       |
|     Pickup Current  :  3.240 sec.A    324.00 pri.A   3.240 p.u.    A :    0.000         0.00           9999.999 s         |
|     Time Setting    :  0.100 s                                     B :    0.000         0.00                              |
|     Total Time      :  0.120 s                                     C :    0.000         0.00                              |
|   Logic      : Logic                                                                                   :                 |
|     Breaker          Cubicle      Branch                Busbar                 / Substation       Fault Clearing Time      |
|                                                                               /                                            |
|   Closing Logiclosing Logic                     :                                                       :                 |
|     Breaker          Cubicle      Branch                Busbar                 / Substation       Fault Clearing Time      |
|                                                                               /                                            |
------------------------------------------------------------------------------------------------------------------------------
```

The pickup value for overvoltage setting is 10% higher than the nominal voltage. If the bus voltage exceeds 159.39 kV for more than 3 seconds, the capacitor bank will be removed. The 3 second delay enables for the filtering of any noise or transients that may occur on the network. The removal of the capacitor bank from the system protects the capacitor bank from harmful overvoltage effects and also allows the voltage to drop in the vicinity of the installation, thereby protecting the system and the equipment on the system from experiencing excessive over voltages for extended periods of time. The setting of voltage elements on DIGSILENT software is shown in Table 3.19. The under voltage is used to trip the bank in the event of a loss of system voltage, and it is time-delayed allowing for parallel fault clearance and other transient voltage excursions. To minimize early disconnection of the capacitor bank when the network requires voltage support, a two-level strategy will be employed for undervoltage: 1. 90 percent and 2. 80 percent of

nominal voltage value. Time delays of 10 seconds and 5 seconds, respectively, are also advised to provide transient filtering while providing the necessary network support.

Table 3.19. Configuration settings for undervoltage and overvoltage protection

	Protection Devi...	Location	Branch	Manufacturer	Model	Stage (Phase)	Voltage [pri.V]	Voltage [sec.V]	Voltage [p.u.]	Time	Characteristic
▶ 1	Relay Model	Bus 3		Schweitzer	SEL 751-1A	27P1	130410	90.00	0.60	10.00	Definite
						27P2	115195	79.50	0.53	5.00	Definite
						59P1	158666	109.50	0.73	3.00	Definite

Following the installation of the voltage protection devices, a three-phase fault is applied to bus 4. Table 3.20 displays the protective functions report, which shows an undervoltage element picking up and issuing a trip after 5 seconds. Figure 3.19 depicts the identical scenario with a snapshot in which a trip signal was issued and the breaker tripped after 5 seconds (5.042).

Table 3.20. The undervoltage element tripping is reported by protection functions

```
-----------------------------------------------------------------------------------------------------------------
|                 |                                                          |   DIgSILENT   | Project:          |
|                 |                                                          | PowerFactory  |-------------------
|                 |                                                          |   2020 SP1B   | Date:  5/31/2020  |
-----------------------------------------------------------------------------------------------------------------
-----------------------------------------------------------------------------------------------------------------
| Relays Detailed                                                                                                 |
| Short-Circuit Calculation / Method : IEC 60909                 3-Phase Short-Circuit    / Max. Short-Circuit Currents |
-----------------------------------------------------------------------------------------------------------------
| Asynchronous Motors                   | Grid Identification                     | Short-Circuit Duration         |
|    Always Considered                  |    Automatic                            |    Break Time              0.10 s |
|                                       |                                         |    Fault Clearing Time (Ith) 1.00 s |
| Decaying Aperiodic Component (idc)    | Conductor Temperature                   | Voltage factor c               |
|    Using Method               B       |    User Defined            No           |    Standard defined table      |
|                                       |                                         |                                |
-----------------------------------------------------------------------------------------------------------------
-----------------------------------------------------------------------------------------------------------------
| Grid: Grid            System Stage: Grid        | Study Case: Study Case        | Annex:                 / 1  |
-----------------------------------------------------------------------------------------------------------------
-----------------------------------------------------------------------------------------------------------------
| Relay Model                  Relay Type : SEL 751-1A                                                            |
|   Ct     : CT 1              Location   : Busbar      : Bus 3         /             Ratio      : 100A/1A       |
|                                           Branch      : Cap 1                        Connection : Y             |
|                                                       :                                                         |
|   CoreCt: CT 1               Location   : Busbar      : Bus 3         /             Ratio      : 100A/1A       |
|                                           Branch      : Cap 1                        Connection : Y             |
|                                                       :                                                         |
|   Vt     : VT 1              Location   : Busbar      : Bus 3         /             Ratio      : 144900V/110V  |
|                                           Branch      :                                         :   - Y         |
|   50P1    : 50P1               ( IEC: I>>  ANSI: 50   )     Tripping Current     [pri.A]      Tripping Time    |
|     Pickup Current  :   1.060 sec.A   106.00 pri.A   1.060 p.u.   A :   0.000       0.00        9999.999 s     |
|     Time Setting    :   2.000 s                                   B :   0.000       0.00                       |
|     Total Time      :   2.020 s                                   C :   0.000       0.00                       |
|   50P2    : 50P2               ( IEC: I>>  ANSI: 50   )     Tripping Current     [pri.A]      Tripping Time    |
|     Pickup Current  :   1.190 sec.A   119.00 pri.A   1.190 p.u.   A :   0.000       0.00        9999.999 s     |
|     Time Setting    :   1.000 s                                   B :   0.000       0.00                       |
|     Total Time      :   1.020 s                                   C :   0.000       0.00                       |
-----------------------------------------------------------------------------------------------------------------
-----------------------------------------------------------------------------------------------------------------
| Grid: Grid            System Stage: Grid        | Study Case: Study Case        | Annex:                 / 2  |
-----------------------------------------------------------------------------------------------------------------
-----------------------------------------------------------------------------------------------------------------
|   50P3    : 50P3               ( IEC: I>>  ANSI: 50   )     Tripping Current     [pri.A]      Tripping Time    |
|     Pickup Current  :   3.570 sec.A   357.00 pri.A   3.570 p.u.   A :   0.000       0.00        9999.999 s     |
|     Time Setting    :   0.100 s                                   B :   0.000       0.00                       |
|     Total Time      :   0.120 s                                   C :   0.000       0.00                       |
|   Logic     : Logic                                                           yout          :    5.020 s     |
|     Breaker         Cubicle      Branch               Busbar           / Substation     Fault Clearing Time  |
|                                                                         /                                     |
|   Closing Logiclosing Logic       Tripping Block:                            Tripping      :  9999.999 s     |
|     Breaker         Cubicle      Branch               Busbar           / Substation     Fault Clearing Time  |
|                                                                         /                                     |
-----------------------------------------------------------------------------------------------------------------
```

```
(t=010:000 ms) ------------------------------------------------------------
(t=010:000 ms) 'Grid\Bus 4.ElmTerm':
(t=010:000 ms) 3-Phase Short-Circuit.
(t=010:000 ms) with Fault Impedance Rf = 0.000000 Ohm Xf = 0.000000 Ohm
(t=05:042 s) ------------------------------------------------------------
(t=05:042 s) 'Grid\Bus 3\Cub_3\Relay Model.ElmRelay':
(t=05:042 s) Relay is tripping. 'Open' signal is sent to the connected breaker(s).
```

Figure 3.19. Trip signal is sent after 5 seconds

The overvoltage element is also evaluated, and the results of the protection functions report are shown in Table 3.21. To avoid misunderstanding, the overcurrent elements have been turned off, and the network settings have been altered to simulate an overvoltage state. Figure 3.20 depicts a recorded voltage of 159.8 kV, which is greater than the threshold of 159.39 kV and caused the breaker to trip. According to the protective functions report in Table 3.21, the overvoltage element is selected and a breaker trip signal is issued in 5.02 seconds, as configured.

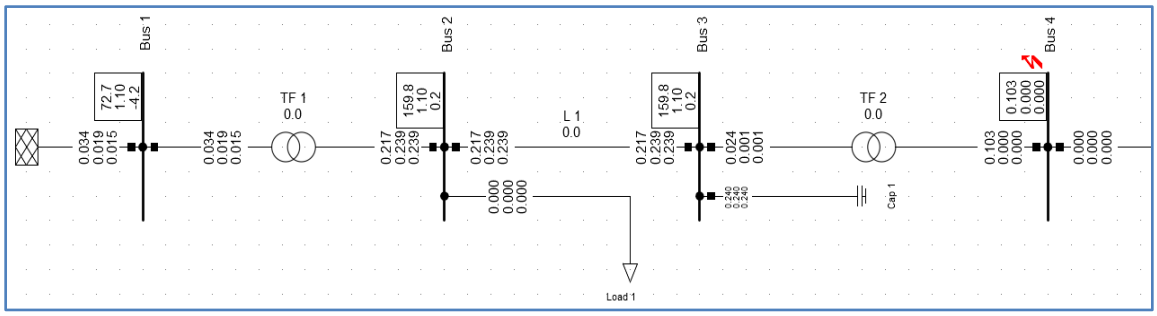

Figure 3.20. The network's overvoltage simulation

Overcurrent and over/under voltage protection systems were used to implement backup protection, and these were successfully tested. Chapter discussions and conclusions are presented in the following subsections.

Table 3.21. Overvoltage element tripping is reported by protection functions

				DIgSILENT PowerFactory 2020 SP1B	Project: Date: 5/31/2020
Relays Detailed					
Short-Circuit Calculation / Method : IEC 60909				Single Phase to Ground	/ Max. Short-Circuit Currents
Asynchronous Motors	Grid Identification			Short-Circuit Duration	
Always Considered	Automatic			Break Time	0.10 s
				Fault Clearing Time (Ith)	1.00 s
	Conductor Temperature			Voltage factor c	
	User Defined	No		Standard defined table	
Grid: Grid	System Stage: Grid		Study Case: Study Case		Annex: / 1
Relay Model		Relay Type : SEL 751-1A			
Ct : CT 1		Location : Busbar	: Bus 3	/	Ratio : 100A/1A
		Branch	: Cap 1		Connection : Y
			:		
CoreCt: CT 1		Location : Busbar	: Bus 3	/	Ratio : 100A/1A
		Branch	: Cap 1		Connection : Y
			:		
Vt : VT 1		Location : Busbar	: Bus 3	/	Ratio : 144900V/110V
		Branch	:		: - Y
Logic : Logic				yout	: 3.020 s
Breaker	Cubicle	Branch	Busbar	/ Substation	Fault Clearing Time
				/	
Closing Logic	closing Logic	Tripping Block:		Tripping	: 9999.999 s
Breaker	Cubicle	Branch	Busbar	/ Substation	Fault Clearing Time
				/	

3.5 Discussions

Capacitor bank protection is divided into two parts: system protection (the system is protected from induced over voltages from the capacitor bank) and bank protection (the capacitor bank is protected from system events that may be harmful to capacitor bank units), and bank protection (individual capacitor units/elements are protected from faults within the capacitor bank). A voltage differential protection method, as explained in the following sections, is employed for bank protection, while overcurrent and under/over voltage safeguards are provided for system protection.

Overcurrent and voltage protection techniques were tested, and the results were good. The use of voltage protection aided in the protection of defects that did not have zero-sequence components. Under voltage protection disconnects the capacitor bank from the system when the voltage dips below 90% but above 80% for 10 seconds and below 80% for 5 seconds, whilst over voltage protection disconnects the capacitor bank when the voltage exceeds 110 percent nominal for more than 3 seconds.

3.6 Conclusions

The chapter has examined electrical network simulation in DIGSILENT Power Factory software, as well as system protection of capacitor banks using overcurrent and over/under voltage protection schemes as backup protection. Load flow studies were performed to confirm that the network was correctly simulated and to assess the usual operation of the network, which will aid in the computation of protection settings. The voltage profile on bus 4 needed some adjustment in the original network because the voltage was at 0.93 p.u. The use of reactive power compensation technologies to improve the voltage profile of the network was considered. Among the options presented, shunt capacitor bank installation was chosen as the least expensive and easiest to install approach. Based on the list of available capacitor sizes, an Ideal Capacitor Placement study was performed on the application software to find the optimal size and location of the capacitor bank. The optimal capacitor size of 22 MVar was chosen from a list of capacitor bank sizes provided by the study. Load flow experiments were repeated, and the voltage profile improved to within acceptable ranges.

Following the load flow investigations, short circuit studies were also carried out. The purpose of short circuit studies is twofold: first, during the planning stage, where the results can be used to determine equipment ratings, etc., and second, during the operation stage, to determine and ensure that operational limits are not exceeded, thereby ensuring the supply's security and safety. Maximum and minimum short circuits are calculated, which is useful when calculating protection settings.

The rated capacitor bank current at the rated voltage and reactive power were used to compute the protective settings for the overcurrent protection scheme. During single phase to ground faults/zero-sequence faults, the overcurrent settings were effective. There was a requirement to defend against three-phase or phase-to-phase errors that did not have zero-sequence components. As a result, an under/over voltage protection strategy was devised and tested. As a backup protection mechanism for voltage differential protection, two protection systems, overcurrent protection and under/voltage protection, and their settings, were implemented and tested. These two protection mechanisms are used for system protection, defending against mistakes that arise outside of the capacitor bank.

The following part covers over bank protection concept and how voltage differential protection will be used. The protection philosophy focuses on fault protection inside the capacitor bank installation.

4. CHAPTER FOUR: VOLTAGE DIFFERENTIAL PROTECTION SETTINGS CALCULATIONS

4.1 Introduction

Capacitor bank protection is covered in this chapter. There are a number of distinct bank protection philosophies that utilise unbalanced protection methods. Methods of unbalance a capacitor bank are listed in an IEEE Guide for Protecting Shunt Capacitor Banks and they are:

I. Phase Voltage Differential
II. Neutral Voltage Unbalance
III. Phase Current Unbalance
IV. Neutral Current Unbalance

Unbalance protection schemes are supposed to be fast in order to minimize the spread of failures to adjacent equipment and equipment damage. Protecting against phase voltage differentials is the focus of this chapter. As can be seen in Figure 4.1, the organization of this chapter and the topics covered in each section are shown.

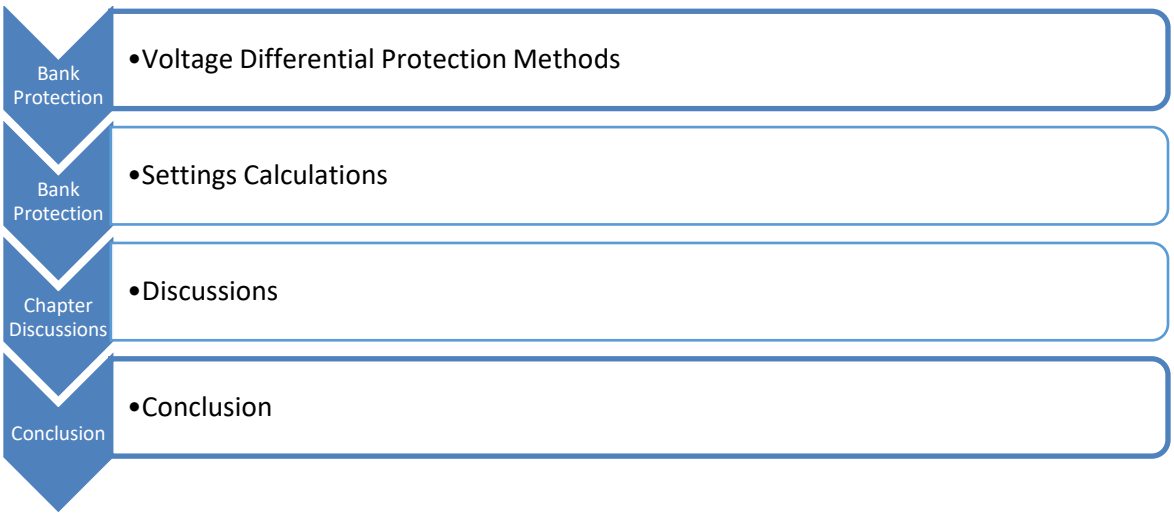

Figure 4.1. Chapter 4 flow diagram

There are four sections to this chapter. Section 4.1 introduces the chapter, Section 4.2 describes voltage differential protection methods, Section 4.3 presents phase voltage

differential protection settings calculations, and Section 4.4-chapter discussions and conclusions.

4.2 Voltage differential protection methods

Voltage differential protection solutions for capacitor bank protection are discussed in this section. For example, Figure 4.2 comparing bus bar and capacitor bank tap voltages indicates if there is a difference in magnitude that could result in impaired with the capacitor bank. In most cases, this type of protection serves as the principal safeguard against capacitor bank failures. Both phase and neutral voltage differential protection approaches are depicted in Figure 4.2 and Figure 4.3, respectively from Schweitzer Engineering Laboratory's (SEL487) manual on voltage differential protection.

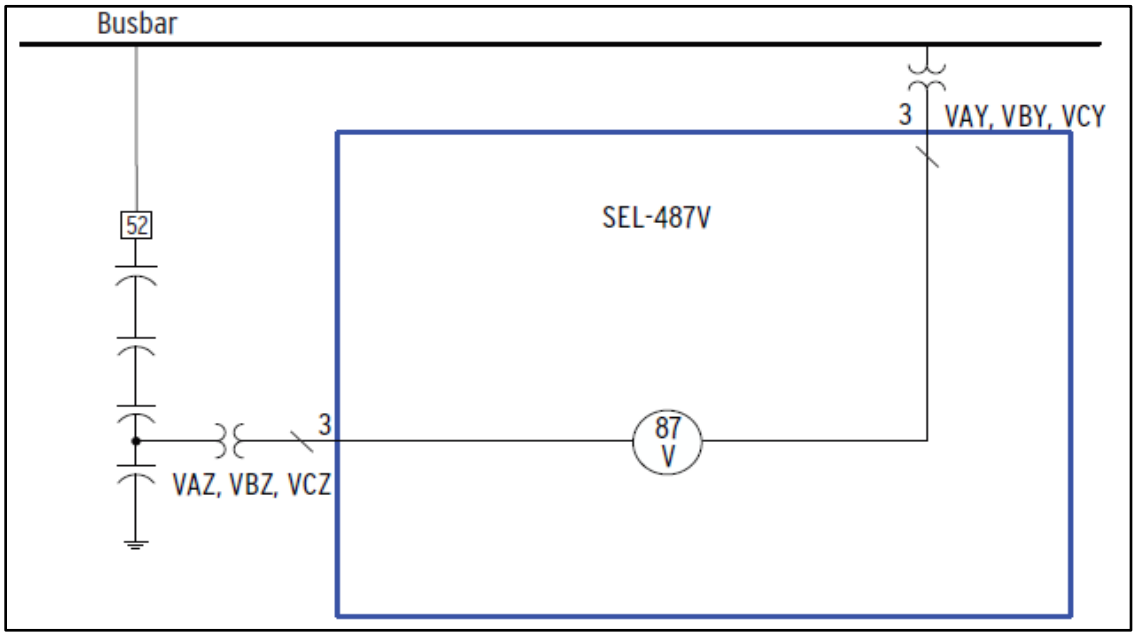

Figure 4.2. Phase voltage differential diagram, SEL-487V Relay Instruction Manual

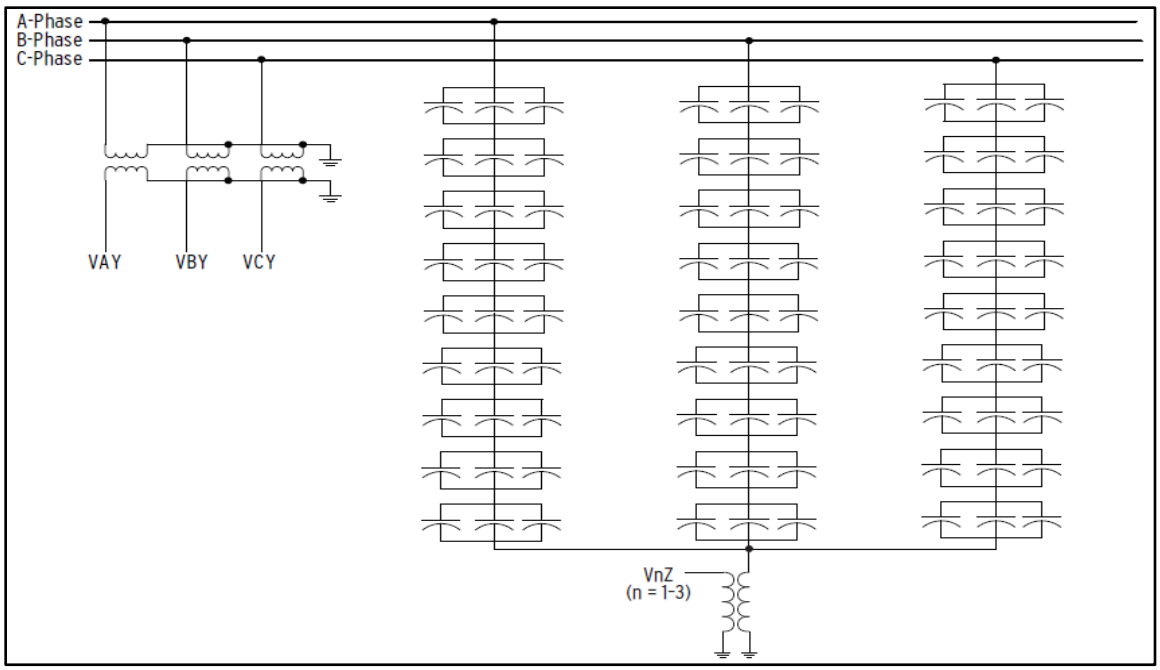

Figure 4.3. Neutral voltage differential diagram, SEL-487V Relay Instruction Manual

Capacitor bank tap and neutral point measurements of bus bar voltages are compared for phase differential protection or neutral differential protection, as illustrated in both of the figures. There should be an alarm or the capacitor bank should be removed from the system if there is any variation in terms of magnitude from the typical value defined during commissioning. On the basis of the deviation's magnitude and its threshold, it's best to issue an alarm or remove the capacitor bank.

Capacitor banks should be removed whenever the voltage across an individual element reaches 110 percent of nominal, according to the IEEE Guide for the Protection of Shunt Capacitor Banks. abnormalities that don't need immediate action and that the capacitor bank can continue to function normally for a little period can be detected by the alarm trigger. To prevent further failures and the eventual replacement of the capacitor bank, an outage might be arranged to rectify any defects on impacted capacitor units.

When the deviation surpasses 110 percent of nominal, the capacitor bank must be quickly removed as a third line of defense to avoid catastrophic failures that could harm the entire system. ***As proposed by Randy Horton and colleagues in their 2002 publication, "Unbalance Protection of Fuseless, Split-Wye, Grounded, Shunt Capacitor Banks,"***

0.5s for a trip signal and 2s for an alert. A maximum of five cycles (0.120s) is suggested for a high set.

In this study, only phase voltage differential protection approaches are discussed. Calculating voltage deviations is done by using the formula 4.1.

$$dV = V_{bus} - V_{tap} \quad 4.1$$

Whereby,

dV	Voltage deviation
V_{bus}	Bus voltage
V_{tap}	Tap voltage

The deviation voltage is normally equal to Zero "0" indicates that all of the elements in the system are functioning properly. A correction factor, k, is used because the bus voltage is substantially larger than the tap or neutral voltage. The k factor is then included in the formula:

$$dV = V_{bus} - kV_{tap} \quad 4.2$$

The formula can be rearranged as follows to find out the value of k:

$$k = \frac{V_{bus}}{V_{tap}} \quad 4.3$$

This type of protection allows for the location of the fault to be identified, either above or below the tap. A negative sign of dV, as given by formula 4.2, indicates that the tap voltage has increased, implying that there is an impedance change above the tap that produced the voltage increase. This phenomenon is used to pinpoint the location of defects inside the capacitor bank, minimizing faultfinding and downtime.

The study is based on the SEL Application Guide, Protecting a Grounded Fuseless Capacitor Bank with the SEL-487V, but with a modified capacitor bank size of 22 Mvar according to the capacitor bank optimization calculations in Chapter 3. Shorting of

capacitor elements causes the impedance of the capacitor unit to fluctuate, influencing the voltage ratio between bus voltage and tap voltage. A problem above the tap is shown by a negative differential voltage, whereas a fault below the tap is represented by a positive differential voltage, as shown in Figure 4.4 from the SEL Application Guide. The details of the capacitor bank under consideration are depicted in Figure 4.5.

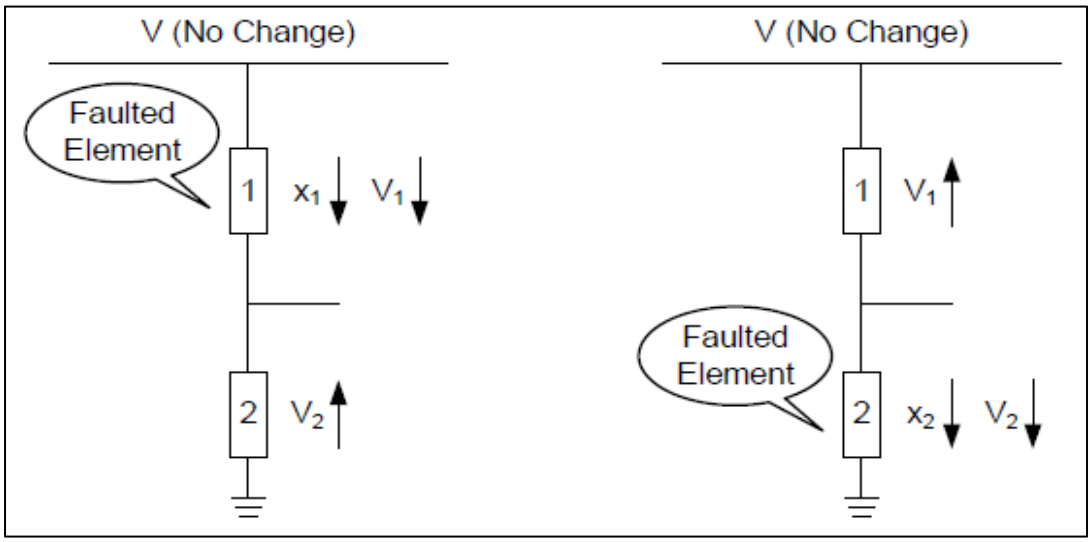

Figure 4.4. Fault location identification in capacitor bank configuration (Amberg and Young, 2010)

The network's nominal bus voltage is 144.9 kV, and the capacitor bank is center tapped, with three series units below and three above the tap. The voltage transformer ratios for Tap and Bus VT are 300:1 and 693:1, respectively. The Figure 4.5 also shows that each phase includes two parallel threads, each string with three units of eight elements in series. Each unit has a rating of 612 kVar and 14.4 kV, which converts to 76.5 kVar and 1.8 kV per element, and the capacitor bank voltage rating is 149.65 kV.

Based on this data, the total number of elements above the tap per phase is forty-eight, however the number of series connected elements is twenty-four. This is also true for the capacitor bank's below the tap design. As a result, applying the voltage divider rule yields equal voltages across both bank halves. Because the impedance in both sides is the same, the bus voltage is divided evenly in half. These are the capacitor bank's normal

operating circumstances, with no problems. Any change in impedance, indicating the failure of an element that fails by shorting itself, will be detected as a voltage variation.

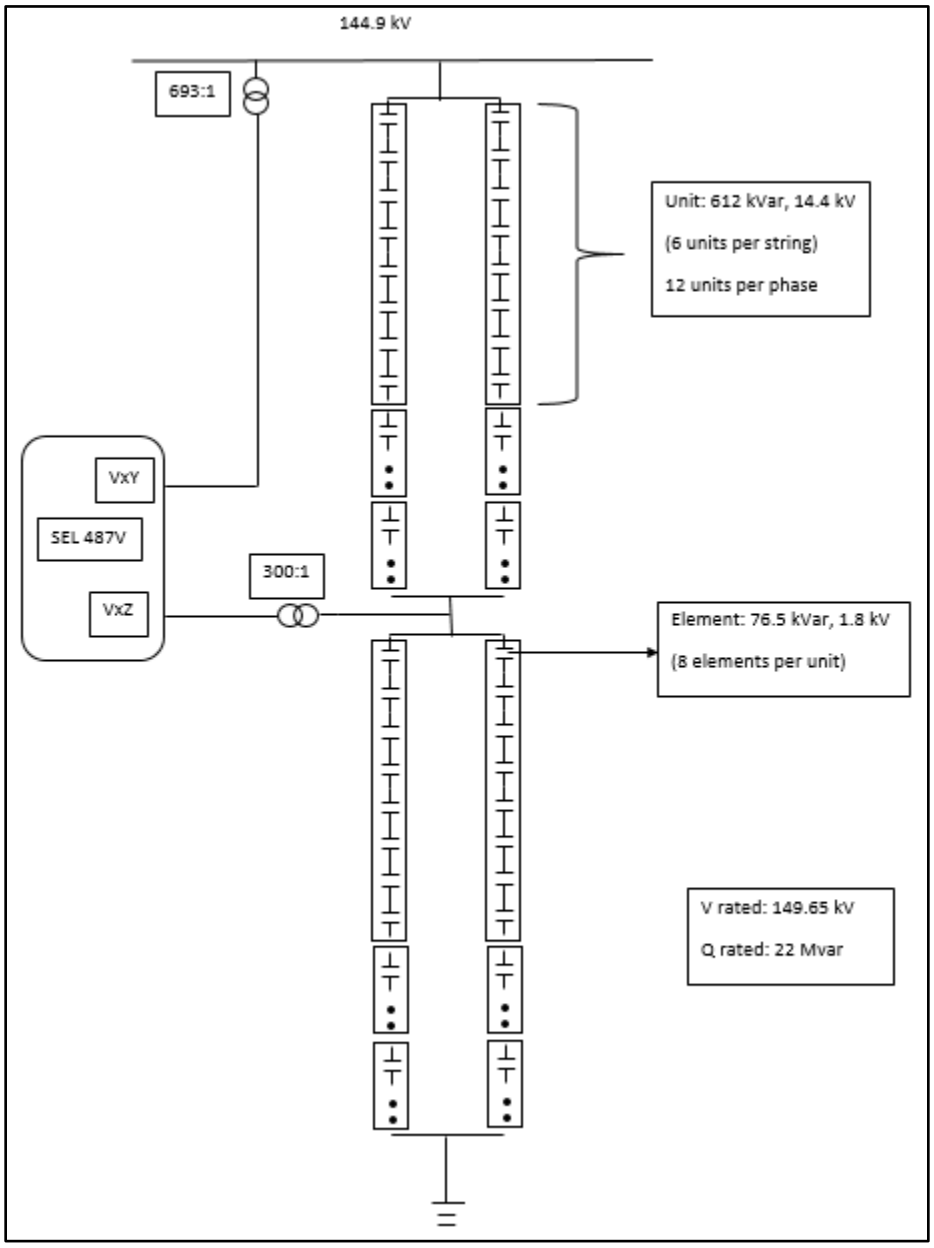

Figure 4.5. Single line diagram of the capacitor bank configuration

The next section covers the process of calculating protection settings values for all three protection levels, alarm, trip, and high set.

4.3 Voltage differential protection settings calculations

This section explains the mathematical procedure used to determine voltage differential function protection settings. Given the voltage rating of each element and the reactive power rating, an equivalent impedance can be derived as illustrated next.

$$Z_{eq} = \frac{V_{erat}^2}{S_{erat}} = 42.35\ \Omega \qquad 4.4$$

Whereby,

Z_{eq} Element equivalent impedance

V_{erat} Rated element voltage

S_{erat} Rated element power

As specified in the preceding section, the number of capacitor bank components connected in series (one string) above the tap is twenty-four, which is equal to the number of elements below the tap because the capacitor bank is centre tapped. The overall number of elements in each half, including the parallel strings, is forty-eight, whereas the total number of elements in one phase is ninety-six, including the parallel strings. These two parts' impedances will also be the same, therefore calculations for one half will be sufficient.

$$Z_{TAeq} = \frac{(Z_{eq}x24).(Z_{eq}x24)}{(Z_{eq}x48)} = 508.2\ \Omega \qquad 4.3$$

Whereby,

Z_{TAeq} Total element equivalent impedance above the tap

Therefore,

$$Z_{Teq} = 2\ x\ Z_{TAeq} = 1016.4\ \Omega$$

As previously stated, the number of elements above or below the tap for each string is twenty-four and can be represented as follows,

$C_{eRS} = 24$

$C_{eLS} = 24$

Whereby,

C_{eRS} Number of capacitor elements on the right-hand side string

C_{eLS} Number of capacitor elements on the left-hand side string

Appendix A.3 has a detailed description of the calculation process. The sections that follow go through the calculation findings based on where the failures happened on the capacitor bank, such as on the same string, below the tap, and so on.

4.3.1 Element failures on the same string

The section addresses calculations in which element failures on the same string are taken into account. Calculations involve determining the effect of element failures on the voltage loading of each element on the affected string(s) of the capacitor bank. The Voltage differential protection calculations as a result of one capacitor element failed above the tap point on the same string is given as follows:

The total equivalent impedance is calculated as given in Eq. (4.6)

$$Z_{TAeq} = \frac{(Z_{eq}x24).(Z_{eq}x23)}{(Z_{eq}x47)} = 497.39\,\Omega \quad 4.6$$

The capacitor current is calculated as given in Eq. (4.7)

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 83.19\ A \quad (4.7)$$

Applying a voltage divider rule to find differential voltage is given in the following Equations Eq. (4.8) to Eq. (4.10),

$$V_{tap} = V_{bus} x \frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 42\ 278.69\ V \quad (4.8)$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 140.93\ V \quad (4.9)$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 140.93 = -1.33\ V \quad (4.10)$$

Therefore, the current flowing through right string with one failed element is found using a current divider rule as given in Eq. (4.11)

$$I_{strR} = I_{cap} x \frac{Z_{strL}}{Z_{strL}+Z_{strR}} = 42.48\ A \quad (4.11)$$

Whereby,

I_{strR} Left string current

Z_{strL} Left string impedance

Z_{strR} Right string impedance

$$V_e = Z_{eq} x\ I_{strR} = \ 1799.03\ V$$

Therefore, voltage on the capacitor bank elements on the string with one failed element is calculated as given in Eq. (4.12):

$$V_{eop} = \frac{V_e}{V_{erat}} = 99.95\ \% \quad (4.12)$$

The rest of the calculations for Voltage differential as a result of two, three, four and five capacitor element failures above the tap point on the same string are given in Appendix A.3.1 to A.3.4 respectively. The results of the calculations are shown in Table 4.1 as well as the influence of each element failure on the voltage measured across each element. The calculation findings in the tables are based on the failures occurring on the same string of the capacitor bank above tap point. In Figure 4.6, a capacitor bank unit has two failed elements on the right-hand side string above the tap.

Table 4.1. Voltage differential protection settings as a result of capacitor element failures above the tap point on the same string

Voltage Differential Protection Settings Table (Same string above the tap)						
Failed Elements	K factor	Bus Voltage (Sec V)	Tap Voltage (Sec V)	dV above tap (V)	Voltage loading (%)	Element voltage (V)
0	0.866	120.72	139.43	-0.03	96.84	1743.12
1	0.866	120.72	140.93	-1.33	99.95	1799.03
2	0.866	120.72	142.53	-2.71	103.29	1859.17
3	0.866	120.72	144.24	-4.19	106.84	1923.11
4	0.866	120.72	146.12	-5.82	110.65	1991.72
5	0.866	120.72	148.04	-7.48	114.77	2065.83

Table 4.1 displays the results of the calculations for faults above the tap on the same string. The first column presents the number of element failures, while the second column provides the k factor obtained above. Column 3 of the table provides the measured secondary bus voltage, whereas column 4 shows the measured secondary tap voltage. Columns 5 and 6 represent voltage difference (deviation), whereas columns 7 and 8 represent voltage % loading and actual voltage measured across each impacted string element.

Figure 4.6 shows a failure of two capacitor elements above tap point on the same string as per the calculations presented. The calculations presented for one, three, four and five capacitor element failures are assumed to be on same string as shown in Figure 4.6.

The Voltage differential protection calculations as a result of one capacitor element failed below the tap point on the same string is given as follows:

The total equivalent impedance is calculated as given in Eq. (4.13)

$$Z_{TBeq} = \frac{(Z_{eq}x24).(Z_{eq}x23)}{(Z_{eq}x47)} = 497.39\,\Omega \qquad 4.13$$

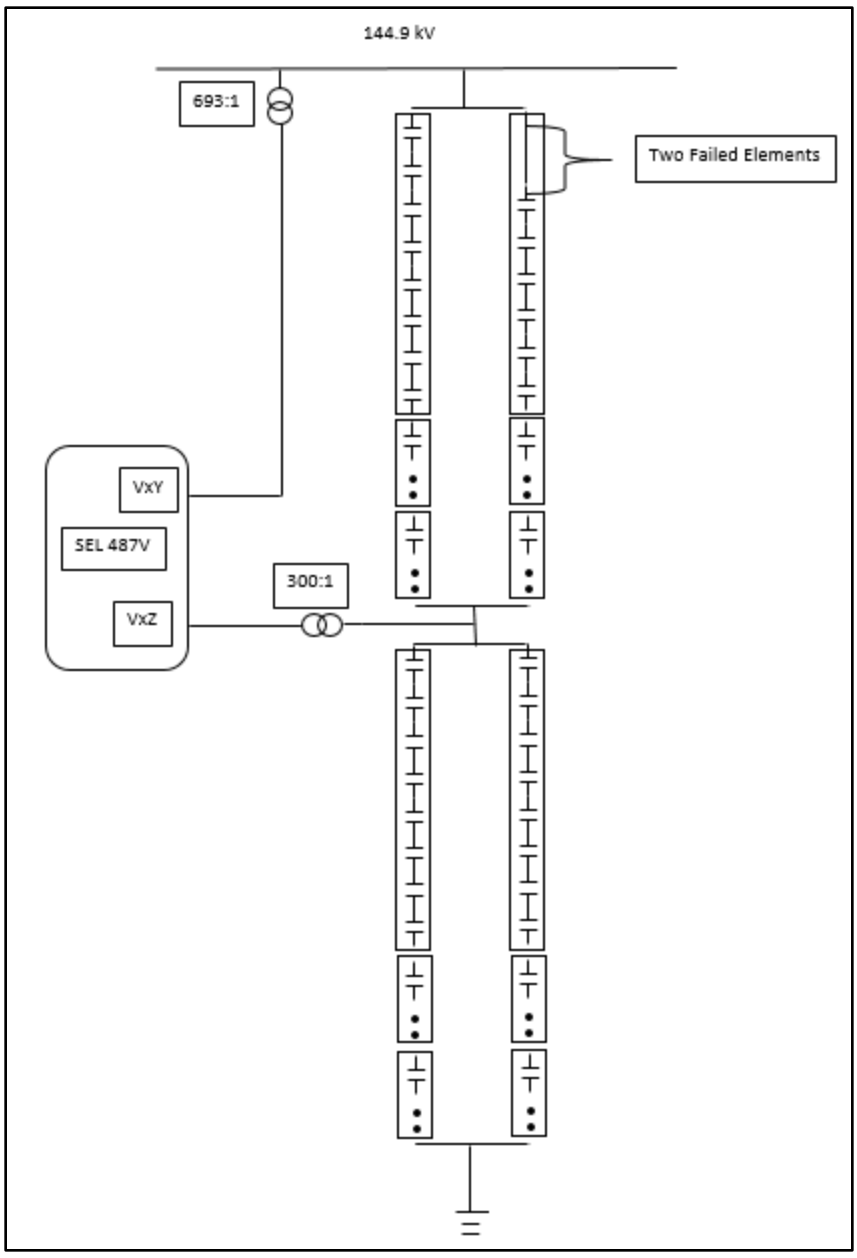

Figure 4.6. Capacitor unit with two failed elements on one string

The capacitor current is calculated as given in Eq. (4.14) and the voltage differential is given in the following Equations Eq. (4.15) to Eq. (4.17),

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 83.19\ A \qquad 4.14$$

Applying a voltage divider rule to find differential voltage as given in Eq. (4.15)

$$V_{tap} = V_{bus} x \frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 41\,379.37\ V \quad 4.15$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 137.93\ V \quad 4.16$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 137.92 = 1.27\ V \quad 4.17$$

Therefore, the current flowing through right string with one failed element is found using a current divider rule as given in Eq. (4.18)

$$I_{strR} = I_{cap} x \frac{Z_{strL}}{Z_{strL}+Z_{strR}} = 42.48\ A \quad 4.18$$

$$V_e = Z_{eq} x\ I_{strR} = \ 1799.03\ V \quad 4.19$$

Therefore, the capacitor bank elements on the string with one failed element is calculated as given in Eq. (4.20):

$$V_{eop} = \frac{V_e}{V_{erat}} = 99.95\ \% \quad 4.20$$

The rest of the calculations for Voltage differential as a result of two, three, four and five capacitor element failures below the tap point on the same string is given in Appendix A.3.5 to A.3.8 respectively. The results of the calculations are shown in Tables 4.2 as well as the influence of each element failure on the voltage measured across each element. As previously discussed, for capacitor element failures above the tap, the differential voltage reported in column 5 is negative and rises as more elements fail. Table 4.2 is identical to Table 4.1, with the exception that it indicates failures below the tap, and as such, differential voltage is positive, as shown in column 5.

Table 4.2. Voltage differential protection settings as a result of capacitor element failures below the tap point on the same string

Voltage Differential Protection Settings Table (Same string below the tap)						
Failed Elements	K factor	Bus Voltage (Sec V)	Tap Voltage (Sec V)	dV below tap (V)	Voltage loading (%)	Element voltage (V)
0	0.866	120.72	139.43	-0.03	96.84	1743.12
1	0.866	120.72	137.93	1.27	99.95	1799.03
2	0.866	120.72	136.33	2.66	103.29	1859.17
3	0.866	120.72	134.62	4.14	106.84	1923.11
4	0.866	120.72	132.79	5.72	110.65	1991.72
5	0.866	120.72	130.82	7.46	114.77	2065.83

Failures of elements, whether above or below the tap, cause the same voltage variation, resulting in the same amount of voltage stress on healthy elements on the affected string. The results show that a single element failure raises the voltage across each element from 96.84 percent to 99.95 percent, while two element failures raise the voltage to just over 103 percent on the affected string. Three element failures raise the voltage to just below 107 percent, four element failures raise it to just over 110 percent, and five element failures raise it to just below 115 percent. Based on this data, the protection settings for various levels of protection, such as alarm at 105 percent, trip at 110 percent, and high set above 110 percent are determined.

According to the calculations results presented in the tables (4.1 and 4.2), a failure of three elements results in a voltage loading of just over 106 percent, and as such, alarming will be set using this value, whereas four elements result in a voltage loading of just over 110 percent, and this value will be used in tripping the capacitor bank breaker. A failure of five elements resulting in a failure rate of more than 110 percent will be setup for high set operation. As previously stated, these results are based on the failures being on the same string.

The following section covers calculations that consider element failures on parallel strings but on the same half of the capacitor bank.

4.3.2 Element failures on parallel strings

The section considers parallel string element failures, and the calculation assumes the failures happen at same time on parallel string of the capacitor bank half, either above or below the tap. Tables 4.3 and 4.4 show the effect of the same number of element failures on parallel strings, within the same capacitor bank half, on the element voltage loading of the affected string. Figure 4.7 shows capacitor bank that has four failed elements, two on each parallel string above the tap.

The Voltage differential protection calculations as a result of two capacitor elements failed above the tap point on the different string is given as follows:

The total equivalent impedance is calculated as given in Eq. (4.21)

$$\boldsymbol{Z_{TAeq}} = \frac{(\boldsymbol{Z_{eq}x23}).(\boldsymbol{Z_{eq}x23})}{(\boldsymbol{Z_{eq}x46})} = 487.03\ \Omega \quad 4.21$$

Therefore, the current flowing through right string with one failed element is found using a current divider rule as given in Eq. (4.22)

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 84.06\ A \quad 4.22$$

Applying a voltage divider rule to find differential voltage as given in Eq. (4.23) to Eq. (4.25)

$$V_{tap} = V_{bus}x\frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 42\ 718.79\ V \quad 4.23$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 142.4\ V \quad 4.24$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 142.4 = -2.6\ V \quad 4.25$$

Therefore, the current flowing through each parallel string with two failed elements is found using a current divider rule as given in the Eq. (4.26)

$$I_{strR} = \frac{I_{cap}}{2} = 42.03\ A \quad 4.26$$

$$V_e = Z_{eq}x\ I_{strR} = \ 1779.97\ V$$

Therefore, the healthy capacitor bank elements on the parallel string with two failed have the voltage stress as given in Eq. (4.27)

$$V_{eop} = \frac{V_e}{V_{erat}} = 98.89\ \% \qquad 4.27$$

The rest of the calculations for Voltage differential protection settings as a result of four, six, eight, ten and twelve capacitor element failures above the tap point on parallel strings is given in Appendix A.3.9 to A.3.13 respectively.

Table 4.3. Voltage differential protection settings as a result of capacitor element failures above the tap point on parallel strings

Voltage Differential Protection Settings Table (Different Strings above the tap)						
Failed Elements	K factor	Bus Voltage (Sec V)	Tap Voltage (Sec V)	dV above tap (V)	Voltage loading (%)	Element voltage (V)
0	0.866	120.72	139.43	-0.03	96.84	1743.12
2	0.866	120.72	142.4	-2.6	98.89	1779.97
4	0.866	120.72	145.49	-5.27	101.05	1818.93
6	0.866	120.72	148.72	-8.07	103.29	1859.16
8	0.866	120.72	152.11	-11.01	105.64	1901.52
10	0.866	120.72	155.6	-14.03	108.09	1945.56
12	0.866	120.72	159.35	-17.28	110.67	1992.14

The Voltage differential protection calculations as a result of two capacitor elements failed below the tap point on the different string is given as follows:

The total equivalent impedance is calculated as given in Eq. (4.28)

$$Z_{TAeq} = \frac{(Z_{eq}x23).(Z_{eq}x23)}{(Z_{eq}x46)} = 487.03\ \Omega \qquad 4.28$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 84.06\ A \qquad 4.29$$

Applying a voltage divider rule to find differential voltage is calculated as given in Eq. (4.30) to Eq. (4.32),

$$V_{tap} = V_{bus} x \frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 40\,939.26\ V \quad 4.30$$

$$\boldsymbol{V_{tsec}} = \frac{V_{tap}}{\boldsymbol{PTR_{tap}}} = 136.46\ V \quad 4.31$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 136.46 = 2.55\ V \quad 4.32$$

Therefore, the current flowing through right string with two failed elements is found using a current divider rule is calculated as given in Eq. (4.33)

$$\boldsymbol{I_{strR}} = \frac{I_{cap}}{2} = 42.03\ A \quad 4.33$$

$$V_e = Z_{eq} x\ I_{strR} = \ 1779.97\ V$$

Therefore, the voltage stress on healthy capacitor bank elements on parallel strings with two failed elements below tap point is calculated and given in Eq. (4.34)

$$V_{eop} = \frac{V_e}{V_{erat}} = 98.89\ \% \quad 4.34$$

The rest of the calculations for Voltage differential protection settings as a result of four, six, eight, ten and twelve capacitor element failures below the tap point on parallel strings is given in Appendix A.3.14 to A.3.18 respectively.

Table 4.4. Voltage differential protection settings as a result of capacitor element failures below the tap point on parallel strings

Voltage Differential Protection Settings Table (Different Strings below the tap)						
Failed Elements	**K factor**	**Bus Voltage (Sec V)**	**Tap Voltage (Sec V)**	**dV below tap (V)**	**Voltage loading (%)**	**Element voltage (V)**
0	0.866	120.72	139.43	-0.03	96.84	1743.12
2	0.866	120.72	136.46	2.55	98.89	1779.97
4	0.866	120.72	133.37	5.22	101.05	1818.93
6	0.866	120.72	130.14	8.02	103.29	1859.17
8	0.866	120.72	126.75	10.95	105.64	1901.52
10	0.866	120.72	123.22	14.01	108.09	1945.56
12	0.866	120.72	119.51	17.22	110.67	1992.14

Tables 4.3 and 4.4 are similar to Tables 4.1 and 4.2, respectively, with the exception of element failures occurring on parallel strings at the same time. It should also be noted that the number of element failures listed in column 1 pertains to one string, which is double the number indicated for both strings in Figure 4.7. Although this is unlikely to occur, it has been considered.

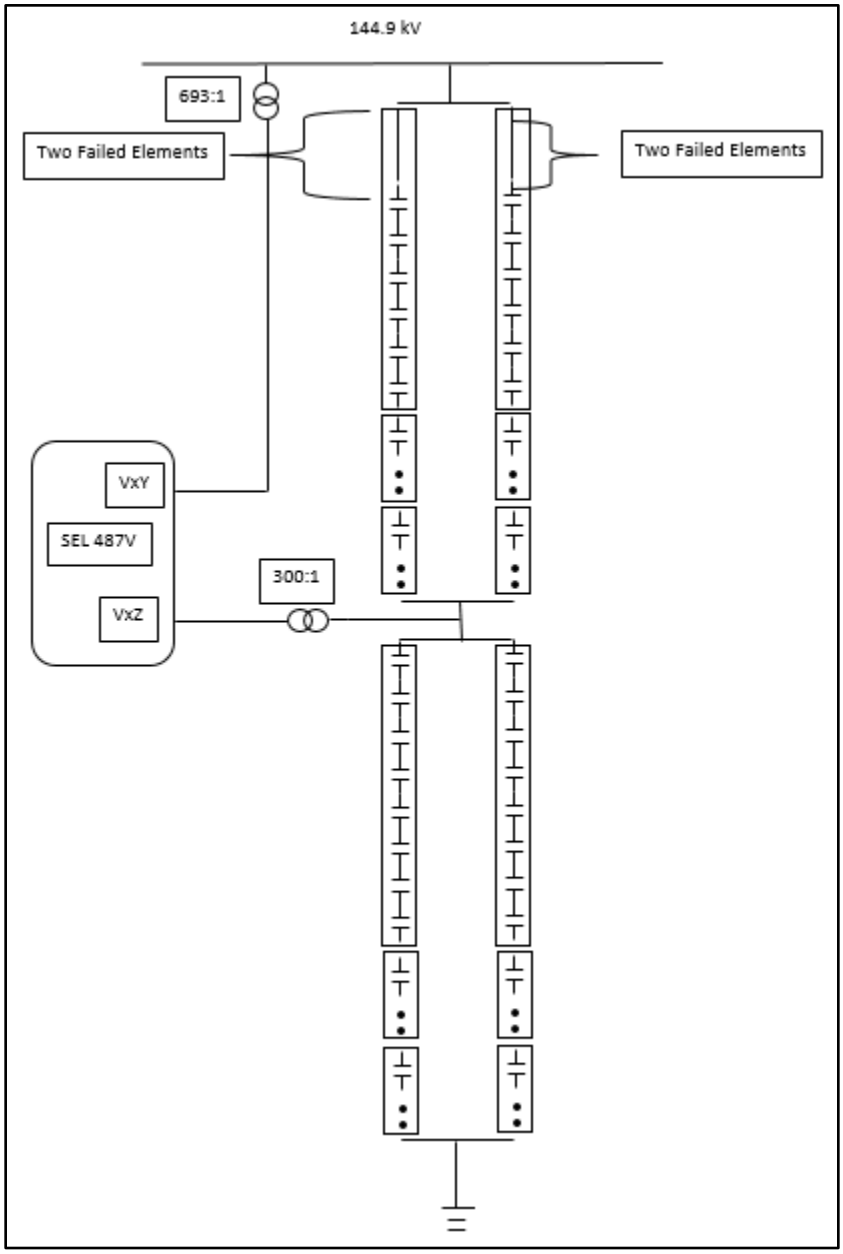

Figure 4.7. Capacitor unit with two failed elements on each parallel string

Table 4.3 and Table 4.4 indicate that a 105 percent voltage loading for alarm pickup is achieved with the failure of approximately 8 elements from each parallel string, resulting in approximately 16 elements, although the voltage variance is around 11 V. At a differential voltage of just over 17 V, 12 element failures from each parallel string result in a 110 percent voltage loading.

The calculation results in the tables show that the element voltage loading is the same for both element failures above and below the tap. A voltage loading of 98.89 percent is encountered on each string of the damaged half bank when two elements fail, one on each string. A failure of another two elements, one from each string, resulting in two elements per string, raises the element voltage loading to just over 101 percent. It should be highlighted that with the failure of 8 pieces, four on each string, a 105 percent is achieved. It should be highlighted that such element failures are extremely unlikely.

The following part deals another possibility in the calculations: components failing on both half of the capacitor bank at the same time.

4.3.3 Capacitor element failures above and below the tap

The section examines the outcomes of calculations that take into account capacitor bank element failures that occur above and below the tap at the same time. This condition is extremely improbable to occur, but it has been studied, and the results of the calculation are reported in Table 4.5. It should be noted that in this situation, alarming should be achieved with the failure of four elements above and below the tap (for a total of eight elements), tripping with a failure of six elements, and high set tripping with a failure of more than six elements. It should be emphasized that this study is primarily based on column 6 of the element voltage loading. Further examination of other columns reveals that the differential voltage remains constant regardless of the number of element failures.

This is because the number of element failures in both halves is always the same, resulting in equal impedances and thus equal voltage divides. The interesting aspect of this scenario is that only the capacitor bank current changes as a result of the total impedance change caused by element failures. As it is picked up, this circumstance causes issues for the differential protection function. Back up protection (overcurrent) should be changed

to accommodate for this event, and the details are covered in the following chapter 5. Two element failures on both capacitor bank halves on the right-hand side strings are shown in Figure 4.8.

Table 4.5. Voltage differential protection settings as a result of capacitor element failures above and below the tap point on the same string

Voltage Differential Protection Settings Table (Both half banks)						
Failed Elements	K factor	Bus Voltage (Sec V)	Tap Voltage (Sec V)	dV above and below tap (V)	Voltage loading (%)	Element voltage (V)
0	0.866	120.72	139.43	-0.03	96.84	1743.12
1	0.866	120.72	139.43	-0.03	98.93	1780.82
2	0.866	120.72	139.43	-0.03	101.24	1822.32
3	0.866	120.72	139.43	-0.03	103.76	1867.64
4	0.866	120.72	139.43	-0.03	106.51	1917.18
5	0.866	120.72	139.43	-0.03	109.57	1972.24
6	0.866	120.72	139.43	-0.03	112.98	2033.65

$$Z_{TAeq} = \frac{(Z_{eq}x24).(Z_{eq}x23)}{(Z_{eq}x47)} = 497.39\ \Omega \quad (4.35)$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 84.1\ A \quad (4.36)$$

Applying a voltage divider rule to find differential voltage is calculated and given in Eq. (4.37) to Eq. (4.39),

$$V_{tap} = V_{bus}x\frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 41\,829.03\ V \quad (4.37)$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 139.43\ V \quad (4.38)$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 139.43 = -0.03\ V \quad (4.39)$$

Therefore, the current flowing through right string with one failed element is found using a current divider rule, is calculated and give in Eq. (4.40)

$$I_{strR} = \frac{I_{cap}}{2} = 42.05\ A \quad (4.40)$$

$$V_e = Z_{eq} x\, I_{strR} = \ 1780.82\, V$$

Therefore, the capacitor bank elements on the string with one failed element is calculated and give in Eq. (4.41)

$$V_{eop} = \frac{V_e}{V_{erat}} = 98.93\ \% \qquad 4.41$$

The rest of the calculations for voltage differential protection settings as a result of four, six, eight, ten and twelve capacitor element failures above and below the tap point on is given in Appendix A.3.19 to A.3.23 respectively.

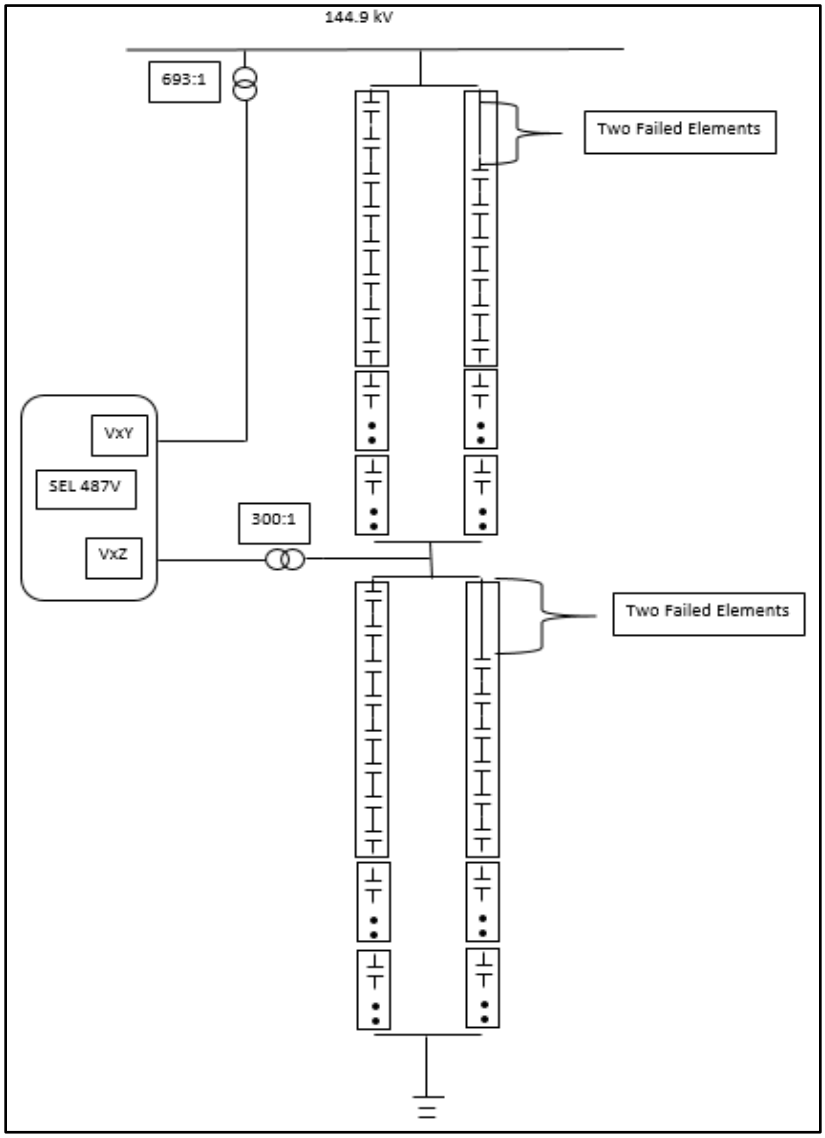

Figure 4.8. Capacitor unit with two failed elements on each half bank

The following section highlights key topics covered in the chapter discussions and conclusions.

4.4 Discussion and conclusion

The chapter discussed capacitor bank protection theory, protection settings calculations and simulations. Voltage differential protection serves as the primary protection mechanism for capacitor banks. To ascertain the difference, the bus bar voltage and tap voltage are continuously monitored and compared. If the variance exceeds the predefined threshold, action is taken. Manual protection settings calculation is used to compute the thresholds for capacitor bank protection settings for element faults above and below the tap. Calculations are conducted for each element failing above and below the tap, either in the same string or in parallel strings.

The scenarios that are important are, i) simultaneous capacitor element failures in parallel strings, and ii) simultaneous capacitor element failures above and below tap, with the first being unlikely to happen and the second being extremely unlikely to happen. The influence of these two scenarios on the system is investigated, and it is observed that in the first scenario, the principal protection (voltage differential) picks up, perhaps with more element failures than usual.

The voltage differential technique does not detect the second scenario since the failures are balanced. The backup protection (overcurrent) protection, which is set to 96 A, aids in catering to and protecting the capacitor bank. The 96 A current was chosen because it is exactly below the 1.1 percent allowed element voltage induced by a failure of 6 capacitor elements above the tap and 6 capacitor elements below the tap.

The computed values in the chapter revealed the need for backup protection. It has been demonstrated that certain circumstances are not covered by the main protection of voltage differential scheme, even though the possibility of those scenarios occurrence is extremely low.

The following section discusses the setup and engineering design of the lab scale implementation in order to validate the performance of the suggested protective scheme.

5. CHAPTER FIVE: SHUNT CAPACITOR BANK PROTECTION LAB-SCALE IMPLEMENTATION AND ENGINEERING CONFIGURATIONS OVERVIEW

5.1 Introduction

The previously calculated protective parameters, as well as simulation studies, are executed on a lab scale environment. The section goes into the design and construction of a lab scale setup for testing the proposed technology. In comparison to traditional methods, the lab size setting allows for system-based testing, which is currently gaining popularity as a preferred way of protection testing. The test technique has benefits such as distributed testing, transient testing, and so forth. The system is engineered and configured in such a way that it solves present and future problems by utilizing future-proof engineering tools and concepts like as the IEC 61850 Standard, system-based testing, and so on.

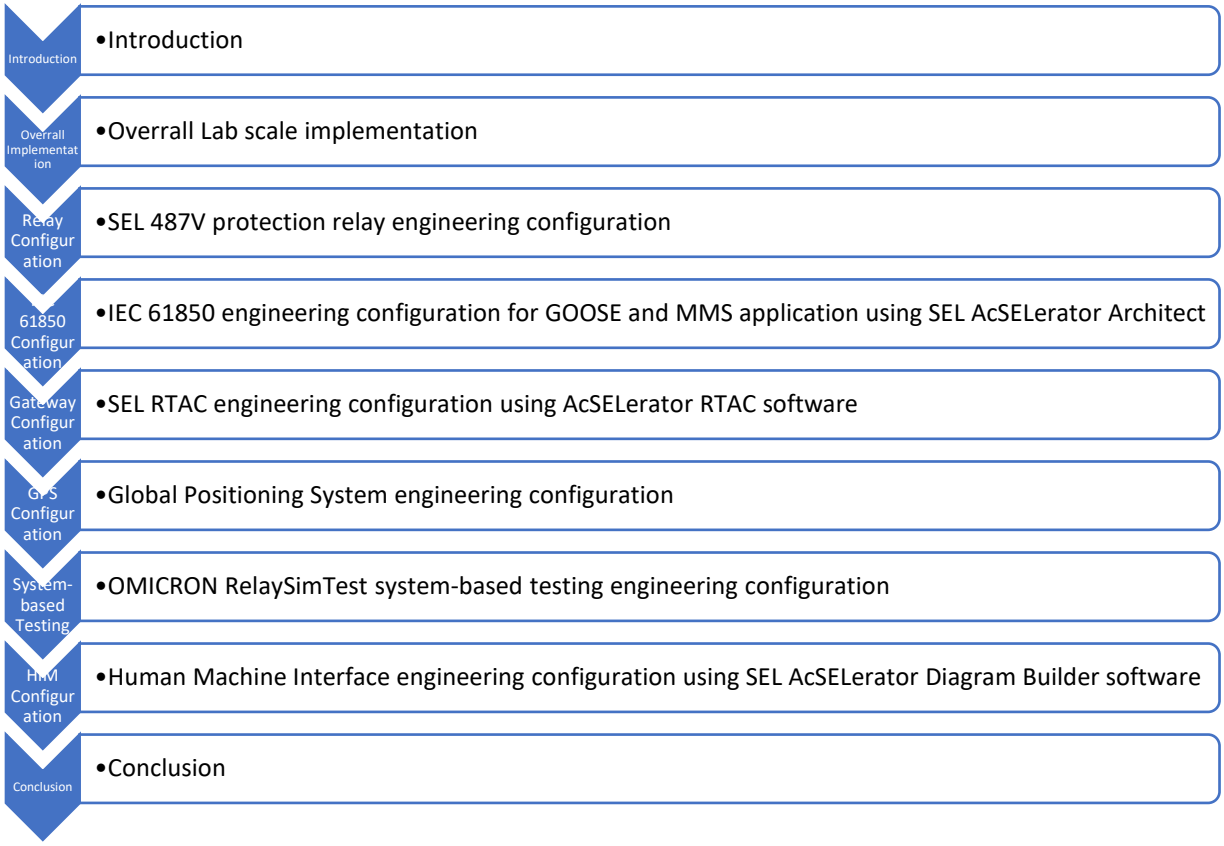

Figure 5.1. Overview of chapter 5 in flow diagram format

As shown in Figure 5.1, the chapter is divided into eight sections: section 5.1 provides an introduction to the chapter, section 5.2 provides an overview of lab scale implementation, section 5.3 discusses SEL 487V protection relay configuration, section 5.4 discusses IEC 61850, MMS, and GOOSE configuration, section 5.5 provides engineering configuration for SEL RTAC gateway, and section 5.6 provides engineering configuration for Global Positioning System.

5.2 Lab-scale implementation

This section of the chapter presents a lab-scale implementation of shunt capacitor bank protection using a voltage differential protection scheme and GOOSE and MMS application of the IEC 61850 standard. Figure 5.2 depicts the lab scale implementation, including all hardware equipment. The hardware equipment configurations, as well as the software and engineering tools used, are presented. In the engineering PC, the power system network given in Figure 5.3 is simulated using RelaySimTest. This simulation includes both steady-state and transient power system conditions and is connected to CMC test sets via a communications network. The RelaySimTest software-simulated instrument transformers (VTs and CTs) are linked with the CMC test set for injection of those measurements into the SEL 487V protection relay.

The GPS clock provides accurate time for all network equipment in two ways: i) Network Time Protocol (NTP) via a TCP connection to devices such as the SEL RTAC gateway and SEL 487V relay, network switch, and engineering PC, and ii) Precision Time Protocol (PTP) for CMCs via OSI layer 2 (Data Link) using MAC addresses. The accuracy provided by NTP and PTP is what distinguishes them. NTP has an accuracy of milliseconds, whereas PTP has an accuracy of nanoseconds or greater depending on the hardware used. PTP uses tremendous amount of bandwidth on communication channels and need specialized channels to avoid interfering with time-critical services like GOOSE communication. In lab-scale implementation PTP time synchronisation for the CMCs has direct links from the GPS clock to CMC test units to avoid clogging the network.

The network switch enables connection between all of these devices, while the SEL RTAC gateway collects all data for communication with SCADA systems or HMIs to aid operators in monitoring and controlling the power system network. OMICRON's RelaySimTest, SEL AcSELerator Architect, SEL AcSELerator QuickSet, SEL AcSELerator Diagram Builder,

OMICRON's Test Universe, SEL SynchroWave Event, and OMICRON's IED Scout are used to configure the system simulation, testing and monitoring.

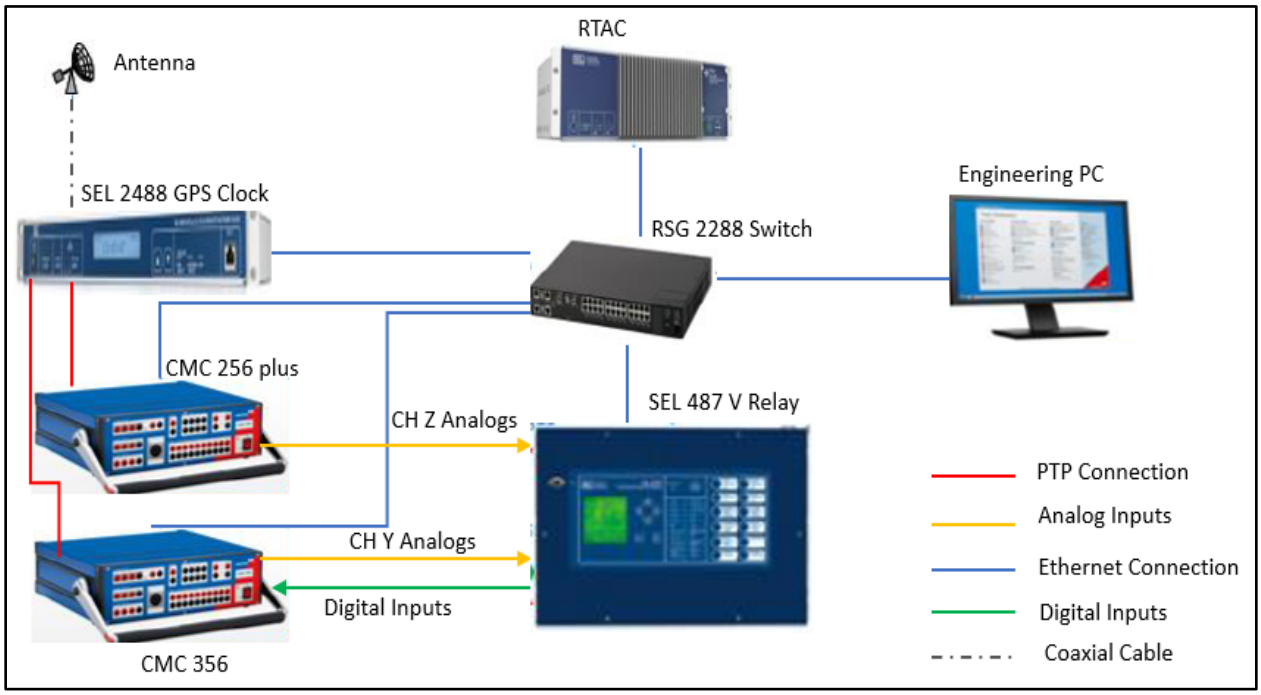

Figure 5.2. Lab-scale implementation to test the protection functions of a shunt capacitor bank

Table 5.1 depicts the assigning of Internet Protocol (IP) addresses to the listed hardware equipment shown in Figure 5.2 in order to create a Local Area Network (LAN) that allows the devices to communicate with one another. The IP addresses in the first column are the primary static IP addresses for the LAN assigned by the user, whereas secondary dynamic IP addresses are device generated one used for engineering configuration setup with those devices. Most of the devices listed in Table 5.1 has two network cards which allow to assign second IP address from vendor side to configure the device itself, whereas the first IP address is user defined one to establish Ethernet communication which allow to communicate other devices on the same network domain. Example, SEL 2488 GPS clock has two network card and its first and second IP addresses are defined as given in Table 5.1.

Table 5.1. LAN IP address allocation

Device	IP Address 1	IP Address 2
SEL 2488 GPS Clock	192.168.1.13	192.168.2.2
Siemens RSG2288 Network Switch	192.168.1.15	N/A
SEL RTAC Gateway	192.168.1.170	N/A
SEL 487V protection relay	192.168.1.150	N/A
CMC 356	192.168.1.149	192.168.3.149
CMC 256 plus	192.168.1.204	192.168.4.204
Engineering PC/Laptop	192.168.1.252	N/A

Figure 5.3 depicts the power system network under study, indicating the capacitor bank that must be protected on bus 3 as described in chapter 3, section 3.2. The power system network is modelled in RelaySimTest, with the capacitor bank serving as the primary simulation.

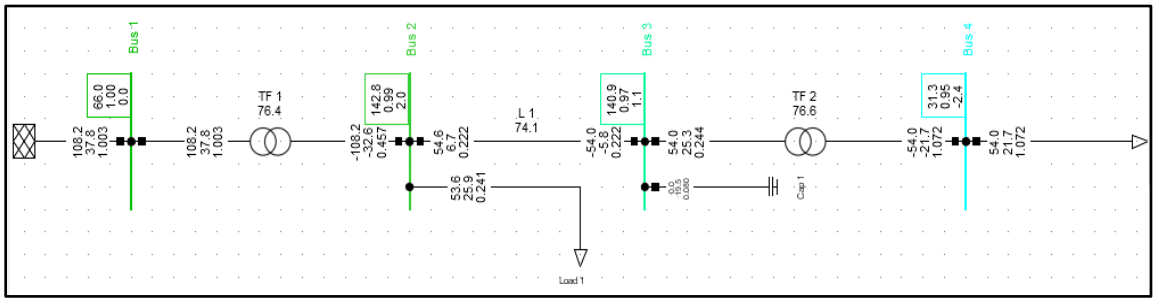

Figure 5.3. Power system network under test

The following section describes the engineering configuration of a SEL 487V protection relay utilizing SEL AcSELerator QuickSet software. The section presents the protection settings calculated in the previous chapters for main and backup protection.

5.3 Protection relay engineering configuration

The section covers and shows how to configure the SEL-487V relay with the SEL AcSELerator QuickSet software. The software home page is depicted in Figure 5.4. As seen on the left side of the screen, many options must be configured, some of which are explained next: Global, Group 1, Outputs, Front Panel, and Port Settings. There are six groups of protection settings that can be specified, as indicated in the screenshot. This enables the setup of multiple settings for different network conditions that may influence

network impedances, hence affecting protections settings, and the activation of these other group settings can be done as needed with the enable that particular group setting. The automation logic tab enables free form programming of automation and computation that may be required for a specific operation. The report tab provides for the configuration of parameters for functions such as event recording and trigger points. DNP map settings tabs, as the name implies, provide mapping configuration to a Distribution Network Protocol for connections with external systems such as SCADA. The bay tab allows you to configure the protected device schematically. The Capacitor Bank Assistant is the final tab, and it was designed to provide computation results for capacitor element failures. Figure 5.5 depicts the tool's restriction in terms of tap measurements, which is emphasized in red.

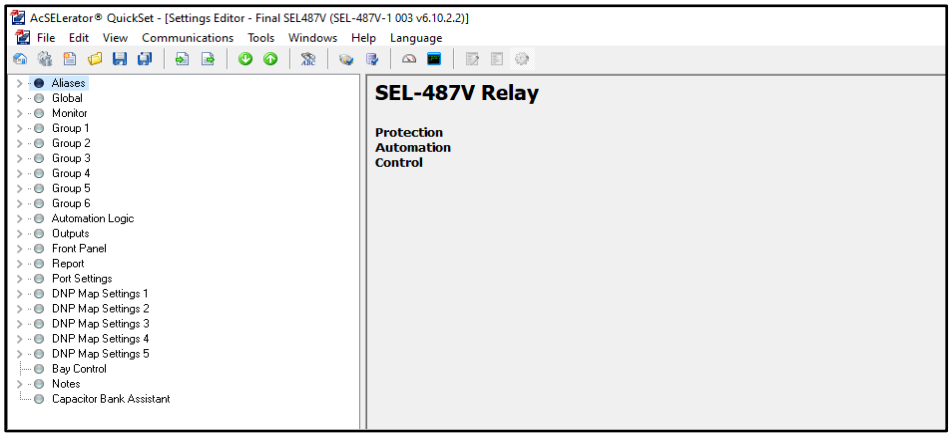

Figure 5.4. SEL 487V AcSELerator QuickSet home page

The constraints indicate that the tool has only been designed for use with Low Voltage Capacitor (LVC), as shown in the SEL application guide that has been adapted for the project. The screenshot in Figure 5.5 reveals that the tap voltage is limited to 10 kV while the reactive voltage is 0.999 MVar, hence the tool could not be utilized for the project because the capacitor bank is centre tapped. Due to these constraints, calculations for capacitor element failures have to be done manually, as provided in Chapter 4, section 4.3 and Appendix A.3, however the same calculation process as presented in the SEL application is guide is followed.

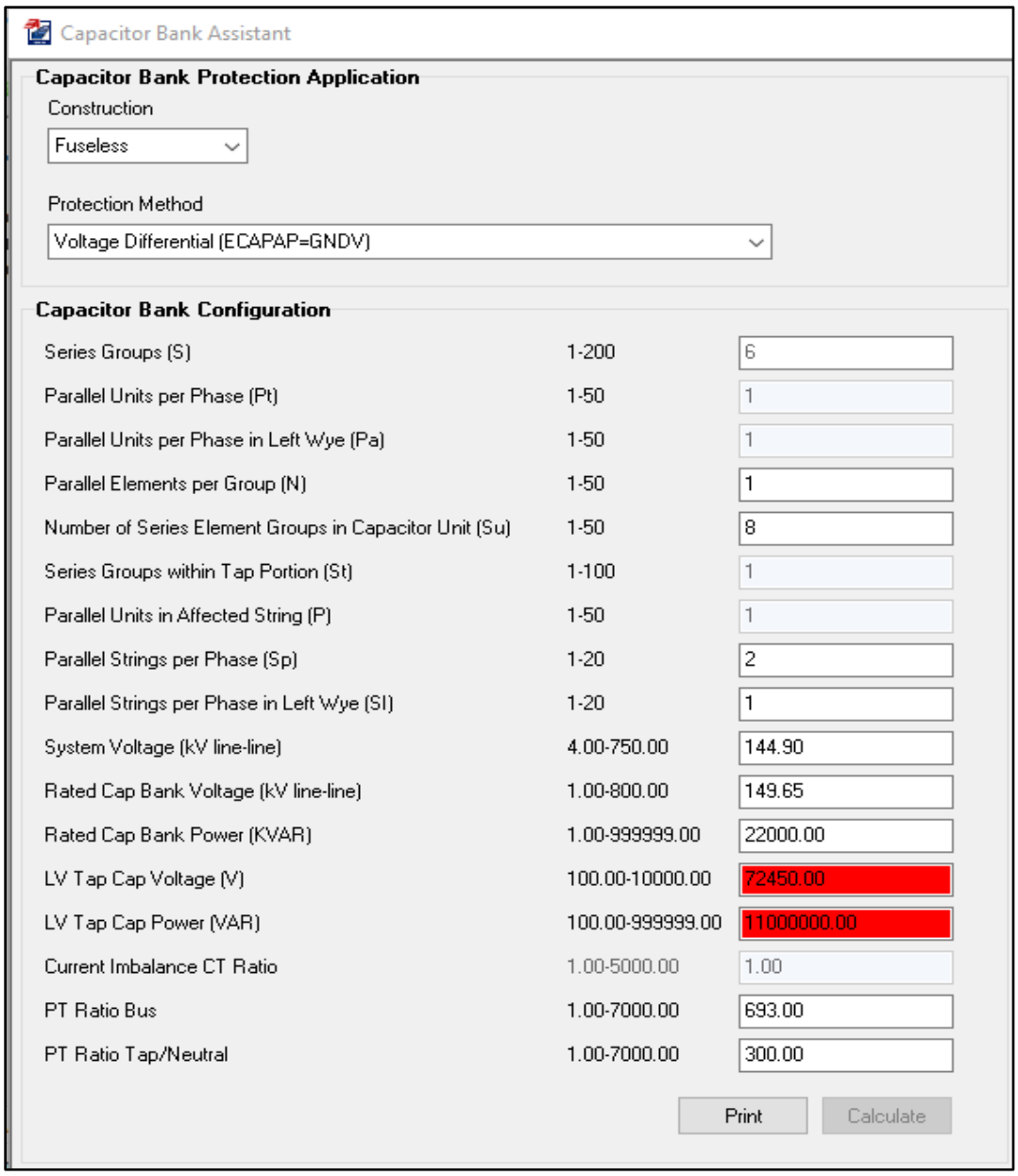

Figure 5.5. SEL 487V Capacitor Bank Assistant (CBA)

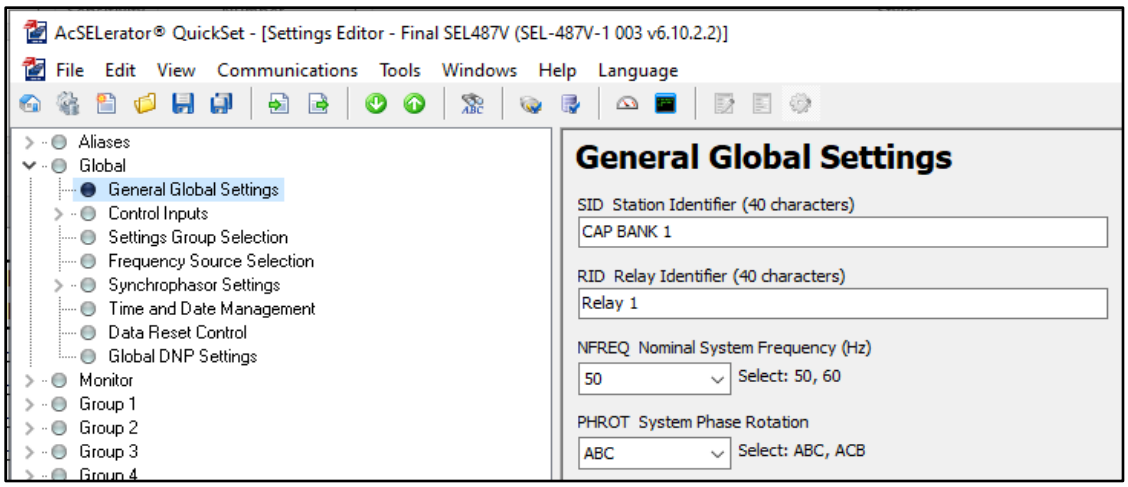

Figure 5.6. Global settings

The Global settings page enables for the overall configuration of the relay, including information such as network frequency and phase rotation, as shown in Figure 5.6. Figure 5.7 depicts Group 1 settings demonstrating the usage of a grounded capacitor bank as well as the activation of the Definite Minimum Time Overcurrent (DMT) function for the capacitor bank incomer while the Inverse Time Overcurrent elements are disabled.

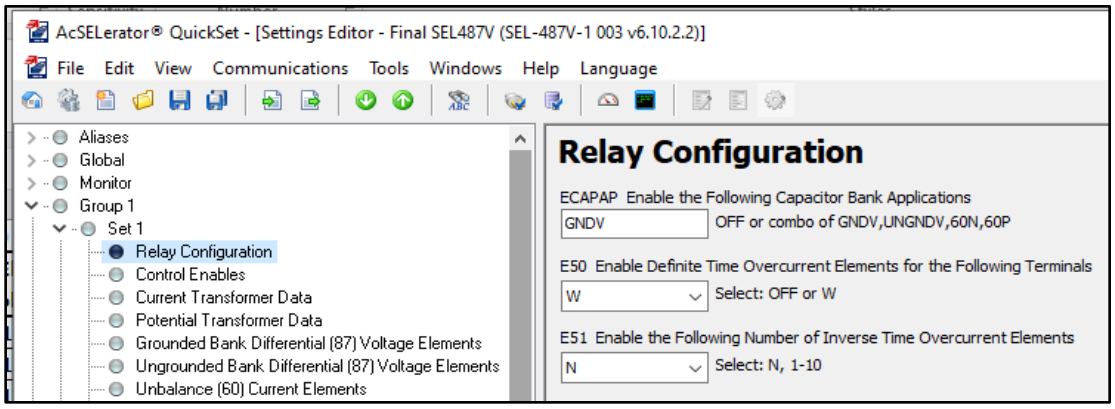

Figure 5.7. Enable protection elements

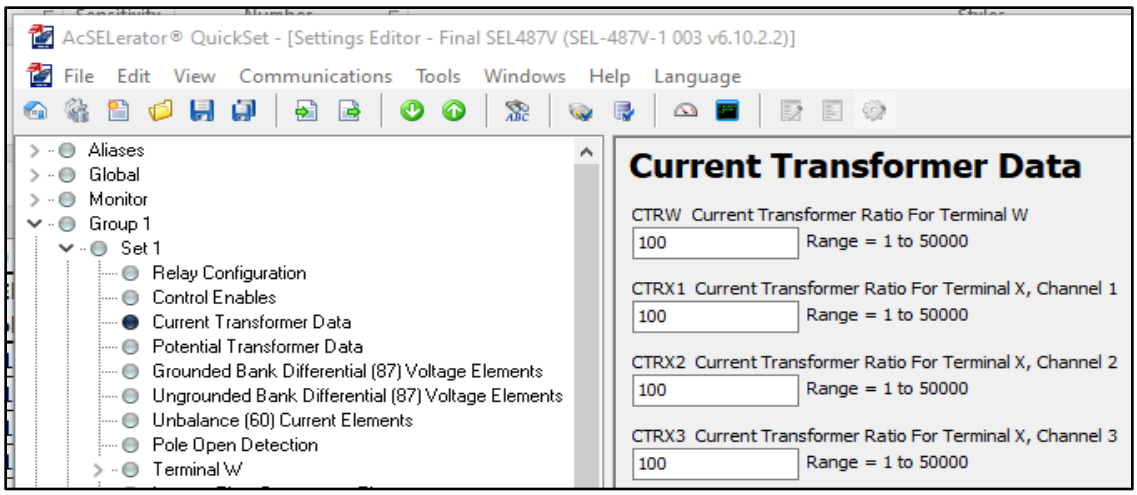

Figure 5.8. CT configuration

Figure 5.8 depicts design of current transformer ratios as discussed in chapter 3, section 3.2. For consistency of measurements, these settings must be consistent with those used in RelaySimTest, and a value of 100:1 is used as shown.

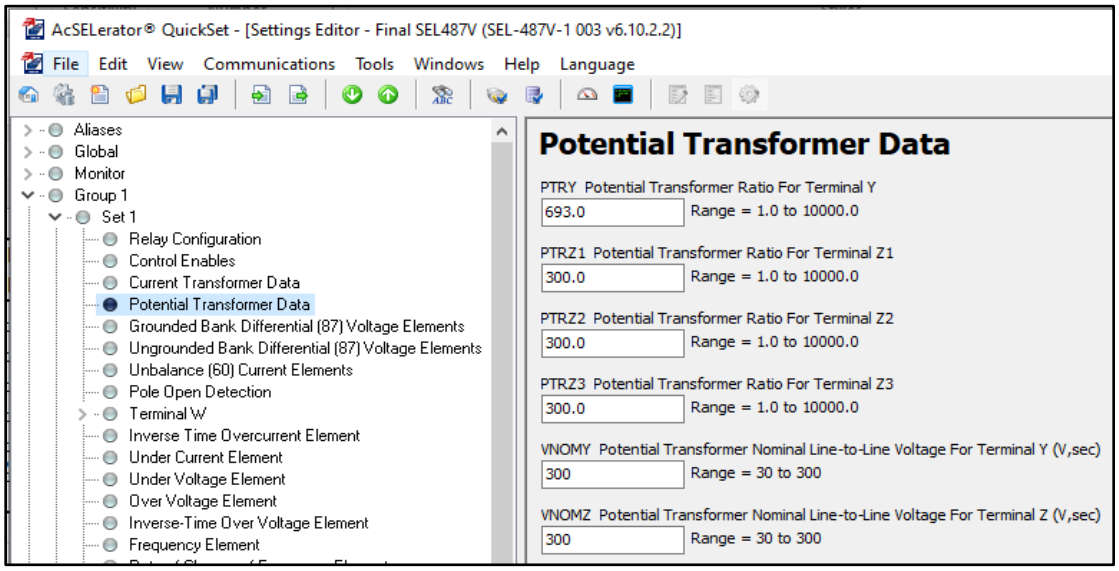

Figure 5.9. VT configuration

Figure 5.9 depicts the voltage transformer ratio setup mentioned in the preceding sections. For consistency of measurements, these settings must be consistent with those used in RelaySimTest, and values of 693:1 and 300:1 are used for bus bar and tap voltages, respectively.

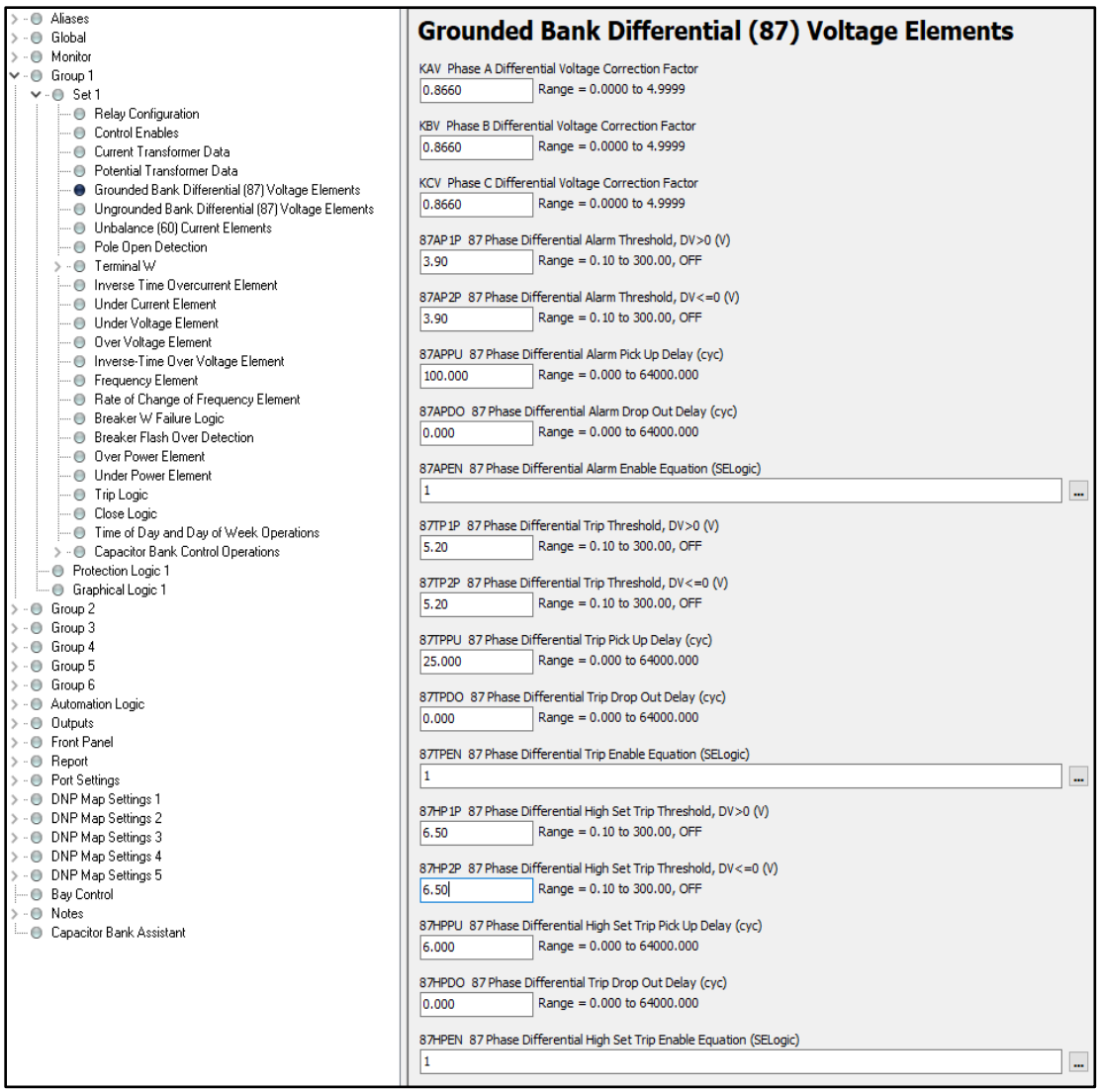

Figure 5.10. Grounded shunt capacitor bank voltage differential configuration

The configuration of voltage differential protection elements is shown in Figure 5.10. The settings used are based on the protective settings calculation results presented in Chapter 4, section 4.3 plus Horton's (2002) recommended time delays. The program enables for the independent setup of distinct dV (differential voltage) values for faults below and above the tap. A value of 0.866 k factor has been configured, along with an alarm pickup of 3.90 V for three capacitor element failures with a delay of 100 cycles, corresponding to 2 seconds or 2000 milliseconds. Pickup settings of 5.20 and 6.5 V for trip and high set have been configured, with 500 milliseconds and 120 milliseconds, respectively.

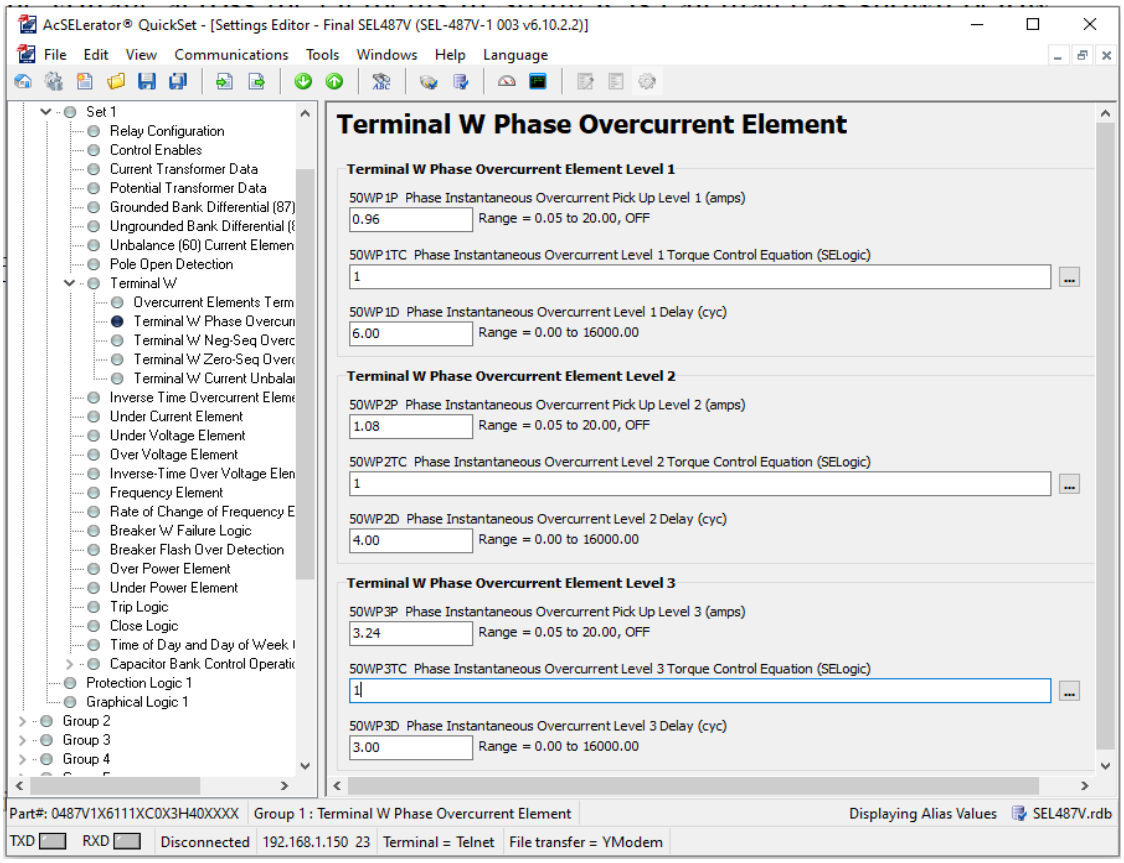

Figure 5.11. Overcurrent element configuration

Specified Minimum Time Overcurrent settings are demonstrated in Figure 5.11, where the pickup current for overcurrent element 1 is set to 96 A primary or 0.96 A secondary with CT ratio of 100:1 and a time delay of 6 cycles, or 120 milliseconds before tripping. element 2 has a pickup value of 108 A with a delay of 80 milliseconds, while element 3 has a pickup value of 324 A with a delay of 60 milliseconds.

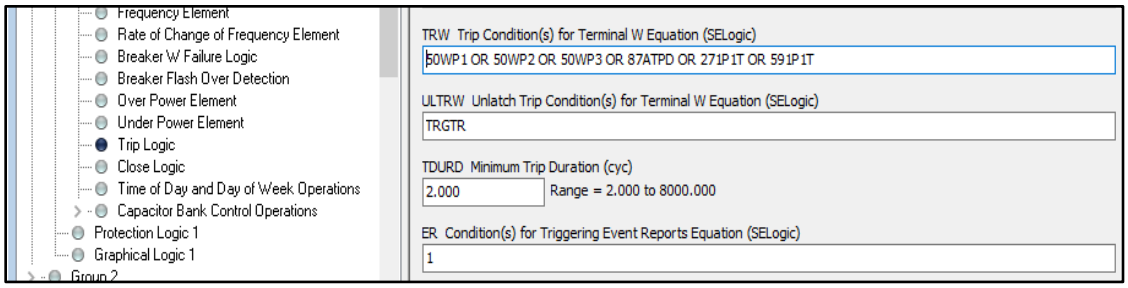

Figure 5.12. TRIP logic configuration

Figure 5.12 depicts trip logic, which decides whether system states or faults trigger the relay to send trip signal to breaker. Overcurrent elements, differential protection elements, and under/over voltage element pickups all generate a relay trip signal, as indicated in the Figure 5.12. In addition, the setup specifies a minimum trip time of 2 cycles or 40 milliseconds as the default value.

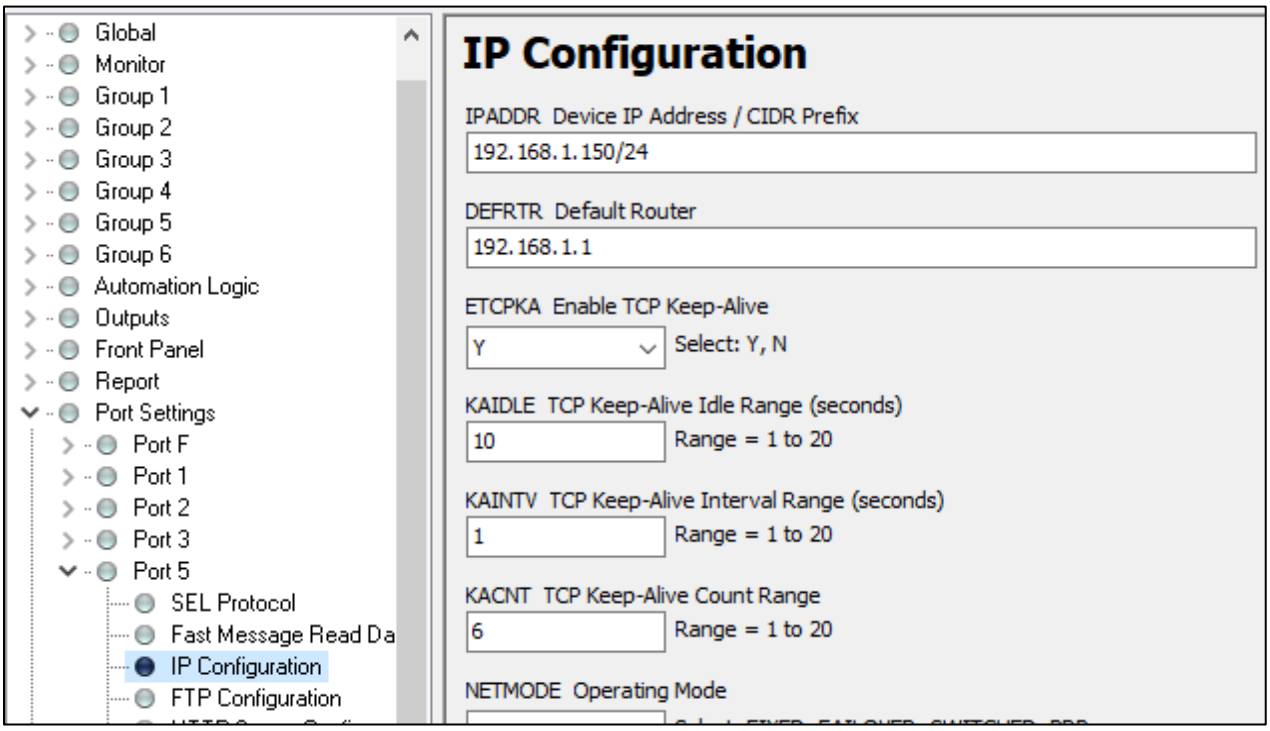

Figure 5.13. IP configuration

Figure 5.13 shows another key parameter that is responsible for communications: the port settings tab, which allows Internet Protocol address adjustments. The correct selection of this parameter enables for proper connectivity with other devices such as the RTAC, which collects data, and the GPS clock for network time synchronization.

The IP address configured is a /24 network, indicating that the last octet is entirely dedicated to hosts, offering 254 useable host IP addresses ranging from 192.168.1.1 to 192.168.1.254. The IP address 192.168.1.255 is designated for broadcasting, while the IP address 192.168.1.0 is reserved for other services. The device's IP address is 192.168.1.150, while the network's default gateway is 192.168.1.1. A default gateway is a device that connects multiple networks by performing routing services.

Table 5.2 depicts the setup of relay target LEDs to help site personnel easily view fundamental system characteristics. As shown in Figure 5.14 to Figure 5.17, various alarm conditions from Table 5.2, such as identification of a faulted phase, above tap, below tap, trip, and so on, are mapped onto the relay target LEDs for ease of inspection, with the RED colour indicating trip conditions and the ORANGE colour indicating alarm conditions. LED 1 is mapped to 87ATPD, which is a voltage differential trip for phase A with the colour RED and latching functionality, as shown in Table 5.2. LEDs 2 and 3 have been arranged identically to the screenshot, with the only variation being the mapping, which indicates differential voltage trip phases B and C, respectively.

Table 5.2. Configuration of the relay target LED

Target LED	ANSI Code	Description	Colour
1	87ATPD	Phase A differential voltage Trip	RED
2	87BTPD	Phase B differential voltage Trip	RED
3	87CTPD	Phase C differential voltage Trip	RED
4	87AHPD	Phase A differential voltage — High set	RED
5	87BHPD	Phase B differential voltage — High set	RED
6	87CHPD	Phase C differential voltage — High set	RED
7	50WP1 50WG1 50WP2 50WG2 50WP3 50WG3	Overcurrent element Level 1 Zero-seq overcurrent element 1 Overcurrent element Level 2 Zero-seq overcurrent element 2 Overcurrent element Level 3 Zero-seq overcurrent element 3	RED
8	271P1 271P2	Under voltage element 1 Under voltage element 2	RED
9	591P1 591P2	Overvoltage Element 1 Overvoltage Element 2	RED
10	87AAP	Phase A differential voltage —Alarm	ORANGE
11	87BAP	Phase B differential voltage —Alarm	ORANGE
12	87CAP	Phase C differential voltage —Alarm	ORANGE
13	87A1PD	Phase differential voltage above tap—Alarm	ORANGE
14	87A2PD	Phase differential voltage below tap—Alarm	ORANGE

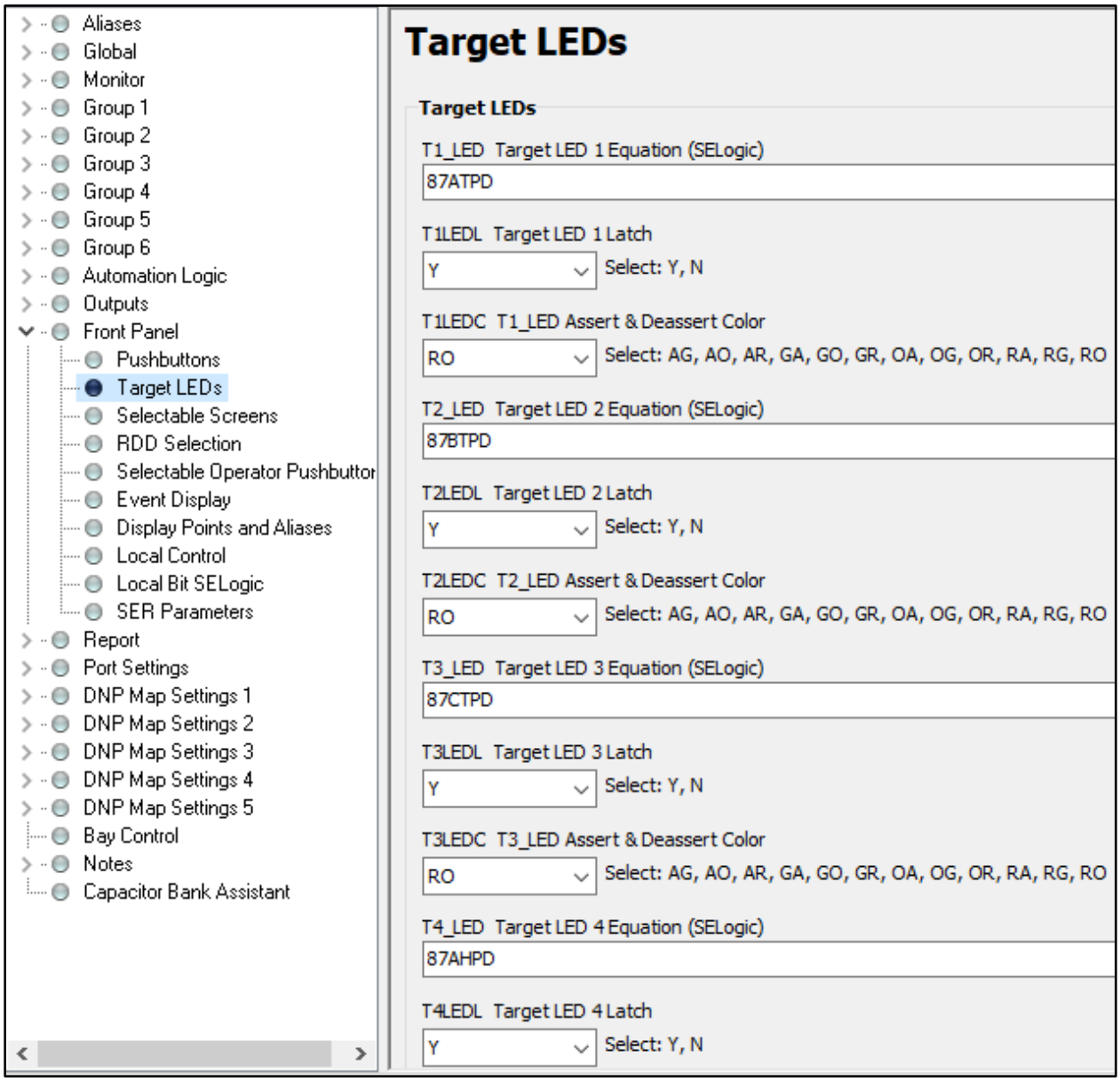

Figure 5.14. Target LED 1 to 4 configuration

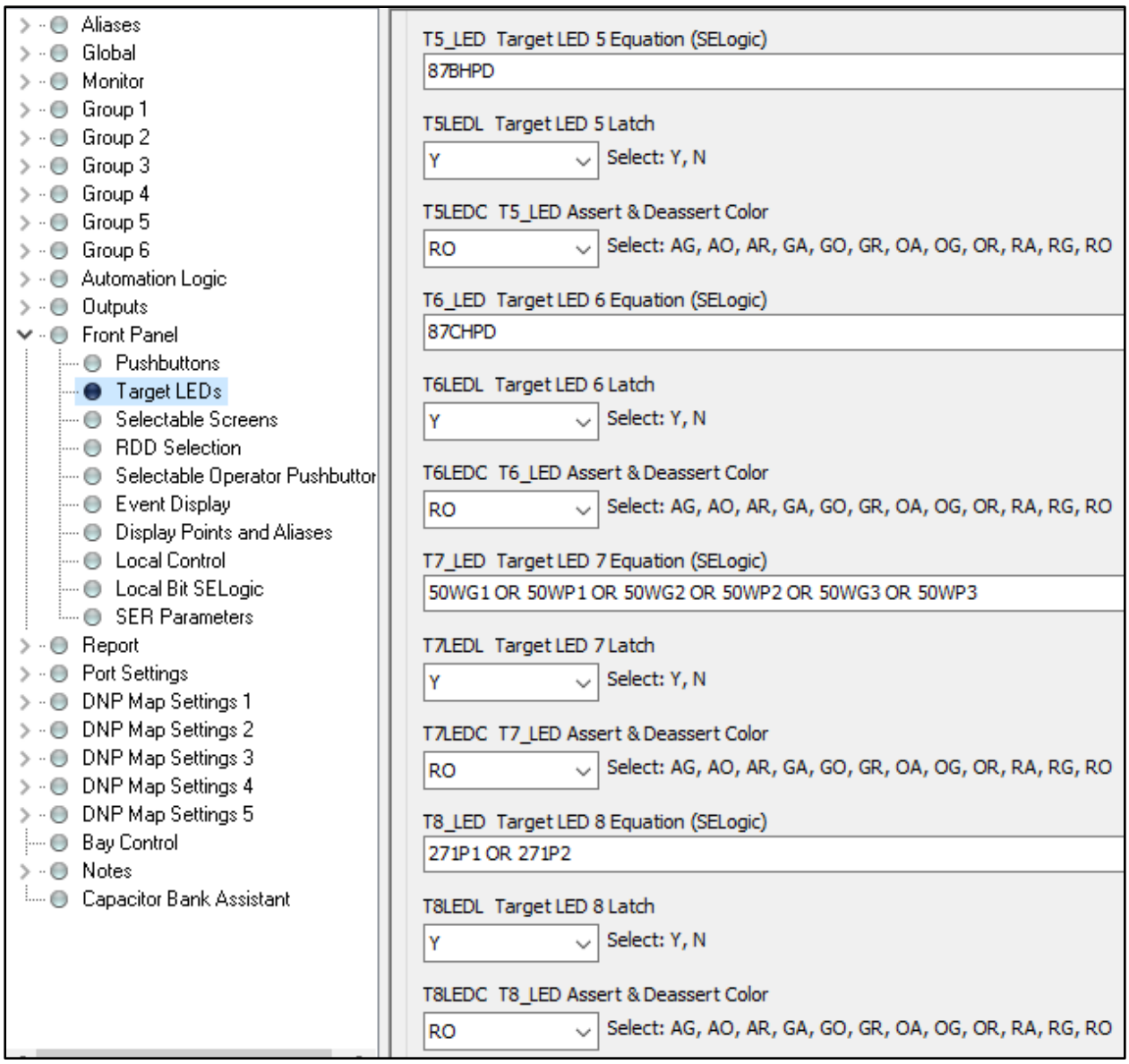

Figure 5.15. Target LED 5 to 8 configuration

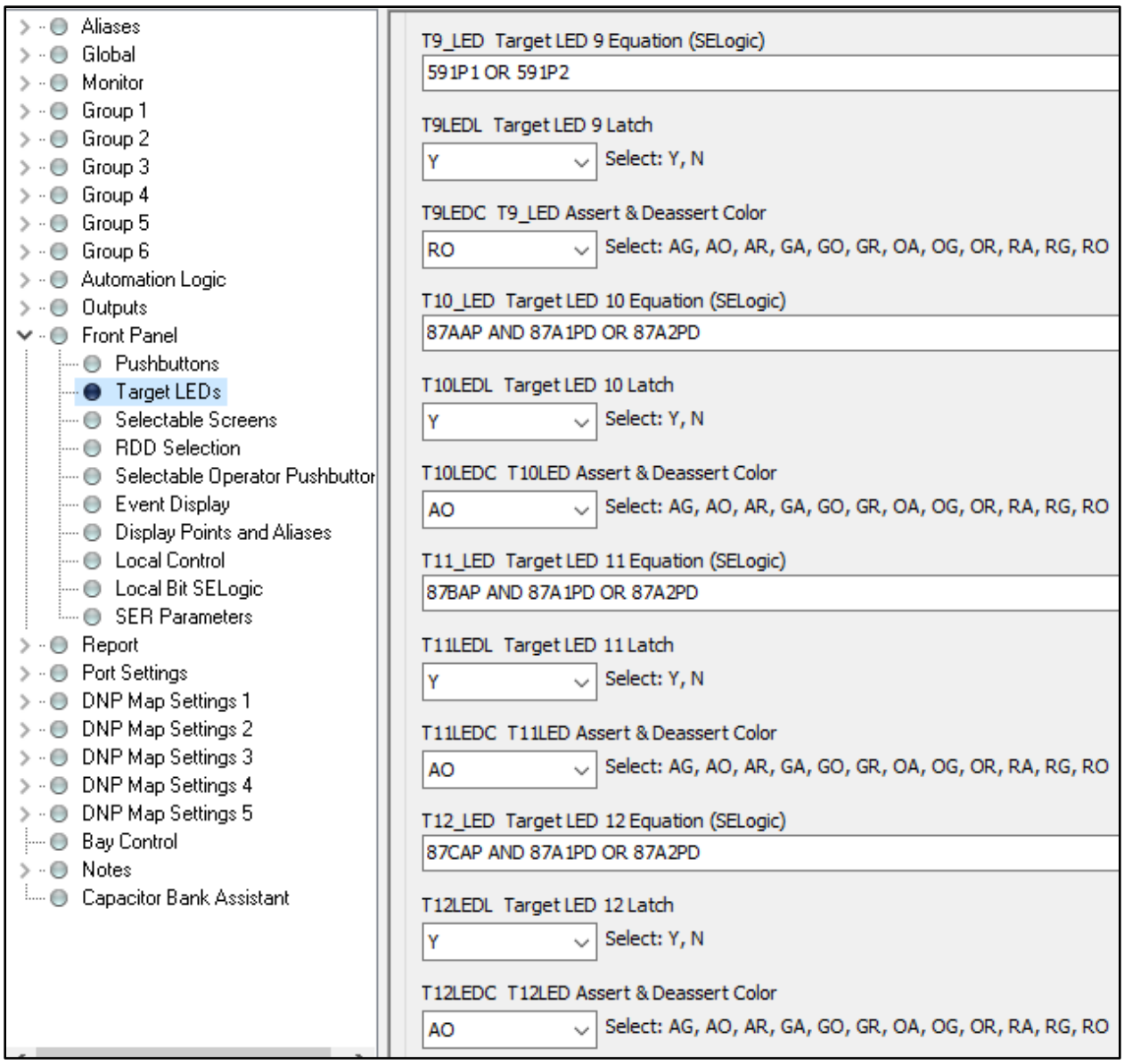

Figure 5.16. Target LED 9 to 12 configuration

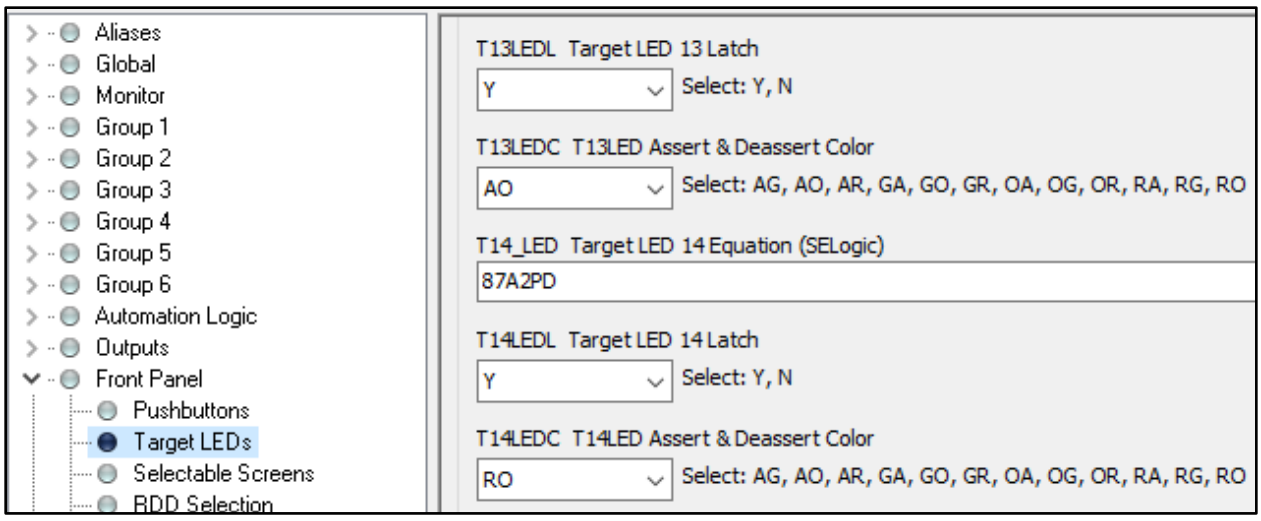

Figure 5.17. Target LED 13 to 14 configuration

The next section discusses IEC 61850 engineering configuration in SEL AcSELerator Architect program.

5.4 IEC 61850 engineering configuration

The section discusses IEC 61850 configuration with MMS for HMI and GOOSE for peer-to-peer communications. The application tool utilized for this purpose is SEL AcSELerator Architect, which is depicted in Figure 5.18, which is the tool's home page. The utility supports configuration using pre-existing SEL device SCL files as well as importing SCL files into the tool. Configuration commences once all SCL files of all network/substation devices have been uploaded.

The configuration of IEC61850 datasets is shown in Figure 5.19. Dataset configuration enables the grouping of tags of a similar type or use to serve a specific purpose. Three datasets were developed for this project: i) SCADA Binaries, ii) SCADA Measurements, and iii) GOOSE Transmit. The names are self-descriptive, however the following explanation is also provided. All binary data selected from the protection relay for SCADA purposes is included in the SCADA Binaries dataset. This dataset is set up as a buffered report, which means that any changes that occur during communication failures are captured and transmitted once communication is restored.

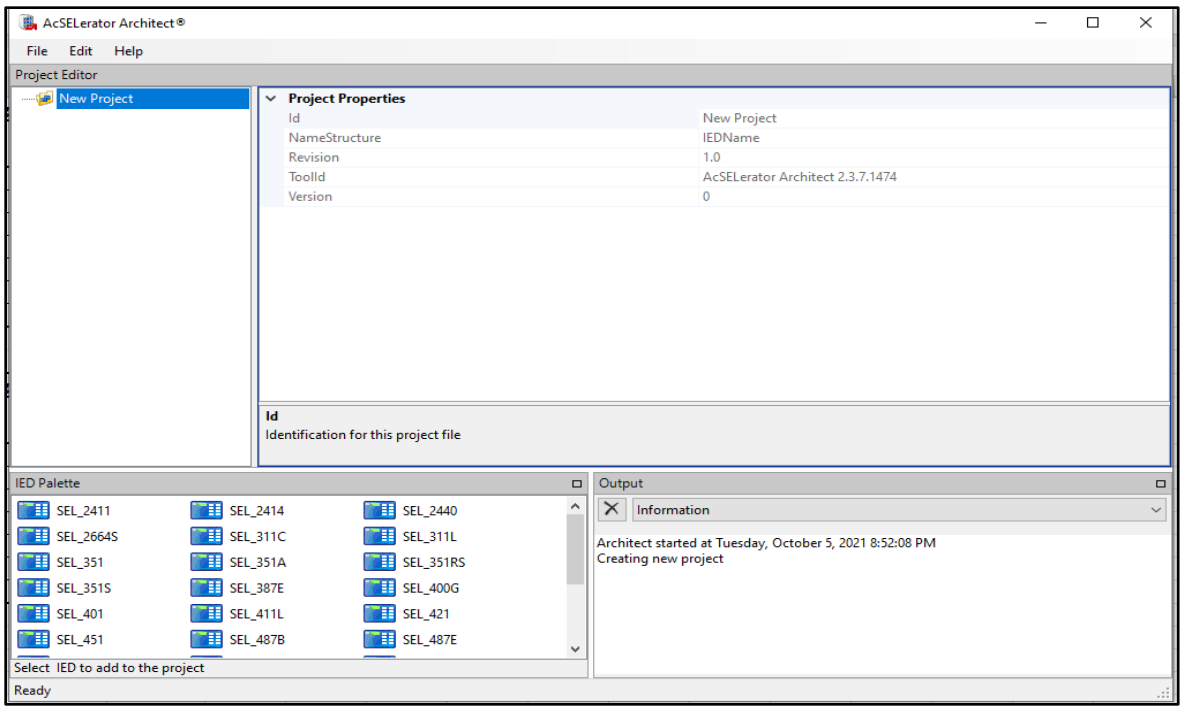

Figure 5.18. SEL AcSELerator Architect home page

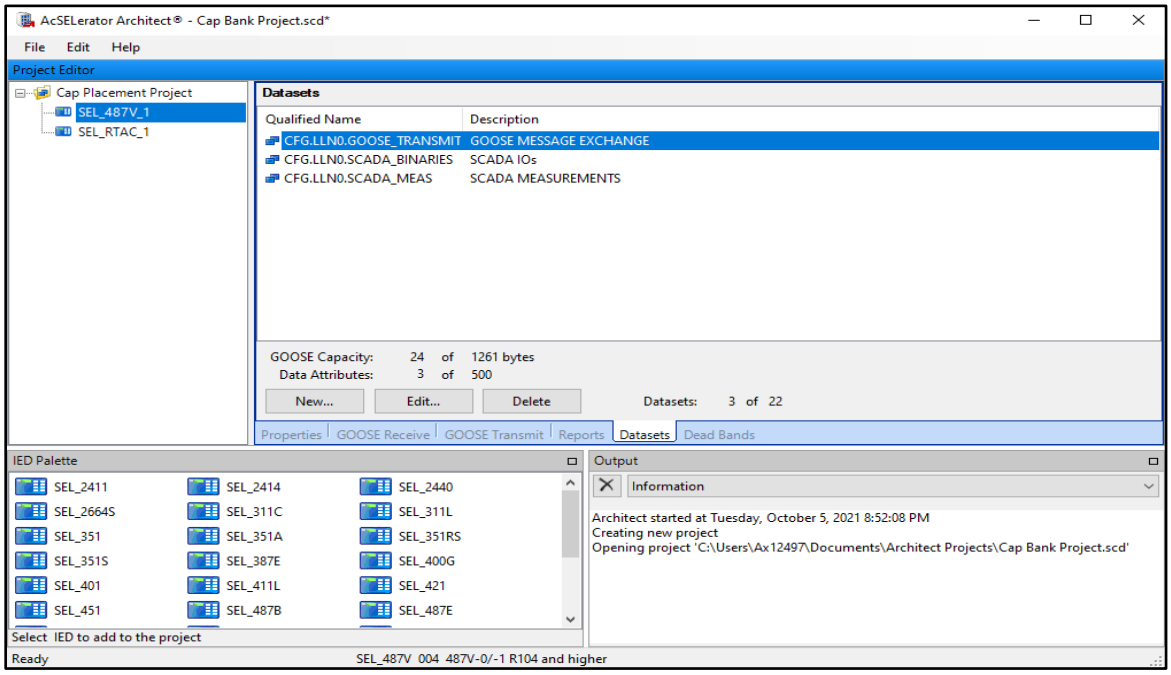

Figure 5.19. Configuring IEC 61850 datasets

Figure 5.20 depicts the ANN.TLEDGGIO1 Logical Node with Ind02 to Ind16 representing the relay target LEDs explained in the preceding section and these are associated with a

conditional trip indicator (trip logic), 87ATPD, 87BTPD, 87CTPD, 87AHPD, 87BHPD, 87CHPD, 50WP1 OR 50WG1 OR 50WP2 OR 50WG2 OR 50WP3 OR 50WG3, 271P1 OR 271P2, 591P1 OR 591P2, 87AAP, 87BAP, 87CAP, 87A2PD, 87A1PD, respectively.

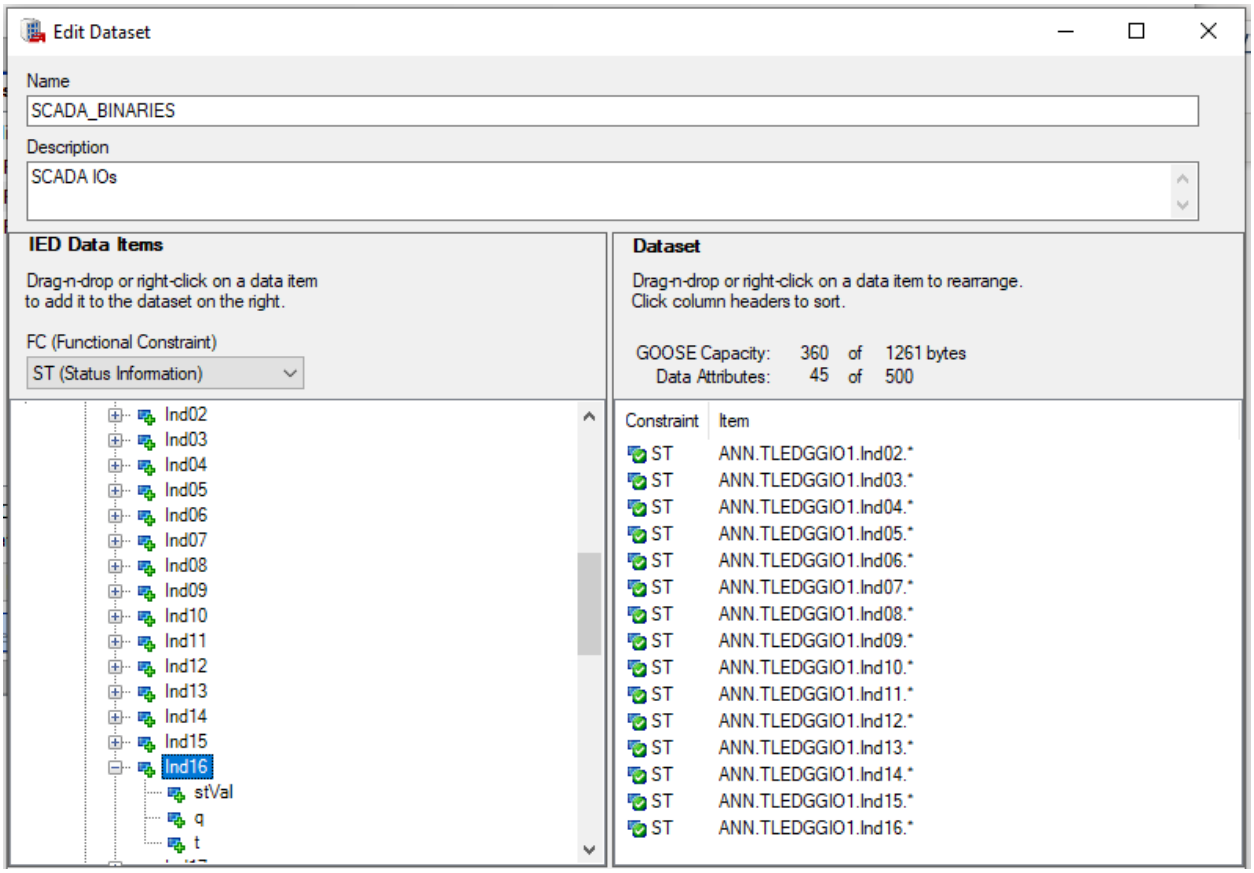

Figure 5.20. SCADA binaries datasets

Internally, ANN.TLEDGGIO1.Ind02 is mapped to relay trip indication, and the user has no access to this setting. The reason for using the ANN.TLEDGGIO1 Logical Nodes instead of mapping directly the logical nodes is that SCADA requires them to be latched as seen on the protection relay because they are transient in nature. SCADA measurement dataset contains all measurements required for SCADA applications and is configured as Unbuffered report, whereas GOOSE transmit specifies which data should be released for other devices to subscribe to. The mapping of relay target LEDs to relay word bits and GGIO logical nodes as established in the IEC 61850 standard for common use is shown in Table 5.3. The Indxx, where xx is a number between 01 and 26, indicate the SEL 487 V relay Light Emitting Diodes (LEDs) as visible on the relay's front panel. Relay Enable and Relay Trip indicators (LEDs) are represented by Ind01 and Ind02, respectively.

Table 5.3. Target LED mapping to logical nodes

Target LED	ANSI Code	Logical Node	Description	Colour
1	87ATPD	TLEDGGIO1.Ind03	Phase A differential voltage Trip	RED
2	87BTPD	TLEDGGIO1.Ind04	Phase B differential voltage Trip	RED
3	87CTPD	TLEDGGIO1.Ind05	Phase C differential voltage Trip	RED
4	87AHPD	TLEDGGIO1.Ind06	Phase A differential voltage — High set	RED
5	87BHPD	TLEDGGIO1.Ind07	Phase B differential voltage — High set	RED
6	87CHPD	TLEDGGIO1.Ind08	Phase C differential voltage — High set	RED
7	50WP1 50WG1 50WP2 50WG2 50WP3 50WG3	TLEDGGIO1.Ind09	Overcurrent element Level 1 Zero-seq overcurrent element 1 Overcurrent element Level 2 Zero-seq overcurrent element 2 Overcurrent element Level 3 Zero-seq overcurrent element 3	RED
8	271P1 271P2	TLEDGGIO1.Ind10	Under voltage element 1 Under voltage element 2	RED
9	591P1 591P2	TLEDGGIO1.Ind11	Overvoltage Element 1 Overvoltage Element 2	RED
10	87AAP	TLEDGGIO1.Ind12	Phase A differential voltage —Alarm	ORANGE
11	87BAP	TLEDGGIO1.Ind13	Phase B differential voltage —Alarm	ORANGE
12	87CAP	TLEDGGIO1.Ind14	Phase C differential voltage —Alarm	ORANGE
13	87A1PD	TLEDGGIO1.Ind15	Phase differential voltage above tap—Alarm	ORANGE
14	87A2PD	TLEDGGIO1.Ind16	Phase differential voltage below tap—Alarm	ORANGE

As indicated in Table 5.3, Ind03 through Ind24 are user programmable and may be mapped to any indication of choice, however Ind01 and Ind02 are not user configurable. SCADA Measurements dataset utilizing METWMMXU1 and METWMMYU1Logical Nodes is shown in Figure 5.21. As the server or source of data, the aforementioned is configured on the SEL 487V relay. The measurements configured are described in Table 5.4, which is based on the reference (SEL 487V relay instruction manual, 2015).

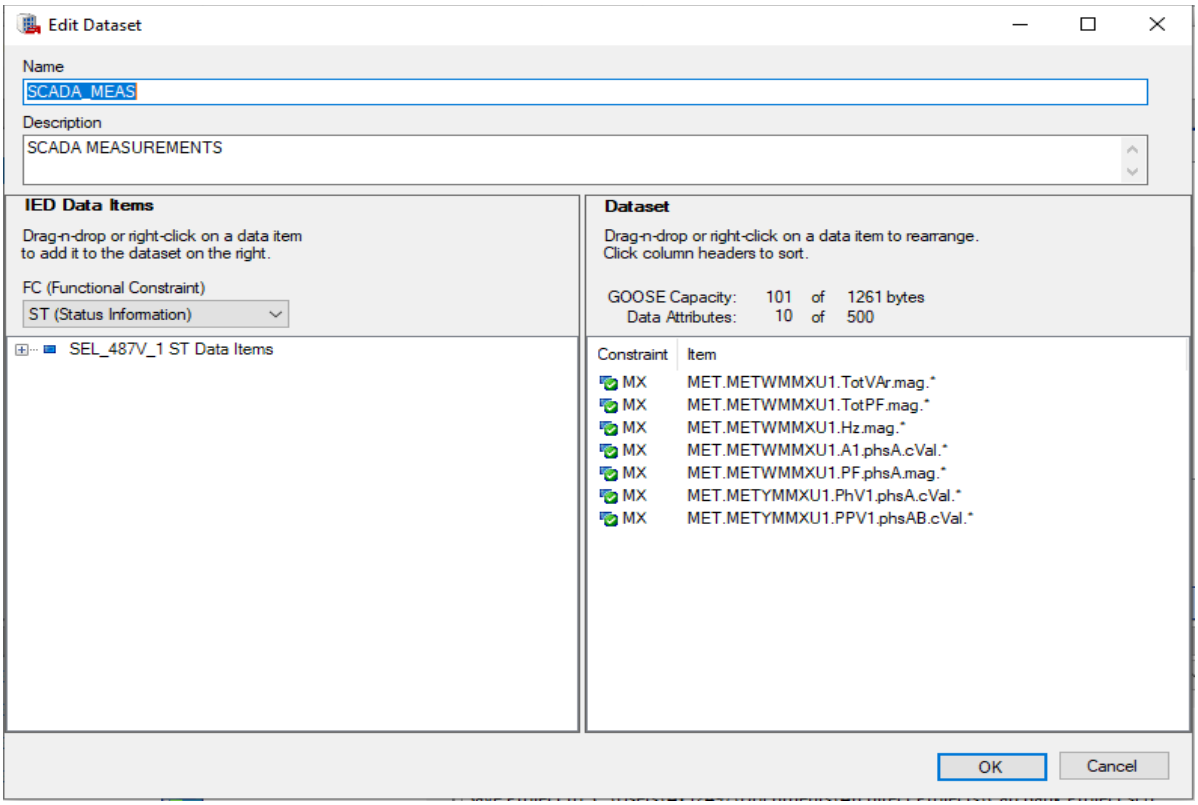

Figure 5.21. SCADA measurements datasets

Table 5.4. Measurements logical nodes description

Logical Node Path	**Description**
MET.METWMMXU1.Tot.VAr.mag	3 phase reactive power on terminal W
MET.METWMMXU1.TotPF.mag	3 phase power factor on terminal W
MET.METWMMXU1.Hz.mag	Tracking frequency
MET.METWMMXU1.A1.phsA.cVal	Phase A current on terminal W
MET.METWMMXU1.PF.phsA.mag	Phase A power factor terminal W
MET.METYMMXU1.PhV1.phsA.cVal	Phase A voltage on terminal Y
MET.METYMMXU1.PPV1.phsAB.cVal	Phase A to phase B voltage on terminal Y

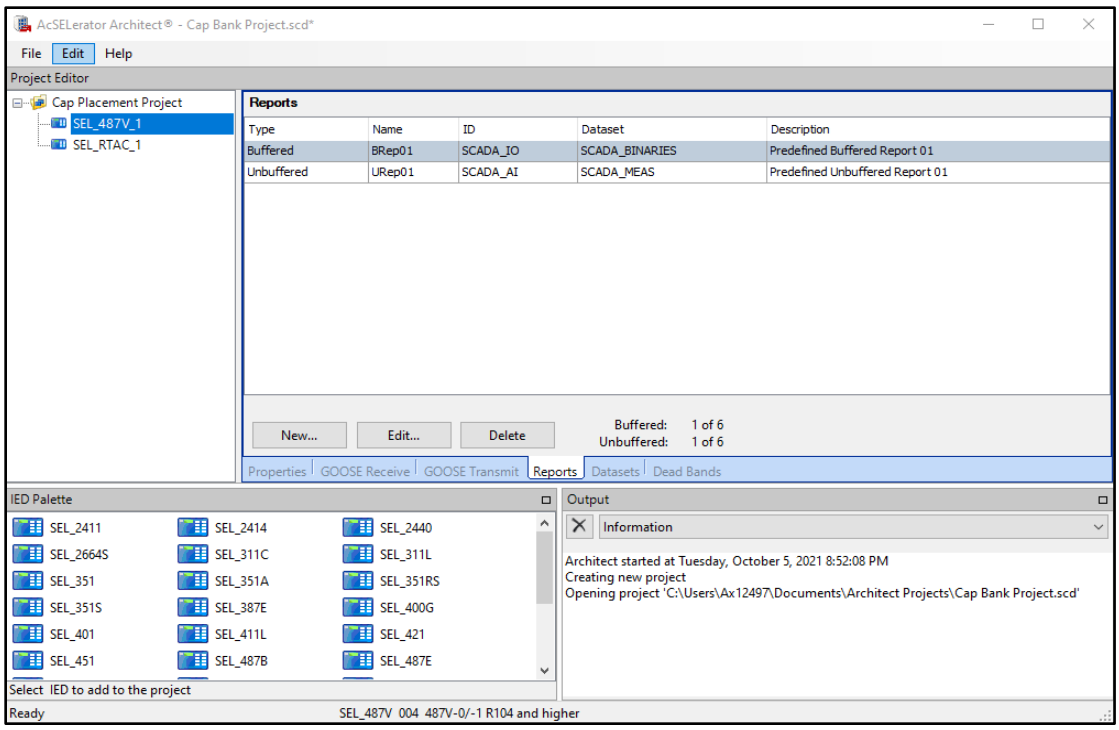

Figure 5.22. Buffered and unbuffered reports

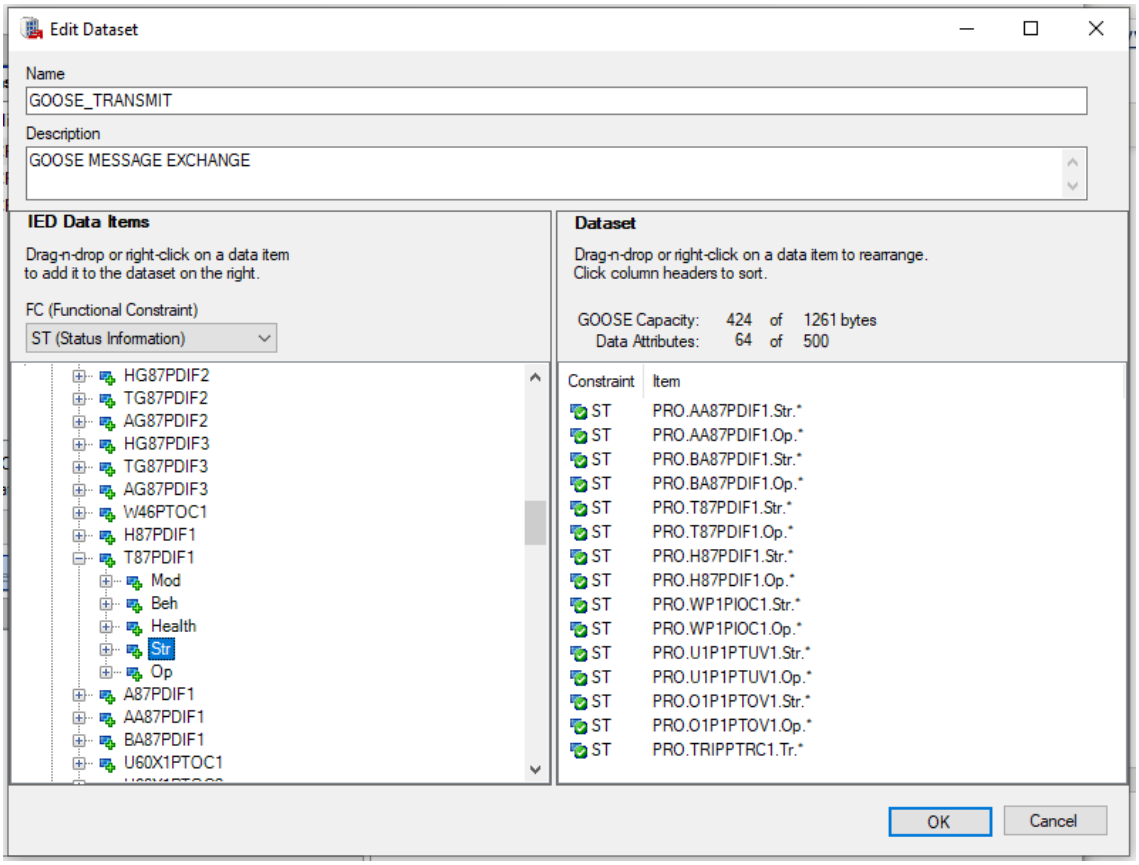

Figure 5.23. IEC 61850 GOOSE protection datasets

Figure 5.22 depicts the reports configuration in which Buffered Report Control Block (BRCB) and Unbuffered Report Control Block (URCB) are allocated to the SCADA Binaries and SCADA measurements datasets, respectively. Figure 5.23 depicts the GOOSE Transmit dataset configuration, in which all protection Logical Nodes given in Table 5.5 are mapped on the dataset for publishing with both quality and time indications. The description of these Logical Nodes, as stated in the IEC 61850 standard and derived from the SEL 487V relay manual, is shown in Table 5.5.

Table 5.5. Protection logical nodes description

Logical Node Path	Description
PRO.AA87PDIF1.Op	Phase differential voltage timed out above tap - Alarm
PRO.BA87PDIF1.Op	Phase differential voltage timed out below tap - Alarm
PRO.WP1PIOC1.Op	Phase torque-controlled overcurrent element level 1 asserted
PRO.H87PDIF1.Op	Instantaneous phase differential voltage timed out - High set
PRO.T87PDIF1.Op	Instantaneous phase differential voltage timed out - Trip
PRO.U1P1PTUV1.Op	Under voltage element 1, level 1 timed out
PRO.O1P1PTOV1.Op	Overvoltage element 1, level 1 timed out
PRO.TRIPPTCR1.Tr	Conditionaltrip signal asserted

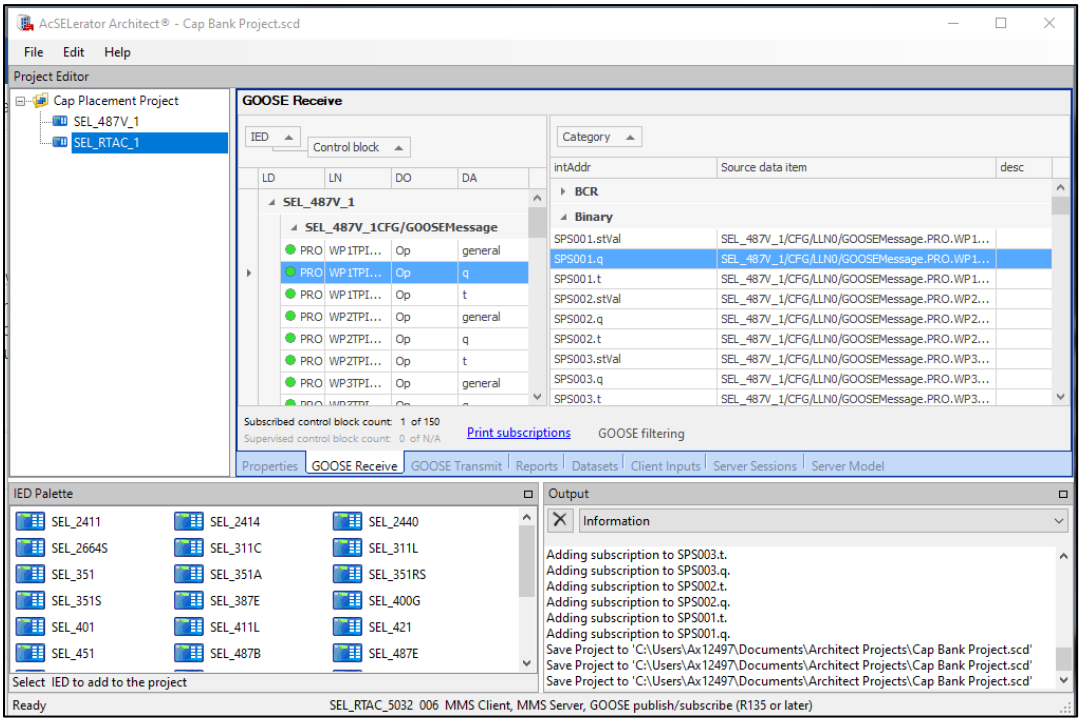

Figure 5.24. SEL RTAC GOOSE receive

Figure 5.24 depicts the SEL RTAC GOOSE Receive dataset configuration, in which all protection Logical Nodes as shown on the GOOSE Transmit dataset in Figure 5.23, is subscribed to by the SEL RTAC device.

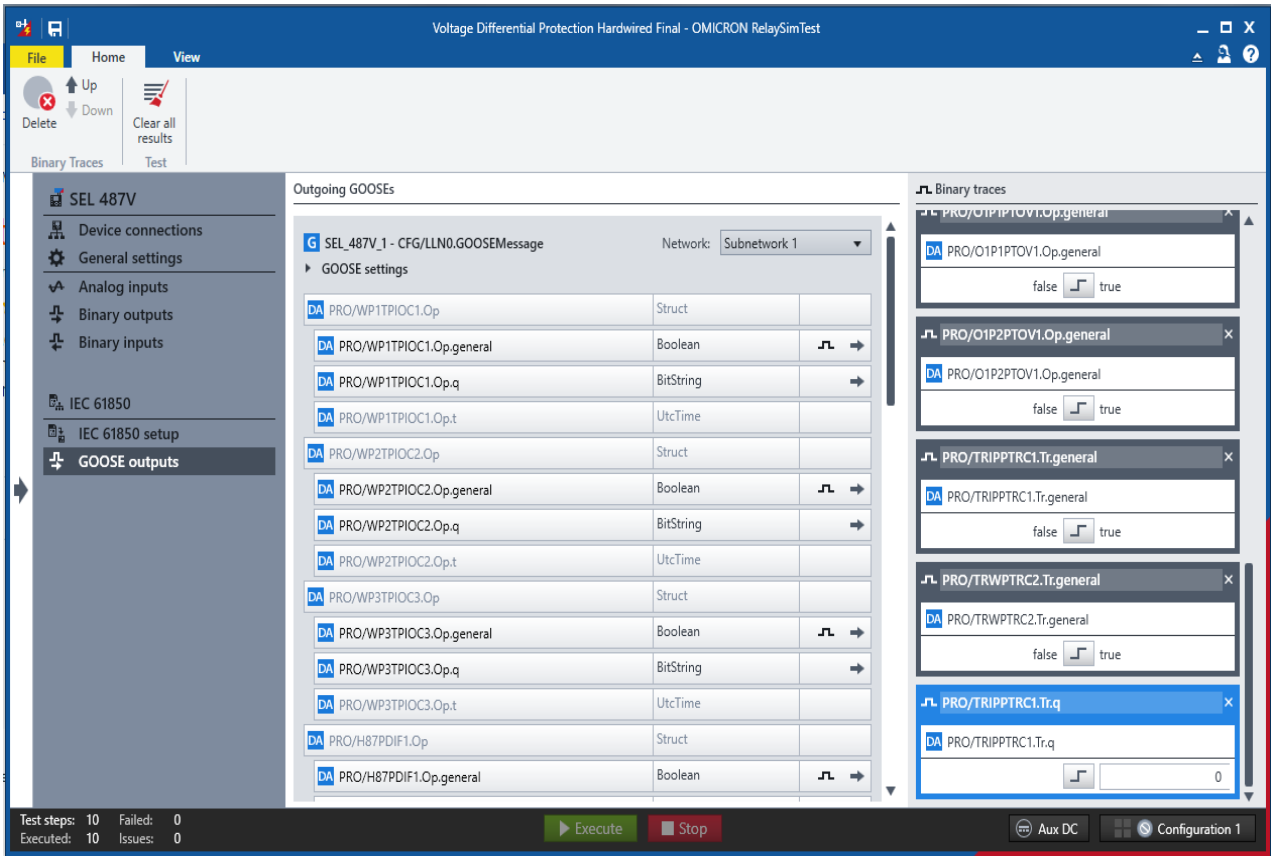

Figure 5.25. IEC 61850 SCD GOOSE subscription file imported into RelaySimTest

Figure 5.25 depicts GOOSE subscription of RelaySimTest to GOOSE Transmit dataset shown in Figure 5.23 which is imported for GOOSE subscription into RelaySimTest software. Figure 5.26 depicts the procedure for sending the SEL 487V SCL file to the protection relay through File Transfer Protocol (FTP). For a successful transfer of SCL files, details such as IP address, login, and password must be provided, as indicated in the Figure 5.26. The file is saved as *.scd, indicating that it is now a substation configuration description file for the entire project/substation, rather than just the specific IED or device. The SCD file is then imported into the RTAC gateway and RelaySimTest, allowing these devices to communicate and subscribe to the published dataset.

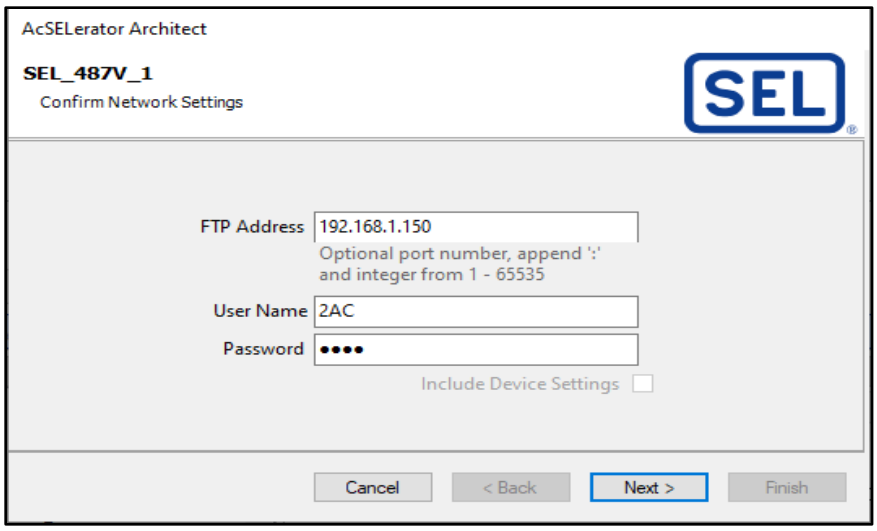

Figure 5.26. Loading substation configuration language file into SEL487V relay

The next section discusses the engineering configuration of the SEL RTAC substation gateway utilizing AcSELerator RTAC software.

5.5 Substation gateway engineering configuration

A substation gateway (SEL RTAC 3555) is used to collect data from all IEDs connected to assist with alert notification and HMI testing. The section discusses the configuration that is created for the RTAC device to support this application. Figure 5.27 depicts the AcSELerator RTAC software's home page. Once logged in, it is possible to create a new project, read from the RTAC device if it is connected, or import a saved/exported project, as illustrated in Figure 5.28, and also update the device firmware, if necessary. The user's name is admin, the password Admin123# and IP address is 192.161.1.170 to login into the RTAC device.

Figure 5.28 appears after a successful login in the RTAC software and displays a list of available projects, if any, the user who created or last edited the projects, the date and time, whether the project is accessible or locked for the logged in user, the firmware version used to create the project, and the device type for which the project was created. The RTAC project generated for this application is called Capacitor Bank Project, it was last updated on October 31, 2021, and it is using RTAC version R142 for the SEL RTAC 3555 device.

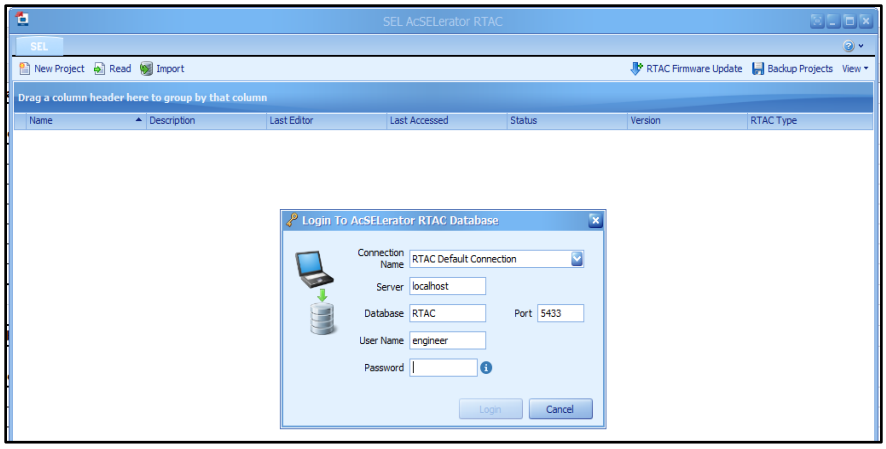

Figure 5.27. SEL AcSELerator RTAC home page

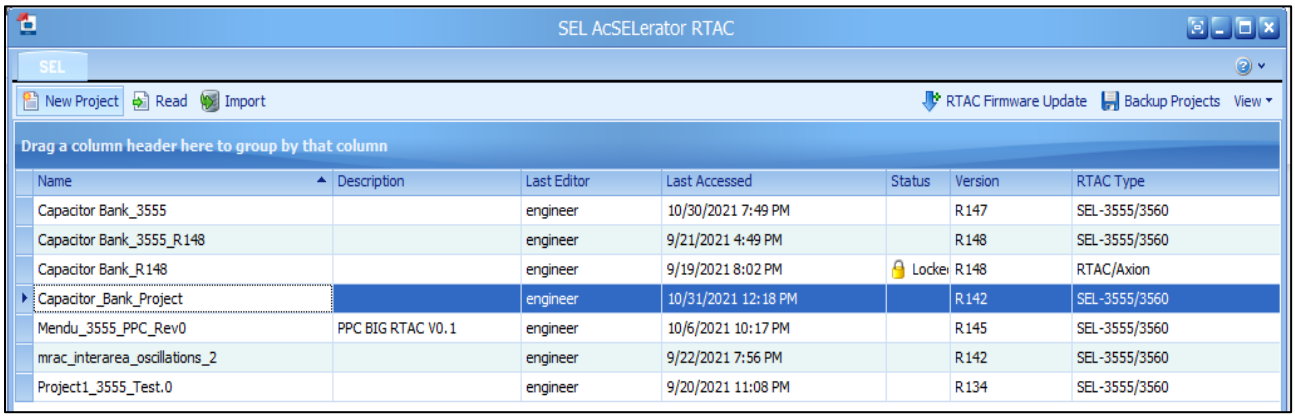

Figure 5.28. SEL RTAC project files

As illustrated in Figure 5.29, the RTAC device also offers web services, which allow for the creation of basic parameters such as IP addresses, user accounts, and so on. The picture also shows any HMI runtime programs that are present. To use the Web interface, open Internet Explorer and enter the RTAC IP address and login information. The screen in Figure 5.29 is displayed after a successful login. This page contains essential information about the device, such as the firmware version loaded, any projects loaded, the state of the Ethernet card, and so on. Some information is indicated with True or False which representing whether a certain configuration is active (True) or in inactive (False), for example, Eth03 to Eth10 are not configured/operational.

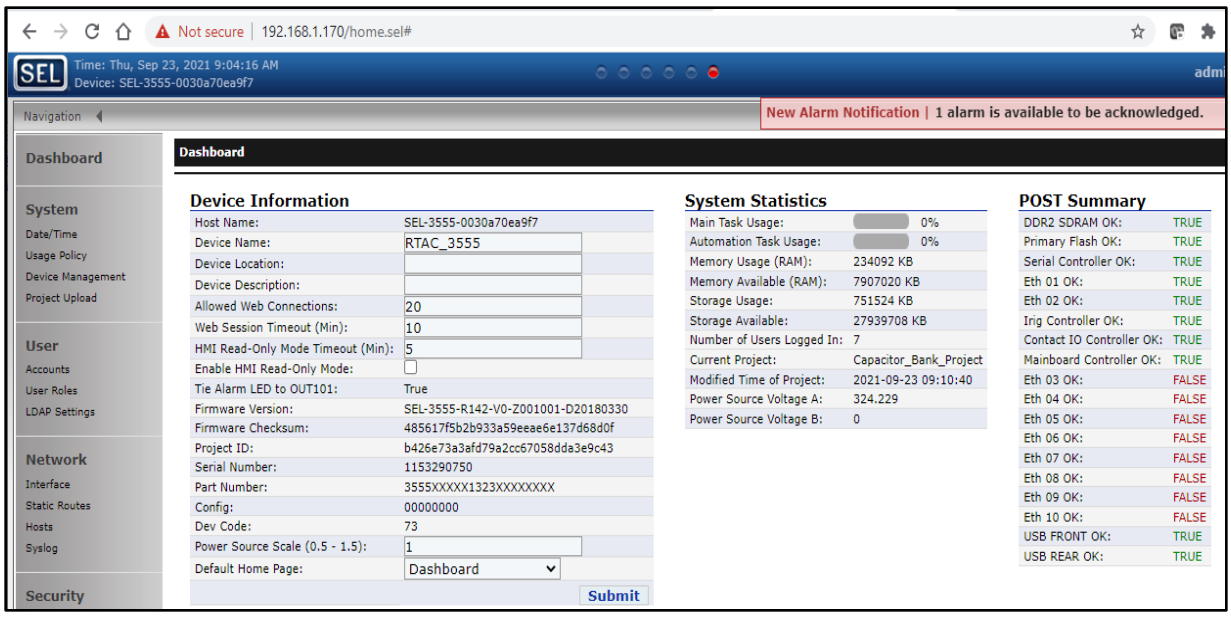

Figure 5.29. SEL RTAC web page configuration

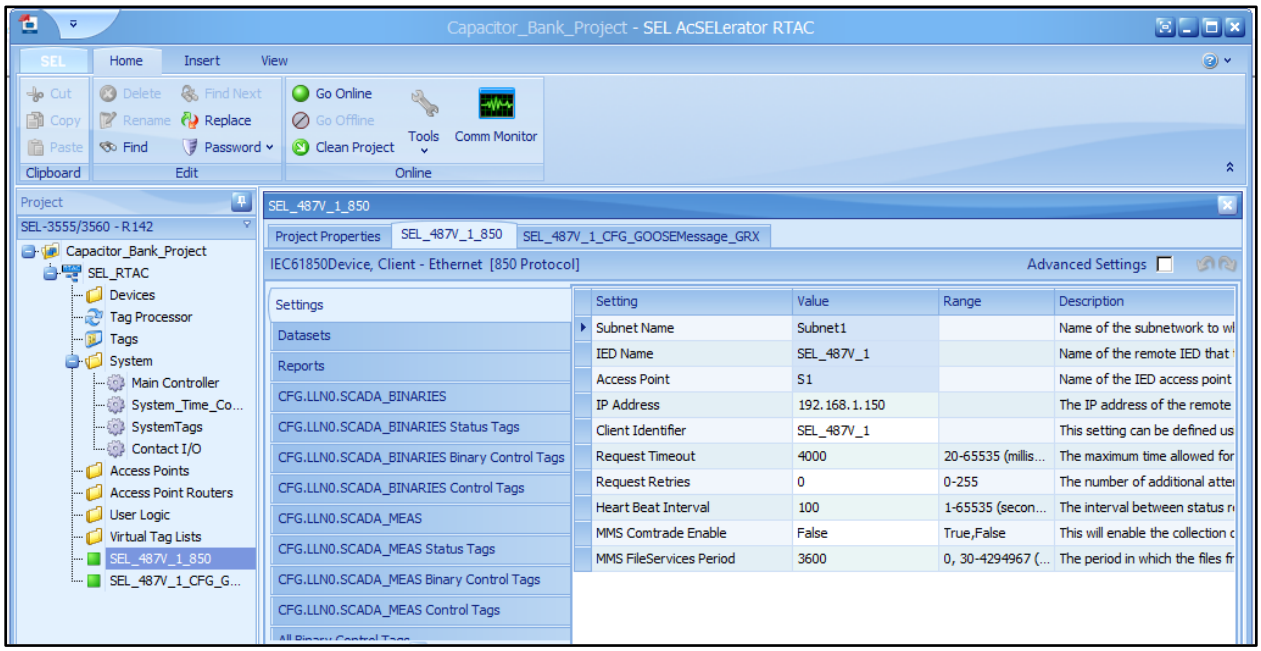

Figure 5.30. SEL RTAC IEC 61850 configuration

Figure 5.30 depicts a loaded RTAC configuration in the unit, which was built by importing a SEL AcSELerator Architect file (.SCD) into the RTAC. The Figure depicts only one device connected to the RTAC for data collection through the IEC 61850 standard. The RTAC is only collecting data from the SEL 487V relay, despite the presence of two green

connection symbols. These icons reflect the communication types (methods) employed, which in this case are Manufacturing Message Specification (MMS) and Generic Object Oriented Substation Event (GOOSE). When you imported SCD file, RTAC create two sperate tag groups for MMS and GOOSE as shown in Figure 5.30.

Figure 5.31 depicts the MMS Datasets as configured in the Architect software, whereas Figures 5.32 and 5.33 depict the data included within these Datasets. SCADA Binaries DataSet displays binary input data, while SCADA Meas DataSet displays measurements. RTAC takes data from the reports generated (buffered and unbuffered) by the SEL 487V relay via MMS communication. These reports are used for SCADA and HMI. RTAC, on the other hand, subscribes to the dataset published by the SEL 487V relay for GOOSE communication. Figure 5.34 depicts the GOOSE Transmit Datasets as configured in the SEL AcSELerator Architect software, with the data mapped inside as detailed in the preceding section.

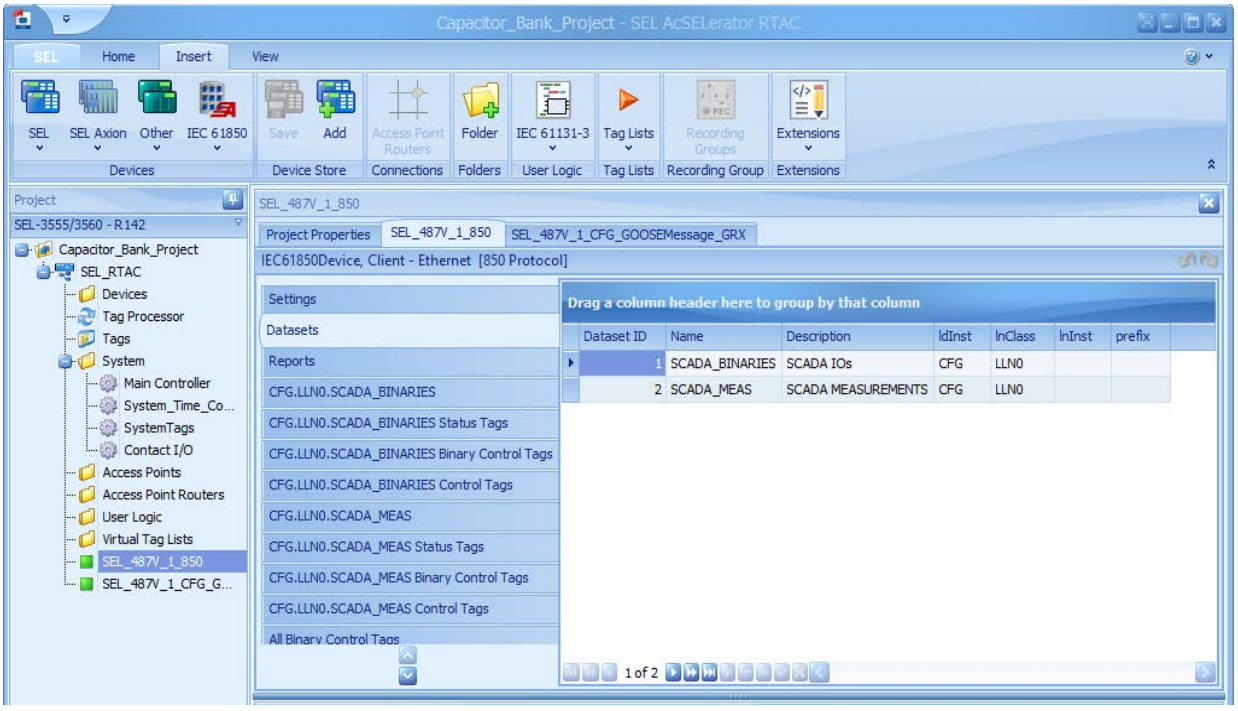

Figure 5.31. IEC 61850 datasets in SEL RTAC

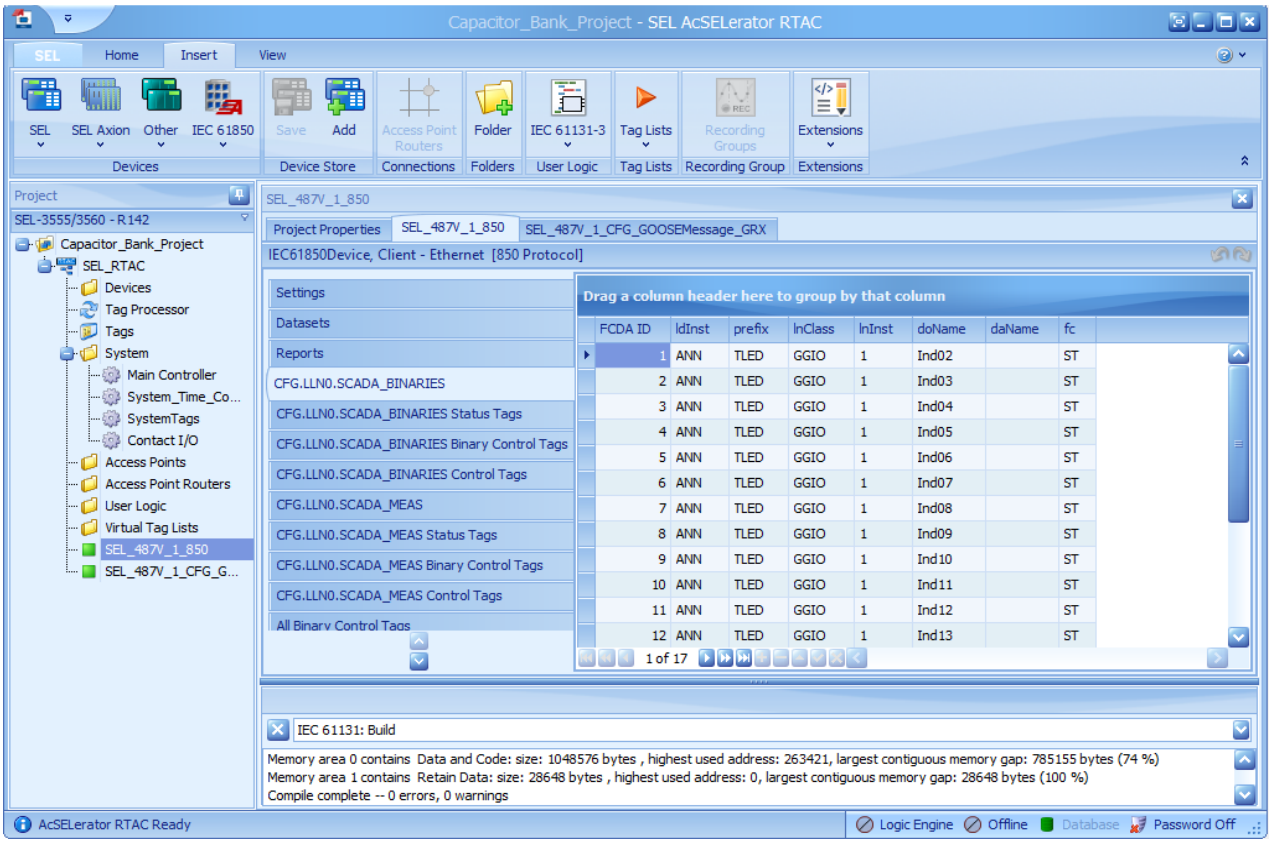

Figure 5.32. SEL RTAC IEC 61850 SCADA binaries dataset

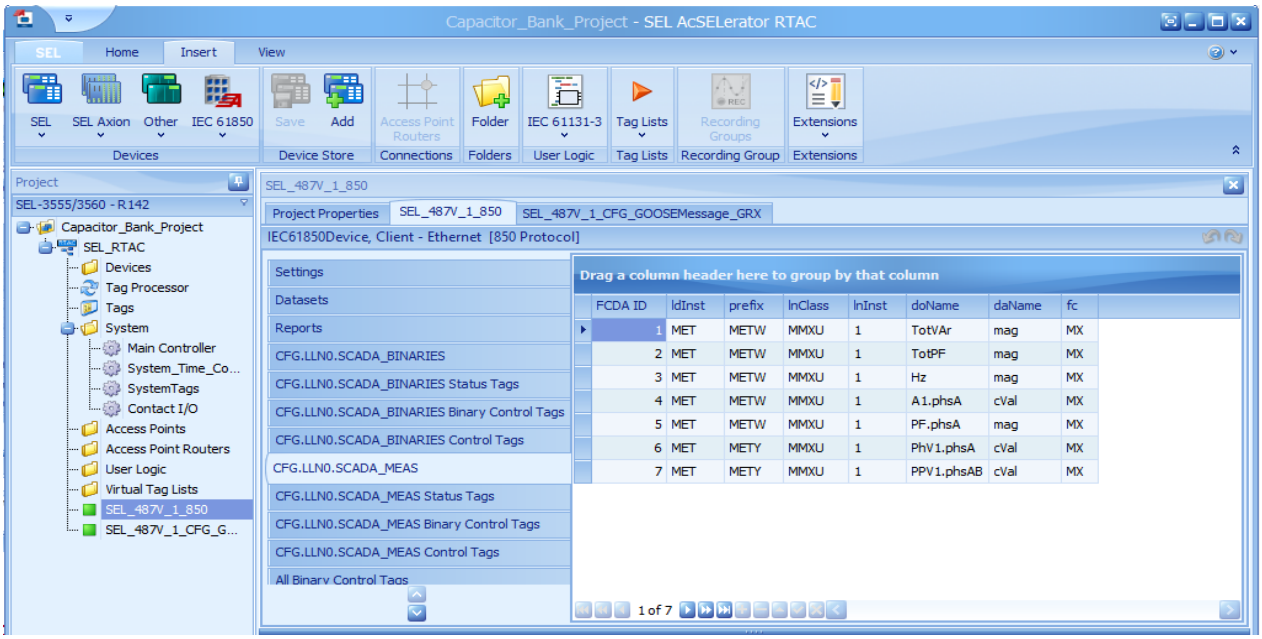

Figure 5.33. SEL RTAC IEC 61850 SCADA measurement dataset

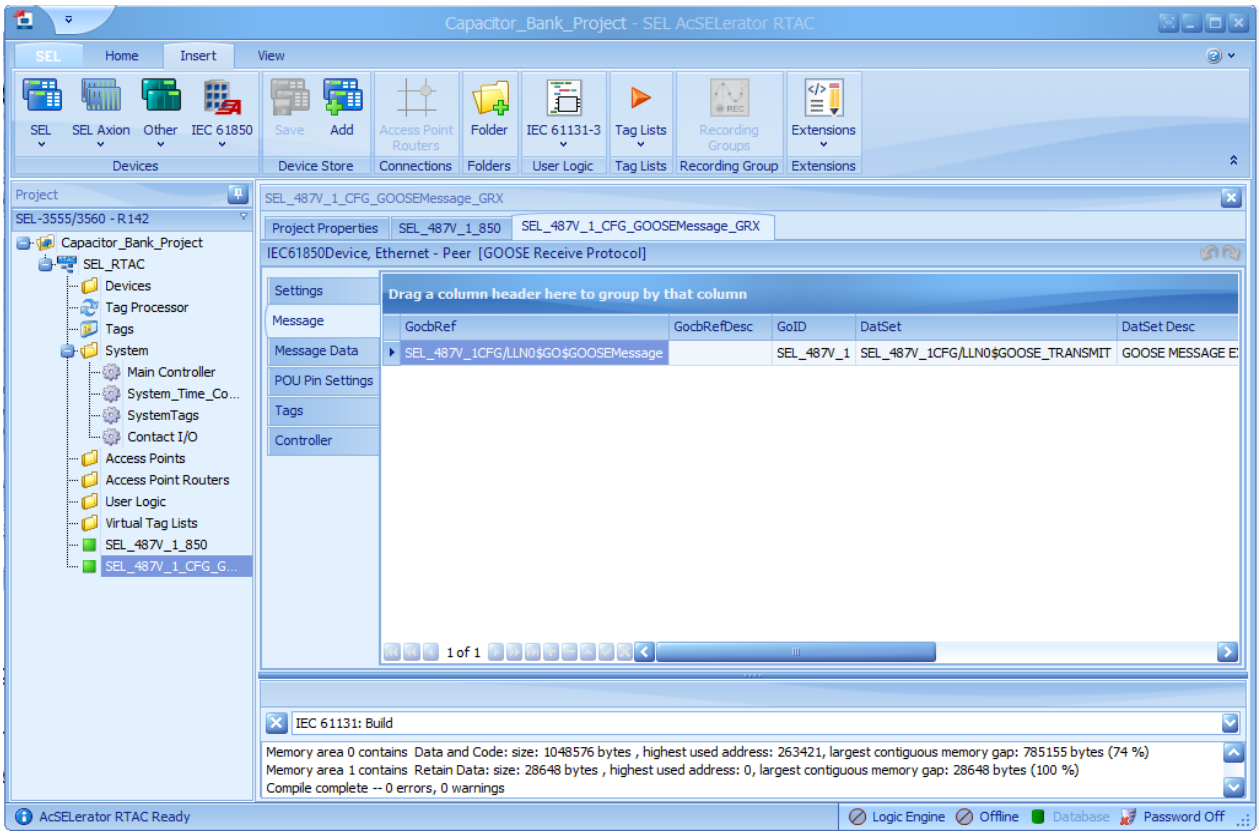

Figure 5.34. SEL RTAC IEC 61850 GOOSE transmit subscription

As previously stated, Figure 5.34 depicts the RTAC device's subscription to the GOOSE Transmit Dataset. The following section covers the time synchronization process that use a GPS clock.

5.6 Global Positioning System (GPS) engineering configuration

In order to execute the test cases, RelaySimTest requires time synchronization. As a result, a GPS clock is used to verify that all devices under test are time synchronized. The project makes use of a SEL 2488 GPS clock that can be configured using a web interface, as shown in Figure 5.35. The SEL 2488 device is accessed using following username, Admin and password Admin123#. Provide the physical connection diagram from GPS antenna to SEL satellite clock and from SEL Clock to CMCs.

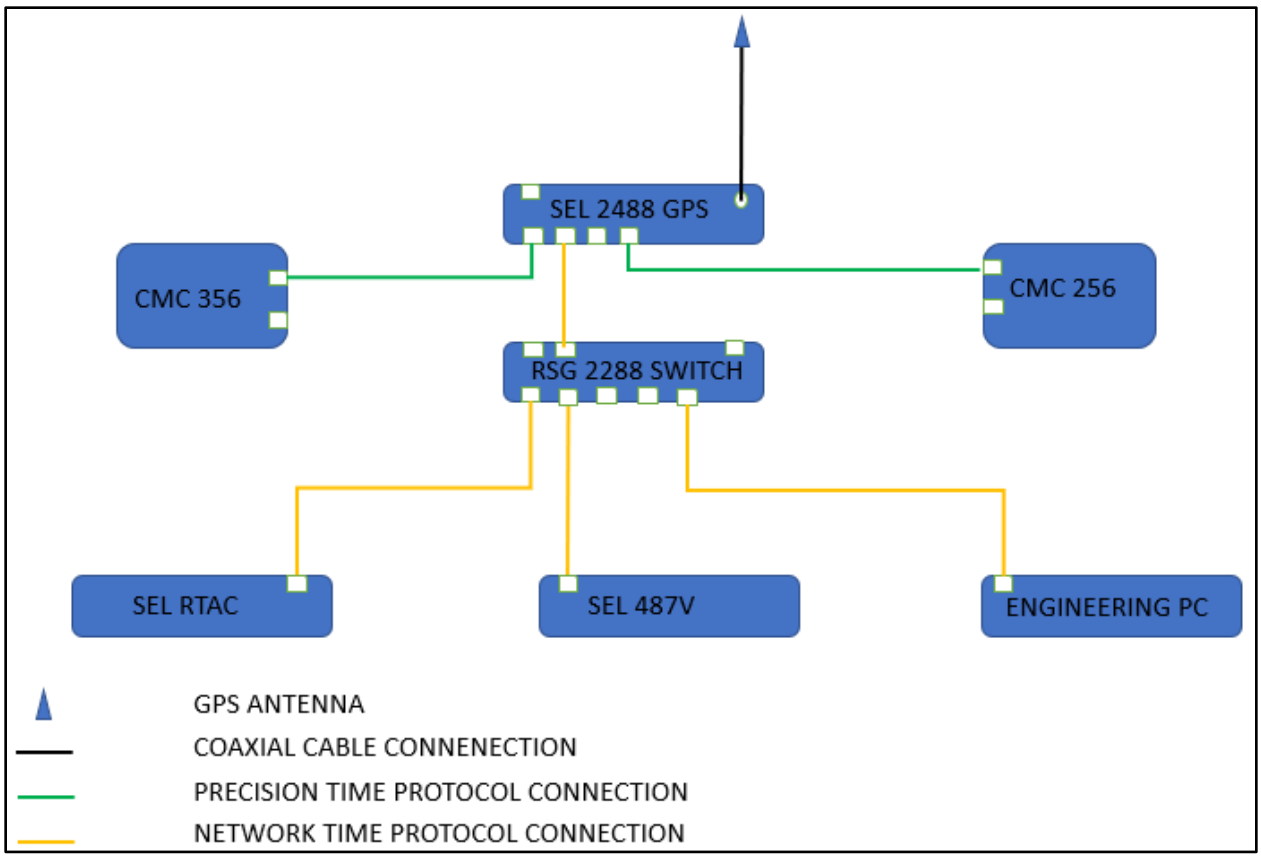

Figure 5.35. GPS clock and time synchronization connection diagram

In order to obtain correct time, the GPS unit is attached to an antenna that connects to a satellite in space as shown in Figure 5.35 with NTP and PPT connections. Four Ethernet ports have been activated, as illustrated in Figure 5.37. The front port is used for device configuration, ETH 1 is configured as the Network Time Protocol server (NTP server) as shown in Figure 5.36, which provides time synch messages via the Transmission Control Protocol (TCP), and ETH 2, ETH 3 and ETH 4 are configured as Precision Time Protocol servers (PTP server) as shown in Figure 5.37 and these PTP ports are connected directly on port 2 of the CMCs.

NTP services are used to synchronize hardware such as the SEL 487V and SEL RTAC over a local area network (LAN). The network address of the utilized LAN is 192.168.1.0/24. The IP address 192.168.1.13 is used for the NTP server configuration (ETH 1), whereas the IP address 192.168.2.2 is used for the ETH F (front port) for device configuration. PTP communicates on a lower level (Data Link) on the Open System Interconnect stack, which does not require IP addresses, so Media Access Control (MAC) addresses are used for the other two ports.

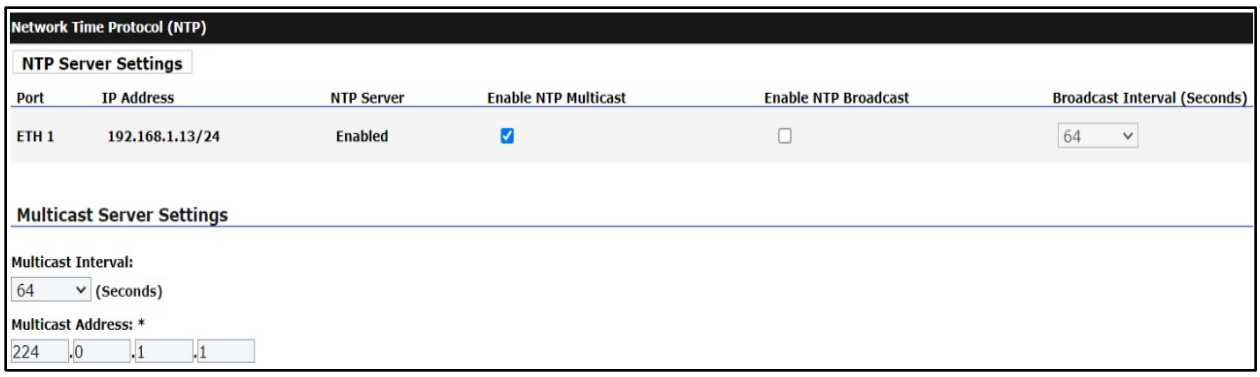

Figure 5.36. SEL 2488 GPS clock NTP configuration

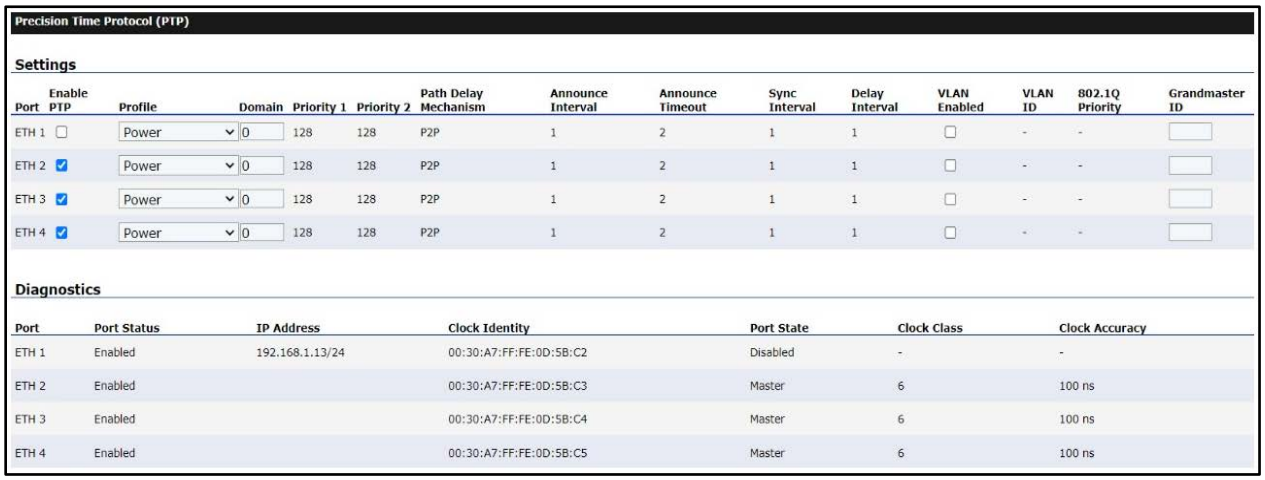

Figure 5.37. SEL 2488 GPS clock PTP configuration

Figure 5.38 depicts a screenshot with one CMC that is not synchronized. CMC 256 + indicates that time synchronisation is in progress and that the device is searching for satellites, whereas CMC 356 is successfully synchronised and ready for execution. The synchronised device additionally indicates that it was synced using the Precision Time Protocol. It is not possible to conduct the test cases with only one CMC or no CMC synchronized, hence both CMCs must be synchronized. The configuration of ETH 2 and ETH 1 on the SEL 2488 device, which are configured solely for PTP time sync messages, and the direct connection to ETH 2 of the CMCs to guarantee that network switches are not overloaded, is working well, as shown in Figure 5.39 with both CMCs synchronized.

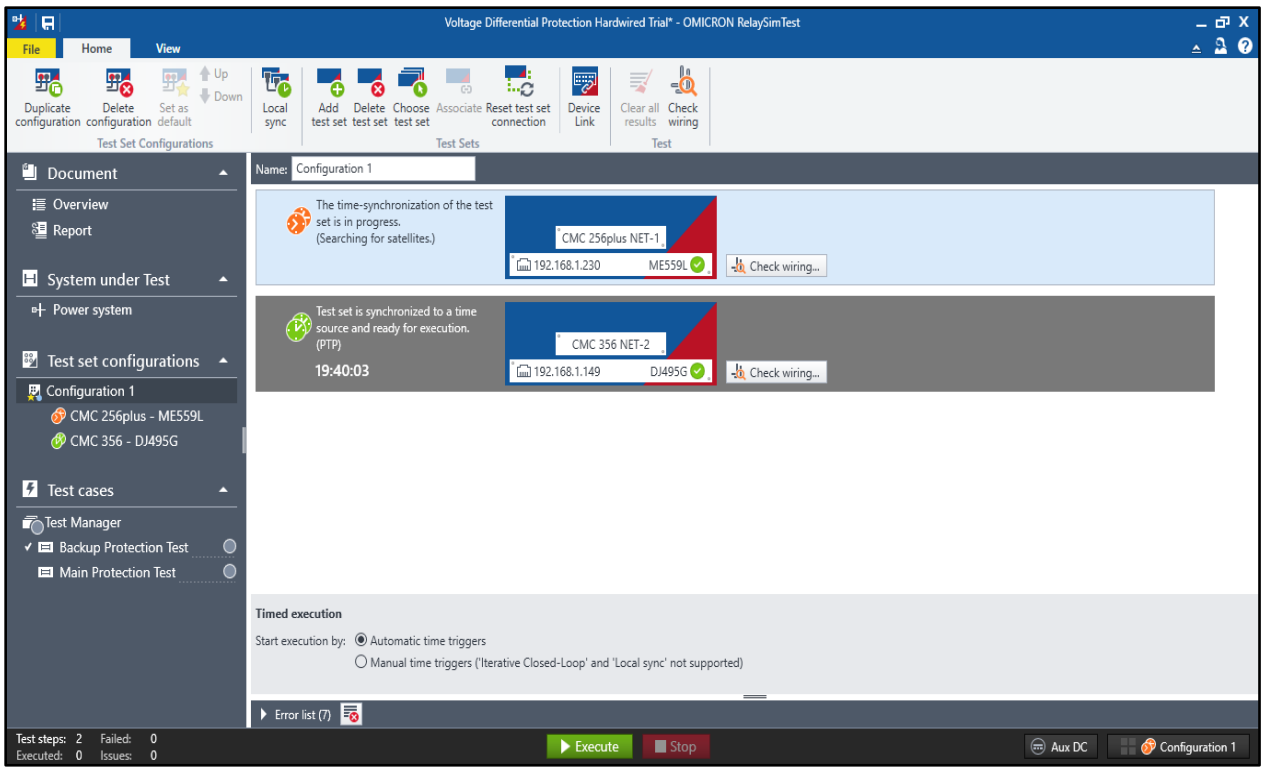

Figure 5.38. RelaySimTest time synchronization unsuccessful

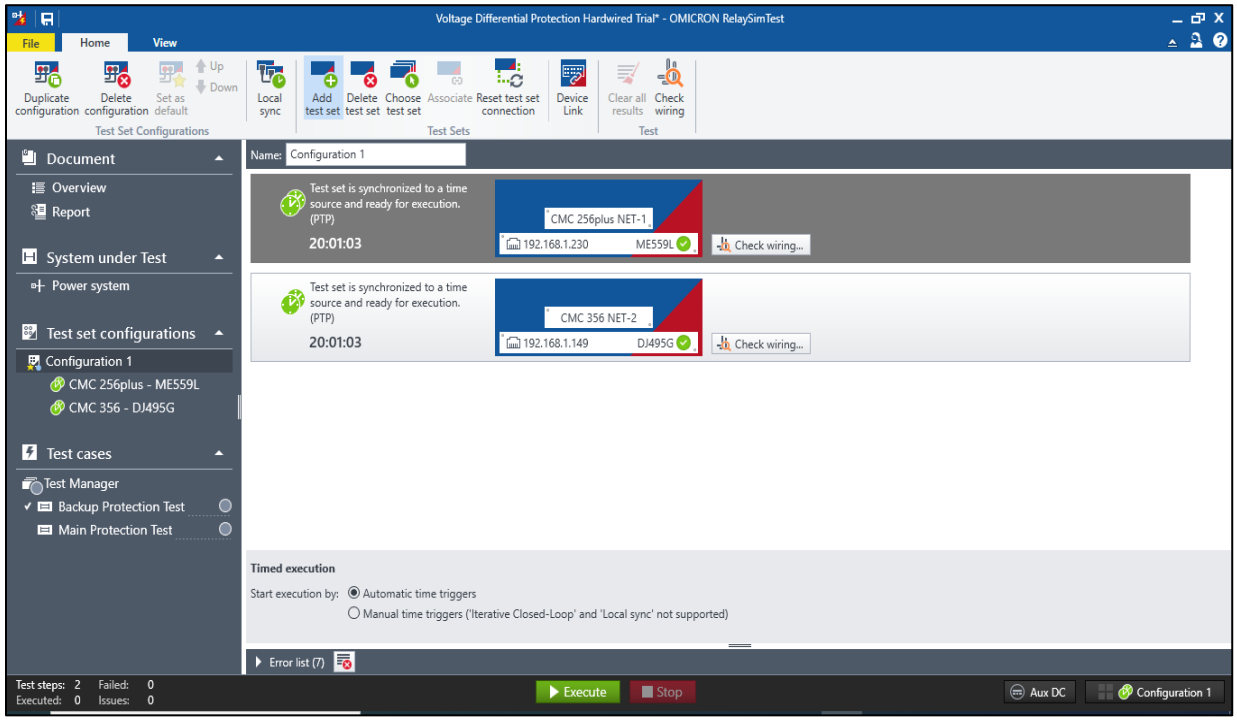

Figure 5.39. RelaySimTest time synchronization successful

These RTAC and SEL 487V devices are time synced over the network using an NTP server of SEL 2488 GPS clock. The NPT server broadcasts time sync messages via the communications network to all devices that require time. Figure 5.40 shows a Wireshark snapshot for NTP published messages in the network to IP address 224.0.1.1. Two methods were used for determining whether the device received time sync messages from the server: i) manually setting incorrect date and time on the device to see if it will be updated to correct date and time and ii) using a network analyser tool (Wire Shark) to filter for time sync messages as shown in Figure 5.40. Using both test techniques, it was demonstrated that the NTP server is operating correctly, as time sync messages are observed in the network analyser tool as well as a manually set date time that was updated to the same time as the NTP server.

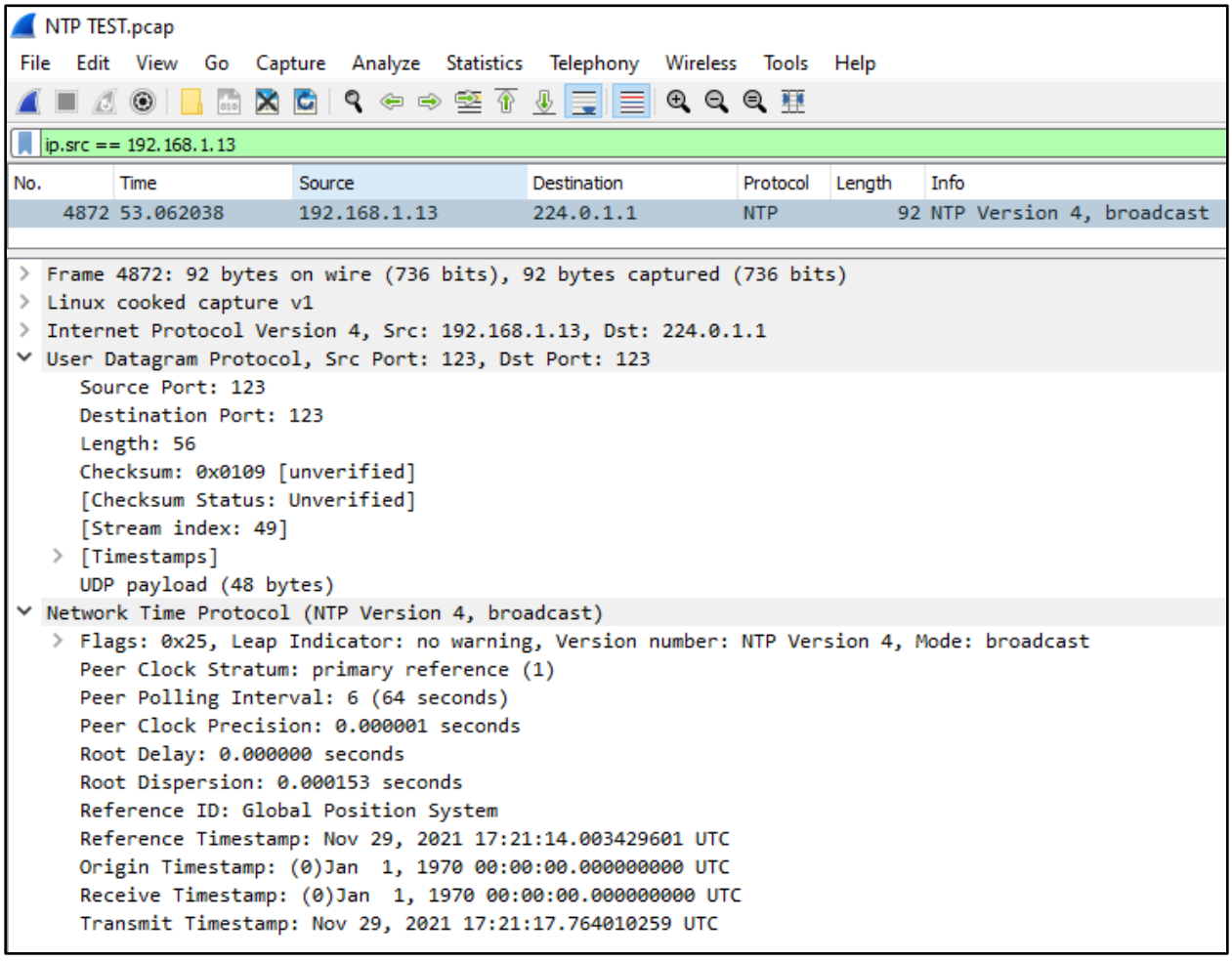

Figure 5.40. NTP broadcast messages

The following section describes how to configure OMICRON's RelaySimTest for system-based testing.

5.7 System-based testing engineering configuration

The network represented in Figure 5.2 is simulated using RelaySimTest, as seen in Figure 5.41 to Figure 5.44. The application is used for system-based testing, which enables for distributed testing, including equipment testing from remote locations. System-based testing also enables for the testing of not only steady-state settings, but also transient conditions, which are more representative of real-world site conditions. It should be noted that the majority of the drawing depicts the modelling of capacitor bank elements. The capacitor bank is centre tapped, which means that it is split into two halves, top and bottom. As indicated in the diagram (Figure 5.41), each half has two parallel threads with six units, each string with three units, and each unit with eight elements. Circuit breakers are used to simulate faults by closing them to produce a short circuit across the capacitor element and then opening the breaker to clear the fault. The configuration enables for the testing of various element failure situations while monitoring the protection performance with the applied relay settings based on power system conditions.

On RelaySimTest program, the capacitor elements and capacitor units are simulated using impedances calculated in Chapter 5 and Appendix A.3, as shown in Figure 5.45. The simulation yields a capacitor element impedance of 42.350 and a capacitor unit impedance of 338.80, as estimated in appendix A.3. At 149.65 kV, these impedance values produce a capacitor bank reactive power rating of 22 Mvar. The rest of the power system parameters, such as transformers, lines, and loads, are the same as in Chapter 3. The modelling of the entire network enables for the simulation of external fault situations outside of the capacitor bank unit, as well as the monitoring of the influence of such external faults on the capacitor bank protection. This type of protection is known as system protection, and it refers to the bank's protection from power system circumstances. Short circuit faults (ground linked or phase only linked) on other areas of the network are examples of such faults.

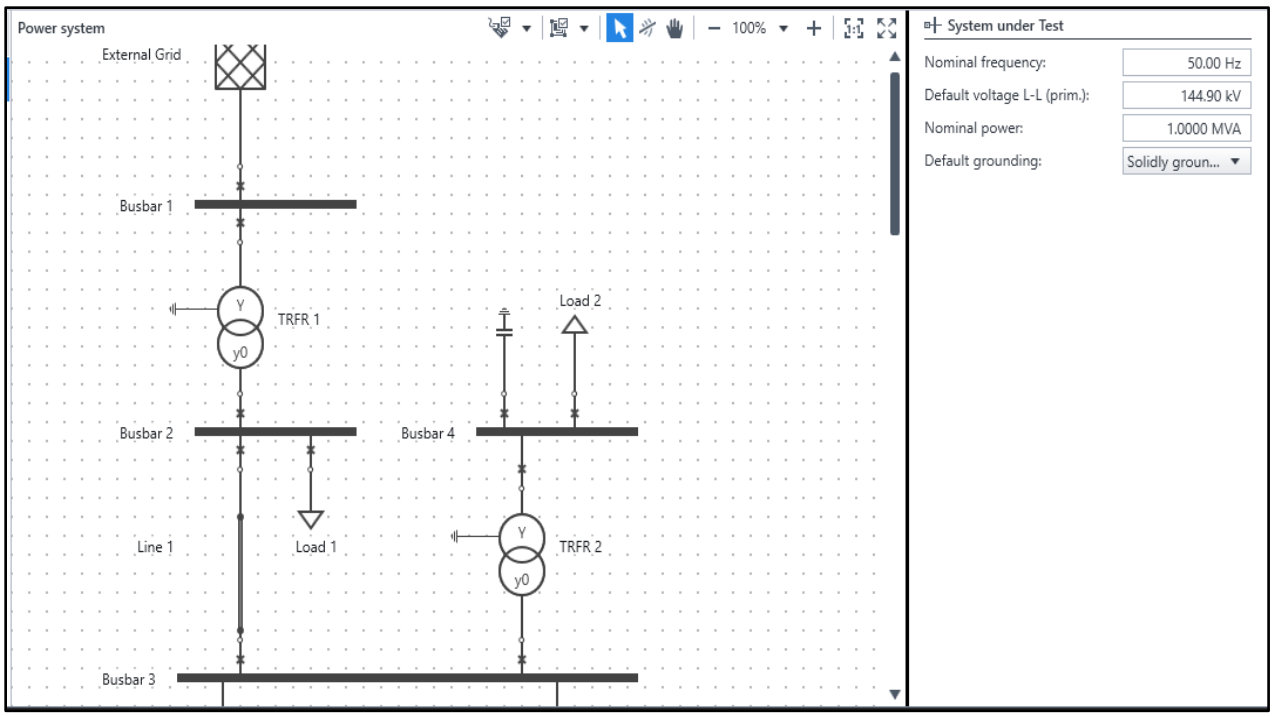

Figure 5.41. Section A of power system network under study in RelaySimTest

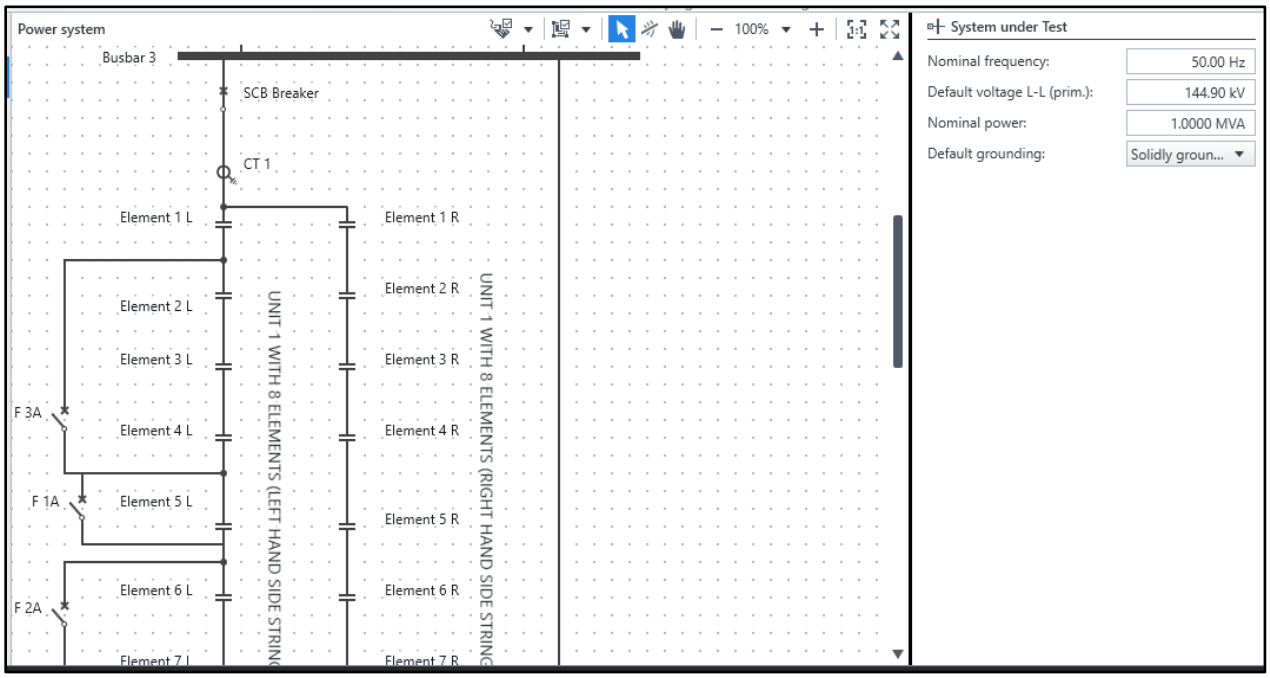

Figure 5.42. Section B of power system network under study in RelaySimTest

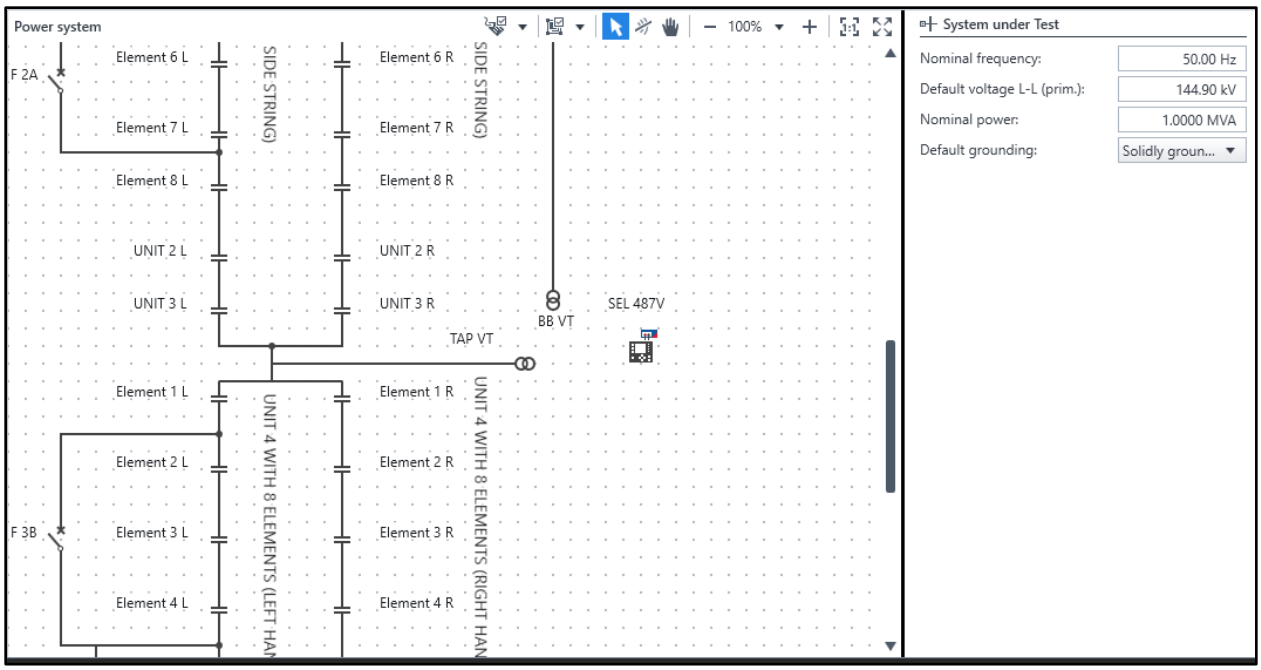

Figure 5.43. Section C of power system network under study in RelaySimTest

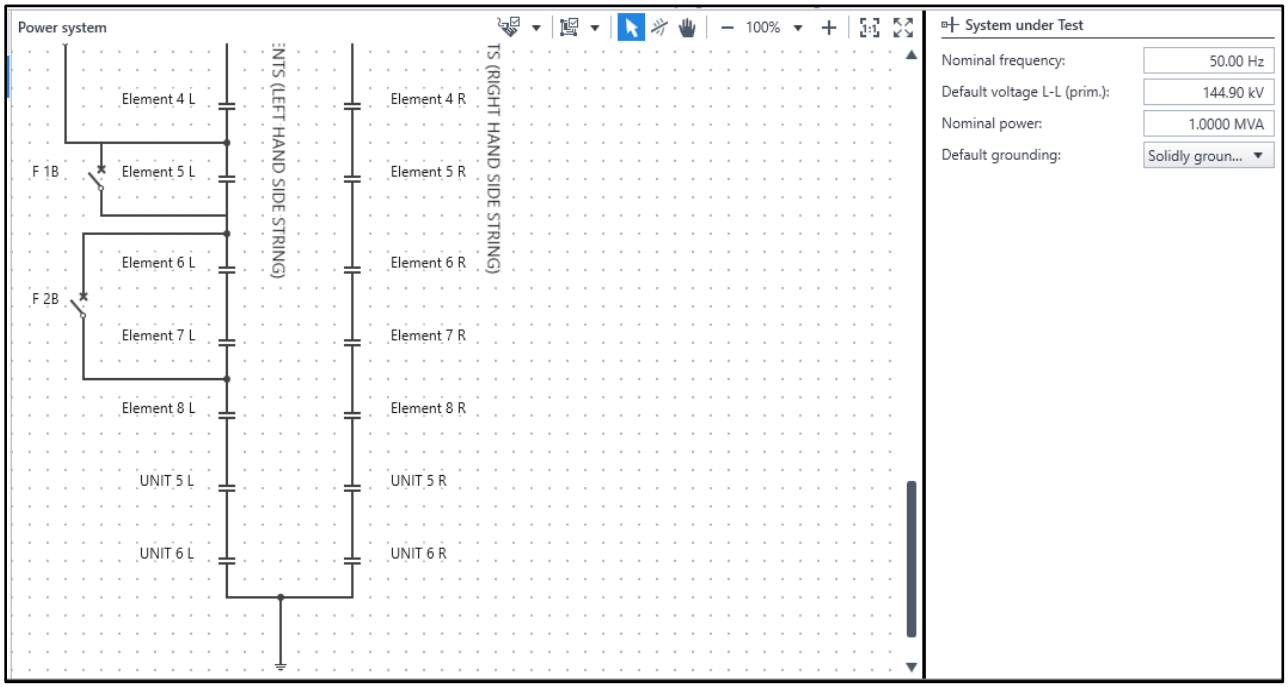

Figure 5.44. Section D of power system network under study in RelaySimTest

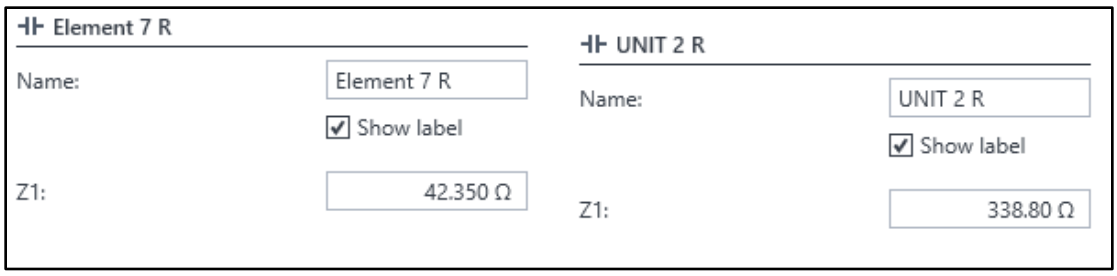

Figure 5.45. Capacitor element and its impedance configuration

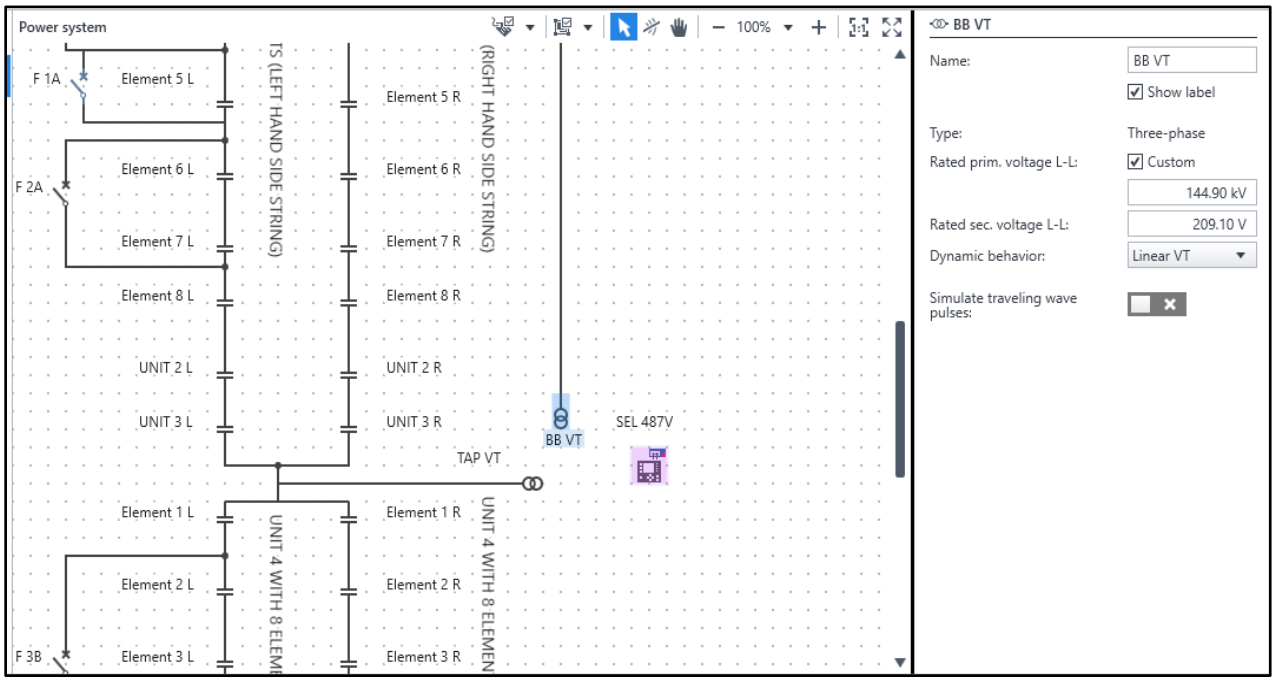

Figure 5.46. RelaySimTest bus VT configuration

There are two voltage transformers, one for measuring bus bar voltage and the other for measuring tap voltage, as illustrated in Figures 5.46 and 5.47. The voltage transformers depicted in Figures 5.47 and 5.46 have VT ratios of 300:1 (72.450 kV:241.5 V) and 693:1 (144.90 kV:209.10 V), respectively, and are connected to OMICRON CMC 256 plus for tap VT and OMICRON 356 for bus bar VT.

There are three important areas to configure on RelaySimTest, i) Power System, ii) Test set configurations, and ii) Test cases, as shown in the leftmost Figures 5.50 (dark in colour). Figure 5.41 to Figure 5.44 show the power system portion, whereas Figure 5.48 and Figure 5.49 illustrate the test set setup (CMC configurations).

Figure 5.50 and Figure 5.51 depict the test cases as they are setup for this implementation of the primary protection and backup protection test cases, respectively. Different capacitor bank failure situations outlined in chapter 4 are used in the test cases.

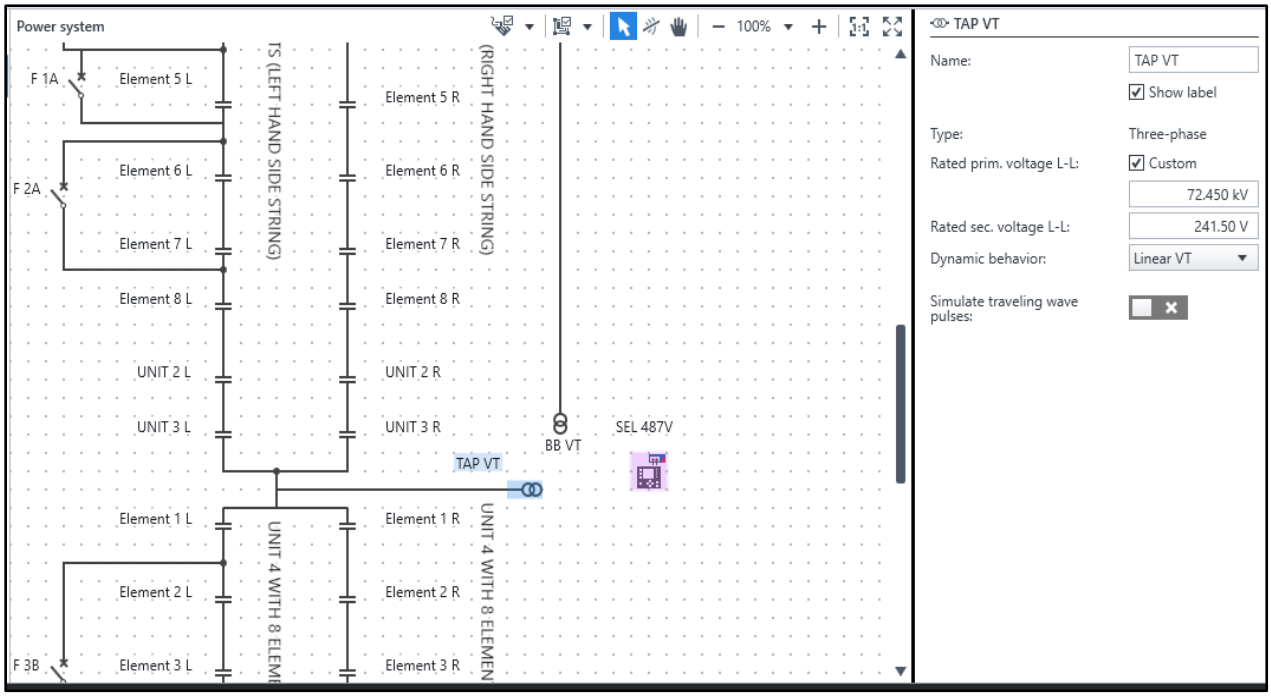

Figure 5.47. RelaySimTest tap VT configuration

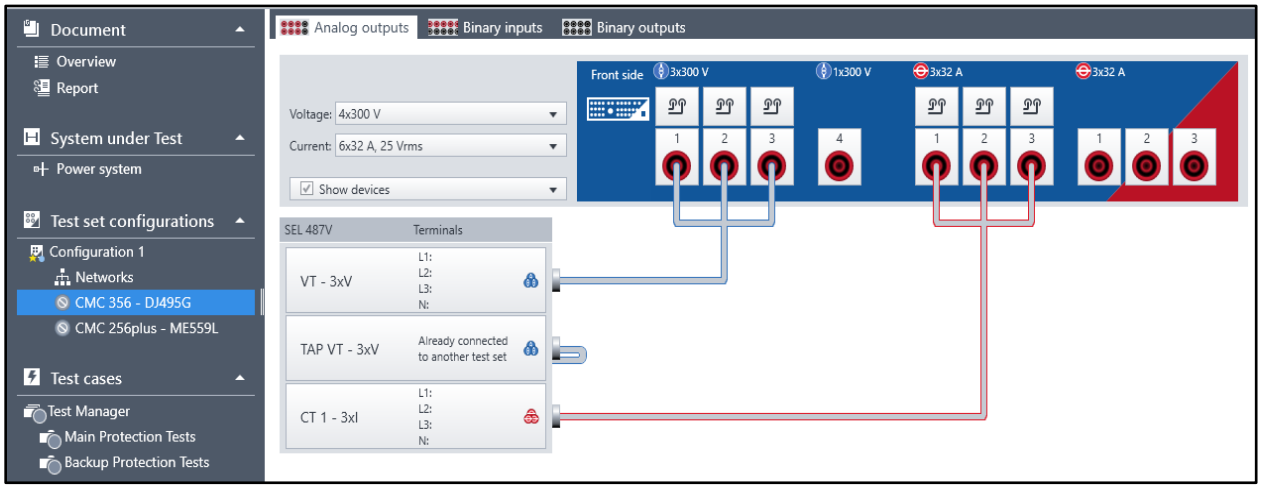

Figure 5.48. RelaySimTest CMC 356 configuration

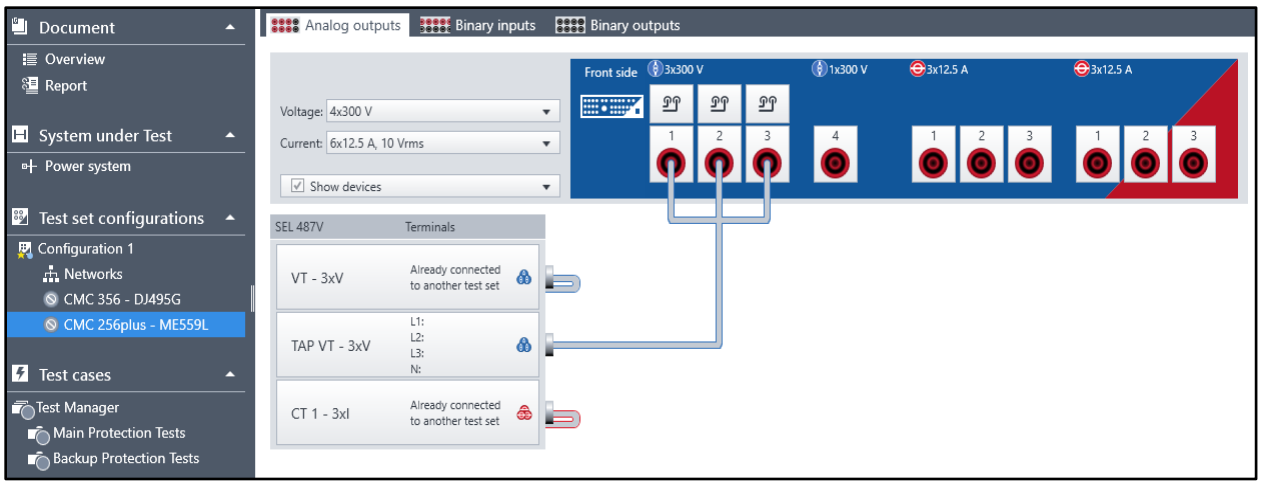

Figure 5.49. RelaySimTest CMC 256 plus configuration

Figure 5.48 illustrates the configuration of the OMICRON CMC 356 unit with the bus bar voltage (BB VT) and the capacitor bank current transformer (CT 1) attached to it, whereas Figure 5.49 shows the OMICRON CMC 256 plus with tap VT connections to it. Figure 5.50 and Figure 5.51 display the project's test cases and these are divided into two categories: primary and backup. Circuit breakers are used to short the capacitor elements as part of the main protection test scenario to simulate capacitor element failures. Above and below tap, alarm, trip, and high set are some of the test cases that can be used to verify the normal operation of the device (above and below tap). According to the theoretical calculations made for each test scenario, a description of how it is simulated and how it is predicted to perform is protection requirements. Secondly, we'll be looking at the backup protection. Protection parameters computed in the previous chapters have been tested in overcurrent and over/under voltage test situations. Using the voltage differential function as discussed in the previous chapters an overload condition is simulated. Overload without tripping occurs in the first test scenario because the overload current is smaller than the pickup current. Because of the increased number of element failures, more currents than the pickup value are simulated, which should trigger the breaker.

Figure 5.50. RelaySimTest main test cases configuration

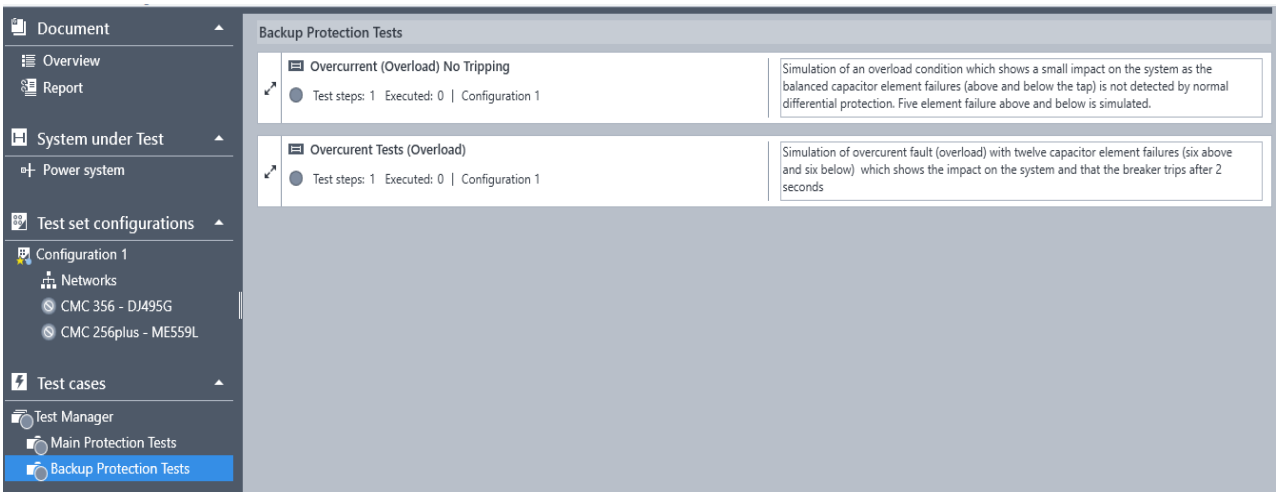

Figure 5.51. RelaySimTest backup test cases configuration

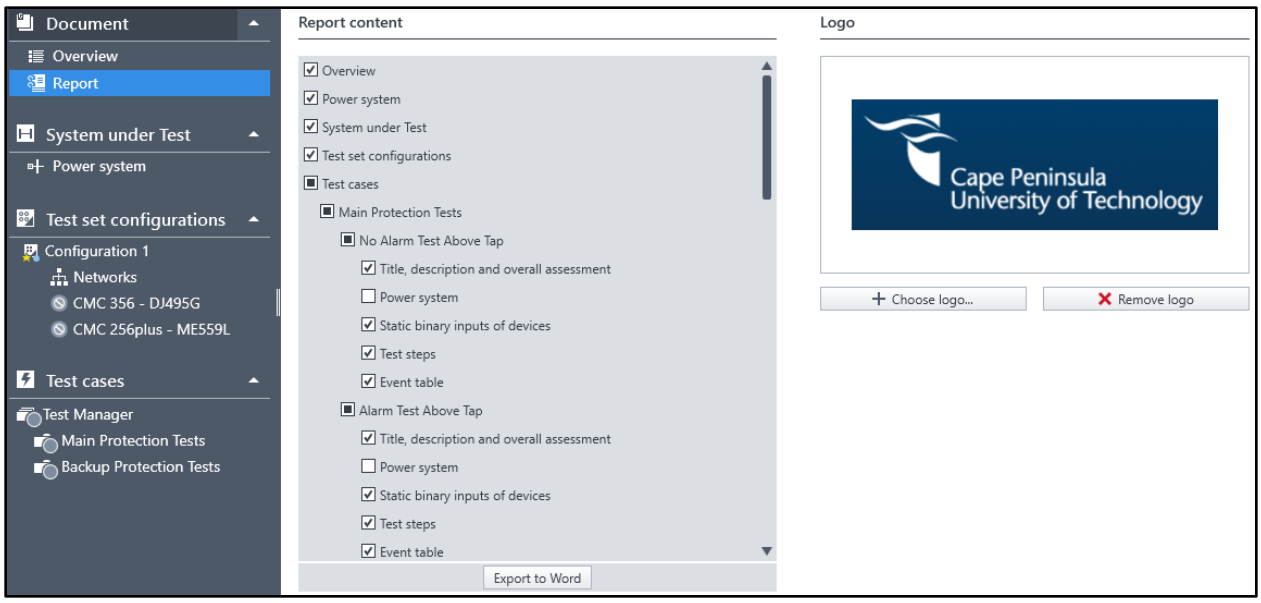

Figure 5.52. RelaySimTest report configuration

The fourth component of RelaySimTest, depicted in Figure 5.52, is where reports are set up. To configure the report and what it needs to show/include, this option allows the report to be exported to Microsoft Word, and a logo may also be added as shown on the right-hand side of the Figure 5.52. Annexure C of the research project contains the exported report. In the following section, we'll cover through how to set up an HMI with the SEL AcSELerator Diagram Builder program.

5.8 Human Machine Interface (HMI) engineering configuration

This section explains how the project's Human-Machine Interface (HMI) was set up. The SEL AcSELerator Diagram builder was chosen for HMI purposes because of its ease of use and the ability to view capacitor bank alarms. There are a number of ways to import tags into the diagram builder program for configuring the HMI. Tags can be imported in two methods, one directly from the RTAC device online and the other from the RTAC database offline, as seen in the screenshot. Loopback IP address and Database login details (Username and password) are entered in the second choice as shown in Figure 5.53, while the device's IP address and login details should be entered for the first option.

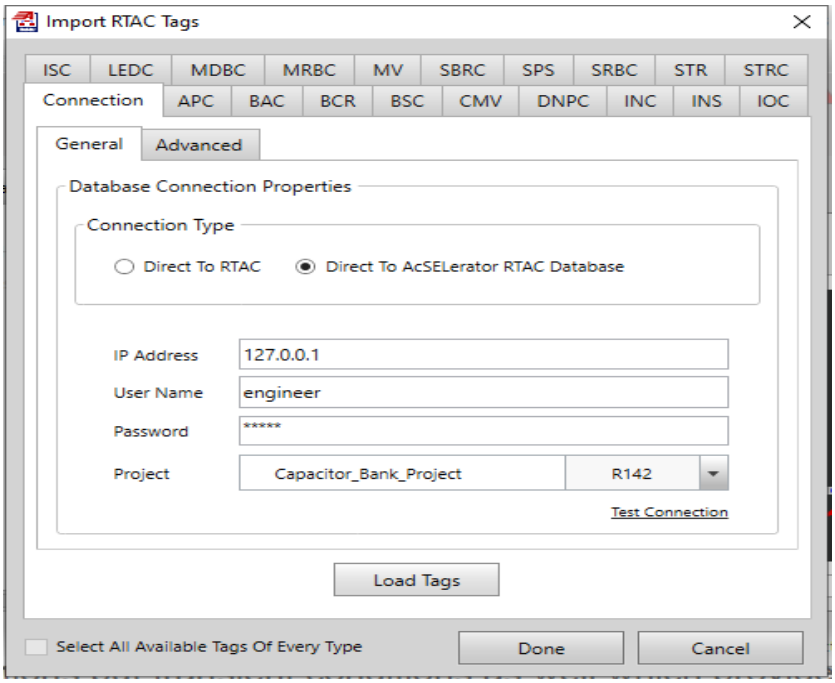

Figure 5.53. RTAC tag import in SEL AcSELerator Diagram Builder

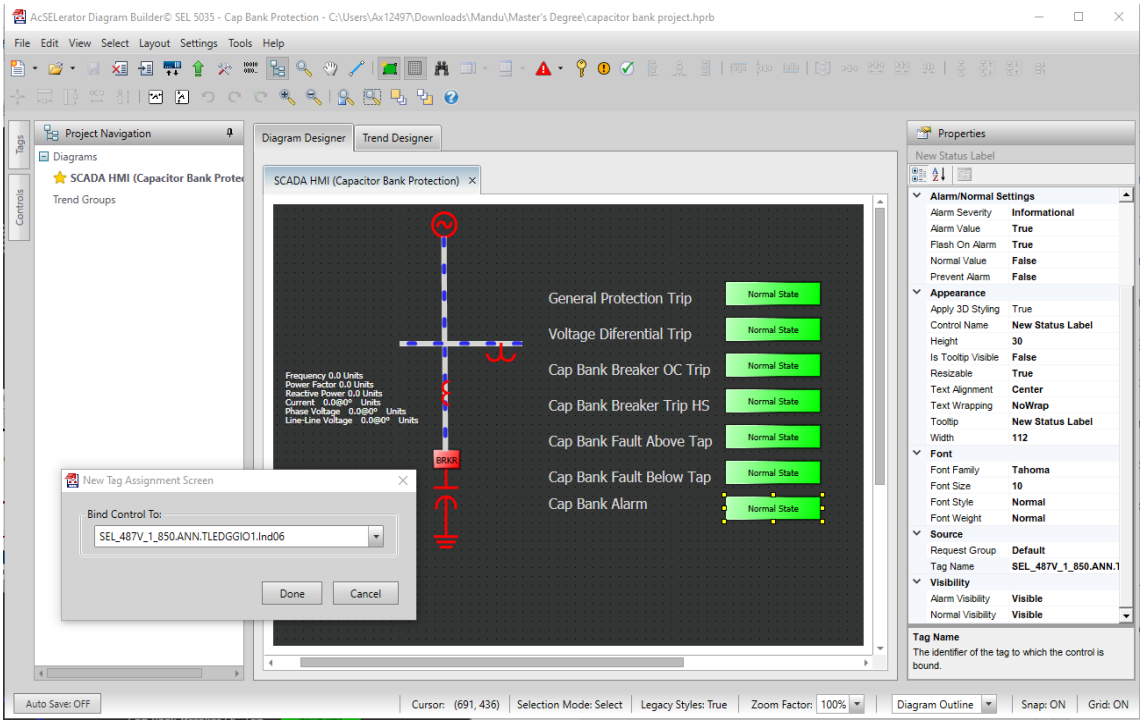

Figure 5.54. HMI linking in SEL AcSELerator Diagram Builder

Figure 5.54 displays the HMI's tag linking on Diagram Builder, which is then imported into SEL RTAC for online viewing. To attach a tag to a signal, click on the tag name cell on the right-hand side of the screen under the properties tab, which then opens a little window on the screen. It shows a few tags connected on the screen in normal (binary 0) and abnormal (binary 1) states represented by the colours green and red. However, not all of these tags are displayed on the screen, as some only appear as alarms or events in an alarm list or event list, respectively.

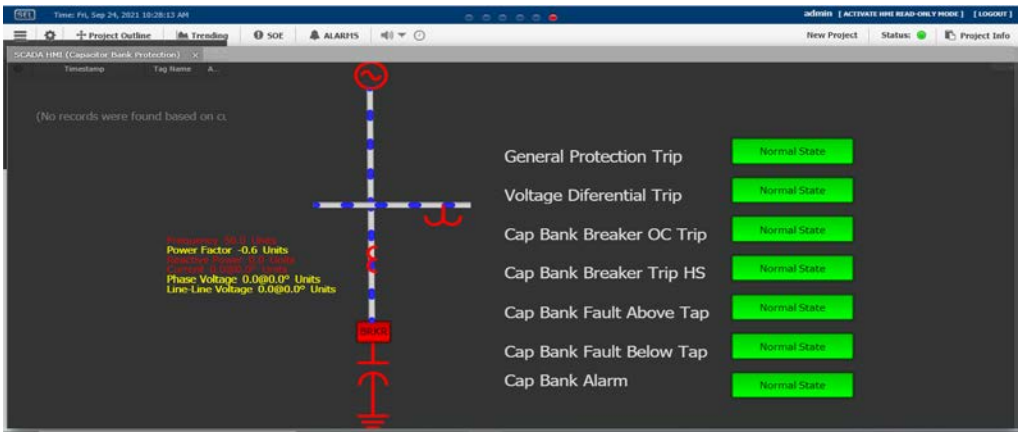

Figure 5.55. HMI Runtime in normal state

There are no alarms displayed on the RTAC HMI screen in Figure 5.55 because the system is running normally, except for measurements that are in alarm mode due to CMC injections being performed. Chapter 6 discusses test findings for an engineering configuration that was previously described here.

5.9 Conclusion

In this chapter, the engineering configuration of SEL AcSELerator QuickSet, SEL AcSELerator Architect, gateway engineering configuration, GPS engineering of SEL 2488 using the web service interface, system-based testing engineering configuration via OMICRON RelaySimTest software, and HMI engineering configuration using SEL AcSELerator Diagram Builder are discussed in detail.

6. CHAPTER SIX: SHUNT CAPACITOR BANK PROTECTION TESTING

6.1 Introduction

The chapter analyses the lab scale implementation test results reported in Chapter 5. The benefits of employing system-based testing methods over traditional testing methods include, but are not limited to, the ability to test not only steady-state situations, but also transient-state conditions, and the ability to conduct distributed testing in remote places.

Figure 6.1 depicts the chapter layout, which includes an introduction in section 6.1, test results discussion on failure of two capacitor elements above tap in section 6.2, failure of three elements above tap in section 6.3, failure of four elements below tap in section 6.4, failure of five elements above tap in section 6.5, and failure of six elements above and below tap in section 6.6, simulation results discussion in section 6.7 and conclusion in 6.8. More test cases results are provided in Appendix A.4 RelaySimTest report.

The previous chapter's engineering setup for shunt capacitor protection is being tested, and the results are analysed. The full capability of the lab scale implementation is to validate the simulation tests and to confirm if the engineering configuration is acceptable and its protection function operated correctly and produced the predicted simulation results based on theoretical calculations and simulations. Tables 6.1 and 6.2 show the scenarios being examined as well as the expected outcomes. Simulation results are monitored in this chapter in all different configuration parts of the lab scale test bench, including HMI and IEC 61850 configuration.

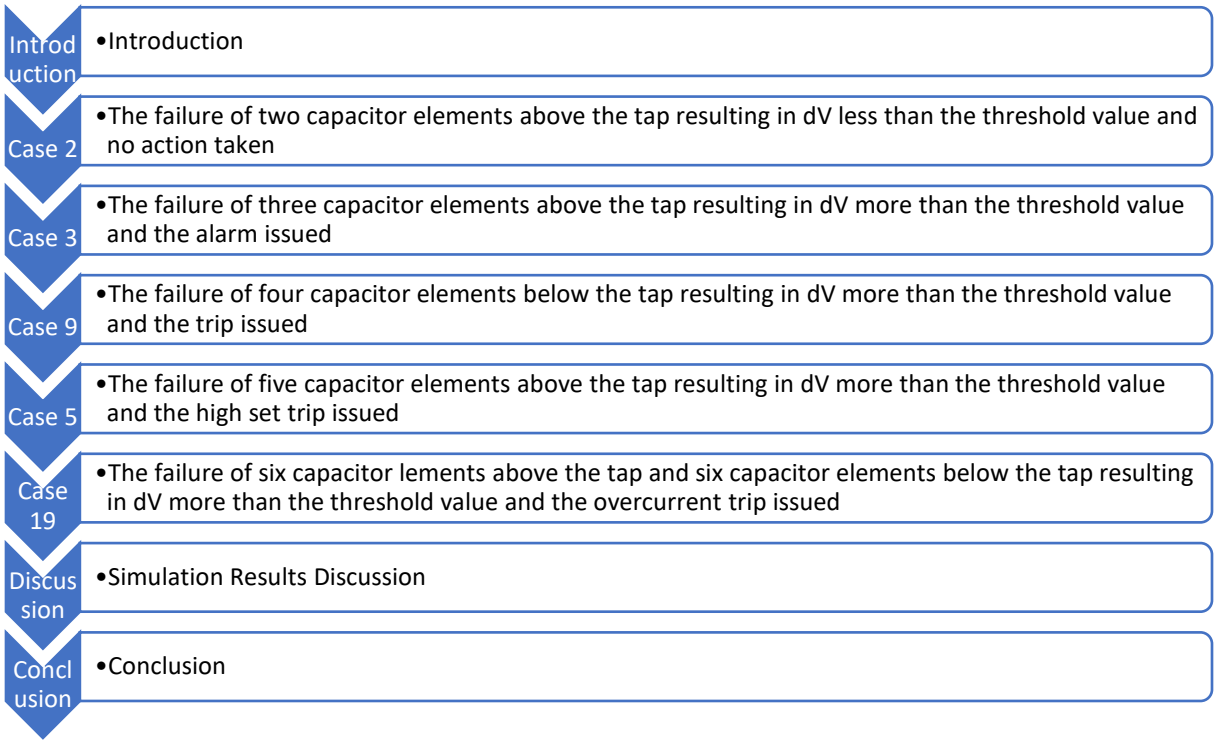

Figure 6.1. Overview of chapter 6 in flow diagram form

The time stamp for alarm, Trip and high set trip adopted in Table 6.1 with reference to Horton, 2002 as follows: the alarm, trip, and high set protection settings are established in accordance with Horton, 2002, with the alarm set at 105 percent voltage level after 2 seconds, the trip level at 110 percent after 500 milliseconds, and the high set above 110 percent after 120 milliseconds.

Table 6.1 depicts the principal protection test method configuration created in RelaySimTest as stated in Chapter 5, section 5.3, as well as the expected results. The failure of one capacitor element was not included in the analysis because it produces the same outcomes as the failure of two capacitor components, and the results are described in detail in the following sections.

Table 6.2 shows a backup test technique for failures that occur outside of the capacitor bank installation as well as those that are not detected by the main protection system.

Table 6.1. Main protection test procedure

Test Procedure for Shunt Capacitor Bank Element Failures Above the Tap				
Case	**Element Failure**	**Action**	**Mode of operation**	**Procedure using Figure 6.1.2**
1	1	No action	Normal	Close F1 A Breaker
2	2	No action	Normal	Close F2 A Breaker
3	3	Alarm after 2s	Alarm	Close F3 A Breaker
4	4	Trip after 0.5s	Trip	Close F3 A and F1 A
5	5	Trip after 0.12s	High Set	Close F3 A and F2 A Breakers
Test Procedure for Shunt Capacitor Bank Element Failures Below the Tap				
6	1	No action	Normal	Close F1 B Breaker
7	2	No action	Normal	Close F2 B Breaker
8	3	Alarm after 2s	Alarm	Close F3 B Breaker
9	4	Trip after 0.5s	Trip	Close F3 B and F1 B Breakers
10	5	Trip after 0.12s	High Set	Close F3 B and F2 B Breakers

The operating times defined in Table 6.2 for backup protection functions overcurrent, overvoltage, under voltage, are extracted from IEC 60255 and IEEE C37.112 Standards although these times have been amended for test purposes. From the test cases presented on Table 6.1 and Table 6.2 only the following test cases are included in the test results analysis: case 2, case 3, case 9, case 5, and case 19, for all different parts of the system to demonstrate the effectiveness of the implemented protection scheme. Figure 6.2 depicts a RelaySimTest power system simulation that can be used as a reference for test case procedures.

Table 6.2. Backup protection test procedure

Test Procedure for Shunt Capacitor Bank Element Failures Above the Tap				
Case	**Element Failure**	**Action**	**Mode of operation**	**Procedure using Figure 6.1.2**
11	Three phase fault	UV Trip after 5s	Trip	Three phase fault on Bus 4
12	Three phase fault	UV Trip after 5s	Trip	Three phase fault on Bus 3
13	Three phase fault	UV Trip after 5s	Trip	Three phase fault on Bus 2
14	Three phase fault	UV Trip after 5s	Trip	Three phase fault on Bus 1
15	Single phase fault to ground	UV Trip after 5s	Trip	Single phase to ground fault on Bus 4
16	Single phase fault to ground	OC Trip after 0.06s UV Trip after 5s	Trip	Single phase to ground fault on Bus 3
17	Single phase fault to ground	OC Trip after 0.06s OV Trip after 3s UV Trip after 5s	Trip	Single phase to ground fault on Bus 2
18	Single phase fault to ground	UV Trip after 5s	Trip	Single phase to ground fault on Bus 1
19	Fault within bank (6 above and 6 below tap)	OC Trip after 0.120s	Trip	Internal fault within the capacitor bank (Close F3 A, F2 A, F1 A, F3 B, F2 B and F1 B)

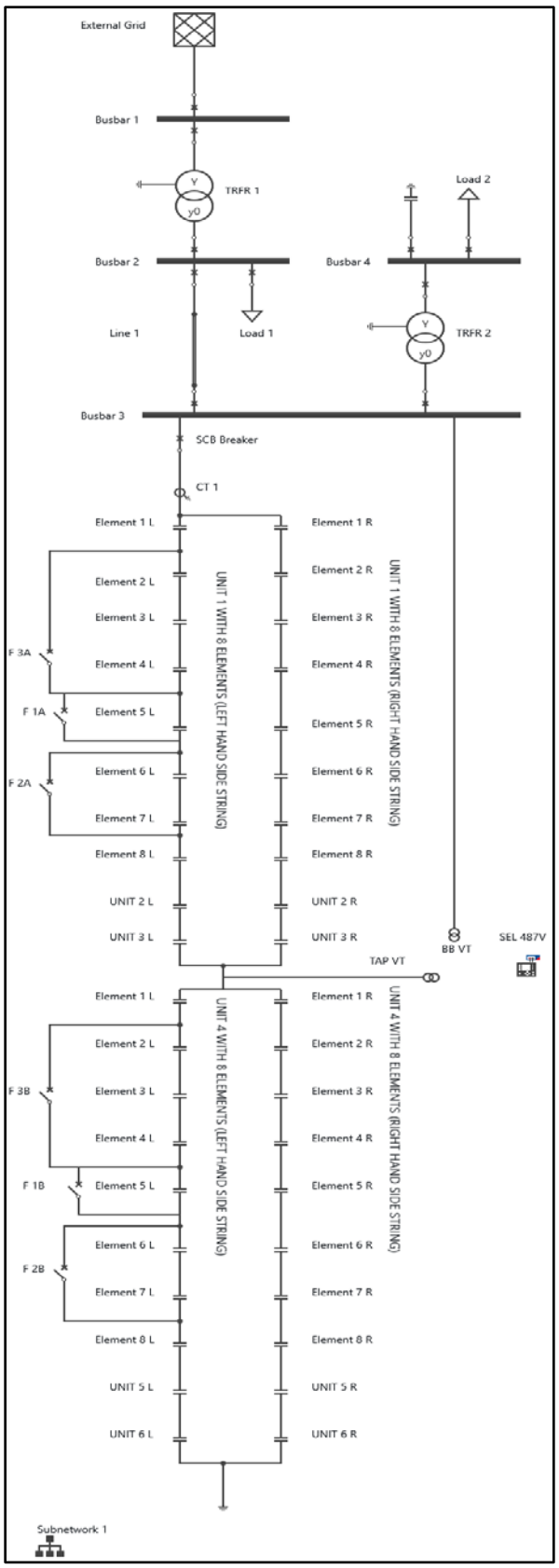

Figure 6.2. RelaySimTest power system simulation

Figure 6.3. RelaySimTest successful execution of test cases

6.2 Case 2: Two element failures above tap

Case 2 presents a simulation of two capacitor element failures caused by shorting them, and the protection relay takes no action since dV is less than the threshold value, and the capacitor bank continues to operate normally. The case is simulated in RelaySimTest software, and the system simulation begins at typical steady-state conditions before shorting two elements above the tap 500ms later.

Figure 6.4 depicts the Human Machine Interface representation of the capacitor bank during normal operation, with two capacitor element failures simulated. There are no alerts displayed on the HMI, and the injected reactive power is 20.6 MVar, with a current of 82.3 A. The phase voltage is 83.6 kV, while the line-to-line voltage is 144.8 kV. Data (binary and measurements) are gathered via buffered and unbuffered control reports as stated in the IEC 61850 standard, as well as MMS, as discussed in Chapter 5, section 5.4.

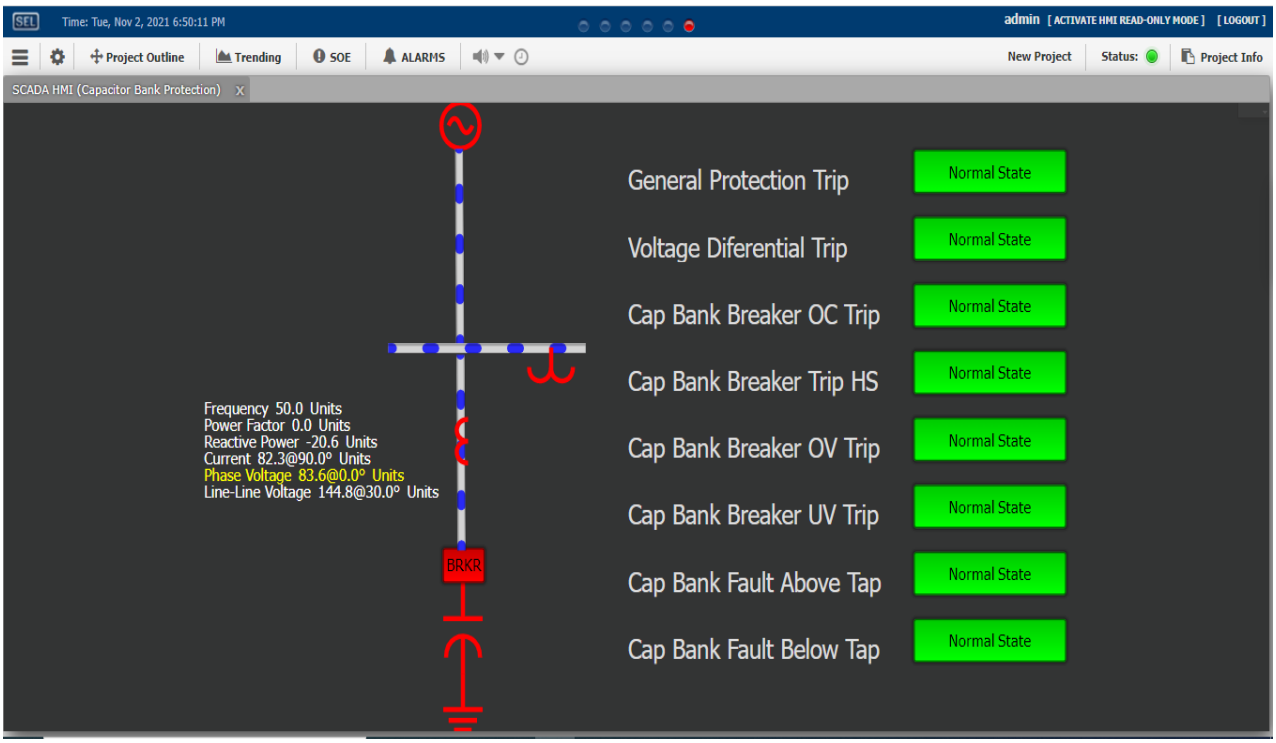

Figure 6.4. SCADA system for capacitor bank configuration during normal operation

The alarms (binary data) are mapped to relay target LEDs for latching purposes and to ensure that the HMI displays exactly what is shown on the relay physically. Figure 6.4 depicts the simulation results of RelaySimTest with two capacitor element failures. The simulation begins with the incomer breaker closed, and two capacitor elements fail 500ms later. With two element failures, the total impedance reduced, resulting in voltage drops as seen in the screenshot, while current increased but no warning was triggered. According to RelaySimTest, the BB secondary voltage is 120.81 V and the Tap secondary voltage is 136.43 V, resulting in a computed differential voltage of 2.66 V, which is less than the set pickup voltage of 3.9 V. Because the delay selected is 2 seconds, the simulation ran for 3 seconds to guarantee that no alarm is triggered. The screenshot shows SEL 487V binary outputs for hardwired relay outputs for breaker trip and close signals, as well as SEL 487V GOOSE outputs for IEC61850 standard implementation.

As seen in the screenshot, the following logical nodes have been configured for RelaySimTest to subscribe to: i) AA87PDIF1 (alarm above tap), ii) BA87PDIF1 (alarm below tap), ii) T87PDIF1 (trip), iv) H87PDIF1, v) WP1PIOC1 (overcurrent), vi) U1P1PTUV1 (under voltage), vii) O1P1PTOV1 (general trip). Despite the two capacitor element failures, none of these GOOSE logical nodes are asserted, indicating that the capacitor bank is operating normally.

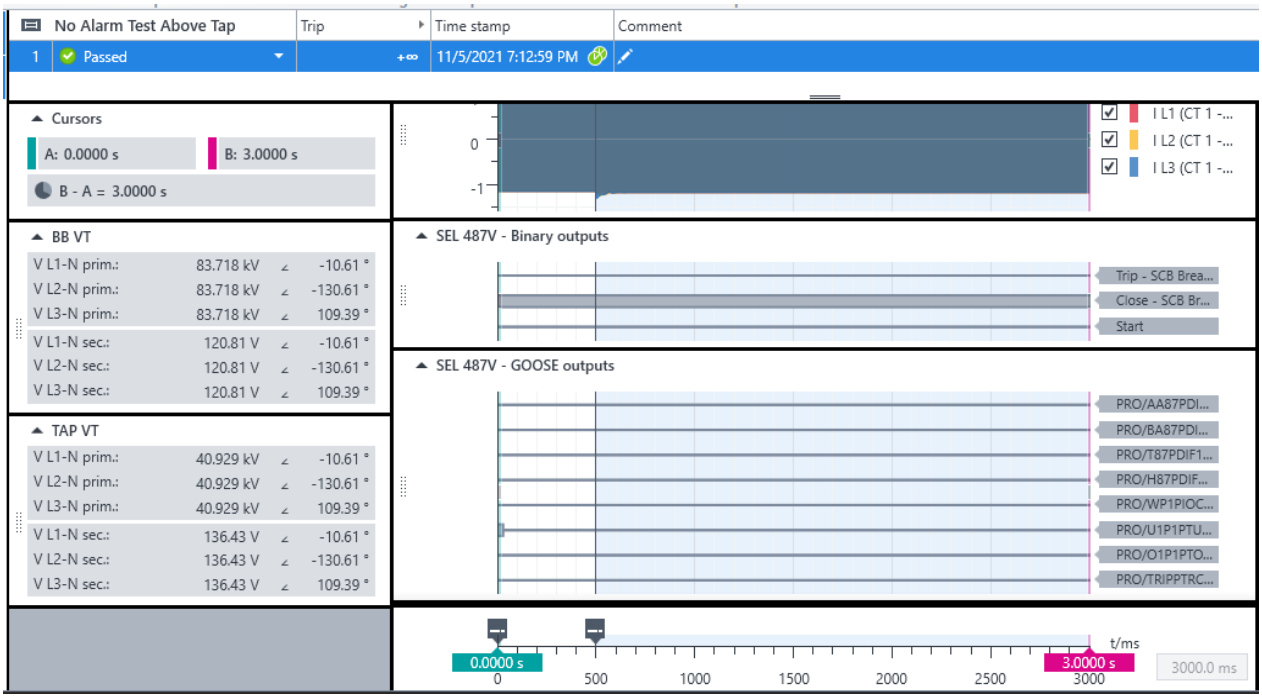

Figure 6.5. RelaySimTest simulation results for two element failures above tap

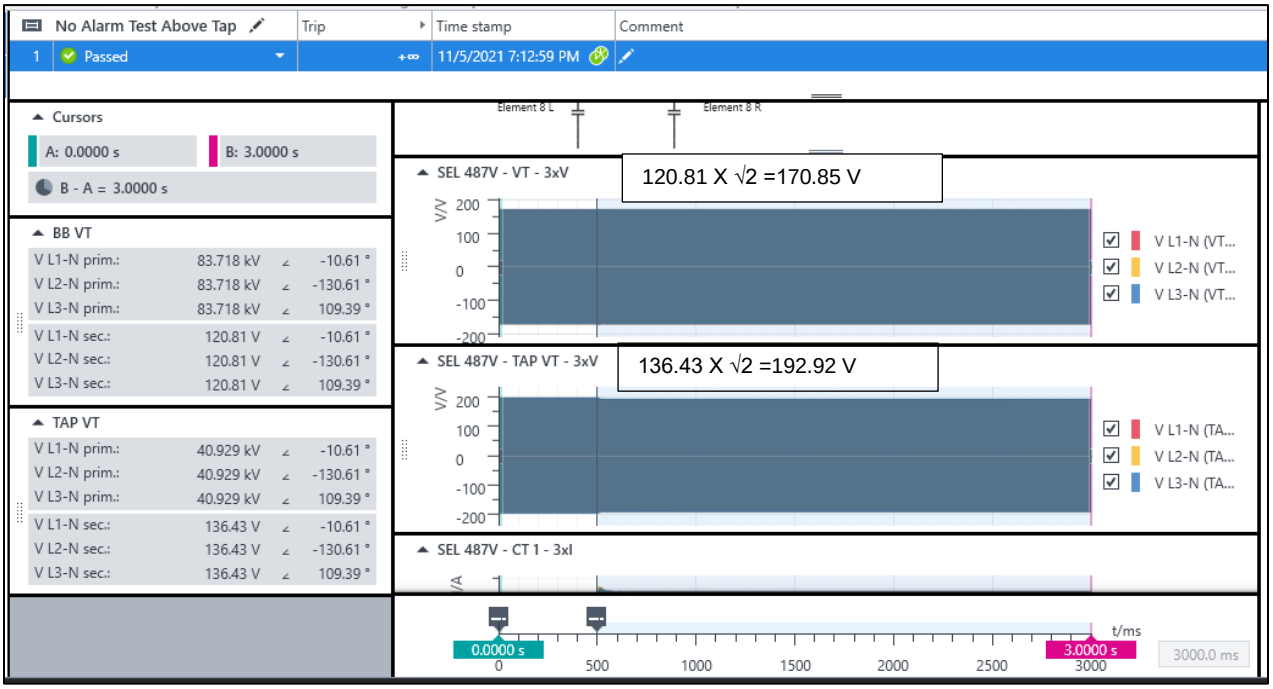

Figure 6.6. RelaySimTest simulation voltage waveforms for two element failures above tap

RelaySimTest voltage waveforms for both BB and Tap voltages are shown in Figure 6.6 After 500 milliseconds from simulation start, there is a small decrease in voltage on the tap voltage, which is consistent with the value of 135.43 V as visible on the digital display, which decreased from 139.43 V for normal operation with no element failures. Figure 6.7 is a screenshot of the AcSELerator QuickSet HMI with a real-time connection to the relay. The target LED mapping is presented, and there is no alert or trip on the relay because the capacitor bank is in normal operation. This corresponds to the screenshots of the SCADA HMI and RelaySimTest mentioned. The TRIP LED depicted in the picture below the ENABLED LED represents the TRIPPTRC logical node, which is mapped to Ind02 for SCADA HMI. The remaining LEDs are depicted and detailed in Table 5.2.

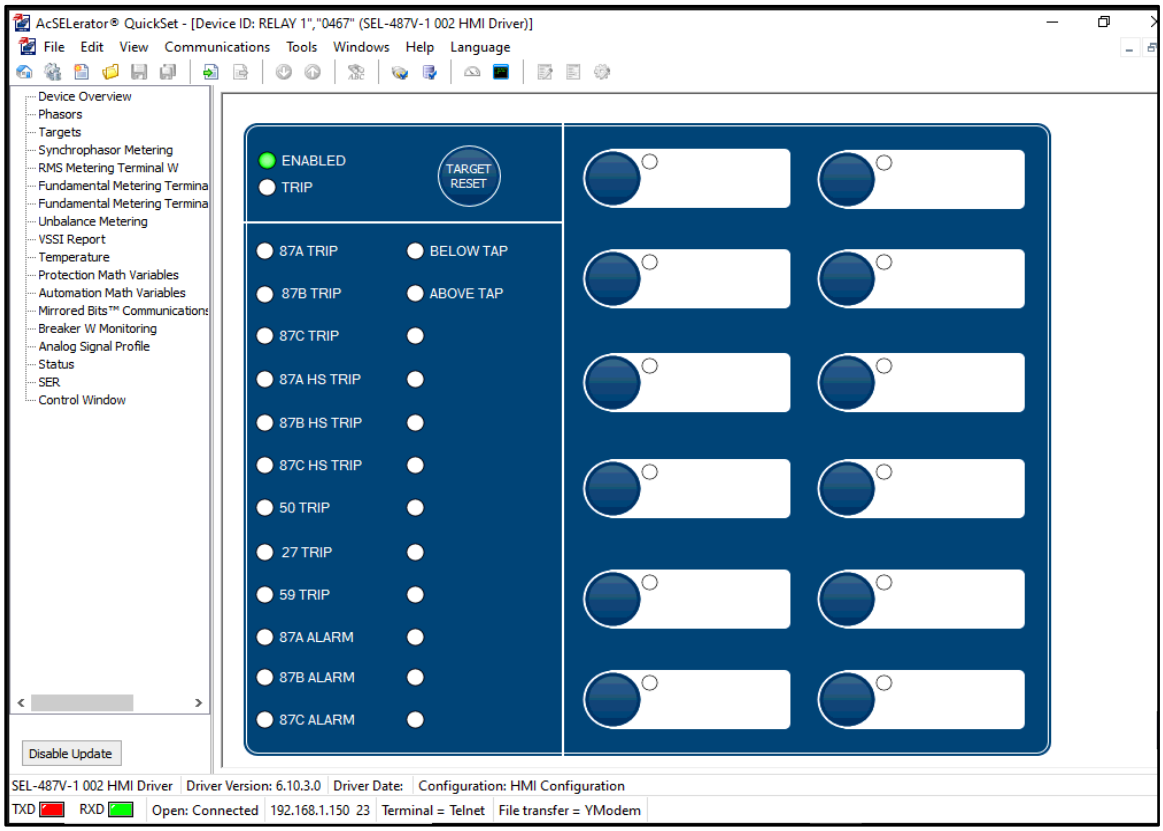

Figure 6.7. Online HMI for two element capacitor failures above tap

The overview of test results using primary and secondary voltage measurements is shown in Table 6.3. As stated in the table, the differential voltage is 2.66 V, which is less than the relay's configured pickup voltage of 3.9 V. The following section covers on three element failures for test case 3.

Table 6.3. Two element failures above tap simulation results summary

TWO CAPACITOR ELEMENT FAILURES ABOVE TAP: (CASE TWO)				
	RelaySimTest Results		SynchroWAVe Event Test Results	
	Bus Bar Voltage	Tap Voltage	Bus Bar Voltage	Tap Voltage
Primary (L-N)	83.718 kV	40.929 kV	N/A	N/A
Secondary (L-N)	120.81 V	136.43 V	N/A	N/A
Differential Voltage	2.66 V		N/A	

The protective elements are not triggered in normal mode of operation, therefore SyncroWAVe event and associated data are not applicable in this scenario as indicated in Table 6.3. Case 3 test results are discussed in the following section.

6.3 Case 3: Three element failures above tap

RelaySimTest program simulates three capacitor element failures, and Figure 6.8 shows a screenshot of the RelaySimTest case 3 test results. Voltage measurements, both main and secondary, from both VTs are presented on the left side of the screen. Secondary voltages of 120.86 V (bus bar) and 134.78 V (tap) are presented depending on which time of the simulation is selected, in this case the fault time. The system's normal condition, with no capacitor element failures, measures 120.72 V on the bus bar, whereas the tap voltage is 139.43 V. The differential voltage measured by the relay is 4.14 V, which is greater than the relay's pickup value of 3.9 V. The bottom centre of the screen, behind the CT readings graph, indicates that there was no trip and that the breaker stayed closed. The simulation begins with a capacitor breaker closed (normal conditions), then 500 milliseconds later, three capacitor elements fail, causing the simulation to halt after three seconds. According to the protection settings, logical node AA87PDIF1, which represents the alarm above the tap, is asserted 2500 milliseconds, or 2.5 seconds, after the fault began. The alarm issued assists site employees in planning repairs and determining the location of the faulty capacitor elements.

RelaySimTest voltage waveforms for both BB and Tap voltages are shown in Figure 6.9. After 500 milliseconds from simulation start, there is a small decrease in voltage on the tap voltage, which is consistent with the value of 134.78 V as visible on the digital display, which decreased from 139.43 V for normal operation with no element failures.

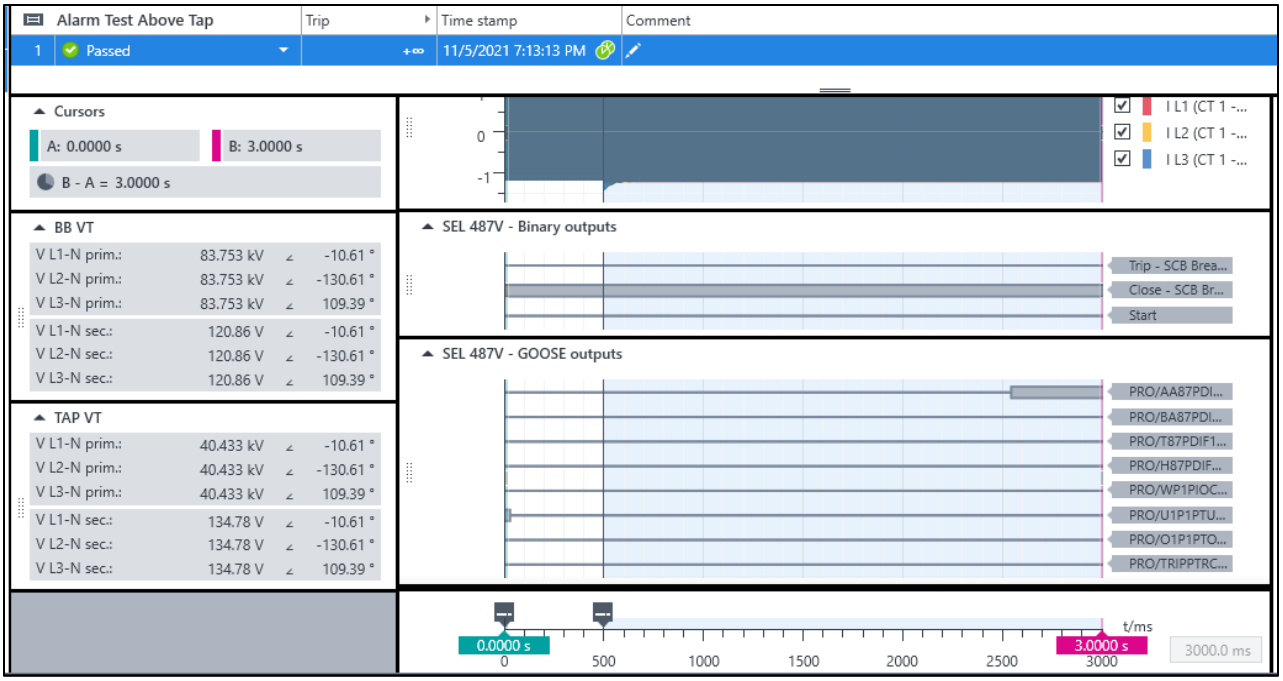

Figure 6.8. RelaySimTest alarm mode simulation results for elements failure above the tap

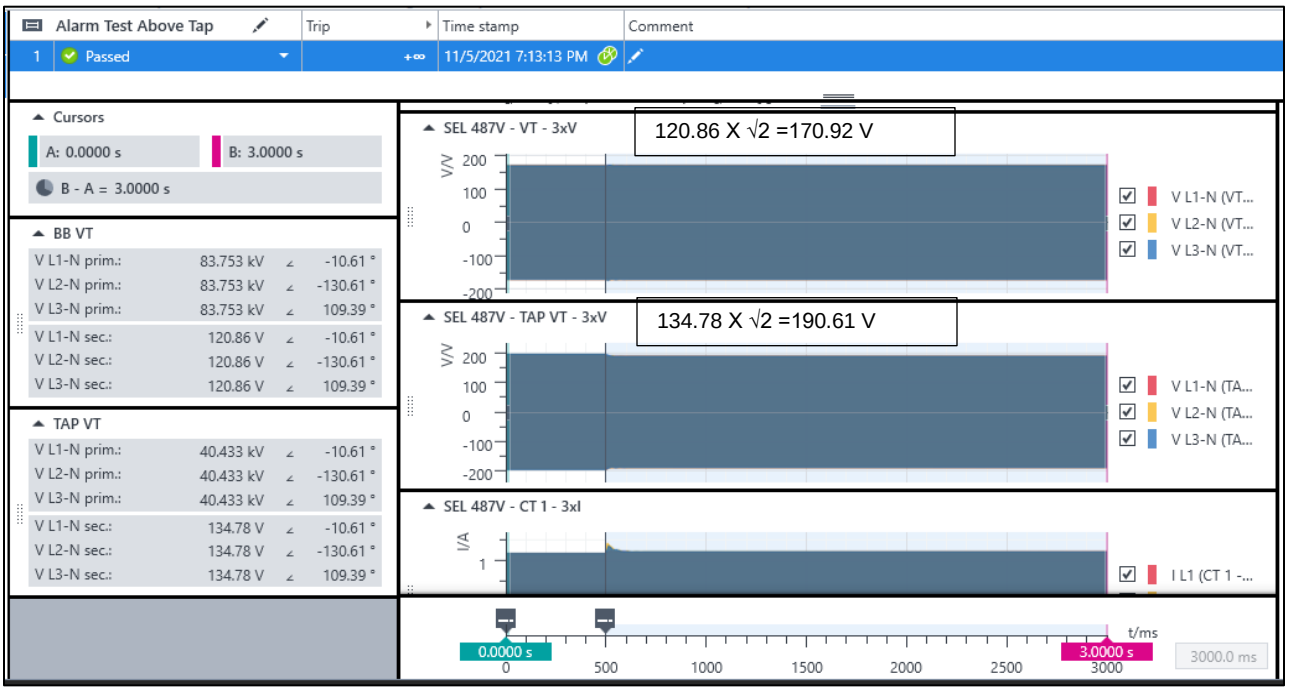

Figure 6.9. RelaySimTest simulation voltage waveforms for three element failures above tap

Figure 6.10 depicts a SCADA HMI snapshot with an alarm above the tap visible on the SCADA screen following the loss of three capacitor elements. This is the same representation that was explained and shown in Figure 6.4. The SCADA HMI is often housed in a remote control center, and when this alert is sent, control center operators notify relevant site staff so that they can take the necessary steps. When site staff approach the relay, the above tap alarm target LED illuminates, as shown in Figure 6.10. The problem of fault location benefits maintenance employees on-site by reducing fault-finding times and thereby enhancing capacitor bank availability to support the power system.

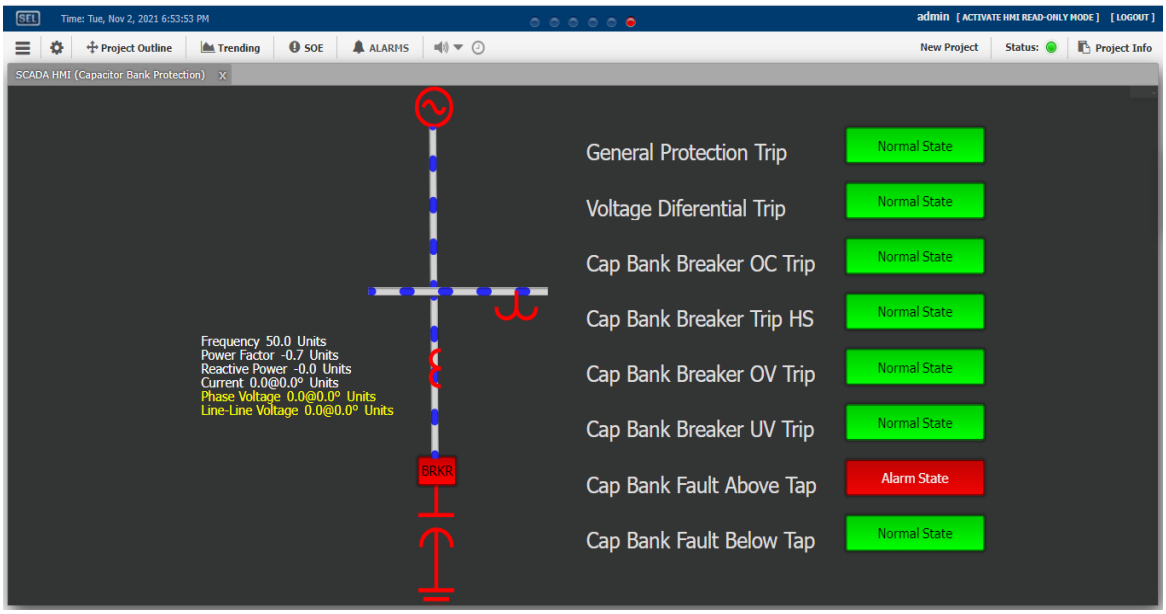

Figure 6.10. SCADA HMI for alarm mode of operation for three elements failure above the capacitor bank tap

Table 6.4 summarizes the test results on RelaySimTest program. As shown in Table 6.4, the measured differential voltage is 4.14 V, which is greater than the alarm mode threshold pickup voltage of 3.9 V.

Table 6.4. Three element failures above tap simulation results summary

THREE CAPACITOR ELEMENT FAILURES ABOVE TAP: (CASE THREE)				
	RelaySimTest Results		SynchroWAVe Event Test Results	
	Bus Bar Voltage	Tap Voltage	Bus Bar Voltage	Tap Voltage
Primary (L-N)	83.753 kV	40.433	N/A	N/A
Secondary (L-N)	120.86 V	134.78 V	N/A	N/A
Differential Voltage	4.14 V		N/A	

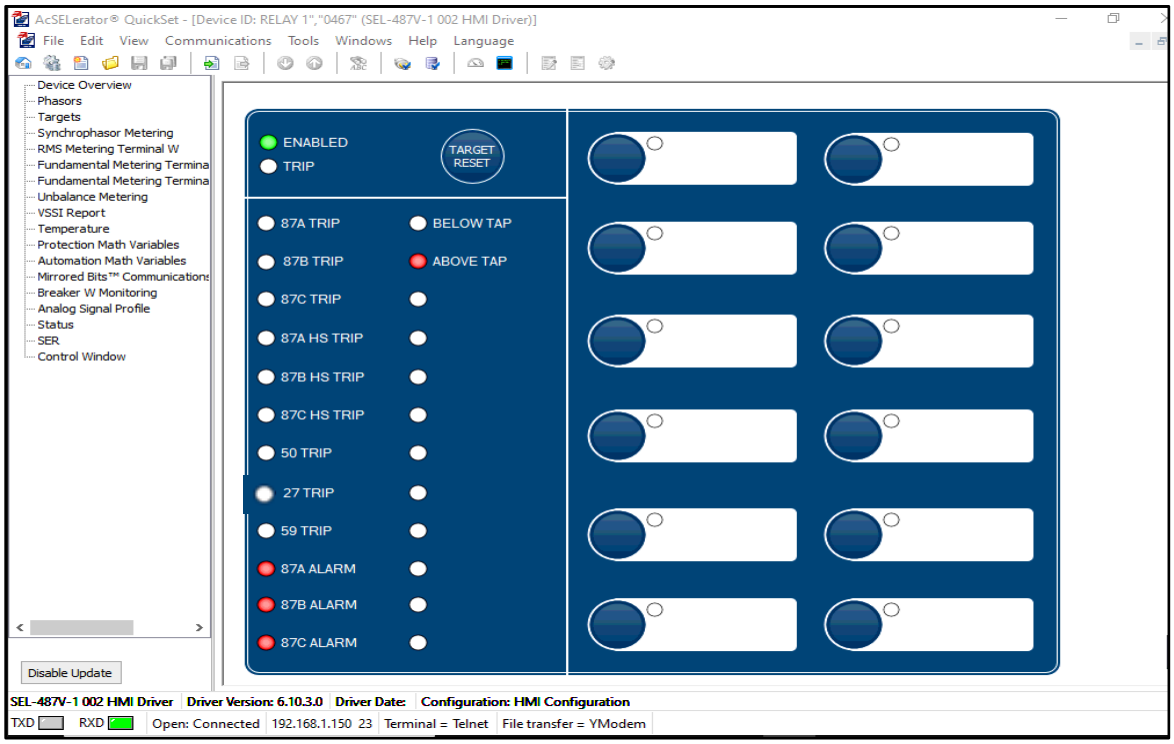

Figure 6.11. HMI for alarm mode operation for three elements failure above capacitor bank tap

Because the protective elements are not triggered in alarm mode, the SyncroWAVe event and associated data are not applicable in this scenario as given in Table 6.4. The trip below tap, which is case 9 simulation of four capacitor element failures, is presented in the next section.

6.4 Case 9: Four element failures below tap

Figure 6.12 shows a four-element failure below the capacitor bank tap simulated in RelaySimTest simulation environment. The voltages measured on the left side of the screen are 120.92 V (bus bar) and 146.30 V. (Tap). A trip signal is seen exactly 145

milliseconds after the fault occurred at 500 milliseconds from the start of the simulation, which lasted approximately 1150 milliseconds. A trip signal can be seen at both relay hardwired outputs and GOOSE outputs, including T87PDIF1 and TRIPPTRC1 logical nodes. Due to the relatively small distances from the IED and virtual circuit breaker on the lab scale implementation, testing and simulation of GOOSE signals are triggered before the hardwired outputs, however the margins are minimal (around 10 ms).

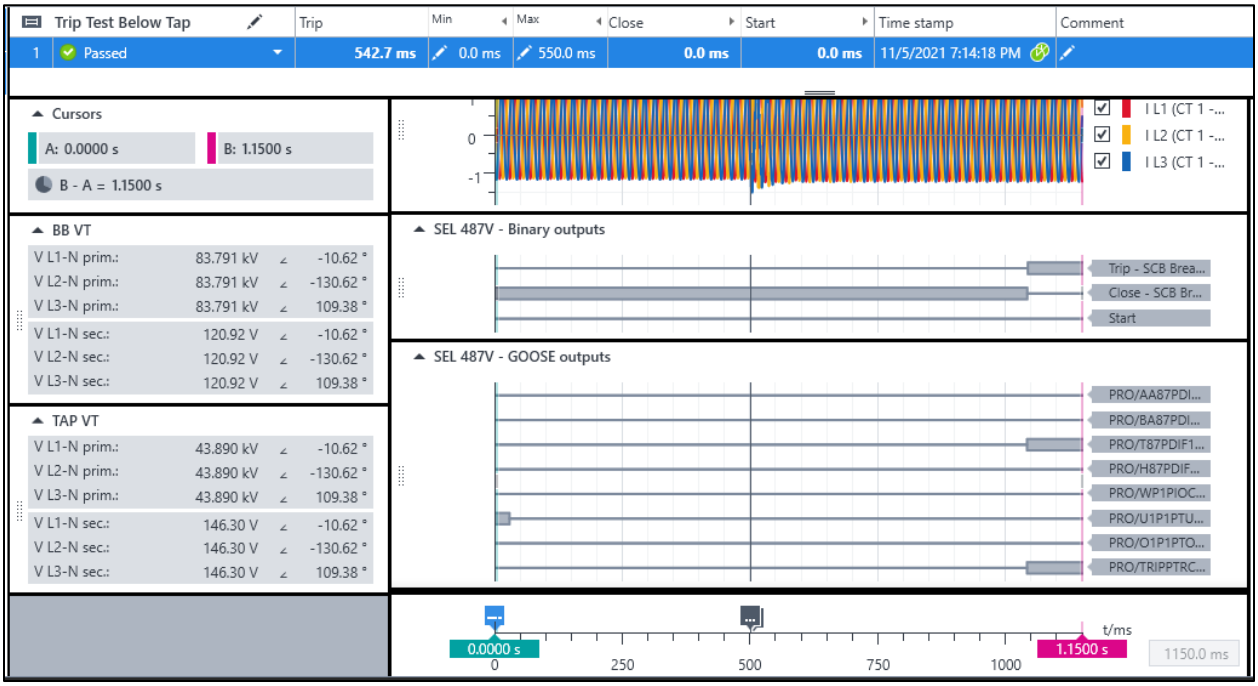

Figure 6.12. RelaySimTest, trip mode operation simulation results for four element failures below the bank tap

RelaySimTest voltage waveforms for both BB and Tap voltages are shown in Figure 6.13. After 500 milliseconds of simulation, there is a small increase in voltage on the tap voltage, which is consistent with the value of 146.30 V shown on the digital display, which has increased from 139.43 V for normal operation with no element failures. The relay trip in SEL487V IED generate event files, which were then analyzed. An SEL software application called SynchroWAVe Event is used to analyze these event files. Figure 6.14 depicts a SynchroWAVe Event for a Trip Below Tap Test Case. The magnitudes of the primary voltages for the bus bar and tap are 83.737 kV (phase A) and 43.903 kV (phase A), respectively.

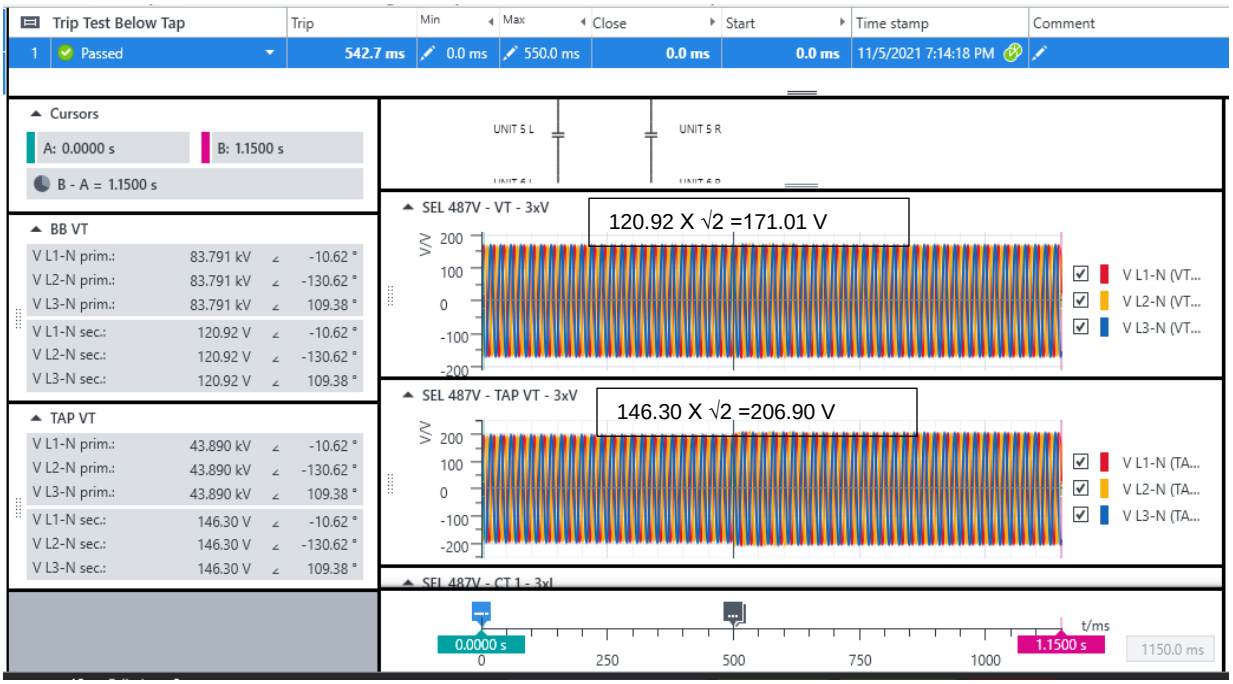

Figure 6.13. RelaySimTest simulation voltage waveforms for four element failures below tap

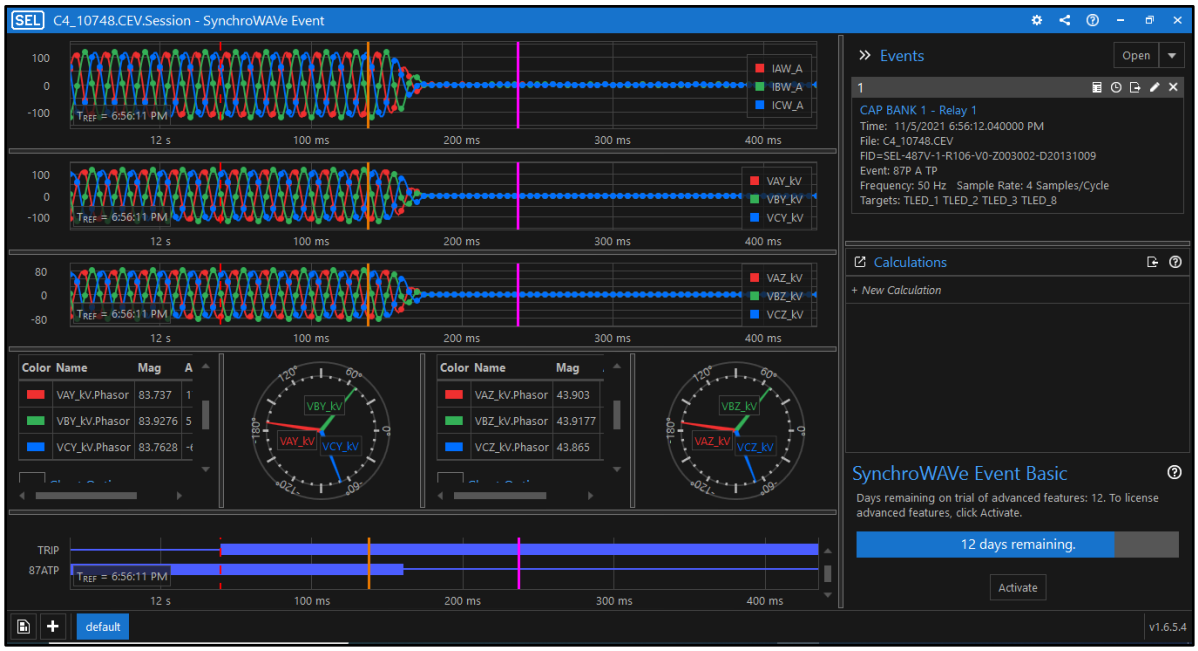

Figure 6.14. SynchroWAVe Event for an 87-voltage differential trip for four element failures below bank tap

When the voltage ratios are used to convert to secondary voltages, the result is 120.83 V for the bus bar and 146.34 V for the tap. The voltages are quite comparable to what is reported on RelaySimTest for the same test case, with a very slight change due to equipment tolerances: 120.92 V for the bus bar and 146.30 V for the tap. A trip signal is shown at the bottom of the screen, which is triggered by the voltage differential element (87ATP) that was detected.

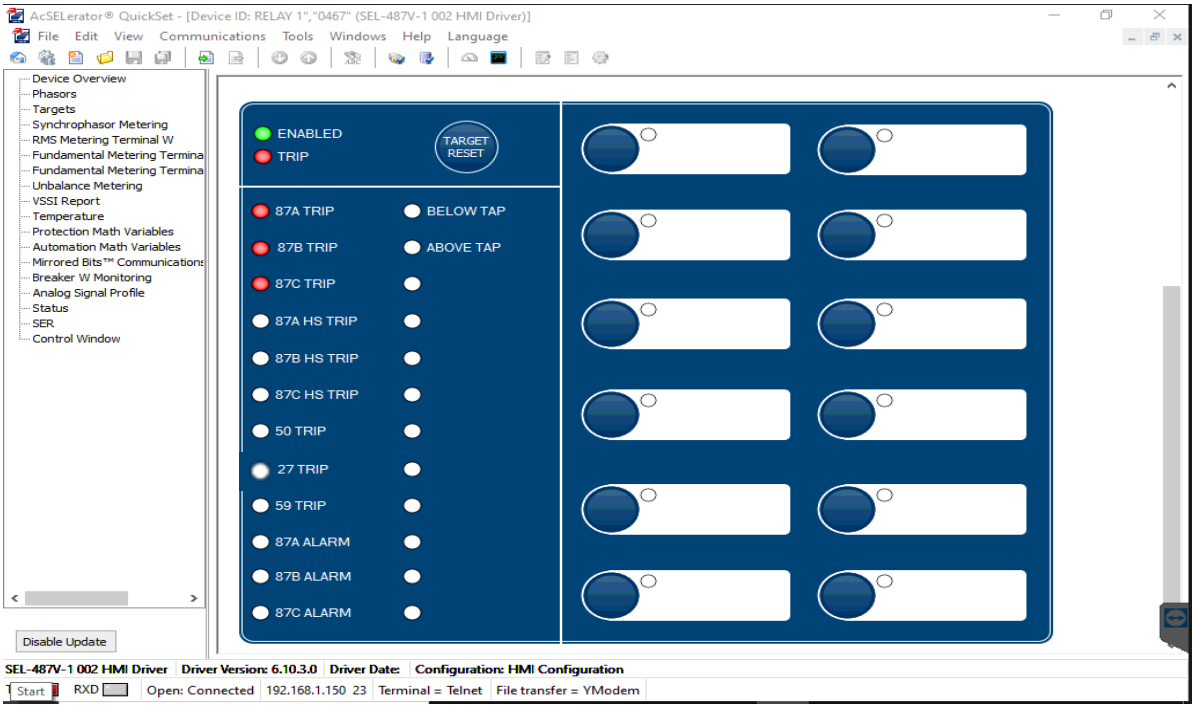

Figure 6.15. Online HMI to view SEL487V trip status via target LED for four capacitor element failure below the tap

A similar depiction of the trip signal is given in Figures 6.15 and 6.16, which feature AcSELerator QuickSet HMI and SCADA HMI, respectively. The QuickSet HMI screenshot shows voltage differential elements for each phase and the general trip element, but the SCADA HMI screenshot shows a voltage differential trip for any phase and general trip signals, which reflect the T87PDIF1 and TRIPPTRC1 logical nodes, respectively. Table 6.5 presents a summary of test findings as well as a comparison of the results of RelaySimTest and SynchroWAVE Event software. As stated in the table, the differential

voltage detected on RelaySimTest is 5.78 V, whereas the differential voltage measured by the relay via the SynhroWAVE software application is 5.90 V.

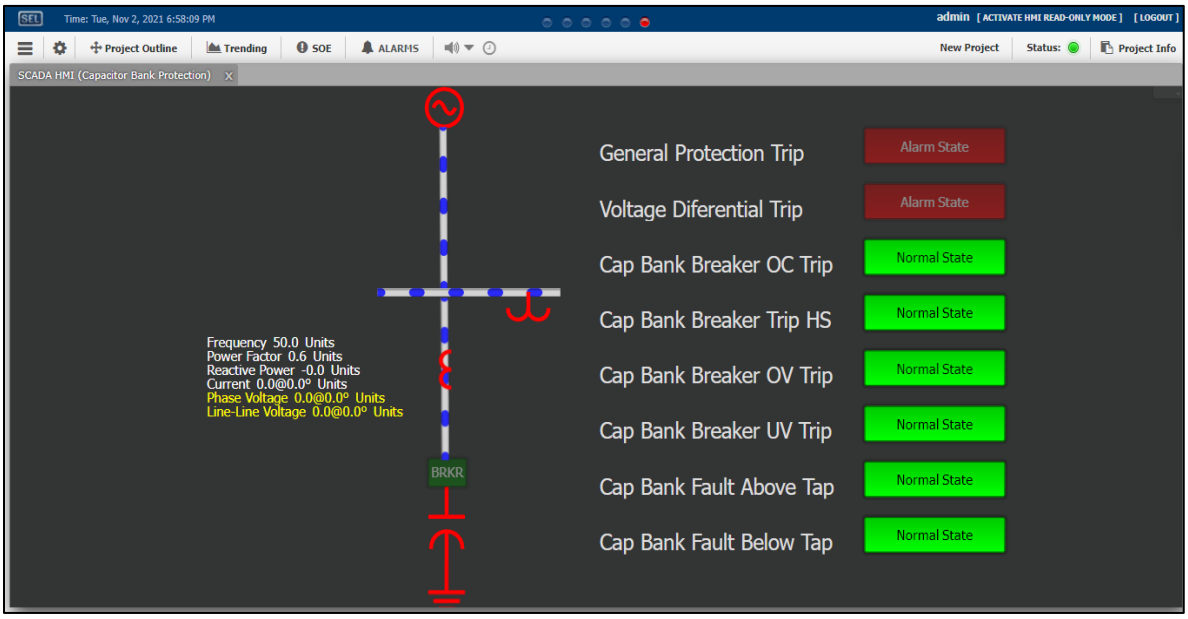

Figure 6.16. SCADA HMI to view SEL487V trip status via IEC 61850 MMS application for four capacitor element failure below the tap

Table 6.5. Four element failures below tap simulation results summary

FOUR CAPACITOR ELEMENT FAILURES BELOW TAP: (CASE NINE)				
	RelaySimTest Results		SynchroWAVe Event Test Results	
	Bus Bar Voltage	Tap Voltage	Bus Bar Voltage (ph A)	Tap Voltage (ph A)
Primary (L-N)	83.791 kV	43.890 kV	83.737 kV	43.903 kV
Secondary (L-N)	120.92 V	146.3 V	120.83	146.34 V
Differential Voltage	5.78 V		5.90 V	

The following section focuses on case 5, which has five capacitor element failures above the tap.

6.5 Case 5: Five element failures above tap

RelaySimTest findings for the high set above tap test case with five capacitor element failures are shown in Figure 6.17. The recorded secondary voltages are 120.97 V (bus bar) and 131.09 V (tap), and a trip indicator appears approximately 150 milliseconds after the fault occurs at 500 milliseconds from simulation start. A trip signal can be seen at both

relay hardwired outputs and GOOSE outputs, particularly at the H87PDIF1 and TRIPPTRC1 logical nodes. Due to the relatively small distances from the IED and virtual circuit breaker on the lab scale implementation, testing and simulation of GOOSE signals are triggered before the hardwired outputs, however the margins are minimal (around 10 ms). RelaySimTest voltage waveforms for both BB and Tap voltages are shown in Figure 6.18. After 500 milliseconds from simulation start, there is a small decrease in voltage on the tap voltage, which is consistent with the value of 131.09 V as visible on the digital display, which decreased from 139.43 V for normal operation with no element failures.

Figure 6.19 depicts a SynchroWAVe Event for a high set above tap test case. The magnitudes of the primary voltages for the bus bar and tap are 83.8079 kV (phase A) and 39.2654 kV (phase A), respectively. When the voltage ratios are used to convert to secondary voltages, the result is 120.93 V for the bus bar and 130.88 V for the tap. The voltages are quite comparable to what is reported on RelaySimTest for the same test scenario, with a very minor difference due to equipment tolerances: 120.97 V for the bus bar and 131.09 V for the tap. A trip signal is shown at the bottom of the screen, which is triggered by the voltage differential element (87ATP) that was detected.

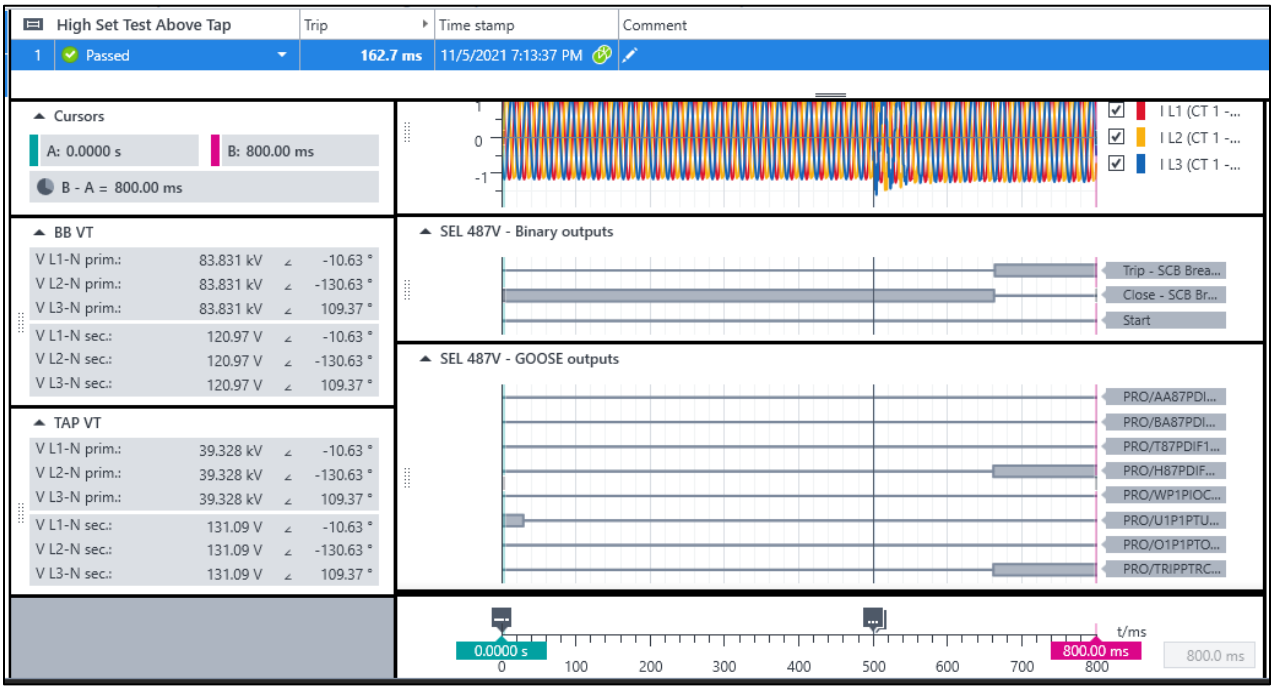

Figure 6.17. RelaySimTest, high set trip mode operation simulation results for five element failures above the tap

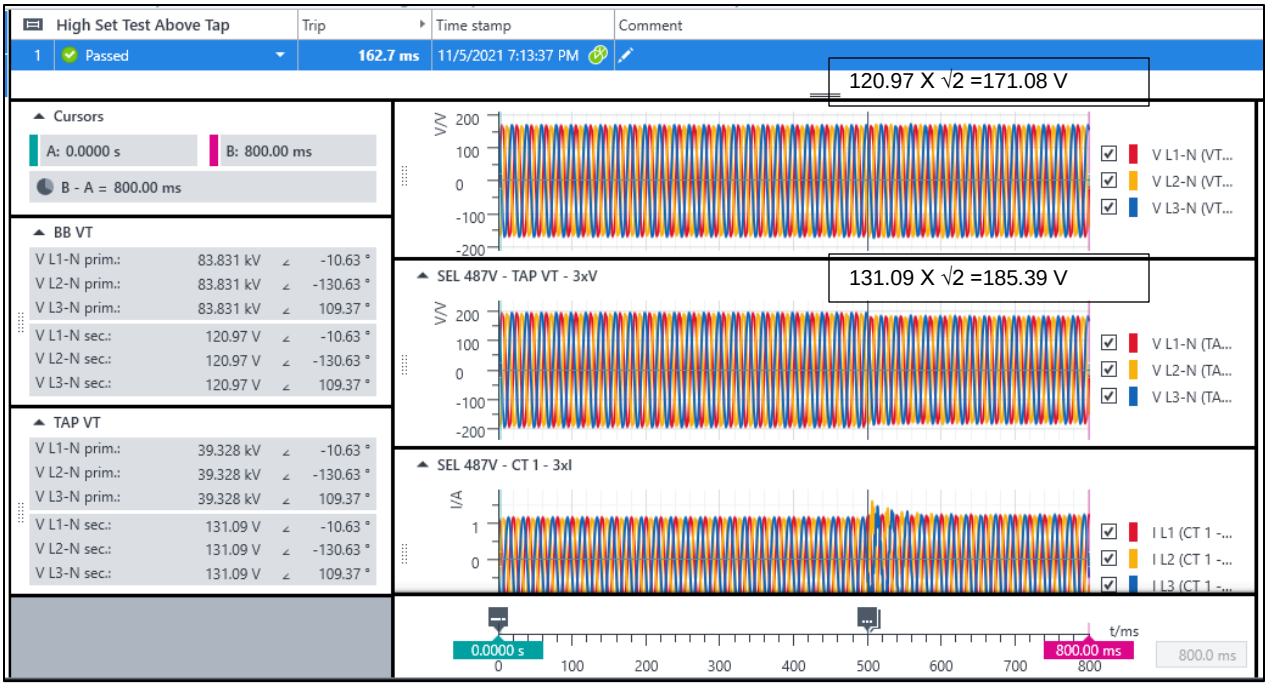

Figure 6.18. RelaySimTest simulation voltage waveforms for five element failures above tap

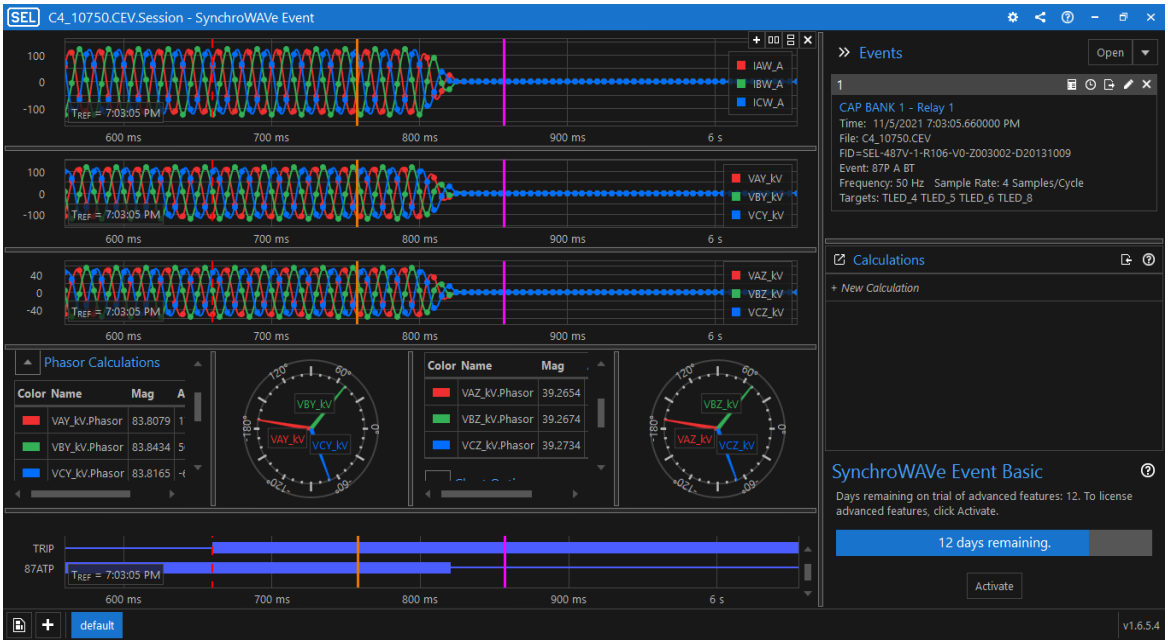

Figure 6.19. SynchroWAVe Event for a high set voltage differential trip for five element failure above the tap

Figure 6.20 depicts a SCADA HMI depiction in which the Trip High Set and general trip signals are asserted as a result of a failure of five capacitor elements above the tap. This helps to notify control room operators of the malfunction, who will then notify site workers who will execute maintenance services. Visual inspection of the relay on-site reveals the target LEDs, as illustrated in Figure 6.21, which is represented by the AcSELerator QuickSet HMI. As illustrated in the screenshot, a general trip and high set trip signal is displayed for all three phases, assisting maintenance technicians in identifying the faulted phases, lowering fault finding times and boosting capacitor bank availability.

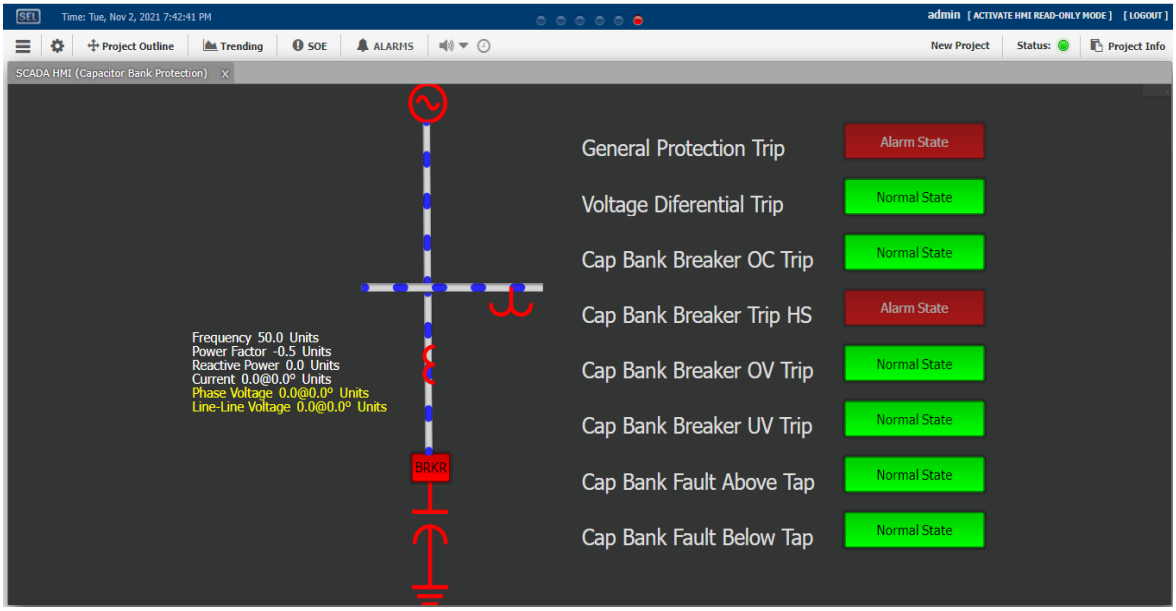

Figure 6.20. SCADA HMI to view SEL487V highest trip status via IEC 61850 MMS application for five capacitor element failure above the tap

Table 6.6. Simulation results summary for five element failures below the tap

FIVE CAPACITOR ELEMENT FAILURES BELOW TAP: (CASE FIVE)				
	RelaySimTest Results		SynchroWAVe Event Test Results	
	Bus Bar Voltage	Tap Voltage	Bus Bar Voltage	Tap Voltage
Primary (L-N)	83.831 kV	39.328 kV	83.8079 kV	39.2654 kV
Secondary (L-N)	120.97 V	131.09 V	120.93 V	130.88 V
Differential Voltage	7.44 V		7.59 V	

Table 6.6 presents a summary of test findings and a comparison of RelaySimTest and SynchroWAVE Event software application results. As demonstrated in the table, there is

only a 0.15 V difference in voltage differential measurements seen by these software applications, which is most likely attributable to equipment tolerances.

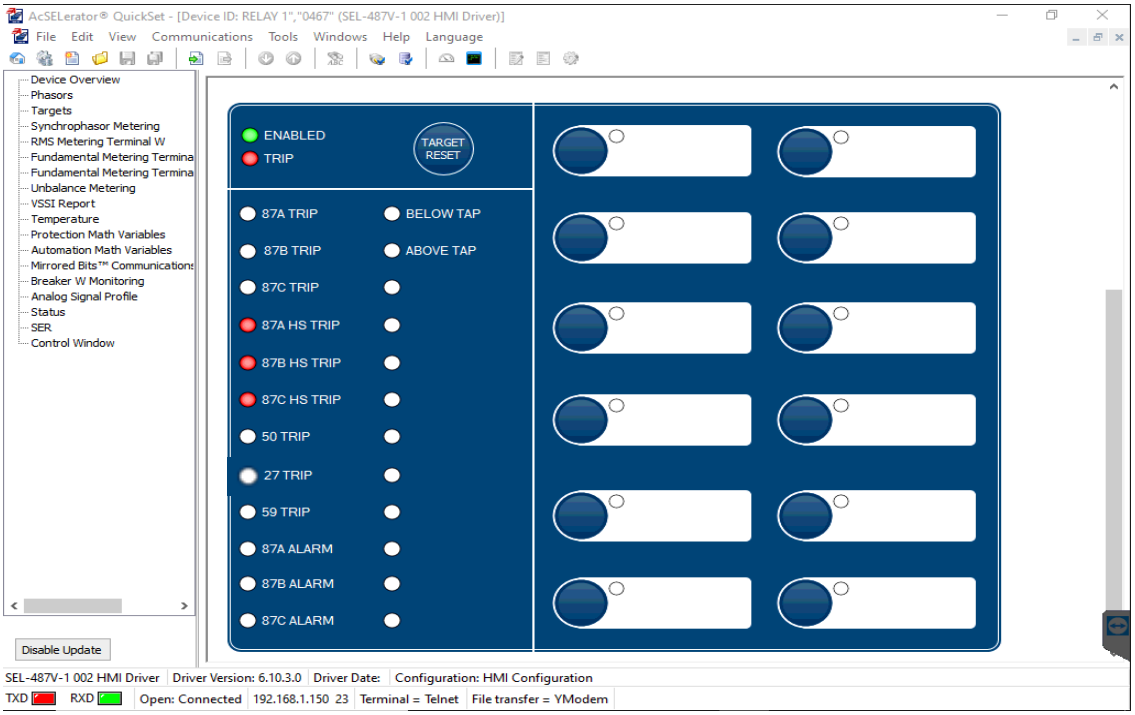

Figure 6.21. Online HMI to view SEL487V highest trip status via target LED for five capacitor element failure above the tap

The next section describes a highly improbable circumstance in which six capacitor element failures above the tap and six capacitor element failures below the tap occur concurrently.

6.6 Case 19: Six element failures above and below tap

Case 19 represents a highly unusual circumstance in which six element failures above tap and six element failures below tap occur concurrently. Because of the balanced pattern of failures, the main voltage differential protection method does not detect this problem because the resultant voltage differential remains zero throughout the various number of element failures (above and below). However, the state creates greater currents since the total impedance drops and the voltages across the remaining individual capacitor parts increase, causing strain. For this circumstance, the pickup current is set to 96 A, which is equal to 110 percent voltage loading across the remaining capacitor elements. Figure 6.22

depicts the results of an Overcurrent (Overload) Test Case simulation. The voltage readings for the bus bar show 121.41 V, whereas the voltage measurements for the tap show 140.22 V. In this scenario, as mentioned in the protective settings calculation chapter, the differential voltage remains constant since the failures above and below the tap are balanced, despite the failure of 12 (6 above and 6 below) capacitor parts. The fault current is observed to have exceeded the pickup value of 96 A to 96.57 A, resulting in the receipt of a trip signal around 150 milliseconds after the incident. The CT 1 measurements signals provides a graphical representation of current growth, which reveals a significant increase in current. Trip signals from hardwired binary outputs and GOOSE outputs are displayed on the screen, with GOOSE signals outperform the hardwired outputs. TRIPPTRC1 (generic conditional trip) and WP1PIOC1 are the GOOSE logical nodes with a high status (overcurrent element).

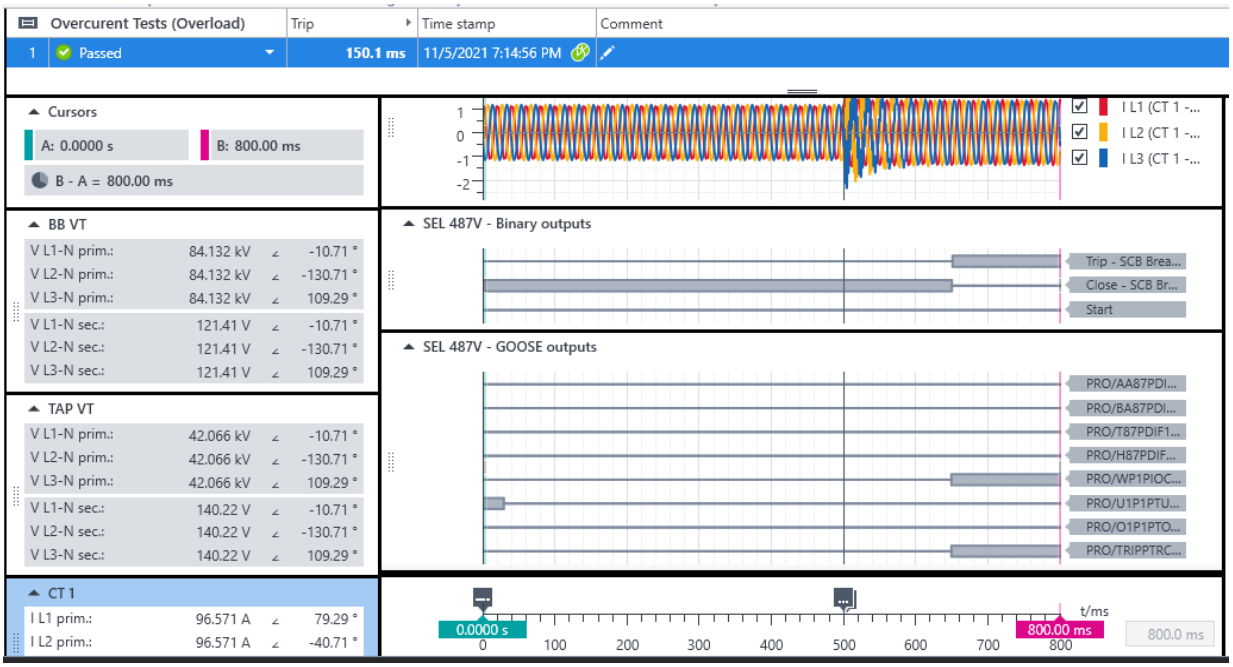

Figure 6.22. RelaySimTest overcurrent simulation results for six element failures above and below the tap

RelaySimTest voltage waveforms for both BB and Tap voltages are shown in Figure 6.23. After 500 milliseconds of simulation, there is a small decrease in voltage on the tap and BB voltages; nonetheless, the increase is proportional and results in differential voltages of 0 V.

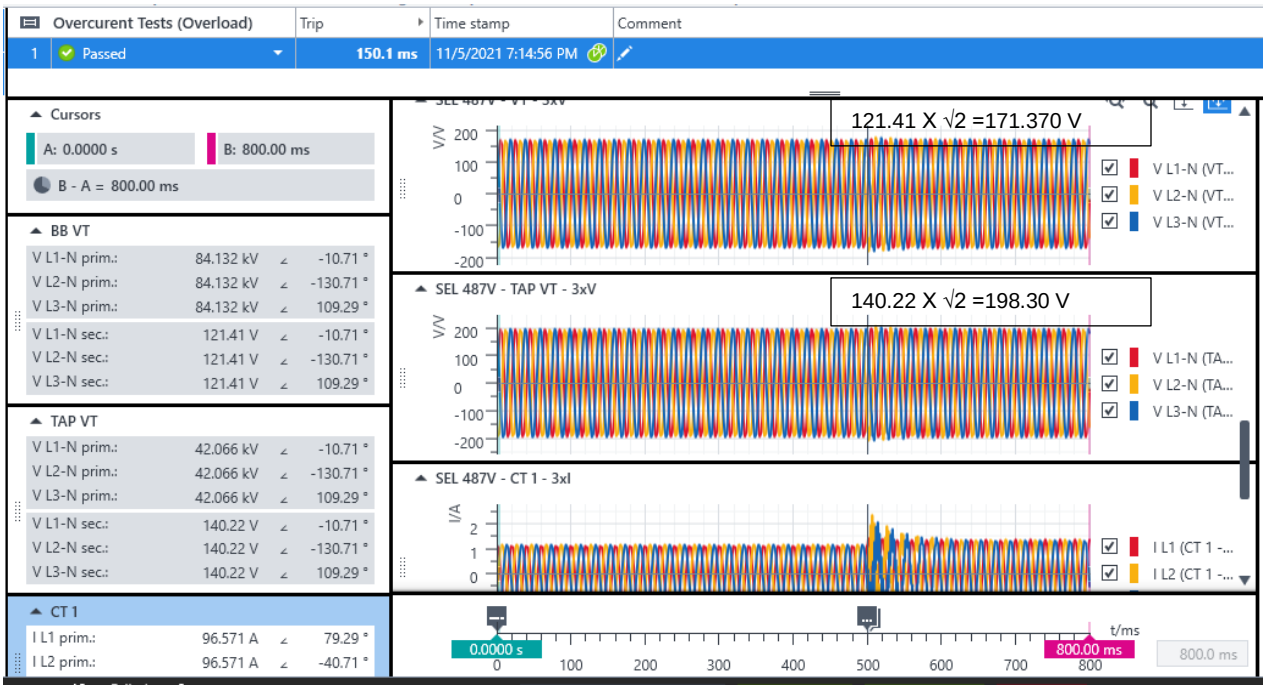

Figure 6.23. RelaySimTest voltage waveforms for overcurrent simulation results for six element failures above and below the tap

Figure 6.24 depicts a SynchroWAVe Event for an Overcurrent (Overload) Test Case in which a total of twelve capacitor element failures (six above and six below) occur concurrently. The magnitudes of the primary voltages for the bus bar and tap are 84.0867 kV (phase A) and 42.0595 kV (phase A), respectively. When the voltage ratios are used to convert to secondary voltages, the result is 121.34 V for the bus bar and 140.198 V for the tap. The voltages are quite close to what is seen on RelaySimTest for the same test scenario, with 121.41 V for the bus bar and 140.22 V for the tap, with a very minor discrepancy owing to equipment tolerances. A trip signal is shown at the bottom of the screen, which is created by the overcurrent element rather than the voltage differential element (87ATP), which did not pick up in this case. The second measurement, which depicts current phasor diagrams, reveals current magnitudes greater than 96.4 A, which is greater than the pickup value of 96 A.

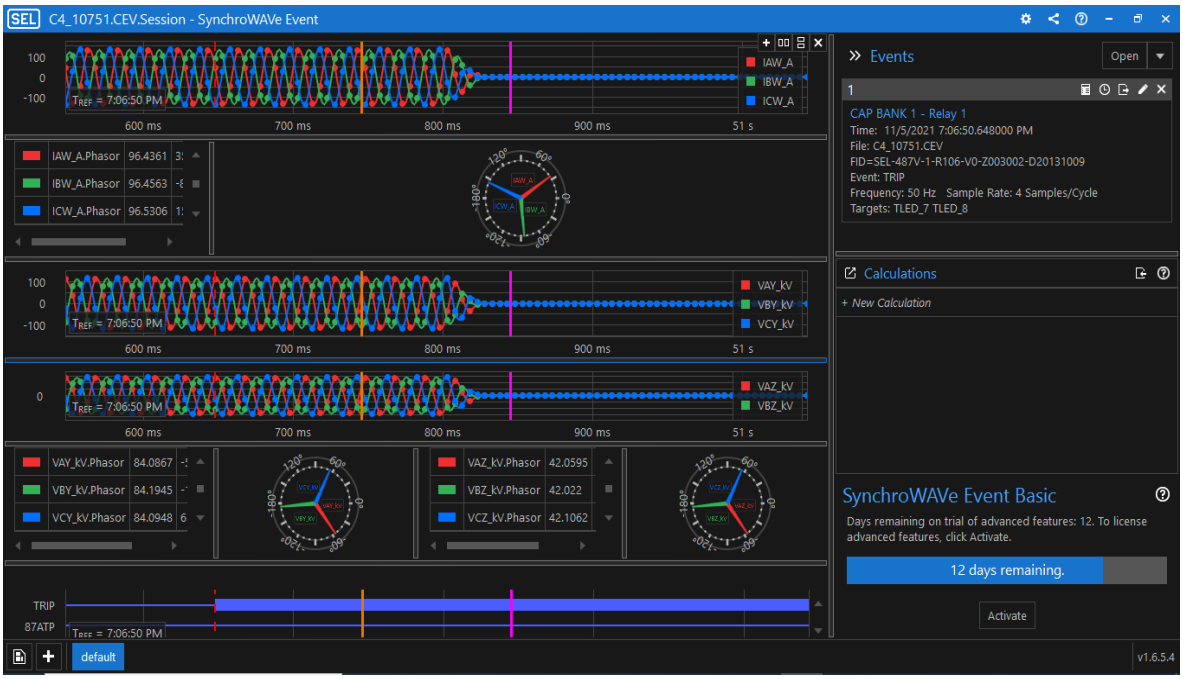

Figure 6.24. SynchroWAVe Event for an overcurrent simulation results for six element failures above and below the tap

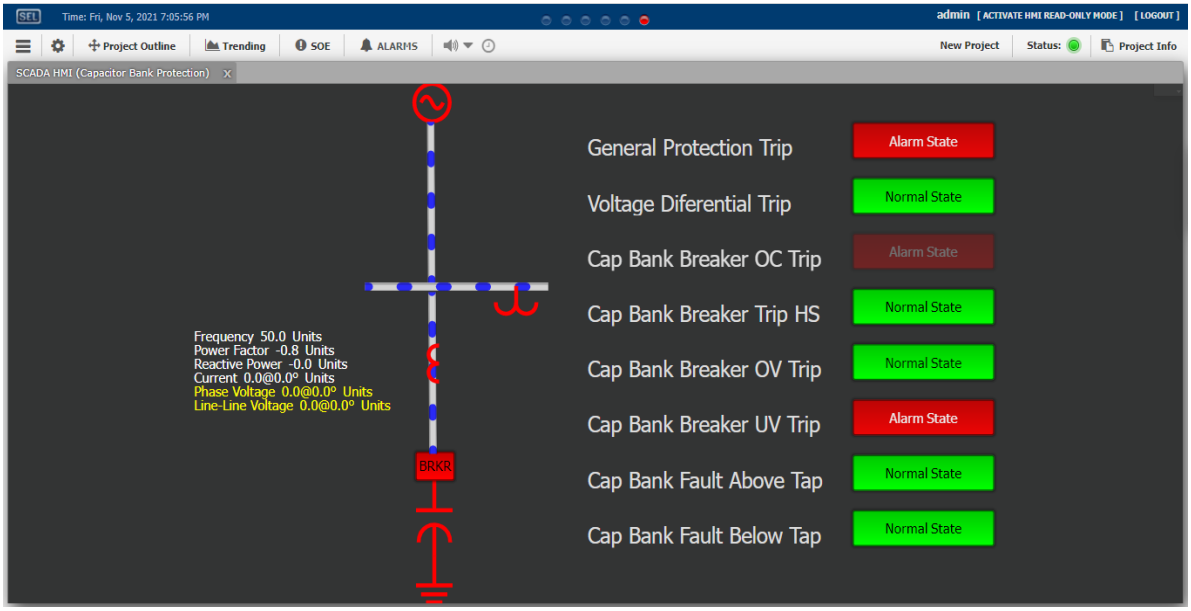

Figure 6.25. SCADA HMI to view SEL487V overcurrent trip status via IEC 61850 MMS application for six element failures above and below the tap

Figure 6.25 depicts a SCADA HMI representation of case 19 with six capacitor element failures above the tap and six capacitor element failures below the tap. To signify a breaker

trip due to an overcurrent condition, a general trip signal and an overcurrent trip signal are asserted. The screen also shows an undervoltage because it was not turned off for the test but was omitted in the trip logic during testing.

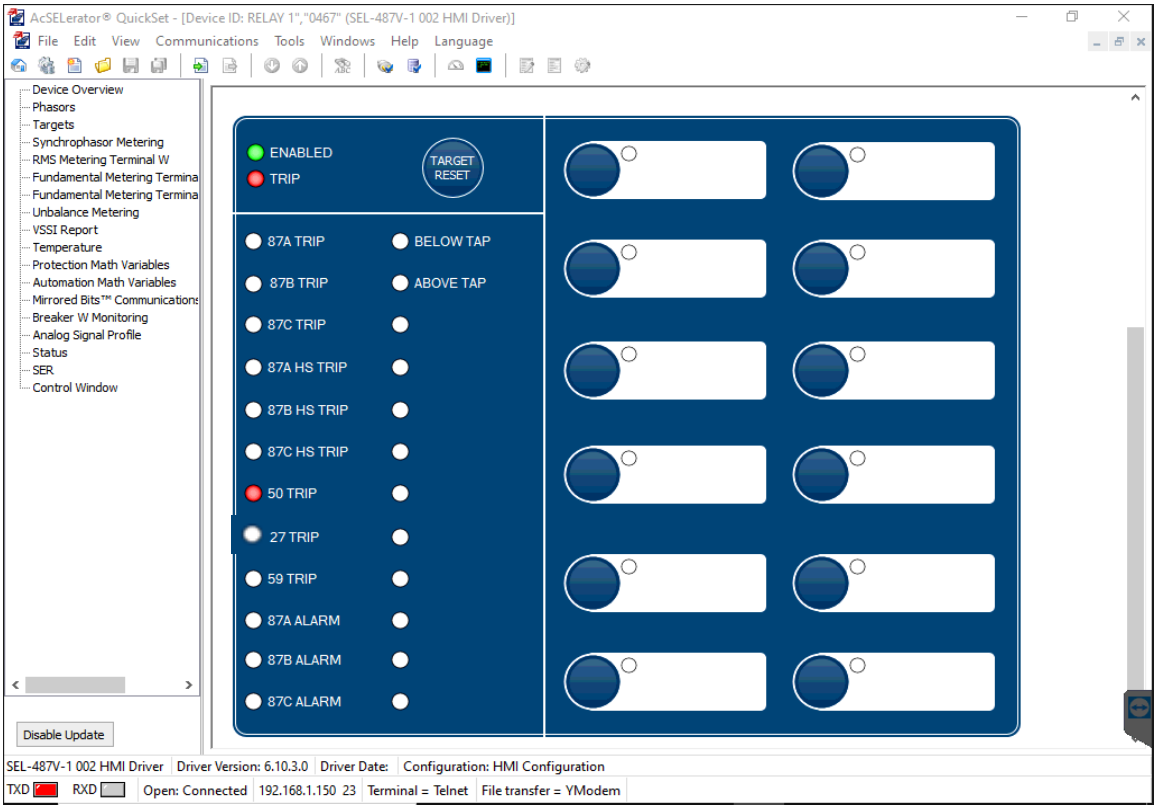

Figure 6.26. Online HMI to view SEL487V overcurrent simulation trip status via target LED for six element failures above and below the tap

Figure 6.26 depicts an AcSELerator QuickSet HMI for an overcurrent trip state, with relay LEDs illuminated. When analyzing the relay operation after a fault, this is what is observed. An overcurrent trip LED and a general trip indication LED are both enabled. Also shown is an under voltage trip LED, which was not switched off during the test but was excluded in the trip logic. Table 6.7 presents a summary of test findings as well as a comparison of the RelaySimTest and SynhcorWAVE Event software applications. The differential voltages measured by these two software tools are quite similar, with only a 0.05 V variation. As demonstrated in the table, despite the ongoing failure of capacitor elements, the differential voltages remain zero since the failures are balanced above and below the tap.

Table 6.7. Simulation results summary for six element failures above and below the tap

TWELVE CAPACITOR ELEMENT FAILURES (SIX BELOW AND SIX ABOVE TAP): (CASE NINENTEEN)				
	RelaySimTest Results		SynchroWAVe Event Test Results	
	Bus Bar Voltage	Tap Voltage	Bus Bar Voltage	Tap Voltage
Primary (L-N)	84.132 kV	42.066 kV	84.0867 kV	42.0595 kV
Secondary (L-N)	121.41 V	140.22 V	121.34	140.198 V
Differential Voltage	0.021 V		0.071 V	

The following section provides chapter conclusion with summary and discussion on simulation results.

6.7 Simulation results discussion

Sections 6.2 to 6.6 analyse the test results of the specified test cases, while the section summarizes the results. As described in section 6.2, the failure of two capacitor elements results in differential voltages below the specified pickup value, and no action is done in both alarm and trip mode operation modes. A failure of three elements above tap causes a differential voltage above alarm pickup value of 3.9 V, resulting in an alarm above tap being issued to the SCADA system and shown on relay target LEDs. When four of the following elements fail, the differential voltage rises over the trip pickup value, and the relay issues a trip signal 500 milliseconds after pickup. Five capacitor element failures above tap caused differential voltages to exceed the high set pickup value, resulting in a trip signal being issued after 150 milliseconds. Six element failures above and six element failures below the tap result in differential voltages of 0 V, and an overcurrent backup system is engaged, issuing a trip signal after 150 milliseconds. The test results are consistent with the expectations and calculations provided in the protection scheme's chapters 3, 4, and Appendix A.3. Voltage differential protection scheme as a primary protection scheme and backup protection methods applied prove to be fast and reliable for all test scenarios provided.

The next section provides conclusion, summary on simulation test results presented in this chapter.

6.8 Conclusion

The engineering setup and lab scale test bench outlined in Chapter 5 are evaluated, and the findings are discussed in Chapter 6. Case 2 (two element failures above tap), Case 3 (three element failures above tap), Case 9 (three element failures below tap), Case 5 (five element failures above tap), and Case 19 are the five test cases are presented and analysed (simultaneous failure of six element failures above tap and six element failures below tap). The examination of the findings revealed that the configured protection settings for the implemented protection schemes proved to be very successful and provide efficient capacitor bank protection.

The use of the IEC 61850 standard enhances communication and reduces the amount of wiring required in typical systems. AA87PDIF1 (alarm above tap), BA87PDIF1 (alarm below tap), T87PDIF1 (Differential Trip), H87PDIF1 (High Set Differential Trip), WP1PIOC1 (Overcurrent), U1P1PTUV1 (Under voltage), O1P1PTOV1 (Overvoltage), and TRIPPTRC1 are among the GOOSE logical nodes used (general conditional trip). IEC 61850 MMS is used for SCADA communications, with buffered report control blocks (BRCB) for binary data and unbuffered report control blocks (URCB) for non-binary data (URBC).

The use of a voltage differential protection method with a SEL 487V protection relay proved useful since it allows for the identification of a fault site on a specific phase and whether it is above or below the tap. System-based testing approach has been shown to be more effective than traditional testing methods since it provides not only steady state system settings but also transient state system circumstances. RelaySimTest, which is utilized for system-based testing methodologies, has been discovered to be a very intuitive and effective means of testing protection systems.

The next Chapter provides conclusion, project deliverables, future work and publications.

7. CHAPTER SEVEN: DISCUSSIONS AND CONCLUSIONS

7.1 Introduction

The chapter discusses and concludes the thesis on capacitor bank protection, substation automation, system-based testing, and lab scale implementation test findings. The chapter is organized as follows, as shown in Figure 7.1: section 7.2 discusses the overall thesis, section 7.3 concludes the thesis deliverables, section 7.4 discusses the thesis application to academic/research and industry, section 7.5 discusses future work and recommendations, section 7.6 discusses publications, and section 7.7 concludes the overall thesis.

Figure 7.1. Overview of chapter 7 in flow diagram form

The next section provides overall thesis discussion.

7.2 Discussions

Capacitor banks play a crucial part in power system networks, and their availability after installation should be practically ensured when needed. The critical components of the network, ensuring voltage profile improvement, loss minimization, power factor correction, and so on. The simulation studies performed in Chapter 3, sections 3.2 to section 3.4, with DIGSILENT software have successfully proved that the above listed benefits are achieved. With the addition of a 22 MVar capacitor bank in the considered power system network, voltage on Bus 3 improved from 0.96 p.u. to 0.97 p.u., while voltage on Bus 4 increased from 0.93 p.u. to 0.95 p.u. Active power losses were reduced from 0.82 MW to 0.66 MW, and reactive power losses were reduced from 10.89 MVar to 9.74 MVar. According to the studies, without the capacitor bank, the network's customer supply requirements cannot be met, and such voltage sensitive equipment may be damage by such low voltages. This circumstance may result in penalties being imposed on the utility or the consumer who makes claims for inadequate supply and damaged equipment. As a result, capacitor banks require fast and dependable protection.

Thesis Chapter4 discusses voltage differential protection as a suitable scheme for the project. The protection settings are calculated manually for each failure of capacitor elements. This is done to define the trigger points or thresholds for each element that must be taken to ensure better capacitor bank availability while ensuring ease of maintenance for site workers. The thresholds to be determined for alarming when a few capacitor elements fail but the voltage on the remaining elements is around 105 percent, a trip condition when the voltage is 110 percent, and a high set when the voltage is greater than 110 percent. There are temporal delays connected with these threshold points: 2 seconds for the alert, 500 milliseconds for the trip, and 120 milliseconds for the high set.

Using different scenarios to calculate settings, it was revealed that there are two possibilities that are rare and highly unlikely to occur. The first is the failure of capacitor components on parallel strings in the same part of the bank. As the differential voltage varies in small steps, more elements must fail before they can be picked up than in the regular scenario. The second possibility is a failure of capacitor elements on both bank halves (small voltage deviation) at the same time that is not detected by the protection method, resulting in a differential voltage of zero. As more capacitor element failures were simulated, the voltage computed on the remaining healthy capacitor elements exceeded

110 percent, up to six element failures above and six element failures below the tap. This scenario requires the adoption of backup protection with the aid of DMT Overcurrent protection is utilized. According to the computation, the threshold for stage 1 is 96 A, which is linked to 6 element failures above tap and 6 element failures below tap. The values for stages 2 and 3 were calculated to be 108 A and 324 A, respectively. Another type of backup protection method is the over/under voltage scheme, which is utilized as system protection for defects that occur outside of the bank installation. This protection technique was mostly useful for non-ground failures because there were no zero-sequence components to flow through the capacitor bank to ground.

Using system-based testing methodologies, a lab size test bench is used to confirm the correct operation and effectiveness of the voltage differential protection scheme as described. The test bench required the configuration of relay software and hardware setup. The simulation test findings are the protection requirements and are included in the thesis. The research outcome intends to use distributed type of protection testing using RelaySimTest application suite, but there are several areas for improvement, which are mentioned in the following section. Using system-based testing methodologies, a lab size test bench is used to confirm the correct operation and effectiveness of the voltage differential protection scheme as described. The test bench required the configuration of relay software and hardware setup. The simulation test findings are the protection requirements and are included in the thesis. The research outcome intends to use distributed type of protection testing using RelaySimTest application suite.

7.3 Thesis deliverables

The thesis is divided into seven chapters, with the following major contributions: a) A review of the literature on shunt capacitor bank protection, IEC 61850 GOOSE and MMS applications for shunt capacitor bank protection, b) Network work modelling, simulation, and fault study using the DIGSILENT simulation tool, c) Capacitor bank protection relay (SEL487V) engineering configuration settings, GOOSE and MMS configurations, differential voltage calculations (dv), and finally validating the configuration d) The simulation findings reported for the various case studies demonstrate that IEC 61850

simulation results outperformed hardwired outputs and meet protection speed and reliability requirements.

7.3.1 Research methodology

The research methodology of the project work is provided in SLD in Figure 3.4 in Chapter 3 and its methodology for lab-scale implementation is provided in Figure 1.1 and described in Chapter1, section 1.9.
Using the methodology, the lab-scale testing, simulation results for the voltage differential main and OC, OV, UV backup protection schemes are provided in Chapter 6 for the considered case studies.

7.3.2 Literature review

The deliverables for Chapter 2 are to give a literature review of publications relating to the study problem and background theory to the research topic, all of which is successfully presented in the thesis. Literature review is divided into three groups, i) Substation Automation System (SAS) whereby IEC 61850 implementation and application review is discussed, ii) Capacitor Bank Protection (CBP) which provides review of published material about capacitor bank protection, iii) System-Based Testing (SBT) which provides literature review on material published about newly developed test method.

7.3.3 Modelling of distribution networks, DIGSILENT simulation, fault and protection study for shunt capacitor banks

The thesis successfully completed chapter three deliverables, which comprised short circuit calculations, backup protection settings computation, DIGSILENT network simulations, backup protection settings testing, and findings presentation.

7.3.4 Theoretical approach for calculating shunt capacitor bank protection settings

The thesis deliverables for chapter four include voltage differential protection settings calculations for several failure scenarios as the main protection for a shunt capacitor bank, as well as results presented.

7.3.5 Lab-scale implementation and engineering configurations for protection relays, IEC 61850 configurations for GOOSE and MMS applications for shunt capacitor banks

The fifth chapter included lab scale implementation, which included engineering configuration of the entire protection system employing protection relays, a substation gateway, a system-based testing tool, time synchronization tools, and so on.

7.3.6 The findings of system-based testing and simulation for the case studies under consideration

The test results of the configuration described in chapter five were successfully reported in chapter six, and many case studies were examined. The second test scenario detailed a breakdown of two capacitor elements above tap, which results in no action being performed because the pickup thresholds are not surpassed. In test scenario 3, a failure of three capacitor elements above tap is described, and an alarm is issued after 2 seconds if the differential voltage exceeds the threshold value. In test case 9, four element failures below tap are discussed, and a trip signal is sent after 500 milliseconds if the trip threshold value is surpassed. Test case 5 is given, which represents five element failures above the tap and results in a high set trip signal issued after 120 milliseconds. An overcurrent backup protection test case 19 is discussed, which simulates a failure of six elements above tap and six elements below tap. After 120 milliseconds, a trip signal for test case 19 is issued. The listed test scenarios performed as expected and within the time constraints.

Chapter seven discusses and concludes the thesis, making recommendations and speculating on future study. Chapter one deliverables comprise the following: background to problem, thesis layout, give problem definition, project aims, project motivation, research design methodology, and so on, all of which are clearly documented in the thesis.

7.4 Application to academic/research and industries

The findings of the tests shed light on the testing of capacitor bank voltage differential protection solutions using system-based testing tools. The utilization of system-based testing methods allows for the testing of both steady-state and transient conditions.

Furthermore, the adoption of system-based testing methodologies, such as RelaySimTest software, enables for distributed protection testing, which allows for time synchronization of CMC test sets in accordance with the IEEE C37.118 Standard for Synchrophasor Measurements.

Cost savings are possible because to the remote testing capability provided by system-based testing, as testing may be performed from a remote location or central point for all end devices of interest. As a result, it is expected that the industry application will grow as additional test cases demonstrating various applications of system-based testing are published. It is also anticipated that the use of system-based testing in distribution systems will play an important role in smart grid applications.

The study establishes a foundation for distributed system testing for capacitor bank protection strategies using system-based testing. More study is needed to look at different applications, improve on present research, and ensure full implementation of the IEC 61850 Standard, including the IEEE C37.118 Standard.
At the moment, there is very little awareness about distributed testing with the usage of system-based testing in South Africa and around the world. In South Africa, Cape Peninsula University of Technology was the first to publish a Masters-level research thesis on the implementation of distributed testing methods. Because the institution possesses the essential support and tools at the Centre for Substation Automation and Energy Management Systems (CSAEMS) lab, distributed testing methodologies using system-based testing tools should be included in the curriculum from undergraduate to postgraduate.

7.5 Future work and recommendations

The section provides discussion on possible future work and recommendations that are necessary.

7.5.1 Future work

A complete implementation of the IEC 61850 standard, including the use of Sampled Values to ensure that no hardwiring is done between the CMCs and the protection relay.

The use of internally and externally fused capacitor banks for both grounded and ungrounded capacitor banks will also be examined. To establish the most fast and reliable protection system, a comparison of different capacitor bank protection schemes such as current unbalance, both phase and neutral, and neutral voltage differential must be performed. It is interesting to investigate the use of the IEC 61850 part 7-420 standard for capacitor bank protection with renewable integrated power plant.

7.5.2 Recommendations

The AcSELerator QuickSet Capacitor Bank Assistant tool, which is used to calculate differential voltage (dV) for varied number of capacitor element failures for both above and below the tap, should be improved to accommodate voltages greater than 10 kV and reactive power greater than 1 MVar. This is to expand the application's support to include not only low voltage capacitor (LVC) banks, but also centre tapped capacitor banks with greater ratings seen in transmission systems.
Another suggestion is to improve the software on the SEL 487V relay to accommodate sampled value data, allowing for full digitalization of capacitor bank protection schemes.
The listed recommendations may be valid across vendors, however the candidate only experienced with SEL vendor relay in this Thesis research work.

7.6 Publications

S Krishnamurthy, R Jones, MA Mquqwana 2020. System-based testing of a voltage differential protection scheme for shunt capacitor bank, Energy Reports 6, 243-259.
MA Mquqwana and S Krishnamurthy. 2021. System-based voltage differential testing for center-tapped shunt capacitor bank protection, Submitted to International Journal of Protection and Control of Modern Power Systems.

7.7 Conclusion

The protection method used for capacitor banks should be fast and reliable in order to protect the capacitor bank from faults within the bank as well as faults from the external system, while also protecting the system from the destructive repercussions that may be generated by the capacitor bank failure. The voltage differential protection scheme chosen as the primary protection in the project, proved to be adequate with supported backup

overcurrent and over/under voltage protection schemes. The protection requirements were met by the lab-scale tests, simulation results, and findings of the different case studies studied.

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A. Appendices

A.1 Short circuit calculations

This section contains extensive short circuit calculations that can be used to determine the maximum and minimum fault currents. Furthermore, by altering the fault position from bus 1 to bus 4, this appendix shows the minimum and maximum faults. This computation is important for configuring the protection functionalities outlined in Appendix A.3.

A.1.1. Short circuit current calculation at bus 1

Step 1: Maximum short circuit currents

$$Z_{B1max} = \frac{C_{max}\, x\, U_{NB1}}{\sqrt{3}\ x\, I''_{B1}} \cdot \frac{1}{t_r^2} \qquad \text{A.1}$$

Whereby,

Z_{B1max}	Impedance measured at bus 1 from the source/feeder
C_{max}	Voltage correction factor for maximum short circuit currents
U_{NB1}	Nominal system voltage at the connect point bus 1
I''_{B1}	Initial symmetrical short circuit current at the feeder connection bus 1
t_r	Rated transformation ration of the transformer

$Z_{B1max} = \frac{1.1\ x\, 66000}{\sqrt{3}\ x\, 8750} \cdot \frac{144900^2}{66000^2}$ = 23.09 Ω

$X_{B1} = 0.995\ Z_{B1}$ = 22.975 Ω

$R_{B1} = 0.1\ X_{B1}$ = 2.2975 Ω

Therefore,

Z_{B1max} = 2.2975 + j 22.975 Ω

Step 2: Minimum short circuit currents

$$Z_{B1min} = \frac{C_{min}\ x\ U_{NB1}}{\sqrt{3}\ x\ I''_{B1}} . \frac{1}{t_r^2}$$ A.2

Whereby,

C_{min} Voltage correction factor for maximum short circuit currents

$Z_{B1min} = \frac{1\ x\ 66000}{\sqrt{3}\ x\ 6998} . \frac{144900^2}{66000^2}$ = 26.25 Ω

$X_{B1} = 0.995\ Z_{B1min}$ = 26.12 Ω

$R_{B1} = 0.1\ X_{B1}$ = 2.612 Ω

Therefore,

Z_{B1min} = 2.612 + j 26.12 Ω

Step 3: Transformer 1

$$Z_T = \frac{U_{kr}}{100\%}\ x\ \frac{U_{rT}^2}{S_{rT}}$$ A.3

Whereby,

Z_T Impedance of the transformer

U_{rT} Rated voltage of the transformer HV side

S_{rT} Rated apparent power of the transformer

U_{kr} Short circuit voltage at rated current in percentage

$Z_T = \frac{6}{100}\ x\ \frac{144900^2}{150000000}$ = 8.398 Ω

$$R_T = P_{kr} x \frac{U_{rT}^2}{S_{rt}^2}$$ A.4

$R_T = 4500x \frac{144900^2}{150000000^2}$ = 0.0042 Ω

$U_{Rr} = \frac{P_{kr}}{S_{rt}} x\ 100\%$

$U_{Rr} = \frac{4500}{150000000} x\ 100\%$ = 0.0003%

$$U_{xr} = \sqrt{U_{kr}^2 - U_{Rr}^2}$$ A.5

$U_{xr} = \sqrt{6^2 - 0.0003^2}$ = 5.9999999%

$$X_T = \sqrt{Z_T^2 - R_T^2}$$ A.6

$X_T = \sqrt{8.398^2 - 0.0042^2}$ = 8.39799895 Ω

Therefore,

Z_T = 0.0042 + j 8.39799895 Ω

Step 4: Calculating transformer impedance correction factors

Step 4.1: Maximum short circuit currents

$$K_{Tmax} = 0.95\ x\ \frac{C_{max}}{1+0.6\ X_T}$$ A.7

$K_{Tmax} = 0.95\ x\ \frac{1.1}{1+0.6\ x0.059999999}$ = 1.0087

$$Z_{TKTmax} = Z_T\ x\ K_{Tmax}$$ A.8

$Z_{TKTmax} = Z_T \, x \, K_{Tmax}$ = (0.0042 + j 8.39799895 Ω) x 1.0087

Z_{TKTmax} = 0.00424 + j 8.471062 Ω

Step 4.2: Minimum short circuit currents

$K_{Tmin} = 0.95 \, x \, \frac{C_{min}}{1+0.6 \, X_T}$ A.9

$K_{Tmin} = 0.95 \, x \, \frac{1}{1+0.6 \, x 0.059999999}$ = 0.92

$Z_{TKTmin} = Z_T \, x \, K_{Tmin}$ = (0.0042 + j 8.39799895 Ω) x 0.92

Z_{TKTmin} = 0.0039 + j 7.726 Ω

A.1.2. Short circuit current calculation at bus 2

Step 1: Maximum short circuit currents

First, add the impedances Z_{B1max} and Z_{TKTmax} and then convert them from rectangular form to polar form.

$Z_{B2max} = Z_{B1} + Z_{TKTmax}$

Whereby,

Z_{B2Pmax} Total impedance in rectangular form at Bus 2

Z_{B2max} = (2.2975 + j 22.975 Ω) + (0.00424 + j 8.471062 Ω)

Z_{B2max} = 2.30174 + j 31.4461 Ω

Z_{B2Pmax} = 31.53∟85.81°

Step 2: Minimum short circuit currents

First, add the impedances Z_{B1min} and Z_{TKTmin} and then convert them from rectangular form to polar form.

$Z_{B2min} = Z_{B1min} + Z_{TKTmin}$

Whereby,

Z_{B2Pmin} Total impedance in polar form at Bus 2

Z_{B2min} = (2.612 + j 26.12 Ω) + (0.0039 + j 7.726 Ω)

Z_{B2min} = 2.6159 + j 33.846 Ω

Z_{B2Pmin} = $33.95 \angle 85.58^{\circ}$

Step 3: Short circuit calculation

$$I''_{kmax} = \frac{C_{max}\ x\ U_n}{\sqrt{3}\ x\ Z_{B2Pmax}}$$

$$I''_{kmax} = \frac{1.1\ x\ 144900}{\sqrt{3}\ x\ 31.53}$$

I''_{kmax} = 2918.6 A or 2.92 kA

$$I''_{kmin} = \frac{C_{min}\ x\ U_n}{\sqrt{3}\ x\ Z_{B2Pmin}}$$

$$I''_{kmin} = \frac{1\ x\ 144900}{\sqrt{3}\ x\ 33.95}$$

I''_{kmin} = 2464.15 A or 2.46 kA

Step 4: Line 1

The impedance information is given per kilometer for both positive sequence and negative sequence where positive sequence is the same as the negative sequence. The only calculation done is multiplying the given data by the length of the line, 18.56 km.

$R_1 = R_2 = 0.2376\ x\ 18.56\ km$ = 4.409856 Ω A.10

$X_1 = X_2 = 0.3465\ x\ 18.56\ km$ = 6.43104 Ω A.11

$Z_1 = Z_2$ = 4.409856 + j 6.43104 Ω

$R_0 = 0.2546\ x\ 18.56\ km$ = 4.4725376 Ω A.12

$X_0 = 0.3245\ x\ 18.56\ km$ = 6.02272 Ω A.13

Z_0 = 4.4725376 + j 6.02272 Ω

$R_L = \left[1 + \alpha\left(\theta_e - 20\mathring{}\right)\right] x\ R_{L20}$

Whereby,

R_{L20} The resistance at a temperature of 20° Celsius

α A factor which is equal to 0.004/K for aluminium, copper and aluminium alloy

θ_e The conductor temperature in Degrees Celsius at the end of short circuit

A.1.3. Short circuit current calculation at bus 3

Step 1: Maximum short circuit currents

First, add the impedances Z_1 and Z_{B2max} and then convert them from rectangular form to polar form.

$Z_{B3max} = Z_1 + Z_{B2max}$

Whereby,

Z_{B3max} Total impedance in rectangular form at Bus 3

Z_{B3max} = (4.409856 + j 6.43104 Ω) + (2.30174 + j 31.4461 Ω)

Z_{B3max} = 6.712 + j 37.877 Ω

Z_{B3Pmax} = 38.467∟79.95°

Step 2: Minimum short circuit currents

$Z_{B3min} = Z_1 + Z_{B2min}$

Whereby,

Z_{B3min} Total impedance in rectangular form at Bus 3

Z_{B3min} = (4.409856 + j 6.43104 Ω) + (2.6159 + j 33.846 Ω)

Z_{B3min} = 7.026 + j 40.277 Ω

Z_{B3Pmin} = 40.885∟80.10°

Step 3: Short circuit calculation

$I''_{kmax} = \frac{C_{max}\ x\ U_n}{\sqrt{3}\ x\ Z_{B3P}}$

$I''_{kmax} = \frac{1.1\ x\ 144900}{\sqrt{3}\ x\ 38.467}$

I''_{kmax} = 2392.28 A or 2.39 kA

$I''_{kmin} = \frac{C_{min}\ x\ U_n}{\sqrt{3}\ x\ Z_{B3P}}$

$I''_{kmin} = \frac{1\ x\ 144900}{\sqrt{3}\ x\ 40.885}$

I''_{kmin} = 2046.18 A or 2.05 kA

Step 4: Transformer 2

Transformer 2 High Voltage incomer is treated the same as the feeder incomer of transformer 1 and as such, calculation procedures followed are similar.

Step 4.1: Maximum short circuit current

$Z_{Bmax} = \frac{1.1\ x\ 144900}{\sqrt{3}\ x\ 2392} . \frac{33000^2}{144900^2}$ = 2.0005 Ω

$X_B = 0.995\ Z_B$ = 1.99052 Ω

$R_B = 0.1\ X_B$ = 0.199052 Ω

Therefore,

Z_{Bmax} = 0.199052 + j 1.99052 Ω

Step 4.2: Minimum short circuit current

$Z_{Bmin} = \frac{1\ x\ 144900}{\sqrt{3}\ x\ 2046} . \frac{33000^2}{144900^2}$ = 2.1262 Ω

$X_B = 0.995\ Z_{Bmin}$ = 2.1156 Ω

$R_B = 0.1\ X_B$ = 0.21156 Ω

Therefore,

Z_{Bmin} = 0.21156 + j 2.1156 Ω

$$Z_T = \frac{U_{kr}}{100\%} x \frac{U_{rT}^2}{S_{rT}}$$

$$Z_T = \frac{7.5}{100} x \frac{33000^2}{80000000} = 1.02094\ \Omega$$

$$R_T = P_{kr} x \frac{U_{rT}^2}{S_{rt}^2}$$

$$R_T = 5500\ x \frac{33000^2}{80000000^2} = 0.00094\ \Omega$$

$$U_{Rr} = \frac{P_{kr}}{S_{rt}} x\ 100\%$$

$$U_{Rr} = \frac{5500}{80000000} x\ 100\% = 0.006875\%$$

$$U_{xr} = \sqrt{U_{kr}^2 - U_{Rr}^2}$$

$$U_{xr} = \sqrt{7.5^2 - 0.006875^2} = 7.499997\%$$

$$X_T = \sqrt{Z_T^2 - R_T^2}$$

$$X_T = \sqrt{1.02094^2 - 0.00094^2} = 1.02094\ \Omega$$

Therefore,

Z_T = 0.00094 + j 1.02094 Ω

Step 5: Calculating transformer impedance correction factors

Step 5.1: Maximum short circuit current

$K_{Tmax} = 0.95\ x\ \frac{C_{max}}{1+0.6\ X_T}$

$K_{Tmax} = 0.95\ x\ \frac{1.1}{1+0.6\ x\ 0.07499997}$ = 1.0000017

$Z_{TKTmax} = Z_T\ x\ K_T$

$Z_{TKTmax} = Z_T\ x\ K_T$ = (0.00094 + j 1.02094 Ω) x 1.0000017

Z_{TKTmax} = 0.00094 + j 1.02094 Ω

Therefore,

$Z_{BTmax} = Z_{TKTmax} + Z_{Bmax}$

Z_{BTmax} = (0.00094 + j 1.02094 Ω) + (0.199052 + j 1.99052 Ω)

Z_{BTmax} = 0.199992 + j 3.0115 Ω

Whereby,

Z_{BTmax} Total impedance at the incomer connection point (HV side)

Step 5.2: Minimum short circuit current

$K_{Tmin} = 0.95\ x\ \frac{C_{min}}{1+0.6\ X_T}$

$K_{Tmin} = 0.95\ x\ \frac{1}{1+0.6\ x\ 0.07499997}$ = 0.91

$Z_{TKTmin} = Z_T \, x \, K_{Tmin}$

$Z_{TKTmin} = Z_T \, x \, K_{Tmin}$ = (0.00094 + j 1.02094 Ω) x 0.91

Z_{TKTmin} = 0.00086 + j 0.929 Ω

Therefore,

$Z_{BTmin} = Z_{Bmin} + Z_{Tmin}$

Z_{BTmin} = (0.00086 + j 0.929 Ω) + (0.21156 + j 2.1156 Ω)

Z_{BTmin} = 0.21246 + j 3.0446 Ω

Whereby,

Z_{BTmin} Total impedance at the incomer connection point (HV side)

A.1.4. Short circuit current calculation at bus 4

First convert Z_{BTmax} from rectangular form to polar form

Z_{BTmax} = 0.199992 + j 3.0115 Ω

Z_{BTPmax} = $3.02 \angle 86.20^{\circ}$

Z_{BTmin} = 0.21246 + j 3.0446 Ω

Z_{BTPmin} = $3.052 \angle 86.01^{\circ}$

Step 1: Short circuit current calculation

Step 1.1: Maximum short current

$$I''_{kmax} = \frac{C_{max}\, x\, U_n}{\sqrt{3}\, x\, Z_{BTPmax}}$$

$$I''_{kmax} = \frac{1.1\, x\, 33000}{\sqrt{3}\, x\, 3.02}$$

I''_{kmax} = 6939.67 A or 6.94 kA

Step 1.2: Minimum short circuit current

$$I''_{kmin} = \frac{C_{min}\, x\, U_n}{\sqrt{3}\, x\, Z_{BTPmin}}$$

$$I''_{kmin} = \frac{1\, x\, 33000}{\sqrt{3}\, x\, 3.052}$$

I''_{kmin} = 6242.65 A or 6.24 kA

A.2. Capacitor bank theory

A capacitor is made by an arrangement of two conductors separated by insulator (dielectric) and is defined as a device that stores electric charge. The two conductors have equal charge, but opposite polarity and a potential difference exist between these two conductors. When the capacitor discharged/uncharged the charge on either of the conductors is zero, which in turn causes a zero-potential difference across the conductors. Figure A.1 shows two parallel plates (conductors) making a capacitor.

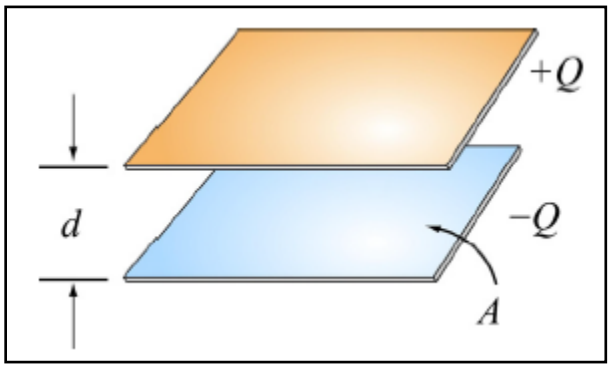


Figure A.1. Capacitor representation

Theory has proven that the amount of charge stored in a capacitor is linearly proportional to the potential difference between the plates. In the formula it can be represented as follows.

$$Q = C|\Delta V| \quad \text{A.14}$$

Whereby,

C	constant called capacitance
ΔV	potential difference

Capacitance is defined as a measure of the electric charge storing capacity for a given potential difference and the SI unit is Farad (f). Farad is given as follows:

1 F = 1 coulomb/volt = 1 C/V A.15

A capacitor is graphically represented with following symbols as shown in Figure A.2.

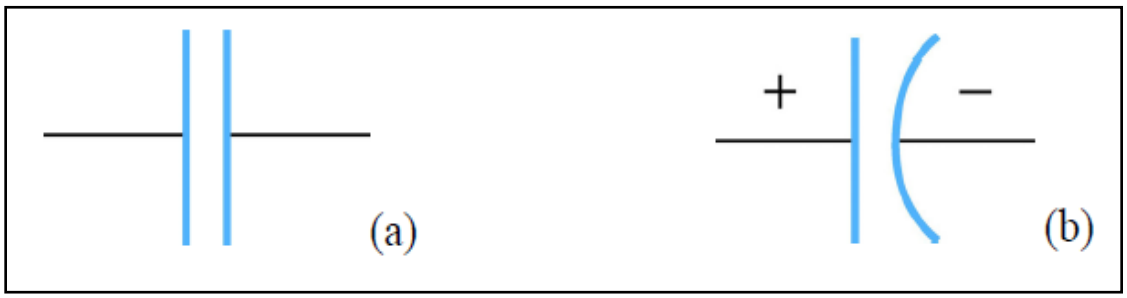


Figure A.2. Capacitor symbols

Using Figure A.1 capacitance can be calculated as follows,

$$C = \frac{\in_r x \in_0 x\, A}{d} \quad \text{A.16}$$

Whereby,

C	capacitance
$\in_r$	relative permittivity of the dielectric between the plates
$\in_0$	permittivity of free space $= 8.854x10^{-12}$ F/m
A	Area
d	distance between the plates (m)

Rawlins, (2000) provides reactance is calculation formula as shown next.

$$X_c = \frac{1}{2\,\pi\, f\, C} \quad \text{A.17}$$

Whereby,

X_c	Capacitive reactance
C	Capacitance
f	Frequency

The known electrical power system power formulae are shown next,

$$S = P + jQ = I^2 Z = \frac{V^2}{Z} \quad \text{A.18}$$

$$|S| = \sqrt{P^2 + Q^2} \quad \text{A.19}$$

Whereby,

S	Apparent power
P	Active power
Q	Reactive power

The assumption that the capacitor is a perfect capacitor and has no resistance but only reactance, the following can be deduced.

$Z = X_c$

$S = Q$

From the above the formula A.18 can be represented as follows.

$$Q = \frac{V^2}{X_c} \qquad \text{A.20}$$

Rearranging A.20 to make X_c the subject of the formula, the following is deduced.

$$X_c = \frac{V^2}{Q} \qquad \text{A.21}$$

The above, A.21, is the formula used to calculate the impedances for the capacitor elements, units and the complete capacitor bank which are used in RelaySimTest software. The impedance values are shown next.

From the capacitor bank data provided, reactive power rating of the complete capacitor bank is 22 Mvar with a voltage rating of 149.65 kV. Using formula A.21 capacitor bank impedance is.

$$X_c = \frac{V^2}{Q} = \frac{149650^2}{22000000} = 1018\ \Omega$$

The capacitor unit reactive power rating is given as 612 kVar with voltage rating of 14.4 kV. Using formula A.21 capacitor unit impedance is,

$$X_c = \frac{V^2}{Q} = \frac{14400^2}{612000} = 338.8\ \Omega$$

The capacitor element reactive power rating is given as 76.5 kVar with voltage rating of 1.8 kV. Using formula A.21 capacitor element impedance is,

$$X_c = \frac{V^2}{Q} = \frac{1800^2}{76500} = 42.35\ \Omega$$

Manipulating formula A.17 to make C the subject of the formula, the following if found,

$$C = \frac{1}{2\,\pi\,f\,X_c} \qquad \text{A.22}$$

With A.22 formula the capacitance values can be determined, and the following were found for capacitor bank, capacitor unit and capacitor element,

For the capacitor,

$$C = \frac{1}{2\,\pi\,f\,X_c} = \frac{1}{2x3.14x50x1018} = 3.13\ uF$$

Capacitor unit,

$$C = \frac{1}{2\,\pi\,f\,X_c} = \frac{1}{2x3.14x50x338.8} = 9.4\ uF$$

For the capacitor element,

$$C = \frac{1}{2\,\pi\,f\,X_c} = \frac{1}{2x3.14x50x42.35} = 75.2\ uF$$

A.3. Voltage differential settings calculations

The appendix provides calculations process followed to determine voltage differential settings, element voltage loading based on the number of failed elements and the location on bank where these elements have failed. Figure A.3 is a schematic diagram of the capacitor bank under study and the rating details are provided. The reactive power rating is 22 MVar at 149.65 kV and has 12 units per phase rated at 612 kVar and 14.4 kV and each unit has 8 elements rated at 76.5 kVar and 1.8 kV each. The settings calculated will be used applied on SEL-487 V relay and the connections are as shown on the figure. The first part of testing is using only the OMICRON CMC test units and Test Universe to confirm the correct application of settings and the second part is system-based testing using OMICRON RelaySimTest whereby simulation of element failures as the calculations will be performed.

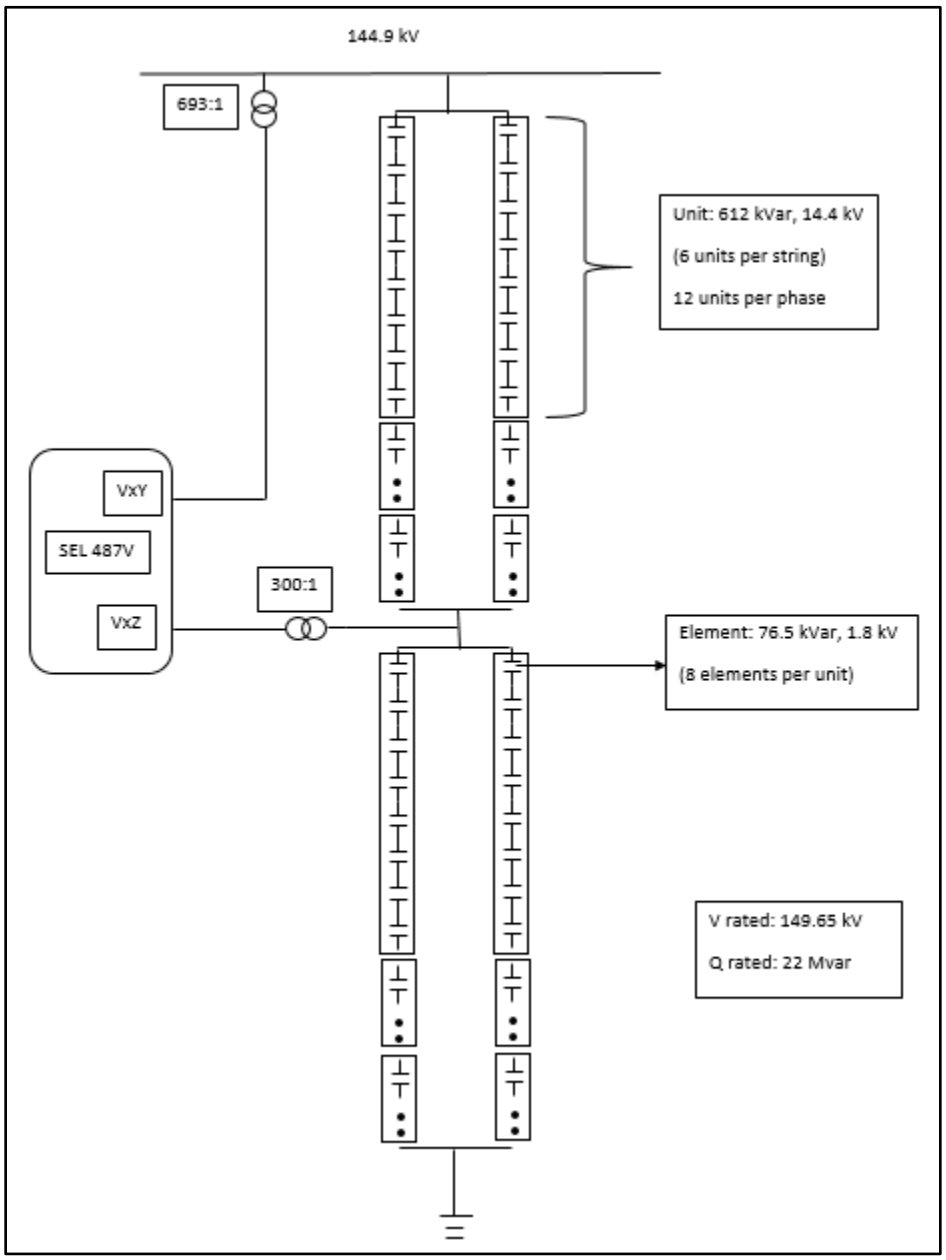


Figure A.3. Capacitor bank under study

$$Z_{eq} = \frac{V_{erat}^2}{S_{erat}} = 42.35\ \Omega \quad \text{A.23}$$

Whereby,

Z_{eq} Element equivalent impedance
V_{erat} Rated element voltage
S_{erat} Rated element power

The number of capacitor bank elements connected in series (one string) above and below the tap is the same, 24, as the capacitor bank is center tapped however, the total number of elements above and below is 48 including the parallel string. The impedances for will also be same so calculating for one will be sufficient.

$$Z_{TAeq} = \frac{(Z_{eq}x24).(Z_{eq}x24)}{(Z_{eq}x48)} = 508.2\ \Omega \quad \text{A.24}$$

Whereby,

Z_{TAeq} Total element equivalent impedance above the tap

Therefore,

$$Z_{Teq} = 2\ x\ Z_{TAeq} = 1016.4\ \Omega$$

As mentioned for each string, above or below the tap the number of elements is 24 and can be represented as follows,

$$C_{eRS} = 24$$
$$C_{eLS} = 24$$

Whereby,

C_{eRS} Number of capacitor elements on the right-hand side string

C_{eLS} Number of capacitor elements on the left-hand side string

Calculating the current through a single phase of the capacitor bank,

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 82.31\ A \quad \text{A.25}$$

Whereby,

V_{bus} Rated bus phase voltage

Therefore, the current flowing through each string is;

$$I_{str} = \frac{I_{cap}}{2} = 41.15\ A \quad \text{A.26}$$

Whereby,

I_{str} String current

$$V_e = Z_{eq} x\ I_{str} = \ 1742.7\ V \quad \text{A.27}$$

Whereby,

V_e Element voltage

The normal operation of the capacitor element is show next,

$$V_{eop} = \frac{V_e}{V_{erat}} = 96.82\ \%$$

Whereby,

V_{eop} Normal operational element voltage as a percentage

Calculating the voltage measured by the SEL 487V relay,

$$V_{bsec} = \frac{V_{bus}}{PTR_{bus}} = 120.72\ V \quad \text{A.28}$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 139.43\ V \quad \text{A.29}$$

Whereby,

V_{bsec} Secondary voltage of the bus VT

V_{tsec} Secondary voltage of the tap VT

The tap primary voltage is assumed to be half the bus voltage as the tap point is centered.

Applying formula 4.3, the k factor can be found,

$$k = \frac{V_{bsec}}{V_{tsec}} = 0.866$$

Therefore, for normal operating conditions of the capacitor bank with no failed element the differential voltage is zero and is verified.

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 139.43 = -0.03\ V$$

A.3.1 Two capacitor elements failed above the tap point on the same string

$$Z_{TAeq} = \frac{(Z_{eq}x24).(Z_{eq}x22)}{(Z_{eq}x46)} = 486.1\ \Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 84.14\ A$$

Applying a voltage divider rule to find differential voltage,

$$V_{tap} = V_{bus} x \frac{Z_{TBeq}}{Z_{TAeq} + Z_{TBeq}} = 42\ 758.75\ V$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 142.53\ V$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 142.53 = -2.71\ V$$

Therefore, the current flowing through right string with two failed elements is found using a current divider rule,

$$I_{strR} = I_{cap} x \frac{Z_{strL}}{Z_{strL} + Z_{strR}} = 43.9\ A$$

$$V_e = Z_{eq} x\ I_{strR} = \ 1859.17\ V$$

Therefore, the capacitor bank elements on the string with two failed elements

$$V_{eop} = \frac{V_e}{V_{erat}} = 103.29\ \%$$

A.3.2 Three capacitor elements failed above the tap point on the same string

$$Z_{TAeq} = \frac{(Z_{eq} x24).(Z_{eq} x21)}{(Z_{eq} x45)} = 474.32\ \Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 85.15\ A$$

Applying a voltage divider rule to find differential voltage,

$$V_{tap} = V_{bus} x \frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 43\ 271.42\ V$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 144.24\ V$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 144.24 = -4.19\ V$$

Therefore, the current flowing through right string with three failed elements is found using a current divider rule,

$$I_{strR} = I_{cap} x \frac{Z_{strL}}{Z_{strL}+Z_{strR}} = 45.41\ A$$

$$V_e = Z_{eq} x\ I_{strR} = \ 1923.11\ V$$

Therefore, the capacitor bank elements on the string with three failed elements

$$V_{eop} = \frac{V_e}{V_{erat}} = 106.84\ \%$$

A.3.3: Four capacitor elements failed above the tap point on the same string

$$Z_{TAeq} = \frac{(Z_{eq}x24).(Z_{eq}x20)}{(Z_{eq}x44)} = 462\ \Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 86.23\ A$$

Applying a voltage divider rule to find differential voltage,

$$V_{tap} = V_{bus} x \frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 43\ 836.82\ V$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 146.12\,V$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\,x\,146.12 = -5.82\,V$$

Therefore, the current flowing through right string with four failed elements is found using a current divider rule,

$$I_{strR} = I_{cap} x \frac{Z_{strL}}{Z_{strL} + Z_{strR}} = 47.03\,A$$
$$V_e = Z_{eq} x\, I_{strR} = \ 1991.72\,V$$

Therefore, the capacitor bank elements on the string with four failed elements

$$V_{eop} = \frac{V_e}{V_{erat}} = 110.65\ \%$$

A.3.4: Five capacitor elements failed above the tap point on the same string

$$Z_{TAeq} = \frac{(Z_{eq}x24).(Z_{eq}x19)}{(Z_{eq}x43)} = 449.11\,\Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 87.39\,A$$

Applying a voltage divider rule to find differential voltage,

$$V_{tap} = V_{bus} x \frac{Z_{TBeq}}{Z_{TAeq} + Z_{TBeq}} = 44\ 410.93\,V$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 148.04\,V$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\,x\,148.04 = -7.48\,V$$

Therefore, the current flowing through right string with five failed elements is found using a current divider rule,

$$I_{strR} = I_{cap} x \frac{Z_{strL}}{Z_{strL}+Z_{strR}} = 48.78\ A$$

$$V_e = Z_{eq} x\ I_{strR} = \ 2065.83\ V$$

Therefore, the capacitor bank elements on the string with five failed elements

$$V_{eop} = \frac{V_e}{V_{erat}} = 114.77\ \%$$

The below the tap calculations are similar as the above the tap calculations, see the following process,

A.3.5: Two capacitor element failed below the tap point on the same string

$$Z_{TBeq} = \frac{(Z_{eq}x24).(Z_{eq}x22)}{(Z_{eq}x46)} = 486.1\ \Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 84.14\ A$$

Applying a voltage divider rule to find differential voltage,

$$V_{tap} = V_{bus} x \frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 40\ 899.31\ V$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 136.33\ V$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 136.33 = 2.66\ V$$

Therefore, the current flowing through right string with two failed elements is found using a current divider rule,

$$I_{strR} = I_{cap} x \frac{Z_{strL}}{Z_{strL}+Z_{strR}} = 43.9\ A$$

$$V_e = Z_{eq} x\ I_{strR} = \ 1859.17\ V$$

Therefore, the capacitor bank elements on the string with two failed elements

$$V_{eop} = \frac{V_e}{V_{erat}} = 103.12\ \%$$

A.3.6: Three capacitor elements failed below the tap point on the same string

$$Z_{TAeq} = \frac{(Z_{eq}x24).(Z_{eq}x21)}{(Z_{eq}x45)} = 474.32\ \Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 85.15\ A$$

Applying a voltage divider rule to find differential voltage,

$$V_{tap} = V_{bus} x \frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 40\ 386.65\ V$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 134.62\ V$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 134.62 = 4.14\ V$$

Therefore, the current flowing through right string with three failed elements is found using a current divider rule,

$$I_{strR} = I_{cap} x \frac{Z_{strL}}{Z_{strL}+Z_{strR}} = 45.41\ A$$

$$V_e = Z_{eq} x\ I_{strR} = \ 1923.11\ V$$

Therefore, the capacitor bank elements on the string with three failed elements

$$V_{eop} = \frac{V_e}{V_{erat}} = 106.84\ \%$$

A.3.7: Four capacitor elements failed below the tap point on the same string

$$Z_{TAeq} = \frac{(Z_{eq}x24).(Z_{eq}x20)}{(Z_{eq}x44)} = 462\ \Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 86.23\ A$$

Applying a voltage divider rule to find differential voltage,

$$V_{tap} = V_{bus}x\frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 39\ 837.17\ V$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 132.79\ V$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 132.79 = 5.72\ V$$

Therefore, the current flowing through right string with four failed elements is found using a current divider rule,

$$I_{strR} = I_{cap}x\frac{Z_{strL}}{Z_{strL}+Z_{strR}} = 47.03\ A$$

$$V_e = Z_{eq}x\ I_{strR} = \ 1991.72\ V$$

Therefore, the capacitor bank elements on the string with four failed elements

$$V_{eop} = \frac{V_e}{V_{erat}} = 110.65\ \%$$

A.3.8: Five capacitor elements failed below the tap point on the same string

$$Z_{TAeq} = \frac{(Z_{eq}x24).(Z_{eq}x19)}{(Z_{eq}x43)} = 449.11\ \Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 87.39\ A$$

Applying a voltage divider rule to find differential voltage,

$$V_{tap} = V_{bus}x\frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 39\ 247.13\ V$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 130.82\ V$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 130.82 = 7.46\ V$$

Therefore, the current flowing through right string with five failed elements is found using a current divider rule,

$$I_{strR} = I_{cap}x\frac{Z_{strL}}{Z_{strL}+Z_{strR}} = 48.78\ A$$

$$V_e = Z_{eq}x\ I_{strR} = \ 2065.83\ V$$

Therefore, the capacitor bank elements on the string with five failed elements

$$V_{eop} = \frac{V_e}{V_{erat}} = 114.77\ \%$$

A.3.9: Four capacitor elements failed above the tap point on the parallel string

$$Z_{TAeq} = \frac{(Z_{eq}x22).(Z_{eq}x22)}{(Z_{eq}x44)} = 465.85\ \Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 85.89\ A$$

Applying a voltage divider rule to find differential voltage,

$V_{tap} = V_{bus} x \frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 43\,647.78\,V$

$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 145.49\,V$

$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\,x\,145.49 = -5.27\,V$

Therefore, the current flowing through right string with four failed elements is found using a current divider rule,

$I_{strR} = \frac{I_{cap}}{2} = 42.95\,A$

$V_e = Z_{eq} x\, I_{strR} = \ 1818.93\,V$

Therefore, the capacitor bank elements on the string with four failed elements

$V_{eop} = \frac{V_e}{V_{erat}} = 101.05\ \%$

A.3.10: Six capacitor elements failed above the tap point on the parallel string

$Z_{TAeq} = \frac{(Z_{eq}x21).(Z_{eq}x21)}{(Z_{eq}x42)} = 444.68\,\Omega$

$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 87.79\,A$

Applying a voltage divider rule to find differential voltage,

$V_{tap} = V_{bus} x \frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 44\,617.39\,V$

$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 148.72\,V$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 148.72 = -8.07\ V$$

Therefore, the current flowing through right string with six failed elements is found using a current divider rule,

$$I_{strR} = \frac{I_{cap}}{2} = 43.9\ A$$

$$V_e = Z_{eq} x\ I_{strR} = \ 1859.16\ V$$

Therefore, the capacitor bank elements on the string with six failed elements

$$V_{eop} = \frac{V_e}{V_{erat}} = 103.29\ \%$$

A.3.11: Eight capacitor elements failed above the tap point on the parallel string

$$Z_{TAeq} = \frac{(Z_{eq}x20).(Z_{eq}x20)}{(Z_{eq}x40)} = 423.5\ \Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 89.79\ A$$

Applying a voltage divider rule to find differential voltage,

$$V_{tap} = V_{bus} x \frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 45\ 631.67\ V$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 152.11\ V$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 152.11 = -11.01\ V$$

Therefore, the current flowing through right string with eight failed elements is found using a current divider rule,

$$I_{strR} = \frac{I_{cap}}{2} = 44.9\ A$$

$$V_e = Z_{eq}x\ I_{strR} = \ 1901.52\ V$$

Therefore, the capacitor bank elements on the string with eight failed elements

$$V_{eop} = \frac{V_e}{V_{erat}} = 105.64\ \%$$

A.3.12: Ten capacitor elements failed above the tap point on the parallel string

$$Z_{TAeq} = \frac{(Z_{eq}x19).(Z_{eq}x19)}{(Z_{eq}x38)} = 402.33\ \Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 91.88\ A$$

Applying a voltage divider rule to find differential voltage,

$$V_{tap} = V_{bus}x\frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 46\ 692.61\ V$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 155.6\ V$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 155.6 = -14.03\ V$$

Therefore, the current flowing through right string with ten failed elements is found using a current divider rule,

$$I_{strR} = \frac{I_{cap}}{2} = 45.94\ A$$

$V_e = Z_{eq} x\ I_{strR} = \ 1945.56\ V$

Therefore, the capacitor bank elements on the string with ten failed elements

$V_{eop} = \frac{V_e}{V_{erat}} = 108.09\%$

A.3.13: Twelve capacitor elements failed above the tap point on the parallel string

$Z_{TAeq} = \frac{(Z_{eq}x18).(Z_{eq}x18)}{(Z_{eq}x36)} = 381.15\ \Omega$

$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 94.07\ A$

Applying a voltage divider rule to find differential voltage,

$V_{tap} = V_{bus} x \frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 47\ 804.6\ V$

$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 159.35\ V$

$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 159.35 = -17.28\ V$

Therefore, the current flowing through right string with twelve failed elements is found using a current divider rule,

$I_{strR} = \frac{I_{cap}}{2} = 47.04\ A$

$V_e = Z_{eq} x\ I_{strR} = \ 1992.14\ V$

Therefore, the capacitor bank elements on the string with twelve failed elements

$V_{eop} = \frac{V_e}{V_{erat}} = 110.67\ \%$

The below the tap calculations are similar as the above the tap calculations as shown in the following process,

A.3.14: Four capacitor elements failed below the tap point on the parallel string

$$Z_{TAeq} = \frac{(Z_{eq}x22).(Z_{eq}x22)}{(Z_{eq}x44)} = 465.85\ \Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 85.89\ A$$

Applying a voltage divider rule to find differential voltage,

$$V_{tap} = V_{bus}x\frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 40\ 010.37\ V$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 133.37\ V$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 133.37 = 5.22\ V$$

Therefore, the current flowing through right string with four failed elements is found using a current divider rule,

$$I_{strR} = \frac{I_{cap}}{2} = 42.95\ A$$

$$V_e = Z_{eq}x\ I_{strR} = \ 1818.93\ V$$

Therefore, the capacitor bank elements on the string with four failed elements

$$V_{eop} = \frac{V_e}{V_{erat}} = 101.05\ \%$$

A.3.15: Six capacitor elements failed below the tap point on the parallel string

$$Z_{TAeq} = \frac{(Z_{eq}x21).(Z_{eq}x21)}{(Z_{eq}x42)} = 444.68\,\Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 87.79\,A$$

Applying a voltage divider rule to find differential voltage,

$$V_{tap} = V_{bus}x\frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 39\,040.66\,V$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 130.14\,V$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\,x\,130.14 = 8.02\,V$$

Therefore, the current flowing through right string with six failed elements is found using a current divider rule,

$$I_{strR} = \frac{I_{cap}}{2} = 43.9\,A$$
$$V_e = Z_{eq}x\,I_{strR} = \ 1859.17\,V$$

Therefore, the capacitor bank elements on the string with six failed elements

$$V_{eop} = \frac{V_e}{V_{erat}} = 103.29\ \%$$

A.3.16: Eight capacitor elements failed below the tap point on the parallel string

$$Z_{TAeq} = \frac{(Z_{eq}x20).(Z_{eq}x20)}{(Z_{eq}x40)} = 423.5\,\Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 89.79\,A$$

Applying a voltage divider rule to find differential voltage,

$$V_{tap} = V_{bus} x \frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 38\,026.39\ V$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 126.75\ V$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 126.75 = 10.95\ V$$

Therefore, the current flowing through right string with eight failed elements is found using a current divider rule,

$$I_{strR} = \frac{I_{cap}}{2} = 44.9\ A$$

$$V_e = Z_{eq} x\ I_{strR} = \ 1901.52\ V$$

Therefore, the capacitor bank elements on the string with eight failed elements

$$V_{eop} = \frac{V_e}{V_{erat}} = 105.64\ \%$$

A.3.17: Ten capacitor elements failed below the tap point on the parallel string

$$Z_{TAeq} = \frac{(Z_{eq}x19).(Z_{eq}x19)}{(Z_{eq}x38)} = 402.33\ \Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 91.88\ A$$

Applying a voltage divider rule to find differential voltage,

$$V_{tap} = V_{bus} x \frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 36\,965.44\ V$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 123.22\ V$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 123.22 = 14.01\ V$$

Therefore, the current flowing through right string with ten failed elements is found using a current divider rule,

$$I_{strR} = \frac{I_{cap}}{2} = 45.94\ A$$

$$V_e = Z_{eq} x\ I_{strR} = \ 1945.56\ V$$

Therefore, the capacitor bank elements on the string with ten failed elements

$$V_{eop} = \frac{V_e}{V_{erat}} = 108.09\ \%$$

A.3.18: Twelve capacitor elements failed below the tap point on the parallel string

$$Z_{TAeq} = \frac{(Z_{eq}x18).(Z_{eq}x18)}{(Z_{eq}x36)} = 381.15\ \Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 94.07\ A$$

Applying a voltage divider rule to find differential voltage,

$$V_{tap} = V_{bus} x \frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 35\ 853.45\ V$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 119.51\ V$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 119.51 = 17.22\ V$$

Therefore, the current flowing through right string with twelve failed elements is found using a current divider rule,

$$I_{strR} = \frac{I_{cap}}{2} = 47.04\ A$$

$$V_e = Z_{eq}x\ I_{strR} = \ 1992.14\ V$$

Therefore, the capacitor bank elements on the string with twelve failed elements

$$V_{eop} = \frac{V_e}{V_{erat}} = 110.67\ \%$$

A.3.19: Two capacitor elements failed above and below the tap point on the left string

$$Z_{TAeq} = \frac{(Z_{eq}x24).(Z_{eq}x22)}{(Z_{eq}x46)} = 486.1\ \Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 86.05\ A$$

Applying a voltage divider rule to find differential voltage,

$$V_{tap} = V_{bus}x\frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 41\ 829.03\ V$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 139.43\ V$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 139.43 = -0.03\ V$$

Therefore, the current flowing through right string with two failed elements is found using a current divider rule,

$$I_{strR} = \frac{I_{cap}}{2} = 43.03\ A$$

$$V_e = Z_{eq}x\ I_{strR} = \ 1822.32\ V$$

Therefore, the capacitor bank elements on the string with two failed elements

$$V_{eop} = \frac{V_e}{V_{erat}} = 101.24\ \%$$

A.3.20: Three capacitor elements failed above and below the tap point on the left string

$$Z_{TAeq} = \frac{(Z_{eq}x24).(Z_{eq}x21)}{(Z_{eq}x45)} = 474.32\ \Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 88.19\ A$$

Applying a voltage divider rule to find differential voltage,

$$V_{tap} = V_{bus}x\frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 41\,829.03\ V$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 139.43\ V$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 139.43 = -0.03\ V$$

Therefore, the current flowing through right string with three failed elements is found using a current divider rule,

$$I_{strR} = \frac{I_{cap}}{2} = 44.1\ A$$

$$V_e = Z_{eq}x\ I_{strR} = \ 1867.64\ V$$

Therefore, the capacitor bank elements on the string with three failed elements

$$V_{eop} = \frac{V_e}{V_{erat}} = 103.76\ \%$$

A.3.21: Four capacitor elements failed above and below the tap point on the left string

$$Z_{TAeq} = \frac{(Z_{eq}x24).(Z_{eq}x20)}{(Z_{eq}x44)} = 462\ \Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 90.54\ A$$

Applying a voltage divider rule to find differential voltage,

$$V_{tap} = V_{bus}x\frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 41\,829.03\ V$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 139.03\ V$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 139.43 = -0.03\ V$$

Therefore, the current flowing through right string with four failed elements is found using a current divider rule,

$$I_{strR} = I_{cap}x\frac{Z_{strL}}{Z_{strL}+Z_{strR}} = 45.27\ A$$

$$V_e = Z_{eq}x\ I_{strR} = \ 1917.18\ V$$

Therefore, the capacitor bank elements on the string with four failed elements

$$V_{eop} = \frac{V_e}{V_{erat}} = 106.51\ \%$$

A.3.22: Five capacitor elements failed above and below the tap point on the left string

$$Z_{TAeq} = \frac{(Z_{eq}x24).(Z_{eq}x19)}{(Z_{eq}x43)} = 449.11\ \Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 93.14\ A$$

Applying a voltage divider rule to find differential voltage,

$$V_{tap} = V_{bus}x\frac{Z_{TBeq}}{Z_{TAeq}+Z_{TBeq}} = 41\,829.03\ V$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 139.43\ V$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 139.43 = -0.03\ V$$

Therefore, the current flowing through right string with five failed elements is found using a current divider rule,

$$I_{strR} = \frac{I_{cap}}{2} = 46.57\ A$$

$$V_e = Z_{eq}x\ I_{strR} = \ 1972.24\ V$$

Therefore, the capacitor bank elements on the string with five failed elements

$$V_{eop} = \frac{V_e}{V_{erat}} = 109.57\ \%$$

A.3.23: Six capacitor elements failed above and below the tap point on the left string

$$Z_{TAeq} = \frac{(Z_{eq}x24).(Z_{eq}x18)}{(Z_{eq}x42)} = 435.6\ \Omega$$

$$I_{cap} = \frac{V_{bus}}{Z_{Teq}} = 96.03\ A$$

Applying a voltage divider rule to find differential voltage,

$$V_{tap} = V_{bus} x \frac{Z_{TBeq}}{Z_{TAeq} + Z_{TBeq}} = 41\ 829.03\ V$$

$$V_{tsec} = \frac{V_{tap}}{PTR_{tap}} = 139.43\ V$$

$$dV = V_{bus} - kV_{tap} = 120.72 - 0.866\ x\ 139.43 = -0.03\ V$$

Therefore, the current flowing through right string with six failed elements is found using a current divider rule,

$$I_{strR} = \frac{I_{cap}}{2} = 48.02\ A$$

$$V_e = Z_{eq} x\ I_{strR} = \ 2033.65\ V$$

Therefore, the capacitor bank elements on the string with six failed elements

$$V_{eop} = \frac{V_e}{V_{erat}} = 112.98\ \%$$

A.4 RealySimTest report

A.4.1 Report overview

The report overview provides information such as date creation or last modified configuration, the status of the execution whether the test cases passed or failed based on predetermined measures.

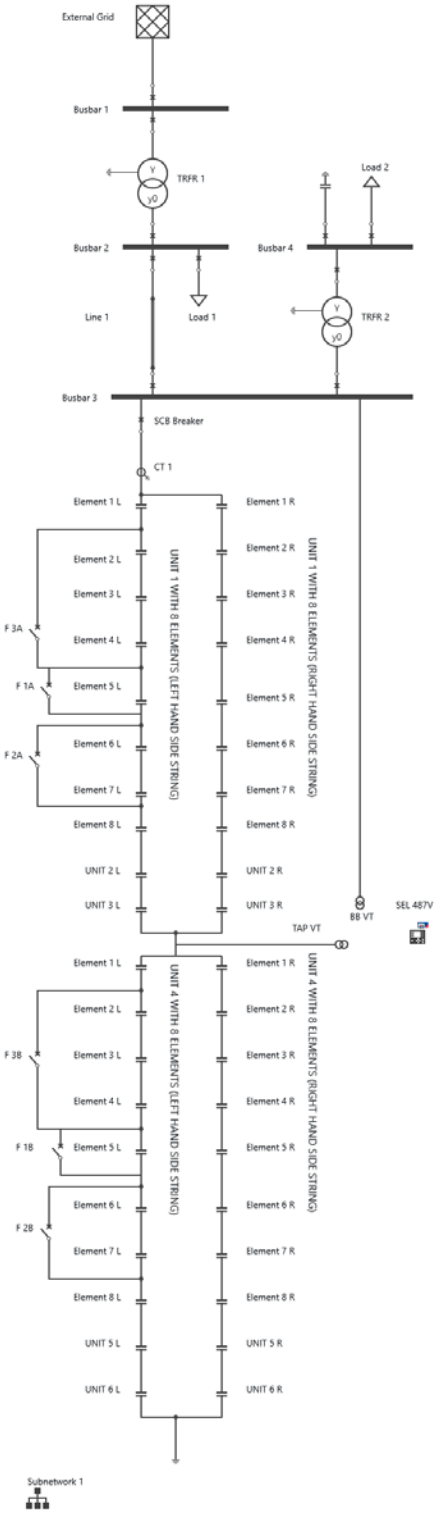
Creation date / last modified:	**11/2/2021 7:58:06 PM**
Created by:	M Mquqwana
Execution date:	11/5/2021 7:15:02 PM
Executed by:	ax12497

Executed:	10 of 10
Issues:	0
Passed:	10
Failed:	0
Overall assessment:	Passed

Comment:	The project is designated for testing Capacitor Bank Voltage Differential Protection

A.4.2 Power system under test

The system under test as presented in chapter four, section 4.3 and chapter five, section 5.6 is shown.



A.4.3 System and equipment settings

System information such as frequency, protection relay, current and voltage transformer configurations as well as breaker trip and close times are shown.

Nominal frequency:	50.00 Hz
Device type:	487V

CT 1	**100.00 A : 1.0000 A**
Type	Three-phase
BB VT	**144.90 kV : 209.10 V**
Type	Three-phase
TAP VT	**72.450 kV : 241.50 V**
Type	Three-phase
SCB Breaker	
Breaker type:	Three-pole
Trip time	20.000 ms
Close time	50.0

A.4.4 CMC test set configurations

The CMC configuration shows the two units used in the project and how they have been configured including their serial numbers, voltage and current measurements configurations.

CMC 356

Serial number:	DJ495G
Voltages:	4x300 V
Currents:	6x32 A, 25 Vrms

CMC 256plus

Serial number:	ME559L
Voltages:	4x300 V
Currents:	6x12.5 A, 10 Vrms

A.4.5 Main protection tests

Main protection test procedure is developed to ensure testing of different fault conditions that may occur internally to bank. A failure of few capacitor elements with no action taken to failure of more capacitor elements whereby high set threshold is triggered are simulated, for both above and below tap positions. The voltage differential functions is able to identify which phase of the bank has the failure and whether above or below the tap and these are discussed next.

A.4.5.1 No alarm test above tap

A failure of two capacitor elements below the tap is simulated and no alarm or trip occurred as the minimum threshold is not exceeded. The failure of capacitor elements is simulated to occur after 500 milliseconds from the start of simulation and the simulation ran for 3000 milliseconds.

Test case status: **Passed**

Description:	Simulation of 2 capacitor element failures above the tap showing that it has a very small impact on the system, as such no alarm is sent to the SCADA system nor a breaker is tripping

No.	Status	Time stamp	Comment
1	**Passed**	**11/5/2021 7:12:59 PM**	

Trip

+∞

Absolute time	Name	Event type
1.0 ms	SCB Breaker	Close
501.0 ms	F 2B	Close
3000.0 ms	Test step	End

A.4.5.2 Alarm test above tap

A failure of three capacitor elements above the tap is simulated and it resulted in an alarm being issued 2000 milliseconds. The failure of capacitor elements is simulated to occur after 500 milliseconds from the start of simulation and the simulation ran for 3000 milliseconds.

Test case status:	**Passed**
Description:	Simulation of 3 capacitor element failures above the tap showing that it has small impact on the system, as such and alarm is sent to the SCADA system but no breaker trip

No.	Status	Time stamp	Comment
1	**Passed**	**11/5/2021 7:13:13 PM**	

Trip

+∞

Absolute time	Name	Event type
1.0 ms	SCB Breaker	Close
501.0 ms	F 3B	Close
3000.0 ms	Test step	End

A.4.5.3 Trip test above tap

A failure of four capacitor elements above the tap is simulated and it resulted in breaker operating at about 542 milliseconds. The failure of capacitor elements is simulated to occur after 500 milliseconds from the start of simulation.

Test case status: **Passed**

Description: Simulation of 4 capacitor element failures above the tap showing that it has an impact on the system and as such the breaker trips in 120 milliseconds

No.	Status	Time stamp	Comment
1	**Passed**	**11/5/2021 7:13:26 PM**	

Trip
542.7 ms

Absolute time	Name	Event type
1.0 ms	SCB Breaker	Close
501.0 ms	F 3B	Close
501.0 ms	F 1B	Close
1150.0 ms	Test step	End

A.4.5.4 High set test above tap

A failure of five capacitor elements above the tap is simulated and it resulted in breaker operating at about 162 milliseconds. The failure of capacitor elements is simulated to occur after 500 milliseconds from the start of simulation.

Test case status: **Passed**

Description: Simulation of 5 capacitor element failures above the tap showing that it has a big impact on the system and as such the breaker trips in 60 milliseconds

No.	Status	Time stamp	Comment
1	**Passed**	**11/5/2021 7:13:37 PM**	

Trip
162.7 ms

Absolute time	**Name**	**Event type**
1.0 ms	SCB Breaker	Close
501.0 ms	F 3B	Close
501.0 ms	F 2B	Close
800.0 ms	Test step	End

A.4.5.5 No alarm test below tap

A failure of two capacitor elements below the tap is simulated and no alarm or trip occurred as the minimum threshold is not exceeded. The failure of capacitor elements is simulated to occur after 500 milliseconds from the start of simulation and the simulation ran for 3000 milliseconds.

Test case status: **Passed**

Description: Simulation of 2 capacitor element failures below the tap showing that it has a very small impact on the system, as such no alarm is sent to the SCADA system nor a breaker is tripping

No.	Status	Time stamp	Comment
1	**Passed**	**11/5/2021 7:13:50 PM**	

Trip
+∞

Absolute time	Name	Event type
1.0 ms	SCB Breaker	Close
501.0 ms	F 2A	Close
3000.0 ms	Test step	End

A.4.5.6 alarm test below tap

A failure of three capacitor elements below the tap is simulated and it resulted in an alarm being issued 2000 milliseconds. The failure of capacitor elements is simulated to occur after 500 milliseconds from the start of simulation and the simulation ran for 3000 milliseconds.

Test case status:	**Passed**
Description:	Simulation of 3 capacitor element failures below the tap showing that it has small impact on the system, as such and alarm is sent to the SCADA system but no breaker trip

No.	Status	Time stamp	Comment
1	**Passed**	**11/5/2021 7:14:04 PM**	

Trip
+∞

Absolute time	Name	Event type
1.0 ms	SCB Breaker	Close

Absolute time	Name	Event type
501.0 ms	F 3A	Close
3000.0 ms	Test step	End

A.4.5.7 Trip test below tap

A failure of four capacitor elements below the tap is simulated and it resulted in breaker operating at about 542 milliseconds. The failure of capacitor elements is simulated to occur after 500 milliseconds from the start of simulation.

Test case status:	**Passed**
Description:	Simulation of 4 capacitor element failures below the tap showing that it has an impact on the system and as such the breaker trips in 120 milliseconds

No.	Status	Time stamp	Comment
1	**Passed**	**11/5/2021 7:14:18 PM**	

Trip	Close	Start
542.7 ms	0.0 ms	0.0 ms

Absolute time	Name	Event type
1.0 ms	SCB Breaker	Close
501.0 ms	F 1A	Close
501.0 ms	F 3A	Close
1150.0 ms	Test step	End

A.4.5.8 High set test below tap

A failure of five capacitor elements below the tap is simulated and it resulted in breaker operating at about 162 milliseconds. The failure of capacitor elements is simulated to occur after 500 milliseconds from the start of simulation.

Test case status:	**Passed**
Description:	Simulation of 5 capacitor element failures below the tap showing that it has a big impact on the system and as such the breaker trips in 60 milliseconds

No.	Status	Time stamp	Comment
1	**Passed**	**11/5/2021 7:14:30 PM**	

Trip
162.7 ms

Absolute time	**Name**	**Event type**
1.0 ms	SCB Breaker	Close
501.0 ms	F 3A	Close
501.0 ms	F 2A	Close
800.0 ms	Test step	End

A.4.6 Backup protection tests

The test cases provide protection backup protection to main protection for faults that main protection does not pickup to ensure that the capacitor bank protected from any faults that may occur, internally or externally to the capacitor bank.

A.4.6.1 Overcurrent (overload) no tripping

The test case considers the balanced failure of capacitor elements above and below tap whereby five element failures above and five element failures below are simulated, and the protection settings response is monitored. No action is taken as the overcurrent threshold is not exceeded.

Test case status:	**Passed**

Description:	Simulation of an overload condition which shows a small impact on the system as the balanced capacitor element failures (above and below the tap) is not detected by normal differential protection. Five element failure above and below is simulated.

No.	Status	Time stamp	Comment
1	**Passed**	**11/5/2021 7:14:43 PM**	

Trip
+∞

Absolute time	**Name**	**Event type**
1.0 ms	SCB Breaker	Close
501.0 ms	F 3A	Close
501.0 ms	F 2A	Close
501.0 ms	F 3B	Close
501.0 ms	F 2B	Close
3000.0 ms	Test step	End

A.4.6.2 Overcurrent tests (overload)

The test case considers the balanced failure of capacitor elements above and below tap whereby six element failures above and six element failures below are simulated, and the protection settings response is monitored. The test results show that the breaker tripped just after 150 milliseconds.

Test case status:	**Passed**
Description:	Simulation of overcurrent fault (overload) with twelve capacitor element failures (six above and six below) which shows the impact on the system and that the breaker trips after 2 seconds

No.	Status	Time stamp	Comment
1	**Passed**	**11/5/2021 7:14:56 PM**	

Trip
150.1 ms

Absolute time	Name	Event type
1.0 ms	SCB Breaker	Close
501.0 ms	F 3A	Close
501.0 ms	F 1A	Close
501.0 ms	F 2A	Close
501.0 ms	F 3B	Close
501.0 ms	F 1B	Close
501.0 ms	F 2B	Close
800.0 ms	Test step	End

A.5 Relay command summary

Table A.1 shows some of the relay commands that are used to view configuration, reports, events and settings, configure the device, extract data, etc.

Table A.1. SEL 487 V relay commands

Command	Description
2ACCESS	Go to access level 2 (full control of relay)
ACCESS	Access level 1 (monitor)
CONTROL	Set, clear, or pulse internal Relay Word bits RB01 through RB32
DATE	View and set the relay date
EVENT	View and acknowledge filtered event reports
ETHERNET	Displays Ethernet port (Port 5) configuration and status
EXIT	Terminates a Telnet session
FILE	Transfer files between the relay and external software
GOOSE	Transfer files between the relay and external software
GROUP	View present group number; change the active group
HELP	List of commands available at the present access level
ID	Display identification codes
KSET	Calculates protection correction factors
MAC	Displays the Media Access Control address
MAP	View the organization of the relay database
METER	Displays power system quantities (voltages, currents, frequency, remote analogs, etc.) and internal relay operating quantities (math variables and analog quantities)
PASSOWRD	Control password protection for relay access levels
QUIT	Revert to Access Level 0 (exit relay control)
RTC	Display all data received on synchrophasor client channels
SER	Command to retrieve SER (Sequential Events Recorder) records
SET	Command to change relay settings
SHOW	Command to show relay settings
STATUS	Reports relay status information
SUMMARY	View event summary reports
TARGET	Display elements for a selected row in the Relay Word bit table
TIME	View and set the relay time clock
TRIGGER	Initiates data captures for high-resolution oscillography and event reports
VERSION	Displays the relay hardware and software configuration
VIEW	Examine data within the relay database

A.6 Protection settings extract using relay commands

The appendix shows group 1 relay settings configuration extracted using command, show.

=>SHOW

A.6.1 Group 1

Protection settings for group 1 for SEL 487 V relay are shown next.

A.6.1.1 Relay configuration

```
ECAPAP  := "GNDV"   E50    := "W"     E51    := N       E46    := OFF
E37    := N       E59    := 1       E27    := 1       E59T   := N
E81    := N       E81R   := N       EBFL   := OFF     EFOD   := N
E32    := N       EITCO  := N
```

A.6.1.2 Control enables

```
ETOD   := N       ECPBNKC := N
```

A.6.1.3 Current transformer data

```
CTRW   := 100     CTRX1  := 100     CTRX2  := 100     CTRX3  := 100
```

A.6.1.4 Potential transformer data

```
PTRY   := 693.0   PTRZ1  := 300.0   PTRZ2  := 300.0   PTRZ3  := 300.0
VNOMY  := 300     VNOMZ  := 300
```

A.6.1.5 Grounded bank differential (87) voltage elements

```
KAV    := 0.8660  KBV    := 0.8660  KCV    := 0.8660  87AP1P  := 3.90
87AP2P  := 3.90    87APPU  := 100.000  87APDO  := 0.000
```

87APEN := 1

87TP1P := 5.20 87TP2P := 5.20 87TPPU := 25.000 87TPDO := 0.000

87TPEN := 1

87HP1P := 6.50 87HP2P := 6.50 87HPPU := 6.000 87HPDO := 0.000

87HPEN := 1

87PF := N

A.6.1.6 Pole open detection

EPO := OFF

A.6.1.7 Terminal W

Overcurrent Elements Terminal W

E50W := "P" E67W := N

Terminal W Phase Overcurrent Element Level 1

50WP1P := 0.96

50WP1TC := 1

50WP1D := 6.00

Terminal W Phase Overcurrent Element Level 2

50WP2P := 1.08

50WP2TC := 1

50WP2D := 4.00

Terminal W Phase Overcurrent Element Level 3

50WP3P := 3.24

50WP3TC := 1

50WP3D := 3.00

Under Voltage (27) Element 1

27O1   := VPMINYF 27P1P1 := 188.18

27TC1   := 1

27P1D1 := 250.00   27P1P2 := 177.74

Over Voltage (59) Element 1

59O1   := VNMAXYF 59P1P1 := 230.00

59TC1   := 1

59P1D1 := 100.00   59P1P2 := 235.00

A.6.1.8 Trip logic

TRW   := 50WP1T OR 50WG1T OR 50WP2T OR 50WG2T OR 50WP3T OR 50WG3T OR \

87TPD OR 87HPD OR 271P1T OR 591P1T

ULTRW   := TRGTR

TDURD   := 2.000

ER   := 1

FAULT   := 1

A.6.1.9 Close logic

CLW := CCW AND PCT01Q

ULCLW := 52CLW

CFD := 4.000