The Design and Construction of the Front End Section of an L-band Receiver for Nano-Satellite Application

Etnard Louw

October 2015

The Design and Construction of the Front End Section of an L-band Receiver for Nano-Satellite application

by

Etnard Louw

Baccalaureus Technologiae in Electrical Engineering,

Cape Peninsula University of Technology

Submitted to the Department of Electrical Engineering

in partial fulfilment of the requirements for

Masters Technologiae in Electrical Engineering

at the

CAPE PENINSULA UNIVERSITY OF TECHNOLOGY

October 2015

Signature of Candidate……..……..

EW Louw

Candidate

Department of Electrical Engineering

October 2015

Certified by……..……

Mr. CV Whaits

Senior Lecturer

Thesis Supervisor

Declaration

I, Etnard Wynand Louw, declare that the contents of this dissertation/thesis represent my own unaided work, and that the dissertation/thesis has not previously been submitted for academic examination towards any qualification. Furthermore, it represents my own opinions and not necessarily those of the Cape Peninsula University of Technology.

Signed **Date**

Acknowledgements

I would like to thank:

My parents and my wife for allowing me the opportunity to study and for all their continued support, motivation and prayers throughout my studies.

My friends, co-students and lecturers in the F'SATI program at CPUT. Thanks for all your support and motivation during these past two years and for making this a fun and exciting learning experience, a great time to remember!

EBV Electrolink for supplying me with components for this project.

Mr. Whaits for all his input into this dissertation. Thanks for all his motivation and time spent helping me finish this dissertation.

And most importantly, The Lord Jesus Christ, for giving me the talent, passion for electronics and strength so that I could successfully complete this project.

Abstract

Optimum communication can only be achieved with a very sensitive front-end section in the receiver on a satellite because the transmitted signal from the ground station must travel hundreds of kilometres through the earth's atmosphere to a low earth orbit (LEO) satellite. This dissertation presents the design of the front end section of the receiver suitable for use in a nano-satellite. Specifically, various transistor technologies are evaluated by designing five low noise amplifiers to determine the optimum performing amplifier. The bandwidth of the front end section was controlled by designing coupled line microstrip filter.

For consistency, the same design technique was followed in the design of each LNA. Simulations were performed and the results were compared to the actual measured results of the constructed amplifiers to facilitate conclusions to be made.

Design specifications for the LNAs were obtained from the F'SATI Space CubeSat Programme Technical Specification document.

To control the bandwidth of the front end section, various types of band-pass filters were investigated, resulting in a coupled line band-pass filter being simulated and implemented. The simulated results were compared to the measured results of the constructed filter.

In the final stage of this dissertation, comparisons of each amplifier's performance were made, resulting in the final recommendation for this project.

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List of Abbreviations

ADCS	:	Attitude Determination and Control System
ADS	:	Advanced Design System
BJT	:	Bipolar Junction Transistor
BPF	:	Band-Pass Filter
DC	:	Direct Current
DR	:	Dynamic range
FET	:	Field-Effect Transistor
F'SATI	:	French South Institute of Technology
HBT	:	Hetero-junction Bipolar Transistor
HEMT	:	High Electron Mobility Transistor
IC	:	Integrated Circuit
IF	:	Intermediate Frequency
IMD	:	Intermodulation Distortion
LEO	:	Low Earth Orbit
LNA	:	Low Noise Amplifier
LPF	:	Low-Pass Filter
NF	:	Noise Figure
OIP_3	:	Output Third Order Intercept Point
PCB	:	Printed Circuit Board
PFD	:	Phase-Frequency Detector
PHEMT	:	Pseudomorphic High Electron Mobility Transistor
QPSK	:	Quadrature Phase Shift Keying
RF	:	Radio Frequency
SOLT	:	Short-Open-Load-Thru
IIP_3	:	Input Third Order Intercept Point
IP_3	:	Third Order Intercept Point
VNA	:	Vector Network Analyser

Chapter 1

Introduction

1.1 Introduction to a Cubesat

The interest in space and space science is a growing worldwide phenomenon resulting in an improvement in space grade technology. The space industry is growing substantially worldwide and more opportunities are available to become part of the space community. The Department of Science and Technology in South Africa has a ten-year innovation plan which includes the expansion and development of space science and technology (South Africa. Department Of Science and Technology, 2008:11). At the French South African Institute of Technology (F'SATI), a satellite systems engineering programme was developed, and the opportunity to put an experimental Cubesat into orbit presented itself and was seized.

The term "Cubesat" refers to a small satellite of not more than 10 kg, and must be built according to the Cubesat design standards and specifications (Puig-Suari &Twiggs, 2008:7). The Cubesat features all the subsystems of a commercial satellite with the advantage that they are low cost with a shorter development and integration time. The Cubesat being developed by F'SATI is an academic project, and students are given the chance to obtain experience in developing and testing a small 3U nano-satellite of about 10 cm × 10 cm × 30 cm, with a camera as the main payload. The images taken by the satellite of the surface of the earth must be transmitted to the ground station, and new commands and payload data must be transmitted or received by the satellite on every overpass. In order to receive these new commands, a reliable communications link between the satellite in orbit and the ground station must be established.

1.2 Background to the Research Problem

Optimum communication can only be achieved with a very sensitive front-end receiver on the satellite because the transmitted signal from the ground station must travel hundreds of kilometres through the earth's atmosphere to the low earth orbit (LEO) satellite. This process causes the transmitted signal to be severely attenuated and a significant amount of noise is added to the signal before it is received by the satellite (Ippolito, 2008:61). It is therefore understandable why the radio frequency (RF) front end forms the most important part of any radio receiver system as it must be able to receive extremely small signals and recover the original data from them (MacPherson & Whaits, 2002,(5):1).

The weakest signal detectable by a communications system is mainly determined by the noise level in the front end of the receiver. To minimise the noise level in the entire receiver, additional noise and losses in the front end must be minimal. The RF front end comprises all the components between the antenna and the digital baseband system. These components include all the filters, low noise amplifiers (LNAs), and down conversion mixers needed to process the modulated signals received at the antenna into signals suitable for use in the stages which follow the front end (Love & Ajluni, 2009:116). Figure 1.1 shows the basic block diagram of the front end in a receiver.

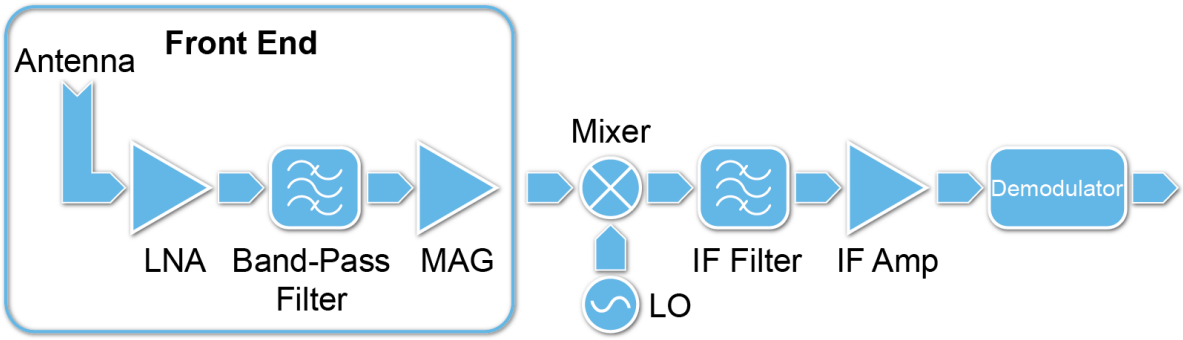


Figure 1.1: Block Diagram of a Typical Receiver System

1.3 Aims of the Research Project

- Investigate past and current trends in the design of low noise amplifiers and band-pass filters (BPF);
- Investigate different active device technologies, bias techniques and physical layouts of an LNA to determine the best option for the specific application;
- Investigate the different types, design techniques and layouts of RF filters in order determine the best option for the specific application;
- Perform computer simulations on all designed circuits using the Advanced Design System

(ADS) software package from Agilent Technologies;

- Physically build and construct the LNAs and BPF using common off the shelf (COTS) components on a printed circuit board (PCB);
- Couple the LNA and BPF circuits to produce the final RF front end which satisfies the design requirements.

1.4 Literature Review

The front end of the receiver must be able to detect and amplify the small signals that are received by the antenna between the frequencies of 1.26 GHz and 1.27 GHz. After amplification, any out-of-band signals must be filtered out before the signal is passed to the rest of the receiver and demodulator. There are different techniques for designing low noise amplifiers and band-pass filters. In the literature review some of the current and past trends for designing these components are discussed and motivation is given for the chosen circuits.

1.5 Significance of the Research

The research will firstly investigate the design and construction of an LNA that, once implemented, will add as little noise possible to overall system noise. Secondly, the design and construction of a band-pass filter with a very low amount of insertion loss in the specified passband. Both of these circuits must be optimised to use as little power as possible, as the power on-board the Cubesat is extremely limited. A few advantages include the following:

- Lower cost
- Performance above industry standards

The outcome of this project will be an RF front end section which adds as little noise as possible to the overall system noise figure with sufficient power gain, operating at optimum power efficiency while conforming to the requirements of the specified in the F'SATI Space CubeSat Programme Technical Specification.

1.6 Research Methodology

Existing technology used in nano-satellites will be carefully analysed to ensure the appropriate components are selected for the construction of the LNA. The correct models of the particular components selected will be sourced from the manufacturers so as to ensure accurate simulated results are achieved during the design process. The physical architecture and the space constraints of the actual

Cubesat will be analysed so as to ensure that the physical size of the design conforms to the constraints of the Cubesat.

The LNA and filter will then be designed and optimised using ADS software. Then the circuit will be constructed in the correct form factor so as to be easily integrated into the Cubesat structure.

1.6.1 Research Design Tools

ADS (Advanced Design System) simulation software will be used for the entire design process, including a planar electromagnetic method-of-moments simulator within ADS, will be used to optimise the final design to ensure that the required specifications are met.

1.6.2 Design Methodology

- Defining the specifications for the LNA and BPF by analysing the details of the *L*-band communications system in the Cubesat;
- Simulating each designed LNA of the *L*-band front end section individually and optimising its performance using ADS simulation software by Agilent Technologies;
- Simulate the designed LNAs and the selected PCB (printed circuit board) substrate using Agilent's Momentum EM simulator;
- Purchase the necessary components that will be required for the LNA and BPF;
- Construct and test final circuit and optimise the RF the front end section to meet the design specifications.

1.7 Expected Outcomes

- The design and construction of a fully functional front end section for the *L*-band receiver on a Cubesat;
- The LNA must add minimum noise to the overall system noise figure while providing moderate amplification of the received signal. Furthermore the BPF must have a minimum insertion loss and a passband between the frequencies of 1260 MHz and 1270 MHz so that it will not degrade the performance of the overall communication system;
- The RF front end must use as little power as possible to conform to the power budget of the Cubesat;

1.8 Delineation of the Research

In this project, an in depth study will be done on the first two stages of the front end section of a receiver, which are the LNA and the RF (radio frequency) filter, usually a BPF. These networks will be investigated by comparing different active device technologies, bias networks and physical layouts. This will ensure that a well informed decision can be made in choosing the optimal combination of these critical stages in order to maximise the overall performance of the entire receiver.

Although there are advantages in placing the BPF before the LNA in the receiver chain, it was decided to position this filter after the LNA in order to achieve the lowest possible noise figure. Placing the filter before the LNA would ensure minimal external interference from entering the receiver. However, it would compromise the lowest achievable noise figure as verified by Friis's Equation.

1.9 Chapter Overview

Chapter One: Introduction
Chapter Two: Review of Cubesat standards
Chapter Three: Small signal amplifier theory
Chapter Four: Filter theory
Chapter Five: Front-end design
Chapter Six: Band-pass filter design
Chapter Seven: Measurements and results
Chapter Eight: Conclusions and recommendations

Chapter 2

Cubesats and System Architecture

Chapter two presents the basic theory of the Cubesat standard and the satellite system bus. All of the subsystems comprising the satellite will be briefly described together with their basic operations and functions, with a more detailed overview on the important subsystems and processes. The entire communications subsystem will be outlined last before going into the detail of the *L*-band receiver, followed by an in-depth literature review in chapter three.

2.1 The Cubesat Standard

Developed in 1999 by Prof. Twiggs of Stanford University, with the intention of making it possible for students and learners to gain hands-on experience and knowledge of space and space level hardware, the Cubesat became the next generation of satellite technology. As previously mentioned, a 10 × 10 × 10 cm cube, roughly weighing 1 kg per unit, forms the most basic element and is commonly referred to as a 1U (Unit) Cubesat. Units can be stacked to form, for example a 3U Cubesat as shown in Figure 2.1 (Puig-Suari & Twiggs, 2008:7). The developed Cubesat specifications allow for institutions and universities across the world to develop Cubesats using COTS components and send them into orbit with any type of launch vehicle without compatibility issues (Puig-Suari, Turner & Twiggs, 2001:1).

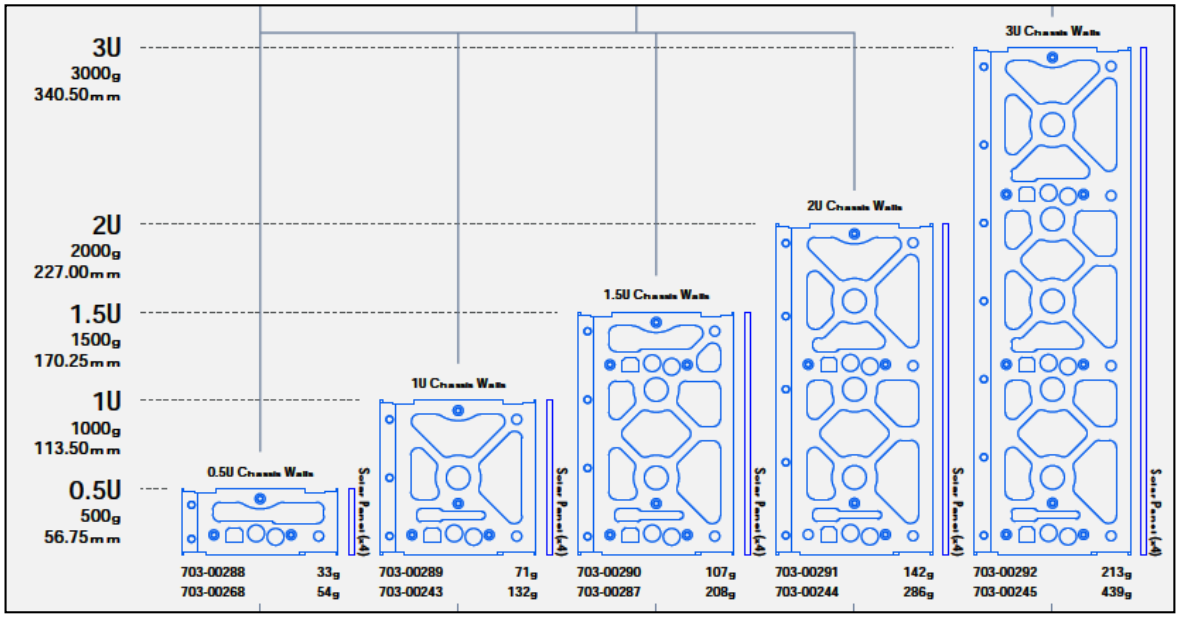


Figure 2.1: The Cubesat Structure

The Cubesat, like any other commercial satellite, irrespective of size and purpose, will exhibit the same basic design procedure and system bus. Within the structure of the satellite the following subsystems can be identified.

- On-board computer (OBC)
- Attitude determination control system (ADCS)
- Electrical power system (EPS)
- Payload
- Communications

2.2 On-board Computer

The OBC is a very complex piece of equipment and acts as the brain of the entire satellite. It is in control of every single part and function of the satellite and monitors and records all events and operations. The OBC is also responsible for controlling the different states in which the satellite will operate while orbiting the earth. The main functions of this subsystem are as follows:

- Data handling
- Computation for other subsystems
- System health logging
- Command execution
- Payload operation
- Error handling and diagnosis

- Communication with ground station

The processing and data handling is achieved with a single microcontroller, controlling all other subsystems.

2.3 Attitude Determination Control System

After ejection into space from the launch vehicle, the satellite will go into a tumble around its own centre of gravity relative to earth. The rotational movement caused by the ejection is unfavourable for the satellite operating at full power mode to establish communication with the ground station; that is, to receive commands and provide information about critical subsystems and the attitude of the satellite towards the earth. Most importantly, the satellite has to orientate itself toward the sun so that the solar panels are in an optimum position, where maximum solar energy is incident on them (Makovec, Turner, & Hall, 2002:180).

The attitude determination control system (ADCS) uses a number of actuators, flywheels and magnetic torque rods together with sun, horizon and star sensors that determine the attitude of the satellite towards the earth. The reason for this is to keep the satellite stable and pointing the narrow beam width antennas towards the ground station during communication or alternatively, towards points of interest that must be captured by the camera. The ADCS also counters some other factors, such as atmospheric drag, solar pressure and magnetic fields, which cause the satellite to deviate from its desired position, and which create disturbances that cause the satellite to wobble (Larson & Wertz, 1992:355).

2.4 Electrical Power System

Electrical energy is needed for the satellite to operate in outer space. The primary objective of the EPS is to conform to the power budget of the Cubesat and to provide electrical energy to all other subsystems, equipment and payload. Furthermore, the EPS is required to convert incident sunlight on the solar panels into electrical energy and to charge the batteries for use during peak power usage situations and eclipse periods when the earth is between the satellite and the sun. The EPS must also regulate the charging of the battery to prevent it from overcharging and lastly, provide the OBC with housekeeping data such as voltage levels, system status and temperature readings from subsystems and components.

2.5 Payload

The payload is the primary goal of the mission. Since this is an experimental and research based mission, the Cubesat will have several payloads, but the main payload will be the imager. The purpose of the imager is to capture images of the surface of the earth from specified locations and convert them into digital data that can be stored on-board and processed once it is transmitted to the ground station. The images will be taken with a commercial matrix sensor and pictures will be taken in the visible light spectrum.

2.6 Communications

To relay payload data, system information and commands between the satellite and ground station, some form of link must be created between them. The primary goal of the communications subsystem is to establish a reliable and stable link to convey information between the satellite and ground station.

To ensure optimum communication over the distance between the satellite in orbit around the earth and the ground station, a few prudent selections can be made. By choosing the correct modulation scheme for communication, the highest data rate can be achieved within the allocated channel bandwidth while simultaneously achieving the best error performance. Data can also be encrypted to prevent other parties from accessing the data (Ippolito, 2008:75).

The 2.4 GHz frequency band (*S*-band) is used for the high speed downlink to send the acquired images to the ground station. For the uplink, the range of frequencies between 1.26 GHz and 1.27 GHz (*L*-Band) will be used to send commands to the satellite. Figure 2.2 depicts the proposed communications systems for the Cubesat.

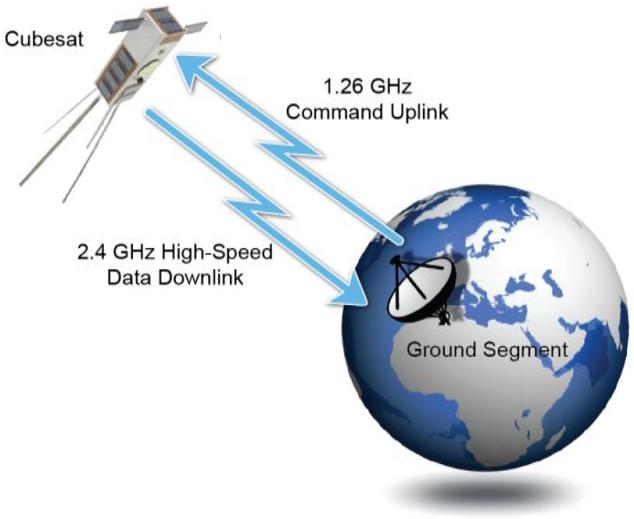


Figure 2.2: Communications Uplink and Downlink of Proposed Cubesat

The remainder of this dissertation will be dedicated to in depth research of the *L*-band on-board receiver, focussing specifically on the front end section. Figure 2.3 shows the letter band designations in the microwave frequency bands.

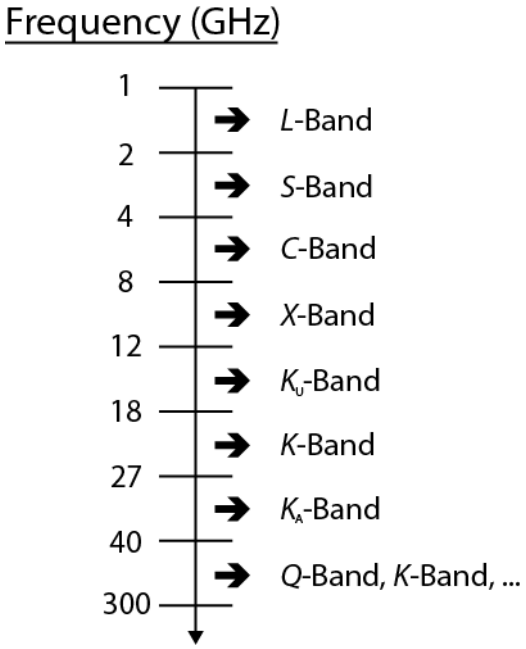


Figure 2.3: Letter Band Frequency Designations

Chapter 3

Small Signal Amplifier Theory

3.1 Introduction

To completely understand the reasoning behind certain design processes as well as decisions made in the design of amplifiers and filters, some basic principles and terms must first be clarified. In this chapter the theory and background of communications and the RF front end will be discussed in detail.

In modern communication systems the small signal amplifier (SSA) is without a doubt one of the most important and widely used circuits. These SSAs are designed to be either an LNA or an amplifier designed for maximum gain. That is, the LNA is designed specifically to provide moderate gain while adding as little noise as possible to the received signal. The maximum gain amplifier, for example an IF amplifier, is an SSA specifically designed to provide maximum gain. In many applications, trade-offs are involved because the techniques used to achieve a minimum noise figure are different from those used to achieve a maximum gain; that is, the two techniques are mutually exclusive. An LNA is the first stage in the front end of the receiver system and also plays a vital role in the overall system performance. It must provide enough amplification to the extremely weak signals received by the system as well as providing the following stages with a suitable signal level whilst generating and adding as little noise as possible to the signal.

3.2 *S*-parameters

The behavior of a two port network can be fully characterised by a set of four parameters. Any two port network can be defined as a network with a pair of terminals where a signal (voltage or current) enters or leaves the circuit. For lower frequencies of operation, admittance (*y*), impedance (*z*), hybrid (*h*) or chain (*ABCD*) parameters are suitable and used to describe a two port network. Unfortunately, when the frequency of operation is increased to the VHF, UHF and higher microwave frequency bands, the open-circuit and short-circuit techniques used to measure these parameters over a broader range of frequencies become more difficult and less accurate. For the *y*-, *h*-, *z*-, and *ABCD* parameters the resultant voltages and currents at the input and output ports are measured to characterise the network. According to Gonzalez (1997:24), at microwave frequencies another set of parameters, called scattering parameters (*S*-parameters) is used. Through the use of these *S*-parameters, a two-port network can fully be described as seen at its ports. Rather than using currents and voltages, *S*-parameters characterise a network by means of travelling waves and are physically measured using a Vector Network Analyser (VNA). The main reason for using *S*-parameters in small signal amplifier design is because semiconductor manufacturers now provide specialised information, which is not always contained in the data sheet, about the microwave frequency transistors for certain biasing conditions and for a range of operating frequencies. By using scattering parameters, every aspect of the amplifier, with the exception of noise, can be described. These include matching, gain, input and output voltage standing wave ratio (VSWR) and stability conditions (Dye & Granberg, 2001:219).

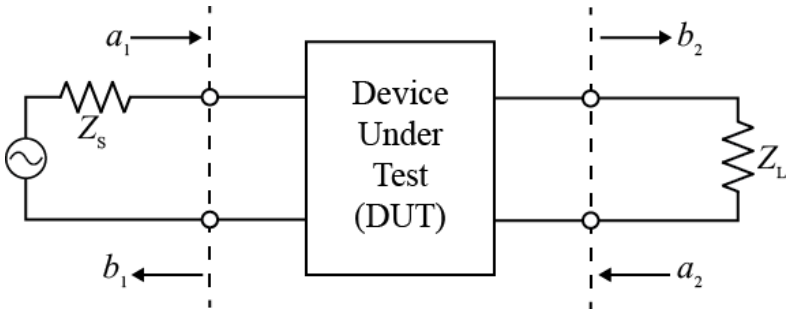


Figure 3.1: Two-port *S*-parameter Definitions

The set of *S*-parameters of the two port network are defined as:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \tag{3.1}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \tag{3.2}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \tag{3.3}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \tag{3.4}$$

where

a_1	=	the square root of the incident power on port 1
a_2	=	the square root of the incident power on port 2
b_1	=	the square root of the reflected power on port 1
b_2	=	the square root of the reflected power on port 2

Since an amplifier can be classified as a two-port network, the signal received by the antenna enters the input port (port 1) and after amplification, leaves the amplifier via the output port (port 2). Scattering parameters of this network embedded in a 50 Ω system are used to describe the interaction between different terminals as illustrated in Figure 3.1 (MacPherson et al., 2002,(3):3). The input and output ports are both terminated in 50 Ω; therefore when operating in a 50 Ω system, all traveling waves generated by the source will be absorbed by the load. The traveling waves are called incident waves. In the case of a mismatch, meaning that the port is terminated in an impedance other than 50 Ω, at either the input or output ports, the incident waves will be partially reflected. By calculating the coefficients of the incident and reflected waves, the *S*-parameters for the network are obtained (Dye & Granberg, 2001:220).

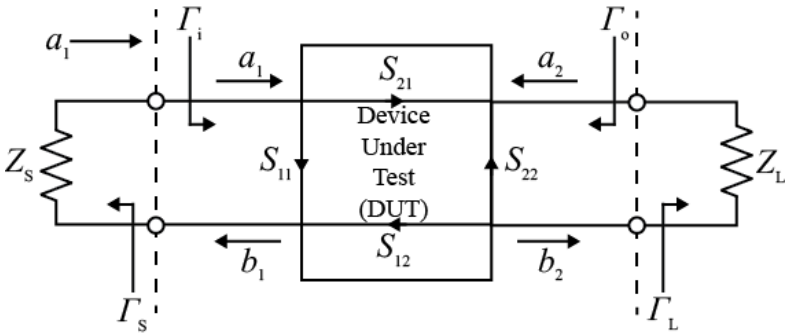


Figure 3.2: General Case of Reflection Coefficients Related to a Two Port Network

Figure 3.2 shows the general case of reflection coefficients related to a two port network and are given by:

$$\Gamma_i = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{3.5}$$

$$\Gamma_o = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{3.6}$$

If the DUT is terminated in a reflection coefficient which is the complex conjugate of Γ_o, and the input port is terminated in the complex conjugate of Γ_i, that is, simultaneous complex conjugate matching is implemented at both the input and output ports of the DUT, then a maximum gain will be achieved. This technique of matching is used in the design for maximum gain amplifiers. However, in the case of an LNA, a different approach is used and will be presented in the following sections.

3.2.1 Power Gain

The power gain of an amplifier is a performance parameter that compares the power of the signal developed across the input port to the power of the signal developed in the load and is expressed in dB. It is a measure of how much the received signal is amplified. Three types of power gains can be derived using the *S*-parameters of the two port network together with the reflection coefficients, Γ_S and Γ_L of the source and load (MacPherson et al., 2002,(3):11).

- Transducer power gain, G_T, is dependent on both Γ_S and Γ_L and is the ratio of power delivered to the load (P_L) to the power available from the source (P_{AVS}), and is given by

$$G_T = \frac{P_L}{P_{AVS}} \tag{3.7}$$

- Operating power gain, G_P, is independent of Γ_S but is a function of Γ_L and is defined as the ratio of power dissipated in the load to the power delivered to the input port (P_i) of the network and is given by

$$G_T = \frac{P_L}{P_i} \tag{3.8}$$

- Lastly the available power gain, G_A, is defined as the ratio of power available from the network to the power available from the source and is independent of Γ_L but is a function of Γ_S and is given by

$$G_A = \frac{P_{AVN}}{P_{AVS}} \tag{3.9}$$

These different power gains are used depending on which type of SSA is being designed.

3.3 Noise

Noise can be defined as random fluctuations in voltage and current. It is present throughout the entire frequency spectrum and is an unwanted type of energy that adds to the transmitted signal. Noise is critical to the performance of all RF communication systems because it corrupts the signal and affects the minimum signal level that can be reliably detected and amplified by the receiver (MacPherson & Whaits, 2002,(3):1). The noise figure of a system is a commonly used measure of the performance of an amplifier. It is a figure of merit that gives a good understanding of how much noise is added to the received signal by the amplifier itself. For a low overall system noise figure, the noise generated by the first stage must be kept as low as possible because the noise figure of the first stage determines the majority of noise figure of the whole receiver system (Love & Ajluni, 2009:116). There are different sources of noise and these can be classified into two broad categories, namely, external noise and internal noise.

3.3.1 External Noise

According to Pozar (1998:488) external noise is noise generated outside the receiver circuitry and examples are: atmospheric noise, solar noise, cosmic noise and many types of man-made noise. The level of these types of external noise cannot be controlled and the satellite will be exposed to the harsh space environment, resulting in more external noise present in the satellite subsystems.

3.3.2 Internal Noise

Internal noise is noise generated within the circuitry and can be divided into three broad groups:

- The most common type of internal noise is thermal noise and is caused by thermal agitation of electrons in a conductor. Thermal noise is generated in any resistive material and is proportional to the absolute temperature of the material. It is also sometimes referred to as Nyquist, Johnson or white noise. Every block in the communication system can be represented by an equivalent noise temperature, T_e, and defines the noise power produced per unit bandwidth measured at the temperature of the device and is given by the following equation (Ippolito, 2008: 62).

$$P_n = kTB \quad \text{watt} \tag{3.10}$$

where:

P_n	=	Available noise power in watts
T	=	Temperature of the conductor in kelvins
B	=	Bandwidth in hertz
K	=	Boltzmann's constant in joules per kelvin (1.38×10^{-23} J/K)

- Flicker noise occurs in a wide variety of systems, for example, electronic, biological and all solid state devices. Another name for this type of noise is 1/*f*-noise, because it shows a power spectral density which varies inversely as frequency increases (Pozar, 1998:488). Flicker noise occurs more commonly in Field Effect Transistors (FETs) because of the smaller channel length in FETs. The smaller the channel length, the greater the flicker noise. Bulky carbon transistors also cause flicker noise when conducting direct current, hence the use of small metal film components in low noise design (Iulian Rosu. n.d.).
- Shot noise is the time dependent fluctuations in electrical current and is caused by random arrivals of electron charges. Solid state devices such as Schottky barrier diodes, tunnel junctions and PN junctions generate more shot noise. Shot noise increases as bias current level is increased and is inversely proportional to the square of the frequency $\frac{1}{f^2}$ (De Jong, 1996:22)

3.4 Noise Parameters

Unlike man-made noise and thermal noise, which cannot be controlled or prevented from degrading the received signal, the noise and losses contributed by the receiver and related components is the most significant noise source and must be optimised and kept to a minimum through careful and clever design. To quantify the amount of noise added to the received signal by the front end alone, the ratio of output signal power to the output noise power (*S*/*N*) is considered. In a real world noisy circuit, the signal and noise applied to the input port of an amplifier are generally equally amplified, but additional noise is added by active devices and noisy components. Therefore the output noise power will be increased more than the output signal was increased and the output signal-to-noise ratio will thus decrease (Pozar, 1998:493). In 1944 Harald T. Friis introduced the concept of noise factor, *F*. The noise factor characterises the degradation in the signal-to-noise ratio between the input and output ports of the front end and is defined as

$$F = \frac{S_i / N_i}{S_o / N_o} \geq 1 \tag{3.11}$$

The noise figure (*NF*) of a network is a logarithmic quantity expressed in decibels and is obtained from the noise factor using Equation (3.12)

$$NF = 10\log_{10}(F) \qquad \text{dB} \qquad (3.12)$$

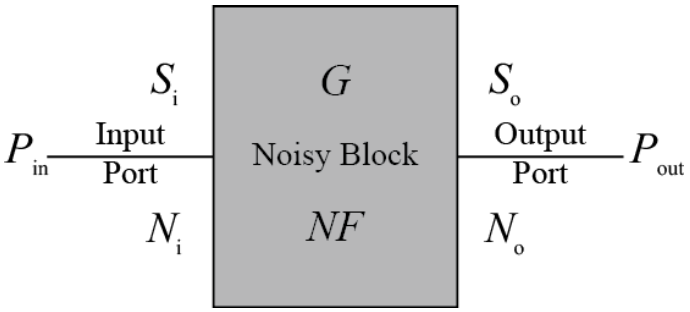


Figure 3.3: Parameters Associated with a Real World RF Network

Figure 3.3 represents a real world RF network with the various parameters associated with it. The total output noise power given in Equation (3.13) shows that the total output noise power of the network will always be greater than the output noise power when only considering input noise.

$$P_{no} = G_A P_{ni} + P_n \qquad \text{watts} \qquad (3.13)$$

where:

P_n	=	Additional noise power produced by circuit in watts
P_{ni}	=	Noise power at the input port in watts
P_{no}	=	Noise power at the output port in watts
G_A	=	Power gain of circuit block

3.5 Noise Factor of Cascaded Networks

In a receiver system each of the various blocks contributes to the overall noise factor of the system by degrading the signal-to-noise ratio to some degree. If the noise factors of the individual stages are known, the overall noise factor can be calculated using Equation (3.14).

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_2 - 1}{G_1 G_2} + \frac{F_3 - 1}{G_1 G_2 G_3} + \ldots \qquad (3.14)$$

where:

F_1	=	the noise factor of the first stage
F_2	=	the noise factor of the second stage
F_3	=	the noise factor of the third stage
G_1	=	the gain of the first stage
G_2	=	the gain of the second stage

From Equation (3.14) it is clear that the overall noise factor of the entire system is largely determined by the noise factor of the first stage (Vendelin, Pavio, & Rohde, 2005:333). By optimising the noise factor of the first stage and keeping it as low as possible, it will guarantee a very low overall noise factor. Also, the noise generated in subsequent stages will have very little or no effect on the overall noise performance of the system and these subsequent stages can be designed for maximum gain which will increase the overall gain of the system.

3.6 Dynamic Range

In theory, an increase in the power level of the signal at the input port of an amplifier should result in a linear increase in the power level of the signal at its output port. However, because the ideal transistor does not exist, the effect of thermal noise and some external noise riding on the received signal causes the noise floor to rise and at very low input power levels and the output response of a real world transistor will be non-linear. On the other hand, as the power level of the input signal is increased, the amplifier is driven into saturation and the increase in output power level will not follow in a linear manner due to the physical construction and nonlinearities of the device itself (Pozar, 1998:500). The region in-between the noise floor and where the amplifier goes into saturation is called the dynamic range and is ideally where one would want to operate the amplifier. The dynamic range of an amplifier is illustrated in Figure 3.4 and is given by Equation (3.15).

$$DR = OP_{1\text{dB}} - P_{\text{o(MDS)}} \qquad \text{dB} \tag{3.15}$$

where: $OP_{1\text{dB}}$ is the output one dB compression point

$P_{\text{o(MDS)}}$ is the output minimum detectable signal level

The $P_{\text{o(MDS)}}$ can only be found once a minimum detectable input signal, $P_{\text{i(MDS)}}$ is amplified enough such that $P_{\text{o(MDS)}}$ is above the noise power level. The output thermal noise power level of a two port network, with a noise factor F and gain G_{A}, as described by Equation (3.10) is given by

$$P_{\text{no}} = F.G_{\text{A}}.k.T_0.B \qquad \text{watt} \tag{3.16}$$

where:

$k.T_0.B = -174$ dBm.Hz^{-1}

and assuming that the minimum detectable signal is x dB above the noise floor, the following equations can be derived.

$$P_{\text{i(MDS)}} = -174 + 10\log B + 10\log F + x \qquad \text{dBm} \tag{3.17}$$

$$P_{o(MDS)} = -174 + 10\log B + 10\log F + x + 10\log G_A \quad \text{dBm} \tag{3.18}$$

Unless stated otherwise, *x* will be assumed to be 0 dB for all practical uses, it is however common to use *x* equal to 3 dB in other literature sources (MacPherson et al, 2007,(6):2).

3.7 1dB Compression Point

The 1 dB compression point, denoted P_{1dB}, is a performance parameter of a SSA and gives an indication of the maximum power that can be delivered to a load, or in other words, the point at which the output power level ceases to increase proportionally to an increase in input power level. The 1 dB compression point is the point where the output power of the amplifier is exactly 1 dB less than the ideal linear output power curve due to the non-linearities in the active device and is clearly illustrated in Figure 3.4.

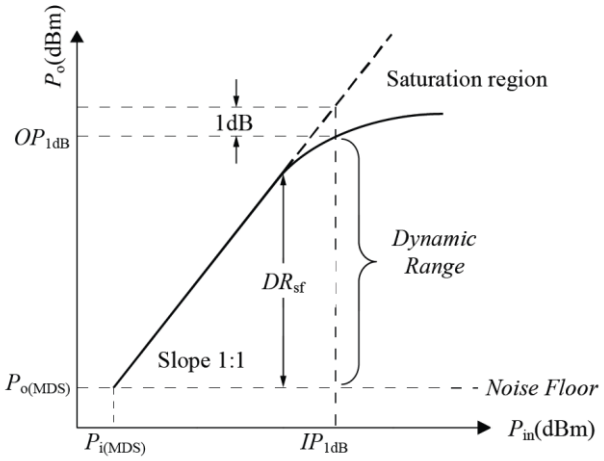


Figure 3.4: Illustration of the Dynamic Range and Spurious Free Dynamic Range

where:

P_o(dBm)	=	output power of the amplifier measured in dBm
OP_{1dB}	=	output power of the amplifier at the1 dB compression point
$P_{o(MDS)}$	=	output power level for a minimum detectable input signal
$P_{i(MDS)}$	=	input power level of minimum detectable input signal
IP_{1dB}	=	input power level at the 1 dB compression point

The 1 dB compression point can be referenced to the input or output power of the amplifier. The output 1 dB compression point (OP_{1dB}) is calculated using Equation (3.19).

$$OP_{1dB} = IP_{1dB} + G_A \quad \text{dBm} \tag{3.19}$$

3.8 Third Order Intercept Point

When a signal is applied to a non-linear device, harmonic components at multiples of the fundamental frequency can be measured at the output port of the device. These harmonics are the result of the non-linear behaviour of the device. The antenna of a receiver system will not only couple the wanted signal, but various other signals which may fall within the passband of the amplifier and, depending on the magnitude of these signals, more harmonics may be produced. If two of these unwanted signals are spaced close to each other and fall within the passband of the amplifier, the sum and differences cause higher order intermodulation distortion (*IMD*) products to be produced as illustrated in Figure 3.5 (White, 2004:458). Resultant in-band intermodulation products cause distortion of the wanted signal and cannot be attenuated by the filtering characteristics of the amplifier to such a degree that they are insignificant. It is important to have an amplifier in which the in-band intermodulation products are at a significantly lower level to the wanted signals.

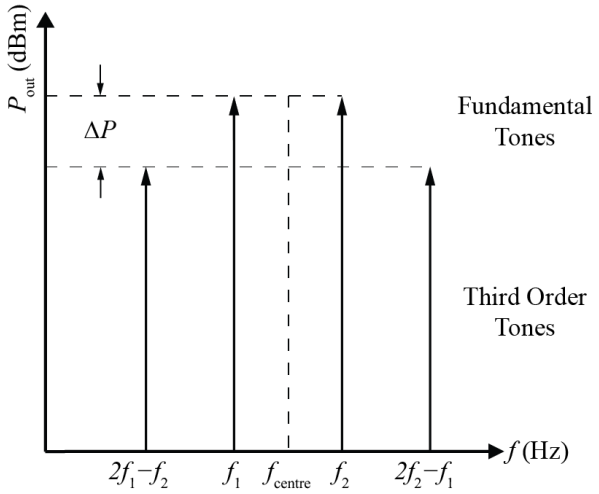


Figure 3.5: Frequency Spectrum of Fundamental and Third Order Intermodulation Products

The third order intercept point (*TOI*) is the point where the power of the ideal linear output response of an amplifier is equal to the ideal output power response of the third order product as shown in Figure 3.6. The *TOI* point can be expressed with reference to the input or output power of the amplifier. Conventionally the output power is used to define the *TOI* point and is denoted as OIP_3. The OIP_3 is a performance parameter which indicates the linearity of the amplifier, and is given by Equation (3.20). The OIP_3 is usually about 10 to 15 dB higher than the output 1 dB compression point.

$$OIP_3 = P_{\text{out}} + \frac{\Delta P}{2} \qquad \text{dBm} \tag{3.20}$$

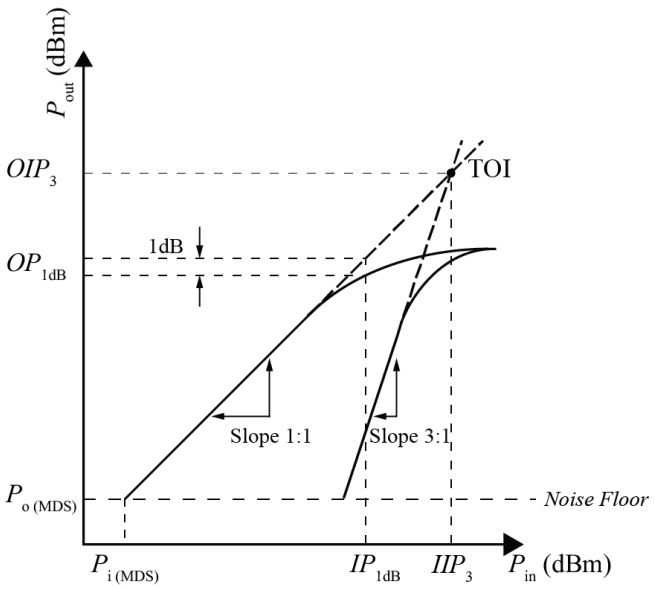


Figure 3.6: Third Order Intercept Point

When designing for low noise, a high OIP_3 value cannot be achieved as the OIP_3 point is a function of the collector current of the active device and for a minimum *NF*, the collector current is kept as low as possible.

3.9 Active Devices and Technology

In the design procedure of an SSA, selecting the correct and appropriate active device is the first step and is an important decision. The design specifications together with the type of application must be carefully considered when making this decision. Unfortunately in the design of an LNA some performance parameters must be compromised, but by choosing the appropriate active device, an excellent noise figure and a relatively high power gain can be obtained simultaneously with few compromises made (Pozar, 1998:558). Taking the space environment into consideration, where the device will be used, an active device with an extremely low *NF* must be chosen to meet the demanding specifications.

Bipolar junction transistors (BJT) are commonly used as active devices in high frequency amplifier design. Due to advances made in BJT manufacturing, they have proven to be reliable, stable and robust. The physical structure of a BJT enables it to operate from a single power supply and therefore simplifies the design. For low noise performance and low power consumption at lower frequencies up to 2 GHz, the performance of a BJT is unmatched and with recent technologies, can operate efficiently and reliably up to 6 GHz.

The design techniques used when using a BJT are similar to those used when designing with a field effect transistor (FET). FETs are very sensitive to any DC voltages and electrostatic discharge (ESD).

Excessive DC potential across the gate and source terminals of the active device will cause the gate to rupture and the device to malfunction. Generally FETs are extremely unstable and tend to oscillate at frequencies below 1 GHz. For this reason they are rather used in higher frequency designs ranging from 2 - 18 GHz and offer better high order *IMD* performance than BJTs (Dye & Granberg, 2001:45). FETs require a very precise and high drain-source current which is difficult to achieve with passive biasing and makes low power devices less practical. Using direct biasing with dual power supplies offer best performance for FET devices but makes it impractical for use in mobile applications. Fortunately technology has advanced and active device manufacturers have developed gallium arsenide field-effect transistors (GaAs FET) that use enhancement mode pseudomorphic high electron mobility transistor (E-pHEMT) technology. This technology allows the device to have a combination of high linearity and power added efficiency (PAE), allowing low voltage operation, high gain and low noise figures to be achieved while operating at low power consumption from a single power supply (Avago Technologies 2010:2).

While BJTs can operate at frequencies up to 6 GHz and FETs up to 18 GHz, the technology behind developing silicon germanium (SiGe) hetrojunction bipolar transistor (HBT) enables the device to operate at frequencies up to 60 GHz for low power devices and up to a few hundred gigahertz for high power HBT devices (Feng, Shen, Caruth & Huang, 2004:359). The main advantage of using a SiGe HBT device is that the best characteristics of both a FET and BJT are combined in one device with added benefits. Biasing of the device is simple, with low power consumption giving extremely low noise performance and high gain while operating from low to high frequencies (Vendelin et al., 2005:333).

3.10 Stability of the Active Device

Designing with real world transistors and the fact that they are used within a network means that there will be a small amount of power fed back from the output port to the input port of the active device, given by the reverse transmission coefficient, S_{12}. This is due to the relatively high gain of the active device and, combined with the input reflection coefficient (S_{11}) already present at the input port, a resultant value for S_{11} whose magnitude exceeds unity is produced, which indicates potential instability of the active device (White, 2004:458). A device that is potentially unstable or that is only conditionally stable is not acceptable to design with since out-of-band oscillations may occur when terminated in certain passive load and source impedances. The ideal is to design using an unconditionally stable active device, such that the active device could be terminated with any value of impedance at its input or output port and it would not oscillate or become unstable, and is only possible when $|\Gamma_L| < 1$ and $|\Gamma_o| < 1$.

It must be noted that the stability condition of a network is frequency dependent and the same device can be unstable at the frequency of operation but stable at another. If a device is potentially unstable, it does not mean that it is unsuitable for use. There is a technique that can be used when designing with potentially unstable devices. The most practical method and the one that will be implemented in the following designs is to resistively load the active device before designing matching networks, thus forcing it to become unconditionally stable. Since the *S*-parameters of the active device are given in the data sheet of the manufacturer, the Rollet stability factor (*K*) for a two port network at a specific frequency can easily be calculated and is given by:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} \tag{3.21}$$

where

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \tag{3.22}$$

For the circuit to be unconditionally stable, Equation (3.27) must be satisfied.

$$K > 1 \quad \text{and} \quad |\Delta| < 1 \tag{3.23}$$

This condition can be achieved by resistively loading the active device. A number of techniques are available to make the device unconditionally stable and the following options were evaluated:

- Connecting a resistor in series with the base of the transistor.
- Connecting a resistor in shunt with the base of the transistor.
- Connecting a resistor in series with the collector of the transistor.
- Connecting a resistor in shunt with the collector of the transistor.

Due to a poor noise factor and low power gain performance the first two techniques listed above are not normally implemented. The most popular and also the technique that will be used in the SSA designs, is the fourth one. It is simple to implement and offers a good noise figure and power gain (MacPherson et al, 2002,(4):3).

Load and Source Stability Circles

As mentioned in the previous section, if the amplifier is terminated in a particular load or source impedance it may become unstable and oscillate. By using Equations (3.5) and (3.6) and applying the requirements for unconditional stability the following equations can be derived.

$$\left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \tag{3.24}$$

and

$$\left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1 \tag{3.25}$$

With the aid of a Smith chart certain regions are determined where values for Γ_S and Γ_L can be chosen and the amplifier will not oscillate. To define this range of values for Γ_S and Γ_L, the magnitudes of Equations (3.24) and (3.25) are equated to one. Solving for Γ_S and Γ_L, the solutions form independent circles that, when plotted on a Smith chart, define the boundaries between the stable and potentially unstable regions of values for Γ_S and Γ_L. These circles are called load and source stability circles and are defined as the loci of Γ_S values where $|\Gamma_o| = 1$ and Γ_L values where $|\Gamma_i| = 1$ respectively. The radii and centres can be calculated using Equations (3.26) through (3.29) for the load stability circle with a centre C_L and radius r_L, where

$$C_L = \frac{\left(S_{22} - \Delta S_{11}^*\right)^*}{|S_{22}|^2 - |\Delta|^2} \qquad \text{(Centre)} \tag{3.26}$$

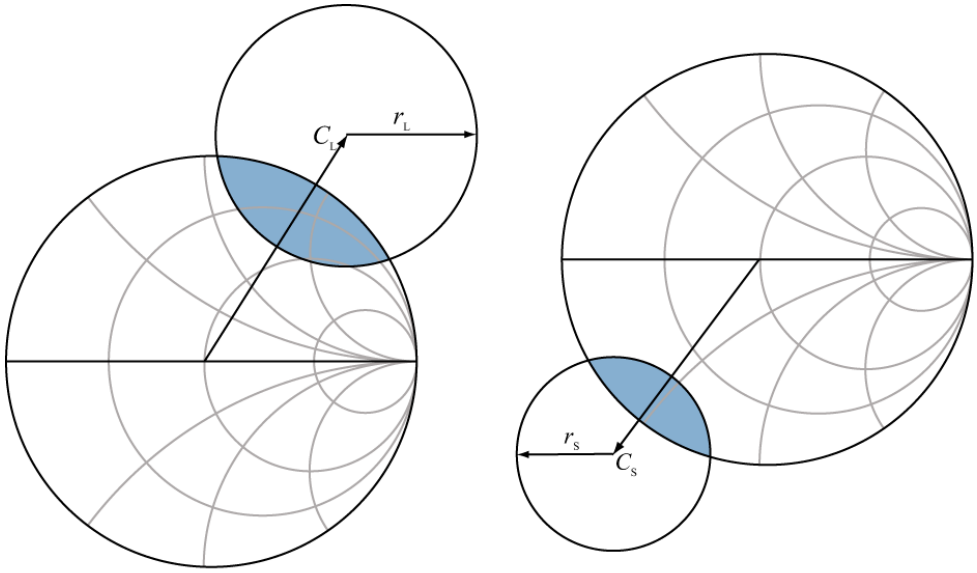
$$r_L = \left| \frac{\left(S_{12}S_{21}\right)}{|S_{22}|^2 - |\Delta|^2} \right| \qquad \text{(Radius)} \tag{3.27}$$

Similar results can be obtained for the source stability circle:

$$C_S = \frac{\left(S_{11} - \Delta S_{22}^*\right)^*}{|S_{11}|^2 - |\Delta|^2} \qquad \text{(Centre)} \tag{3.28}$$

$$r_S = \left| \frac{\left(S_{12}S_{21}\right)}{|S_{11}|^2 - |\Delta|^2} \right| \qquad \text{(Radius)} \tag{3.29}$$

Using the *S*-parameters of the active device, the load and source stability circles can be plotted and the unstable and stable regions on a Smith chart can be defined. Figure 3.7 illustrates this concept and gives a better understanding of the stable and unstable (highlighted) regions on the Smith chart for the illustrated load and source stability circles.



a) Load stability circle *b) Source stability circle*

Figure 3.7: Smith Chart with Load and Source Stability Circles

If the load stability circle represents $|\Gamma_i| = 1$ then the one side of the boundary circle represents $|\Gamma_i| < 1$ and the other side $|\Gamma_i| > 1$, and similarly for the source stability circle representing $|\Gamma_o| = 1$. One must determine which side of the circle is stable and which unstable; in other words, for which values of Γ_L will $|\Gamma_i| < 1$ and which values of Γ_S produce $|\Gamma_o| < 1$. If the output port of the amplifier is terminated in the system characteristic impedance, $Z_L = Z_0$, then $\Gamma_L = 0$ and according to Equation (3.5) it can be shown that $|\Gamma_i| = |S_{11}|$. Therefore, if $|S_{11}| < 1$ then $|\Gamma_i| < 1$, meaning that $\Gamma_L = 0$ must be in a stable region. From this it can be concluded that the area of the Smith chart not covered by the load stability circle is the stable area because $\Gamma_L = 0$ is the centre of the Smith chart. For values of $|S_{11}| > 1$, when $Z_L = Z_0$, then $|\Gamma_i| > 1$ and only the area of the Smith chart covered by the load stability circle is the stable region. The same principle is applied for $S_{22} \geq 1$ because $|\Gamma_o| = |S_{22}|$ when $Z_S = Z_0$ and then $\Gamma_S = 0$, as illustrated in Figure 3.8 for the source stability circle.

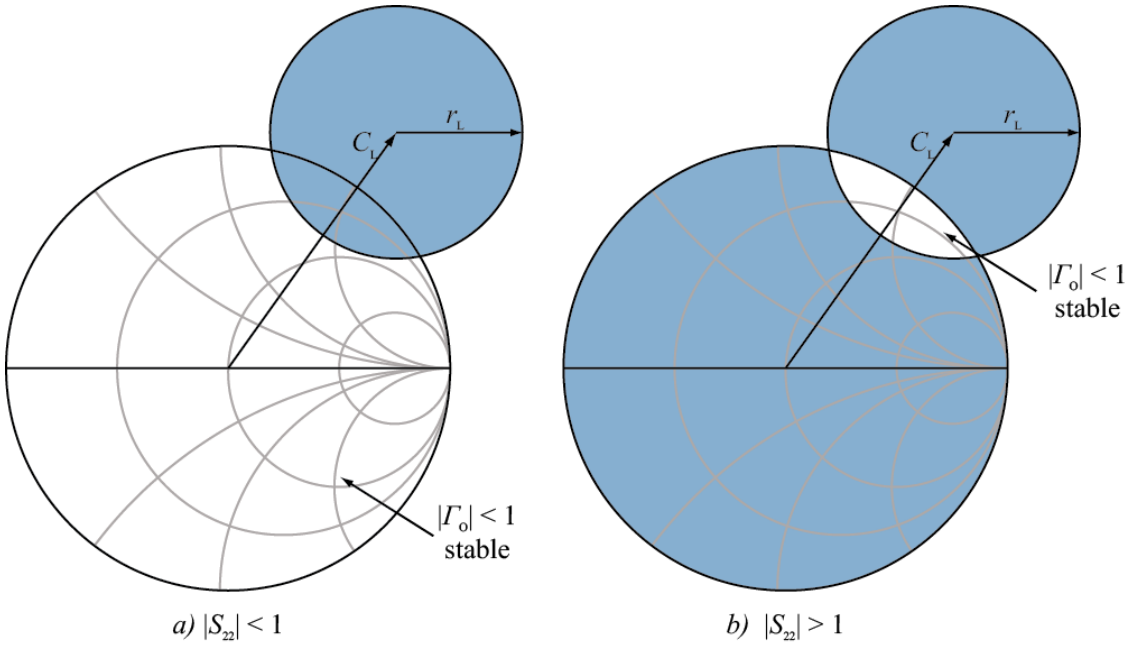


Figure 3.8: Source Stablity Circles for a Conditionally Stable Device

3.11 Impedance Matching

Impedance matching is an important and integral part in the design of high frequency small signal amplifiers. Impedance matching not only allows for maximum power transfer from source to load but is also responsible for meeting minor constraints such as maximising power handling capabilities and ensuring a more linear output power response. By matching small signal components, the overall signal-to-noise ratio of the system can be improved and unnecessary losses kept to a bare minimum (Bogdanov & Ludwig, 2000:417).

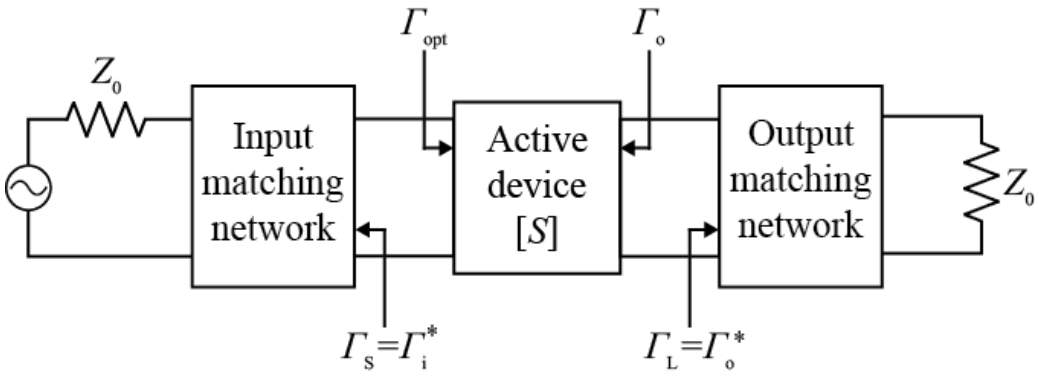


Figure 3.9: Active Device with Matching Networks Connected

Matching networks are used to enable the operation of the active device in a 50 Ω system. They match the impedance presented by the input and output ports of the transistor to the impedances presented by the generator and the load respectively, which are usually 50 Ω. Different techniques and types of matching networks are available and offer a range of advantages for specific applications. For the

proposed SSA designs, passive matching networks will be used but both lumped and distributed element designs will be considered and compared, as they both operate effectively at low GHz frequency ranges (Vendelin et al., 2005:252).

In small signal amplifier design the most commonly used matching topologies are T-, Pi- and L-matching networks. T- and Pi-matching networks are used for narrowband amplifier designs because the quality factor (*Q*-factor) of the network can be specified and controlled, together with the passband of the matching network. On the other hand L-matching networks have a relatively wide bandwidth, with a lower *Q*-factor but still meet the specifications and have fewer components. In a later chapter it will also be shown that the input and output matching networks contribute to minimising the component count of the circuit as well as optimising the layout of the final design (Iulian Rosu. n.d.).

3.12 Lumped Element Matching

L-matching networks were given the name because of the arrangement of the reactive elements in the network. In designing an L-matching network, one of two procedures can be followed namely:

- Calculate the values of the elements using analytical methods
- Using the Smith chart to determine the values of the matching elements

By using the analytical process, very accurate and precise results can be obtained. Doing the calculations by hand is tedious and time consuming, but by using computer-aided techniques the results can be obtained easy and accurately.

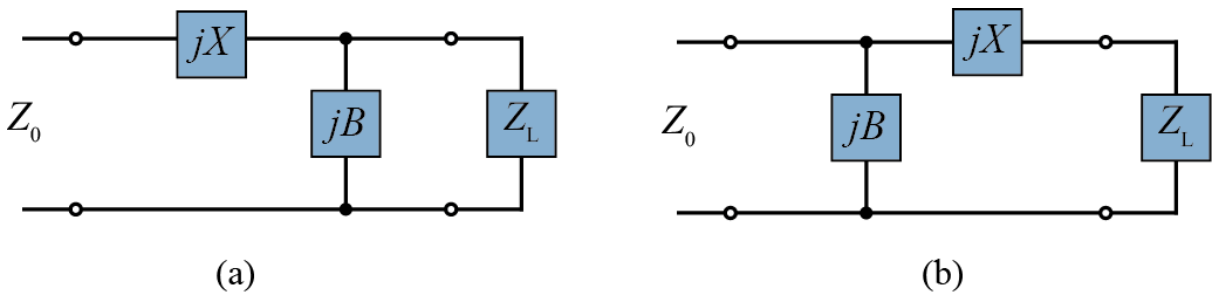


Figure 3.10: L-section Matching Network Configurations

Considering Figure 3.10(a) when $Z_L = R_L + jX_L$, the impedance presented by the matching network must be equal to Z_0. Thus, for a match:

$$Z_0 = jX + \frac{1}{jB + 1/(R_L + jX_L)} \quad \Omega \tag{3.30}$$

Rearranging and separating Equation (3.30) into real and imaginary parts gives two equations for the two unknowns, X and B:

$$B\left(XR_{\mathrm{L}} - X_{\mathrm{L}}Z_0\right) = R_{\mathrm{L}} - Z_0 \tag{3.31}$$

$$X\left(1 - BX_{\mathrm{L}}\right) = BZ_0R_{\mathrm{L}} - X_{\mathrm{L}} \tag{3.32}$$

Solving Equation (3.31) for X and substituting into (3.32) yields a quadratic equation in B. Solving for B yields:

$$B = \frac{X_{\mathrm{L}} \pm \sqrt{R_{\mathrm{L}}^2/Z_0}\sqrt{R_{\mathrm{L}}^2 + X_{\mathrm{L}}^2 - Z_0R_{\mathrm{L}}}}{R_{\mathrm{L}}^2 + X_{\mathrm{L}}^2} \qquad \text{siemens} \tag{3.33}$$

Since $R_{\mathrm{L}} > Z_0$, the argument of the second square root is always positive. The series reactance is given by:

$$X = \frac{1}{B} + \frac{X_{\mathrm{L}}Z_0}{R_{\mathrm{L}}} - \frac{Z_0}{BR_{\mathrm{L}}} \qquad \Omega \tag{3.34}$$

There are possibly two solutions for B and X. In the case of a positive solution the configuration of reactive components results in a shunt capacitor and a series inductor. A negative solution results in a shunt inductor and series capacitor. For the second L-match network in Figure 3.10b where $R_{\mathrm{L}} < Z_0$ the admittance presented to the rest of the circuit by the matching network together with the inductive load impedance must equal $1/Z_0$.

$$\frac{1}{Z_0} = jB + \frac{1}{R_{\mathrm{L}} + j\left(X + X_{\mathrm{L}}\right)} \qquad \text{siemens} \tag{3.35}$$

Rearranging and separating the terms into real and imaginary parts gives two equations for the two unknowns:

$$BZ_0\left(X + X_{\mathrm{L}}\right) = Z_0 - R_{\mathrm{L}} \tag{3.36}$$

$$X + X_{\mathrm{L}} = BZ_0R_{\mathrm{L}} \tag{3.37}$$

Solving for *X* and *B* gives:

$$X = \pm\sqrt{R_L\left(Z_0 - R_L\right)} - X_L \qquad \Omega \qquad (3.38)$$

$$B = \pm\frac{\sqrt{\left(Z_0 - R_L\right)/R_L}}{Z_0} \qquad \text{siemens} \qquad (3.39)$$

The positive and negative signs indicate that there are two possible solutions. A positive reactance corresponds to an inductor and a negative reactance to a capacitor. In a similar fashion, a positive susceptance would mean that a capacitor will be selected and a negative susceptance implies an inductor (Pozar, 1998:224).

3.13 Distributed Element Matching

When using lumped elements for matching at microwave frequencies, the component values become too small and impractical while the influence of parasitic inductance and capacitance in them increases and is no longer negligible. Even in cases when there are critical height constrains placed on the design, resorting to distributed element matching holds advantages, such as reduced component count and ease of tuning microstrip elements. Several techniques and topologies for microstrip impedance matching are available but in small signal amplifier design the one that is practically simple and easy to fabricate is a single stub tuning circuit. It is implemented by using a single open-circuited or short-circuited length of transmission line, called a stub, placed in parallel or series at a specific distance from the load being matched, as illustrated in Figure 3.11 (Pozar, 1998:228).

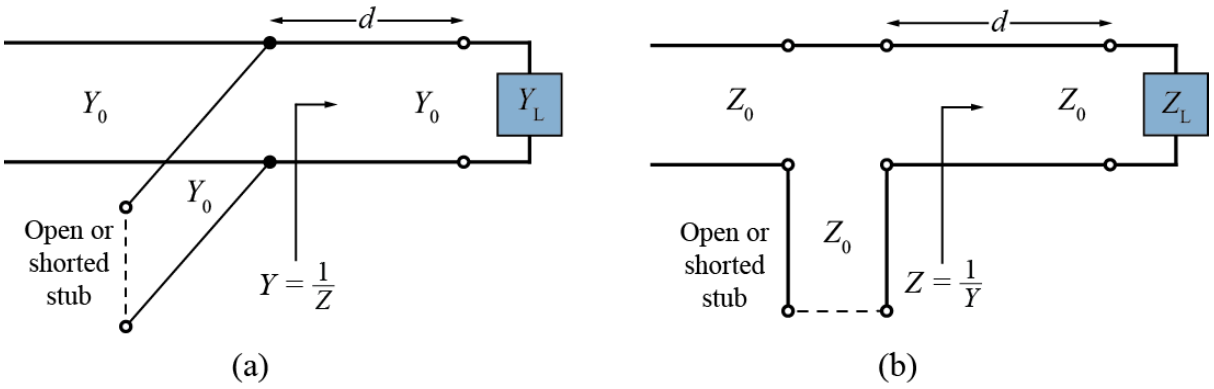


Figure 3.11: Design Process of Open and Short Stub Matching Networks

Often the short circuit stub matching technique is implemented by using vias connected to the ground plane situated on the opposite side of the PC board, which create some complications. The DC supply connected to the line must be blocked by placing a capacitor between the stub and ground thus increasing the component count, and by using vias, additional parasitic elements are introduced.

For a single shunt stub, a distance, *d*, is moved away from the load to where the admittance at that point, *Y*, is in the form $Y_0 \pm jB$ when looking back towards the load. The length of the stub, *l*, is now chosen such that the susceptance is equal to $0 \mp jB$ so that when the stub is connected, the admittance seen looking back into the line is Y_0 and the impedance is therefore equal to Z_0 (MacPherson et al, 2002,(4):3). A Smith chart can be used to design the short circuit stub matching network, or simple analytic solutions can be derived and solved using appropriate software. The stub will be placed in parallel, so for a given load impedance:

$$Z_{\mathrm{L}} = R_{\mathrm{L}} + jX_{\mathrm{L}} \qquad \Omega \tag{3.40}$$

$$Y_{\mathrm{L}} = G + jB = \frac{1}{Z_{\mathrm{L}}} \qquad \text{siemens} \tag{3.41}$$

The impedance at a distance *d* from the load is given as

$$Z = Z_0 \frac{\left(R_{\mathrm{L}} + jX_{\mathrm{L}}\right) + jZ_0 t}{Z_0 + j\left(R_{\mathrm{L}} + jX_{\mathrm{L}}\right)t} \qquad \Omega \tag{3.42}$$

where $t = \tan \beta d$. Separating Equation (3.46) into the real and imaginary parts yields:

$$G = Z_0 \frac{R_{\mathrm{L}}\left(1 + t^2\right)}{R_{\mathrm{L}}^2 + \left(X_{\mathrm{L}} + Z_0 t\right)^2} \qquad \text{siemens} \tag{3.43}$$

$$B = \frac{R_{\mathrm{L}}^2 t - \left(Z_0 - X_{\mathrm{L}} t\right)\left(X_{\mathrm{L}} + Z_0 t\right)}{Z_0\left[R_{\mathrm{L}}^2 + \left(X_{\mathrm{L}} + Z_0 t\right)^2\right]} \qquad \text{siemens} \tag{3.44}$$

Solving for *t* gives

$$t = \frac{X_{\mathrm{L}} \pm \sqrt{R_{\mathrm{L}}\left[\left(Z_0 - R_{\mathrm{L}}\right)^2 + X_{\mathrm{L}}^2 / Z_0\right]}}{X_{\mathrm{L}} - Z_0} \qquad \text{for } R_{\mathrm{L}} \neq Z_0 \tag{3.45}$$

The two principal solutions for *d* are

$$\frac{d}{\lambda} = \begin{cases} \dfrac{1}{2\pi}\tan^{-1} t, & (t \geq 0) \\ \dfrac{1}{2\pi}\left(\pi + \tan^{-1} t\right), & (t < 0) \end{cases} \tag{3.46}$$

At this point, the normalised admittance is equal to $1 + jB/Y_0$, and the length of the open circuited stub is calculated to resonate out the reactive part. The length of the open circuited stub to be connected in parallel, taking $B_s = -B$ from the result of Equation (3.44), is calculated by using Equation (3.47) (Pozar, 1998:232).

$$\frac{l_{oc}}{\lambda} = \frac{1}{2\pi}\tan^{-1}\left(\frac{B_s}{Y_0}\right) = \frac{-1}{2\pi}\tan^{-1}\left(\frac{B}{Y_0}\right) \tag{3.47}$$

3.14 Microstrip Dimensions

One of the objectives of this dissertation was to determine whether or not the lumped components of the matching networks implemented in microstrip would improve the performance of the amplifier. For the frequency that the amplifier will be operating at, lumped components are available. Although the values are small, they are not impractical and more commonly used than distributed elements because of the longer wavelength and physical size of the circuits when implemented in microstrip. A section of a microstrip transmission line is shown in Figure 3.12.

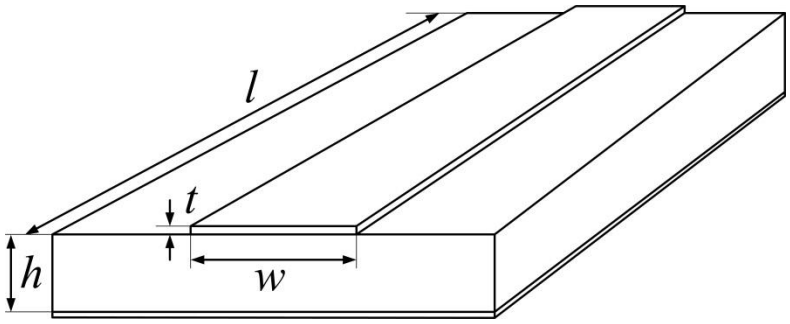


Figure 3.12: Microstrip Transmission Line

Gonzalez (1997:144) states that the effective dielectric constant (ε_{eff}) of the microstrip line with $w/h > 1$, can be approximated by:

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + 12\frac{h}{w}\right)^{-0.5} \tag{3.48}$$

For a given characteristic impedance, Z_0, and dielectric constant, ε_r, the w/h ratios can be calculated. For the ratio where $w/h \leq 2$, Equation (3.49) is used. If w/h is greater than or equal to two, Equation (3.50) is used. If the thickness of the substrate, h, is known then the width, w, of the microstrip line is calculated by multiplying Equations (3.49) or (3.50) by h (Ludwig et al, 2000:67).

$$\frac{w}{h} = \frac{8e^{A}}{e^{2A} - 2} \tag{3.49}$$

$$\frac{w}{h} = \frac{2}{\pi} + \left(B - 1 - \ln(2B - 1) + \frac{\varepsilon_r - 1}{2\varepsilon_r} \left[\ln(B - 1) + 0.39 - \frac{0.61}{\varepsilon_r} \right] \right) \tag{3.50}$$

where:

$$A = 2\pi \frac{Z_0}{60} \sqrt{\frac{\varepsilon_r + 1}{2}} + \frac{\varepsilon_r - 1}{\varepsilon_r + 1} \left(0.23 + \frac{0.11}{\varepsilon_r} \right) \tag{3.51}$$

$$B = \frac{377\pi}{2Z_0\sqrt{\varepsilon_r}} \tag{3.52}$$

The electrical length (θ_l) of the microstrip line with a physical track length of l metres can be calculated in radians by using the following equation:

$$\theta_l = \frac{\sqrt{\varepsilon_{eff}}\,\omega l}{c} \qquad \text{rad} \tag{3.53}$$

3.15 DC Biasing

In order for the active device to amplify the received signals while operating in a linear manner, the device must be correctly biased. The *S*-parameters of the active device specified on the data sheet are measured by the manufacturer at a specific bias point and it is important that this specific point be obtained and maintained under all conditions. A deviation from this bias point will cause a change in the *S*-parameters of the active device, resulting in the input and output matching networks not operating optimally.

The data sheet of an active device provides a curve depicting the relationship between the collector current, I_C, and the collector emitter voltage, V_{CE}, for a BJT or in the case of a FET, the drain current, I_D, and drain-source voltage, V_{DS}. From this curve, a point that satisfies the design requirements must

be selected where the active device is operating in its linear region. When designing for best noise performance, a lower value for I_C must be selected. Finally, the bias point must be selected so that the active device will operate in its linear region and not be driven into saturation, or in the worst case, go into thermal breakdown and break or damage the device permanently (Dye & Granberg, 2001:222).

For BJTs and HBTs various active and passive biasing networks are available. The amplifier in this dissertation is designed for space application, which means that it will be subjected to extreme temperature variations. It is thus imperative that the DC bias point remain as stable as possible throughout operating temperature variations (Gonzalez, 1997:273). Due to the limited power available for each subsystem on board the satellite, active bias networks were not considered. Figure 3.13 shows the possible choices for a passive bias network.

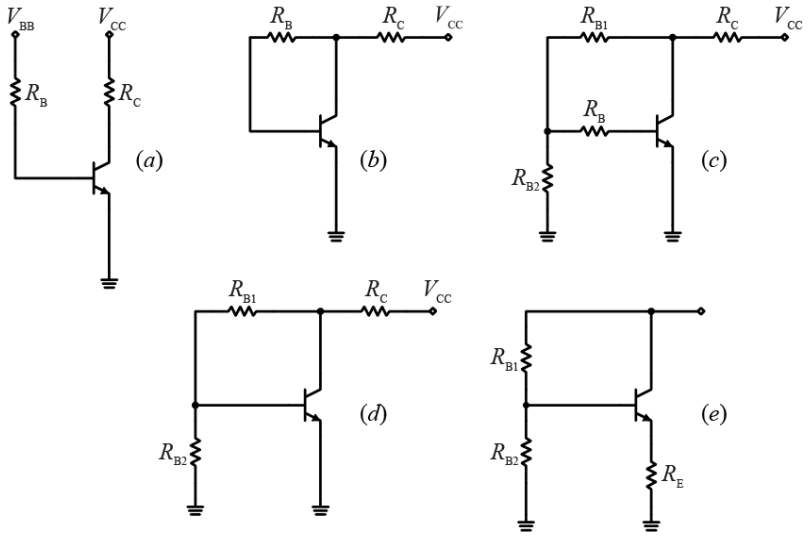


Figure 3.13: Different Types of Biasing Networks

Amongst all the passive biasing networks available, the most commonly used ones in RF design are the *voltage feedback constant base current source* and the *voltage feedback* network, shown in Figures 3.13(c) and (d) respectively. The bias network shown in Figure 3.13(c) was selected for this LNA because it provides the best temperature stability and maintains the quiescent state over large changes in ambient temperature. This bias topology also contributes towards reducing the overall component count in the optimisation of the final design.

FETs usually require a bipolar power supply since a negative gate-source voltage is needed to turn the device on. Again, active biasing biasing circuits require more than one power supply and use more power for operation. Alternative solutions were therefore considered. Figure 3.14 illustrates the configuration of a passive self bias circuit for FET operation.

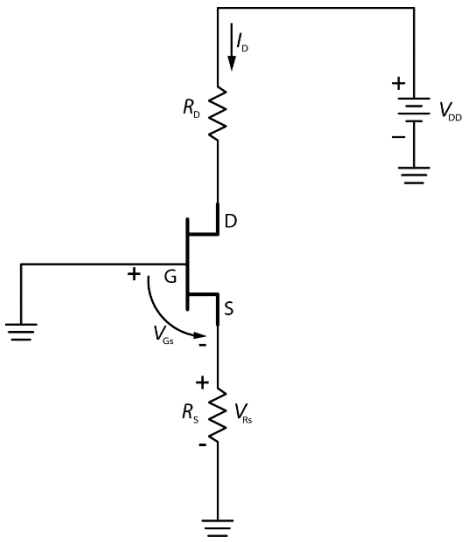


Figure 3.14: Passive Self-Biasing Network for FET Devices

This technique uses the active device itself to provide DC regulation. A single small value resistor (R_s) is placed between the source and ground, resulting in a small amount of current flowing through R_s, thus making the source voltage greater than ground potential. Since the gate is connected to ground the current will flow from the source to the gate, resulting in a negative voltage applied across the gate source junction and turning the device on. Transient protection is automatically provided in the biasing technique that uses a source resistor with a single power supply (Gonzalez, 1997:282).

3.16 SSA Design Trade-offs

When designing an SSA for a minimum noise figure, various choices and important decisions must be made due to mutually conflicting requirements of the performance parameters of an SSA. A perfect SSA will present the following characteristics.

- Low noise figure
- High gain
- Very low input and output return loss
- High 1 dB compression point
- High third order intercept point
- Low power consumption
- Large dynamic range

Unfortunately most of these parameters are conflicting. For the best noise performance, the smallest possible collector current must be used for operation; in contrast, for greater power gain the collector current must be increased. When designing for low noise, good linearity, which consists of a higher

value for *OIP3* and OP_{1dB}, cannot be achieved because the linearity of the output response is a function of the current drained by the active device.

For a low input return loss, the input port of the active device must be presented with the complex conjugate of the input reflection coefficient so that $\Gamma_S = \Gamma_i^*$ at the input port of the active device. This point will always be different from the complex conjugate point, Γ_{opt}, which represents the optimum value of Γ_s to match for lowest noise figure. A good input return loss is therefore compromised for better noise performance.

Designing with a potentially unstable active device means that a low *NF* and high power gain can be achieved, but in the unstable condition the active device will oscillate when terminated in an impedance that is located in the unstable area of the Smith chart. Making the active device unconditionally stable by using the technique of resistive loading results in a degradation of *NF* and power gain (Iulian Rosu, n.d.).

When one considers all of the above mentioned design issues, it becomes very clear why the design of high frequency circuits poses such a challenge. It is understandable why RF engineers use amplifiers in the form of a single integrated circuit, rather than putting in the hours designing them. However, when such a design is complete and the specifications are met, the overwhelming satisfaction to the designer is indescribable.

Chapter 4

Filter Theory

4.1 Introduction

Several methods of designing RF and microwave filters exist. Chapter four presents the literature review on filter design and the parameters related to filters. The different types of filters and designs will be compared and discussed and the motivation for the choice of a filter will be presented.

In order to achieve the lowest possible noise figure in an LNA, wideband matching networks are often used. The disadvantage is that other unwanted signals that fall within the passband are amplified as well as the wanted signal. To prevent the unwanted signals from causing interference, a filter will be designed and implemented to reduce the overall circuit bandwidth and hence ensure that only the wanted signal that falls between the upper and lower cut-off limits is passed through to the following stages. According to Pozar (1998:389), the perfect filter would present the following characteristics when implemented in a system:

- Zero insertion loss in the passband
- Infinite attenuation in the stopband
- Linear phase response to avoid signal distortion

Unfortunately in practice such performance cannot be achieved and some parameters must be compromised since they conflict with one another. Some commonly used RF and microwave filter types are:

- Lumped element filters: Lumped are components are implemented in the filter design, but these component types are not used at operating frequencies above 1 GHz.
- Distributed element stub filters: These filters are designed by using transmission lines to replace lumped components.

- Coupled line filters: The design of these filters involves the use of quarter-wave transmission lines sections as resonators which are then coupled together (Love & Ajluni, 2009:294).
- Interdigital filters: These filters are also implemented using microstrip lines where the filter consists of an array of quarter-wave transmission line sections which are short circuited on one end and open circuited at the other end, and alternating the orientation of the following element.(Hong & Lancaster, 2001:133).
- Comb-line filters: This type of filter consist of an array of quarter-wave coupled resonators, which are open circuited at the one end and capacitively coupled to ground at the other end using a lumped element capacitor (Hong & Lancaster, 2001:148).

4.2 Insertion Loss

An RF signal would pass through a perfect filter with no loss of power. Only the wanted frequency range of signals would be presented at the output port of the filter, with all signals at other frequency bands attenuated. In real life the filter causes loss of signal power when it passes through the filter due to its physical properties and the components it consists of. This power loss associated with the filter is called the insertion loss and quantifies how much below the 0 dB margin the power amplitude response drops (Ludwig & Bretchko, 2000:204).

4.3 Passband

The passband is defined as the range of frequencies that pass through the filter. These frequencies fall within the 3 dB attenuation points. By looking at the passband, the percentage bandwidth of the filter can be calculated. For our application, the filter response is required to be extremely narrowband. For band-pass filters, a narrowband filter is typically a filter with a passband of 0% - 20% of the centre frequency of the filter (Love & Ajluni, 2009:294).

4.4 Lumped Element Filters

Lumped element filters are more practical at operating frequencies up to 1 GHz. Lumped element filters are smaller in size and offer better spurious-free rejection than distributed element filters. On the other hand, real world lumped elements have a low *Q*-factor and lumped element filters have greater insertion loss than distributed element filters. Parasitic capacitances, as well as series resistance limit the uses of lumped components. The frequency response of lumped (and distributed) filters can change drastically if a hand, metallic object, or dielectric material is placed in close proximity of the circuit (Sayre, 2001:310-315).

4.5 Distributed and Microstrip Filters

Designing a distributed element low-pass filter is a relatively straightforward exercise. Unfortunately the design of a distributed element band-pass filter is a far greater challenge. To obtain a narrow passband with acceptable insertion loss, specialized band-pass structures must be used. These structures require laborious hand calculations but if done correctly, yield superior performance and results (Love & Ajluni, 2009:294) (Hong & Lancaster, 2001:4). Among these, the following topologies will be considered:

- Stepped impedance,
- Parallel coupled line,
- End-coupled line (very large structure at design frequency),
- Comb-line,
- Hairpin.

4.6 Lumped Element Filter Design Using the Insertion Loss Method

In the design of satellite communication systems one of the most important parameters is the insertion loss, also known as the power loss ratio of the system. If the losses in the front end can be kept to a minimum, less power needs to be transmitted for the information to be received successfully. A modern method that incorporates network synthesis techniques in designing the filter is called *the insertion loss method*. The insertion loss (*IL*) method of filter design allows the designer to design the filter for a specific insertion loss. By using this method, or by simply choosing a higher order filter, several other parameters can be optimized or improved with little compromise. (Pozar, 1998:389). It can be applied to the design of low-pass, high-pass, band-pass and band-stop filters. A band-pass filter is designed by using a low-pass filter prototype and is normalised in terms of impedance and frequency. Transformations are then applied to convert the prototypes to the desired frequency range (Vendelin et al., 2005:274).

When designing using the insertion loss method, the filter response is characterised by its insertion loss, or power loss ratio, P_{LR}

$$P_{LR} = \frac{\text{Power available from source}}{\text{Power delivered to load}} = \frac{P_{inc}}{P_{load}} = \frac{1}{1-|\Gamma(\omega)|^2} \tag{4.1}$$

Pozar (1998:402) states that when both the source and load of the network are matched, then P_{LR} is equal to $|S_{12}|^2$. The insertion loss can be expressed in dB and is given by

$$IL = 10\log P_{LR} \quad \text{dB} \tag{4.2}$$

To realise a low-pass prototype filter using the insertion loss method, the specifications of the filter must be considered and a type of frequency response must be chosen.

Maximally Flat Response Filter

Another name for the maximally flat low-pass prototype filter is a Binomial or Butterworth response as illustrated in Figure 4.1. It is a medium *Q* type of filter and the Butterworth response offers the flattest possible passband frequency response that contains no ripple for the chosen order of filter. The roll off rate of the Butterworth filter is not very steep because it is rated as a medium *Q* filter, but offers reasonable steepness for the simplicity of the design and order of the filter. (Bowick, Blyler & Ajluni, 2008:40). For a low-pass filter, the response is given by

$$P_{LR} = 1 + k^2\left(\frac{\omega}{\omega_C}\right)^{2N} \tag{4.3}$$

where:

N	=	order of filter
ω_c	=	the cutoff frequency (ω_{3dB}) of the filter
ω	=	frequency at which attenuation is required
$1 + k^2$	=	power loss ratio at the band edge

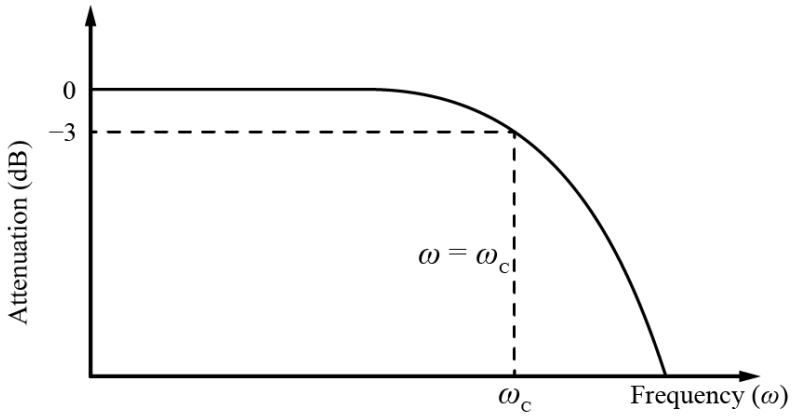


Figure 4.1: Normalised Butterworth Filter Frequency Response

The passband extends from $\omega = 0$ to $\omega = \omega_c$. For $\omega > \omega_c$, the insertion loss increases monotonically as the frequency is increased, but when $\omega >> \omega_c$ the insertion loss increases at the rate of 20 dB per decade with an increase in frequency. A disadvantage of the Butterworth transfer function is that it is not suitable for use where uniform transmission of signals in the passband is required or applications where a very steep roll off rate at cutoff is specified (Grebennikov, 2011:211).

Equal Ripple Response Filter

The Equal Ripple or Chebyshev filter has a higher *Q* value than the maximally flat response filter and hence a steeper roll off rate, but comes at the cost of some ripple included in the passband as illustrated in Figure 4.2. Chebyshev polynomials are used to define the insertion loss of an *N*-order low-pass filter and are given by

$$P_{\mathrm{LR}} = 1 + k^2 T_{\mathrm{N}}^2 \left(\frac{\omega}{\omega_{\mathrm{c}}}\right) \tag{4.4}$$

where k is the ripple constant and $T_{\mathrm{N}}^2(\omega/\omega_{\mathrm{c}})$ is a Chebyshev polynomial of order N. The steeper the roll off rate is made, the more passband ripple is introduced. The amplitude of the passband ripple is given by $1 + k^2$, as illustrated in Figure 4.2 (Bowick et al., 2008:40).

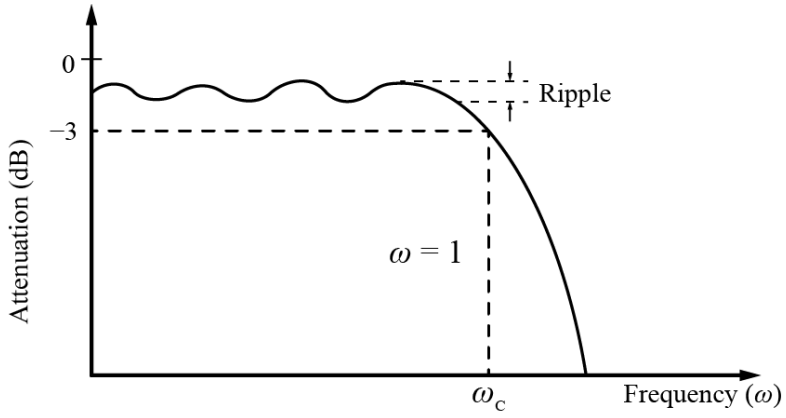


Figure 4.2: Frequency Response of Chebychev Filter

Once again, when $\omega >> \omega_{\mathrm{c}}$ the insertion loss increases at the rate of 20 dB per decade with an increase in frequency. Compared to the binomial response, at any given frequency where $\omega >> \omega_{\mathrm{c}}$ the insertion loss for the Chebychev response is $(2^{2\mathrm{N}})/4$ greater than the insertion loss of the binomial response. A disadvantage of the Chebychev response filter is that the phase response is poor with a rapid increase in the group delay variations at the band edges.

Linear Phase Low-Pass Filter

In some applications a linear group phase response in the passband is preferred rather than a steep roll-off rate and good attenuation outside the passband. For this type of application the linear phase response is chosen to avoid signal distortion. Equation 4.5 is used when designing for a linear phase response.

$$\phi(\omega) = A\omega\left[1 + p\left(\frac{\omega}{\omega_{\mathrm{C}}}\right)^{2N}\right] \tag{4.5}$$

where $\phi(\omega)$ is the phase of the voltage transfer function, A is the attenuation and p is a constant. The derivative of this function defines the group delay and also shows that it is a maximally flat response type filter (Pozar, 1998:391). This group delay is given by

$$\tau_{\mathrm{d}} = \frac{d\phi}{d\omega} = A\left[1 + p(2N+1)\left(\frac{\omega}{\omega_{\mathrm{C}}}\right)^{2N}\right] \tag{4.6}$$

As mentioned earlier, the maximally flat, Chebychev and linear phase response low-pass filter prototypes are transformed to realise high-pass, low-pass, band-pass and band-stop frequency responses by using tables that are derived from the equations of the different filter responses. After the low-pass prototypes are scaled to the correct frequency and impedance, the lumped components are replaced with distributed elements to operate at microwave frequencies.

4.7 Filter Transformations

In the design of the low-pass filter prototypes the process was simplified by normalising the impedance of the source (R_{s}) to 1 Ω and the cutoff frequency (ω_{c}) to 1 rad/s. By de-normalising and frequency scaling the design, the low-pass prototype can be converted into any desired type of filter response (Grebennikov, 2011:222).

To obtain a band-pass response from the low-pass prototype with a passband ranging from ω_1, the lower cutoff frequency, to ω_2, the higher cutoff frequency, the following frequency substitution is used:

$$\omega \leftarrow \frac{\omega_0}{\omega_2 - \omega_1}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right) = \frac{1}{\Delta}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right) \tag{4.7}$$

where
$$\Delta = \left(\frac{\omega_2 - \omega_1}{\omega_0}\right) \tag{4.8}$$

is the fractional bandwidth of the passband. By choosing the center frequency of the filter passband (ω_0) as the geometric mean, given by Equation 4.9 rather than the arithmetic mean, the equations in the remainder of the design can be simplified.

$$\omega_0 = \sqrt{\omega_2 \omega_1} \qquad \text{rads/sec} \tag{4.9}$$

By using the characteristics displayed by the band-pass response in Figure 4.3 (b) together with Equation 4.7, the transformation to a low-pass prototype response, illustrated in Figure 4.3 (a), is achieved with the following equations.

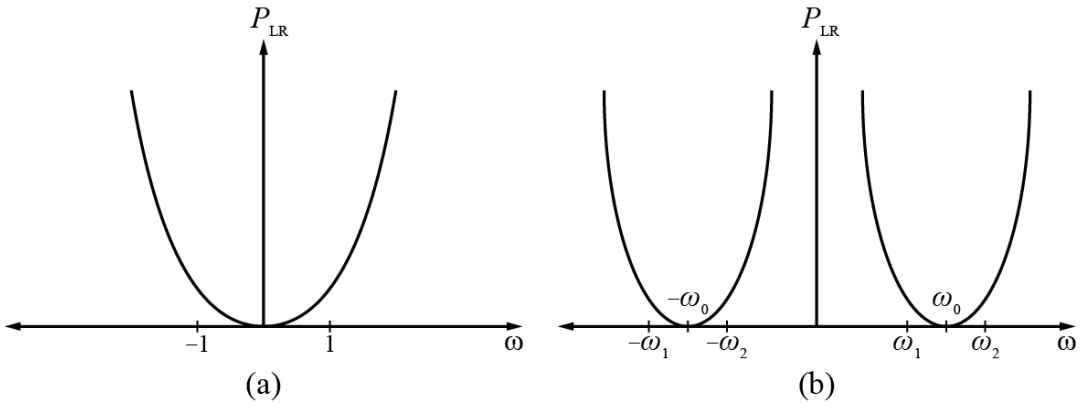


Figure 4.3: Band-pass Frequency Transformation. (a) Low-pass Filter Prototype Response for $\omega_c = 1$. (b) Transformation to Band-pass Response

for $\omega = \omega_0$,
$$\frac{1}{\Delta}\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)=0$$

for $\omega = \omega_1$,
$$\frac{1}{\Delta}\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)=\frac{1}{\Delta}\left(\frac{\omega_1^2-\omega_0^2}{\omega_0\omega_1}\right)=-1$$

for $\omega = \omega_2$,
$$\frac{1}{\Delta}\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)=\frac{1}{\Delta}\left(\frac{\omega_2^2-\omega_0^2}{\omega_0\omega_2}\right)=1$$

As a result, the same can be done with the elements that make up the filter. A series inductor L_k is transformed into a series resonant circuit with a reactance of X_k, an inductor $L_k^{'}$ and capacitor $C_k^{'}$ as follows:

$$jX_k=\frac{j}{\Delta}\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)L_k=j\frac{\omega L_k}{\Delta\omega_0}-j\frac{\omega_0 L_k}{\Delta\omega}=j\omega L_k^{'}-j\frac{1}{\omega C_k^{'}} \quad \Omega \qquad (4.10)$$

where
$$L_k^{'}=\frac{L_k}{\Delta\omega_0} \quad \text{H} \qquad (4.11a)$$

$$C_k^{'}=\frac{\Delta}{\omega_0 L_k} \quad \text{F} \qquad (4.11b)$$

By following the same principal, a shunt capacitor C_k can be transformed into a shunt resonant circuit with a reactance of B_k, an inductor L_k' and capacitor C_k'.

$$jB_k = \frac{j}{\Delta}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)C_k = j\frac{\omega C_k}{\Delta\omega_0} - j\frac{\omega_0 C_k}{\Delta\omega} = j\omega C_k' - j\frac{1}{\omega L_k'} \quad \text{siemens} \qquad (4.12)$$

where

$$L_k' = \frac{\Delta}{\omega_0 C_k} \quad \text{H} \qquad (4.13a)$$

$$C_k' = \frac{C_k}{\Delta\omega_0} \quad \text{F} \qquad (4.13b)$$

All of the series elements in the low-pass filter prototype are replaced by series resonant circuits and the parallel elements with their parallel resonant equivalent circuits to transform the low-pass filter to a band-pass filter. Each of the resonant circuits are tuned to resonate at the centre frequency of the filter, ω_0. The actual component values, impedance-scaled and frequency-translated can now be calculated using Equation 4.14 for the components in series resonant circuits and Equation 4.15 for shunt resonant components.

$$L_k' = \frac{g_n Z_0}{\omega_0 \Delta} \quad \text{H} \qquad C_k' = \frac{\Delta}{\omega_0 g_n Z_0} \quad \text{F} \qquad (4.14)$$

$$L_k' = \frac{\Delta Z_0}{\omega_0 g_n} \quad \text{H} \qquad C_k' = \frac{g_n}{\omega_0 \Delta Z_0} \quad \text{F} \qquad (4.15)$$

where Z_0 is the characteristic impedance and the element value (g_n) is the corresponding coefficient from the table of values for the desired roll-off rate and passband filter response type, and is listed in numerous literature sources (Pozar, 1998:402).

4.8 Coupled Line Filters

For narrowband band-pass filters, that is, filters with a passband of less than 20%, the use of coupled line or microstrip structures allows for easier manufacturing and yields excellent performance. The design of parallel coupled line filters is based on the relationship between the physical layout, called the shape ratio of the circuit, and the even and odd-mode characteristic impedances, Z_{0e} and Z_{0o} of the parallel microstrip lines. The shape ratio is defined by the width-to-substrate thickness (W/h) and the gap between lines to substrate thickness (s/h) of the symmetrically coupled microstrip lines illustrated in Figure 4.4 (Akhtarzad, Rowbotham & Johns, 1975:486).

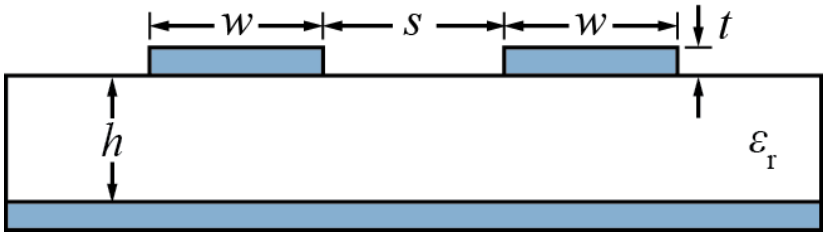


Figure 4.4: Geometry of Symmetrically Coupled Microstrip Lines

With reference to Figure 4.4, the parameters are defined as:

- w = Width of the microstrip lines (mm)
- t = Thickness of the microstrip lines (mm)
- h = Thickness of the substrate (mm)
- ε_r = Relative permittivity of the substrate
- s = Gap between coupled lines (mm)

According to Kuo, Jiang & Chang (2004:85), the n^{th} order parallel coupled microstrip filter will consist of $n + 1$ quarter-wave sections that are resonant at the center frequency, where each section has its own image impedance and are shown in Figure 4.5.

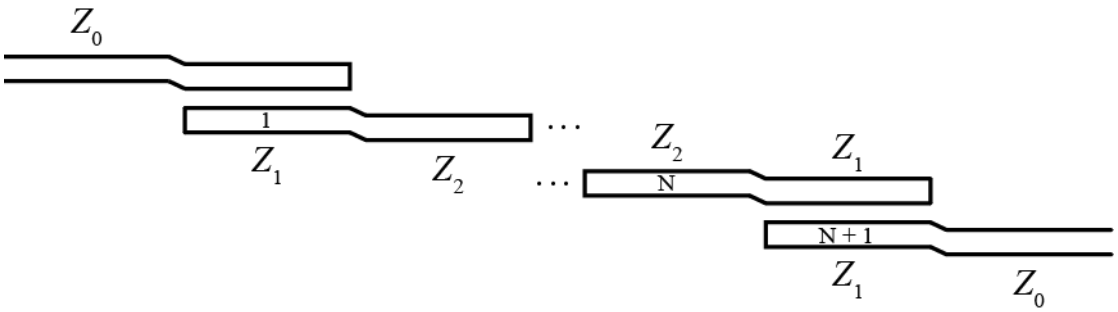


Figure 4.5: Circuit Layout of n^{th} Order Parallel Coupled Line Filter

Each quarter-wave coupled line pair can then be represented with an impedance inverter, J, between them. The equivalent circuit is shown in Figure 4.6.

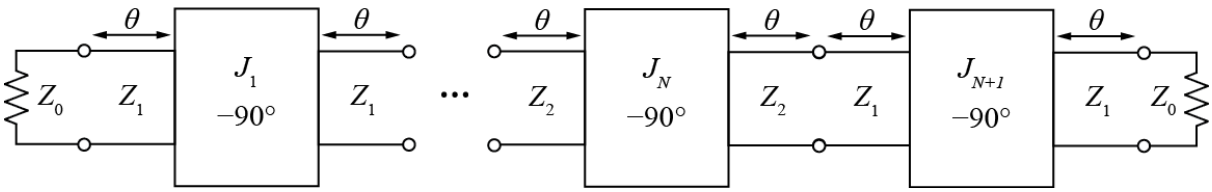


Figure 4.6: Equivalent Circuit of Admittance Inverters

Grebennikov (2011:230) states that an ideal impedance inverter can be represented by a two port network, and has the unique property that for all frequencies of operation, when it is terminated with a load impedance of Z_L, the impedance presented at the input port of the circuit (Z_{in}) is given by Equation 4.16:

$$Z_{in} = \frac{J^2}{Z_L} \quad \Omega \tag{4.16}$$

where J is real and defined as the characteristic impedance of the network. Figure 4.7 illustrates how the network can be implemented in a circuit, also known as a J-inverter, by using a quarter-wave transformer with the correct characteristic impedance.

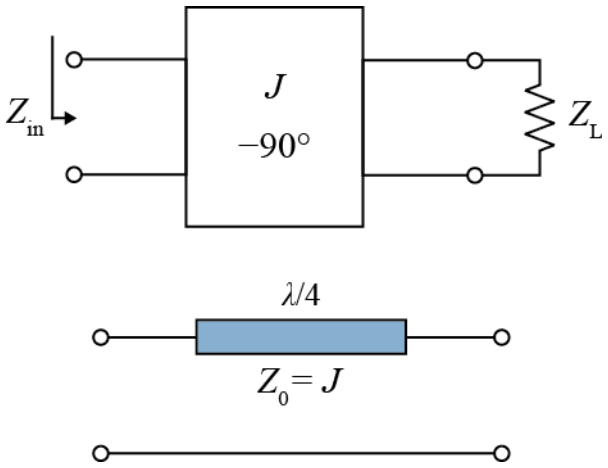


Figure 4.7: Representation of *J*-inverter and its Implementation

For an n section parallel coupled filter, the appropriate passband response is chosen and calculated; alternatively use the related coefficients from the table for the values of g_n that will be used to design the low-pass prototype. To determine the even- and odd-mode characteristic impedances for a band-pass filter with $n+1$ sections, Equations 4.17 through to 4.21 are used to calculate the following parameters:

$$Z_0 J_1 = \sqrt{\frac{\pi\Delta}{2g_1}} \tag{4.17}$$

$$Z_0 J_n = \frac{\pi\Delta}{2\sqrt{g_{n-1}g_n}} \qquad \textit{for } n = 2,3,\ldots,N \tag{4.18}$$

$$Z_0 J_{N+1} = \sqrt{\frac{\pi\Delta}{2g_N g_{N+1}}} \tag{4.19}$$

where Δ was defined earlier in Equation 4.7 and ω in Equation 4.8. The even and odd characteristic line impedances can now be determined as

$$Z_{0o}\big|_{i,i+1} = Z_0\left[1 - Z_0 J_{i,i+1} + \left(Z_0 J_{i,i+1}\right)^2\right] \qquad \Omega \tag{4.20}$$

and

$$Z_{0e}\big|_{i,i+1} = Z_0\left[1 + Z_0 J_{i,i+1} + \left(Z_0 J_{i,i+1}\right)^2\right] \qquad \Omega \tag{4.21}$$

where the indices $i, i+1$ refer to the overlapping sections of microstrip seen in Figure 4.5 and Z_0 is the characteristic line impedance of the first and last sections, which is equal to 50 Ω (Ludwig & Bretchko, 2000:260).

Synthesis Design Method

In the synthesis design method, the values Z_{0e} and Z_{0o} for the coupled line sections must all be known since they are required to calculate the W/h and s/h ratios of each section. Finding the two single-line shape ratios $(W/h)_{se}$ and $(W/h)_{so}$ that correspond to the impedances $Z_{0e}/2$ and $Z_{0o}/2$ respectively, is the first step and given by:

$$\left(W/h\right)_s = \frac{2}{\pi}\left(d-1\right) - \frac{2}{\pi}\log_e\left(2d-1\right) + \frac{\varepsilon_r - 1}{\pi\varepsilon_r}\left(\log_e\left(d-1\right) + 0.293 - \frac{0.517}{\varepsilon_r}\right) \tag{4.22}$$

where

$$d = \frac{60\pi}{Z_0\sqrt{\varepsilon_r}} \tag{4.23}$$

By simultaneously solving Equations 4.24 and 4.25, W/h and s/h for the coupled line sections are determined by:

$$\left(W/h\right)_{se} = \frac{2}{\pi}\cosh^{-1}\left(\frac{2k - g + 1}{g+1}\right) \tag{4.24}$$

$$\left(W/h\right)_{so} = \frac{2}{\pi}\cosh^{-1}\left(\frac{2k-g-1}{g-1}\right) + \frac{4}{\pi\left(1+\varepsilon_r/2\right)}\cosh^{-1}\left(1 + 2\frac{W/h}{s/h}\right), \quad \text{for } \varepsilon_r \le 6 \tag{4.25a}$$

$$\left(W/h\right)_{so} = \frac{2}{\pi}\cosh^{-1}\left(\frac{2k-g-1}{g-1}\right) + \frac{1}{\pi 1}\cosh^{-1}\left(1 + 2\frac{W/h}{s/h}\right), \quad \text{for } \varepsilon_r \ge 6 \tag{4.25b}$$

where

$$g = \cosh\left(\frac{\pi\left(s/h\right)}{2}\right) \tag{4.26}$$

and

$$k = \cosh\left[\pi(W/h) + \frac{\pi(s/h)}{2}\right] \tag{4.27}$$

The solution of simultaneously solving Equations 4.24 and 4.25 is made simpler by ignoring the second term in 4.25. The value for *s*/*h* is given by:

$$(s/h) = \frac{2}{\pi}\cosh^{-1}\left\{\frac{\cosh\left[\frac{\pi}{2}(W/h)_{se}\right] + \cosh\left[\frac{\pi}{2}(W/h)_{so}\right] - 2}{\cosh\left[\frac{\pi}{2}(W/h)_{so}\right] - \cosh\left[\frac{\pi}{2}(W/h)_{se}\right] - 2}\right\} \tag{4.28}$$

When substituting the value obtained from Equation 4.28 into Equations 4.24 and 4.25 the results are then used in the synthesis of the filter design.

Chapter 5

Front End Design

5.1 Introduction

When designing the front end of any RF receiver in a communications system certain basic steps must be followed. In the design of a receiver for satellite applications where limited power is available and reliability must be guaranteed, the design procedure stays relatively consistent except for a few extra steps and important decisions that must be made to conform to the stringent specifications.

The major objective of this dissertation was to construct several low noise amplifiers using various types of active devices for the amplifiers and different band-pass filter layouts, and then implementing them using appropriate design procedures with good RF design techniques. Chapter five will present the steps taken to design different low noise amplifiers using BJT, FET and HBT active devices to achieve the lowest noise figure with reasonable gain while complying with the power budget of the satellite in order to meet the predefined specifications.

5.2 Design Procedure

The design procedure listed below was closely followed in designing the LNAs:

- Generate the design specifications
- Select an active device
- Stabilise the active device
- Select matching topology
- Design the input and output matching networks
- Select a DC bias circuit
- Optimise the circuit for minimum component count and perform computer simulations
- Design the printed circuit board
- Construct and test the amplifier to verify that it meets the specifications

5.3 Specifications

In Table 5.1 the design specifications and requirements for the low noise amplifier are listed. A short explanation of the requirements is given thereafter.

Table 5.1: Generated Specifications for Amplifier

Parameter	Symbol	Specification
Frequency band	f	1260 – 1270 MHz
Supply voltage	V_{cc}/V_{dd}	5 V
Noise figure	NF	< 1 dB
Power gain	G_A	> 13 dB
Power consumption	P_D	< 100 mW
Input return loss	S_{11} (dB)	< –5 dB
Output return loss	S_{22} (dB)	< –15 dB

The LNA will be the first stage in the communications link after the transmitted signal is received by the antenna; hence it will be designed for lowest possible noise figure, and as shown in Section 3.5, the overall system gain can be increased in subsequent stages. These specifications were generated from link budget details as specified in the technical specification of the F'SATI Cubesat (Visser, 2009:32). A sub-1 dB noise figure and a minimum power gain of 13 dB are required to ensure reliable communication between the ground station and satellite.

The system specifications for the Cubesat specified the frequency of operation to fall within the *L*-band between 1260 MHz and 1270 MHz. The specific centre frequency of operation for the LNA was 1265 MHz

The electrical power system of the satellite provides all subsystems with a regulated 5 Volt direct current supply. Depending on the specific transistor used, the operating DC voltage will be determined individually to maximise the performance of each amplifier whilst operating at a voltage of less than 5 Volts. One of the main goals of this dissertation is to design and construct the front end section to be implemented in Cubesat receivers which means that since limited power is available from the satellite, the LNA must operate at minimum power consumption.

The input return loss (*IRL*) and output return loss (*ORL*) are two important properties in the design of an LNA. Not only do they directly affect the gain and noise figure of the circuit, the *IRL* gives an indication of how well the input matching network was designed and the *ORL* in turn indicates how well the output matching network was designed. The more negative the value of these parameters in dB, the better the matching circuit performs, and good matching also means that maximum power is transferred to the load (Gilmore & Besser, 2003:107).

5.4 Selecting an Active Device

For the different LNA amplifiers, active devices were selected on the basis of availability and the description and performance specifications provided by the manufacturer in the manufacturer's data sheet. As specified in Section 1.3, various types of active devices will be used to design low noise amplifiers. The selected devices together with the performance parameters related to each, as specified in the manufacturer's datasheet are listed in Table 5.1.

Table 5.2: Performance Specifications of Selected Transistors

Name	Manufacturer	Type	Frequency (GHz)	Voltage (V)	Current (mA)	*NF* (dB)	Gain (dB)
BFP-740	Infineon	SiGe:C	0.9 – 6	2.5	6	0.5	22
ATF-55143	Avago	E-pHEMT	0.45 – 6	2.7	10	0.5	17.7
AT-32032	Avago	Silicon bipolar	0.9 – 2.4	2.7	5	1.0	13
ATF-36163	Avago	GaAs pHEMT	1.5 – 18	1.5	10	0.5	17
ATF-36077	Avago	GaAs pHEMT	2 – 18	1.5	10	0.3	17

From what was available, a silicon bipolar transistor, a gallium arsenide pseudomorphic high electron mobility transistor (GaAs pHEMT), an enhancement mode pHEMT (e-pHEMT) and a silicon

germanium hetrojunction transistor were selected. By analysing only what is specified by the manufacturer, all the devices should be capable of meeting the required amplifier specifications.

The AT-32032 BJT from Avago Technologies is used in low power operation or circuits that are battery operated and must operate during end-of-life battery condition. Applications include LNAs, oscillators, mixers and down converters. This device is ideal for use between 900 MHz and 2.4 GHz making it perfect for use in the front end of the *L*-band receiver. Since it is a BJT it will be less susceptible to ESD and more robust within the space environment.

A new device from Avago, the ATF-55143 combines high gain, high linearity and low noise performance for use from 450 MHz to 6 GHz. It is a type of pHEMT device but can operate from a single power supply and does not need a negative supply or voltage to make the gate negative with respect to the source. This feature makes the biasing simpler and the same approach as with the BJT devices is followed.

To evaluate the more conventional field effect transistors Avago's ATF-36163 was chosen. The device is recommended for operations between 1.5 GHz and 18 GHz has a lower frequency limit of just below 1.5 GHz (Avago Technologies, 2008:1). The device is also specified for low power battery operated applications with low noise figure performance.

Although the ATF-36163 and the ATF-36077 FETs are closely related, there are some differences in performance and application. The ATF-36077 is specified as an ultra-low noise pHEMT and its performance and consistency makes it useful for high frequency, 2-18 GHz, applications ranging from *C*-Band television receivers to LNAs and *Ku*-band direct broadcast digital satellite systems. (Avago Technologies, 2008:1). The datasheet of the ATF-36077 does not specifically state that the device is not for use below 2 GHz and some of the provided *S*-Parameters start as low as 1 GHz. Because of the excellent noise performance and gain of this device, it would be useful to compare the ATF-36077 with the ATF-36163, as well as to determine if it can be used for applications in the sub 2 GHz range.

5.5 Implementing the Design Procedure

For each of the proposed active devices the same design procedure must be followed, but due to the differences in internal structure and operation of BJTs and FETs the biasing circuits differ slightly. In the following sections the detailed design procedure for each of the chosen active devices will be described together with simulations and related results, starting with the BFP-740. The same design procedure and biasing technique, which is used for most BJTs, will be used for this HBT active device. Since the BFP-740 is also the device with potentially the best performance, the design will be implemented using lumped and distributed matching networks for comparison purposes. The next LNA

uses an Avago ATF-36163 GaAs pHEMT, which will use a self-biasing circuit commonly used with many FET devices. In the design of these LNAs, the differences in designing with a FET device and a BJT are very evident, and every single aspect of LNA design would have been covered in detail. The last two LNAs will make use of the ATF-55143 E-pHEMT followed with the AT-32032 silicone BJT.

5.6 BFP-740 Amplifier Design

For comparison with the AT-32032 BJT, Infineon's BFP740 HBT was chosen. This device offers ultra-low noise and a high gain for operation up to 10 GHz. It is specified for use in wireless communication applications and can operate with very low power consumption. The data sheet indicates improved robustness which makes this device ideal for use in the Cubesat application (Infinion Technologies, 2004:1).

5.6.1 Stabilising the Active Device

After selecting the active device it must be checked for stability at the design frequency. For the active device to be unconditionally stable, Equation 3.19 must hold true. Equations 3.17 and 3.18 can be solved using the *S*-parameters of the active devices as given on the manufacturer's datasheet and also available from their website. By using Agilent's Advanced Design System (ADS) software package the calculations are simplified and can be simulated using the linear model of the active device, which contains measured *S*-parameters of the active device over a wide range of frequencies. To determine the Rollet stability factor (*K*) and the value for Delta (Δ), an *S*-parameter simulation on the active device by itself was done as shown in Figure 5.1.

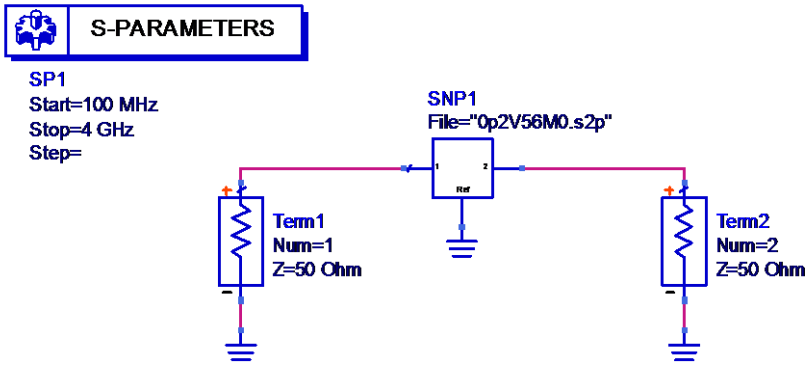


Figure 5.1: *S*-parameter Simulation for Stability Factor

The simulation results for the BFP740 active device are shown in Figure 5.2. From the results it is clear that the active device is potentially unstable (or conditionally stable) and may oscillate for certain values of source and load impedances because *K*, the stability factor, is less than one.

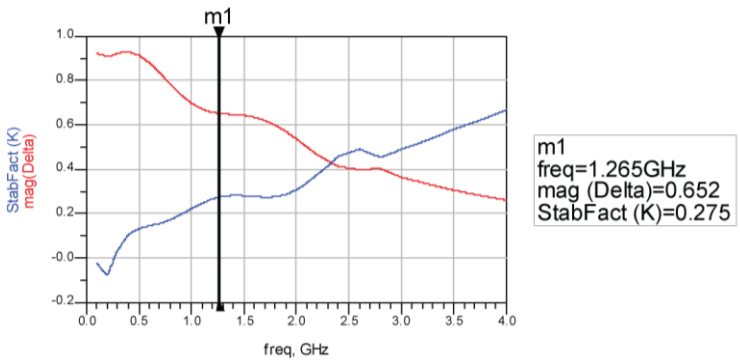


Figure 5.2: Simulation Results for Stability

To stabilise the active device a few options are available, as discussed in Section 3.10. The configuration of a shunt resistor placed on the collector to resistively load the active device was selected because it has the least effect on the gain and *NF* performance, and increases stability. To calculate the value of resistance that will be used, load and source stability circles were plotted on a Smith chart as shown in Figure 5.3.

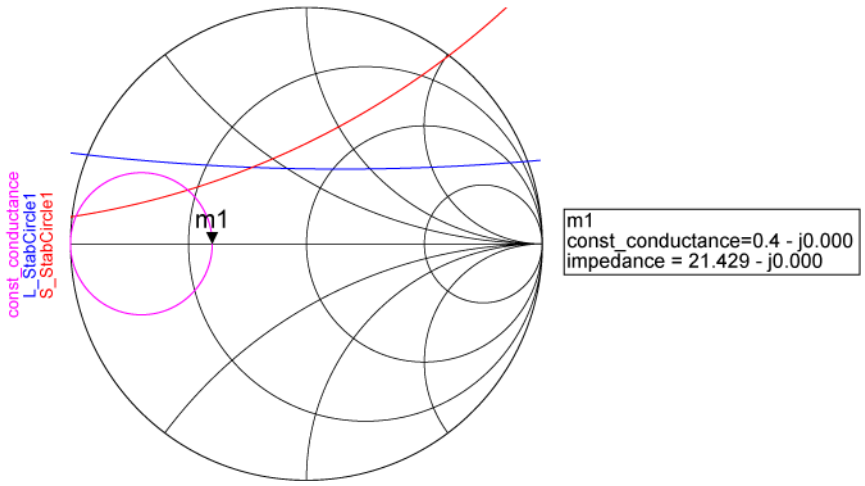


Figure 5.3: Smith Chart with Stability and Conductance Circles

To achieve unconditional stability a constant conductance circle is plotted that passes close to the load stability circle. Conductance is used because the resistor will be placed in shunt or parallel with the collector. The shunt resistance is normalised and the closest standard resistor value is selected. The calculated resistor value of 22 Ω is placed in parallel with the collector, as shown in Figure 5.4, and re-simulated.

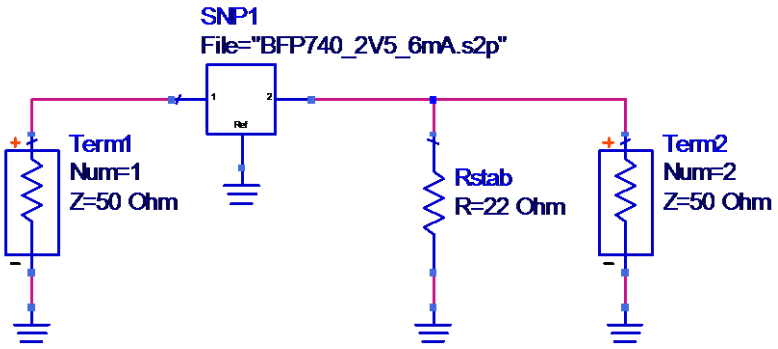
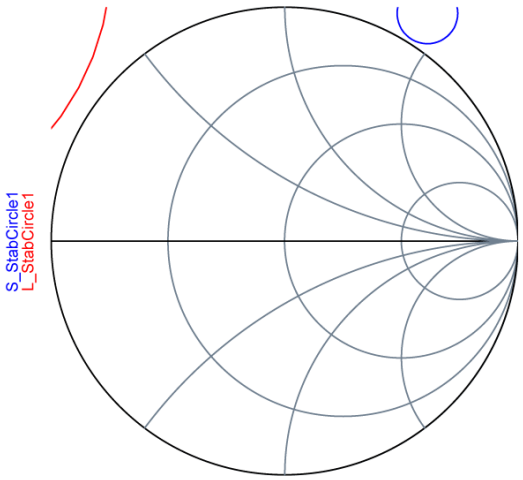


Figure 5.4: Active Device with Stabilisation Resistor

In Figure 5.5 the simulation results clearly show that both the source and load stability circles have moved completely off the Smith chart, indicating that terminating impedances for the active device can be selected anywhere on the Smith chart and the active device will remain in a stable condition. A new set of *S*-parameters for the unconditionally stable active device was generated and is listed in Figure 5.5.



freq	S(1,1)	S(1,2)	S(2,1)	S(2,2)
1.265 GHz	0.861 / -60.426	0.017 / 56.140	4.806 / 136.765	0.437 / -171.435

Figure 5.5: Smith Chart with Load and Source Stability Circles

Figure 5.6 shows that the Rollet stability factor (K) is now greater than one and $|\Delta|$ is less than one for the entire frequency band of interest, thus satisfying Equation 3.19.

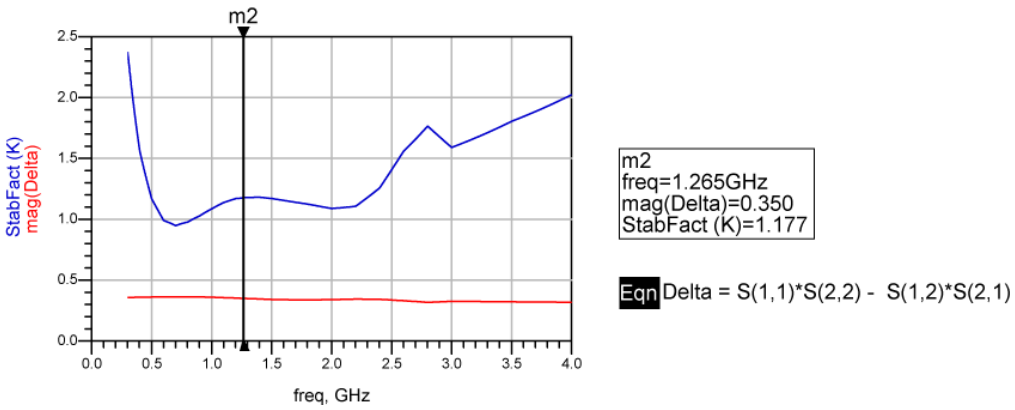


Figure 5.6: Simulated Results for Delta and Rollet Stability Factor after Stabilisation

The active device is now unconditionally stable and matching networks can be designed to match the impedances presented by the input and output ports of the amplifier to 50 Ω.

5.6.2 Design of Matching Networks

The active device is now unconditionally stable and a new set of *S*-parameters was generated for the operating frequency. The next step in the design process will be to design matching networks to ensure maximum power transfer from the source to the load and to make the amplifier suitable for operation in a 50 Ω system.

The optimal *IRL* can only be achieved when the impedance presented by the output port of the input matching network is the complex conjugate of the impedance presented by the input port of the active device, as shown in Figure 3.9. This technique allows for maximum gain, but for optimum noise performance the input port of the active device must be presented with a different value of impedance, compromising a good *IRL* significantly. This value of impedance is obtained from the optimum source reflection coefficient denoted, Γ_{opt}, and is given in the data sheet by the manufacturer or obtained by simulation for the particular frequency of operation. Using the new set of *S*-parameters generated with the stable active device, together with Γ_{opt}, the conditions indicated in the diagram in Figure 5.7 were followed in designing the input and output matching networks for the low noise amplifier.

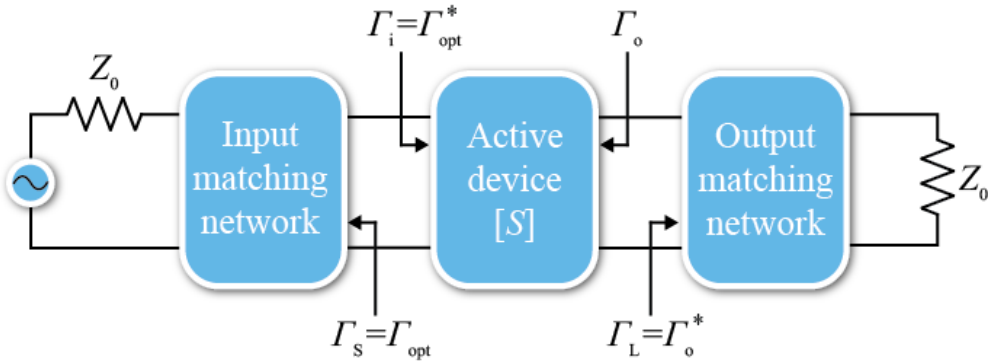


Figure 5.7: Transistor with Matching Networks Optimised for Low Noise Design

Lumped Element Matching

In the design of the input matching network the active device must be presented with a reflection coefficient value of Γ_{opt} as described in Figure 5.7. Γ_{opt} was re-interpolated in ADS as $0.304\angle 29.458$ and Γ_{opt}^*, the complex conjugate, is equal to $0.304\angle -29.458$. Γ_o was calculated to be $0.536\angle -171.453$ using Equation 3.6. The process described in Section 3.12 was used to calculate the physical component values and confirmed using a software program called L-net (v1.0) (Grant, 1998). The following possible matching networks resulted from the calculations:

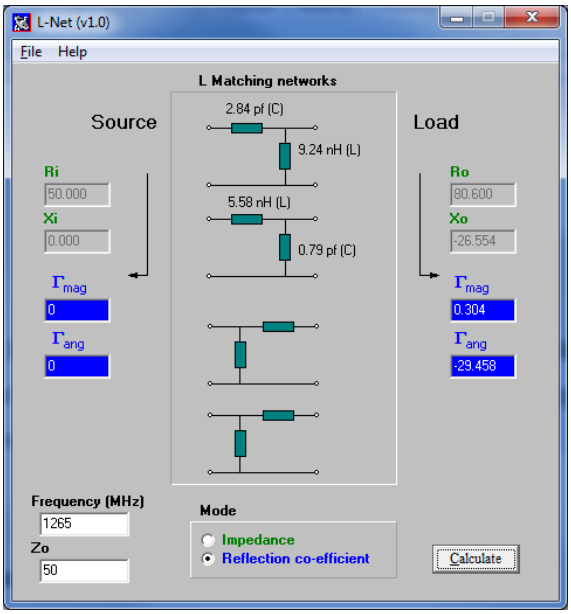


Figure 5.8: Solutions for Input Matching Network

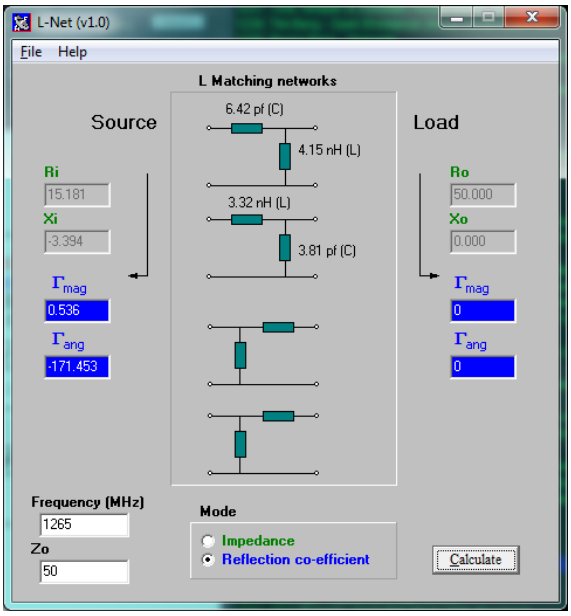


Figure 5.9: Solutions for Output Matching Network

The calculated values for the lumped element L-matching network were implemented and an *S*-parameter simulation was done using the circuit in Figure 5.10.

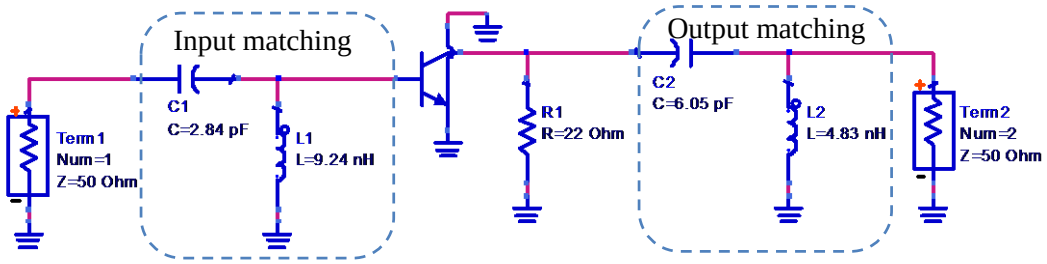


Figure 5.10: Amplifier with Proposed Lumped Element Matching Networks

Ideal components were used in the initial simulation to determine if the calculated component values gave the expected results. Figure 5.11 shows the results obtained from the simulation. A moderately high gain of 16.356 dB and a low noise figure of 0.47 dB were achieved with a good *ORL* of −36.973 dB. As expected the *IRL* is relatively poor because it was compromised for the lowest noise figure.

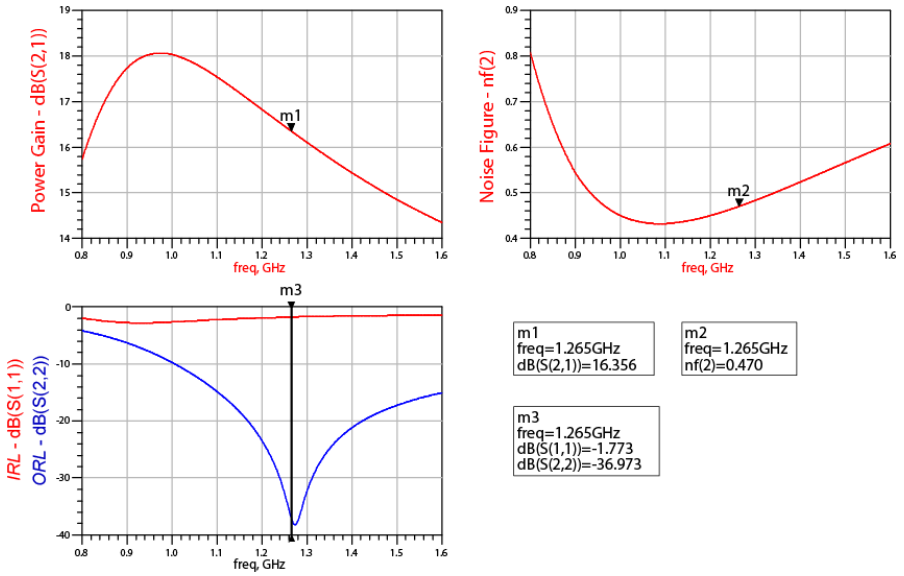


Figure 5.11: Results from Initial Simulation with Ideal Components

Distributed Element Matching

The open circuit single stub matching technique will be used for the distributed matching networks of the LNA. Rogers' RO4003C™ microwave substrate was selected on the basis of availability and how well it compares to top end substrates such as Rogers' GX substrate (Rogers Corporation, 2002:2). The low dielectric constant and low loss at higher frequencies makes this substrate ideal for distributed element applications.

To implement the microstrip matching networks, Equations 3.32 through 3.45 were programmed into MATLAB (Appendix A) together with the substrate and frequency specifications. Once again the input matching network was designed by choosing Γ_s equal to Γ_{opt} then matching to the complex conjugate of $\Gamma_{opt.}$ Then Γ_o is calculated and this value is then matched to 50 Ω. The value for Γ_{opt}, equal to $0.304\angle -29.458$, corresponds to an impedance of $Z_L = 80.6 - j26.554$ Ω. The results of using the MATLAB program to calculate the input matching circuit options are:

```
Open circuit shunt stub:
Solution 1
Distance from load d: 0.11λ, 39.12 degrees, 17.35 mm, 683.03 mills
Length of stub l:     0.41λ, 147.45 degrees, 65.39 mm, 2574.51 mills
Solution 2
Distance from load d: 0.31λ, 111.42 degrees, 49.41 mm, 1945.41 mills
Length of stub l:     0.09λ, 32.55 degrees, 14.43 mm, 568.26 mills
Width of section w:   1.88 mm, 74.11 mills
```

The second solution was selected and implemented in ADS. Figure 5.12 shows the configuration of the circuit for the *S*-parameter simulation with the results shown in Figure 5.13

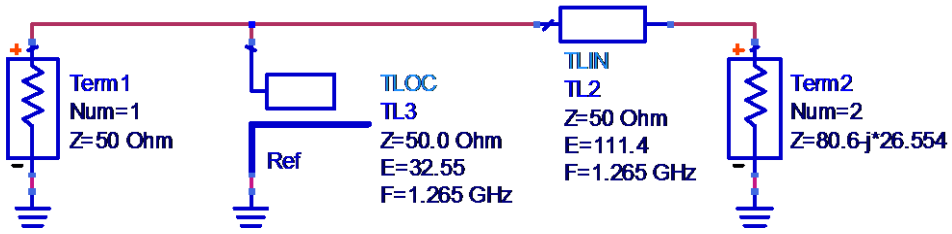


Figure 5.12: *S*-parameter Simulation for Distributed Input Matching Network

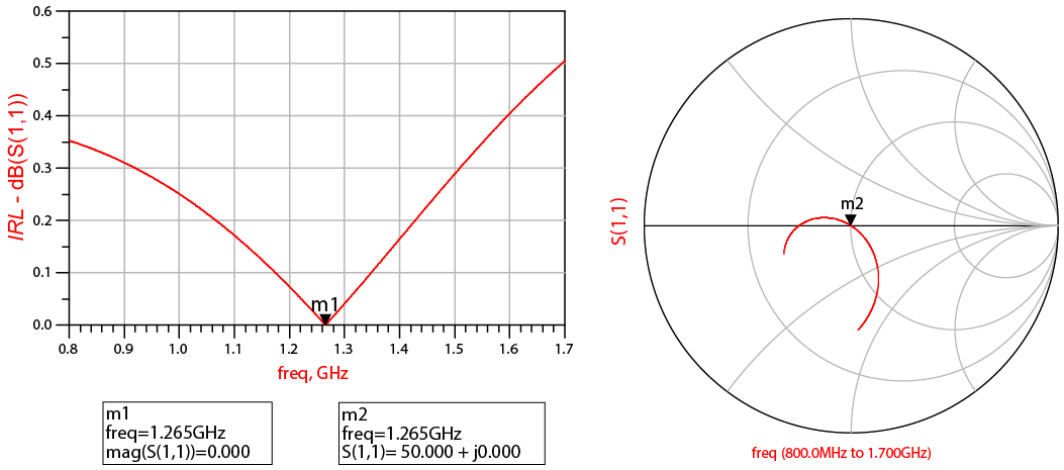


Figure 5.13: Simulation Results for Distributed Input Matching Network

The simulated results show that the input matching network provides a very good match by presenting the source with a 50 Ω impedance. When designing the output matching network, the transistor must be presented with an impedance of $15.281 - j3.394$ Ω. Using the same MATLAB code in Appendix A the following possible solutions for an output matching network were obtained.

```
Open circuit shunt stub:
Solution 1
Distance from load d: 0.43λ, 155.48 degrees, 68.95 mm, 2714.65 mills
Length of stub l:     0.36λ, 128.22 degrees, 56.86 mm, 2238.72 mills

Solution 2
Distance from load d: 0.09λ, 33.07 degrees, 14.67 mm, 577.37 mills
Length of stub l:     0.14λ, 51.78 degrees, 22.96 mm, 904.05 mills
Width of section l:   1.88 mm, 74.11 mills
```

The second option was selected because the physical dimensions are smaller than the first. Simulating the network in ADS, as shown Figure 5.15, confirms that the output matching network was accurately designed and that one can proceed to the next step in the amplifier design process.

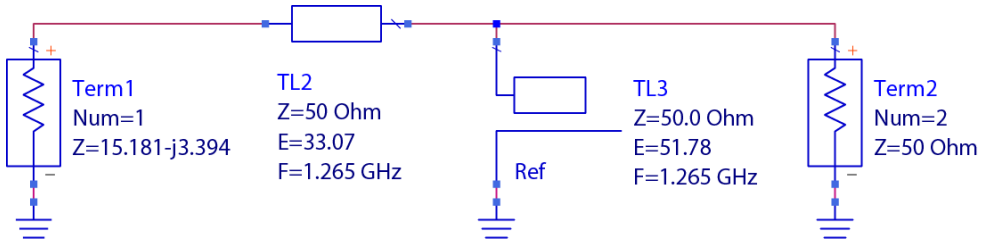


Figure 5.14: *S*-parameter Simulation for Distributed Output Matching Network

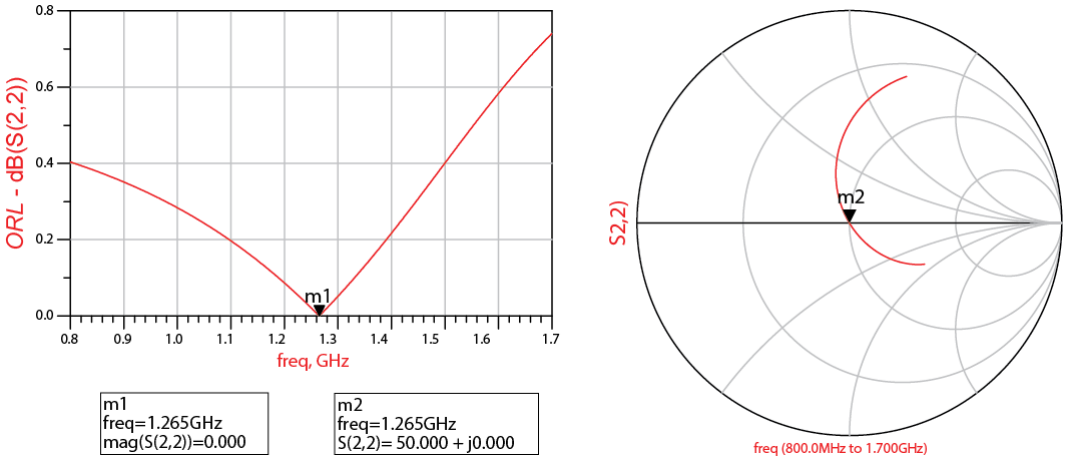


Figure 5.15: Simulation Results for Distributed Output Matching Network

After designing the matching networks an *S*-parameter simulation was done on the circuit with the active device, stabilisation resistor and matching networks in place, as shown in Figure 5.16.

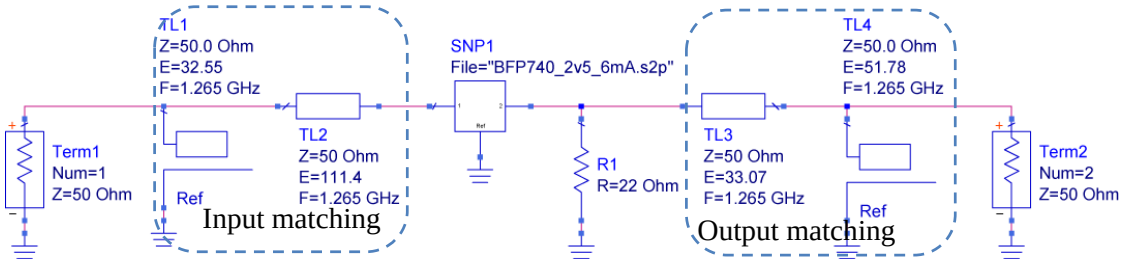


Figure 5.16: Amplifier with Distributed Element Matching Networks Implemented

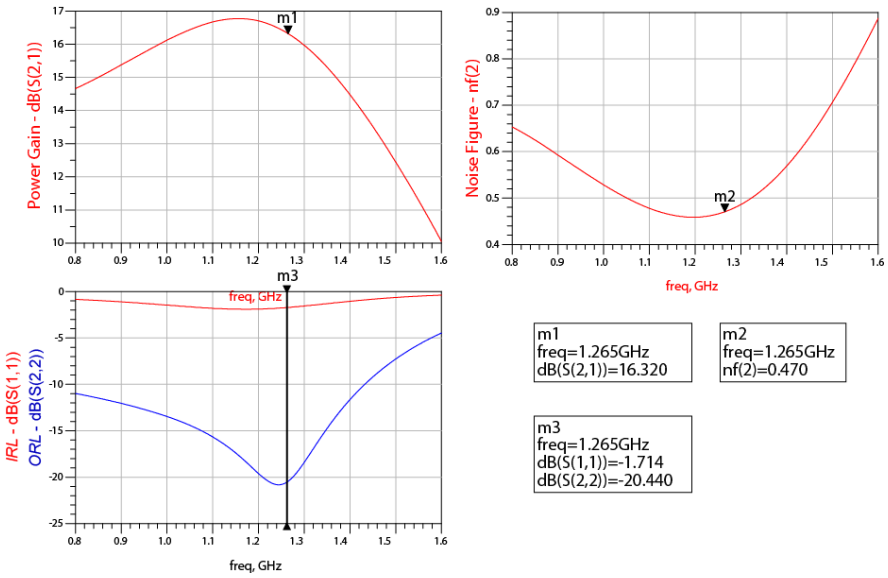


Figure 5.17: Initial Simulation Results of Distributed Matching Amplifier

Comparing the initial results of the lumped, Figure 5.11, and distributed, Figure 5.17, matching techniques indicates that the matching networks are accurately designed and the performance parameters of the amplifiers correlate well.

Up to this point of the design process the transistor model that was used was the linear model that contains the *S*-parameters from actual measurements of the active device done by the manufacturer over a range of frequencies and at a specific bias point. The simulation engine interpolates the simulation results from the data within the model. All components used in the simulations so far were ideal components, meaning that they do not account for any losses or parasitic elements which exist in the physical real world components that will be used to construct the final product.

5.6.3 DC Biasing

When simulating the DC biasing circuit the real world model of the active device must be used. It is called the Die Model and describes the electrical behaviour of the transistor die by a scalable, physics-based sub-circuit model (Versleijen, Bloem, van Steenwijk & Yanson, 2004). It comprises the microscopic components that make up the transistor such as lead inductances and capacitances. As mentioned in Section 3.15 the DC biasing network chosen for the design is a voltage feedback constant base current source configuration presented in Figure 5.18.

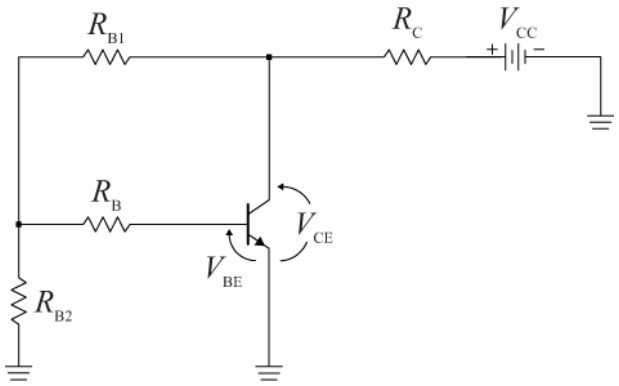


Figure 5.18: Voltage Feedback Constant Base Current Source Bias Circuit

The specifications require low power dissipation by the front end section, so a bias point that can deliver sufficient gain with a low enough noise figure will be chosen.

A bias point of V_{CE} = 2.5 V and I_C = 6 mA was chosen for the BFP740 active device. Since the manufacturer did not supply that specific bias configuration on the data sheet, a simulation in ADS was done to determine whether or not the device would operate in the linear region and to find the optimal value for the base current, I_B. The results of the simulation are shown in Figure 5.19.

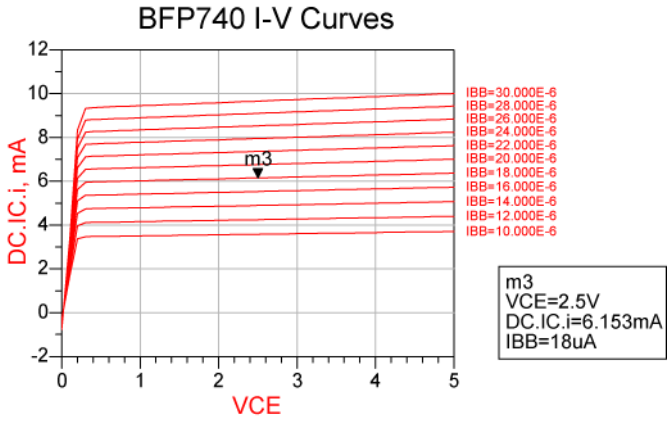


Figure 5.19: I-V curves with Associated Base Current for BFP740

The bias circuit was designed using the software application AppCAD from Agilent Technologies, and the calculated values were verified by performing a DC simulation in ADS, with the results presented in Figure 5.20. The bias network was designed so that resistor values from the standard E12 range could be used. From the simulation it can be seen that the DC biasing network was accurately designed and that simulated values for V_{CE} and I_C correlate well with the specifications and expected results. The correct operation of the DC bias network is of paramount importance because the *S*-parameters used for designing the matching networks are a function of the *Q*-point at which the transistor is biased; hence the values for V_{CE} and I_C should be as close as possible to the specified values.

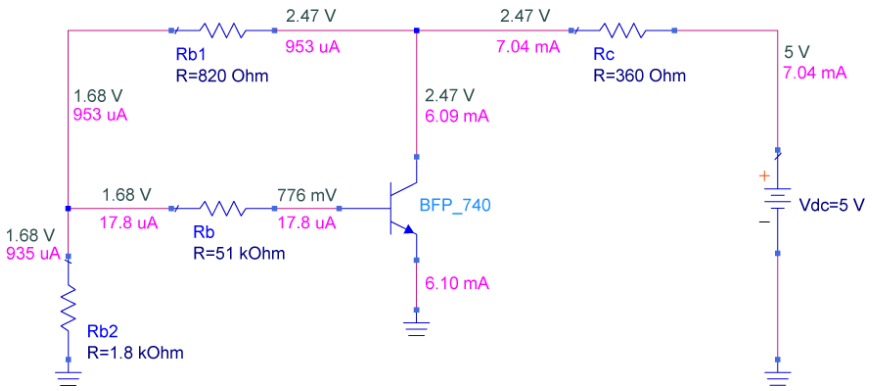


Figure 5.20: Completed DC Biasing Network

5.6.4 PCB Layout and Final Design

The next step in the design process is to integrate the matching networks and the bias circuit. One cannot simply couple the two circuits together. Good RF technique and practice is to ensure that the RF signals are de-coupled from the DC bias circuit and that the DC bias circuit does not affect the signal flow. Fortunately, as mentioned in Section 3.5 the topology of the L-matching networks for the lumped element matching circuit contributes towards solving the problem as well as minimising overall component count. In most cases inductors are placed as RF chokes on the input and output ports of the active device to prevent the AC signal from interfering with the bias circuit, while simultaneously supplying DC voltages to bias the transistor. If any signal should pass through the RF choke, a 1 nF bypass capacitor is placed on the bias network side of the choke to create a low impedance path to ground. For a capacitor to act as a bypass capacitor it must present an impedance of less than 1 Ω to the signal at the frequency of operation (Love & Ajluni, 2009:124). It is prudent to have a capacitor placed in series with the input and output ports of the transistor to provide for good AC coupling between stages and to block DC voltages from affecting the next stage or possibly damaging the expensive test equipment.

In Figure 5.21 the final schematic is shown with stabilising, matching and bias components in place. In the input matching network, consisting of C_1 and L_1, the inductor L_1 was "flipped" up to act as a RF choke while also coupling the DC base voltage to the base terminal. The capacitor C_1, in addition to performing the matching also acts as a DC block, thereby saving two extra components and minimising losses. The layout of the output matching network, C_2 and L_2, was not optimal for minimising the component count and an additional RF choke, L_{RFC}, calculated as 90 nH was inserted. The DC bias circuit is made up by R_C, R_{B1}, R_{B2} and R_{BB}. Remaining components are R_{stab}, the stabilising resistor, and C_3 and C_4, the bypass capacitors. The performance of the simulated amplifier is shown in Figure 5.22.

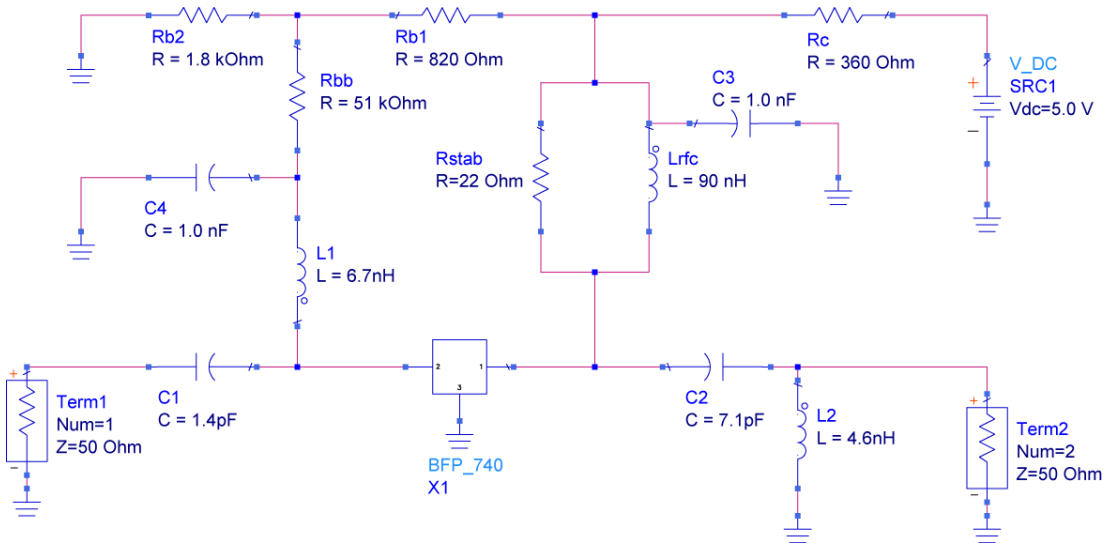


Figure 5.21: Schematic of Completed Lumped Element LNA

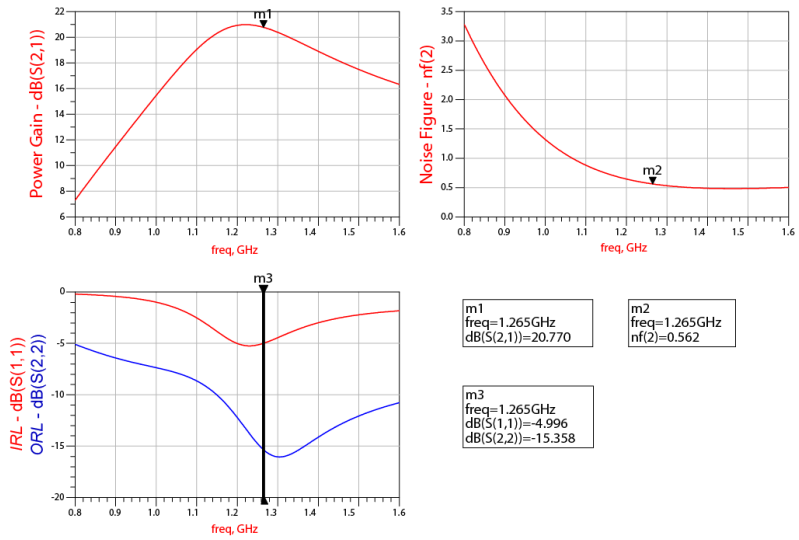


Figure 5.22: Simulated Results Using Ideal Lumped Component Matching Networks

From the simulation results in Figure 5.22 it can be seen that the performance parameters correlate well with the data sheet specifications as summarised in Table 5.2. The power gain is close to the maximum available gain obtainable from the active device under the current bias conditions. Also, the noise figure is close to the minimum value obtainable with this active device. The *ORL* indicates that relatively good matching was achieved at the output port, whereas the *IRL* achieved is the result of purposely mismatching the input port of the transistor for a low *NF*.

The simulated performance parameters in Figure 5.22 were achieved using ideal components, that is, components with an infinite *Q*. Also, the simulations did not take into account any losses of the actual printed circuit board tracks or any parasitic components which exist in the real world situation. To get a better understanding of the effects of actual practical components, the substrate used in the final

constructed amplifier, and to evaluate the resulting degradation in performance of the final product, all the components in the matching networks were replaced with their real world equivalent models. Similar to the models of the active devices, these components consist of actual *S*-parameter values which were measured at several points in the frequency spectrum to completely represent the behaviour of the physical components in the simulations prior to the construction of the physical circuit.

Moving one step closer to simulating the circuit as it would perform in the real world after it is constructed, the PCB substrate parameters for Rogers RO4003C as specified in the manufacturer's data sheet were also programmed into ADS and the tracks of the PCB that physically interconnect the components were inserted before simulation. The results indicated that the losses in the tracks and components alter the matching and hence degrade the performance of the circuit. In preparation for the final simulation, the PCB was laid out and set up so that an electromagnetic (EM) simulation could be performed on it. The layout program within ADS generates an *S*-parameter model of the PCB which completely characterises the particular substrate used. Finally the *S*-parameter model is imported into the EM method of moments simulation program and populated with actual models of the components and re-simulated. Figure 5.23 shows the layout model of the PCB and setup for the final method of moments (Momentum) simulation.

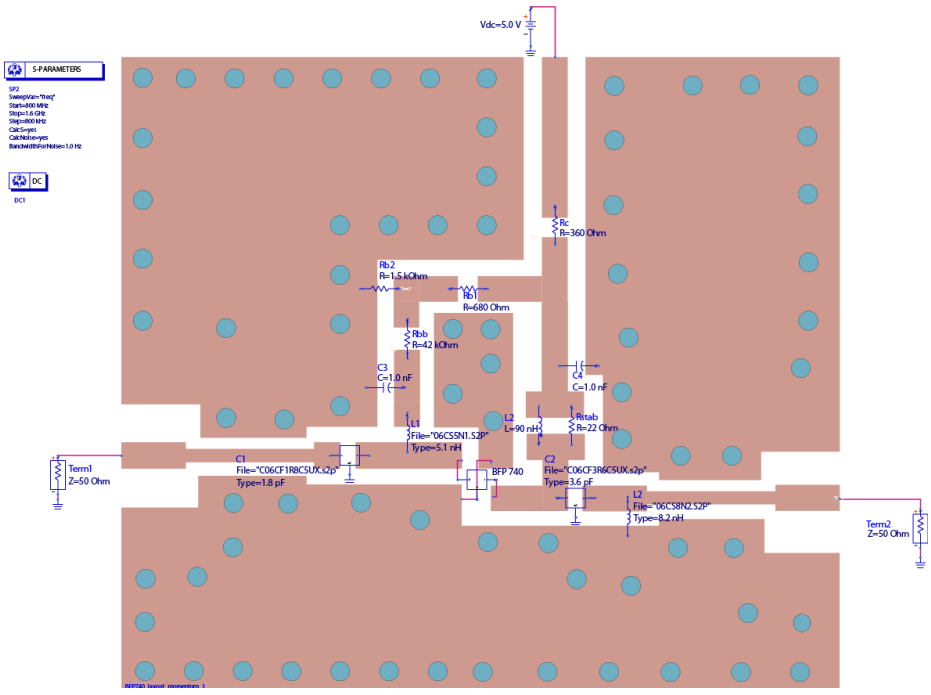


Figure 5.23: ADS Momentum EM Simulation Setup

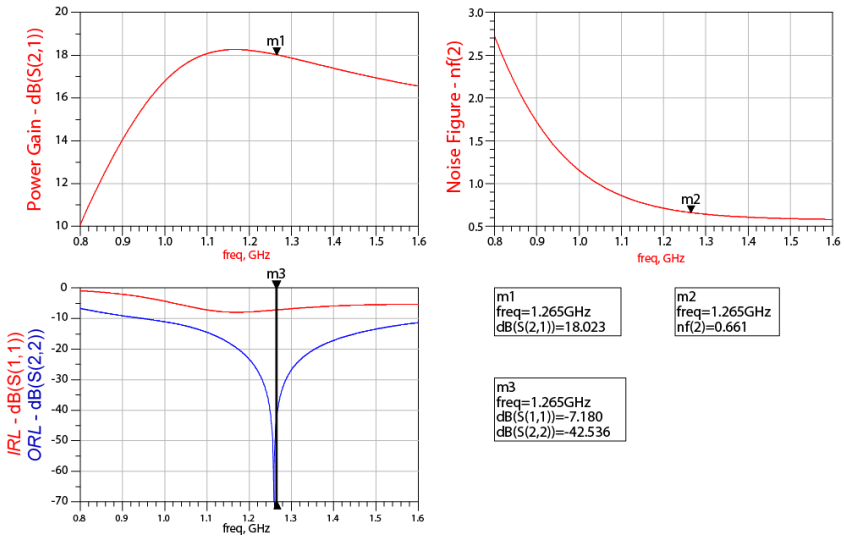


Figure 5.24: Results from Momentum Simulation

The performance parameters obtained from the EM simulations are shown in Figure 5.24 and the performance parameters of the amplifier are clearly degraded from the previous ideal world simulations of the LNA. As expected, the power gain and *NF* is slightly poorer however an improved *IRL* was achieved given that the *IRL* was intentionally degraded for a better noise performance. An excellent output match was achieved as indicated by the very low *ORL* of just below 43 dB. The degradation in power gain and noise performance was expected and is due to the use of real world models of the actual components and losses within the substrate which are now included in the simulation. Component values have to be adjusted for optimum performance in the EM simulation, and the difference in component values used in the ideal and EM simulations is listed in Table 5.2.

Table 5.3: Comparison of Components between Ideal and EM Simulations

Component and Description	Ideal Simulation value	EM Simulation Value
Active device (BFP740)	N/A	N/A
Biasing Resistor (R_C)	360 Ω	360 Ω
Biasing Resistor (R_{B1})	680 Ω	680 Ω
Biasing Resistor (R_{B2})	1.5 kΩ	1.5 kΩ
Biasing Resistor (R_{BB})	42 kΩ	42 kΩ
Stabilising Resistor (R_{stab})	22 Ω	22 Ω
Input Match Capacitor (C_1)	1.4 pF	1.8 pF
Output Match Capacitor (C_2)	7.1 pF	3.6 pF
Decoupling (C_3, C_4)	1 nF	1 nF
Input Match Inductor (L_1)	6.7 nH	5.1 nH
Output Match Inductor (L_2)	4.6 nH	8.2 nH
DC Feed (L_3)	90 nH	90 nH

From Table 5.3 it can be observed that all of the DC bias components were unchanged and operate as expected together with the DC blocking, decoupling capacitors and the DC feed inductor. However, the values of the matching components had to be adjusted. Small changes were made to get the same results for the *IRL* in the Momentum EM simulation and the ideal simulation. Larger adjustments were made to the components in the output matching network to get the lowest possible value for the *ORL* in both simulations. Clearly the behaviour of the substrate necessitated these component value adjustments and this is the reason why it is important to use an EM simulation platform such as Momentum to make sure that the LNA performs optimally when it is physically constructed.

The schematic diagram of the distributed element amplifier using the BFP740 is shown in Figure 5.25. The design is fairly similar to that of the lumped element LNA but since the matching networks were implemented in transmission lines, it was necessary to add specific capacitors and inductors at the input and output ports of the transistor. The capacitors were added to perform the function of AC coupling and DC blocking, while the inductors act as radio frequency chokes and couple the DC power to the bias circuit.

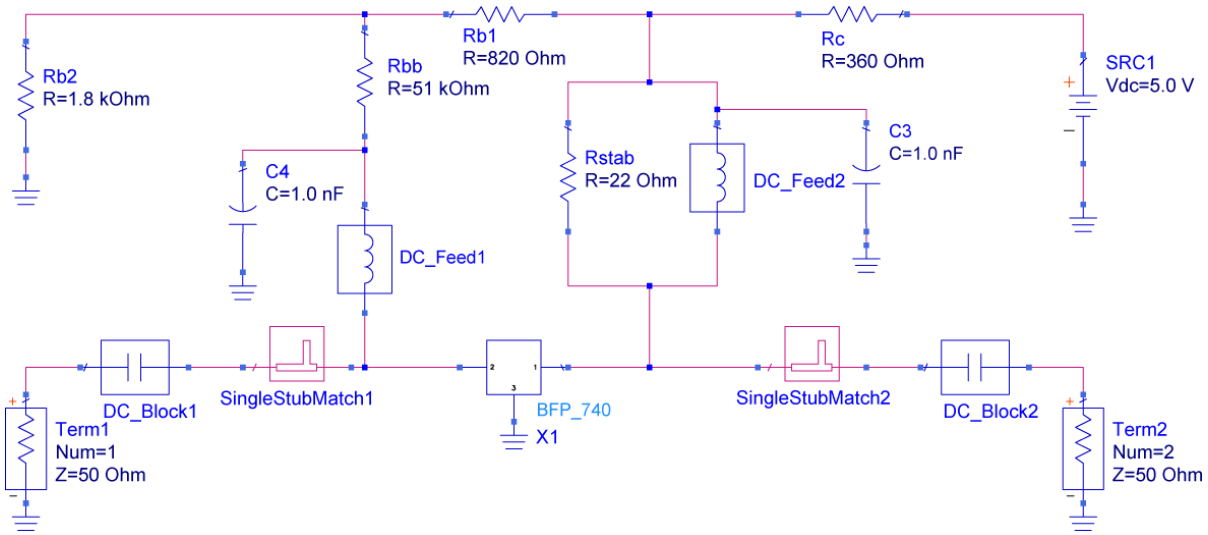


Figure 5.25: Schematic of Completed Distributed Element LNA

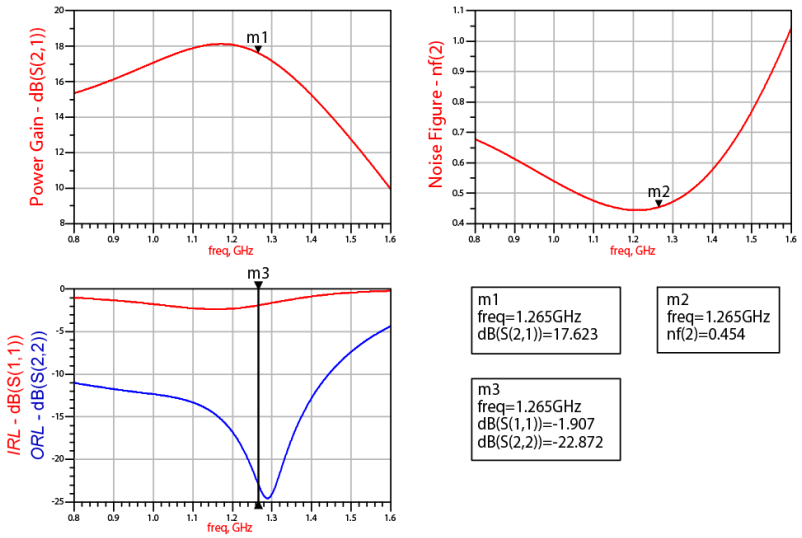


Figure 5.26: Results of Completed Distributed Element LNA

The simulated performance parameters correlate well with those of the lumped element LNA with minor differences in *IRL*, *ORL*, *NF* and gain. All of these performance parameters met the required specifications.

For the momentum EM simulation the ideal stub matching components were replaced with their calculated distributed components, and implemented in the form of microstrip transmission lines. The physical topology of the LNA was designed in the Layout program within ADS where, the properties of the Rogers 4003 substrate were programmed into the simulation engine and an *S*-parameter model of the PCB was generated for use in Momentum. Figure 5.27 shows the completed printed circuit board layout of the distributed element LNA using the BFP740 device. The performance parameters are shown in Figure 5.28.

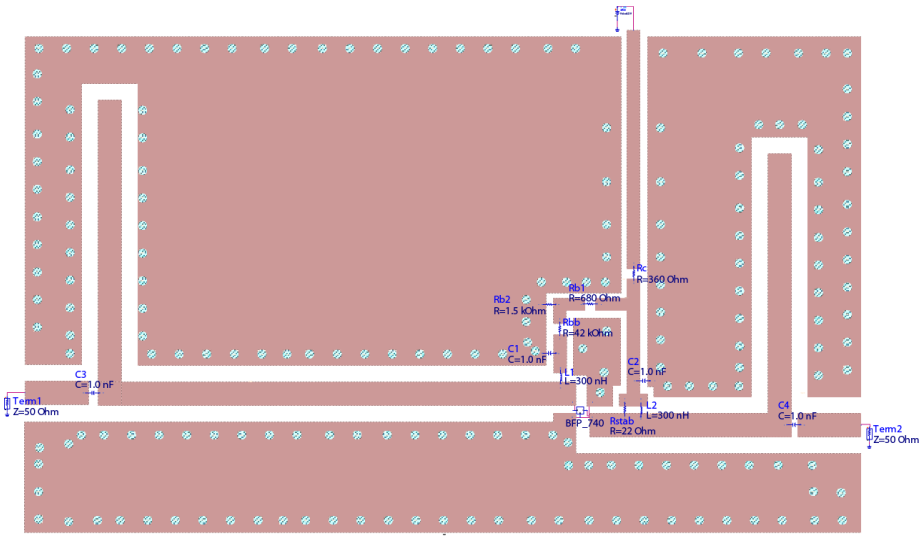


Figure 5.27: ADS Momentum EM Simulation Setup

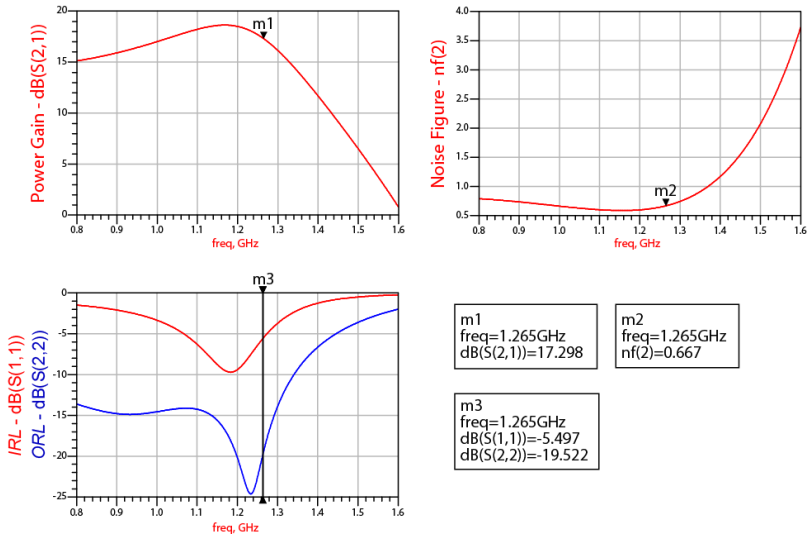


Figure 5.28: Results from Momentum EM Simulation

These results correlate well with those of the previous ideal simulation and meet the specified requirements. The influence of the actual Rogers RO4000C substrate is evident and the widths and lengths of the matching networks had to be adjusted for optimum performance.

One less component was used than on the lumped element equivalent LNA because the matching networks were implemented using series and shunt sections of transmission lines. However, DC blocking and AC coupling capacitors had to be used on the input and output ports of the LNA. These components prevented any DC voltages from being present at the actual connectors and thereby causing possible damage to equipment connected to these ports. Radio frequency chokes (RFC's) were placed on the input and output ports of the active device to stop high frequency signals from flowing through the bias circuitry and DC supply. Table 5.4 lists and describes all the components in the circuit.

Table 5.4: List of Components Used for the Distributed Amplifier Design

Component and Description	Ideal Simulation Value	EM Simulation Value
Active device (BFP740)	N/A	N/A
Biasing Resistor (R_C)	360 Ω	360 Ω
Biasing Resistor (R_{B1})	680 Ω	680 Ω
Biasing Resistor (R_{B2})	1.5 kΩ	1.5 kΩ
Biasing Resistor (R_{BB})	42 kΩ	42 kΩ
Decoupling (C_1, C_2)	1.4 pF	1.4 pF
Coupling/ DC block (C_3, C_4)	1 nF	1 nF
Radio Frequency Choke (L_1, L_1)	300 nH	300 nH
Input Matching	d = 49.41 mm w = 1.88 mm l = 14.43 mm	d = 39.2 mm w = 1.88 mm l = 24.2 mm
Output Matching	d = 14.67 mm w = 1.88 mm l = 22.96 mm	d = 16.35 mm w = 1.88 mm l = 22.73 mm

5.6.5 Non-linear Performance

The final step in the design of the LNA involved evaluating the non-linear performance of the amplifier. Figure 5.29 illustrates the simulation setup for measuring the 1 dB compression point (P_{1dB}) of the LNA with the results shown in Figure 5.29. The main objective of the research was to design an LNA with the best possible noise performance and as a result the non-linear performance parameters, such as the P_{1dB} and the third order intercept (IP_3) points were compromised. However, the dynamic range of an LNA is a function of the P_{1dB} point and the minimum detectable signal level. The P_{1dB} measurements will be used to determine the dynamic range of the LNA.

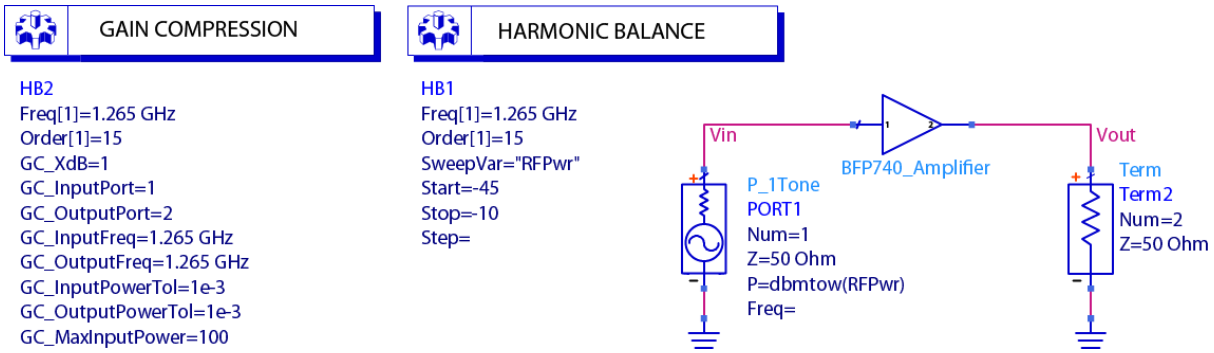


Figure 5.29: Setup for 1dB Compression Point (P_{1dB}) Simulation

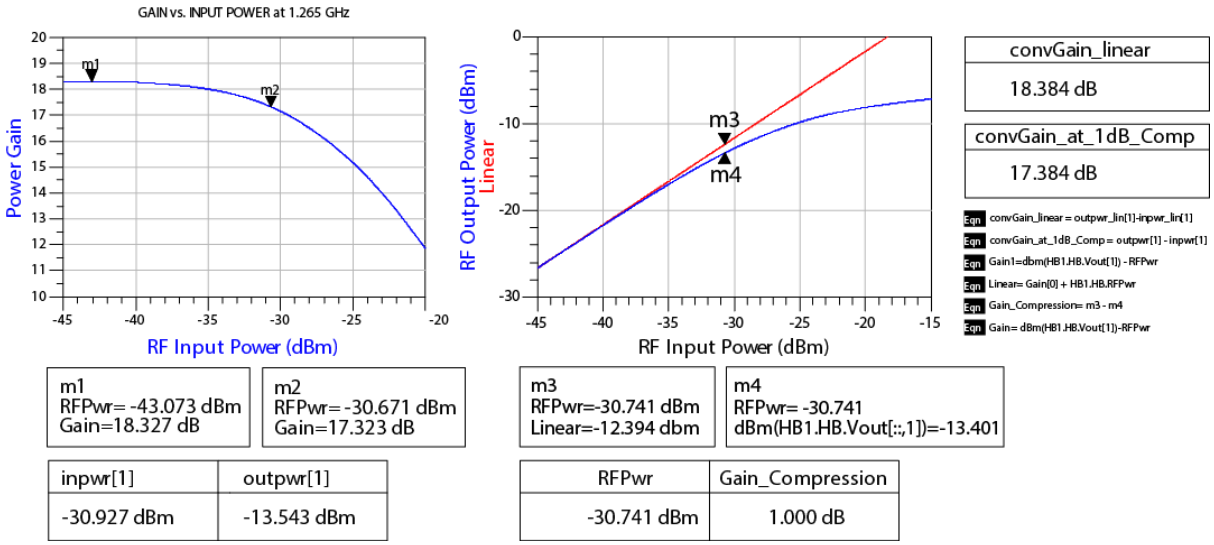


Figure 5.30: Results for 1 dB Compression Point Simulation

The results illustrated in Figure 5.30, show that the IP_{1dB} is at −30.927 dBm and the OP_{1dB} is equal to −13.543 dBm. The reason that these parameters are lower compared to power amplifiers or amplifiers designed for maximum available gain such as in the *IF* stages of radio receivers was described in Section 3.7. The non-linear performance of an amplifier is largely determined by the amount of collector current, and since the LNA was designed for a minimum *NF*, which required a collector current which is as low as possible, the linearity performance of the LNA is compromised. However, what the simulated OP_{1db} does provide is the maximum output power obtainable from the LNA before it goes into compression. Lastly, the IP_3 point was simulated and the setup is shown in Figure 5.31.

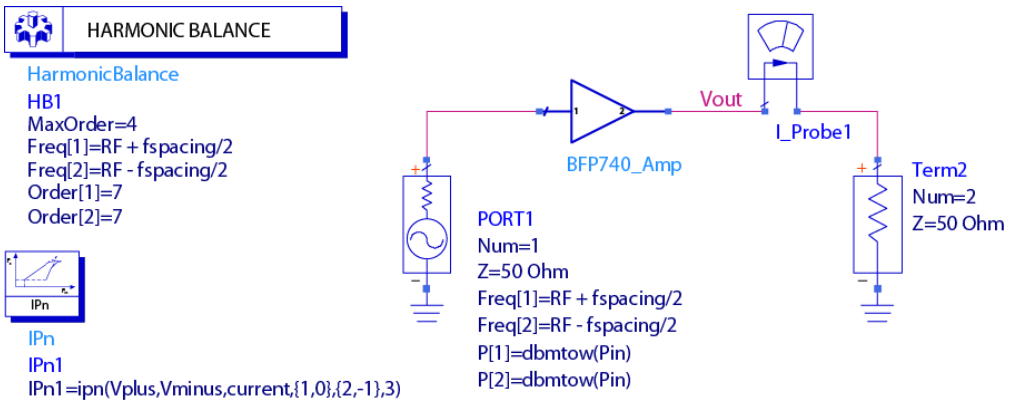
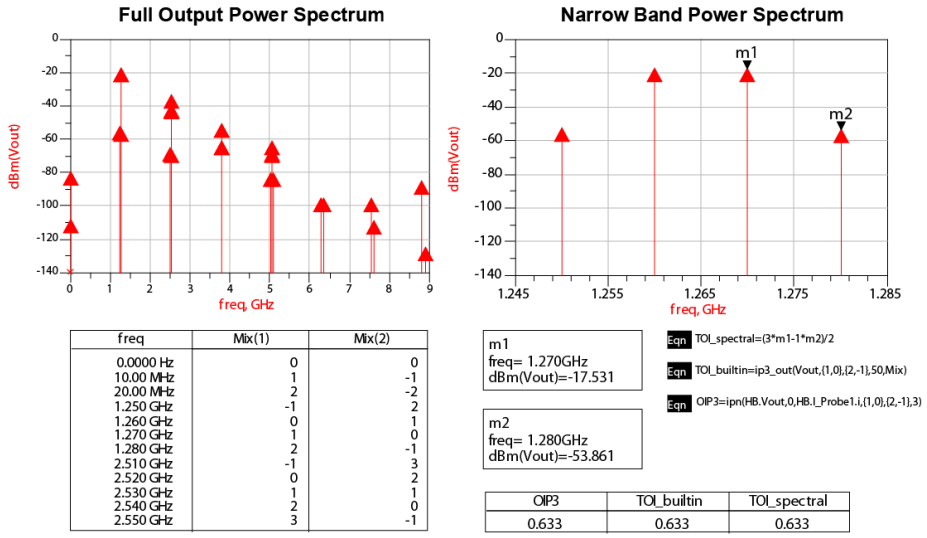


Figure 5.31: Third Order Intercept Point Simulation Setup

The results are illustrated in Figure 5.32. To calculate the output third order intercept point (OIP_3), Equation 3.20 was used and programmed into the simulation engine. To validate the correctness thereof, this calculated value was compared to the built in IP_3 function of the software package. Another method was also used where V_{out} was the signal voltage at the output port of the LNA, $\{1, 0\}$ and $\{2, -1\}$ specify

the harmonic frequencies for the fundamental and the intermodulation spectral components respectively. The OIP_3 was calculated as 0.633 dBm.



freq	Mix(1)	Mix(2)
0.0000 Hz	0	0
10.00 MHz	1	-1
20.00 MHz	2	-2
1.250 GHz	-1	2
1.260 GHz	0	1
1.270 GHz	1	0
1.280 GHz	2	-1
2.510 GHz	-1	3
2.520 GHz	0	2
2.530 GHz	1	1
2.540 GHz	2	0
2.550 GHz	3	-1

OIP3	TOI_builtin	TOI_spectral
0.633	0.633	0.633

Figure 5.32: Third Order Intercept Point Simulation Results

A brief summary of the simulated performance parameters for the LNAs using the BFP740 active device are listed in Table 5.5.

Table 5.5: Summary of Simulated Performance Parameters for BFP740 LNAs

	NF	Gain	*IRL*	*ORL*	IP_{1dB}	OP_{1dB}	OIP_3
Lumped	0.661 dB	18.023 dB	−7.180 dB	−42.530 dB	−30.740 dBm	−13.540 dBm	0.633 dBm
Distributed	0.667 dB	17.298 dB	−5.490 dB	−19.520 dB	−32.240 dBm	−14.750 dBm	0.350 dBm

This comparison indicates that there is little difference in the performance of the lumped and distributed versions of the LNA.

5.7 ATF-55143 Amplifier Design

Avago Technologies' new ATF-55143 is a low noise enhancement mode pseudomorphic HEMT that combines the possibility of high gain, high linearity and low noise figure all into a single active device. This device is ideal for LNAs used in mobile communications (Avago Technologies, 2008:1). The process that was followed in the design of this LNA is exactly the same as for the previous LNAs which used the BFP-740. Hence, the design process will not be presented in as much detail as this will result in mundane repetitiveness. The steps listed in Section 5.2 were followed in the design process for this ATF-55143 LNA.

5.7.1 Stabilising the Active Device

The initial simulation of the ATF-55143 active device by itself at the design frequency shows that the device is unstable and needs to be stabilised before it can be used in the circuit. The simulation to verify the stability factor of the active device is illustrated in Figure 5.33 with the relevant results in Figure 5.34.

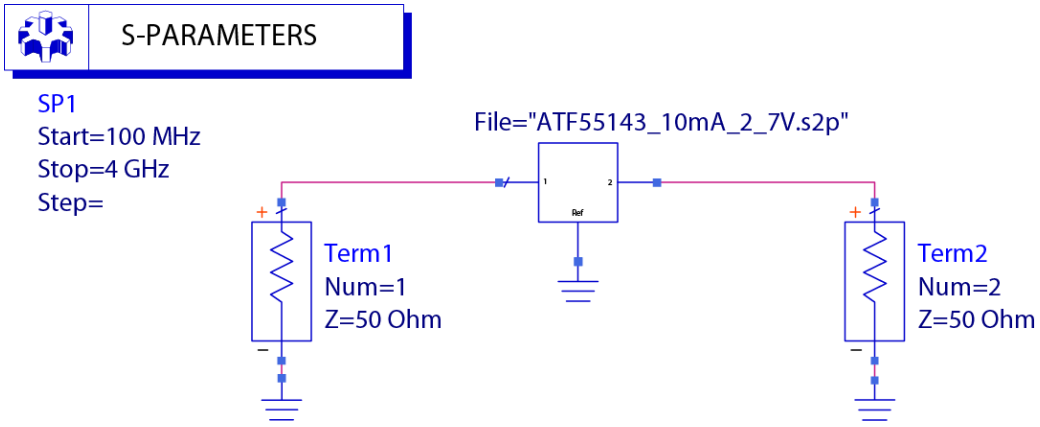


Figure 5.33: Simulation Setup to Determine Stability of Active Device

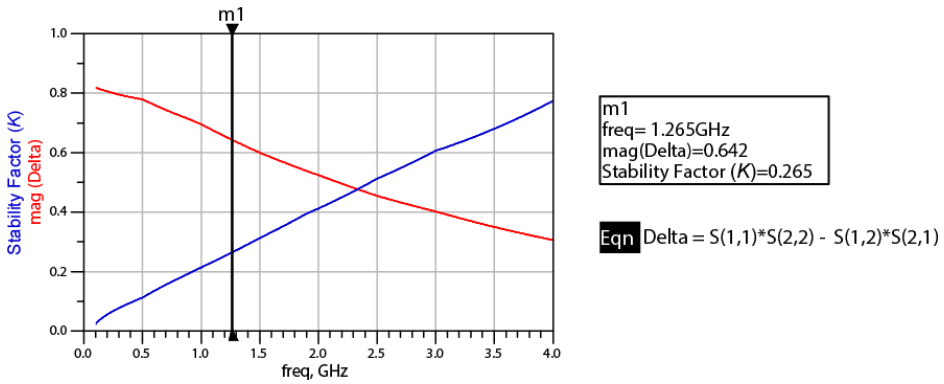


Figure 5.34: Stability Factor Results for ATF-55143 Active Device by Itself

From the results in Figure 5.34 it is clear that the active device is unstable for the entire frequency spectrum. The active device may oscillate for specific load and source terminations and this possibility must be prevented from occurring. The process described in Section 3.10 was followed to stabilise the active device and it was decided to place a resistor in parallel with the output port of the ATF-55143. ADS was used to evaluate the stability of the active device by sweeping the value of the stabilising resistor. The ADS simulation setup is shown is Figure 5.35 and the effect on the stability criteria is illustrated in Figure 5.36.

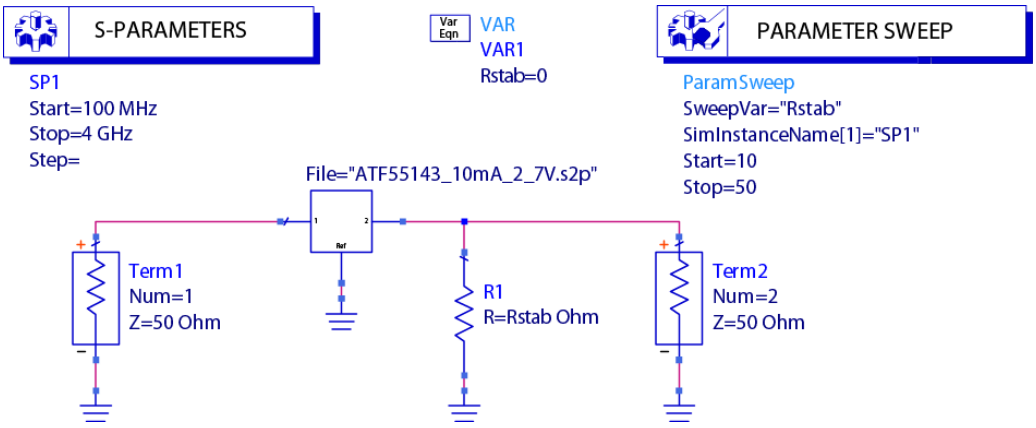


Figure 5.35: Stabilising the Active Device

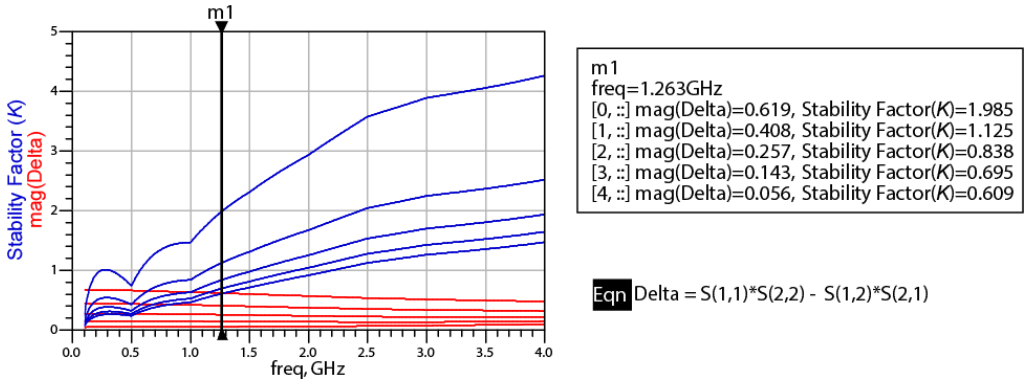
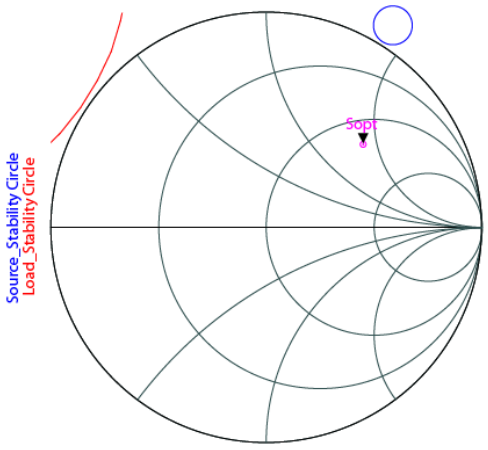


Figure 5.36: Stability Criteria for Swept Values of Stabilising Resistor

Equation 3.19 specifies that $|\Delta|$ (magnitude of delta) must be less than one and the Rollet stability factor (K) greater than one. It was found that a 22 Ω resistor satisfies Equation 3.19 to stabilise the active device as illustrated in Figure 5.36. In order to verify the stability of the stabilised active device, re-interpolated S-parameters were generated in ADS and then load and source stability circles were plotted on a Smith chart as illustrated in Figure 5.37. Figure 5.37 clearly shows that both the source and the load stability circles are off the Smith chart which means that any value of impedance can be selected to terminate the active device in and it will not oscillate. That is, Figure 5.37 confirms unconditional stability of the active device. Once the active device is unconditionally stable the matching networks can be designed.



freq	S(1,1)	S(1,2)	S(2,1)	S(2,2)	Sopt
1.265 GHz	0.906 / -60.014	0.019 / 58.459	3.145 / 134.491	0.436 / -172.357	0.593 / 40.615

Figure 5.37: Re-interpolated *S*-Parameters from Unconditionally Stable Device

5.7.2 Design of Matching Networks

For best noise performance, the input port of the active device must be terminated in a value of Γ_{opt} (denoted Sopt in Figure 5.37), hence the input matching network must match Γ_{opt} to 50 Ω. Using the facts illustrated in Figure 5.7 and substituting the corresponding values into Equation 3.6, Γ_o was calculated to be $0.498\angle -168.941$. By using Equations 3.26 through to 3.35 the component values for the matching networks were obtained. The values and networks were verified using the software program *L-Net* and are illustrated in Figures 5.38 and 5.39.

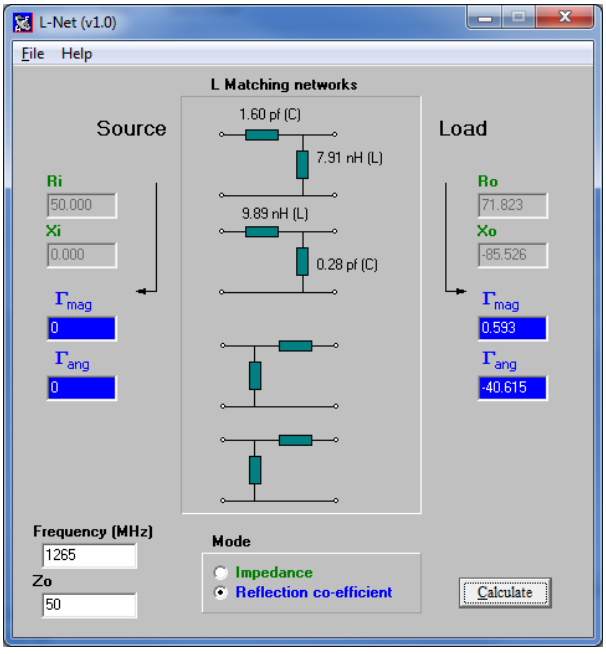


Figure 5.38 Possible Input Matching Networks for ATF-55143 Active Device

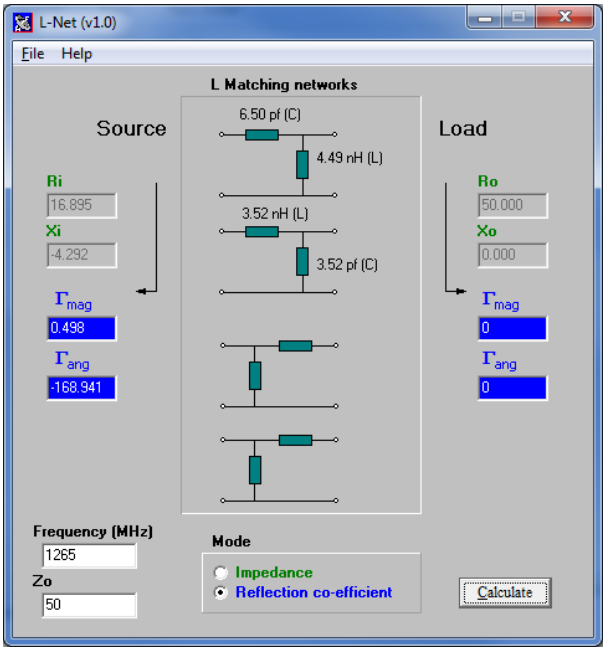


Figure 5.39: Possible Output Matching Networks for ATF-55143 Active Device

From each one of Figures 5.38 and 5.39 the matching network with the series capacitor was selected as it is the optimum topology in that it allows for a minimum component count and for simplifying the circuit layout. Simulations in ADS, as shown in Figure 5.40, were used to verify the accuracy of the matching network design. The simulated parameters for Gain, *IRL*, *ORL* and *NF* are shown in Figure 5.41.

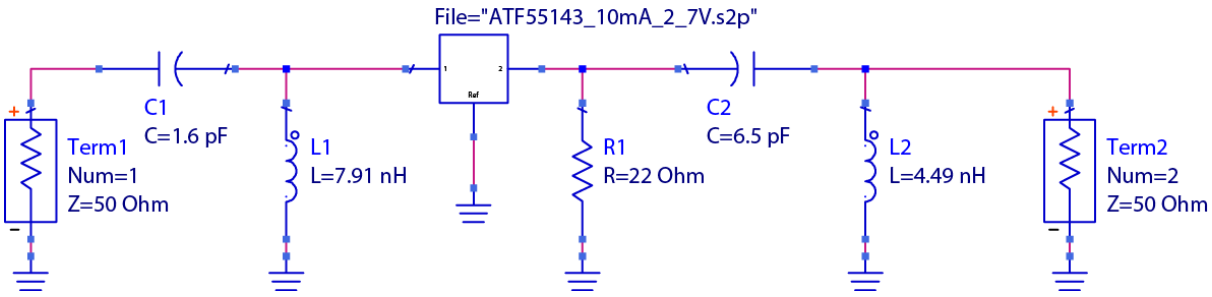


Figure 5.40: Setup for Simulating Matching networks

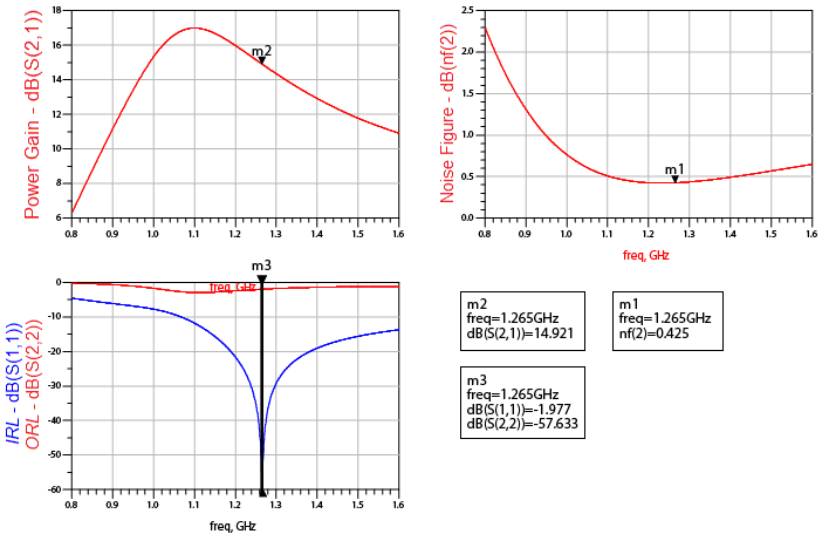


Figure 5.41: Simulated Results for Design of Matching Networks

The preliminary results shown in Figure 5.41 indicate that a good noise figure of 0.425 dB and almost 15 dB power gain can be expected from the LNA. The next step in the process is to design the DC bias network for this ATF-55143 active device.

5.7.3 DC Biasing

In general, FET RF devices are biased using 2 power sources or a single power supply with bipolar voltage settings. The other alternative is to use a self-biasing circuit as explained in Section 3.15, but using this technique always compromises the performance slightly. New PHEMT technology enables the ATF-55143 to be biased using a single power supply and the bias network is similar to that of the BJT devices (Avago Technologies, 2010:1).

The device will be biased for V_{DS} = 2.7 V and I_D = 10 mA. The performance parameters given in the manufacturer's datasheet indicate that one can expect a *NF* of approximately 0.6 dB and good linearity with a OIP_3 exceeding 20 dBm. Figure 5.42 illustrates the DC bias circuit suggested in the ATF-55143 application note from the manufacturer.

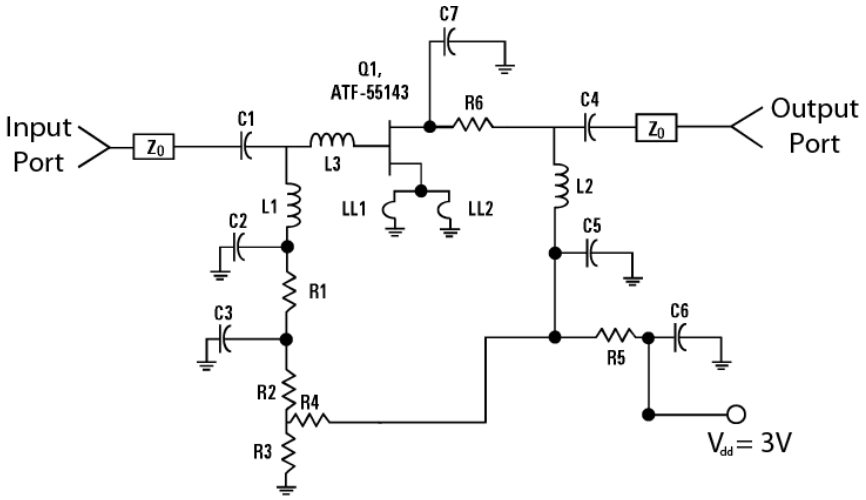


Figure 5.42: Suggested Bias Circuit for the ATF-55143 Active Device (Avago Technologies, 2010:2)

From Figure 5.42 the DC bias circuit is comprised of R_5, R_4, R_3 and R_2. For simulation and evaluation purposes all of the AC components were removed so that only the DC bias circuit remained and the values for the components were calculated. The biasing of the active device is achieved by the voltage divider circuit of R_4 and R_3. The drain current is prevented from fluctuating by a type of feedback circuit, in which the voltage of the divider is derived from the drain voltage. R_2 and R_1 combine to provide current limiting for devices using enhancement mode. This prevents the gate current from driving the device into saturation or compression. The bias circuit component values were calculated as follows:

$$R_3 = \frac{V_{gs}}{I_{BB}} \qquad \Omega$$

$$R_4 = \frac{\left(V_{ds} - V_{gs}\right) \times R_3}{V_{gs}} \qquad \Omega$$

$$R_5 = \frac{V_{DD} - V_{ds}}{I_{ds} - I_{BB}} \qquad \Omega$$

I_{BB}, the current flowing through the R_4, R_3 divider network was chosen as 0.5 mA (at least ten times the maximum expected gate leakage current). The DC biasing network with the calculated resistor values is illustrated in Figure 5.43.

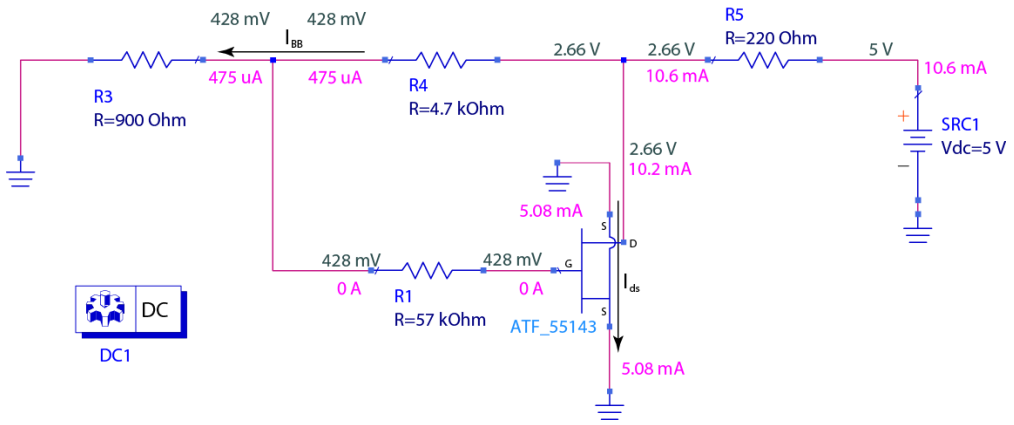


Figure 5.43: DC Bias Network with Simulated I_{DS} and V_{DS}

Once the active device is biased at the specified quiescent point the next step in the design process is to integrate the AC and DC sections of the amplifier.

5.7.4 Final Integrated LNA and PCB Layout

The final step in designing the LNA is to combine the matching networks, the active device and the bias network. Since the bias network for this ATF-55143 FET is the same as that used for a BJT, the same process will be followed when combining the AC and DC sections of the LNA. The inductor of the input matching network, L_1, was "flipped up" and connected to AC ground via bypass capacitor C_4. L_1 also serves as a RFC as well as acting as a DC feed for the gate bias voltage. R_{stab} was also flipped up in parallel with a RFC, the junction of which is shorted to ground by the bypass capacitor C_3. This eliminated the necessity of placing a DC blocking capacitor in series with R_{stab} to prevent it from affecting the bias voltages. The final designed schematic is illustrated in Figure 5.44.

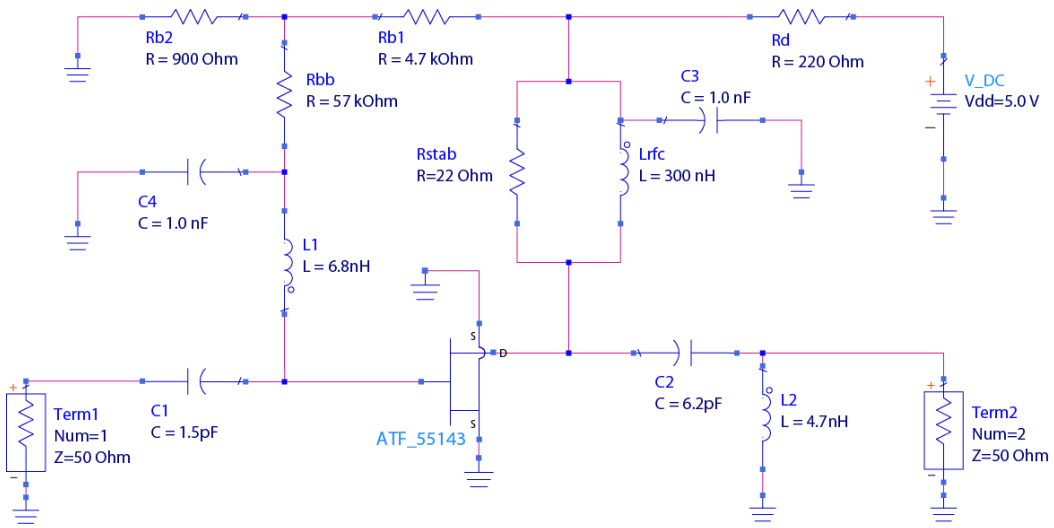


Figure 5.44: Final Schematic of Completed ATF-55143 Amplifier

The ideal components used in the initial amplifier circuit were replaced with their closest equivalent-value real-world models before doing the final simulation and PCB layout. The results of the simulation are illustrated in Figure 5.45.

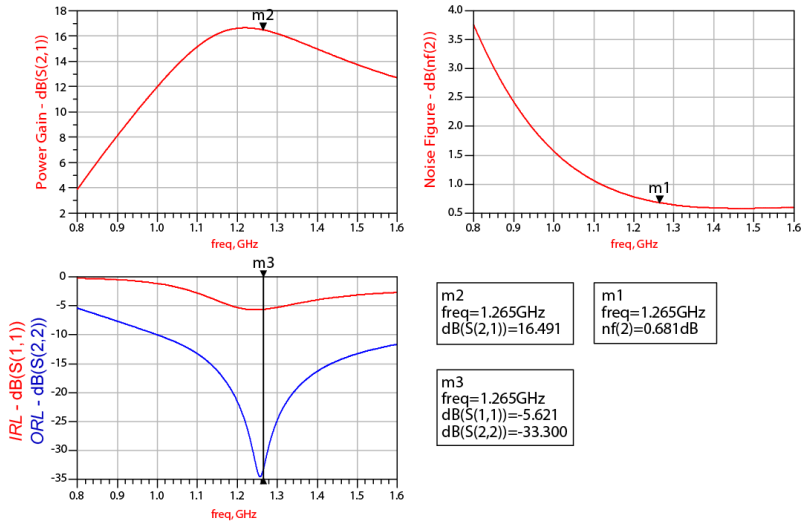


Figure 5.45: Simulated Results of LNA With Real World Lumped Components

The results are as expected and correlate well with those shown in Figure 5.41 of the simulation which uses ideal components to implement the matching networks. The power gain has increased by ±1.5 dB and noise figure has deteriorated slightly, by 0.2 dB, which is still significantly less than the minimum noise figure specified in the requirements. The *ORL* is at the minimum point of the curve, –33.3 dB, indicating that the output matching network is accurately designed and that maximum power is transferred into the load. As expected, the *IRL* indicates a sub-optimum match, however, in the design of a LNA an *IRL* of 5 dB is considered more than acceptable.

Once the performance of the LNA is verified the actual PCB layout can be done. For the final simulation of the current circuit, the PCB layout of the completed ATF-55143 LNA was implemented with real world components and, to achieve even more accurate results, an EM model of the PCB layout was generated. The completed LNA is shown in Figure 5.46 with the results in Figure 5.47.

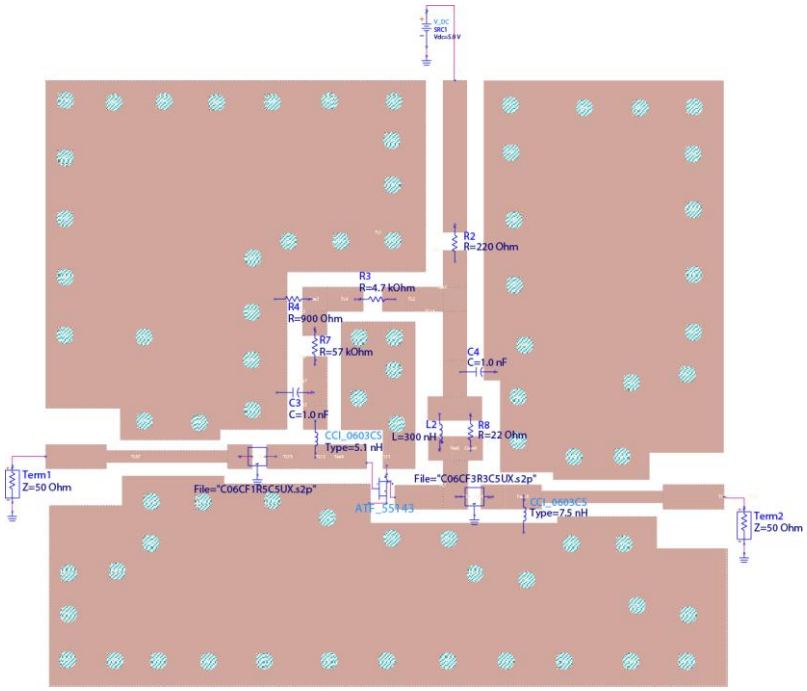


Figure 5.46: Momentum EM Simulation Setup of Completed ATF-55143 LNA

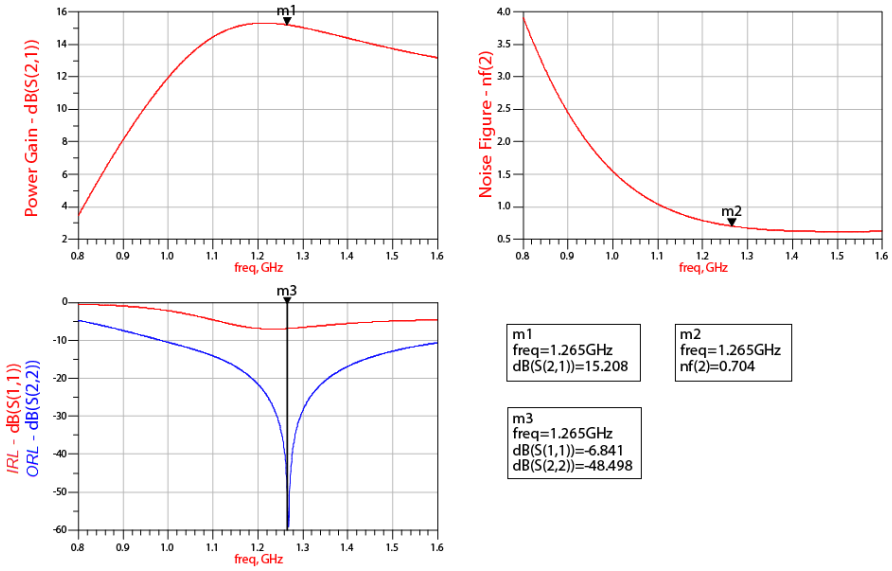


Figure 5.47: Momentum EM Simulation Results of Completed ATF-55143 LNA

Figure 5.47 confirms that the amplifier was optimally designed, showing outstanding performance which correlates well with the results from the initial ideal circuit simulations. As expected, when changing from simulations using ideal components to the Momentum simulation using real world components, the performance parameters are slightly degraded but are still well within the design specifications. The simulated results for this ATF55143 FET clearly indicate a good match at the output port with an *ORL* of 48.5 dB, and a fair match achieved at the input port with an *IRL* of almost 7 dB. The power gain, *ORL*, and *NF* performances are slightly lower when compared to initial simulations of the ATF55143 amplifier.

Table 5.6: Comparison of Components Between Ideal and Real-World Simulations

Component and Description	Ideal Simulation value	EM Simulation Value
Active device (ATF55143)	N/A	N/A
Biasing Resistor (R_D)	220 Ω	220 Ω
Biasing Resistor (R_{B1})	4.7 kΩ	4.7 kΩ
Biasing Resistor (R_{B2})	900 kΩ	900 kΩ
Biasing Resistor (R_{BB})	57 kΩ	57 kΩ
Stabilising Resistor (R_{stab})	22 Ω	22 Ω
Input Match Capacitor (C_1)	1.6 pF	1.5 pF
Output Match Capacitor (C_2)	6.2 pF	3.3 pF
Decoupling (C_3, C_4)	1 nF	1 nF
Input Match Inductor (L_1)	6.7 nH	5.1 nH
Output Match Inductor (L_2)	4.7 nH	7.5 nH
DC Feed (L_{rfc})	300 nH	300 nH

From Table 5.6 it can be observed that the values of all the biasing and DC related components remained unchanged in both types of simulations. The only components in the circuit with a noticeable change in value from the ideal to EM simulation were those in the output matching network. Clearly, these component changes were necessary for optimum performance, and are due to the Momentum simulations taking into account the parasitic effects of the actual substrate material used in the LNA.

5.7.5 Non-linear Performance

For the final section of the ATF-55143 amplifier design the P_{1dB} and IP_3 simulations are performed and the results discussed. These parameters do not play such an important role as does the *NF* of the amplifier but form part of the specifications and must be listed to characterise this specific amplifier and to determine the dynamic range of the LNA. The P_{1dB} simulation setup and the corresponding results are illustrated in Figure 5.48 and Figure 5.49 respectively.

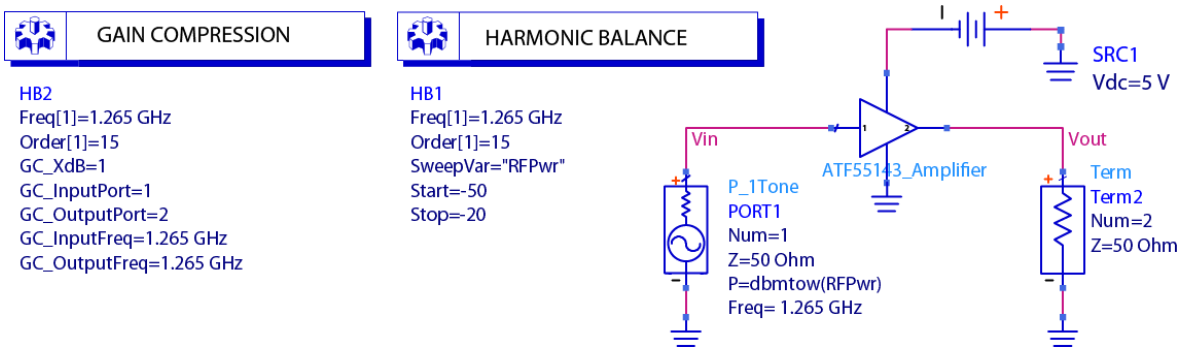


Figure 5.48: Setup for 1dB Compression Point (P_{1dB}) Simulation

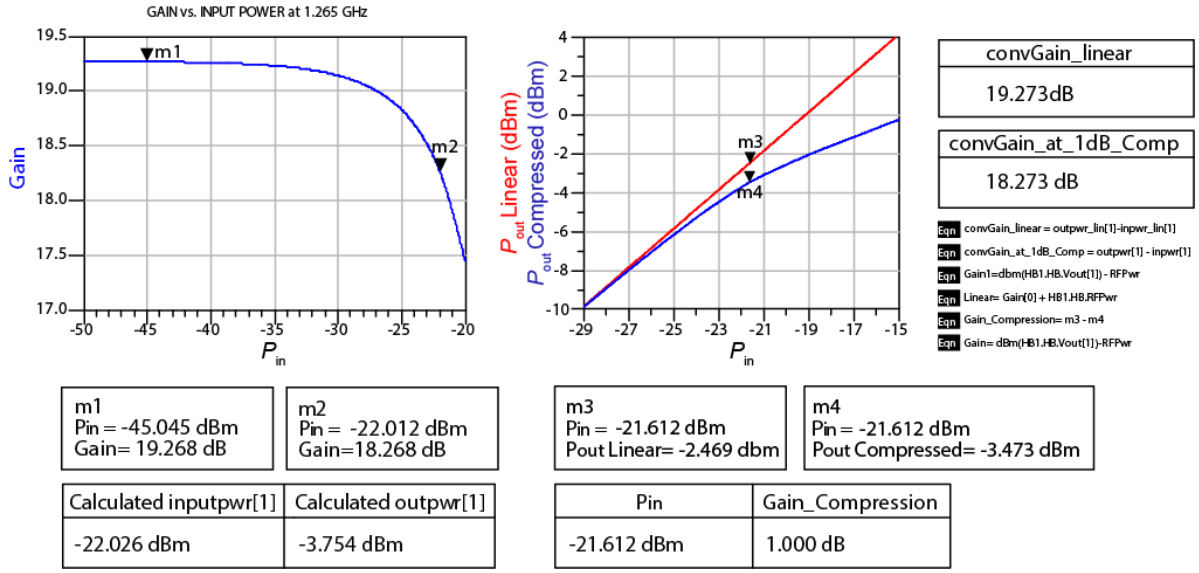


Figure 5.49: Results for 1 dB Compression Point simulation

From the simulated results illustrated in Figure 5.49, the IP_{1dB} is at −22.026 dBm and the OP_{1dB} is at −3.754 dBm. The simulation setup for the IP_3 point is illustrated in Figure 5.50 with the corresponding results in Figure 5.51.

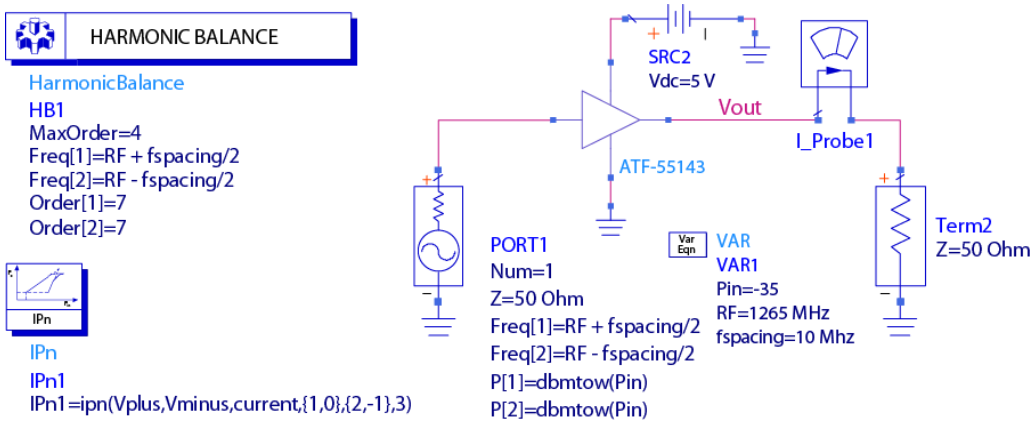
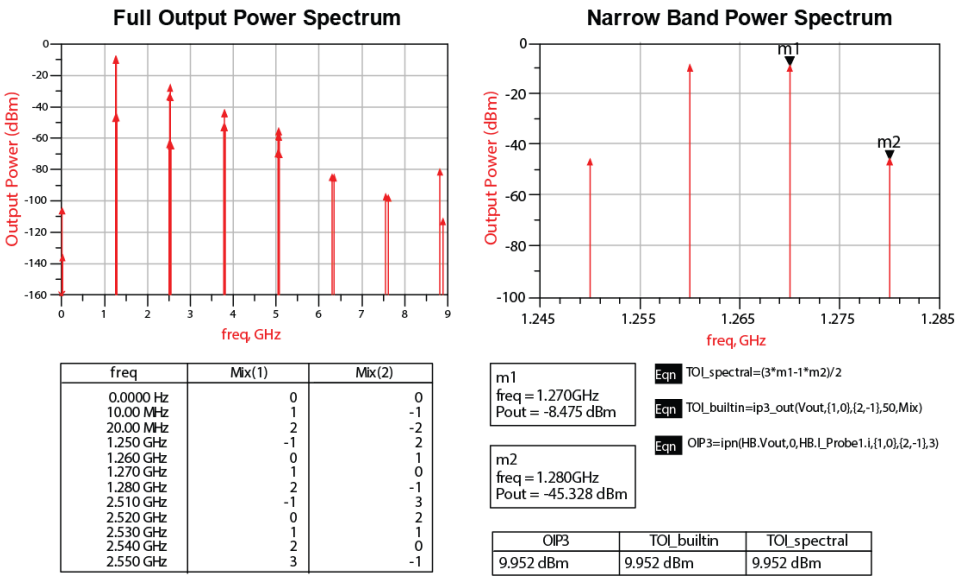


Figure 5.50: Third Order Intercept (IP_3) Point Simulation Setup



freq	Mix(1)	Mix(2)
0.0000 Hz	0	0
10.00 MHz	1	-1
20.00 MHz	2	-2
1.250 GHz	-1	2
1.260 GHz	0	1
1.270 GHz	1	0
1.280 GHz	2	-1
2.510 GHz	-1	3
2.520 GHz	0	2
2.530 GHz	1	1
2.540 GHz	2	0
2.550 GHz	3	-1

OIP3	TOI_builtin	TOI_spectral
9.952 dBm	9.952 dBm	9.952 dBm

Figure 5.51: Third Order Intercept Point Simulation Results

Using Equation 3.20 the IP_3 point was calculated as 9.952 dBm. This value was verified in the simulation using the built-in function from ADS and yielded exactly the same results. An output third order intercept point, OIP_3, of 9.952 dBm using an active device biased to operate at a low current consumption is relatively high compared to the other active devices used for the same application. This indicated a LNA was built with relatively good linearity properties.

The performance parameters of the ATF-55143 LNA is summarised in Table 5.6.

Table 5.7: Summary of Performance Parameters for ATF-55143 LNA

	NF	S_{21}	S_{11}	S_{22}	IP_{1dB}	OP_{1dB}	OIP_3
Ideal simulation	0.681 dB	18.023 dB	−7.180 dB	−42.530 dB	-	-	-
EM simulation	0.704 dB	15.208 dB	−6.840 dB	−48.500 dB	−22.02 dBm	−3.750 dBm	9.952 dBm

When comparing these results with those of the BFP740 LNAs they indicate a slightly poorer *NF* and gain, a very similar *IRL* but a significantly better *ORL*. The linearity of both the lumped element LNAs is the same with the distributed element LNA linearity is slightly poorer.

5.8 AT-32032 Amplifier Design

The Avago AT-32032 active device represents the BJT active device family and is included in the investigation for comparison with the LNAs which use active devices that incorporate the latest integrated circuit (IC) technologies. This BJT is reliable due to ion implantation and self-alignment techniques applied during manufacturing (Avago Technologies, 2009:1). Based on the information provided by the manufacturer in the data sheet this device can potentially meet the required specifications. The manufacturer lists a minimum noise figure between 1 dB and 1.2 dB with a

maximum stable gain of about 15 dB that can be expected at the frequency of operation. To conform to the power budget and to achieve the specified noise figure, this active device will be biased at 2.7 V and 5 mA.

5.8.1 Stabilising the Active Device

The simulation set-up is shown in Figure 5.52, and the signal source was swept across a wide range of frequencies to determine the Rollet stability factor (*K*) of the active device. This will determine whether or not the active device is unconditionally stable and if some form of stabilisation must be implemented.

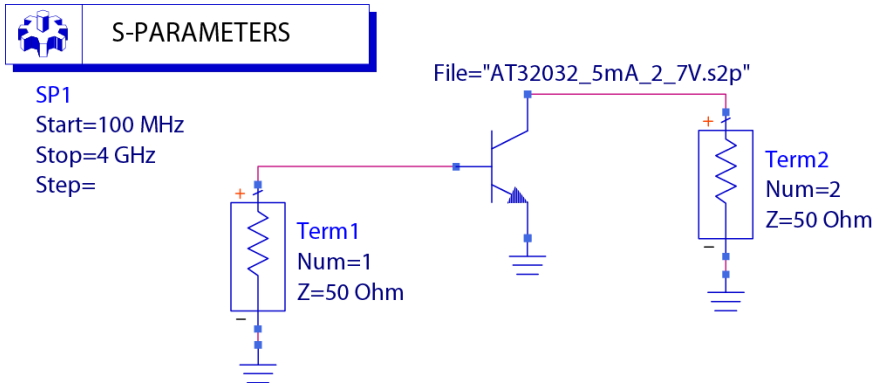


Figure 5.52: Simulation Setup for Stability Factor

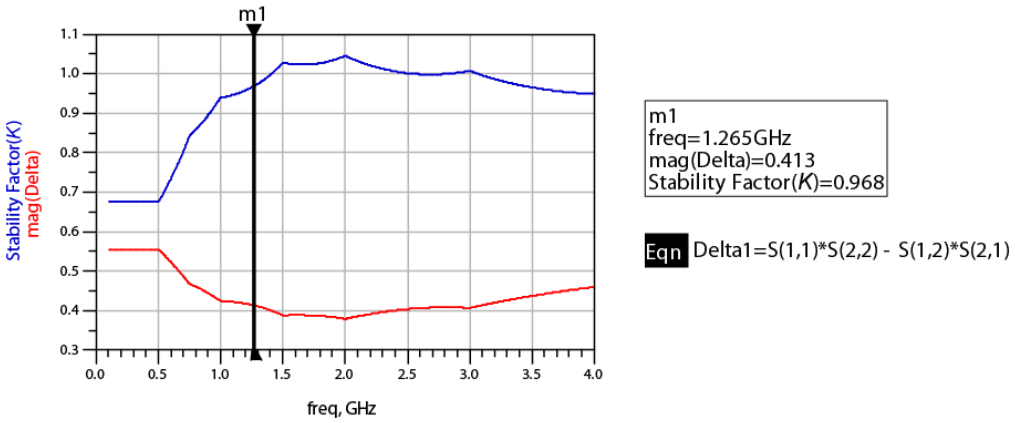


Figure 5.53: Simulated Results for Stability

The results in Figure 5.53 clearly show that the active device is not unconditionally stable at all frequencies of operation and thus the BJT must be stabilised. The same technique of shunt loading of the output port of the active device, as used with all of the previous LNAs, was implemented with this BJT. A 2 kΩ resistor connected in shunt with the collector rendered the BJT unconditionally stable. The results are illustrated in Figure 5.54.

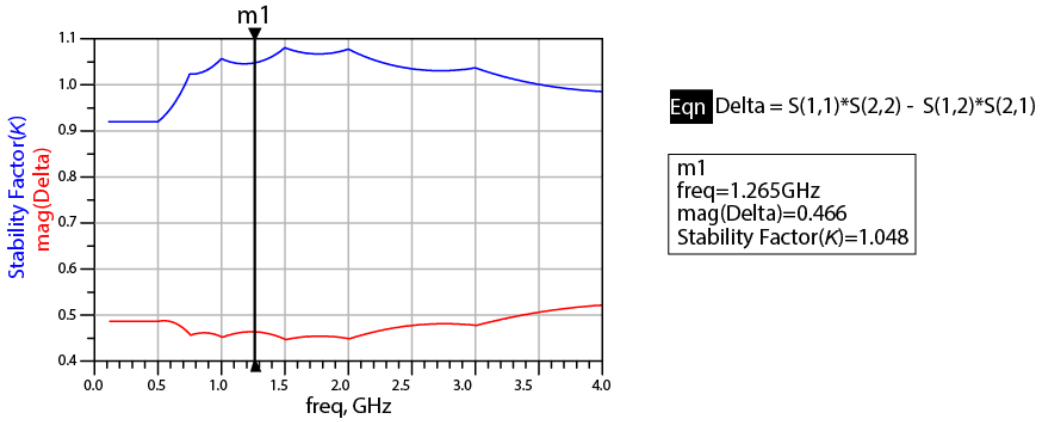


Figure 5.54 Simulated Results for Stabilised Active Device

5.8.2 Design of Matching Networks

With the active device made unconditionally stable, the same process is followed as in the design of the previous LNAs. That is, a new set of *S*-parameters is generated with the resistively loaded BJT and then the optimum source reflection coefficient is calculated for optimum noise performance. The new *S*-Parameters and Γ_{Opt} are listed in Table 5.8.

Table 5.8: *S*-Parameters Generated from Stable Active Device

Frequency	S_{11}	S_{12}	S_{21}	S_{22}	Γ_{Opt}
1.265 GHz	0.110 ∠−111.252	0.104 ∠66.041	4.537 ∠73.741	0.466 ∠−28.190	0.257 ∠97.9

The program *L-Net* was again used to simplify the design of the lumped element matching networks. The *S*-parameter values and the value for Γ_{Opt} from Table 5.8 were used in Equation 3.6 to calculate Γ_o as 0.521∠−44.149. The values for Γ_{Opt}* and Γ_o were then entered into *L-Net* and the possible input and output matching networks, as illustrated in Figures 5.55 and 5.56 respectfully, were synthesised.

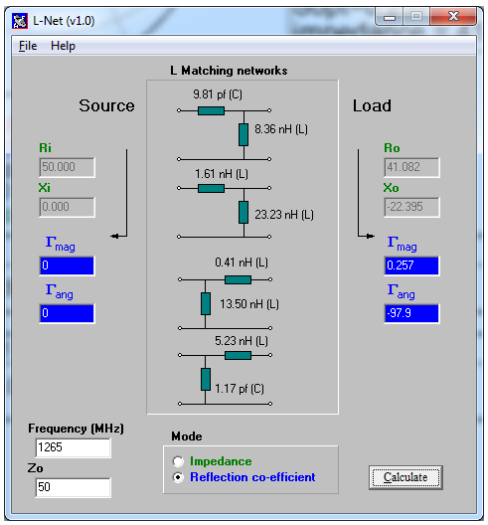


Figure 5.55: Possible Input Matching Networks

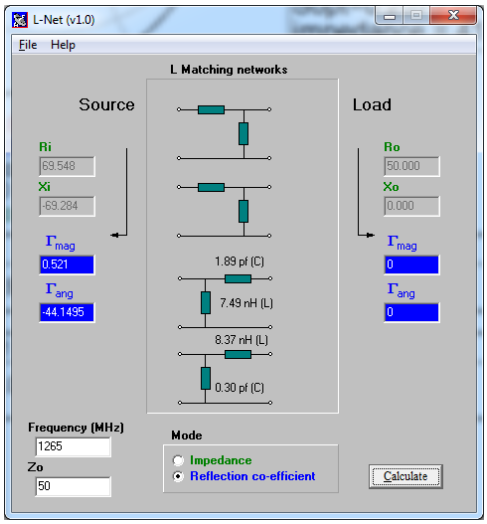


Figure 5.56: Possible Output Matching Networks

The simulation setup in Figure 5.57 illustrates the topology of the input and output matching networks that were selected. They were specifically chosen to simplify the final circuit schematic and minimise the component count. A capacitor in series with the input and output port provides for good coupling between RF stages, and the shunt inductor will later be used as an *RFC* which reduces the overall component count. The results of the simulation are shown in Figure 5.58.

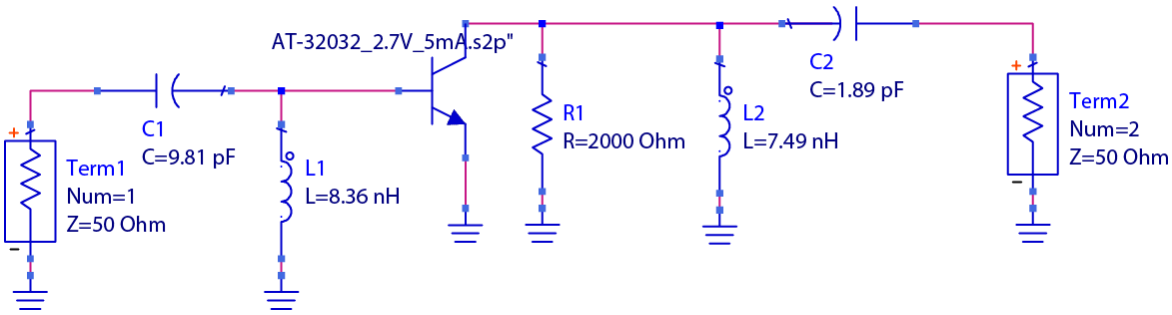


Figure 5.57: Schematic for Simulation of Matching Network Performance

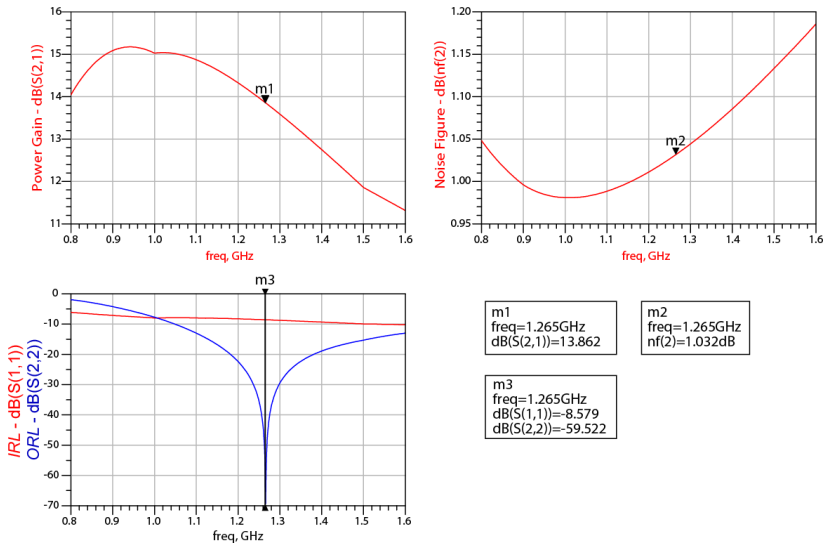


Figure 5.58: Simulated Results of Active Device with Matching Networks

These results are typical of a LNA with medium gain, low *NF*, poor *IRL* and relatively good *ORL*. They also indicate that the amplifier is functioning optimally as an LNA.

5.8.3 DC Biasing

The DC bias network chosen for the AT-32032 BJT active device is a voltage feedback constant base current source configuration, as shown in Figure 5.18. As mentioned in Section 3.15, it provides the best temperature stability of all the possible DC biasing networks for the current application. A simulation was performed on the active device to verify that the selected quiescent operating point is in the linear region of operation. The collector current versus collector-emitter voltage curves are illustrated in Figure 5.59 as well as the selected bias point which clearly indicates linear operation.

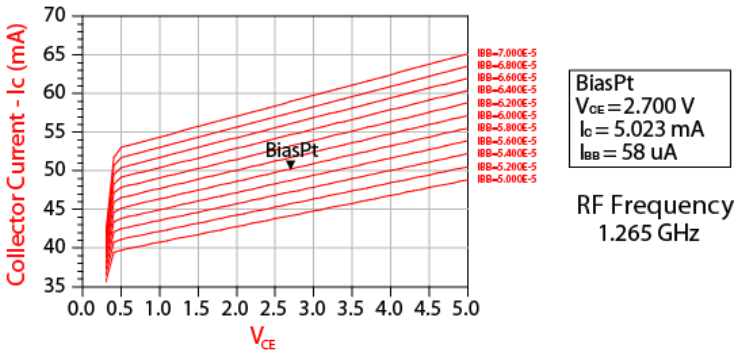


Figure 5.59: Quiescent Point Simulation

The bias conditions for the device to be able to perform according to the specifications were selected as V_{CE} = 2.7 V and I_C = 5 mA. The transistor characteristic properties were programmed into the program *Agilent Technologies AppCAD* to synthesise the bias network and achieve the selected bias conditions. The bias network schematic is illustrated in Figure 5.60.

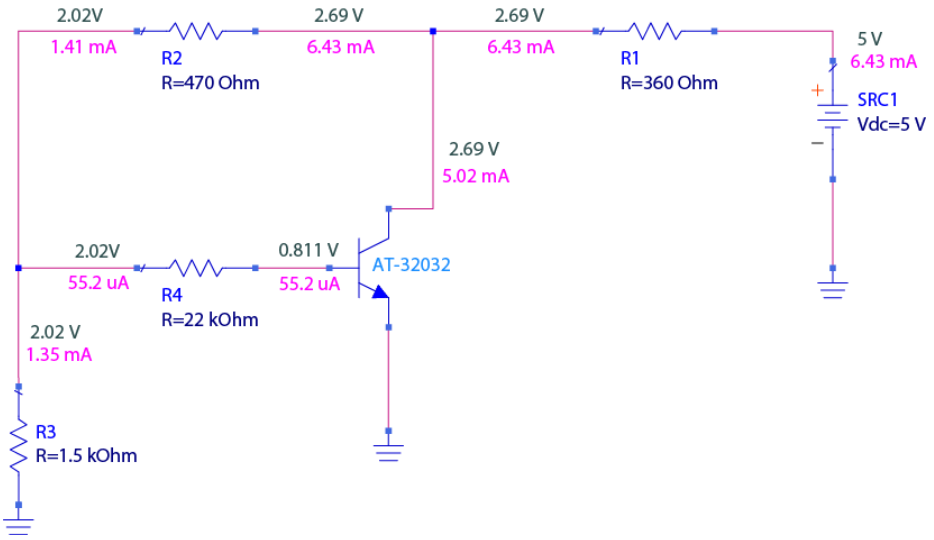


Figure 5.60: DC Bias Network for AT-32032 BJT

5.8.4 Final Schematic Diagram and PCB Layout

For the final simulation, the DC bias circuit and RF matching networks are combined and optimised for a schematic diagram with a minimum component count. Furthermore, the inductors and capacitors that make up the matching networks have been replaced with their real-world equivalent models and are shown in Figure 5.61.

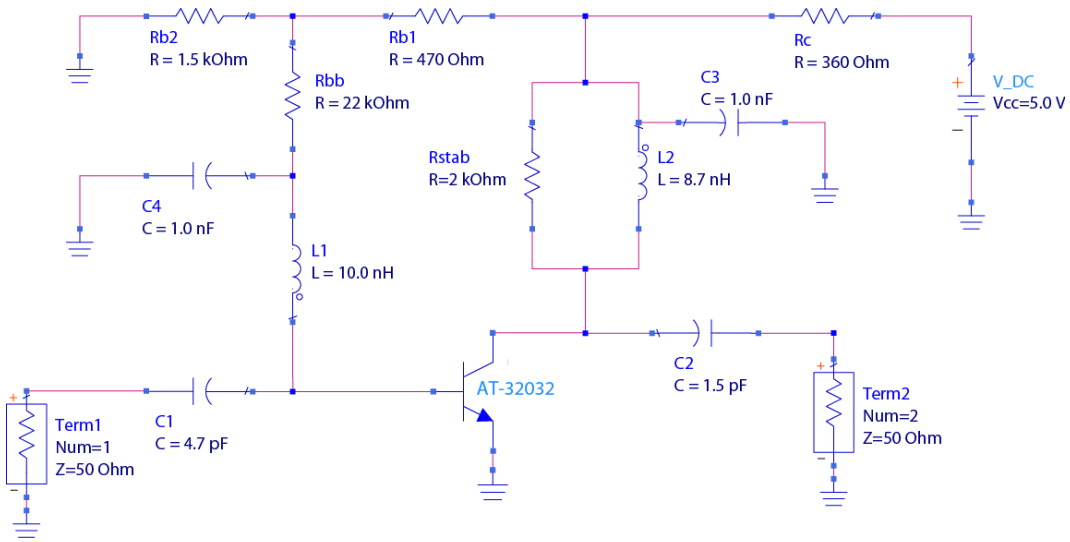


Figure 5.61: Final Schematic of AT-32032

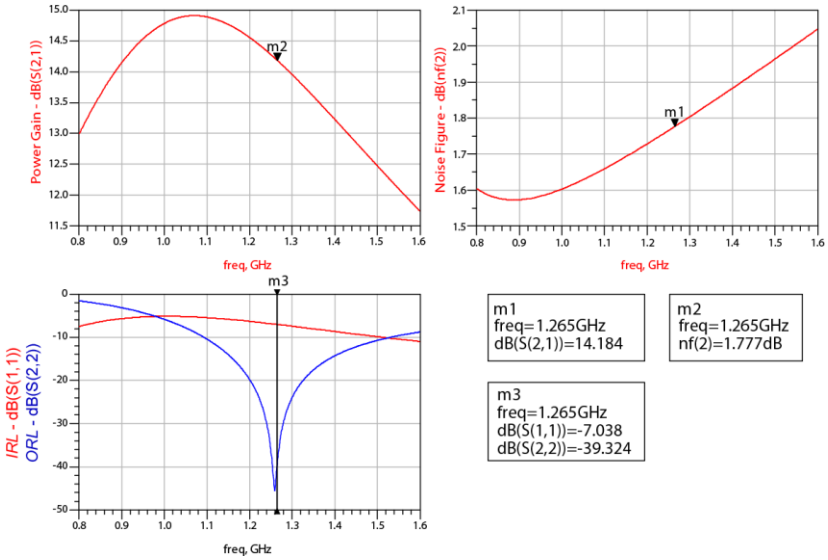


Figure 5.62: Simulated Results of AT-32032 LNA

The performance parameters of this LNA correlate well with those typical of an LNA and of those for the LNA circuits previously designed in this investigation. The next step is to lay out the PCB and then perform the Momentum EM simulation on the circuit using real-world components to obtain the closest possible simulated performance parameters as would be expected when the actual constructed amplifier is tested and measured. The momentum simulation setup is shown in Figure 5.63 and the results of this simulation are shown in Figure 5.64.

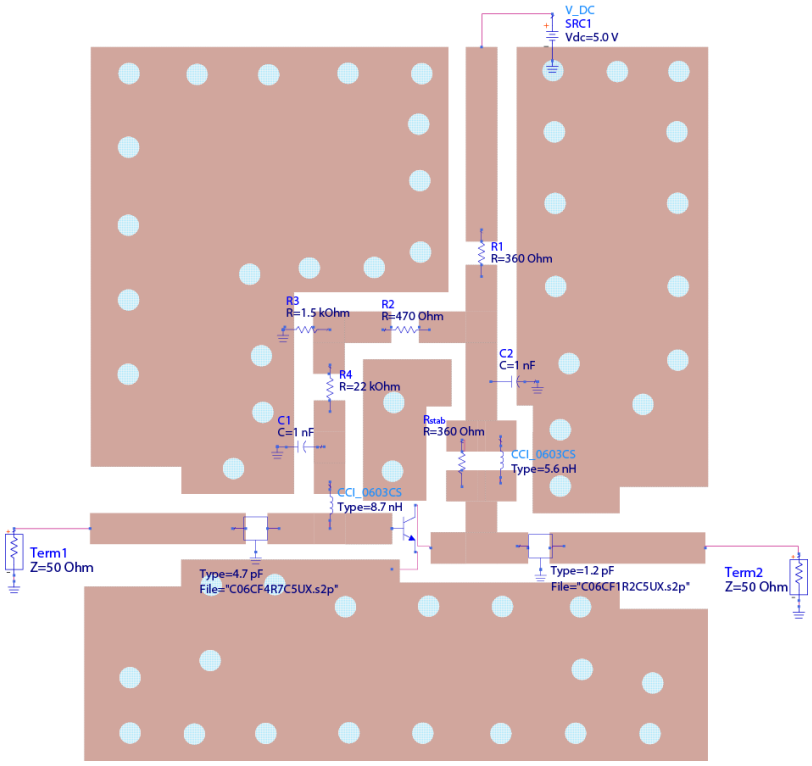


Figure 5.63: Momentum EM Simulation Setup of Completed AT-32032 LNA

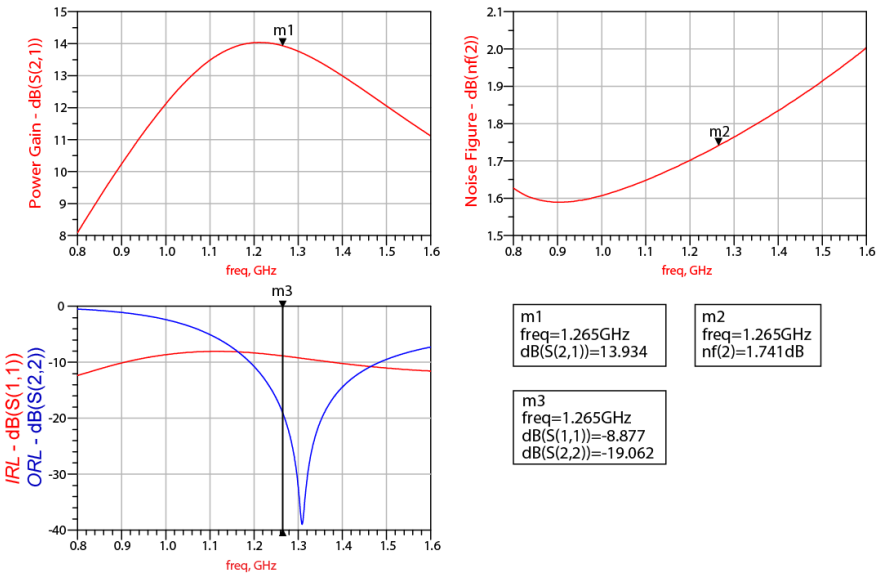


Figure 5.64: Momentum EM Simulation Results of Completed AT32032 LNA

The performance of the final EM simulation compares well with the previous LNA simulations and will be discussed in more detail at the end of this LNA design. Table 5.9 lists the differences in component values between the initial simulation, which uses ideal components and lossless transmission lines to interconnect components, and the Momentum EM simulation. The DC bias components stay unchanged, but one can observe a slight change in most of the matching components. Again, these changes in matching components are due to the EM simulation taking into account the behavior of the substrate material which the initial ideal simulations do not.

Table 5.9: Comparison of Component Values Between Different Simulations

Component and Description	Ideal Simulation value	EM Simulation Value
Active device (AT-32032)	N/A	N/A
Biasing Resistor (R_C)	360 Ω	360 Ω
Biasing Resistor (R_{B1})	470 Ω	470 Ω
Biasing Resistor (R_{B2})	1.5 kΩ	1.5 kΩ
Biasing Resistor (R_{BB})	22 kΩ	22 kΩ
Stabilising Resistor (R_{stab})	2 kΩ	2 kΩ
Input Match Capacitor (C_1)	4.7 pF	4.7 pF
Output Match Capacitor (C_2)	1.5 pF	1.2 pF
Decoupling (C_3, C_4)	1 nF	1 nF
Input Match Inductor (L_1)	10 nH	8.7 nH
Output Match Inductor (L_2)	8.7 nH	5.6 nH

5.8.5 Non-Linear Performance

Since this LNA is designed for best possible noise performance rather than for maximum power gain, the non-linear performance is not of such great importance as is the noise figure or power gain of the amplifier. However, the P_{1dB} and IP_3 points parameters play a role in the characterisation of the amplifier and allow the dynamic range of the LNA to be determined. Figures 5.65 and 5.66 illustrate the simulation and results of the 1 dB compression point.

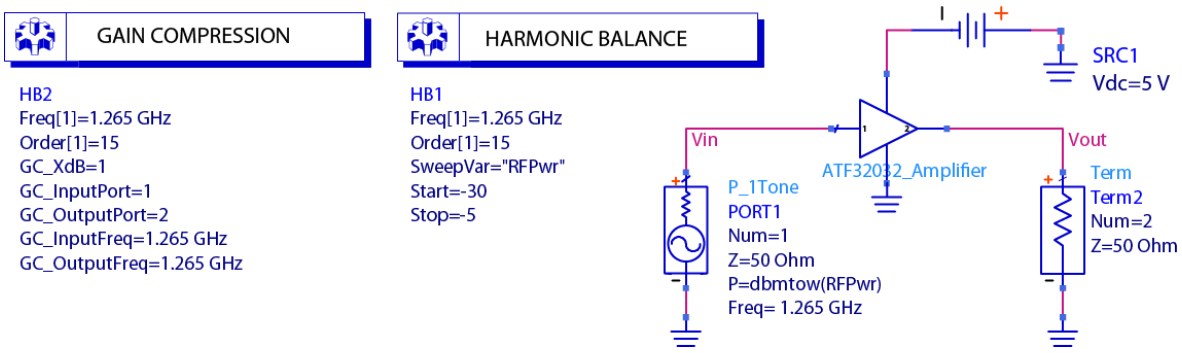


Figure 5.65: P_{1dB} Simulation Setup

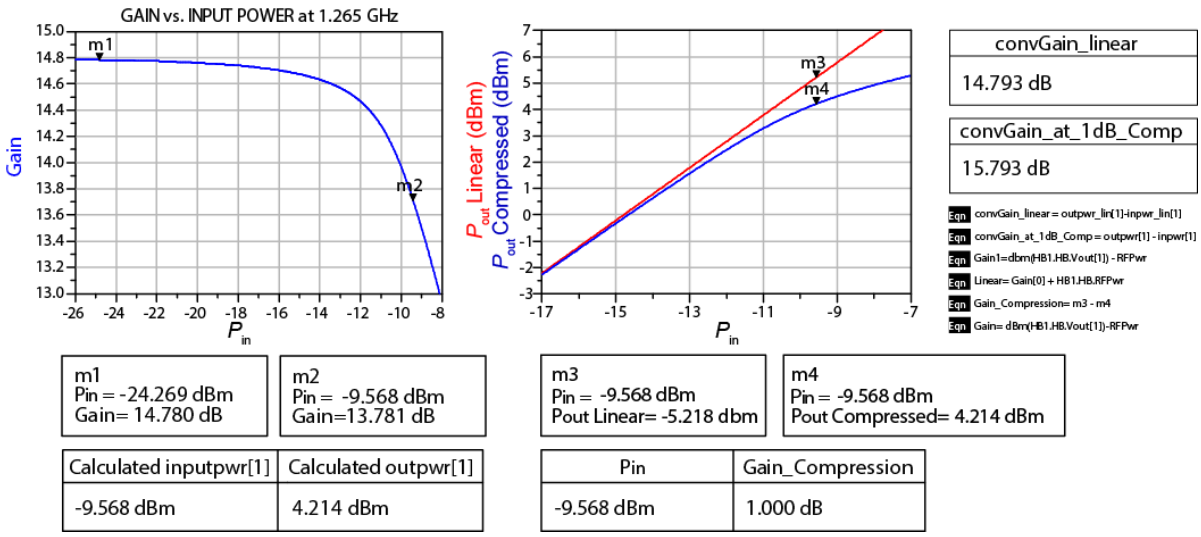


Figure 5.66: Results for P_{1dB} Simulation

The simulated results indicate that the IP_{1dB} is at −9.568 dBm and the OP_{1dB} at 4.214 dBm. To complete the linear characterisation of the LNA, the IP_3 simulation was performed to determine how well the amplifier attenuates in-band inter-modulation products created due to the non-linear behaviour of the amplifier. To calculate the OIP_3 Equation 3.20 can be used, but in this case it will be programmed into the simulation and verified using a built in function that came with the simulation software. The OIP_3 simulation setup and the corresponding results are illustrated in Figures 5.67 and 5.68 respectively.

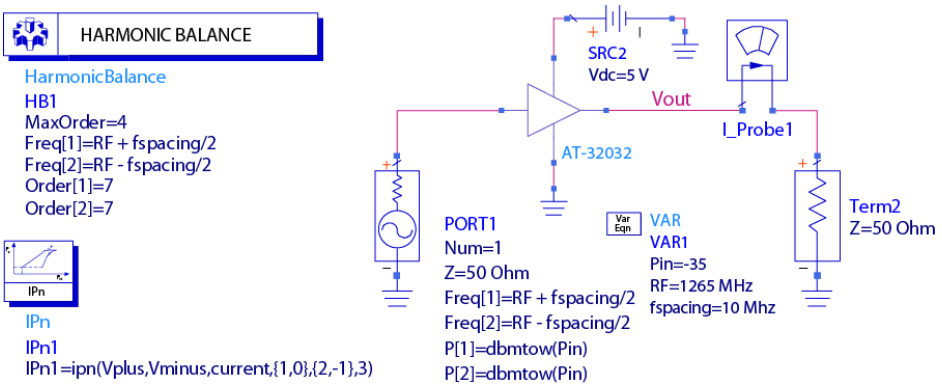
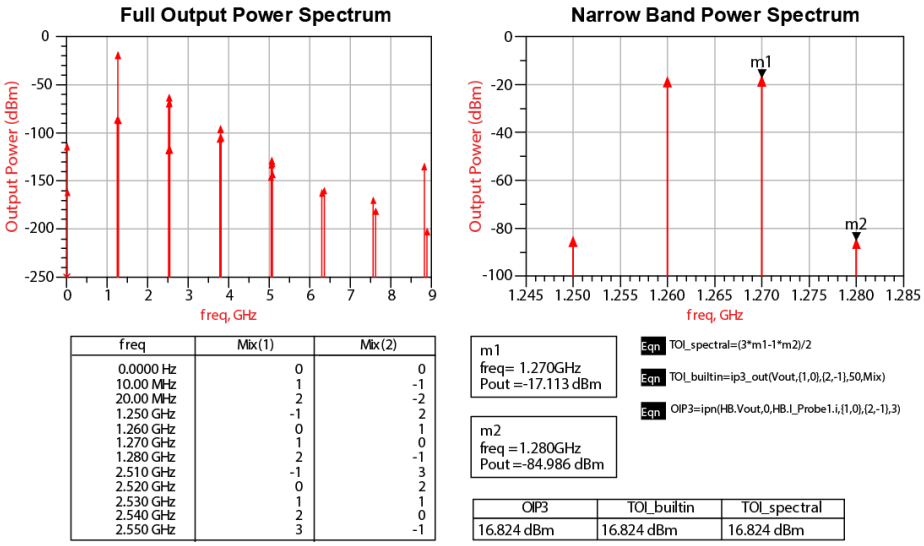


Figure 5.67: Simulation Setup to Determine IP_3 Point for AT-32032 Amplifier



freq	Mix(1)	Mix(2)
0.0000 Hz	0	0
10.00 MHz	1	-1
20.00 MHz	2	-2
1.250 GHz	-1	2
1.260 GHz	0	1
1.270 GHz	1	0
1.280 GHz	2	-1
2.510 GHz	-1	3
2.520 GHz	0	2
2.530 GHz	1	1
2.540 GHz	2	0
2.550 GHz	3	-1

OIP3	TOI_builtin	TOI_spectral
16.824 dBm	16.824 dBm	16.824 dBm

Figure 5.68: Results for IP_3 Simulation

5.8.6 Summary of Results

In general, BJTs are used at sub 1 GHz applications and give better results below this frequency. The AT-32032 had the best potential performance of the BJT active devices that were available and was included in the research to make sure the full range of RF transistors were investigated. Table 5.10 compares the ideal and Momentum EM simulated results.

Table 5.10: Summary of Simulated Results for the AT-32032 LNA

	NF	Gain	*IRL*	*ORL*	IP_{1dB}	OP_{1dB}	OIP_3
Ideal simulation	1.777 dB	14.184 dB	−7.038 dB	−39.324 dB	-	-	-
EM simulation	1.741 dB	13.934 dB	−8.877 dB	−19.062 dB	−9.568 dBm	4.214 dBm	16.820 dBm

The manufacturer's data sheet indicates that a *NF* of 0.9 dB is achievable. During the simulations to design the matching networks, the linear model of the active device was used and the measurements were interpolated from the S2P file of the active device. Very similar results were obtained to what was

specified in the datasheet, but when the real-world non-linear die model was introduced, and with near perfect biasing conditions, the lowest value for the *NF* that could be achieved was just above 1.7 dB. Although the technique used to stabilise the device degrades the obtainable *NF* slightly, one would not expect such a great difference from what is specified and simulated. In all of the previously designed LNAs, the *NF* performance achieved in the Momentum EM simulations were within 0.2 dB of that specified in the manufacturers data sheet. This indicated that the linear and the non-linear models of the active device produced virtually the same results which were expected. In the Momentum simulation of this LNA, a *NF* of 1.741 dB was obtained which is close to what was simulated in the ideal simulation and shows that the design technique is correct and accurate. The results also reflect the fact that the matching networks were designed for optimum noise performance. In the Momentum EM simulations the actual component values were adjusted in accordance with the E12 range of component values which are available in practice. The AT-32032 active device did however display good non-linear results. Compared to the previously designed LNAs, the P_{1dB} and IP_3 performance parameters were significantly higher and indicate a particularly linear LNA.

5.9 ATF-36163 Amplifier Design

The design of the ATF-36163 LNA follows a similar procedure as in the previous design techniques except for the method used to stabilise and bias the active device. Figure 5.69 illustrates the package and pin description of the active device. This active device package is different to the previous active devices in that it has four source terminations and careful consideration must be given to the manner in which the bias network is connected.

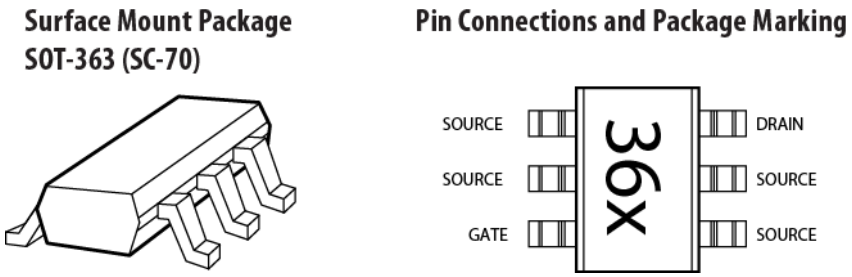


Figure 5.69: Package Information and Pin Configuration of ATF-36163 (Avago Technologies, 2008:1)

5.9.1 Stabilising the Active Device

As explained in Section 3.10, the active device must conform to certain stability criteria before it can be used in the front end of a receiver. If the device is not stable at the design frequency and the Rollet stability factor is less than one, or the requirements of Equation 3.19 are not met, the device must be forced to become stable by adding a resistor in parallel with the output port of the active device. Figure 5.70 shows the simulation setup for stability criteria, with the results illustrated in Figure 5.71.

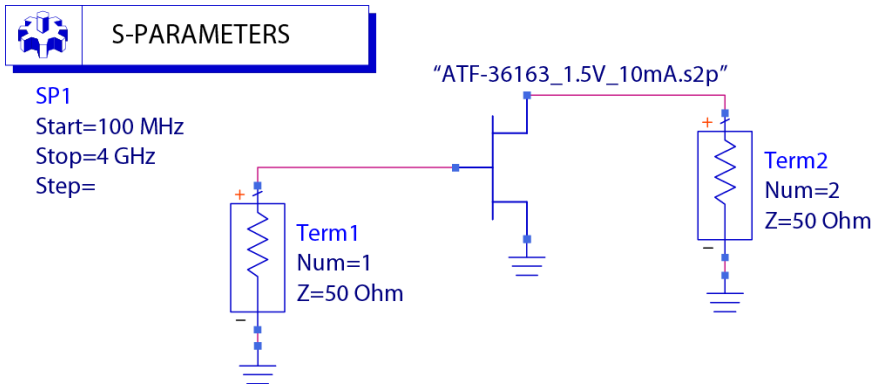


Figure 5.70: Simulation Setup for Stability Criteria

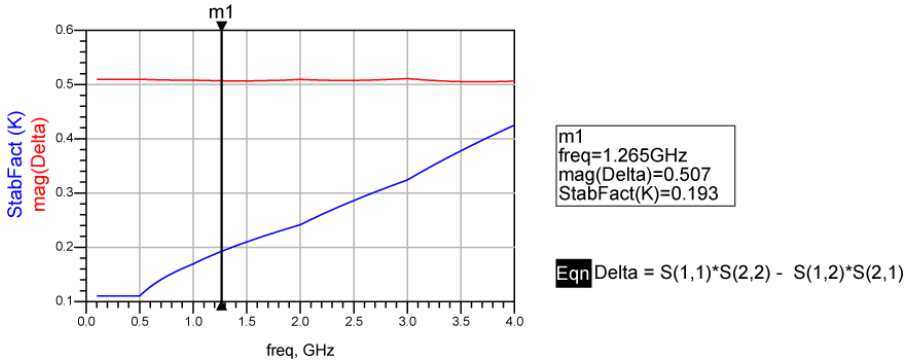


Figure 5.71: Simulated Results for Stability Criteria

From the results in Figure 5.71 the value of *K* is clearly less than one for the entire frequency band of interest. Unfortunately a single shunt resistor alone cannot force the device to become unconditionally stable and, since all the other resistive loading methods of stabilisation degrade the *NF* and power gain of the amplifier excessively, another technique known as source degeneration will be implemented. To implement this technique a 1 nH inductor is placed in series with the source lead of the active device to further increase stability as shown in Figure 5.72.

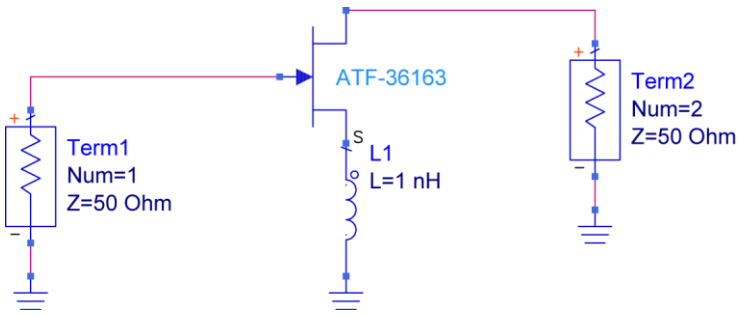


Figure 5.72: Active Device with Source Lead Inductance Added

With the source lead inductance in place, the circuit was re-simulated and load and source stability circles were plotted on a Smith chart and are shown in Figure 5.73. The fact that the circumferences of

the load and source stability circles still overlap onto the Smith chart, indicate that the stabilisation technique of adding source lead inductance is not sufficient for unconditional stability. Hence, a resistor must also be added in shunt with the output port of the transistor. To determine the value of resistor, a constant conductance circle was drawn that passes close to the load stability circle but does not intersect it. The process is illustrated in Figure 5.73. To physically implement the source lead inductance, a small section of microstrip will be used when building the LNA.

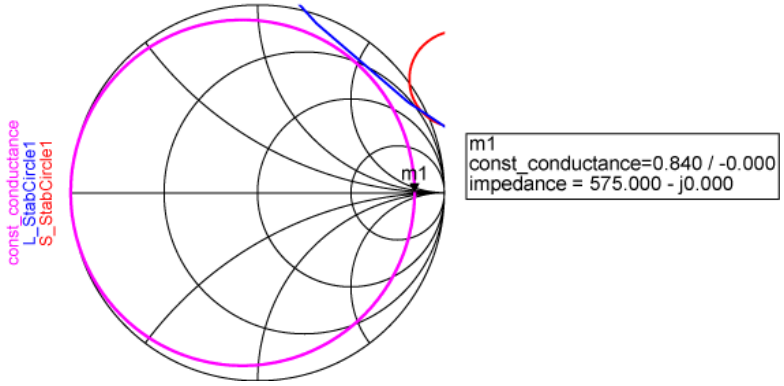


Figure 5.73: Simulation Results from Circuit with Source Inductance Added

The closest E12 series standard resistor value to the simulated value was selected and a 560 Ω resistor was placed in parallel with the drain of the active device. Figure 5.74 illustrates the stabilised active device with both the source lead inductance and parallel resistor included in the circuit.

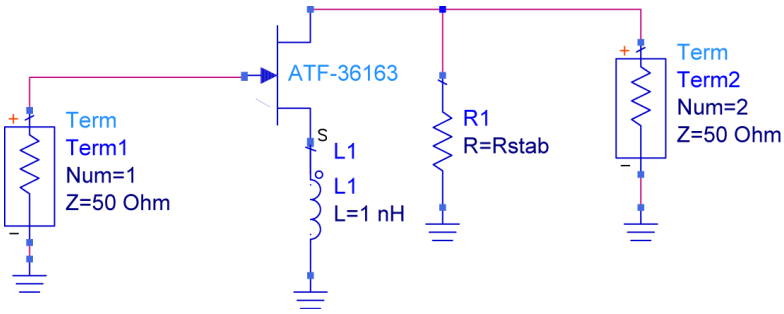


Figure 5.74: Stabilised Active Device

5.9.2 Design of Matching Networks

Since the amplifier will be designed for best noise performance, the active device is matched to the complex conjugate of the optimum source reflection coefficient, denoted Γ_{opt}*. A new set of *S*-parameters was generated after stabilising the active device and the value of $\Gamma_{opt} = 0.767\angle{-28.274}$ was obtained from the simulation. The complex conjugate, Γ_{opt}*, is equal to $0.767\angle{-28.274}$. By using Equation 3.6, the value for Γ_o was calculated and the input and output matching networks were

synthesised using the software program *L-Net* (v1.0) (Grant, 1998). Figures 5.75 and 5.76 illustrate the input and output matching networks which can be implemented.

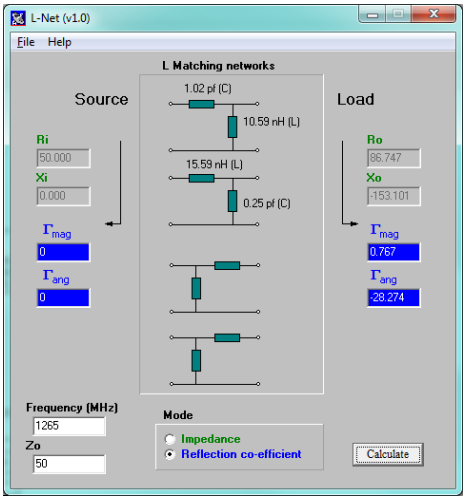


Figure 5.75: Possible Input Matching Networks

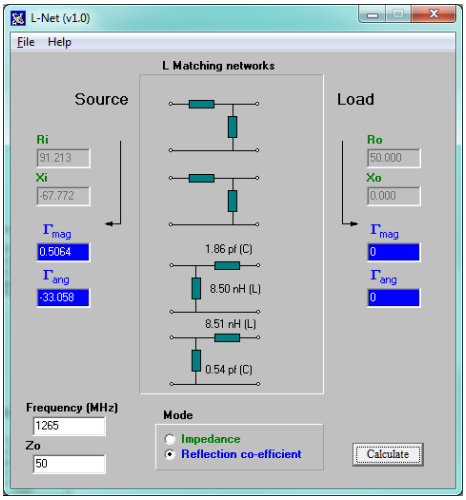


Figure 5.76: Possible Output Matching Networks

The selected matching networks were coupled to the stabilised active device as shown in Figure 5.77 and the performance of the selected topologies was evaluated by simulation. The results of the simulation are illustrated in Figure 5.78.

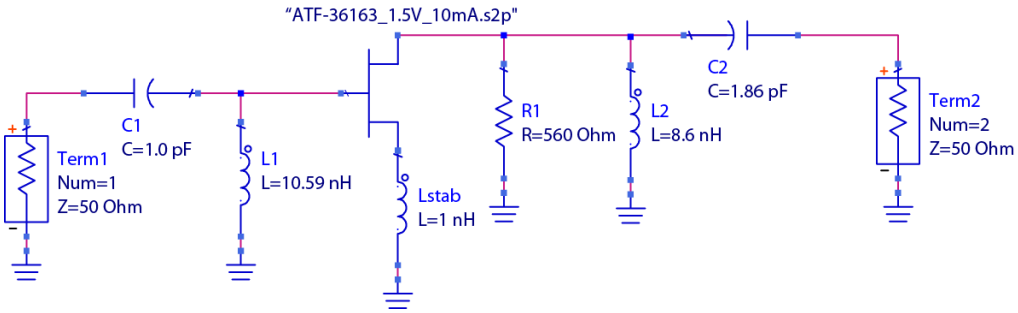


Figure 5.77: Schematic for Simulation of Matching Network Performance

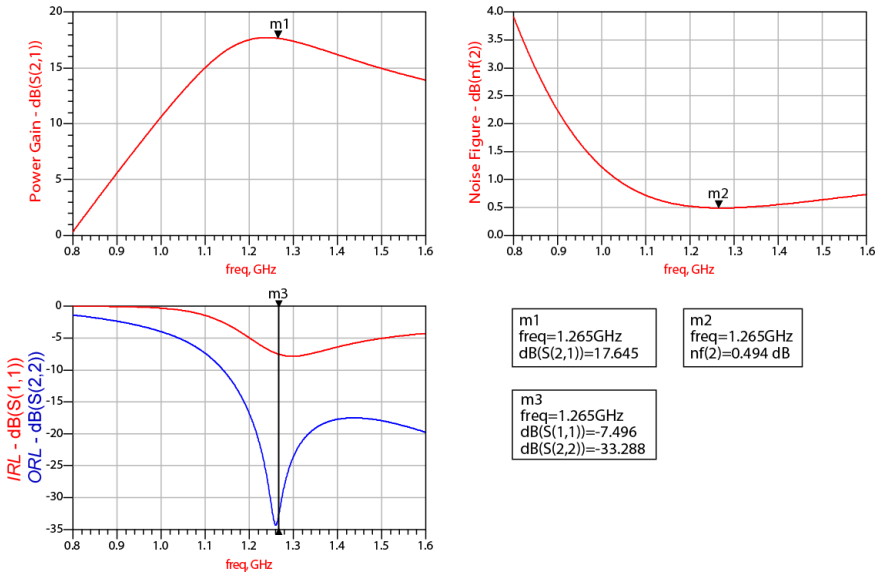


Figure 5.78: Simulated Results of Active Device and Matching Networks

These results indicate a low *NF*, reasonable gain, a sub-optimum *IRL* and a good *ORL*, typical of a LNA.

5.9.3 DC Biasing

When biasing FET devices, in particular a GaAs pHEMT as in the case of the ATF-36163, the convention is to make use of a dual or two separate power supplies. Section 3.15 explains the technique of self-biasing the FET. The most important part is that the active device must be biased in the linear region of operation and that it should keep this quiescent state over changes in ambient temperature. This will be implemented using the circuit shown in Figure 5.79.

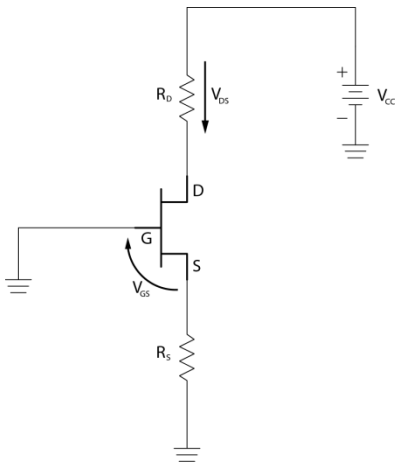


Figure 5.79: FET Bias Circuit

A quiescent bias point of V_{DS} = 1.5 V and I_D = 10 mA was selected from information provided in the active device data sheet. A quiescent point simulation was performed to confirm that the active device is biased in the linear region of operation. Figure 5.80 illustrates the results obtained from the simulation.

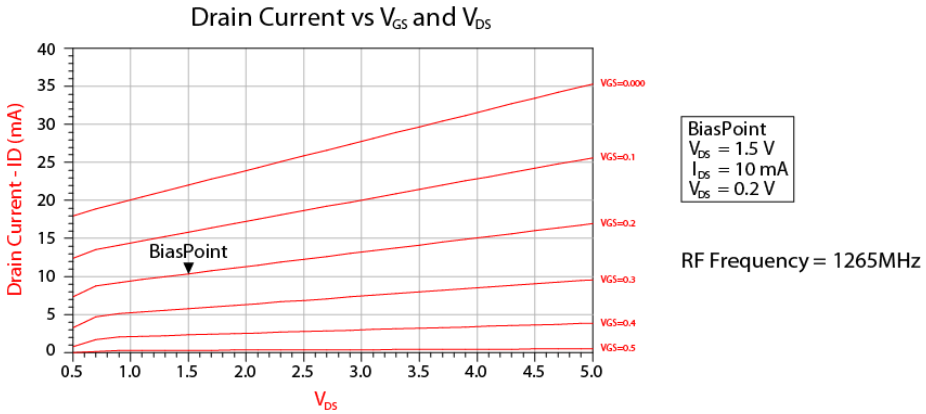


Figure 5.80: Quiescent Point Simulation of Active Device

The results in Figure 5.80 clearly show that the quiescent operating point is in the linear region of operation and that the bias network can now be designed. The values for R_D and R_S were calculated and the bias network was evaluated using *Agilent Technologies' AppCAD* software. The SOT-363 package that the active device is manufactured in has six legs, four of which are connected to the source. Connecting one of the legs to the source bias resistor and leaving the remainder floating may result in instability and unwanted problems due to poor grounding. For this LNA it was decided to connect pins two and three of the source legs together, and the same for pins four and five. This places the two pairs of legs in parallel with each other, so the source resistor values will be calculated to be in parallel. This process, together with the completed bias network, is shown in Figure 5.81. A DC simulation was performed and the results shown in Figure 5.81 confirmed that the active device was appropriately biased.

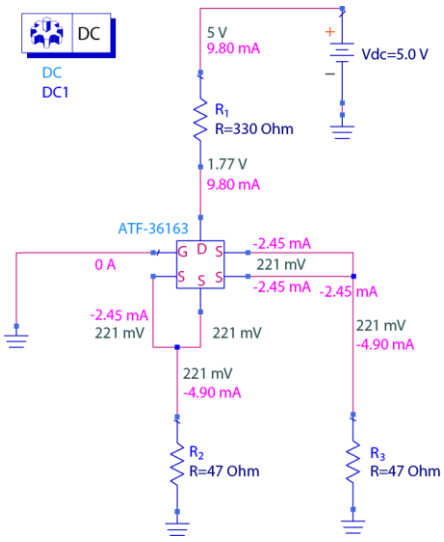


Figure 5.81: Completed Bias Network for FET Device

5.9.4 Final LNA Schematic and PCB Layout

After the FET is biased the AC and DC sections of the amplifier must be combined. To prevent the AC circuitry from affecting the DC circuitry and vice versa, careful decoupling and RF choking must be implemented. Figure 5.82 illustrates the final schematic with these components correctly placed and the simulated results are shown in Figure 5.83.

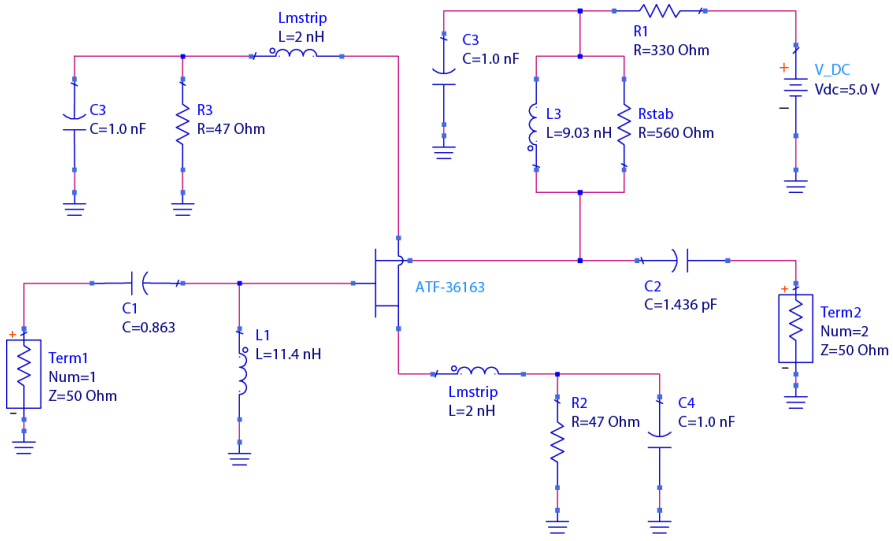


Figure 5.82: Final Circuit Schematic of ATF-36163 LNA

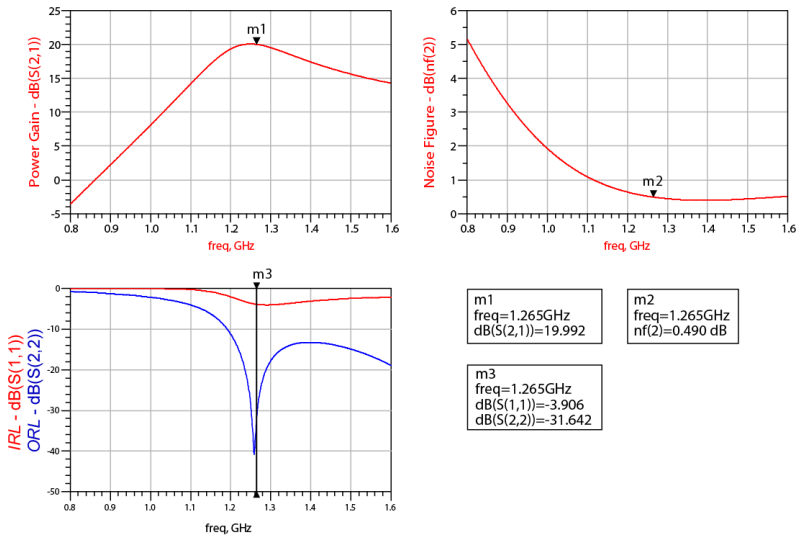


Figure 5.83: Simulated Results of ATF-36163 LNA

The results of the matching network simulation shown in Figure 5.78 and those of the complete LNA in Figure 5.83 correlate very well and again depict the performance parameters typical of those for a LNA. In particular, this ATF-36163 LNA provides a *NF* of 0.49 dB which is the lowest of the LNA's designed so far. The circuit board topology of the LNA was then designed using the Layout program within ADS and then populated with the real-world models of the components used. This complete circuit was then simulated using the EM Momentum simulation software within ADS to obtain as close as practically possible the expected performance parameters for the LNA. Figure 5.84 illustrates the completed layout of the circuit as it would appear after having the PCB made. Note how the inductors which add stability to the active device were implemented in microstrip. After physical construction of the LNA the two capacitors C_3 and C_4 can be moved closer to the active device to obtain the desired stability condition.

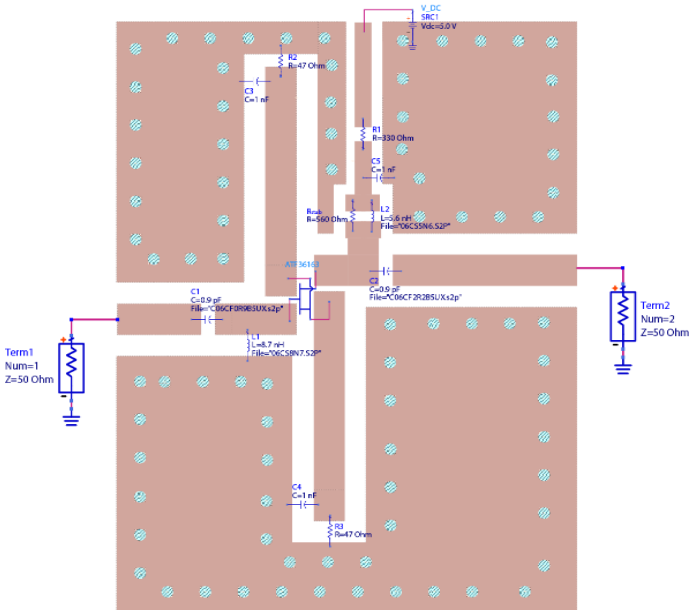


Figure 5.84: Momentum EM Simulation Setup of Completed ATF-36136 LNA

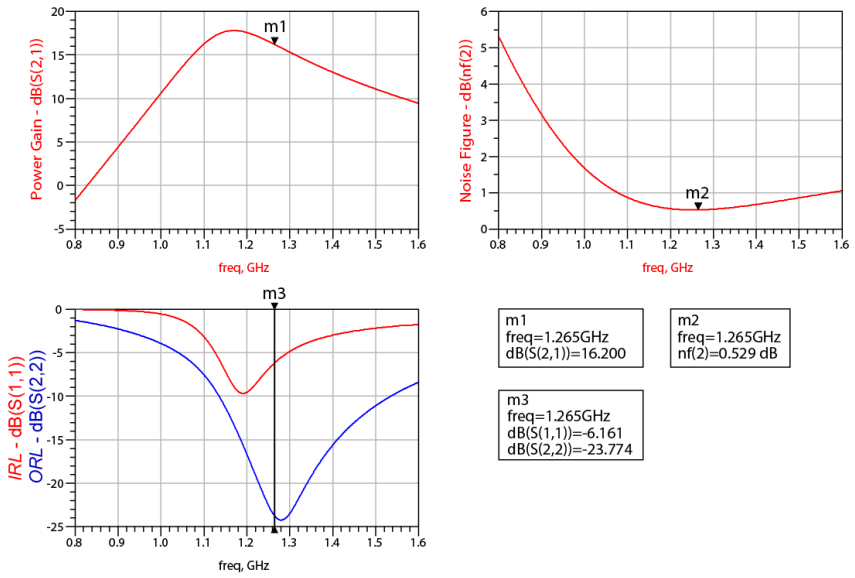


Figure 5.85: Momentum EM Simulated Results of Complete ATF-36163 LNA

The performance parameters achieved in Figure 5.85 compare well with all of the previously designed LNAs. Table 5.11 shows the differences between the component values used in the ideal and EM simulations. It is only the input and output matching components which had to be changed slightly for optimum performance.

Table 5.11: Comparison of Component Values Between Different Simulations

Component and Description	Ideal Simulation value	EM Simulation Value
Active device (ATF-36163)	N/A	N/A
Biasing Resistor (R_D)	330 Ω	330 Ω
Biasing Resistor (R_{S1}, R_{S2})	47 Ω	47 Ω
Stabilising Resistor (R_{stab})	560 Ω	560 kΩ
Input Match Capacitor (C_1)	1.0 pF	0.9 pF
Output Match Capacitor (C_2)	1.86 pF	2.2 pF
Decoupling (C_3, C_4, C_5)	1 nF	1 nF
Input Match Inductor (L_1)	10.6 nH	8.7 nH
Output Match Inductor (L_2)	8.6 nH	5.6 nH

5.9.5 Non-linear Performance

The final section in the design of this LNA is to evaluate its non-linear performance. The simulation setup to obtain the one dB compression point is shown in Figure 5.86 and the respective results in Figure 5.87.

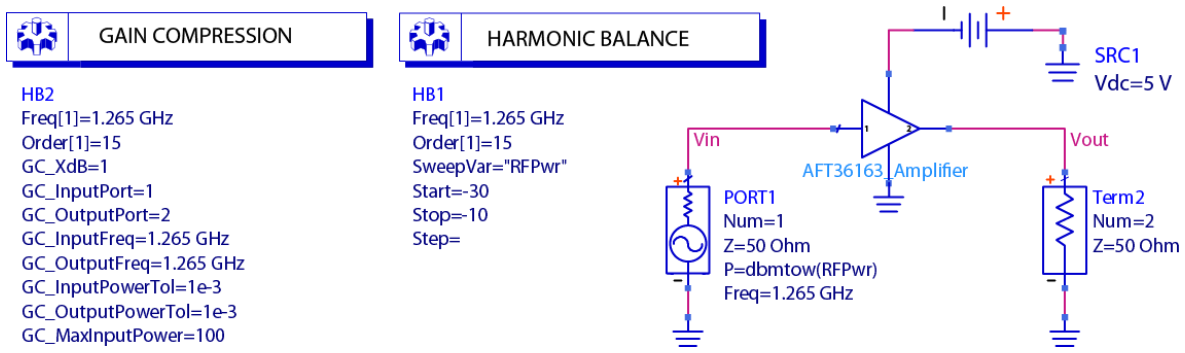


Figure 5.86: P_{1dB} Simulation Setup

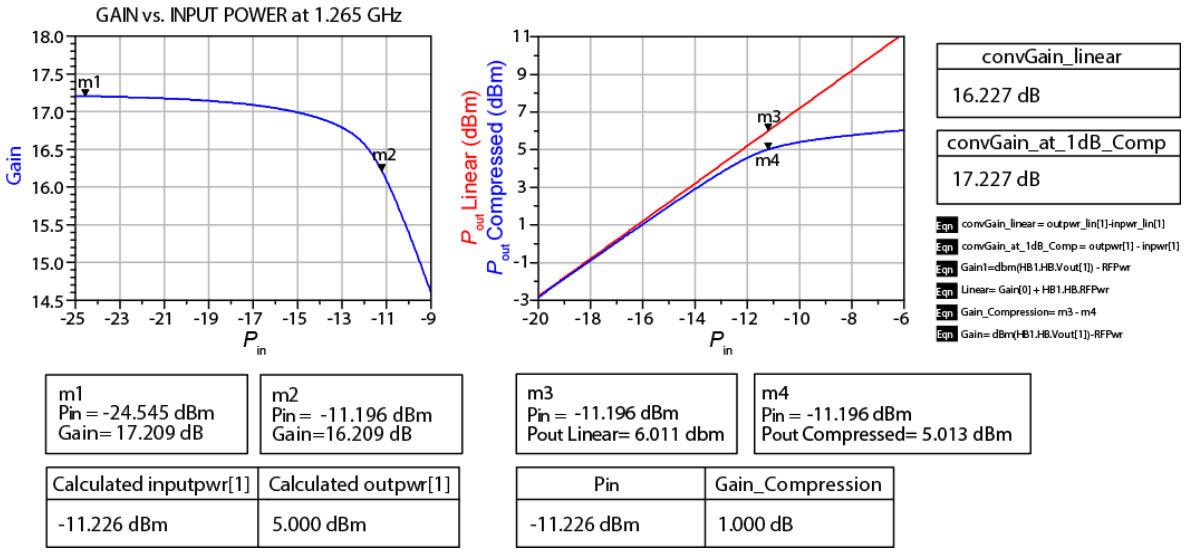


Figure 5.87: Results for P_{1dB} Simulation

The simulated results indicate that the IP_{1dB} is at −11.226 dBm and the OP_{1dB} at 5 dBm which means that the maximum output power obtainable from this LNA is just above 3 mW. The second part of the non-linear performance of the amplifier is given by the IP_3, point the measurement set-up and simulated results of which are illustrated in Figures 5.88 and 5.89 respectively. The performance parameters of the ATF-36163 LNA are summarised in Table 5.11.

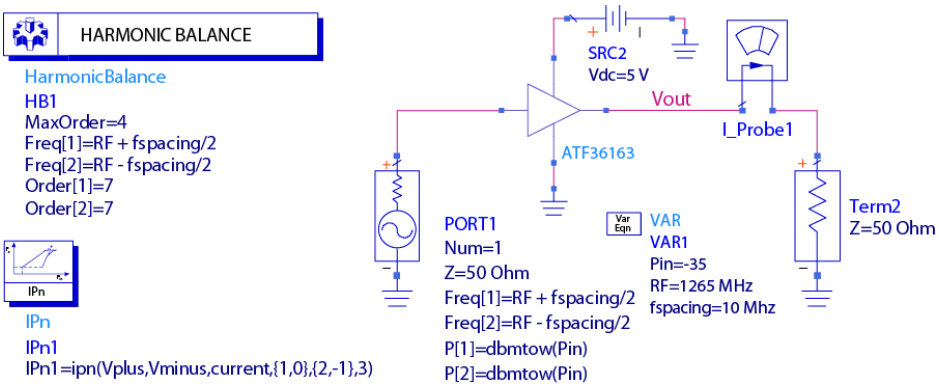


Figure 5.88: Third Order Intercept Simulation Setup

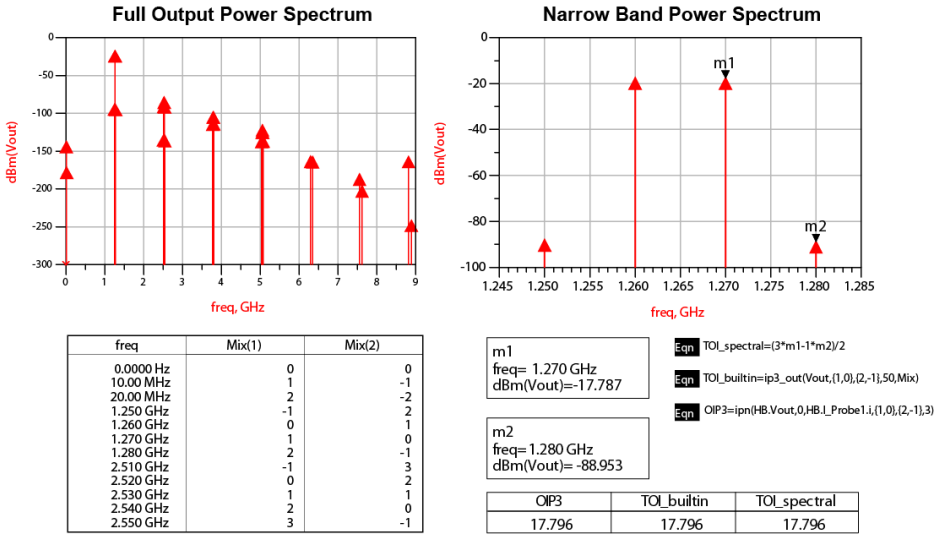


Figure 5.89: Results for IP_3 Simulation

Table 5.12: Summary of Simulated Results for ATF-36163 LNA

	NF	Gain	*IRL*	*ORL*	IP_{1dB}	OP_{1dB}	OIP_3
Ideal simulation	0.367 dB	17.080 dB	−1.925 dB	−54.583 dB	-	-	-
EM simulation	0.529 dB	16.200 dB	−6.160 dB	−23.774 dB	−11.23 dBm	5.000 dBm	17.790 dBm

5.10 ATF-36077 Amplifier Design

Exactly the same design process was used to design the ATF-36077 LNA as was used to design the ATF-36163 LNA. Figure 5.90 shows the package type and pin configuration of the ATF-36077 active device.

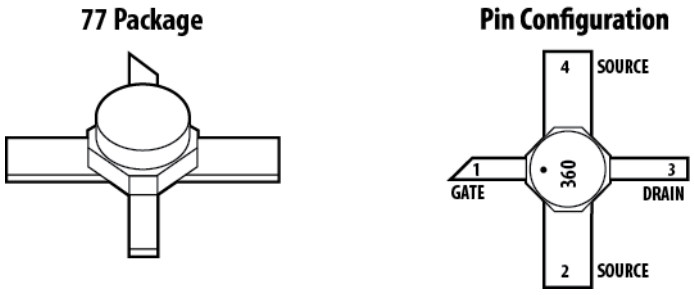


Figure 5.90: Pin Configuration and Package Information of the ATF-36077 (Avago Technologies, 2008:1)

5.10.1 Stabilising the Active Device

S-parameter simulations indicated that it was not possible to stabilise the active device using only resistive loading of the drain terminal. A combination of resistive loading and source degeneration was necessary to render the active device unconditionally stable. Figure 5.91 illustrates the simulation setup for stability and the two techniques used to obtain unconditional stability.

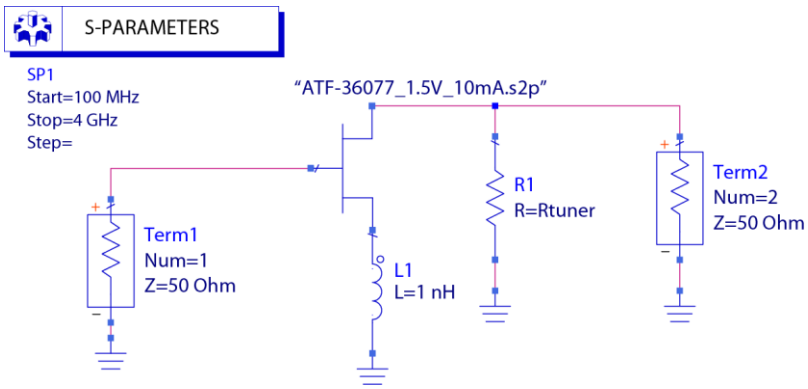


Figure 5.91: Stabilising the Active Device

Calculations show that placing a 680 Ω resistor in parallel with the output port of the active device and a 1 nH inductor in series with the source lead of the active device will unconditionally stabilise it. The stability criteria results obtained are illustrated in Figure 5.92.

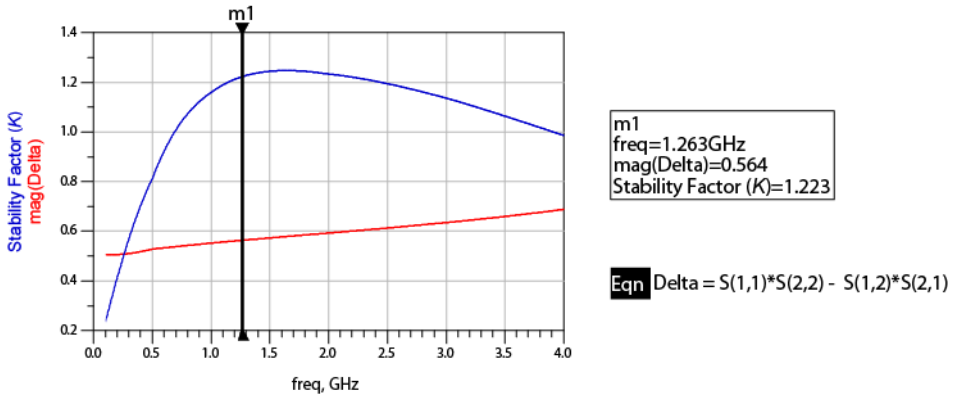


Figure 5.92: Simulated Results for Rollet Stability Criteria

5.10.2 Design of Matching Networks

After the active device was made unconditionally stable, a new set of *S*-Parameters was generated. Γ_{opt}* was obtained from the simulation and is equal to $0.932\angle -15.68$. By using the new *S*-parameters from Table 5.13 and substituting them into Equation 3.6, giving the value for $\Gamma_0 = 0.578\angle -49.665$.

Table 5.13: *S*-parameters Generated from Stable Active Device

Frequency	S_{11}	S_{12}	S_{21}	S_{22}
1.265 GHz	$0.886\angle -17.397$	$0.021\angle 103.938$	$4.015\angle 138.487$	$0.527\angle -2.411$

The matching networks were again synthesized using the software program L-Net (v1.0) (Grant, 1998). Figure 5.93 illustrates the simulation setup of the matching networks with the results shown in Figure 5.94.

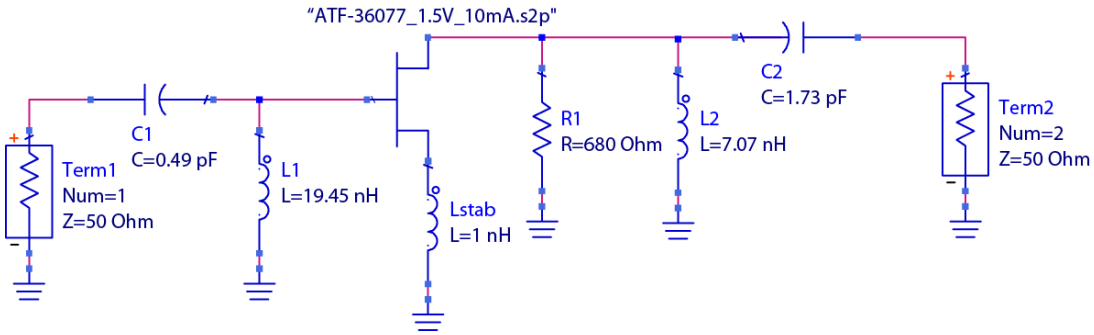


Figure 5.93: Schematic for Simulation of Matching Network Performance

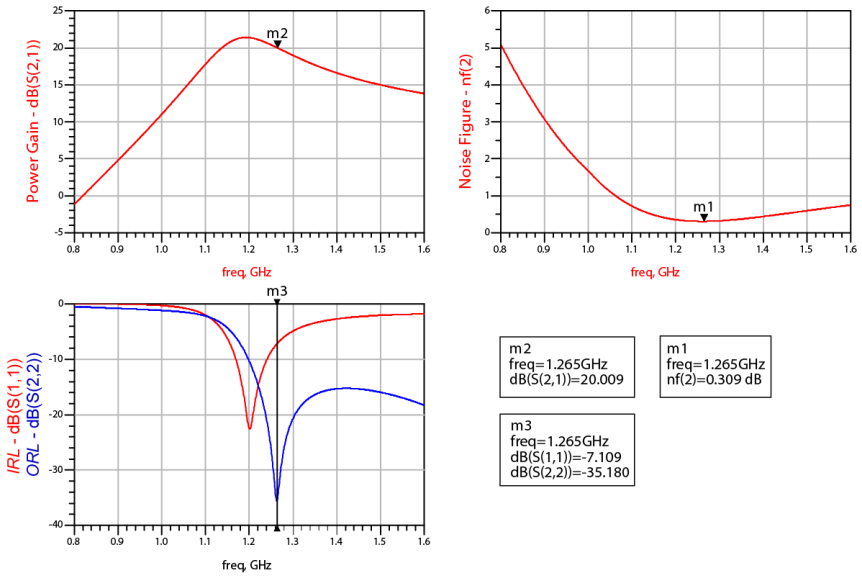


Figure 5.94: Simulated Results for Matching Networks

These preliminary results indicate a relatively high gain and a very low *NF* are achievable.

5.10.3 DC Biasing

As with the previous FET LNA design the self-biasing circuit illustrated in Figure 5.79 will be implemented. The device will be biased for V_{DS} = 1.5 V and I_D = 10 mA. The component values were calculated and verified using the software program AppCad. The final DC bias circuit is illustrated in Figure 5.95.

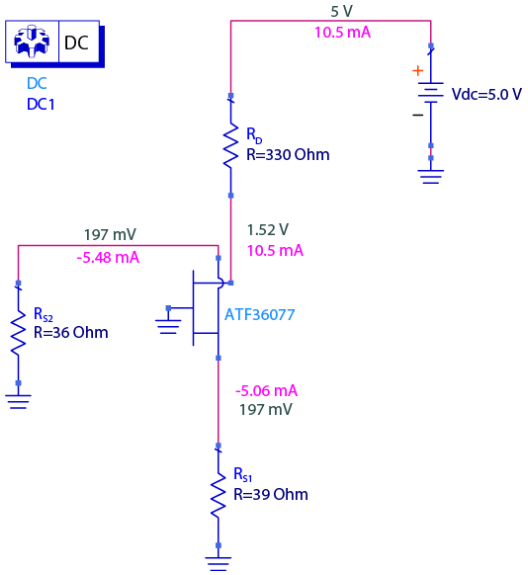


Figure 5.95: Self Bias Circuit for ATF-36077 FET

5.10.4 Final Design and PCB Layout

The DC bias and the AC matching circuits were then combined to form the final schematic which is shown in Figure 5.96 and the simulated results thereof in Figure 5.97.

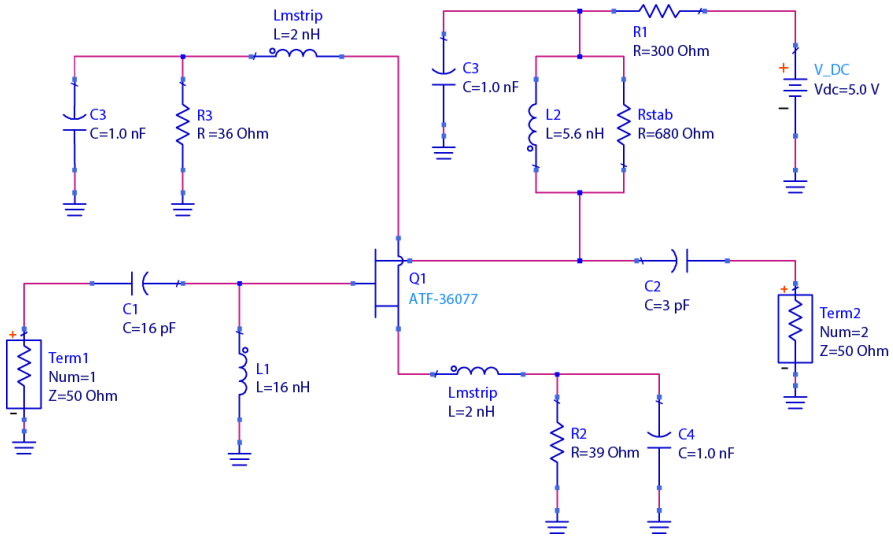


Figure 5.96: Final Circuit Schematic of ATF-36077 LNA

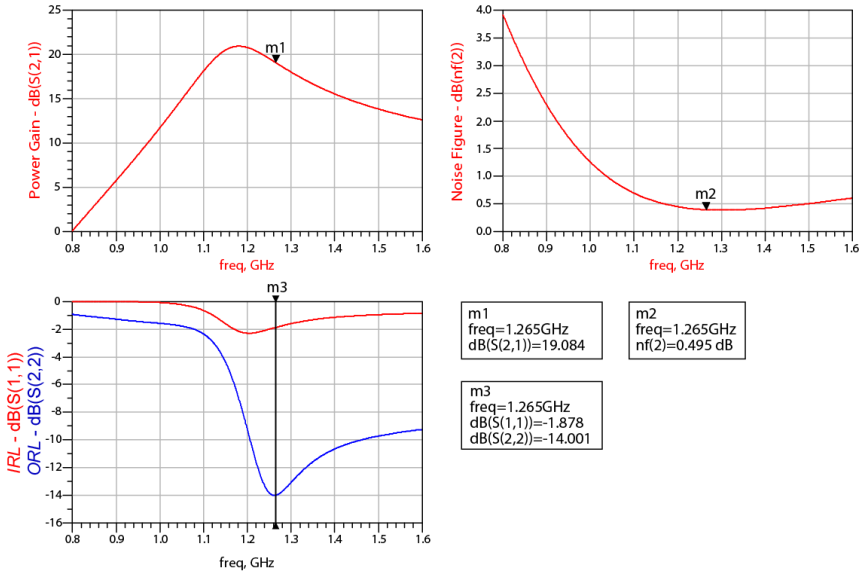


Figure 5.97: Simulated Results of Final Circuit Schematic of ATF-36077 LNA

The final simulated results meet the performance specifications of the LNA with very similar gain and *NF* performance as with the ATF-36136 LNA. Layout software within ADS was used to design the physical PCB for the LNA, followed by Momentum being used to perform the EM simulations with real-world models of the actual components used. The PCB layout and simulation setup is shown in Figure 5.98 and the respective results shown in Figure 5.99.

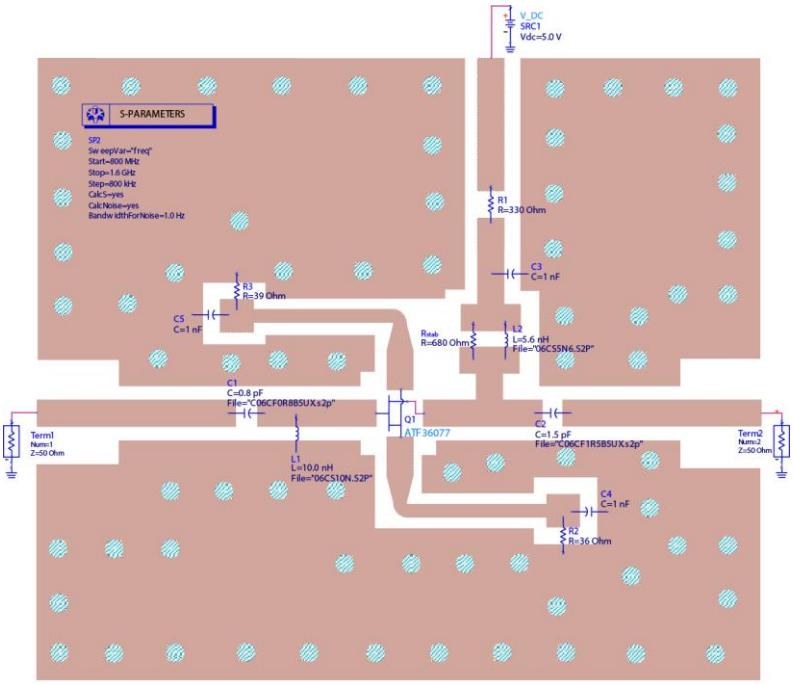


Figure 5.98: Momentum EM Simulation Setup of Complete ATF-36077 LNA

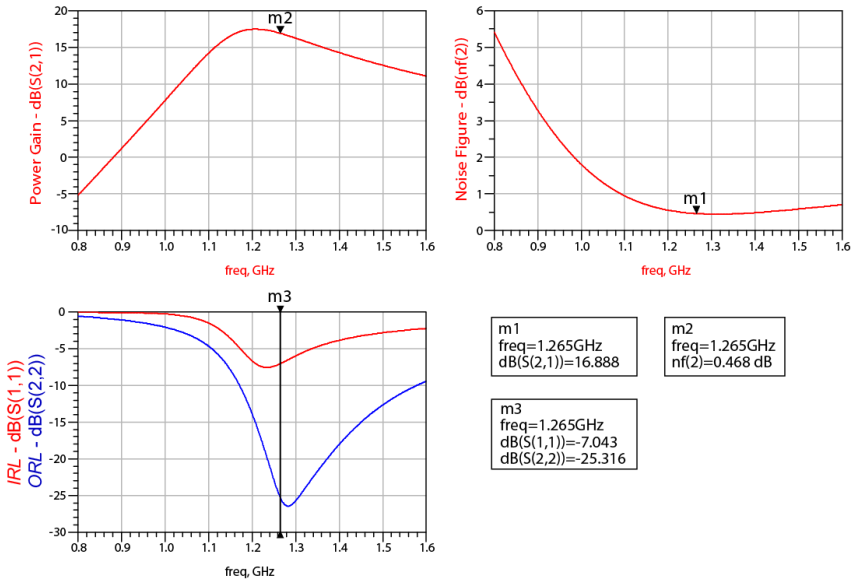


Figure 5.99: Momentum EM Simulated Results of Complete ATF-36077 LNA

These simulated results of the ATF-36077 amplifier indicate that a good noise performance was achieved but with a slightly lower gain than the previous FET LNA. Table 5.14 compares the ideal and EM simulated component values. Here again it is only the components in the input and output matching networks which had to be adjusted to obtain optimum performance of the LNA. These adjustments were necessary due to the Momentum software simulation taking into account the parasitic characteristics of the substrate material used.

Table 5.14: Comparison of Component Values Between Different Simulations

Component and Description	Ideal Simulation value	EM Simulation Value
Active device (ATF-36077)	N/A	N/A
Biasing Resistor (R_D)	330 Ω	330 Ω
Biasing Resistor (R_{S1}, R_{S2})	39 Ω, 36 Ω	39 Ω, 36 Ω
Stabilising Resistor (R_{stab})	680 Ω	680 kΩ
Input Match Capacitor (C_1)	0.49 pF	0.8 pF
Output Match Capacitor (C_2)	1.73 pF	1.5 pF
Decoupling Capacitor (C_3, C_4, C_5)	1 nF	1 nF
Input Match Inductor (L_1)	19.45 nH	10.0 nH
Output Match Inductor (L_2)	7.07 nH	5.6 nH

5.10.5 Non-linear Performance

The non-linear performance of the LNA was analysed in exactly the same manner as for all of the previously designed LNAs. The simulation setup to obtain the 1 dB compression point is illustrated in Figure 5.100 with the results in Figure 5.101.

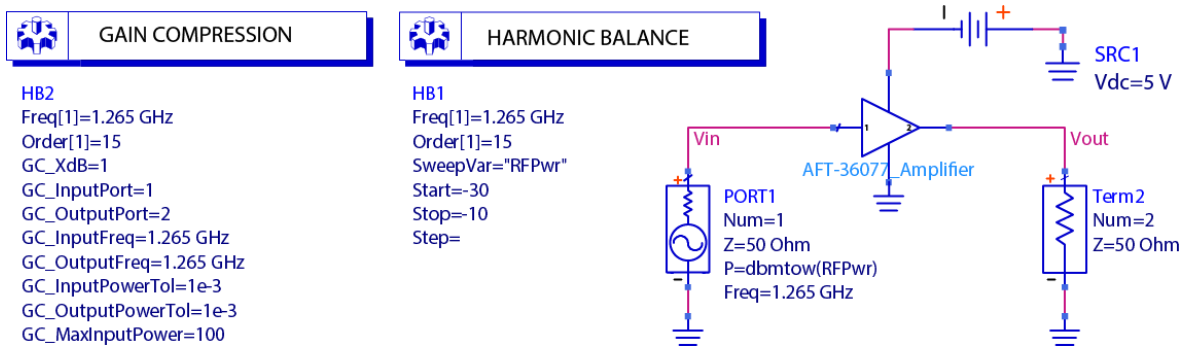


Figure 5.100: P_{1dB} Simulation Setup

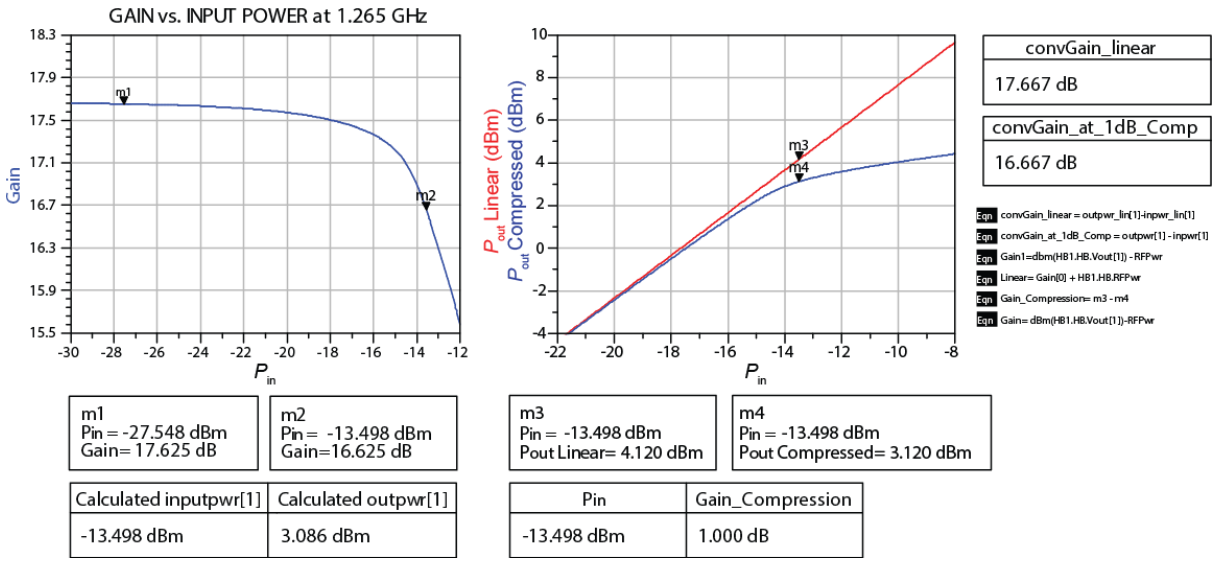


Figure 5.101: Results for P_{1dB} Simulation

The simulated results in Figure 5.101 indicate that the IP_{1dB} is at −13.498 dBm and the OP_{1dB} point is at 3.086 dBm which means that the maximum output power obtainable from this LNA is just above 2 mW. The simulation for the IP_3 point is illustrated in Figure 5.102 with the results in Figure 5.103.

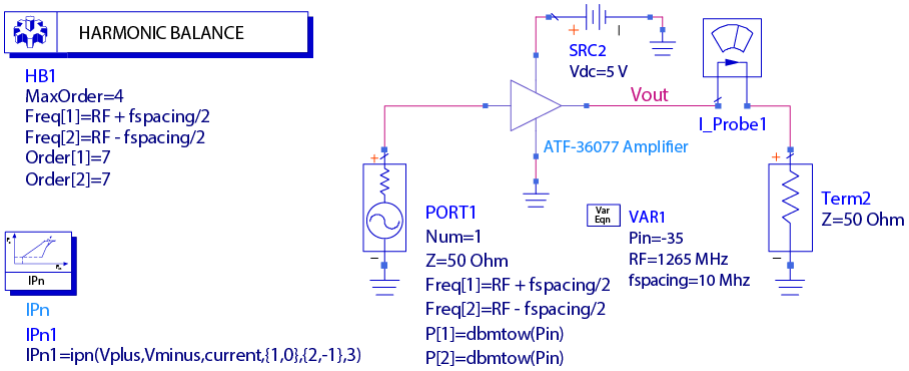
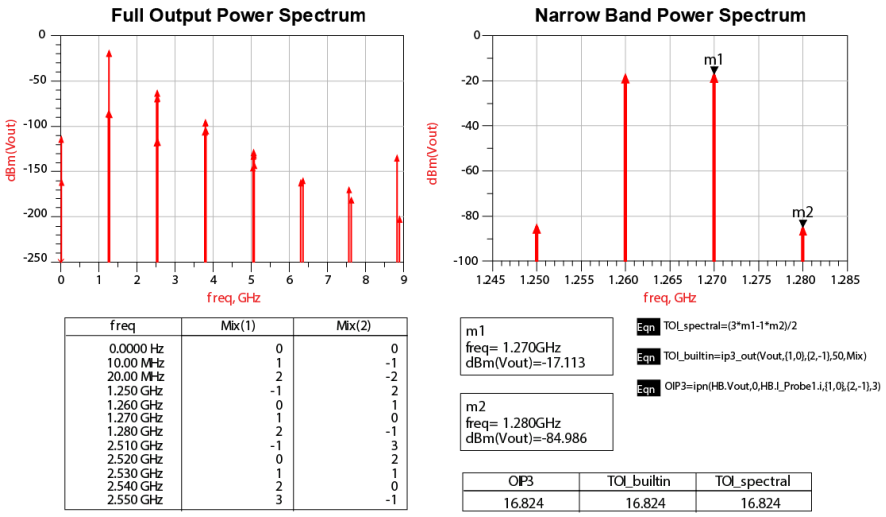


Figure 5.102: Third Order Intercept Simulation Setup



freq	Mix(1)	Mix(2)
0.0000 Hz	0	0
10.00 MHz	1	-1
20.00 MHz	2	-2
1.250 GHz	-1	2
1.260 GHz	0	1
1.270 GHz	1	0
1.280 GHz	2	-1
2.510 GHz	-1	3
2.520 GHz	0	2
2.530 GHz	1	1
2.540 GHz	2	0
2.550 GHz	3	-1

OIP3	TOI_builtin	TOI_spectral
16.824	16.824	16.824

Figure 5.103: Results for IP_3 Simulation

A summary of the results for the ATF36077 LNA is listed in Table 5.15.

Table 5.15: Summary of Simulated Results for ATF-36077 LNA

	NF	Gain	*IRL*	*ORL*	IP_{1dB}	OP_{1dB}	OIP_3
Ideal simulation	0.495 dB	19.084 dB	−1.878 dB	−14.001 dB	-	-	-
EM simulation	0.468 dB	16.888 dB	−7.043dB	−25.316 dB	−13.490 dBm	3.086 dBm	16.820 dBm

Chapter 6

Band-pass Filter Design

In this chapter the process followed to design various band-pass filters will be discussed in detail and decisions that were made are explained and motivated. As stipulated in Capter 4, the amount of insertion loss caused by the filter must be a minimum within the pass-band and out of band signals should be attenuated maximally. An equally important parameter of this filter is the phase response thereof. When using a QPSK modulation scheme, the system is very sensitive to phase distortion, meaning that the response of the band-pass filter should be linear and phase information of the in-phase (*I*) and quadrature (*Q*) channels should be preserved throughout the entire link.

6.1 Design Procedure and Specifications

In designing an appropriate band-pass filter, a lumped element filter will first be designed, followed by some filters implemented in microstrip. At 1265 MHz, lumped components operate well and are regularly used, but one might encounter other problems that will be discussed later in this chapter. In design applications that are sensitive to losses or the effects of parasitic elements caused by lumped components, the use of microstrip implementations of the components becomes more optimal. Unfortunately, when the physical size of the filter is restricted by the limited space available as well as components being implemented in microstrip, implementing a filter at 1265 MHz may be practically not possible since a single wavelength is 23.7 cm long, meaning that a quarter wavelength is about 6 cm long, resulting in a physically large filter. Several aspects need to be taken in consideration before starting the design of the filter. The following specifications must be met by the band-pass filter.

Table 6.1: Band-pass Filter Specifications

Parameter	Symbol	Specification
Operating Frequency	f_c	1265 MHz
Lower Stopband Edge	f_{S1}	1170 MHz
Passband	f_P	1250−1280 MHz
Upper Stopband Edge	f_{S2}	1370 MHz
Passband Ripple		< 1 dB
Insertion Loss	S_{21}	< 4 dB

6.2 Lumped Element Filter Design

The lumped element filter was designed using Equations 4.6 - 4.12 together with the different element values for the various types of filter responses as listed by Pozar (2005:394; 396; 389). A third order Chebychev filter with a 0.5 dB passband ripple would give the required response since it is characterised by a sharp roll off rate, and the passband ripple can be chosen to meet the design specifications. Figures 6.1 and 6.2 illustrate ideal circuit implementation of the two possible solutions for the design of the lumped element filter, with the results of the simulations shown in Figure 6.3.

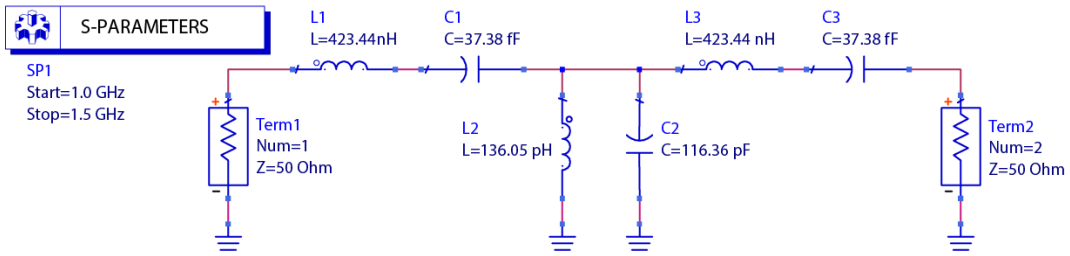


Figure 6.1: Ideal Circuit of Lumped Element Filter with Series Component First

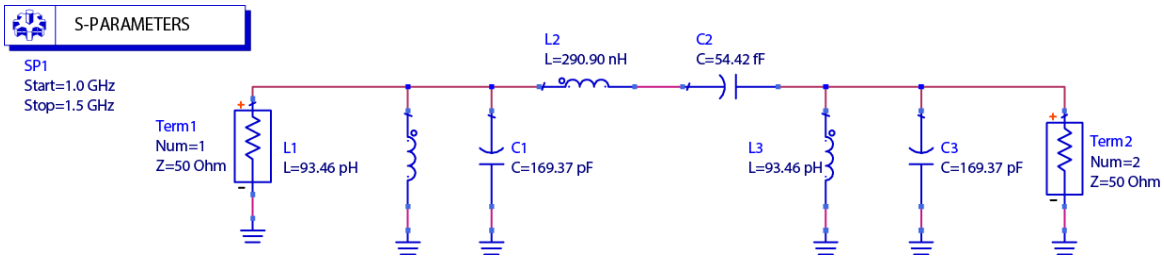


Figure 6.2: Ideal Circuit of Lumped Element Filter with Parallel Component First

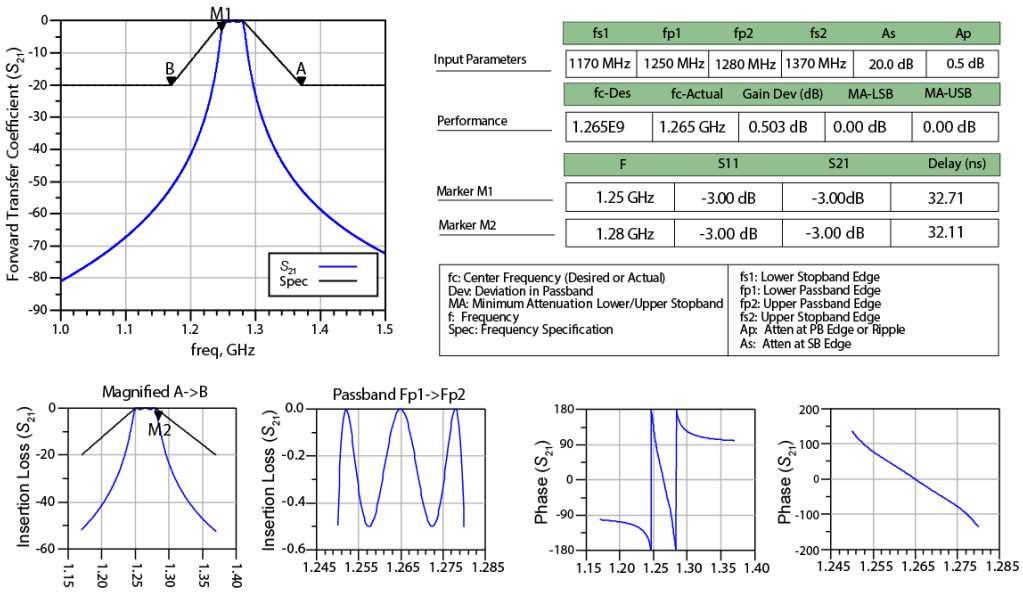


Figure 6.3: Simulated Results of Ideal Lumped Element Filter

Since both filters were designed using exactly the same criteria, and the simulations were implemented using ideal components, both filter simulations gave exactly the same response. It is only the circuit topology that vary, which allows the designer to choose the best filter configuration to use in the system. Figure 6.3 shows that the filter more than meets the specifications, however, it is not possible to practically implement this filter because some of the component values are very small and unobtainable.

6.3 Coupled Line Filter Design

Since it is not practically feasible to implement the lumped element filter, an alternative is to implement the band-pass filter using microstrip transmission lines and a coupled line filter topology. To design this type of filter, Equations 4.17, 4.18, 4.19, 4.20 and 4.21, together with the filter element values as given by Pozar (2005:394; 396; 398) for different filter response types were implemented using Matlab, as shown in Appendix B. To satisfy the specifications, a third order Chebychev filter with a 0.5 dB passband ripple and a fractional bandwidth of 2% will be sufficient. The process described in Section 4.8 was closely followed and the first step was to determine the even- and odd-mode characteristic impedances. The calculated values are listed in Table 6.2.

Table 6.2: Calculated Even and Odd Mode Impedances

Z_{0e_1}	Z_{0o_1}	Z_{0e_2}	Z_{0o_2}	Z_{0e_3}	Z_{0o_3}	Z_{0e_4}	Z_{0o_4}
58.8053 Ω	43.5285 Ω	51.4475 Ω	48.6318 Ω	51.4475 Ω	48.6318 Ω	58.8053 Ω	43.5285 Ω

To verify the accuracy of the calculations, and before continuing with the remainder of the design process, the filter was simulated in ADS using the even and odd mode impedances to verify the

correctness and accuracy of the calculations. The simulation setup using odd and even mode impedances is illustrated in Figure 6.4 with the results in Figure 6.5.

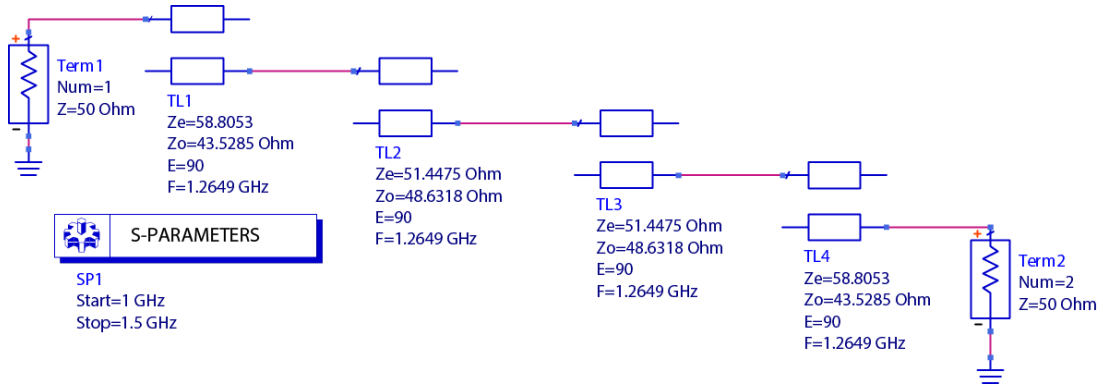


Figure 6.4: Coupled Line Filter Simulation Setup Using Even and Odd Mode Impedances

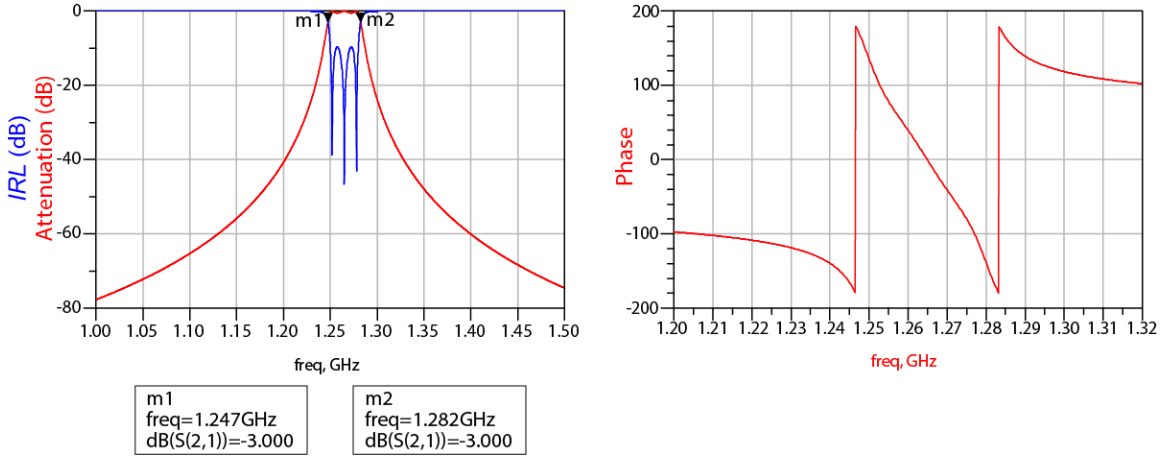


Figure 6.5: Simulated Magnitude and Mhase Response of an Ideal Coupled Line Filter

Figure 6.5 confirms that the calculations were accurate and that a linear phase response throughout the passband was achieved. To transform the filter from an ideal filter that uses even and odd mode impedances to a microstrip line implemented filter, the synthesis method was used. It requires Equations 4.22 through to 4.28 to be programmed into Matlab. The results provide the physical dimensions of the individual microstrip segments and the spacing between them. Another way to obtain the microstrip dimensions is to use the built in tool in ADS called LineCalc. The user enters the even (Z_e) and odd (Z_o) mode impedances, the characteristic impedance (Z_0) and the electrical length (E_EFF) of the segment in degrees together with the characteristic properties of the substrate, Rogers 4003C, and the program will synthesize the parameters and provide the width (W) and length (L) of each coupled line segment, and the spacing (S) between them. The graphic user interface (GUI) of *LineCalc* is illustrated in Figure 6.6.

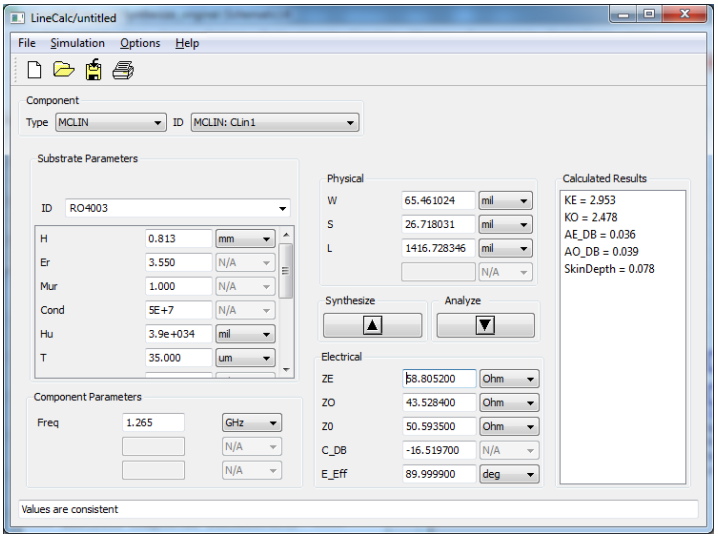


Figure 6.6: ADS LineCalc Microstrip Coupled Line Analysis/Synthesis Tool

Figure 6.7 shows the circuit representation of the coupled line filter after synthesizing each component with the simulated results illustrated in Figure 6.8.

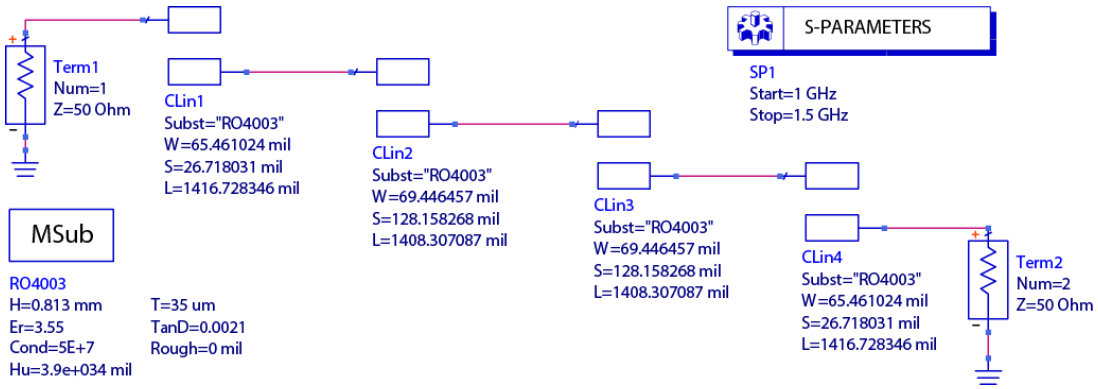


Figure 6.7: Ideal Circuit Representation of Synthesised Coupled Line Filter

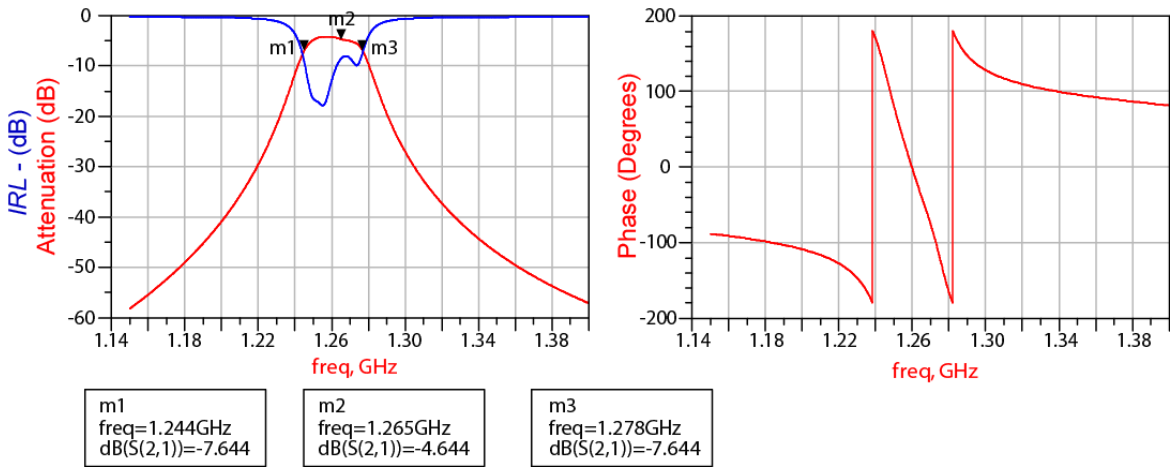


Figure 6.8: Simulated Results of Synthesised Ideal Coupled Line Filter

The magnitude and phase responses in Figure 6.8 show that the cutoff frequencies are correct but the insertion loss is excessive. The magnitude response can now be optimised for less insertion loss in the passband. It must be noted that the percentage bandwidth, defined in Equation 4.8, of the filter is only 0.024% and when working with a fractional bandwidth of less than 0.05% extra care must be taken in the design of the filter because achieving a low insertion loss under these circumstances is extremely difficult. Figure 6.9 illustrates the optimised filter response.

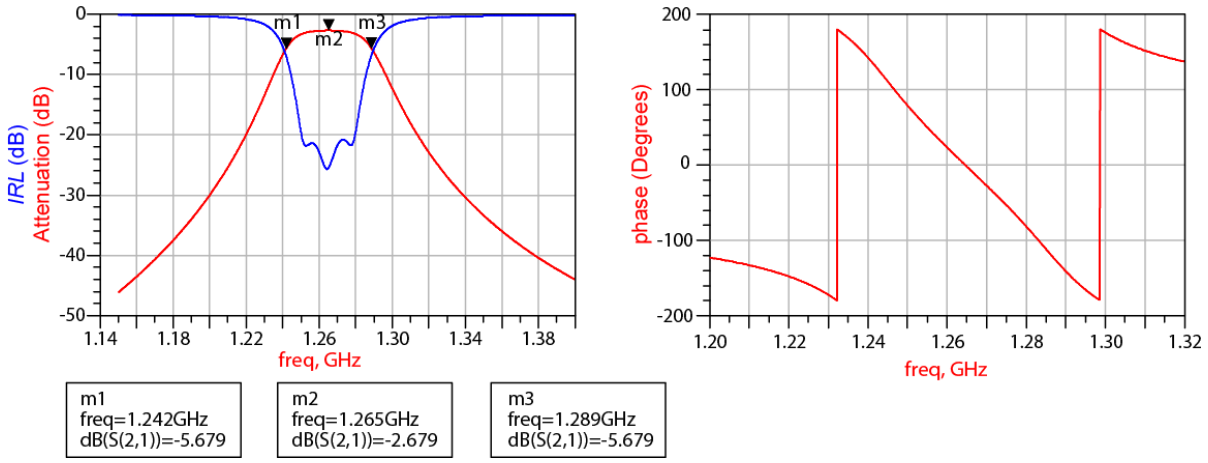


Figure 6.9: Optimised ideal Coupled Line Filter Response

The next step is to simulate the physical structure of the filter, implemented on Rogers RO4003 substrate material, using Momentum EM simulation software. These EM simulated results provide the practically achievable performance parameters and allow for filter optimisation before actual physical implementation. The physical structure of the filter is shown in Figure 6.10. and Figure 6.11 illustrates the Momentum EM simulation setup with the simulated response in Figure 6.12.

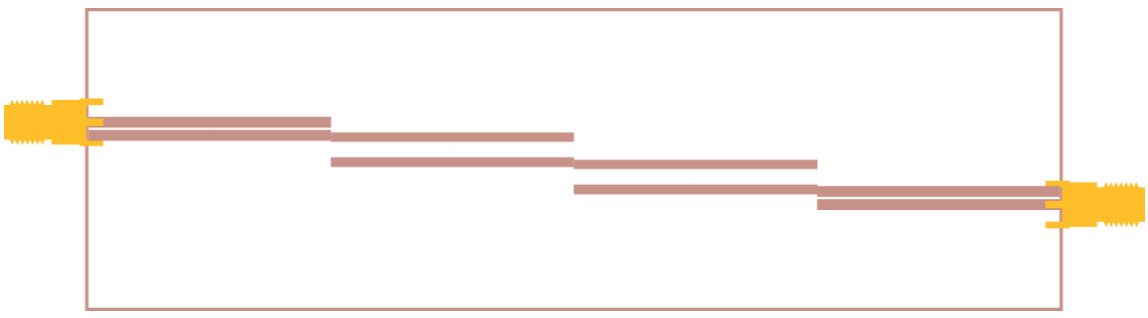


Figure 6.10: Physical Structure of Coupled Line Band-pass Filter

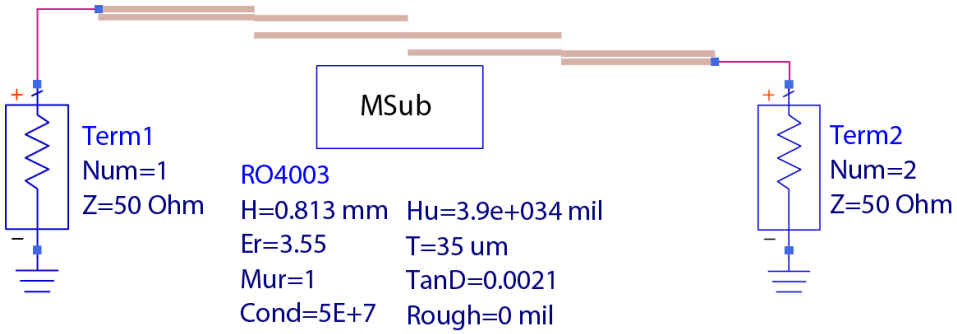


Figure 6.11: Momentum EM Simulation Setup of Coupled Line BPF

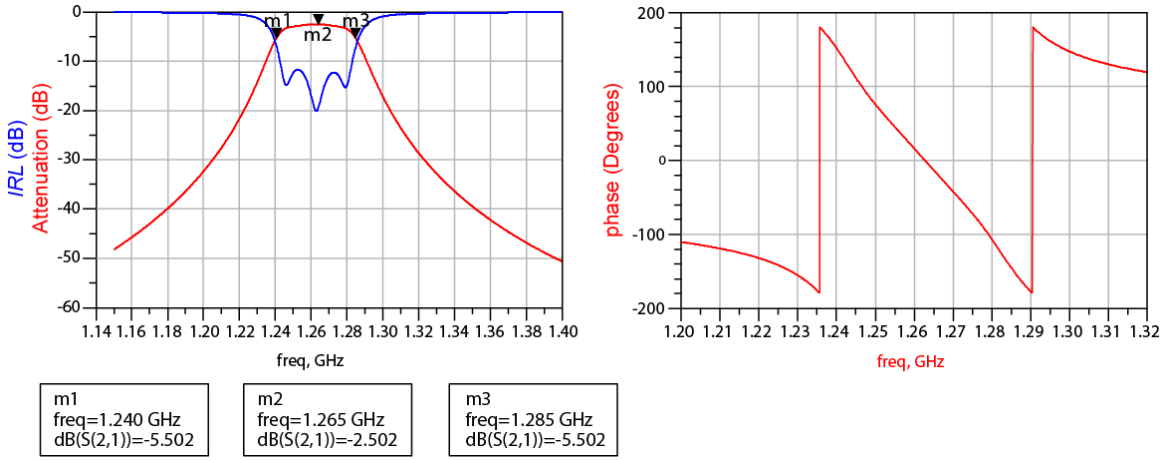


Figure 6.12: Band-pass Filter Response from Momentum EM Simulation

Figure 6.12 shows a slight degradation in the insertion loss of the filter when compared to the results of the ideal BPF in Figure 6.9. This is expected and is due to the EM simulation taking into account the actual behaviour and physical effects of the substrate material at the frequency of operation. The performance of the filter is still within specification and the response is almost identical to the ideal filter simulations, confirming that the design procedure was accurate.

The total length of the microstrip filter that was physically implemented is 14.2 cm and is too long and impractical to implement on a 10 cm × 10 cm printed circuit board. To reduce the physical size of the filter, the topology was modified into a more compact design. The filter structure was optimised to maintain the performance of the previous topology and compensate for the bends in the new layout. Figure 6.13 shows the modified topology of the filter with the filter performance illustrated in Figure 6.14.

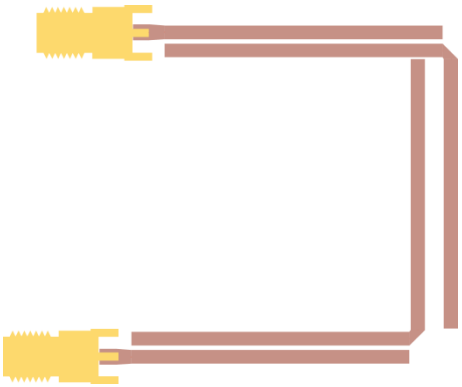


Figure 6.13: Modified Topology of Coupled Line Filter

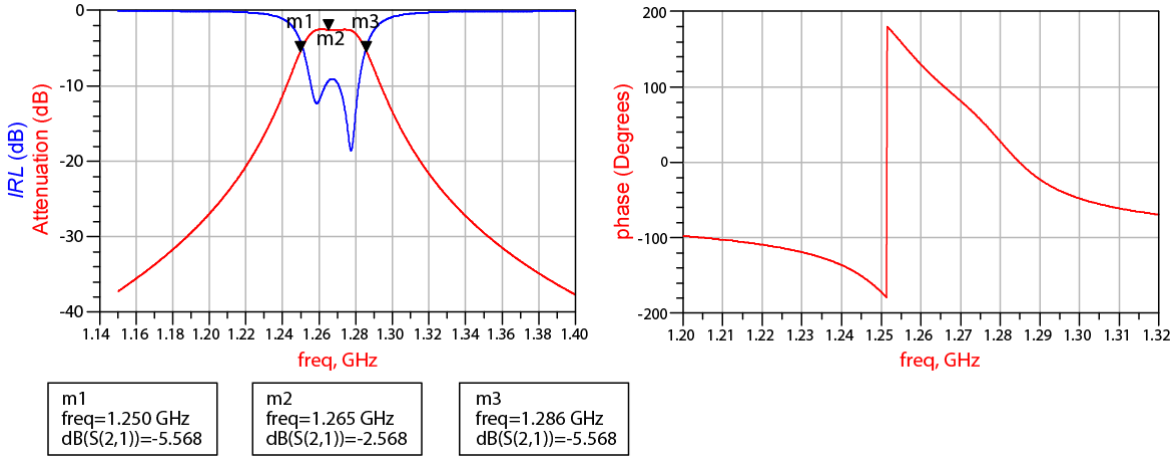


Figure 6.14: Modified Coupled Line Filter Response

When comparing the results in Figure 6.14 to those in Figure 6.12, the performance of the modified filter is the same as those of the original filter shown in Figure 6.10.

Chapter 7

Measurements and Results

7.1 Introduction

In this chapter the process of equipment setup and performance measurement of the constructed amplifiers and filters will be presented in detail. The final measured parameters of each circuit are illustrated in graphical format and then compared to their simulated values. Finally, all results are listed in table format and similarities and/or differences are discussed and explained.

7.2 Measuring Equipment and Calibration

The only measuring instrument that is able to provide results in the same format as the simulations is a *vector network analyser* (VNA). The VNA can simultaneously analyse and provide all of the *S*-parameters related to a circuit. Prior to measurement, the VNA must be calibrated to compensate for losses in the cables and to set the frequency range and amount of frequency points for the measurements that will be made. A full two port calibration was performed using the SOLT (Short-Open-Load-Thru) calibration procedure. The VNA used for the circuit measurements is the Agilent 8753ES 30 kHz - 6 GHz network analyser and the Agilent 85033D 3.5 mm calibration kit was used for calibration.

When measuring the *S*-parameters of the amplifier circuits, it is crucial that the following procedure is followed or the risk of damaging the active device increases greatly. Firstly the DC supply is connected and then the output port of the amplifier is connected to port two of the VNA. Lastly, port one of the VNA is coupled to the input port of the amplifier. The 1dB compression point is also measured using the VNA. Instead of using a frequency sweep as in the case of the *S*-parameters measurements, a power sweep was selected at a specific frequency. The 1dB compression measurement is done by sweeping the input power and placing markers in the linear power gain region and finding the point on the curve where the gain drops off by 1dB and calculating the respective input and output 1dB compression points.

To perform the third-order intercept measurements on the amplifiers, two signals must be simultaneously applied to the input port of an amplifier. These two identical signals were generated using two Agilent N9310A 9 kHz – 3 GHz signal generators and coupled together using a three-port combiner to create a two-tone input signal. Section 3.8 states that the two signals must be spaced close enough together so that their third order products fall within the 3 dB passband of the amplifier. Generating signals at 1.26 GHz and 1.27 GHz respectively using the two signal generators and combining them using an Agilent 11636A DC to 18GHz RF signal combiner will result in third order products at 1.25 GHz and 1.28 GHz. The output port of the amplifier was connected to an Agilent E4404B 9 kHz – 6.7 GHz series spectrum analyser and by placing markers on the generated signals and respective third order tones the OIP_3 value was calculated using Equation 3.16.

The noise figure of each LNAs was measured using an Agilent N8974A 10 MHz - 18 GHz series *noise figure analyser*. The noise figure analyser was firstly calibrated and then actual measurements were performed using a series noise source connected to the input port of the respective amplifier and the output port then connected to the analyser itself where the *NF* and gain parameters were displayed.

All of the LNAs and the filters were implemented using Roger's RO4003 high frequency substrate for best results. The substrate is ideal for high frequency design and features a very low dissipation factor and dielectric constant both resulting in minimal losses and good high frequency performance. Vias were used to implement the required connections to the ground plane. These strategically placed vias prevent the formation of ground loops which may cause unwanted feedback and instability in a circuit. A laser rapid prototyping machine, supplied by LPKF Laser & Electronics and capable of working down to track widths and spacings of 50 µm, was used to manufacture the PCBs.

7.3 LNA Construction and Measurements

All of the amplifiers were constructed using the component values and substrate material that were simulated and listed for each amplifier in Chapter 5. The measurements were performed as described in the previous section. When measured, the performance parameters such as the power gain, input return loss and output return loss were saved in such a format so that it can be imported and re-simulated in *ADS* for post processing. Screen captures of the remainder of the performance parameters were taken from the test equipment while doing the measurements on the device under test (DUT). To calculate the IP_3 value for the constructed amplifiers, Equation 3.20 was used.

7.3.1 The BFP-740 Lumped Element Matching Network LNA

The BFP-740 amplifier using lumped elements for the matching networks was designed for best possible noise performance and both the ideal component and the EM real-world simulations indicated a sub 1 dB noise figure was achievable. The constructed amplifier is shown in Figure 7.1.

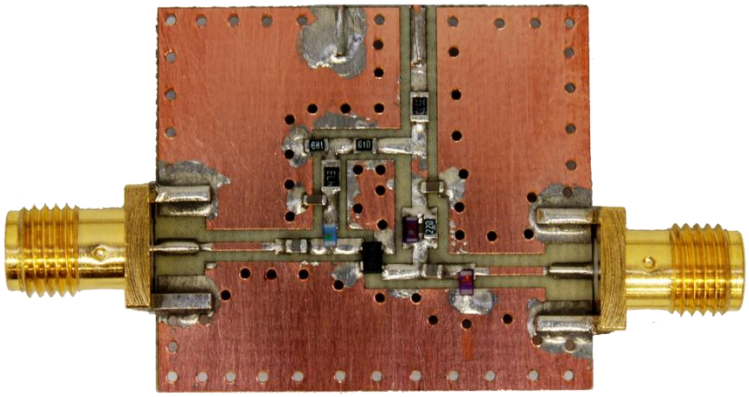


Figure 7.1: Constructed BFP-740 LNA Using Lumped Element Matching Components

The measurements for Gain, *IRL*, *ORL*, *NF*, IP_{1db} and OIP_3 are shown in Figures 7.2, 7.3, 7.4, and 7.5 respectfully. The figures were obtained from the screenshots taken of the display of the actual measuring instrument during the measurement process.

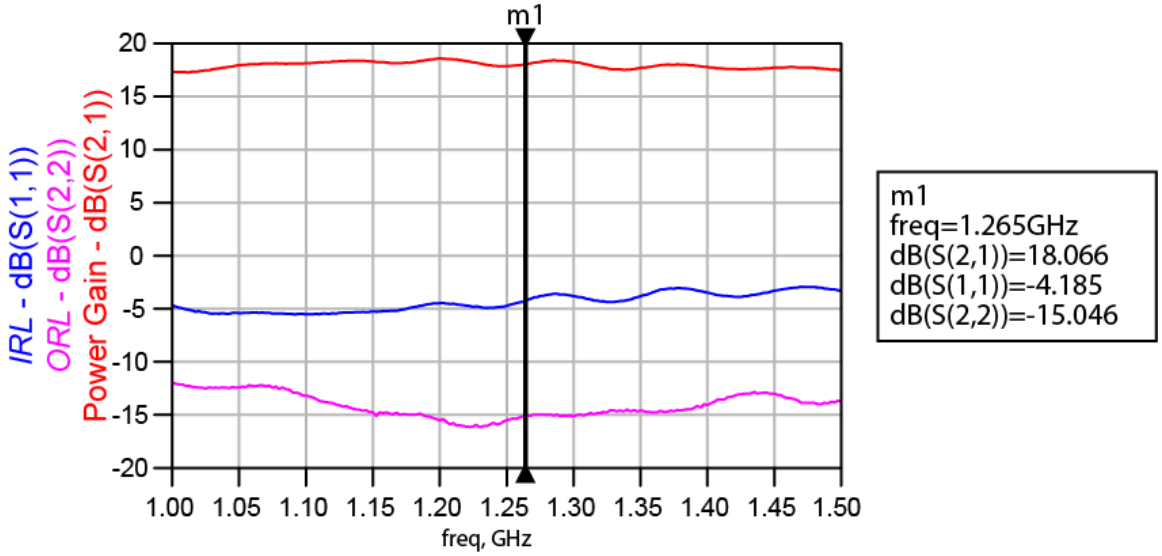


Figure 7.2: Measured Power Gain, *IRL* and *ORL* of the BFP-740 Lumped Element Amplifier

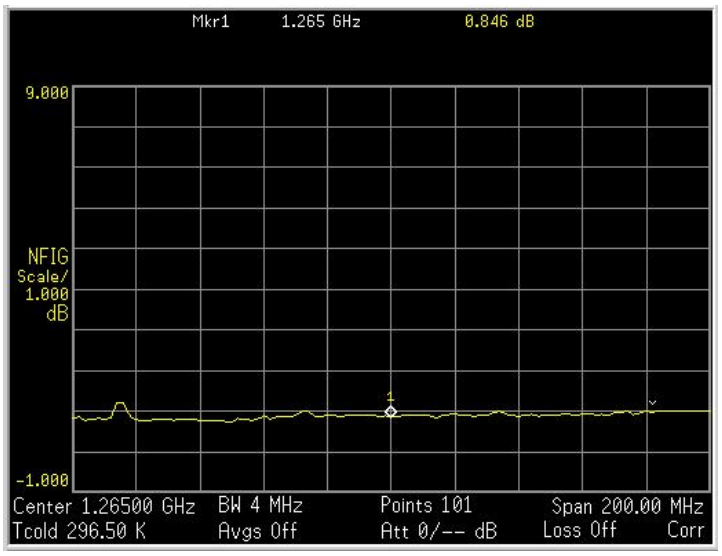


Figure 7.3: Measured *NF* of the BFP-740 Lumped Element Amplifier

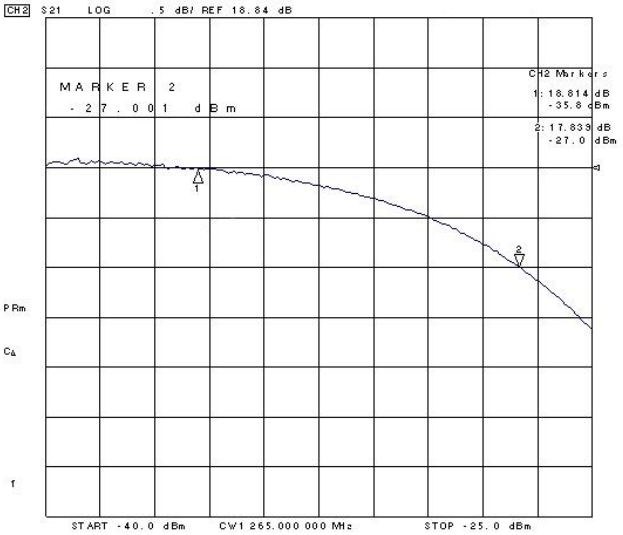


Figure 7.4: Measured IP_{1dB} of the BFP-740 Lumped Element LNA

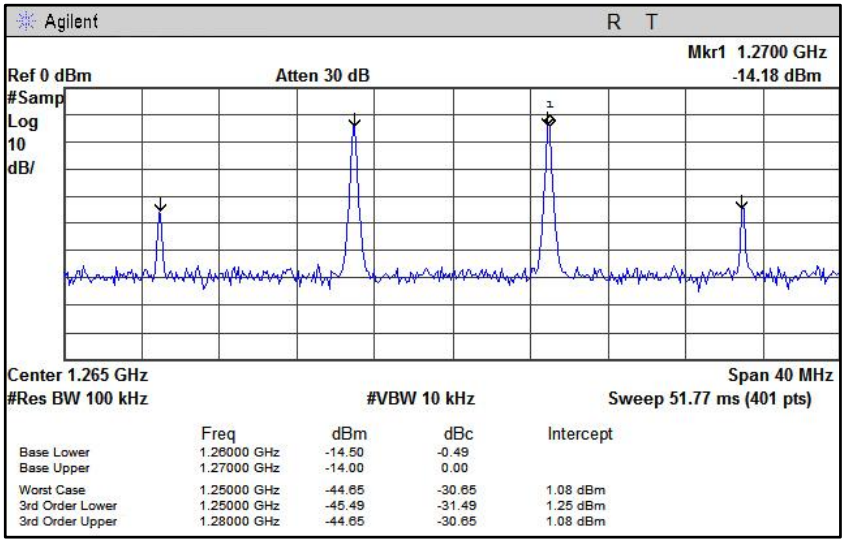


Figure 7.5: Measured OIP_3 point for the BFP-740 Lumped Element LNA

The measured results for the lumped element BFP-740 LNA are summarised in Table 7.1.

Table 7.1: Summary of the Measured Results of the BFP-740 Lumped Element LNA

	NF	Gain	*IRL*	*ORL*	IP_{1dB}	OP_{1dB}	OIP_3
Measured results	0.846 dB	18.066 dB	−4.185 dB	−15.046 dB	−27.000 dBm	−9.160 dBm	1.250 dBm

7.3.2 The BFP-740 Distributed Element Matching Network LNA

The constructed circuit with the matching components implemented using distributed elements is shown in Figure 7.6. All measurements for Gain, *IRL*, *ORL*, *NF*, IP_{1db} and OIP_3 are shown in Figures 7.7, 7.8, 7.9, and 7.10 respectfully.

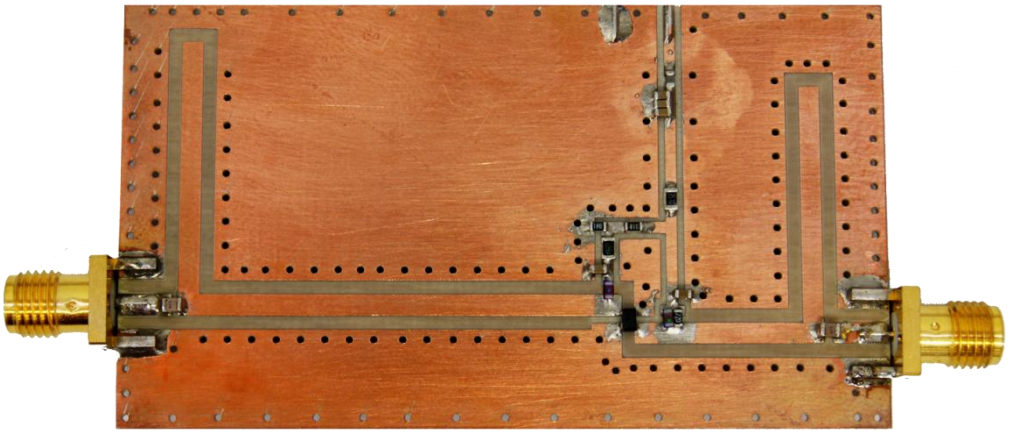


Figure 7.6: Constructed BFP-740 LNA Using Distributed Element Matching

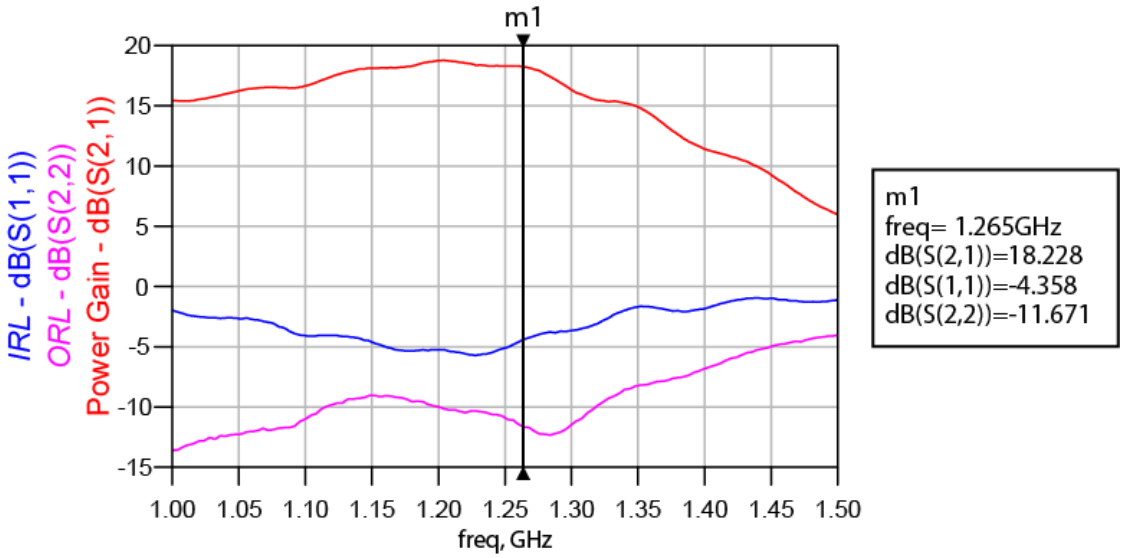


Figure 7.7: Measured Power Gain, *IRL* and *ORL* for of the Distributed Element BFP-740 LNA

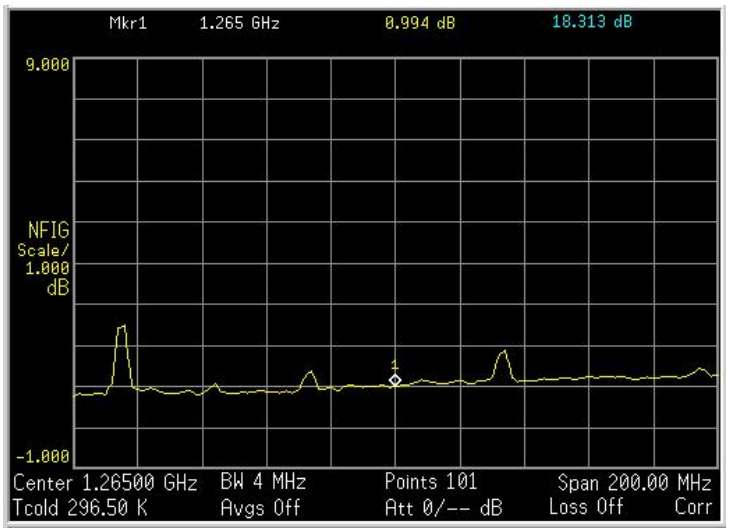


Figure 7.8: Measured *NF* of the Distributed Element BFP-740 LNA

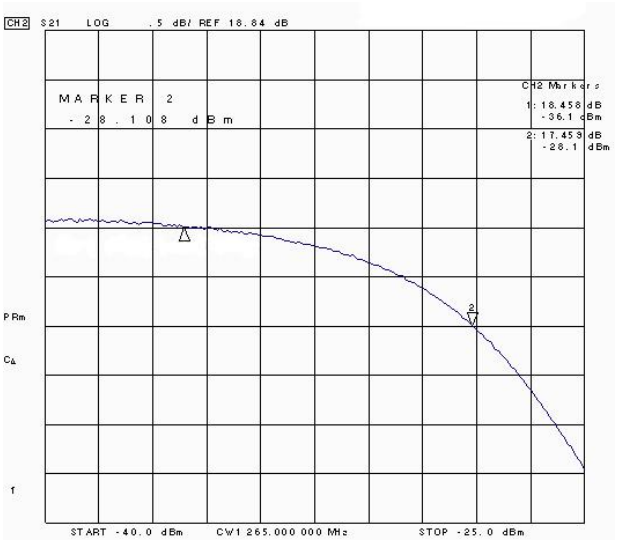


Figure 7.9: Measured IP_{1dB} for the Distributed Element BFP-740 LNA

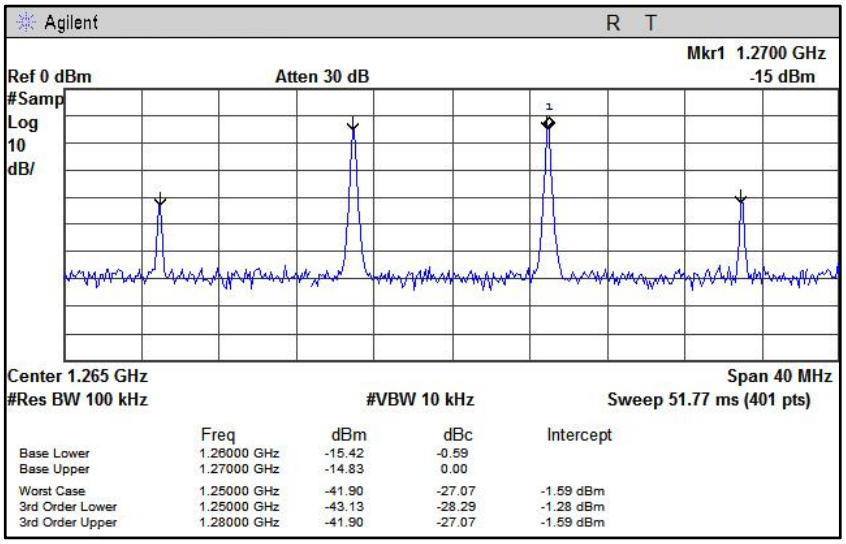


Figure 7.10: Measured OIP_3 Point for the Distributed Element BFP-740 LNA

The measured results for the BFP-740 distributed element LNA are summarised in Table 7.2.

Table 7.2: Summary of the Measured Results for the Distributed Element BFP-740 LNA.

	NF	Gain	*IRL*	*ORL*	IP_{1dB}	OP_{1dB}	OIP_3
Measured results	0.994 dB	18.228 dB	−4.358 dB	−11.671 dB	−28.100 dBm	−10.640 dBm	−1.590 dBm

7.3.3 The ATF-55143 LNA

The constructed LNA is shown in Figure 7.11. All measurements for Gain, *IRL*, *ORL*, *NF*, IP_{1db} and OIP_3 are shown in Figures 7.12, 7.13, 7.14, and 7.15 respectfully.

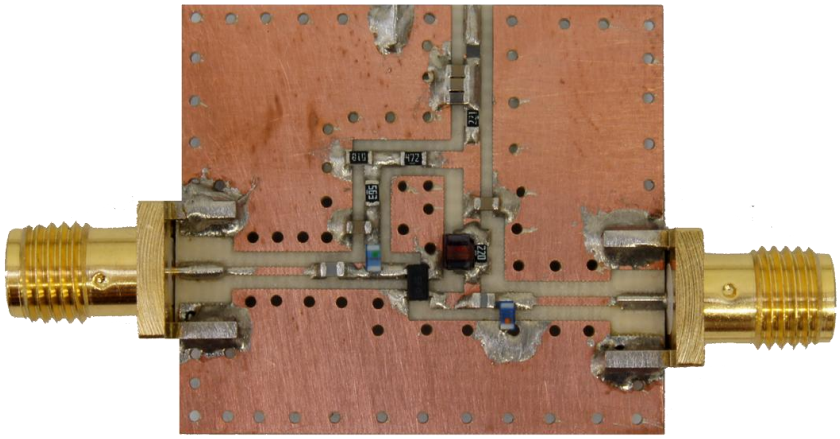


Figure 7.11: The Constructed ATF-55143 LNA

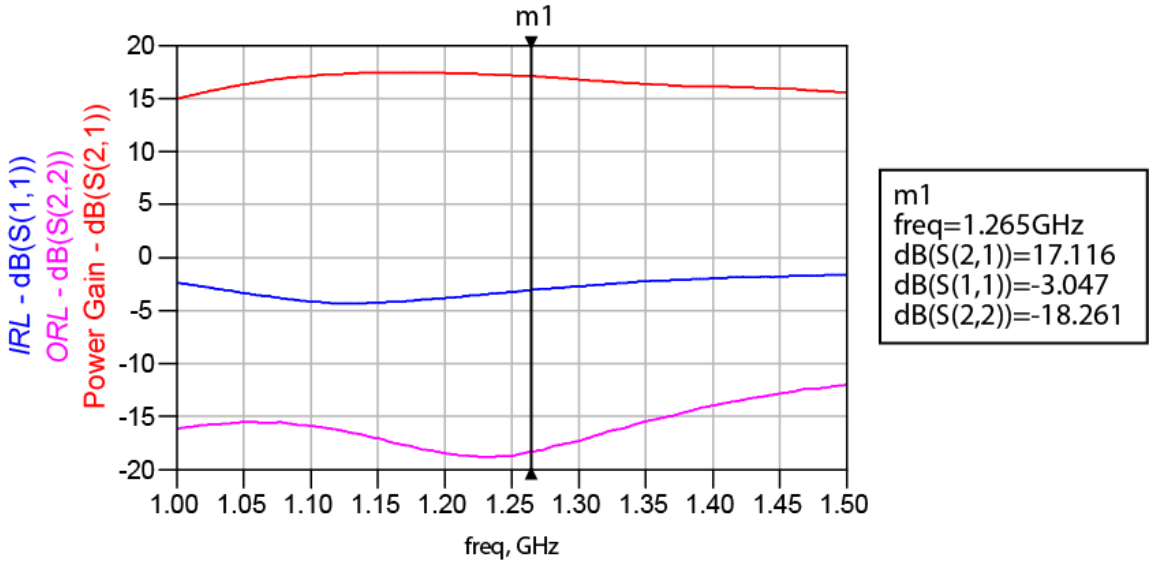


Figure 7.12: Measured Power Gain, *IRL* and *ORL* of the ATF-55142 LNA

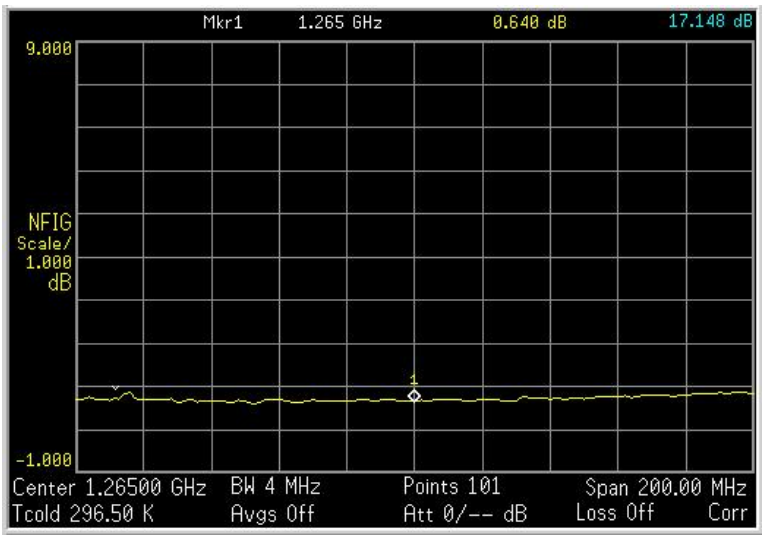


Figure 7.13: Measured *NF* of the ATF-55143 LNA

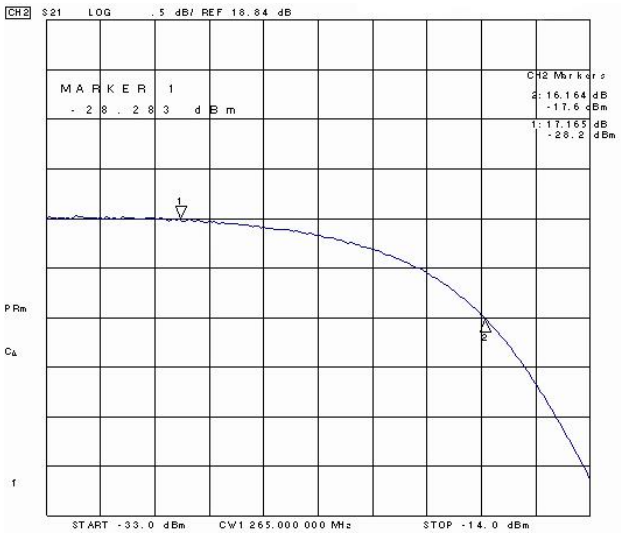


Figure 7.14: Measured IP_{1dB} Point for the ATF-55143 LNA

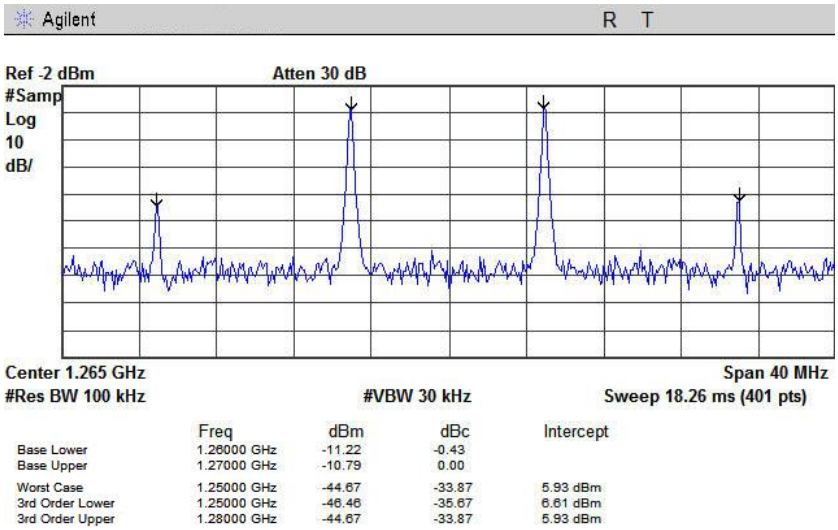


Figure 7.15: Measured OIP_3 Point for the ATF-55143 LNA

Table 7.3: Summary of the Measured Results for the ATF-55143 LNA

	NF	Gain	*IRL*	*ORL*	IP_{1dB}	OP_{1dB}	OIP_3
Measured results	0.640 dB	17.116 dB	−3.047 dB	−18.261 dB	−17.600 dBm	−1.440 dBm	6.610 dBm

7.3.4 The AT-32032 LNA

The constructed LNA is shown in Figure 7.16. All measurements for Gain, *IRL*, *ORL*, *NF*, IP_{1db} and OIP_3 are shown in Figures 7.17, 7.18, 7.19, and 7.20 respectfully.

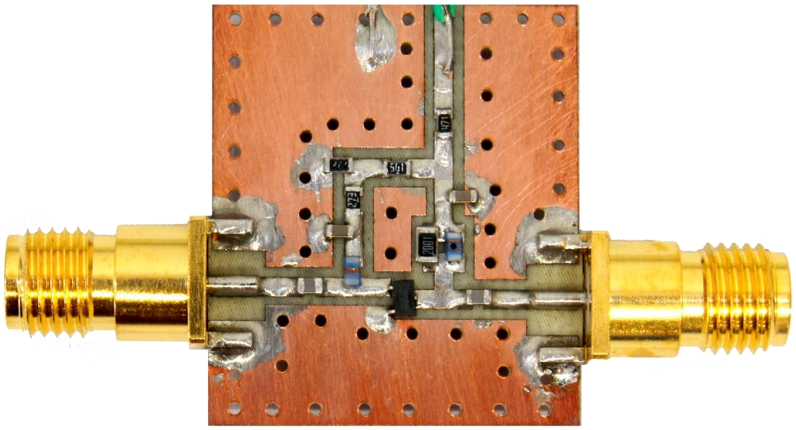


Figure 7.16: The Constructed AT-32032 LNA

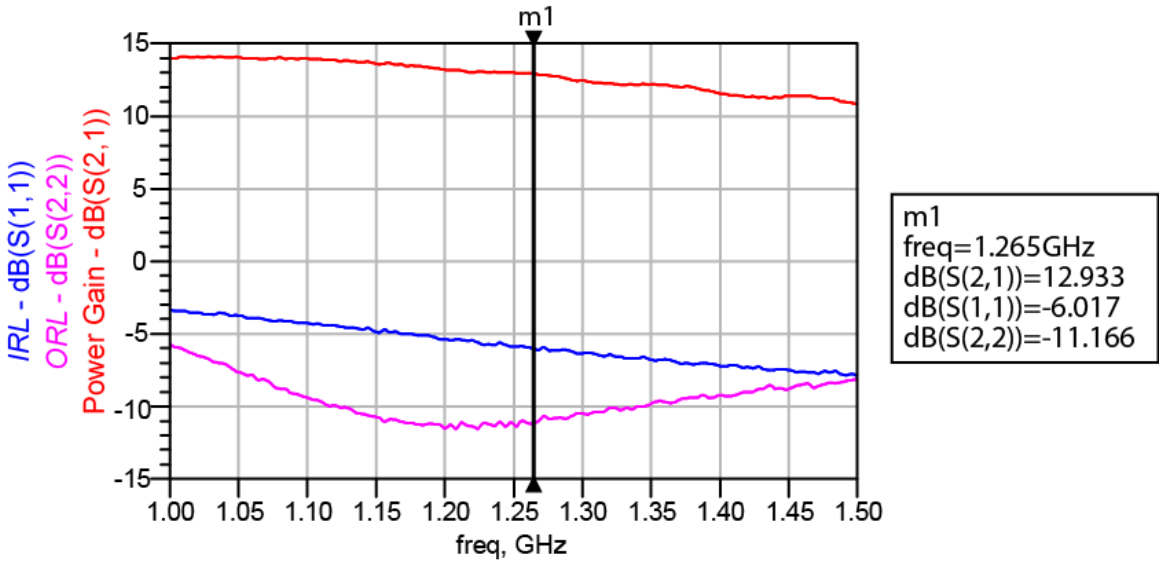


Figure 7.17: Measured Power Gain, *IRL* and *ORL* of the AT-32032 LNA

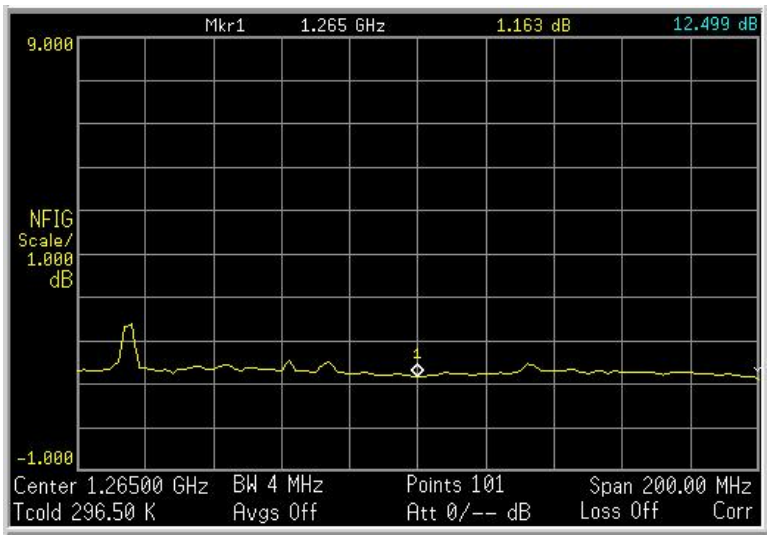


Figure 7.18: Measured *NF* of the AT-32032 LNA

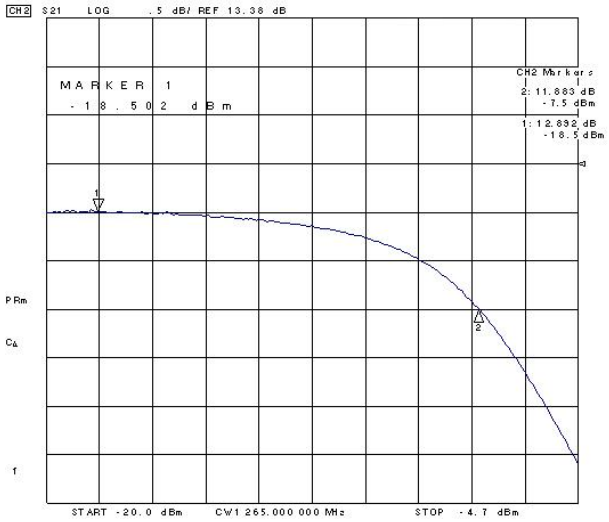


Figure 7.19: Measured IP_{1dB} Point for the AT-32032 LNA

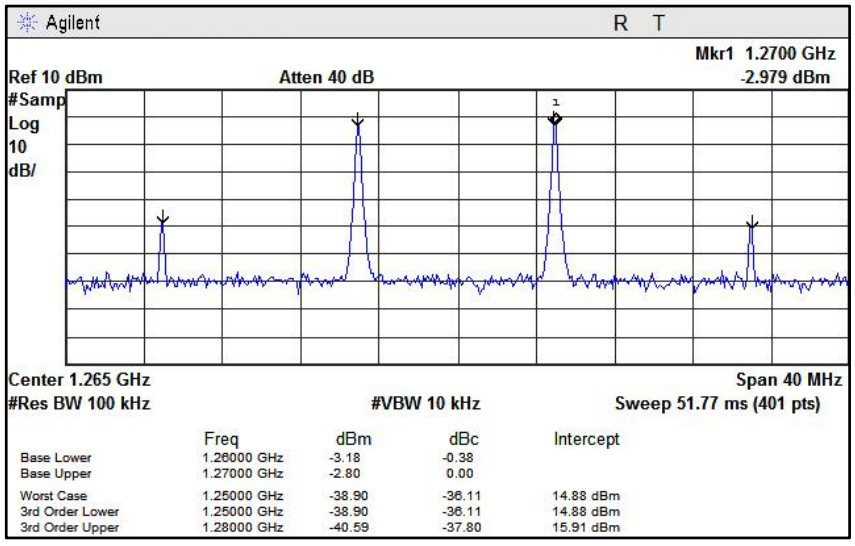


Figure 7.20: Measured OIP_3 Point for the AT-32032 LNA

Table 7.4: Summary of the Measured Results for the AT-32032 LNA

	NF	Gain	*IRL*	*ORL*	IP_{1dB}	OP_{1dB}	OIP_3
Measured results	1.163 dB	12.933 dB	−6.017 dB	−11.166 dB	−7.500 dBm	4.383 dBm	15.910 dBm

7.3.5 ATF-36163 Amplifier Design

The constructed LNA is shown in Figure 7.21. All measurements for Gain, *IRL*, *ORL*, *NF*, IP_{1db} and OIP_3 are shown in Figures 7.22, 7.23, 7.24, and 7.25 respectfully.

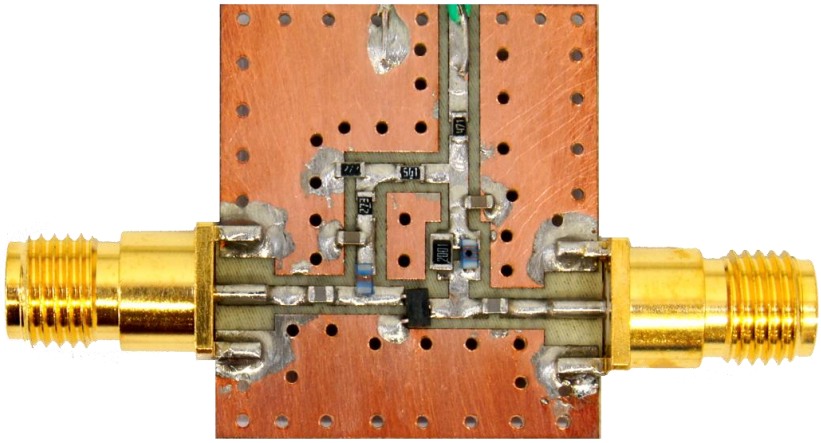


Figure 7.21: The Constructed ATF-36163 LNA

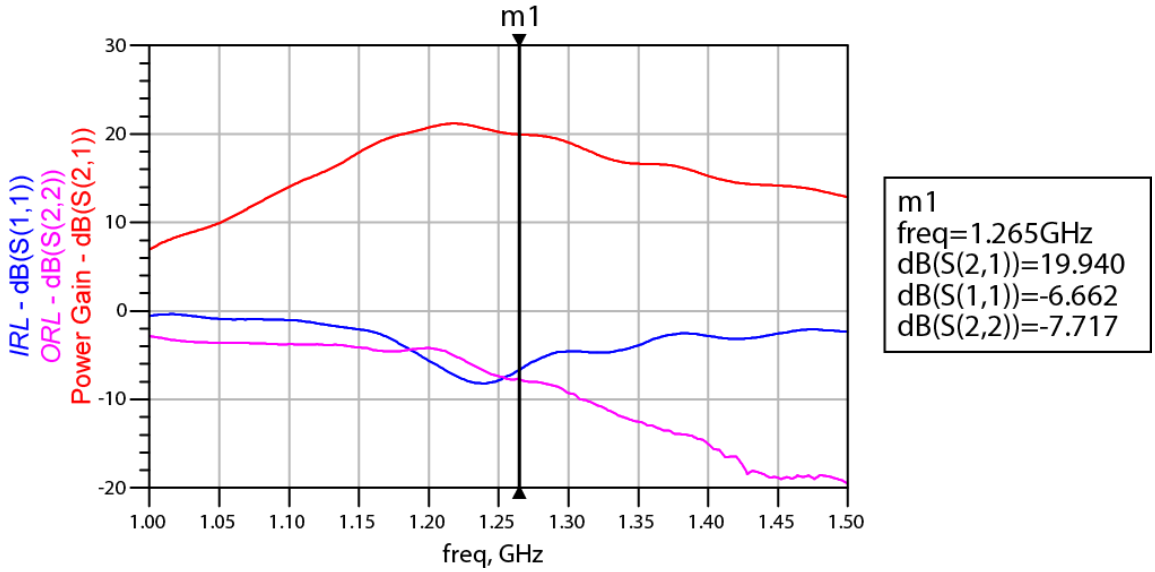


Figure 7.22: Measured Power Gain, *IRL* and *ORL* of the ATF-36163 LNA

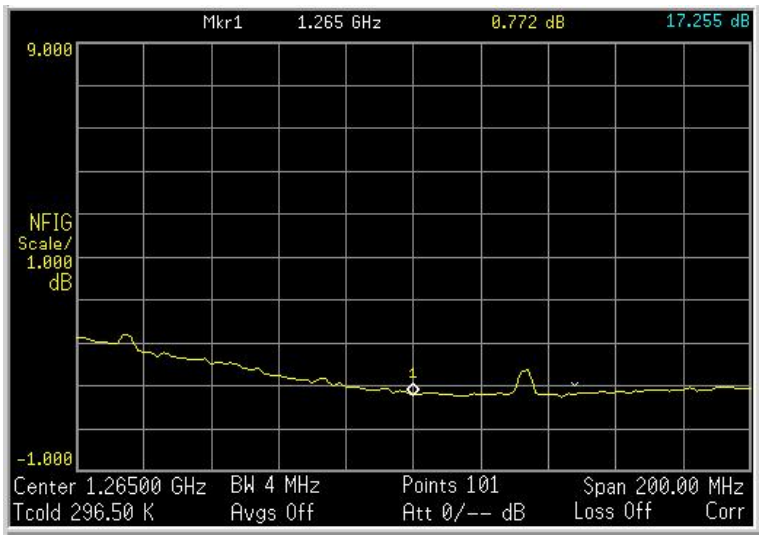


Figure 7.23: Measured *NF* of the ATF-36163 LNA

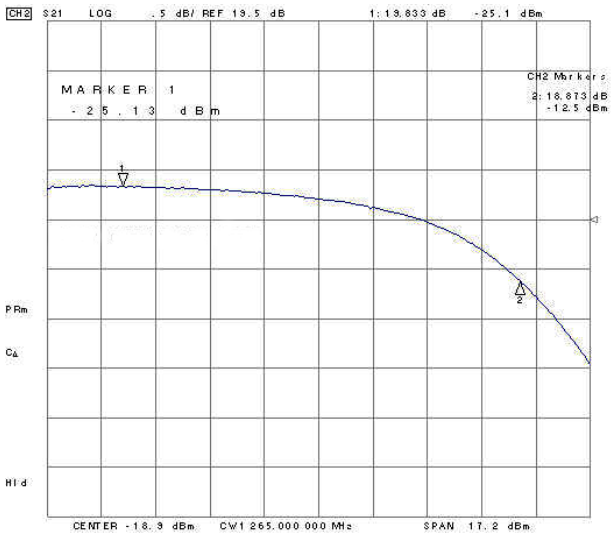


Figure 7.24: Measured IP_{1dB} Point for the ATF-36163 LNA

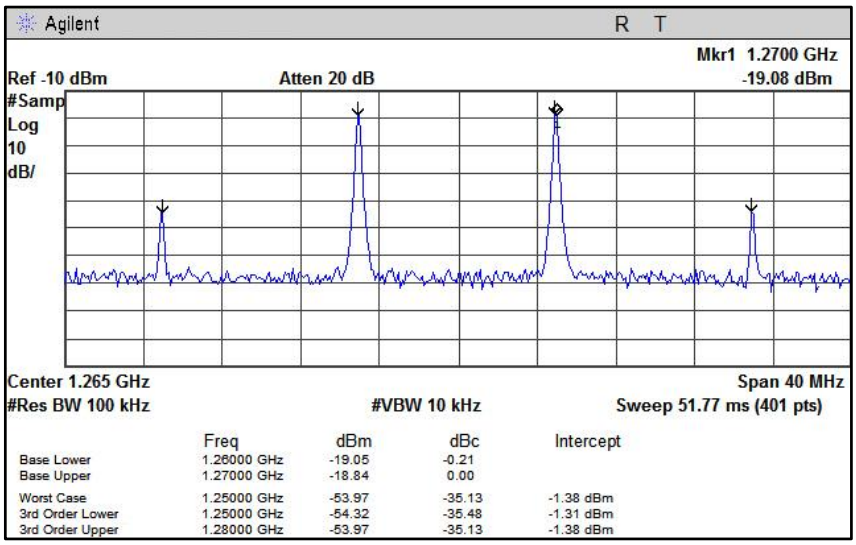


Figure 7.25: Measured OIP_3 Point for the ATF-36163 LNA

Table 7.5: Summary of the Measured Results for the ATF-36163 LNA

	NF	Gain	*IRL*	*ORL*	IP_{1dB}	OP_{1dB}	OIP_3
Measured results	0.722 dB	19.940 dB	−6.662 dB	−7.717 dB	−12.500 dBm	6.373 dBm	−1.380 dBm

7.3.1 The ATF-36077 LNA

The constructed LNA is shown in Figure 7.26. All measurements for Gain, *IRL*, *ORL*, *NF*, IP_{1db} and OIP_3 are shown in Figures 7.27, 7.28, 7.29, and 7.30 respectfully.

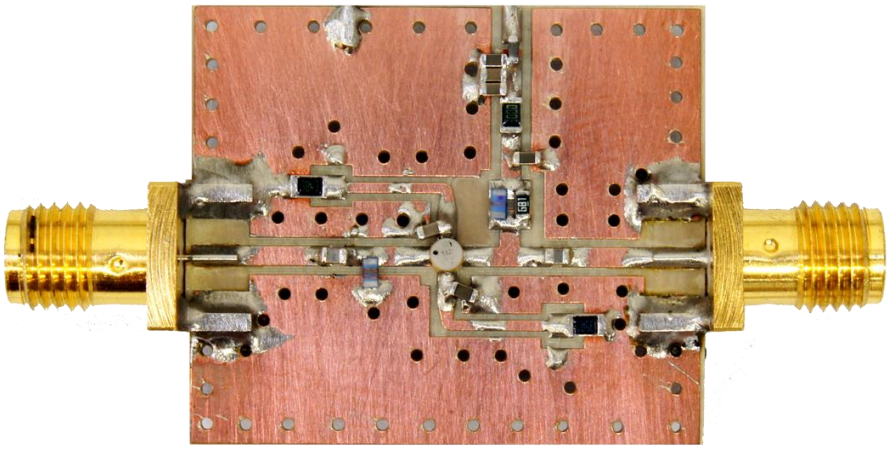


Figure 7.26: The Constructed ATF-36077 LNA

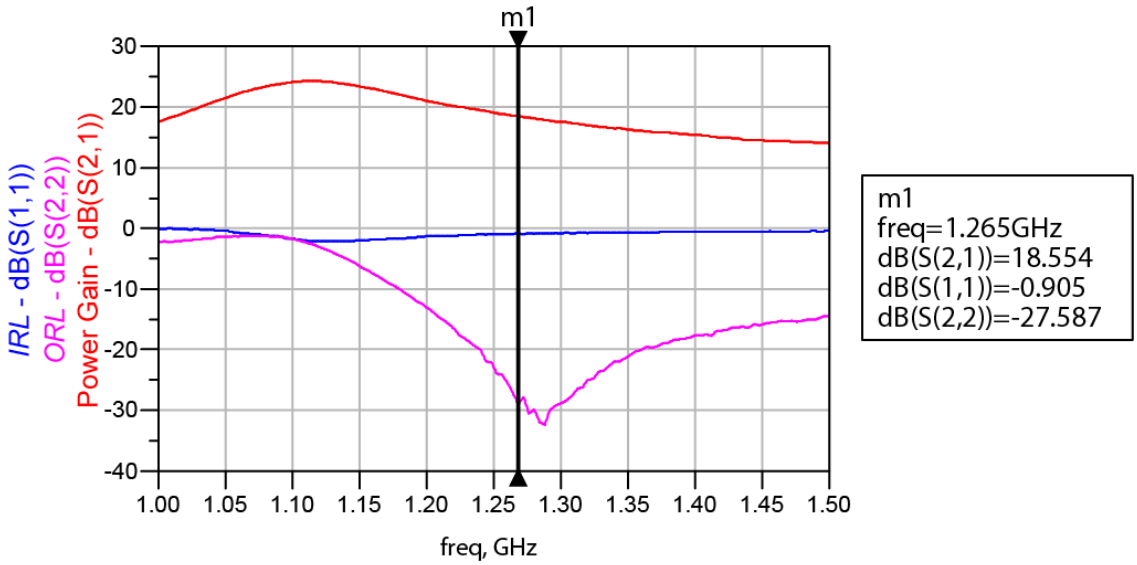


Figure 7.27: Measured Power Gain, *IRL* and *ORL* of the ATF-36077 LNA

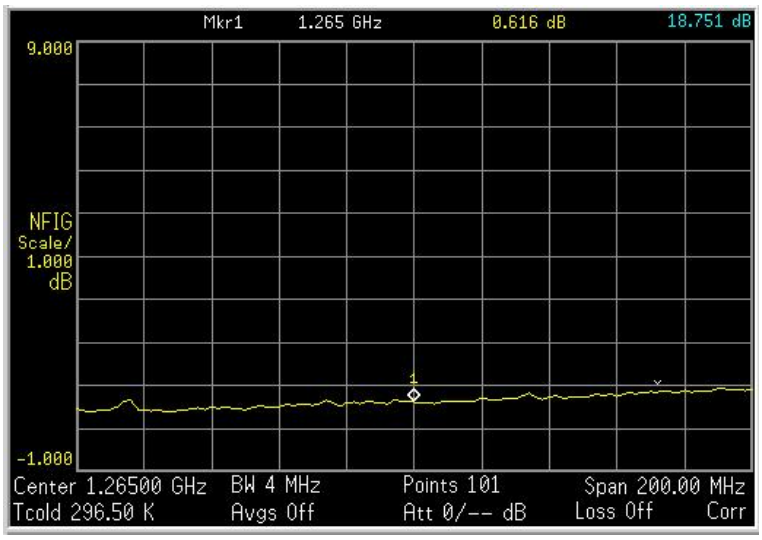


Figure 7.28: Measured *NF* of the ATF-36077 LNA

Figure 7.29: Measured IP_{1dB} Point for the ATF-36077 LNA

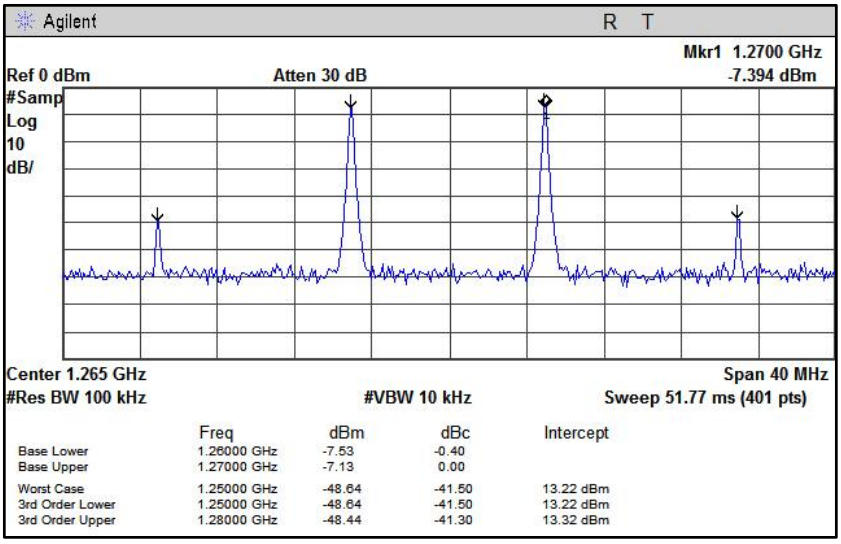


Figure 7.30: Measured OIP_3 Point for the ATF-36077 LNA

Table 7.6: Summary of the Measured Results for the ATF-36077 LNA

	NF	Gain	*IRL*	*ORL*	IP_{1dB}	OP_{1dB}	OIP_3
Measured results	0.616 dB	18.554 dB	−0.905 dB	−27.587 dB	−11.800 dBm	5.855 dBm	13.220 dBm

In order to make a final comparison of the LNAs, all of the simulated and measured performance parameters are illustrated in Figures 7.31 and 7.32 respectively and summarised in Table 7.7. To aid in making a final and conclusive decision on which amplifier to recommend for use in the front end, the dynamic range (*DR*) of each of the amplifiers is also listed. The *DR* was calculated using Equation (3.15). The LNAs are identified in Table 7.7 by their respective active device, with two columns beneath each listed one. The first column lists the simulated results and the second one the actual measured results.

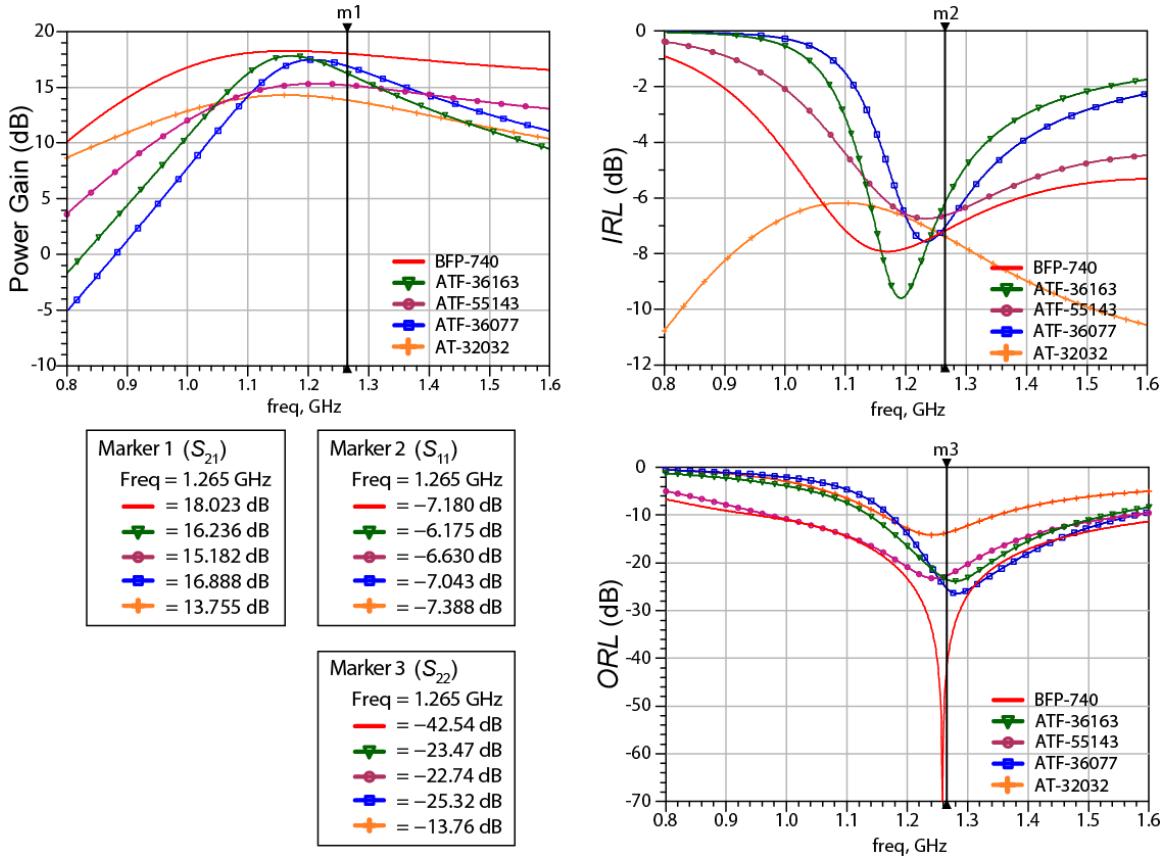


Figure 7.31: Simulated Performance Parameters for all of the LNAs

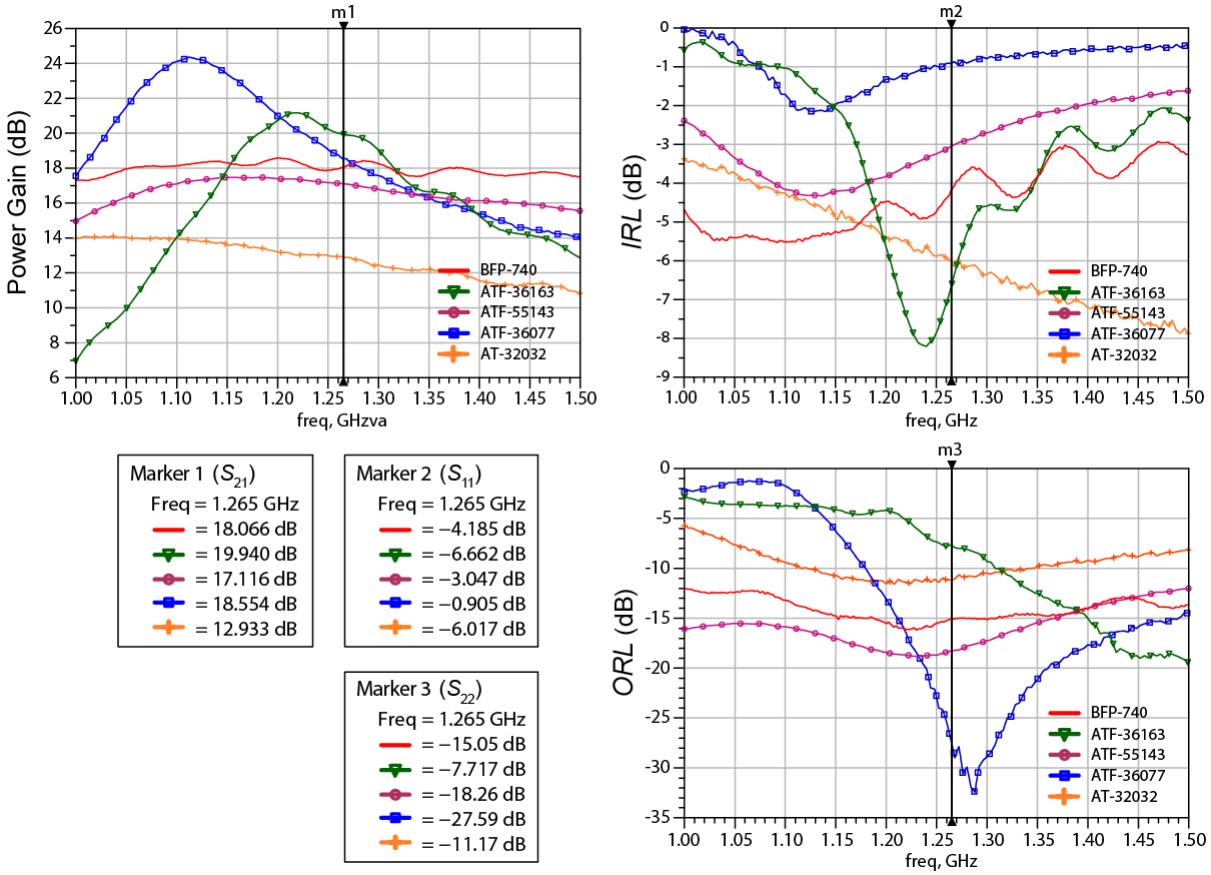


Figure 7.32: Measured Performance Parameters for all of the LNAs

Table 7.7: Simulated and Measured Performance Parameters for all of the LNAs.

	BFP-740		ATF-55143		AT-32032		ATF36163		ATF-36077	
Gain (dB)	18.023	18.066	15.208	17.116	13.934	12.933	16.200	19.940	16.888	18.554
***NF* (dB)**	0.661	0.846	0.704	0.640	1.741	1.163	0.529	0.722	0.468	0.616
***IRL* (dB)**	−7.180	−4.185	−6.841	−3.047	−8.877	−6.017	−6.161	−6.662	−7.043	−0.905
***ORL* (dB)**	−42.536	−15.046	−48.498	−18.261	−19.062	−11.166	−23.774	−7.717	−25.316	−27.590
IP_{1dB} **(dBm)**	−30.74	−27.0	−22.020	−17.600	−9.568	−7.500	−11.230	−12.500	13.498	-11.800
OP_{1dB} **(dBm)**	−13.54	−9.16	−3.750	−1.440	4.214	4.383	5.000	6.373	−3.086	5.855
OIP_3 **(dBm)**	0.63	1.25	11.582	6.610	17.664	15.910	17.796	1.380	16.824	13.220
***DR* (dB)**	72.979	76.277	83.233	85.443	87.644	89.889	92.949	88.571	85.215	81.959
P_{DC} **(mW)**		30		50		25		50		50

The measured power gains of the LNAs ranged from the lowest at just under 13 dB to the highest at almost 20 dB. The measured noise figures range from a minimum of just over 0.6 dB to the highest at almost 1.2 dB. The three FETs produced higher gains and lower noise figures when compared to the AT-32032 BJT. However, the BFP-740 BJT delivered a reasonably good gain of just over 18 dB and an excellent sub-1 dB noise figure of just under 0.85 dB. There are no significant differences in the

measured *IRL* and *ORL* performance parameters with all of the LNAs showing typically sub-optimum *IRL*s with an average value of −4.16 dB. The *ORL*s of the LNAs were relatively good with an average value of −15.956 dB. The linearity parameters of the LNAs were much more varied with OP_{1dB} values varying between just below −9 dBm to a high of just below 6 dBm. The OIP_3 parameters also showed variations between the lowest at 1.25 dBm to the highest at almost 16 dBm. Although the linearity of a LNA is not nearly as important as is the *NF* and gain thereof, it is interesting to see how the selected active devices performed in terms of their linearity parameters. The LNA which used the AT-32032 BJT active device was by far the most linear of the LNAs with a *DR* of almost 90 dB, but the worst when it comes to *NF* and gain. The DC power consumption of all of the LNAs were 50 mW or less and thus they all meet the power constraints of the system which was 100 mW.

7.4 Band-pass Filter Construction and Measurements

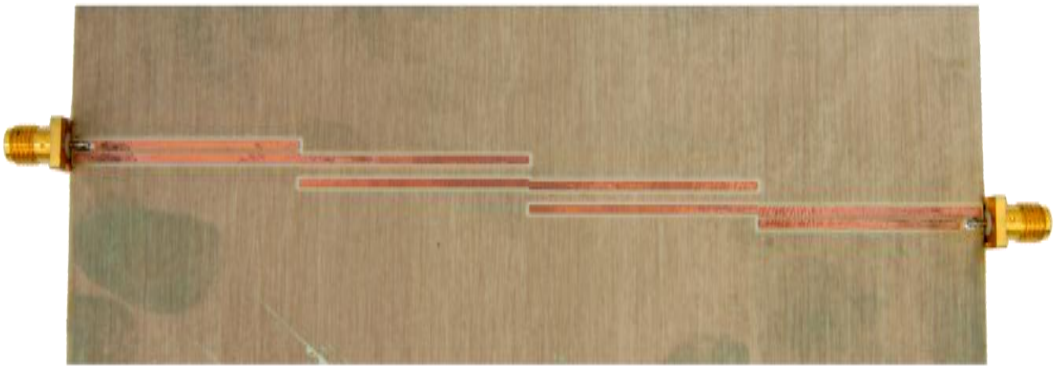


Figure 7.33: The constructed Coupled Line Band-pass Filter

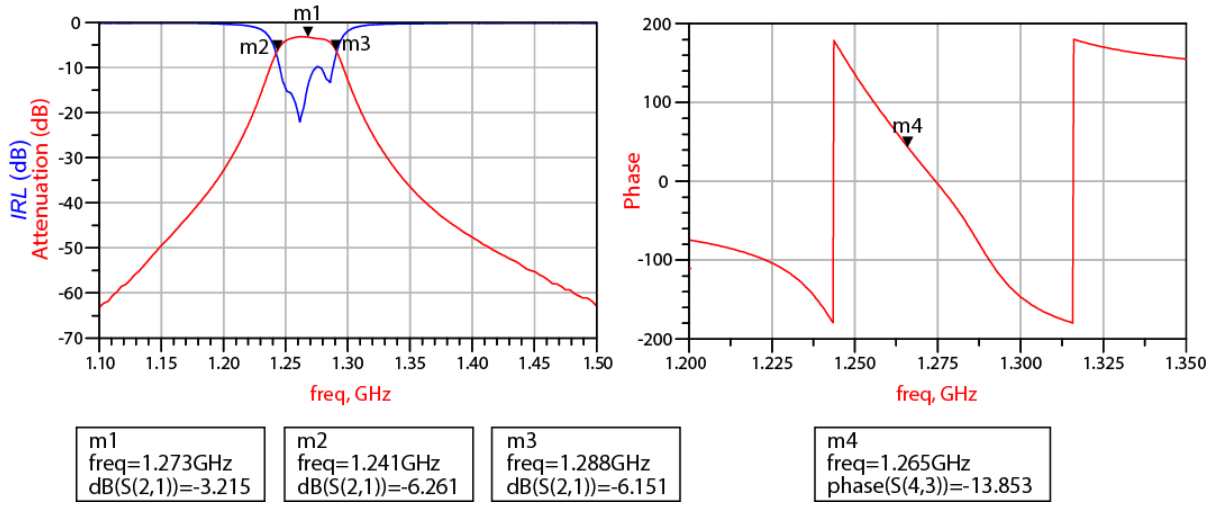


Figure 7.34 Measured Magnitude and Phase Response of the BPF

Table 7.8: Summary of Simulated and Measured Performance Parameters for Band-pass Filter Design

	Simulated	Measured
Center Frequency	1265 MHz	1273 MHz
Lower Stopband Edge	1170 MHz	1170 MHz
Passband	1250 - 1280 MHz	1241 - 1288 MHz
Upper Stopband Edge	1376 MHz	1370 MHz
Insertion Loss	−2.51 dB	−3.215 dB

The simulated and measured results correlated well with minimum insertion loss and a linear phase response in the pass band.

Chapter 8

Conclusions and Recommendations

8.1 Conclusions

The aim of this dissertation was to select the most suitable LNA based on the measured performance parameters thereof. In order to achieve this aim, various active devices were selected based on the specifications detailed in their respective data sheets and their suitability for low noise performance. Each active device was then used in the design of a LNA and the performance of each amplifier was compared to ascertain which configuration provided the lowest *NF* and highest gain with reasonable linearity.

All of the LNAs provided relatively good *NF* and gain performance as depicted in the measured results in Table 7.7. There was no significantly better performing LNA. However, some general comments relating to the design and construction of the LNAs as well as the performance parameters shown in Table 7.7 are presented in the next paragraph.

Designing and working with the GaAs pHEMT active devices was a challenge as they lived up to their notorious reputation of being difficult to stabilise at lower frequencies which was experienced during the design process. The devices were handled with care and precautions for electrostatic discharge (ESD) were always taken during construction and testing. The GaAs pHEMT LNAs showed promising results in the simulations and the usual minor component adjustments had to be made during testing to optimise the performance of the LNA. Careful placement of the capacitors on the source leads was necessary in both the ATF-36077 and the ATF-36136 GaAs pHEMT LNAs, as both circuits initially showed instability tendencies when these capacitors were not optimally placed in proximity to the source leads. The source lead tracks were intentionally made longer so as to facilitate adjustment of the length of the source lead, thereby controlling the amount of source lead inductance necessary to render the active device stable.

The optimisation and adjustment of the input and output matching networks to obtain the best possible gain, *IRL* and *ORL* in these GaAs pHEMT LNAs was very difficult. It was impossible with the available E24 range components to achieve simultaneous maxima and minima for the gain and return loss parameters respectfully, at the design frequency. When comparing the performance parameters of the GaAS pHEMT ATF-36077 and ATF-36163 LNAs in Table 7.7, it is clear that they appear slightly superior to the other LNAs. However, these LNAs are far less robust and much more susceptible to electrostatic damage than some of the other LNAs.

The LNA which used the only BJT as the active device did not meet all the required specifications for this nano-satellite application. The data sheet specified a minimum *NF* of 0.9 dB but this was unobtainable in both the simulations and practically when measuring the constructed LNA. The measured *NF* was 1.163 dB which compares favourably to the specified *NF*s of similar active devices which are available in industry. It is possible that the non-linear model available in the simulation environment is not accurate hence the simulated results not being accurate either.

The measured performance parameters of this AT-32032 BJT LNA indicates that it is not suitable for this nano-satellite application but it does exhibit the best linearity and *DR* of all of the LNAs and therefore may be suitable for use in a maximum available gain small signal amplifier such as an IF amplifier.

The AT-55143 low noise amplifier delivered surprisingly good results and the fact that this e-pHEMT device can be biased in similar fashion to a BJT, made the device surprisingly easy to work with. Also, the simulated performance parameters correlated very well with the actual measured values. When constructing the LNA, no component optimisation adjustments had to be implemented which confirms that the linear and the non-linear models provided in ADS are accurate. This, in addition to the use of the EM Momentum simulations in ADS definitely shortened the development time for this LNA.

The BFP-740 amplifier design process also proved to be a relatively straight forward exercise with no temperamental issues as experienced with the FET active device LNAs. The measured results correlated well with what was simulated and no adjustments to populated components were made on the final product. This active device was definitely less susceptible to external interference caused by cell phones and nearby wifi transmissions during testing and measurements. The excellent gain of just over 18 dB, the sub-1 dB *NF* obtained, the reasonable *IRL* and *ORL* achieved, a *DR* of just over 76 dB and the ease of design make this BFP-740 LNA most suitable for the front end of a nano-satellite application. The distributed version of this BFP-740 LNA also performed reasonably well but unfortunately the implementation of the distributed matching elements at the operating frequency resulted in the final LNA being too bulky to be placed in the very limited space on board a nano-satellite. However, its

inclusion in the design and comparison process provided good comparative criteria for evaluation purposes.

8.2 Recommendations

In this dissertation the latest available active devices were selected based on the system requirements and the information published in the data sheets. The LNA which used the Infinion BFP740 active device is a robust high performing amplifier and is recommended for use in Cubesat receiver systems. It consumed only 30 mW of DC power and provided an excellent *NF* of just over 0.8 dB and a relatively high gain of 18 dB. However, the *DR* of 76 dB could be improved somewhat by using special techniques specifically used to improve the linearity and hence the *DR* of the LNA.

The coupled line filter that was designed met the specifications, but implementing the designed prototype on a PC/104 Cubesat standard PCB would pose a significant challenge in terms of physical size. To reduce this physical size of the filter, some advanced coupling techniques will have to be investigated and implemented. Alternatively, the design of a very small filter with less than 3 dB insertion loss will allow it to be positioned before the LNA and not significantly degrade the *NF* performance of the front end system.

Finally, actual measurements of the constructed circuits should be performed in a proper screened room to eliminate the external interferences which all of the amplifiers in this dissertation were subjected to during measurements. In addition to this, enclosing the LNAs in appropriate RF containers with suitable DC feedthrough capacitors will further enhance the performance of these LNA’s

Appendix A

Matlab Stub Matching Script

```
Fo = 1265;          % Fo.........Centre frequency in (MHz)
Er = 3.38;          % Er.........Dielectric constant
d = 0.813;          % d..........Dielectric thickness (mm)
c = 3e8;            % c..........Speed of light (m/s)
lambdaf = c/(Fo*1e6);
ko=2*pi/lambdaf;

Zo = 50;
Rl = 15.181;        % 80.6;
Xl = -3.394;        % -26.554;
Zl = Rl +i*Xl;      % Equation 3.40
Yo = 1/Zo;          % Equation 3.41

%calculating physical lengths of stub
Aa=Zo/60;
Ab=sqrt((Er+1)/2);
Ac=(Er-1)/(Er+1);
Ad=(0.23+(0.11/Er));
A=Aa*Ab+Ac*Ad;
Wdr1=(8*exp(A))/(exp(2*A)-2);      % Eq 3.49 for W/d ratio < 2


B=(377*pi)/(2*Zo*sqrt(Er));        % Equation 3.52

%%% Equation 3.50 %%%
Wdr2a=(2/pi);
Wdr2b=(B-1-log(2*B-1));
Wdr2c=(Er-1)/(2*Er);
Wdr2d=(log(B-1)+0.39-(0.61/Er));
Wdr2=Wdr2a*(Wdr2b+Wdr2c*Wdr2d);    % W/d ratio > 2

if Wdr1<2
    Wdr=Wdr1;
else
    Wdr=Wdr2;
end

% Calculate line width (mm)
W=Wdr*d;
Wmill = W * 39.3700787;

% Calculate effictive dielectric constant for microstrip
% line of width W on dielectric material of constant Er
Ereff=((Er+1)/2)+((Er-1)/2)*(1+12*(d/(W/1e3))).^-0.5;  % Equation 3.48
Lambdam=lambdaf/sqrt(Ereff)*1000;

% calculating of stub position and electrical lengths
% Equation 3.45
t1 = (Zo - Rl)^2 + Xl^2;
t(1) = (Xl + sqrt((Rl*t1)/Zo)) / (Rl-Zo);
t(2) = (Xl - sqrt((Rl*t1)/Zo)) / (Rl-Zo);
```

```
for N = 1:length(t)

    dl(N) = (2*pi).^-1*atan(t(N));
    if dl(N) < 0
        dl(N) = (2*pi).^-1*(pi + atan(t(N)));
    end

    % Equation 3.44
    B1 = Rl^2*t(N) - (Zo-Xl*t(N))*(Xl+Zo*t(N));
    B2 = Rl^2 + (Xl+Zo*t(N)).^2;
    B(N) = B1 / (Zo.*B2);

    % Equation 3.42
    Z(N) = Zo.* ((Zl+i*(Zo*t(N)))/(Zo+i*(Zl*t(N))));
    Y(N) = 1/Z(N);

    % Equation 3.46
    ls(N) = (2*pi).^-1 * atan(Yo/B(N));
    lo(N) = -(2*pi).^-1 * atan(B(N)/Yo);
    if ls(N) < 0
        ls(N) = ls(N) + 0.5;
    end
    if lo(N) < 0
        lo(N) = lo(N) + 0.5;
    end

    ddeg(N) = dl(N)*360;
    dmm(N) = ddeg(N) / 360 * Lambdam;
    dmill(N) = dmm(N) * 39.3700787;

    lsdeg(N) = ls(N)*360;
    lsmm(N) = lsdeg(N) / 360 * Lambdam;
    lsmill(N) = lsmm(N) * 39.3700787;

    lodeg(N) = lo(N)*360;
    lomm(N) = lodeg(N) / 360 * Lambdam;
    lomill(N) = lomm(N) * 39.3700787;

end

fprintf('open circuit shunt stub:\n');
fprintf('Distance from load d:\t%4.2f wavelengths, %4.2f degrees, %4.2f mm,
        %4.2f mills\n',dl(1), ddeg(1), dmm(1), dmill(1));
fprintf('lenght of stub l:\t\t%4.2f wavelengths, %4.2f degrees, %4.2f mm,
        %4.2f mills\n\n',lo(1), lodeg(1), lomm(1), lomill(1));
fprintf('Distance from load d:\t%4.2f wavelengths, %4.2f degrees, %4.2f mm,
        %4.2f mills\n',dl(2), ddeg(2), dmm(2), dmill(2));
fprintf('lenght of stub l:\t\t%4.2f wavelengths, %4.2f degrees, %4.2f mm,
        %4.2f mills\n\n',lo(2), lodeg(2), lomm(2), lomill(2));
fprintf('width of section l:\t\t%4.2f mm, %4.2f mills\n\n',W, Wmill);

fprintf('short circuit shunt stub:\n');
fprintf('Distance from load d:\t%4.2f wavelengths, %4.2f degrees\n',dl(1),
        ddeg(1));
fprintf('lenght of stub l:\t\t%4.2f wavelengths, %4.2f degrees\n\n',ls(1),
        lsdeg(1));
fprintf('Distance from load d:\t%4.2f wavelengths, %4.2f degrees\n',dl(2),
        ddeg(2));
fprintf('lenght of stub l:\t\t%4.2f wavelengths, %4.2f degrees\n',ls(2),
        lsdeg(1));
```

Appendix B

Calculating Even and Odd Mode Impedances for Coupled Line Filter

```
N = 3; % filter order (3,5,7)
ftype = 1; % chebychev with 0.5 dB ripple (1), chebychev with 3 dB ripple
(2), maximallyflat (3), linear phase (4)
fc =1.265e9; % centre frequency of operation
delta = 0.0237; % fractional bandwith
Z0 = 50; % system characteristic impedance
%Filter element values as found in Pozar
if ftype == 1 && N == 3
G = [1.5963, 1.0967, 1.5963, 1];
end
if ftype == 1 && N == 5
G = [1.7058, 1.2296, 2.5408, 1.2296, 1.7058, 1];
end
if ftype == 1 && N == 7
G = [1.7372, 1.2583, 2.6381, 1.3444, 2.6381, 1.2583, 1.7372, 1];
end
if ftype == 2 && N == 3
G = [3.3487, 0.7117, 3.3487, 1];
end
if ftype == 2 && N == 5
G = [3.4817, 0.7618, 4.5381, 0.7618, 3.4817, 1];
end
if ftype == 2 && N == 7
G = [3.5182, 0.7723, 4.6386, 0.8039, 4.6386, 0.7723, 3.5182, 1];
end
if ftype == 3 && N == 3
G = [1.0, 2.0, 1.0, 1];
end
if ftype == 3 && N == 5
G = [0.618, 1.618, 2, 1.618, 0.618, 1];
end
if ftype == 3 && N == 7
G = [0.445, 1.247, 1.8019, 2, 1.8019, 1.247, 0.445, 1];
end
if ftype == 4 && N == 3
G = [1.255, 0.5528, 0.1922, 1];
end
if ftype == 4 && N == 5
G = [0.9303, 0.4577, 0.3312, 0.2090, 0.0718, 1];
end
if ftype == 4 && N == 7
G = [0.7677, 0.3744, 0.2944, 0.2378, 0.1778, 0.1104, 0.0375, 1];
end
if N == 3
ZoJ1 = sqrt((pi*delta)/(2*G(1)));      % Equation (4.17)
ZoJ2 = (pi*delta)/(2*sqrt(G(1)*G(2))); % Equation (4.18)
ZoJ3 = (pi*delta)/(2*sqrt(G(2)*G(3)));
ZoJ4 = sqrt((pi*delta)/(2*G(3)*G(4))); % Equation (4.19)
Z0e1 = Z0*(1 + ZoJ1 + ZoJ1^2)          % Equation (4.20)
Z0e2 = Z0*(1 + ZoJ2 + ZoJ2^2)
Z0e3 = Z0*(1 + ZoJ3 + ZoJ3^2)
Z0e4 = Z0*(1 + ZoJ4 + ZoJ4^2)
Z0o1 = Z0*(1 - ZoJ1 + ZoJ1^2)          % Equation (4.21)
Z0o2 = Z0*(1 - ZoJ2 + ZoJ2^2)
Z0o3 = Z0*(1 - ZoJ3 + ZoJ3^2)
Z0o4 = Z0*(1 - ZoJ4 + ZoJ4^2)
```

```
end
if N == 5
ZoJ1 = sqrt((pi*delta)/(2*G(1)));       % Equation (4.17)
ZoJ2 = (pi*delta)/(2*sqrt(G(1)*G(2))); % Equation (4.18)
ZoJ3 = (pi*delta)/(2*sqrt(G(2)*G(3)));
ZoJ4 = (pi*delta)/(2*sqrt(G(3)*G(4)));
ZoJ5 = (pi*delta)/(2*sqrt(G(4)*G(5)));
ZoJ6 = sqrt((pi*delta)/(2*G(4)*G(6))); % Equation (4.19)
Z0e1 = Z0*(1 + ZoJ1 + ZoJ1^2)           % Equation (4.20)
Z0e2 = Z0*(1 + ZoJ2 + ZoJ2^2)
Z0e3 = Z0*(1 + ZoJ3 + ZoJ3^2)
Z0e4 = Z0*(1 + ZoJ4 + ZoJ4^2)
Z0e5 = Z0*(1 + ZoJ5 + ZoJ5^2)
Z0e6 = Z0*(1 + ZoJ6 + ZoJ6^2)
Z0o1 = Z0*(1 - ZoJ1 + ZoJ1^2)           % Equation (4.21)
Z0o2 = Z0*(1 - ZoJ2 + ZoJ2^2)
Z0o3 = Z0*(1 - ZoJ3 + ZoJ3^2)
Z0o4 = Z0*(1 - ZoJ4 + ZoJ4^2)
Z0o5 = Z0*(1 - ZoJ5 + ZoJ5^2)
Z0o6 = Z0*(1 - ZoJ6 + ZoJ6^2)
end
if N == 7
ZoJ1 = sqrt((pi*delta)/(2*G(1)));       % Equation (4.17)
ZoJ2 = (pi*delta)/(2*sqrt(G(1)*G(2))); % Equation (4.18)
ZoJ3 = (pi*delta)/(2*sqrt(G(2)*G(3)));
ZoJ4 = (pi*delta)/(2*sqrt(G(3)*G(4)));
ZoJ5 = (pi*delta)/(2*sqrt(G(4)*G(5)));
ZoJ6 = (pi*delta)/(2*sqrt(G(5)*G(6)));
ZoJ7 = (pi*delta)/(2*sqrt(G(6)*G(7)));
ZoJ8 = sqrt((pi*delta)/(2*G(7)*G(8))); %Equation (4.19)
Z0e1 = Z0*(1 + ZoJ1 + ZoJ1^2)           %Equation (4.20)
Z0e2 = Z0*(1 + ZoJ2 + ZoJ2^2)
Z0e3 = Z0*(1 + ZoJ3 + ZoJ3^2)
Z0e4 = Z0*(1 + ZoJ4 + ZoJ4^2)
Z0e5 = Z0*(1 + ZoJ5 + ZoJ5^2)
Z0e6 = Z0*(1 + ZoJ6 + ZoJ6^2)
Z0e7 = Z0*(1 + ZoJ7 + ZoJ7^2)
Z0e8 = Z0*(1 + ZoJ8 + ZoJ8^2)
Z0o1 = Z0*(1 - ZoJ1 + ZoJ1^2)           %Equation (4.21)
Z0o2 = Z0*(1 - ZoJ2 + ZoJ2^2)
Z0o3 = Z0*(1 - ZoJ3 + ZoJ3^2)
Z0o4 = Z0*(1 - ZoJ4 + ZoJ4^2)
Z0o5 = Z0*(1 - ZoJ5 + ZoJ5^2)
Z0o6 = Z0*(1 - ZoJ6 + ZoJ6^2)
Z0o7 = Z0*(1 - ZoJ7 + ZoJ7^2)
Z0o8 = Z0*(1 - ZoJ8 + ZoJ8^2)
end
```

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