

A MICRO COMPUTER BASED
TEST SET FOR
TELECONTROL EQUIPMENT

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A MICRO COMPUTER BASED TEST SET

FOR

TELECONTROL EQUIPMENT

Project:

SELTA TEST SET

FOR THE

SUPERVISORY SECTION

(ESCOM, WESTERN CAPE REGION)

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(ii) Mr. P. Nell (ESCOM)

SYNOPSIS

A micro computer based SELTA test set, that simulates the Selta master was developed and tested to display the following:

Breaker status (open/close), alarms and analogue quantities as Volts, Amps, Freq etc.

The unit is also capable of sending remote controls to the SELTA remote thus changing the breaker status.

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OBJECTIVES

To develop a Selta remote test set, that simulates a Selta master and displays data in a user friendly mode.

The unit must be capable of doing the following:

- (a) Display Breaker Return Indications (B.R.I.) as open/closed or anomaly.
- (b) Analogues (Volts, Amp, etc.) to be displayed as decimal values with sign and engineering units.
- (c) Alarms (Transformer temperature etc.) to be displayed as a list with FAULT/TRUE condition next to the name.
- (d) Transmit a synch word and PVX empty words to the remote.
- (e) Execute remote controls in a user friendly mode.

Controls to be entered has a decimal number (breaker number) and OPEN/CLOSE condition.

The above objectives must be met within the following parameters:

- (a) The total cost of the unit should not exceed R1500-00 (compared to R30000-00 for a master).
- (b) The system should be reliable and easy to maintain.
- (c) The system should provide information in a clear and logical manner.
- (d) The system should be as user friendly as possible.

1.0 ELECTRICITY SUPPLY COMMISSION

- 1.1 The supply system
- 1.2 Power stations (Present/Future)
- 1.3 The National Grid
- 1.4 Geographical details
- 1.5 Monitoring/control at a typical distribution station

The information is not comprehensive, but should provide the reader with background information regarding the above 5 points.

1.1 The Supply System

This is a technical achievement which ranks with the best in the world and most of these developments took place during the past 20 years. The South African consumer generally takes it for granted that an electricity supply will be available, but is often not aware of the sophisticated technical and other expertise that is required, nor the very high generating and distribution costs involved.

A major achievement in 1984 was the commissioning of the first generating set at Koeberg, Africa's first nuclear power station. In its first six months it generated 4 000 million kWh.

ESCOM operates one of the most advanced electricity supply systems in the world and ranks among the ten largest electrical utilities. With 26 power stations, an installed capacity of 24 514 MW and a National grid system of about 150 000 km of high-voltage lines, ESCOM endeavours to supply electricity wherever it is economically feasible in southern Africa.

1.2 Power Stations

1.2.1 As mentioned previously the present system consists of the following:

- (a) 20 coal fired stations
- (b) 1 nuclear power station
- (c) 2 gas turbine power stations
- (d) 2 Hydro electric power stations
- (e) 1 Pump/storage scheme

1.2.2 Power Stations Under Construction

At present there are 5 new coal fired power stations plus one pump/storage power station under construction.

1.3 The National Grid

Since electrical energy cannot be stored, it must be generated, transmitted and distributed to the customer as required.

The National grid is the medium by which the transmission and distribution occurs.

The transmission network conveys the bulk electrical energy from the generating power stations, to major distribution stations that serve their respective areas.

The following map of the Republic of South Africa shows the area served by the National transmission grid.

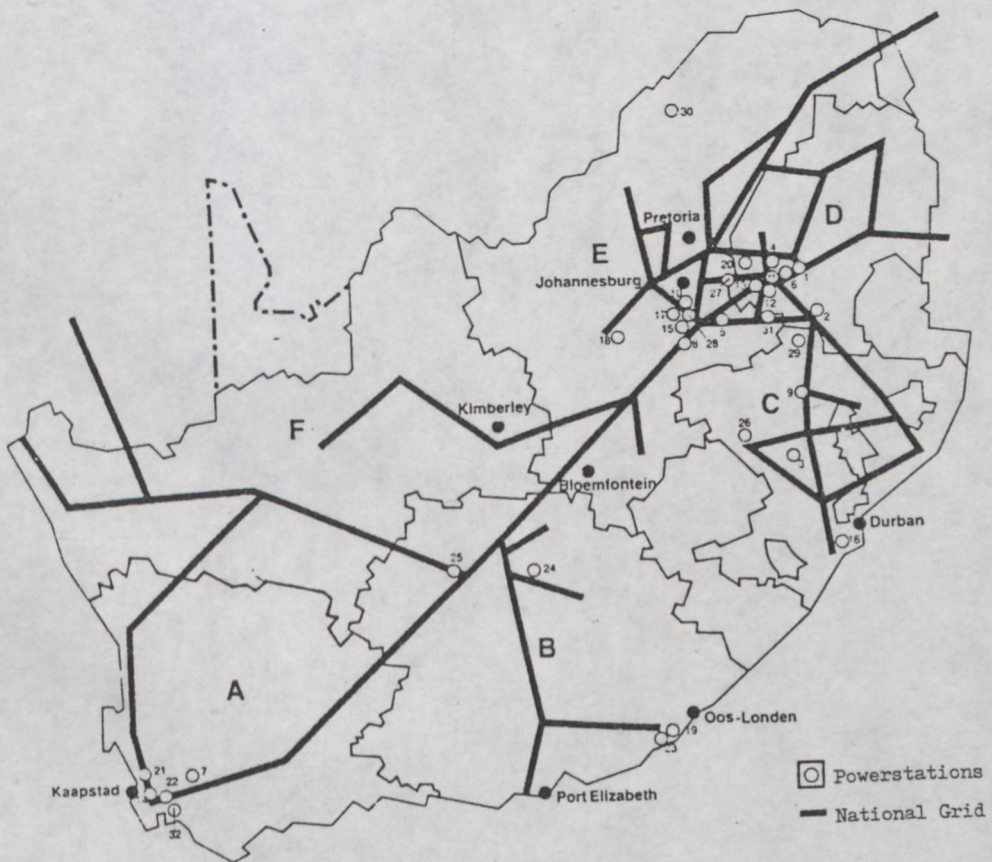


Fig. 1

The National grid is monitored and controlled from the National control centre at Simmerpan, Germiston by means of a sophisticated supervisory, control and load dispatch system (S.C.A.L.D.).

1.4 Geographical Details

The Electricity Supply Commission provides power to its customers through a total of 12 regions which cover the entire Republic of South Africa. The map shown in fig. 2 demarcates these regions.

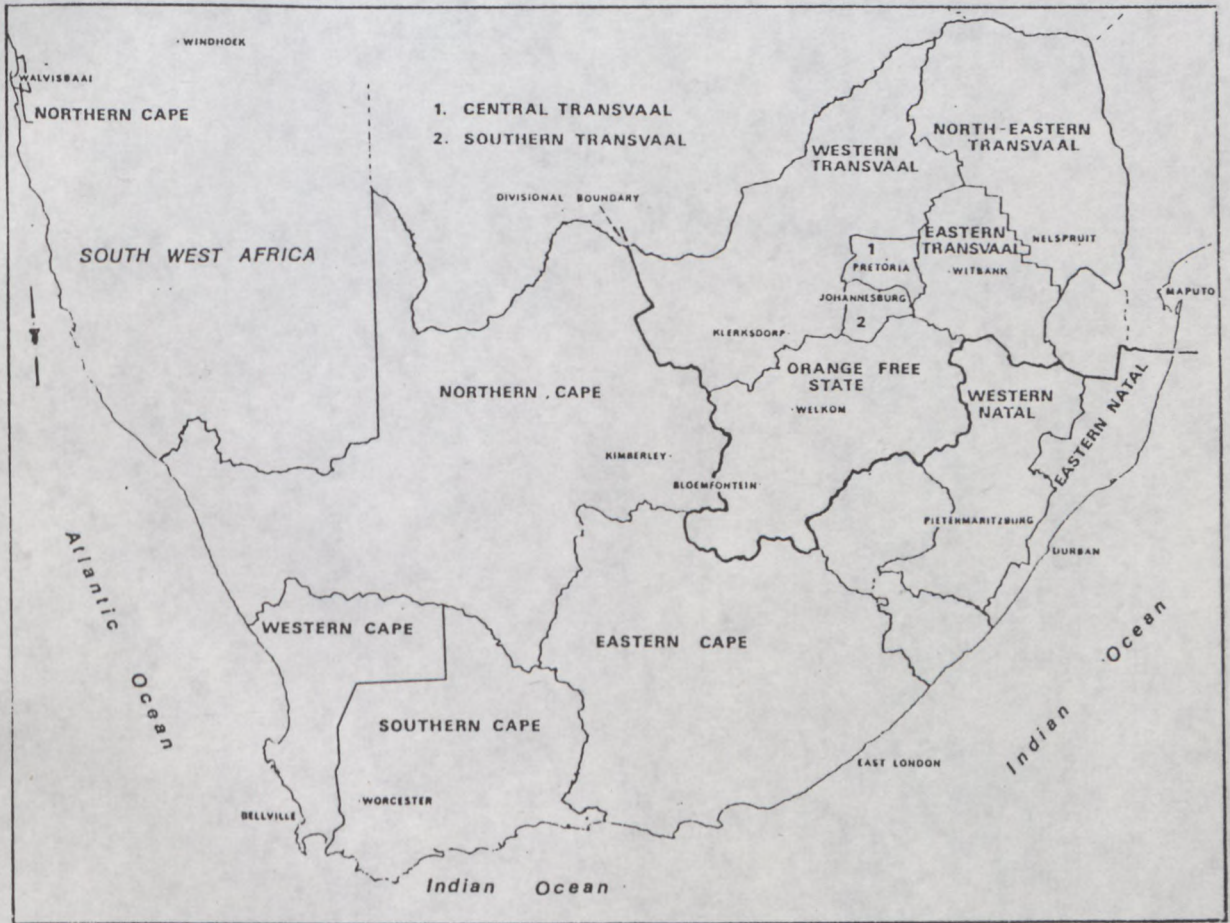


Fig. 2

The regions then distributes the electricity supplied via the National grid under the control of it's own Regional Control Centre.

The distribution stations in these regions, may be controlled from either the National or Regional Control Centres, (this will be discussed in more detail at a later stage).

Each region in turn is devided into distribution areas and districts.

- 1.5 Monitoring/control at a typical distribution station as shown in fig. 3.

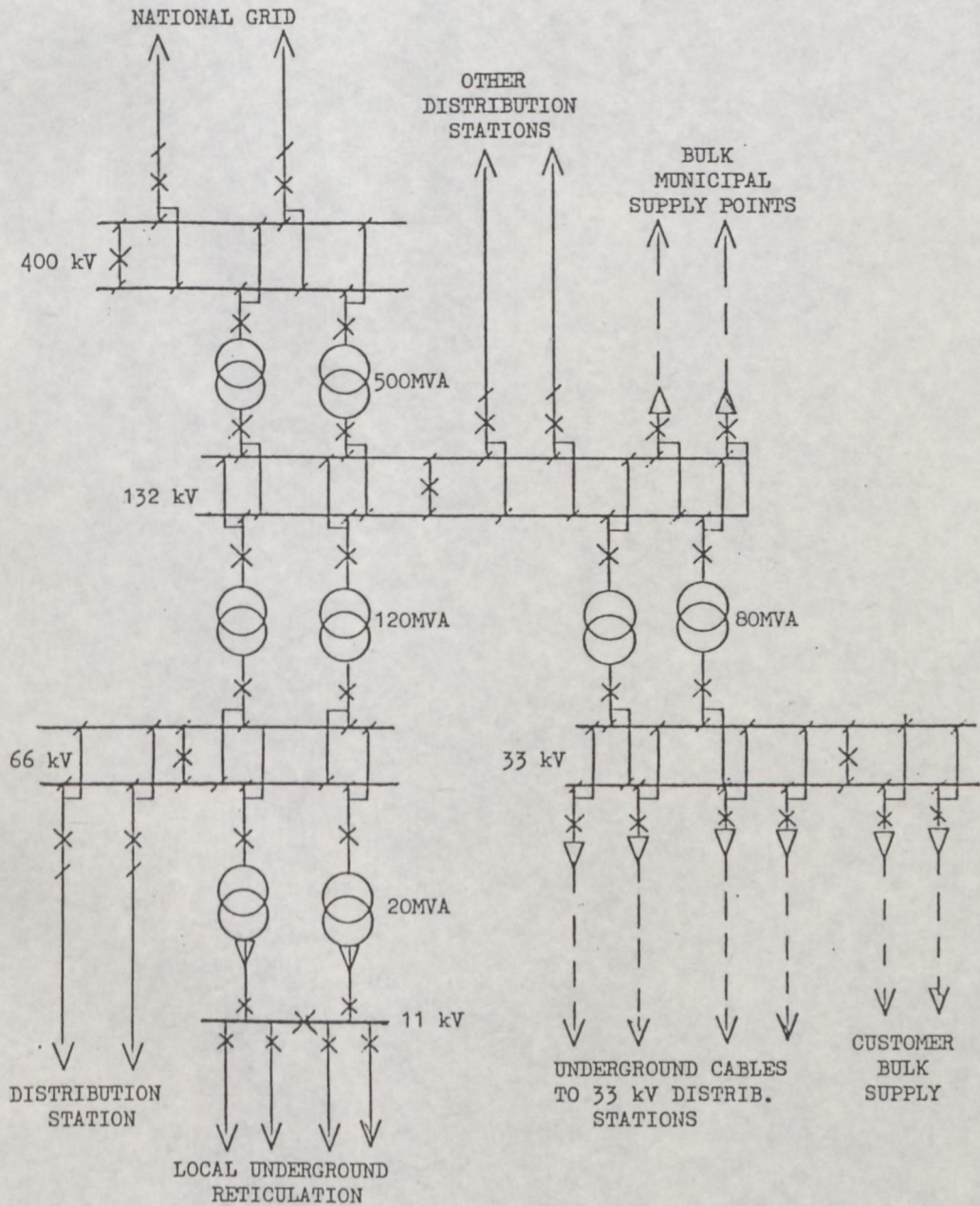


Fig. 3

TYPICAL LAYOUT OF A MAJOR DISTRIBUTION STATION

To ensure optimum availability and reliability of supply from a distribution station, it is essential that these stations are remotely monitored and controlled.

1.5.1 Monitoring

The following is monitored at a typical distribution station.

- (a) Breaker return indication (B.R.I.)
- (b) Alarms eg. Communication alarm, transformer alarms, supply failure alarms, earth fault alarms.
- (c) Analogue quantities eg. MW, MVars, KV, Amps, Freq.

1.5.2 Control

- (a) Breaker OPEN/CLOSE control.
- (b) Isolating links OPEN/CLOSE control.

1.5.3 Parallel monitoring and control by either National/Regional Control Centres is achieved by means of the following:

(a) National Control

Uses a S.C.A.L.D. (Supervisory Control and Load dispatch) system comprising of a Xerox 550 computer situated at the Control Centre and C2020 Leeds and Northrup remotes.

The remotes are situated at the substations and are multi dropped. They operate at 200 bd and 1200 bd rates.

The bearer channel may be a combination of Microwave, Radio link and Power Line Carrier.

(b) Regional Control

Uses 35 links configured point-to-point.

Each point-to-point link consists of a remote situated at the substation and the master at the Control Centre. The equipment used is Telettra Tic 2P/C or Selta.

Baud rates are 50 bd, 100 bd, FSK 4 wire system.

Once again the bearer channel may be a combination of Microwave, Radio and Power Line Carrier.

At the Control Centre the alarms and analogues from the 35 masters are gathered and displayed by a remote alarm and data acquisition system (R.A.D.A). Consisting of 3 M.M.I. (Man machine interface) comprising of keyboard and VDU (Visual display unit).

(c) Substation parallel control

The remotes communicating with either national or regional control, operate in parallel via an interposing relay panel (I.R.P.), connected to the station equipment via an interposing distribution frame (I.D.F.).

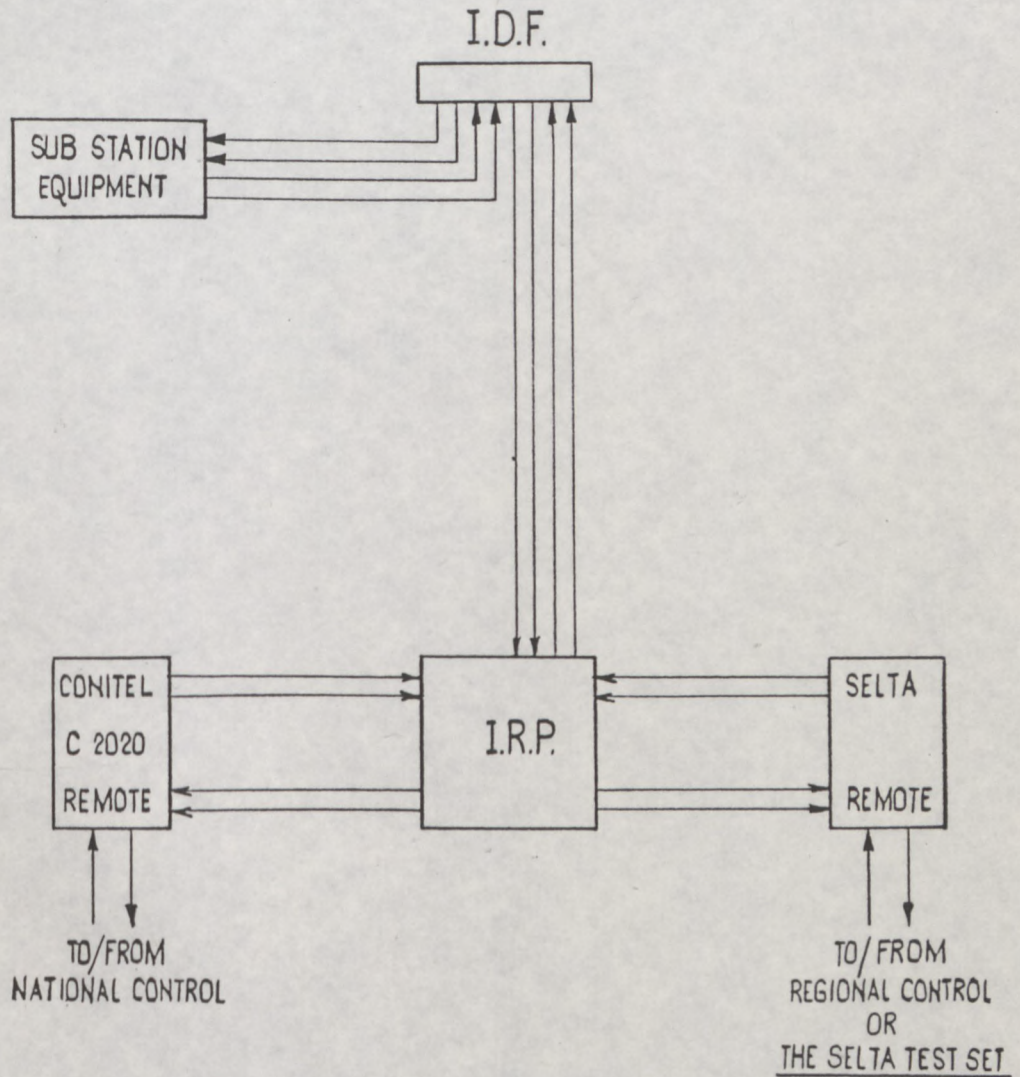


Fig. 5

A simplified block diagram is shown in Fig. 5. Note to simplify the block diagram the two remotes are connected directly to the I.R.P. In practice this is not the case. The equipment would be connected to the I.R.P. via the I.D.F. as shown in the next 3 diagrams.

Fig. 6 shows how controls are generated by either National Control via the Conitel remote, or Regional Control via the Selta remote, through the I.R.P.

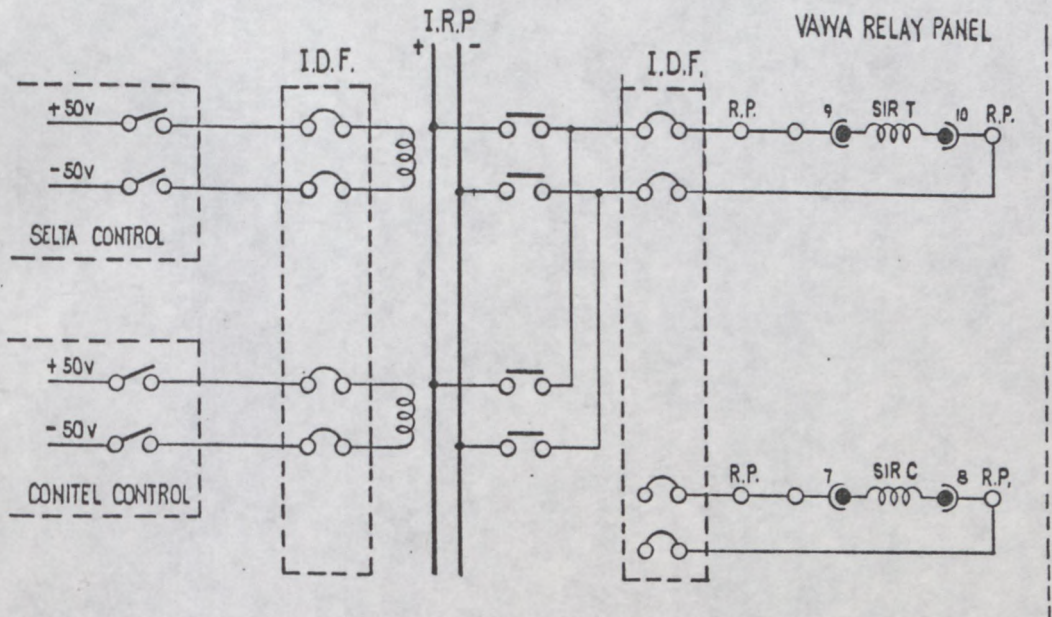


Fig. 6

Fig. 7 shows how a single input from say a B.R.I. is connected to the I.R.P., to provide 2 potential free contacts to be connected to the Conitel and Selta remotes.

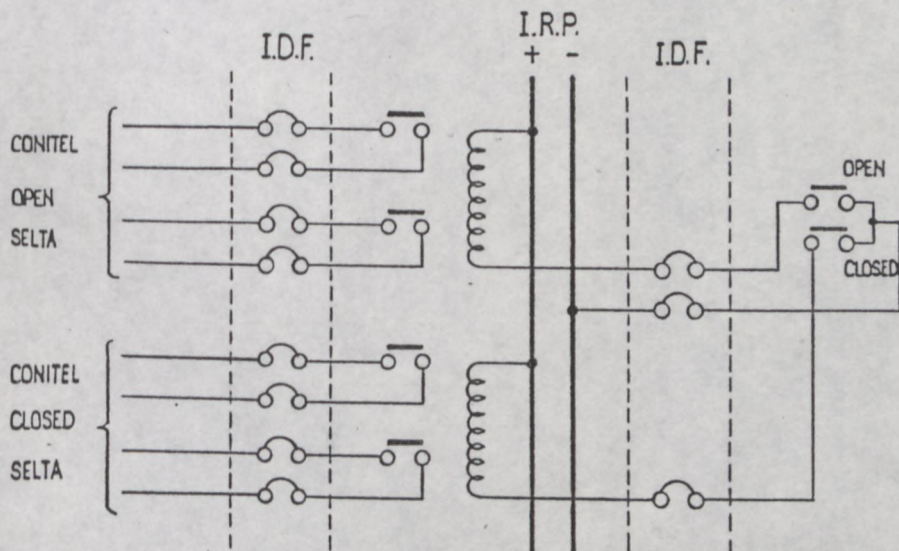


Fig. 7

Fig. 8 shows how a single alarm contact from the plant connected to the I.R.P., provides two potential free contacts to be connected to the Conitel and the Selta remotes.

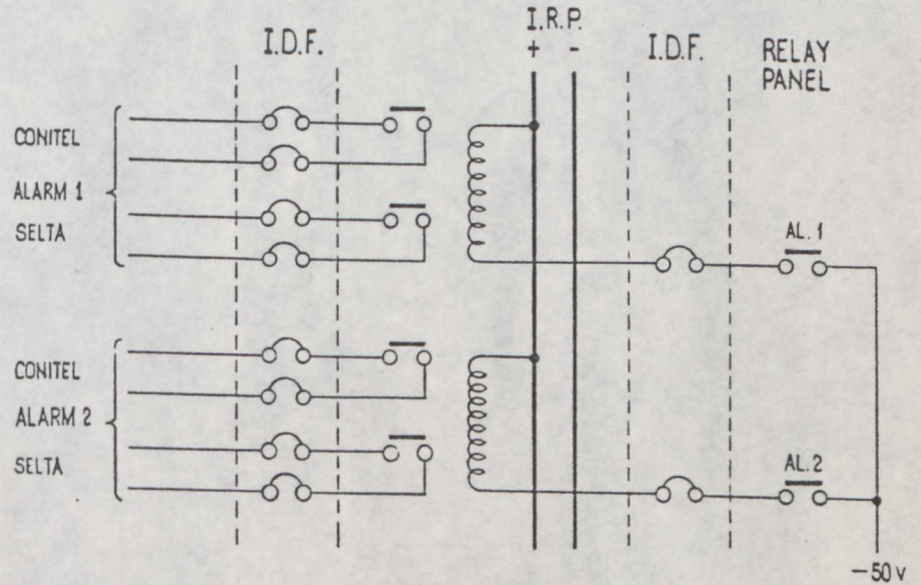


Fig. 8

2.0 PROCEDURE USED TO ACHIEVE SET OBJECTIVES

- 2.1 The main objectives of the project were defined in conjunction with the user.
- 2.2 A market survey was carried out by the author on the different types of test sets available on the market the findings are as follows:

(a) Selta.

Selta Italy was contacted and the author was assured that a test set was not available. The Selta STO-E master/remote and the TELETTRA TIC 2C/P master/remote use a dumb visualizer card. This consists of LED's or lamps that indicate if the bits of a received word are set or reset.

The trigger pulse is obtained via a jumper lead connected to the desired channel time to be viewed.

(b) Motorola Test Set.

This is a more intelligent test set. Data is displayed by means of led's either on or off. The unit can send remote controls and display specific words of a group.

Analogues quantities are displayed as a binary count by means of led's.

(c) Leeds and Northrup Test Set.

This unit is the most sophisticated one presently available on the market.

Data may be displayed by means of led's on or off for alarms and B.R.I., while analogue quantities are displayed by means of a 7 segment display. The binary count displayed must still be converted into an actual analogue quantity using a calculator.

Remote controls are selected by means of push button switches.

(d) Telkor (Pty) Limited.

The above company is presently writing software for the M24 Olivetti PC. The unit will be used as a test set, to test their P.U.T.U. (Programmable Universal Telecontrol Unit) remotes.

The test set should be available on the market by July 1986 (NB: The above test set can only communicate with P.U.T.U. remotes).

The test sets specified in (b), (c) and (d) cannot be used on the Selta remote.

- 2.3 A micro-processor approach was followed in developing the test set. A Spectrum micro computer was used in conjunction with a micro drive. The interface was designed using off-the-shelf components.
- 2.4 Configuration of the system was established. The developed (software) program is stored on cassette. The substations data base are stored on separate cassettes in a pre-defined format.
- 2.5 Suitable hardware was designed to sample incoming data, generate a synchronizing pulse (NMI) and enable the micro to send data to the remote in the form of synchronizing data and remote controls.
- 2.6 The developed software does the following:
 - (a) Receive data and do the required manipulations/calculations.
 - (b) Display data in a user friendly mode.
 - (c) Transmit data to the remote, synchronizing it and shortening it's transmitted message length.
 - (d) Send remote controls to the remote and again resetting it's word counter at the correct message length.
- 2.7 The prototype unit performs the following functions:
 - (a) Receives up to eight analogue quantities, updating the display every 5.4 seconds. The quantities are displayed as a decimal value with sign.
 - (b) Receives up to 20 alarm inputs displayed as 2 pages of 10 alarms each. The alarm status is displayed as true or fault next to alarm names.
 - (c) Receives up to 30 double breaker return indications and displays their status as two pages of 15 B.R.I each. The status will be either open, closed, or anomaly (fault condition), displayed next to breaker names.
 - (d) Sends up to 30 double remote controls. Controls are entered as a decimal number, with status. The program will convert the entered quantity into a suitable code.
 - (e) Data will be sent and received by the test set via two FSK (Rx, Tx) modems.

3.0 THE SELTA SUPERVISORY CONTROL SYSTEM STO-E

The Selta STO-E is a small/medium capacity supervisory control system which allows bidirectional transfer of digital or analogue information used in the remote supervision of various types of installations.

The Selta point to point STO-E system comprises a master station and a remote, communicating in a Full-duplex mode (4 wire system).

Communication between master and remote occurs in a cyclic mode, which means that the remote will continuously send data to the master. The master will respond by sending PVX empty words and a synch word that will reset the remote's word counter.

The remote may transmit a maximum of 32 words but in a standard remote 18 words are sent as follows:

TRANS	1 WORD
SYNCH	1 WORD
B.R.I.	6 WORDS (30 DOUBLE BREAKER RETURN INDICATIONS)
ALARMS	2 WORDS (20 SINGLE BIT ALARMS)
ANALOGUES	8 WORDS (8 ANALOGUE QUANTITIES)

The Selta test set designed by the author is used for testing Selta remotes. The message structure is shown on the following page. See Full Duplex Operation Timing Diagram.

As may be seen in the timing diagram the remote sends data in a cyclic mode. The test set waits to receive the synch word sent by the remote and then proceeds to store the words that follow in their appropriate memories ready to be manipulated.

The test set having detected the remote's synch word will also send to the remote, 15 PVX empty words and a synch word that will reset the remotes word counter at the correct message length. In a normal cycle the message length consists of 18 words, 15 bits each (10 data bits - 5 check bits). For a control cycle the test set will send a total of 8 words, 15 bits each. They are as follows:

SYNCH, PVX, TELEC, GTC, TC, $\overline{\text{GTC}}$, $\overline{\text{TC}}$, SYNCH.

The synch sent at the end of the control message resets the remote word counter and "normal" cyclic transmission resumes. (Note: A software loop is used to generate a 4 m/sec delay when transmitting data from the test set. The delay is counted from the centre of each bit received from the remote and is inserted so that the transmitted bits from the test set coincide with the remote's input data sampling pulses). The received words are stored as follows:

Input serial data temporary store (NB: Addresses shown in HEX = H).

EFDOH - EFDBH	= 6 x B.R.I. words
EFDCH - EFD FH	= 2 x ALARMS WORDS
EFE OH - EFE FH	= 8 x ANALOGUE WORDS

At the end of each received message the contents of EFDOH - EFEFH are transferred to the display working memory locations EFOOH - EF1FH, to prevent the displayed data from changing on the screen during update. The waveforms were checked using a HP1615 logic analyzer and a PM 3551A logic analyzer.

4.0 ANALOGUE QUANTITIES

As previously mentioned the Selta STO-E remote is installed at a substation and is connected to the station equipment via the IDF.

To the remote we may connect up to 8 analogue quantities such as kW, kVars, Amps, kV, Freq.

In the figure below it can be seen how the above quantities are picked off the feeders using CT's, VT's and connected to the remote via transducers, the output of the transducers vary in direct proportion to the quantity under measurement.

Generally the variation of these quantities is slow, so that sampling does not have to be done at high frequencies.

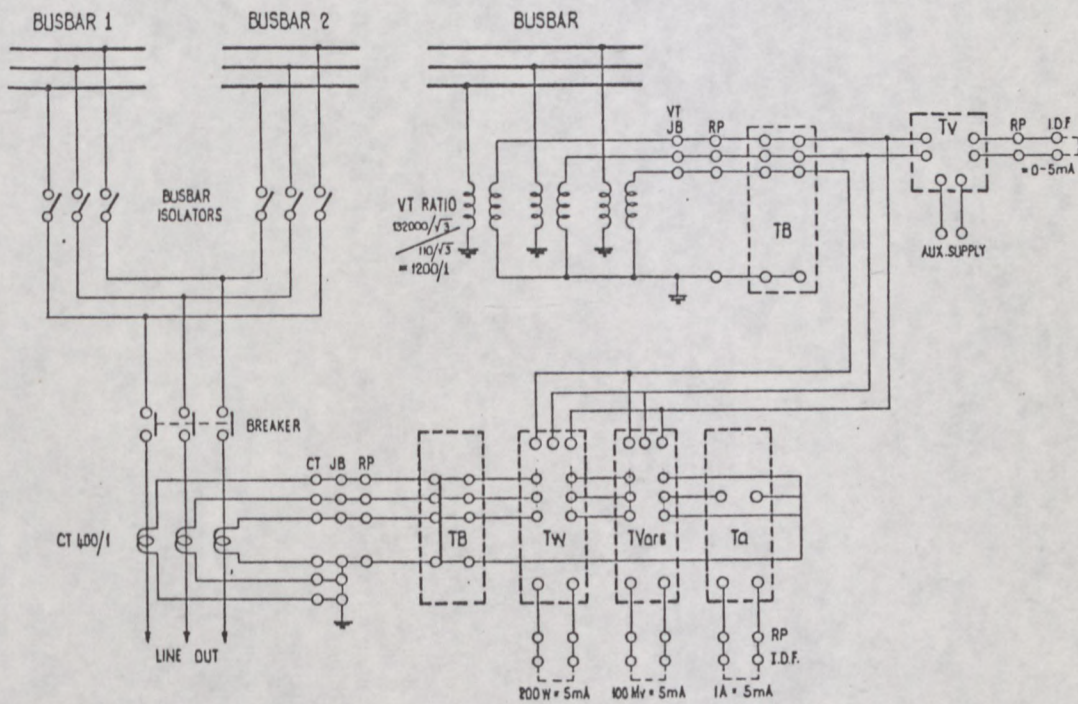


Fig. 10

As shown below the 8 analogue quantities to be transmitted, are permanently present at the input of the remote via the transducers.

Input currents to the remote may vary from 0 to ± 20 mA max; however, the remote may be adapted for lower values of input current.

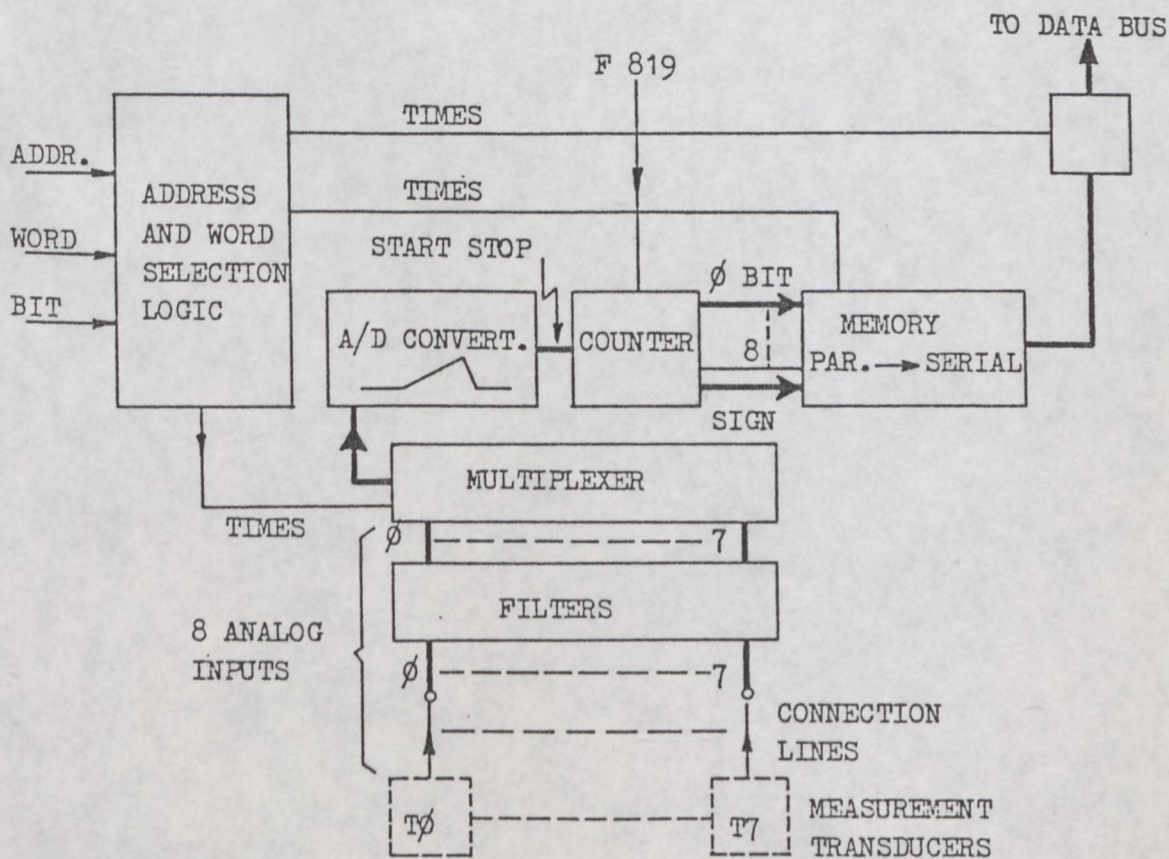


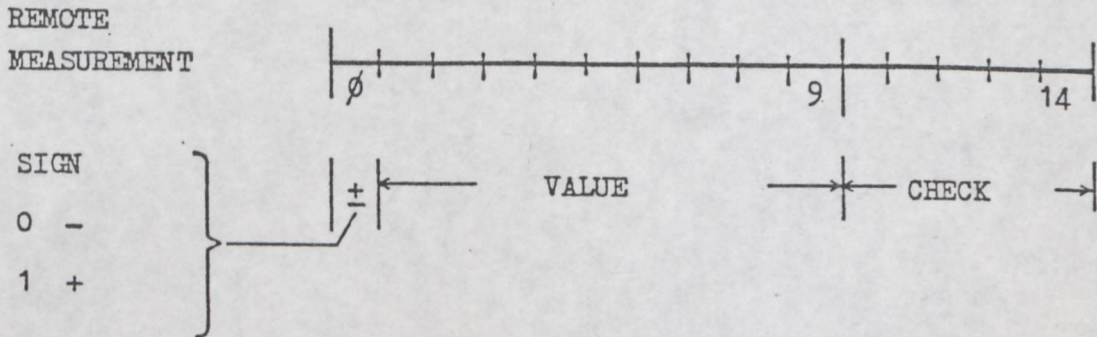
Fig. 11

As shown above the input quantities are sent to the multiplexer, which connects them to the A/D converter one at a time.

This circuit converts the analog quantity into a 9 bit digital quantity, plus one bit for sign. The counter contents are then sent to the parallel to serial converter and then to the output card via the system bus.

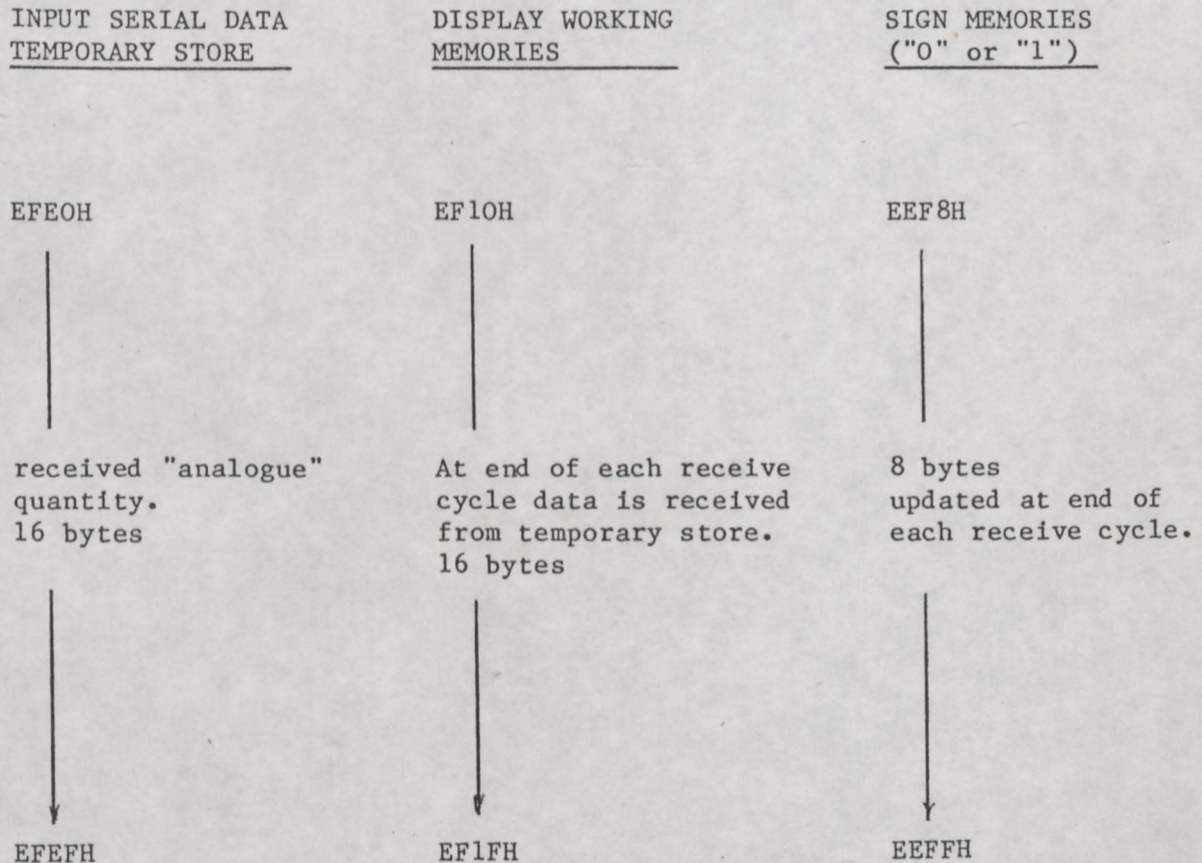
In the output card 5 check bits are generated for each analogue quantity, then the 1 bit sign, plus the 9 bit count and the 5 check bits are sent to the master or the Selta test set as a 15 bit word.

Remote measurement bit format.

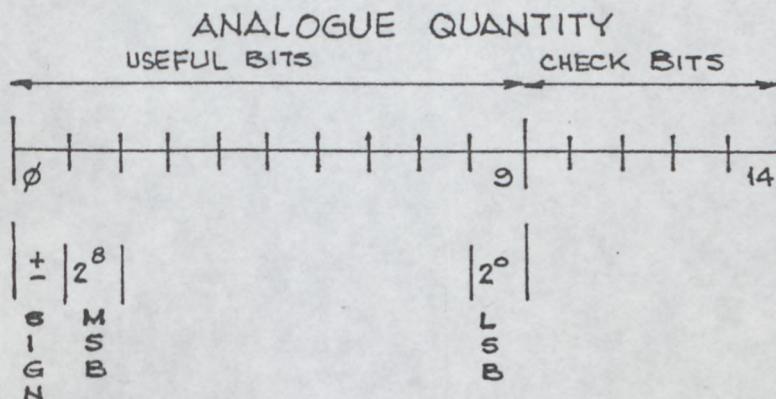


The test set receives the 8 "analogue" words and stores them in memory locations EFEOH - EFEFH note we use 16 bytes, or 2 bytes per "analog" quantity. The above memory locations act as input serial data temporary store and at the end of each received message the memory contents of EFEOH - EFEFH are transferred to the display working memory locations EF10H - EF1FH as shown below.

The above transfer was done to prevent the analogue quantities displayed on the screen from changing during update/calculations.

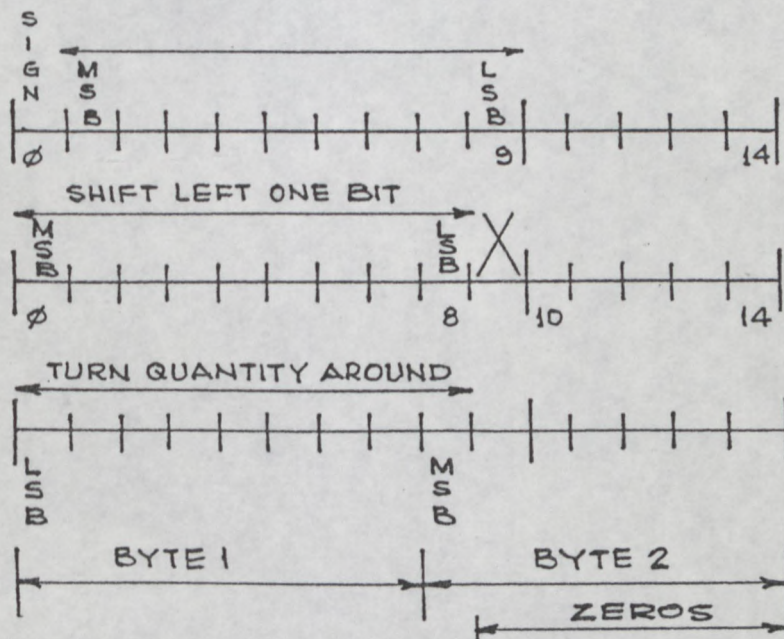


Further explanations are simplified by referring to only one analogue quantity. The analogue quantity is received from the remote in the following format.



The sign is stored in memory locations EE8H - EEFH, (for 8 analogues) and the 5 bit check is removed.

The analogue quantity is adjusted left one bit and then it is turned around.



Note that the 9 bits are stored in two bytes and are moved from EF0/1H to EF10/11H.

Assuming that the quantity received from the remote is $485_{(10)}$, Hex equivalent 1E5H, this quantity will be stored in memory as follows:

EF10H = E5H

EF11H = 01H

Now the received quantity will be multiplied by a scaling factor (multiplier), to produce a product saved on the calculator stack. The product is then divided by scaling factor No 2, the quotient is our required quantity.

More detail on the floating point calculator will be given further on.

The Selta remote analog input card is calibrated to give a maximum count of 500 not (511).

Assuming that a 500 count is to be equal to 1600 MW. We obtain the 1600 by doing the following simple calculation.

$$(500 \times 32) \div 10 = 1600$$

in the following example it is assumed that a 485 count is received.

Therefore: $(485 \times 32) \div 10 = 1552$

$$1552_{(10)} = 0610H$$

0610H is stored in memory locations EF40H - EF41H. The memory locations set aside for the 8 analogues are EF40H to EF4FH.

The following program executes a floating point multiplication and division, using the modified received data from the remote and the previously stored scaling factors.

```
LD      C,      (EF10H)    ;   modified received
LD      B,      (EF11H)    ;   quantity.
Call    2D2BH              ;   "stack BC": Floating point form to
                             value held in BC, then store on
                             calculator stack.

LD      C,      (EF20H)    ;   load scaling factor
LD      B,      (EF21H)    ;   *32
Call    2D2BH              ;   "stack BC" F. point form to value
                             held in BC, store on calculator
                             stack.

RST     28H                ;   call 335BH (F. Point calculator)
DEFB    04H                ;   multiplication call 30CAH.
DEFB    38H                ;   "End calc" or return from calc.

LD      C,      (EF30H)    ;   load scaling factor
LD      B,      (EF31H)    ;   ÷ 10.
Call    2D2BH              ;   "stack BC" F. point form to value
                             held in BC, store on calculator
                             stack.

RST     28H                ;   call 335BH (F.P - calculator)
DEFB    05H                ;   division call 31AFH
DEFB    27H                ;   Integer call 36AFH
DEFB    38H                ;   "End calc" return from calc.

CALL    2DA2H              ;   Floating point to BC subroutine.

LD      (EF40H),C          }
LD      (EF41H),B          } ;   store result in memory.
```

For further details on the floating point calculator refer to the complete Spectrum ROM disassembly manual by Dr. Ian Logan.

As can be seen from the last two steps in the program on the previous page the result is stored as follows:

EF40H = 10H

EF41H = 06H

The above quantity must now be converted into a 4 digit "decimal" value, this is achieved by executing a series of subtractions and additions checking the carry flag.

Explanation as follows:

HL register pair is loaded with the analogue value

HL = 0610H

The BC register pair will be loaded with the following quantities in turn:

BC = 03E8H = 1000₍₁₀₎

BC = 0064H = 100₍₁₀₎

BC = 000AH = 10₍₁₀₎

The BC register pair contents are subtracted from the HL register pair contents, counting the number of subtractions until a negative result is produced. Once this occurs, the result is restored to a positive quantity.

The subtrahend stored in BC register pair is changed to the next value and we subtract again.

A short example is given below:

Load HL = 0610H = (1552₁₀) LOAD BC = 03E8H = 1000₍₁₀₎

The subtractions are done by taking the two's complement of BC contents and adding it to HL.

2's complement of 03E8H =	0000 0011 1110 1000	
	1111 1100 0001 0111 +	1's
	<u> 1</u>	
	1111 1100 0001 1000	2's

Start of subtractions

The carry flag is set to a 1 for a borrow and reset to 0 if there is no borrow.

(Sub)	0000	0110	0001	0000	(HL-BC)
C	1111	1100	0001	1000	
0 1	0000	0010	0010	1000	INC (EF5DH) → 01H

(Sub)	0000	0010	0010	1000	(HL-BC)
C	1111	1100	0001	1000	
1 0	1111	1110	0100	0000	INC (EF5DH) → 02H

(Add)	1111	1110	0100	0000	(HL + BC) restore
C	0000	0011	1110	1000	DEC (EF5DH) → 01H
0 1	0000	0010	0010	1000	

Note: EF5DH will contain 01H, and the contents of BC register pair are changed to 0064H in preparation for the next lot of subtractions.

HL = 0228H, BC = 0064H, EF5EH will now be used as counter.

2's complement of BC contents is as follows:

0000	0000	0110	0100	
1111	1111	1001	1011	1's
			1	
1111	1111	1001	1100	2's

Start of subtractions

(Sub)	0000	0010	0010	1000	(HL - BC)
C	1111	1111	1001	1100	
0 1	0000	0001	1100	0100	INC (EF5EH) → 01H

(Sub)	0000	0001	1100	0100	(HL - BC)
C	1111	1111	1001	1100	
0 1	0000	0001	0110	0000	INC (EF5EH) → 02H

(Sub)	0000	0001	0110	0000	(HL - BC)
C	1111	1111	1001	1100	
0 1	0000	0000	1111	1100	INC (EF5EH) → 03H

(Sub)	0000	0000	1111	1100	(HL - BC)
C	1111	1111	1001	1100	
0 1	0000	0000	1001	1000	INC (EF5EH) → 04H

(Sub)	0000	0000	1001	1000	(HL - BC)
C	1111	1111	1001	1100	
0 1	0000	0000	0011	0100	INC (EF5EH) → 05H

(Sub)	0000	0000	0011	0100	(HL - BC)
C	1111	1111	1001	1100	
1 0	1111	1111	1101	0000	INC (EF5EH) → 06H

(Add)	1111	1111	1101	0000	(HL + BC) restore
C	0000	0000	0110	0100	
0 1	0000	0000	0011	0100	DEC (EF5EH) → 05H

NOTE: EF5EH will contain 05H and the contents of BC register pair are changed to 000AH in preparation for the next lot of subtractions.

HL = 0034H, BC = 000AH, EF5FH will now be used as counter.

2's complement of BC contents is as follows:

0000	0000	0000	1010	
1111	1111	1111	0101	1's
			1	
1111	1111	1111	0110	2's

Start of subtractions

(Sub)	0000	0000	0011	0100	(HL - BC)
C	1111	1111	1111	0110	
0 1	0000	0000	0010	1010	INC (EF5FH) → 01H

(Sub)	0000	0000	0010	1010	(HL - BC)
C	1111	1111	1111	0110	
0 1	0000	0000	0010	0000	INC (EF5FH) → 02H

(Sub)	0000	0000	0010	0000	(HL - BC)
C	1111	1111	1111	0110	
0 1	0000	0000	0001	0110	INC (EF5FH) → 03H

(Sub)	0000	0000	0001	0110	(HL - BC)
C	1111	1111	1111	0110	
0 1	0000	0000	0000	1100	INC (EF5FH) → 04H

(Sub)	0000	0000	0000	1100	(HL - BC)
C	1111	1111	1111	0110	
0 1	0000	0000	0000	0010	INC (EF5FH) → 05H

(Sub)		0000	0000	0000	0010	(HL - BC)
C		1111	1111	1111	0110	
1	0	1111	1111	1111	1000	INC (EF5FH) → 06H

(Add)		1111	1111	1111	1000	(HL + BC) restore
C		0000	0000	0000	1010	
0	1	0000	0000	0000	0010	DEC (EF5FH) → 05H

Having executed 3 lots of subtractions/additions, the remainder left in the HL register pair, is stored in memory location EF60H (Note: least significant byte only).

The memory contents of EF5DH to EF60H are as follows:

EF5DH	EF5EH	EF5FH	EF60H
01H	05H	05H	02H

To display the contents of the above memory locations add 30H to convert the memory contents to ASCII characters, also one must remember that EE8H contains the sign.

EE8H	EF5DH	EF5EH	EF5FH	EF60H
2BH	31H	35H	35H	32H

The print routine will now display the above memory contents on screen as +1552.

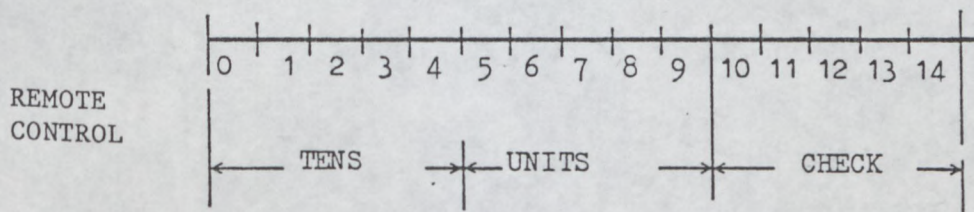
5.0 REMOTE CONTROLS

A standard Selta remote is equipped with 3 output control cards. This enables the remote to execute a total of 60 remote controls, as received from the master or test set.

As previously seen the remote control message consists of 5 words. They are as follows: TELEC, GTC, TC, $\overline{\text{GTC}}$, $\overline{\text{TC}}$ (Synch and PVX are also included).

Here the generation of TC and $\overline{\text{TC}}$ will be discussed briefly.

The remote control word format is shown below.



Note that 100 different combinations may be achieved using the above word format.

The tens and units are obtained using a 2/5 code, 5 bits per digit (tens and units) of which 2 bits will be one's and the other 3 will be zero's.

2/5 table shown below.

BITS

	1	2	3	4	5
0	1	1	0	0	0
1	1	0	1	0	0
2	1	0	0	1	0
3	1	0	0	0	1
4	0	1	1	0	0
5	0	1	0	1	0
6	0	1	0	0	1
7	0	0	1	1	0
8	0	0	1	0	1
9	0	0	0	1	1

Remote control "0", TC word bit format fetched from the look up table is as follows:

BITS:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	1	0	0	0	1	1	0	0	0	1	1	1	0	0
TENS					UNITS					CHECK				

Remote control 30, TC word bit format is as follows:

BITS:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	0	0	0	1	1	1	0	0	0	1	0	1	1	0

TENS					UNITS					CHECK				
------	--	--	--	--	-------	--	--	--	--	-------	--	--	--	--

Once the required control is entered via the keyboard the program will convert the entry into the required code.

As already shown the words sent to the remote for the execution of a control are as follows:

*	SYNCH	0F59H	Synchronizing word
	PVX	FFOBH	empty word
	TELEC	67A4H	fixed Telecontrol word
	GTC	1C63H	Group telecontrol selected at remote by means of straps
	TC	XXXXH	Keyed in telecontrol
	$\overline{\text{GTC}}$	9C07H	negated group telecontrol
	$\overline{\text{TC}}$	XXXXH	negated telecontrol
*	SYNCH	0F59H	Synchronizing word to control remotes message length

The above words are stored in memory locations F00FH to F01CH. It must be pointed out that F00FH and F010H will first store 0F59H, 1st synch word. Then it's contents will be changed to FFOBH or PVX empty word.

Remote Control key entry.

Controls selected via the keyboard may be from 1 to 30, open or close. These entries in turn generate the following table and it's values are used to calculate the offset to obtain TC and $\overline{\text{TC}}$ words.

CONTROL	C	O	CONTROL	C	O	C = Close O = Open
01	0,	1	16	30,	31	
02	2,	3	17	32,	33	
03	4,	5	18	34,	35	
04	6,	7	19	36,	37	
05	8,	9	20	38,	39	
06	10,	11	21	40,	41	
07	12,	13	22	42,	43	
08	14,	15	23	44,	45	
09	16,	17	24	46,	47	
10	18,	19	25	48,	49	
11	20,	21	26	50,	51	
12	22,	23	27	52,	53	
13	24,	25	28	54,	55	
14	26,	27	29	56,	57	
15	28,	29	30	58,	59	

Example: Assuming (01C) has been entered then an offset of 00H will be obtained.

If (090) is entered then an offset of 17 is obtained. See control table on previous page.

Procedure as follows:

Assume (19C), 19 close, has been selected. The 3 key entries will be stored in memory as follows:

FO08H	FO09H	FO0AH
31H	39H	43H

The first two bytes are combined to produce 19H, stored as follows:

FO0BH
19H

Depending on the contents of FO08H, the following values will be subtracted from the contents of FO0BH.

30 if 01 - 09 key entry	subtract value 00H
31 if 10 - 19 key entry	subtract value 06H
32 if 20 - 29 key entry	subtract value 0CH
33 if 30 - - key entry	subtract value 12H

Entered value was 19, so 06H will be subtracted from FO0BH contents.

2's complement of 06H

INVERT	0	0	0	0	0	1	1	0	
	1	1	1	1	1	0	0	1	+
								1	1's
	1	1	1	1	1	0	1	0	2's

2's complement "subtraction"

0	0	0	1	1	0	0	1
1	1	1	1	1	0	1	0
0	0	0	1	0	0	1	1

FO0BH will now contain 0001 0011 or 13H.

Now shift contents of FO0BH left one bit.

0001 0011 - left one bit
0010 0110 - new value

(FO0BH) = 0010 0110 or 26H

Now FO0AH contents must be tested for close/open condition.

43H = C (close) and 4FH = 0 (open)

If equal to 43H, subtract 2 from FO0BH contents.

If equal to 4FH, then subtract 1 from FOOBH contents. In our example it was 43H.

(FOOBH) - 2 → (FOOBH)

2's complement of 2

INVERT

0	0	0	0	0	0	1	0		
1	1	1	1	1	1	0	1	+	1's
							1		
1	1	1	1	1	1	1	1	0	2's

"subtraction":	0	0	1	0	0	1	1	0
	1	1	1	1	1	1	1	0
	0	0	1	0	0	1	0	0

(FOOBH) = 24H or 36₍₁₀₎

As shown previously 19 close = 36₍₁₀₎

19 open = 37₍₁₀₎

The required offset is 24H.

The look up table stores (TC and $\overline{TC}$ words) each remote control, in two memory locations, hence we must multiply our offset by two.

Shift (FOOBH) contents left one place.

```
LD A, (FOOBH)
SL A
LD (FOOBH), A
```

Store back in location FOOBH.

(FOOBH) = 01001000 or 48H.

The modified offset will be added to the contents of IX and HL registers to point to the required control words.

LOAD IX, HL as follows:

IX = E000H start of TC table

HL = E078H start of $\overline{TC}$ table.

The program will execute the following:

```
A. LD BC, (FOOBH)
ADD IX, BC
LD A, (IX + 00H)
LD (F015H), A
LD A, (IX + 01H)
LD (F016H), A
```



```
      ADD    HL, BC
      LD     A, (HL)
      LD     (F019H), A
B.    INC    HL
      LD     A, (HL)
      LD     (F01AH), A
```

As shown on the previous page

```
A:    BC = 48H
      IX = E000H      ADD IX, BC
```

after addition IX = E048H

```
At the end of A:      (F015H) = 51H
                      (F016H) = 2EH
```

```
B:    BC = 48H
      HL = E078H      ADD HL, BC
```

after addition HL = E0C0H

```
At the end of B:      (F019H) = AEH
                      (F01AH) = 35H
```

As shown above TC = 2E51H and $\overline{TC}$ = 35AEH.

Both control codes were fetched from the look-up table stored in memory locations E000H to E0EFH. The "control memory contents" before transmission are as follows:

F00FH	59H	FFH	SYNCH, PVX
F010H	0FH	0BH	
F011H		A4H	TELEC
F012H		67H	
F013H		63H	GTC
F014H		1CH	
F015H		51H	TC
F016H		2EH	
F017H		9CH	$\overline{GTC}$
F018H		07H	
F019H		AEH	$\overline{TC}$
F01AH		35H	
F01BH		59H	SYNCH
F01CH		0FH	

The above bytes will be sent sequentially to the remote to execute remote control 19 close. For further details see program listing and flow charts.

6.0 ALARMS

A standard Selta remote is equipped with one alarm card, enabling the remote to send 20 single bit alarms to the master or test set.

The 20 alarms are sent in two consecutive words. Each word has 10 bits of information relating to the substation alarms state.

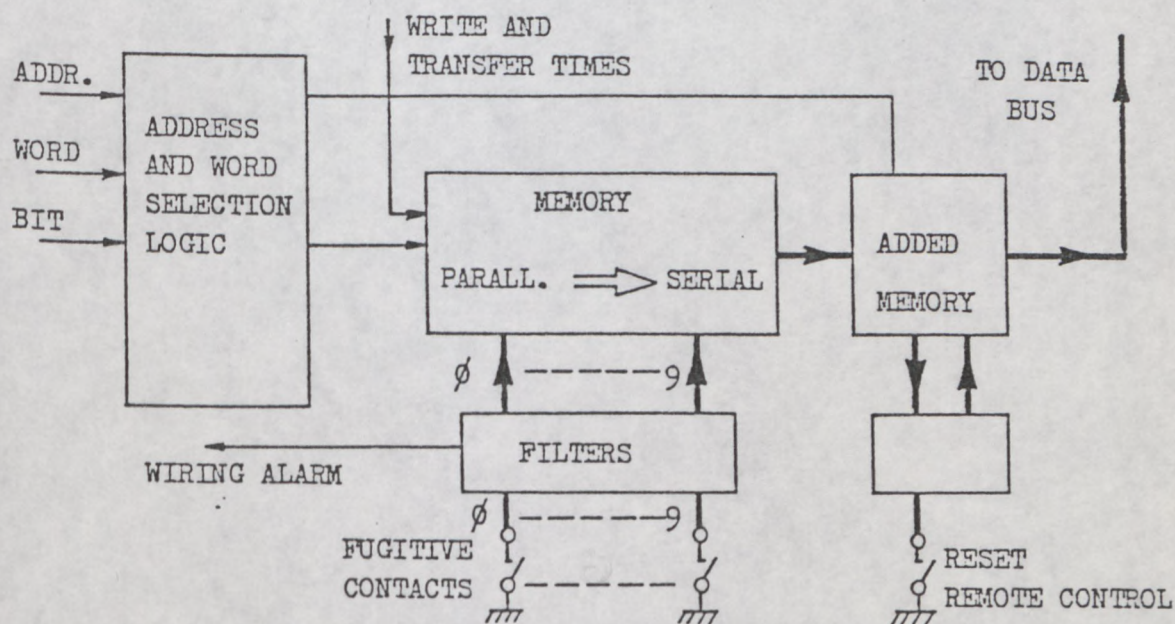


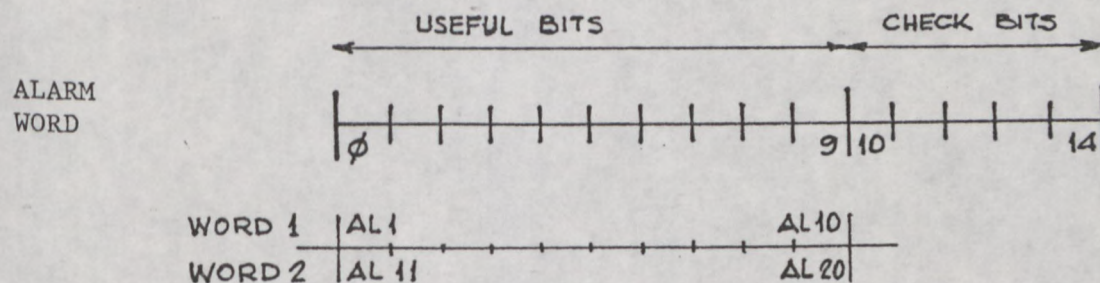
Fig. 12

As shown above is fig. 12, the potential free contacts are connected to the parallel to serial converter via the input filters.

The two consecutive alarm words are then sent to the output card via the system bus.

In the output card the bit check is worked out (5 bit check) and sent to the master, with every 10 bits of information.

The transmitted alarm bit format is as follows:



The following is a brief explanation of how the two alarm words received from the remote are displayed on the screen.

As mentioned previously, 16 words of data are received from the Selta remote and stored in the input serial data temporary store. Memory locations used for the temporary store are EFDOH to EFEFH.

The Contents of the temporary store are transferred to the display working memories EFOOH to EF1FH, at the end of every message received from the remote. The above transfer is to prevent the displayed data from changing on the screen during updating/conversion.

Display working memory locations EFOCH to EFOFH store the two alarm words to be displayed.

The check bits are removed from the 2 alarm words. The 1st group of 10 bits stored in memory locations EFOCH and EFODH are shifted into memory locations EFA5H to EFAEH.

The second group of 10 bits stored in memory locations EFOEH to EFOFH will be shifted into memory locations EFAFH to EFB8H.

At the end of the 20 bit shift the contents of memory locations EFA5H to EFB8H will be either 80H or 00H.

The following is a short routine to convert the 80H or 00H stored in the above memories, into display characters F (fault) or T (true).

```
LD    HL, EFA5H      ;    load conversion start address
LD    E, 00H         ;    E used as counter
GIU4   LD    A, (HL)
CP     00H
JR     Z, GIU0
CP     80H
JR     Z, GIU1
GIU0   LD    (HL), 46H ;    replace the 00H with 46H or (F) fault
JR     GIU3
GIU1   LD    (HL), 54H ;    replace the 80H with 54H or (T).
GIU3   INC    HL
INC     E             ;    increment loop counter
LD     A, E
CP     14H           ;    check if 20 memories converted
JR     NZ, GIU4

(F) fault = 46H
(T) true  = 54H
```

At the end of the above short routine, the contents of memory locations EFA5H to EFB8H will be either T or F.

EFA5H to EFA5H will be displayed as alarms, page 1.
EFADH to EFB8H will be displayed as alarms, page 2.

For further details see program listing and flow charts.

7.0 BREAKER RETURN INDICATIONS (B.R.I.)

A standard Selta STO-E remote is equipped with 3 B.R.I. emitter cards, enabling the remote to transmit to the master, or test set, a total of 30 double B.R.I. sent as 6 sequential words.

The B.R.I. contacts from the plant are connected to the parallel/serial converter via the input filters. The data stored in the memory is sent to the output circuitry via the system bus.

See block diagram shown in fig. 13.

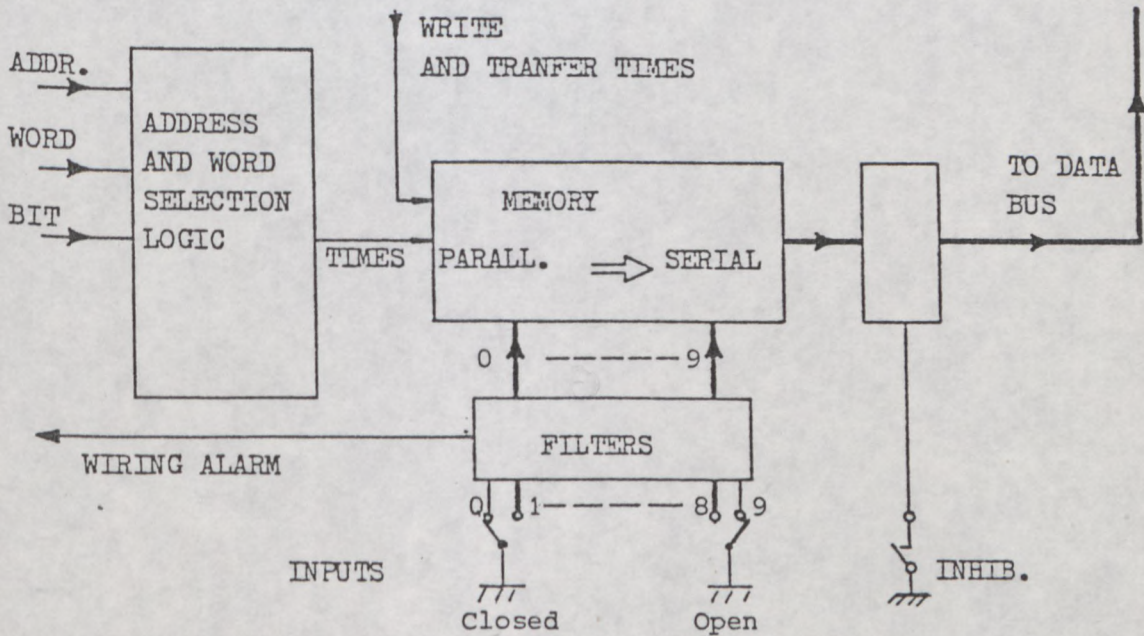


Fig. 13

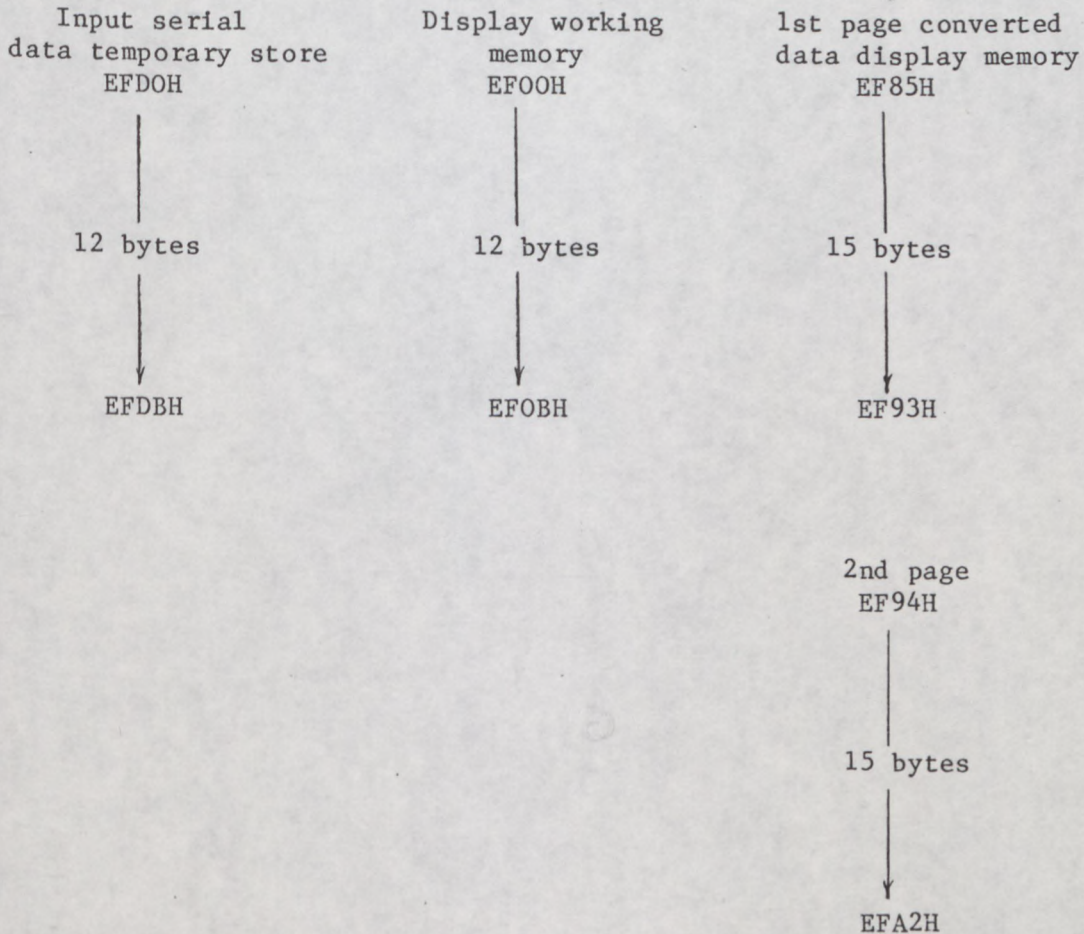
The output circuit will add 5 check bits, to every 10 bits of information received. The 15 bits are then transmitted to the master, as a word.

The B.R.I. bit format is shown below.

BRI	INFORMATION										CHECK	
WORD	0	1	2	3	4	5	6	7	8	9	10	- 14
	CL	OP	CL	OP	CL	OP	CL	OP	CL	OP		

CL = CLOSE, OP = OPEN

The 6 B.R.I. words transmitted from the remote are received by the "test set" and stored as follows:



The received data is transferred from the input serial temporary store, to the display working memory at the end of every received message. This prevents the B.R.I. status displayed on the screen, from changing during update/conversion.

The 6 B.R.I. words stored in 12 bytes of the display working memory, are shifted sequentially into memory locations EF85H to EFA2H.

At the end of the shift, the contents of the above 30 memory locations will be either 00H, 40H, 80H, COH, depending on the breaker status.

A short routine will then convert the stored contents of EF85H to EFA2H into ASCII characters to be displayed on the screen.

00H = 41H = A for anomaly

COH = 41H = A for anomaly

40H = 4FH = 0 for open

80H = 43H = C for closed.

The following routine shifts the 6 words of B.R.I. received from the remote, into 30 bytes of the converted data display memory.

```
ROUT    LD    D, 00H          ; clear word counter.
        LD    HL, EF85H       ; 1st location of converted data display
                                memory.
        LD    IX, EF00H       ; 1st location display working memory.
BIT 1    LD    E, 00H         ; E used as 4 pairs, BRI counter.
        SCF
        CCF                  ; clear carry flag.
BIT 0    LD    (HL), 00H      ; clear converted data display memory
                                location.
        RRC    (IX + 00H)     ; rotate right into carry.
        RR     (HL)
        INC    HL             ; increment pointer to new converted data
                                display memory.
        INC    E              ; increment pair counter.
        LD     A, E
        CP     04H            ; have 4 pairs of BRI been done
        JR     NZ, BIT 0      ; if not go to BIT 0.
        INC    IX             ; increment pointer display working memory.
        LD     (HL), 00H
        RRC    (IX + 00H)
        RR     (HL)
        RRC    (IX + 00H)
        RR     (HL)
        RLC    (IX + 00H)     ; rotate left - restore 2 most
                                significant bits of BRI word.
        RLC    (IX + 00H)
        INC    HL
        INC    D              ; increment word counter.
        INC    IX             ; increment pointer display working memory.
        LD     A, D
        CP     06H            ; have 6 words been done.
        JR     NZ, BIT 1
```


The following table shows the relationship between the 2 bits of a double B.R.I.

	INPUT 0	INPUT 1	CONDITION	DISPLAYED ON SCREEN
(a)	0	0	anomaly	A
(b)	0	1	open	O
(c)	1	0	closed	C
(d)	1	1	anomaly	A

Note that input combinations (a) and (d), will only occur under a fault condition.

For further details see program listing and Flow Charts.

8.0 PROGRAMMING THE Z80 P.I.O.

Programmable Input/Output

The operating mode is established by writing a control word in the control register.

Modes of operation are as follows:

Mode 0	output
Mode 1	input
Mode 2	Bidirectional
Mode 3	Bit control

In our case, Port A is programmed for mode 3 and Port B for mode 0.

- Consider Mode 3: (No handshake required).
(Control)
- (a) Write mode 3 word to the control register.
 - (b) Write input/output control register word selecting port data bus lines as input/output.
 - (c) Interrupt vector (must be loaded).
 - (d) Write the interrupt control word.

Interrupt Control Word = 07H

BITS:	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	<u>0</u>	<u>1</u>	<u>1</u>	<u>1</u>

Identifies control word

- D4 = 0 No mask word follows
- D5 = 0 Input active level low
- D6 = 0 Interrupt generated on "or" function
- D7 = 0 Interrupt disabled

Mode 0 operation: Port B is programmed in this mode, only two words are required; they are as follows:

- (a) Write mode 0 control word to control register.
 - (b) Send required data to data output register.
- (No handshake required)

The Z80 PIO was programmed as follows:

Address port A control register = DBH
Address port B control register = FBH
Address port A data output register = 9BH
Address port B data output register = BBH

```
LD    A, CFH          ; send control word to Port A control register.
OUT   (DBH), A        ; mode 3 operation has been selected.
LD    A, 80H          ; select input, output bits.
OUT   (DBH), A        ; bit 7 = input, the other 7 bits are outputs.
LD    A, FEH          ; Program vector "even if not used"
OUT   (DBH), A        ; send to control register of port A.
LD    A, 07H          ; load, interrupt control word, ENAB INT = 0 BIT 7,
OUT   (DBH), A        ; and/or = 0 bit 6, high/low = 0 bit 5, mask
                        ; follows = 0-bit 4.
LD    A, OFH          ; send control word to port B (output)
OUT   (FBH), A        ; Mode 0 operation has been selected.
LD    A, 00H          ; load acc with 00H, and clear
OUT   (BBH), A        ; port B data lines.
```

Loading the start address of the program, running under the control of the NMI.

Start address AC80H.

```
LD    A, 80H
LD    (5C80H), A
LD    A, ACH
LD    (5CB1H), A
```

Set Port A, bit PA0 to 01H, enable NMI.

```
LD    A, 01H
OUT   (9BH), A
```

NB: When programming one port of the Z80 P.I.O. for mode 3 operation, the INT vector must be loaded, (even if not used).

Omitting the vector will cause problems in programming the other port.

Routine to : Display "END OF PROGRAM" AND DISABLE NMI.

```

DOWN 1    LD      B, 18H

          CALL    OE44H      ; clear 18 lines of screen.

          LD      HL, F810H   ; load start address of message.

          CALL    Disp       ; Print message.

          LD      A, 00H      ; load acc with 00H.

          OUT     (9BH), A    ; clear PA0 of Z80 PIO.
                                This will disable the NMI

          RET                ; Return
    
```

The Z80 P.I.O. pin connections are shown below in Fig. 14.

For further details on the Z80 P.I.O. refer to the Appendix.

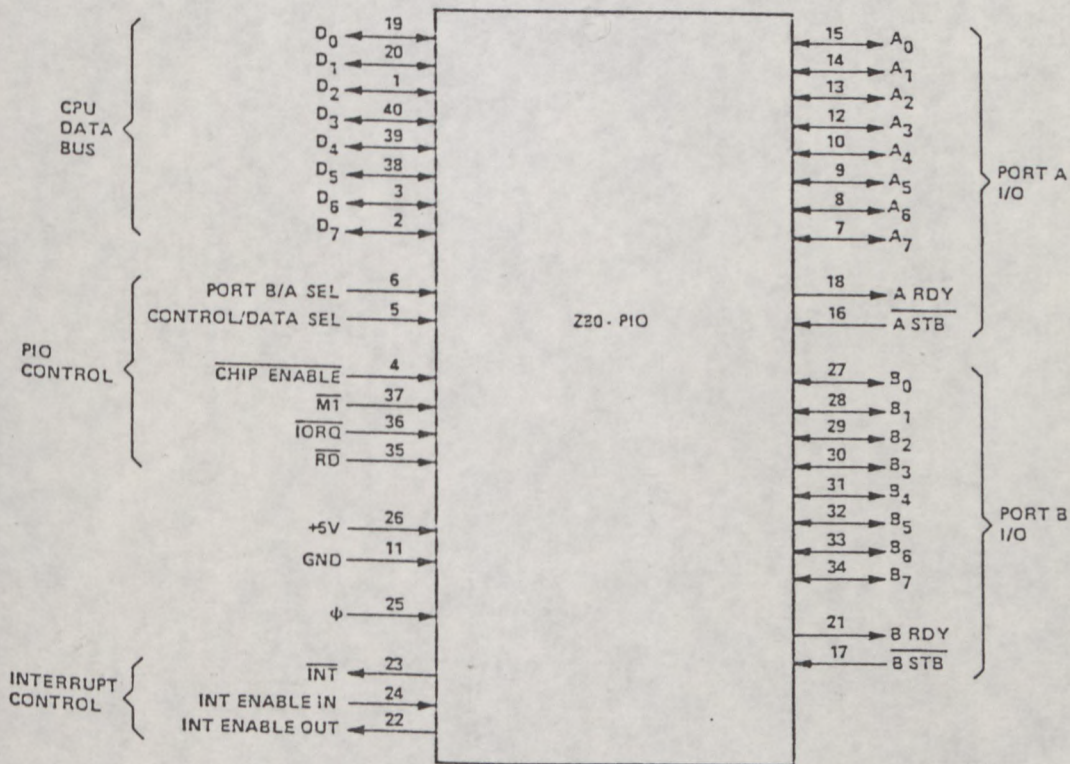
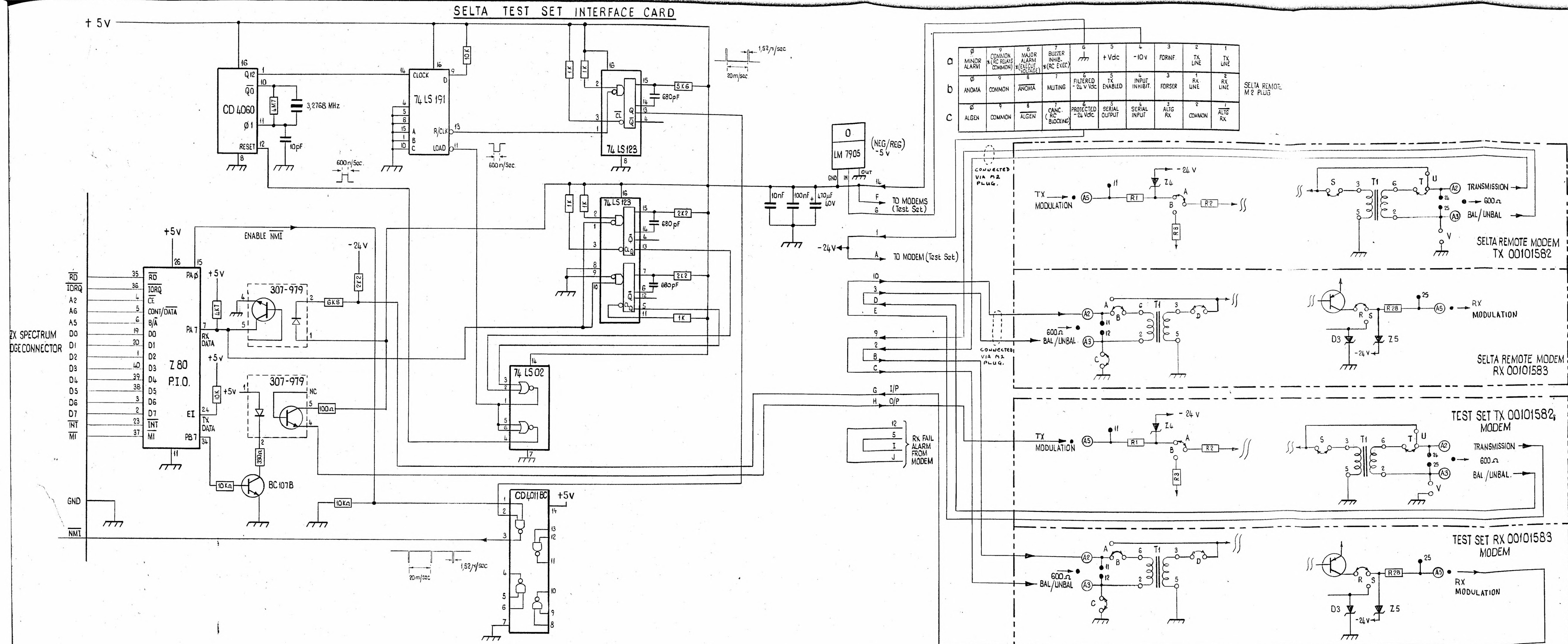


Fig. 14



WAVE FORMS - INTERFACE CARD

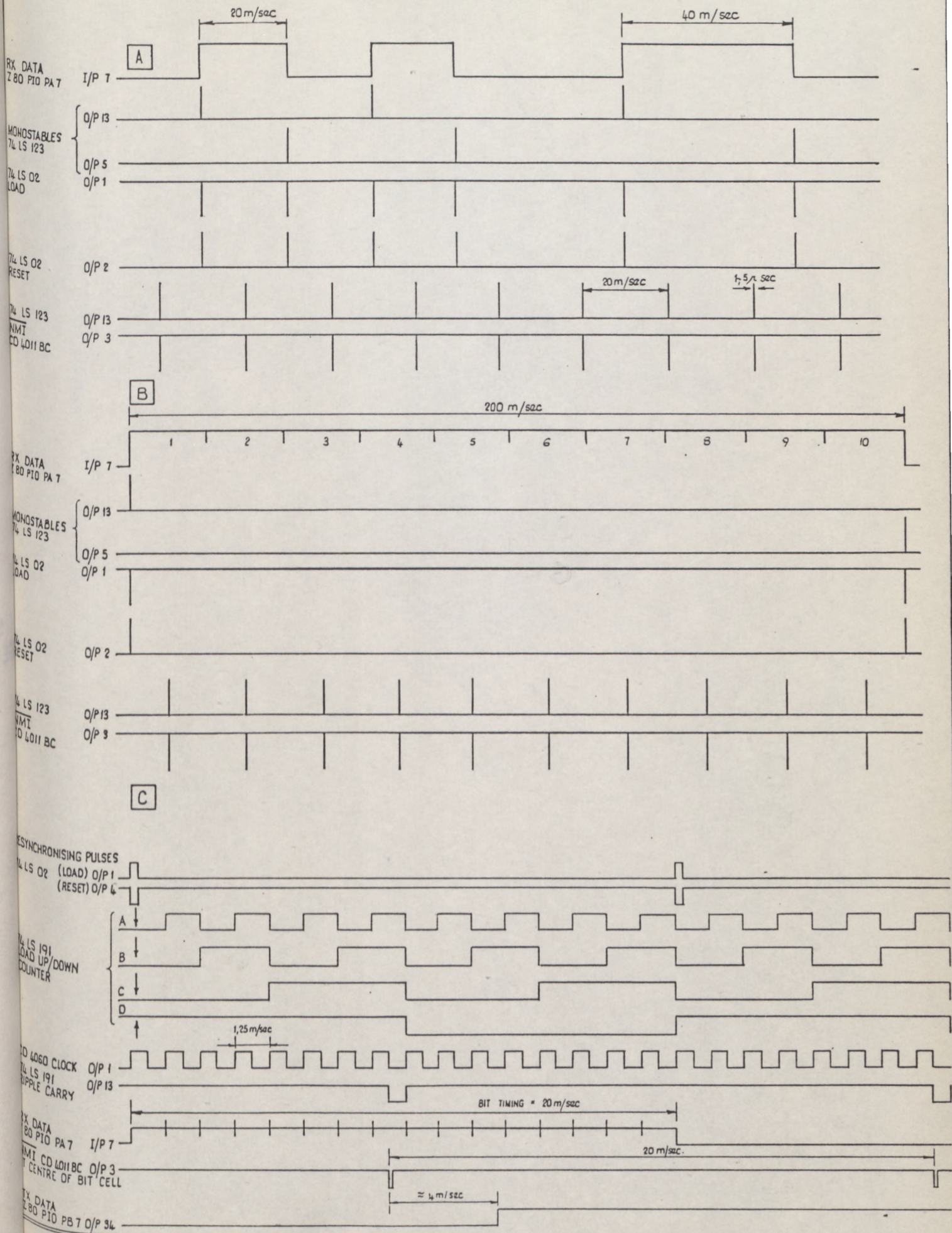


FIG. 15

9.0 INTERFACE CARD

The following is a brief explanation on the given wave forms in fig. 15. Two different Rx input data waveforms are discussed in PART A and PART B.

PART A:

Varying input data is shown on Pin 7, PA7 of the Z80 P.I.O. The 0-1 and 1-0 transitions are detected by the two monostables in the 74LS123 outputs pins 13, 5. The two pulses are combined by the 74LS02 NOR gate and it produces LOAD and RESET pulses for the 74LS191 counter and the CD4060BC 14 stage ripple counter respectively. Under worst conditions synchronization occurs after 40 m/sec. See Rx data Z80 P.I.O. PA7 waveform.

PART B:

Synchronization under worst condition occurs after 200 m/sec this would occur when receiving PVX empty words OBFFH. Pin 7, PA7 of the Z80 P.I.O. would remain high for a total of 10 bits. See Rx data Z80 P.I.O. PA7 waveform.

PART C:

Shown are the expanded waveforms of the events occurring between each generated LOAD and RESET pulses and their relationship to the NMI pulse. It is assumed that 0-1 and 1-0 transitions occur within 20 m/sec. The 74LS191 is loaded with a count of 8, it will then count up and produce an output pulse on the count of 15. The output pulse will be in the centre of the bit cell of the received data.

NB: The transmitted data from the Z80 P.I.O. PB7 output pin 34, is delayed approximately 4 m/sec by means of a software loop. This delay in transmission is introduced so that the transmitted "bits" from the test set coincide with the remote's input data sampling pulses. A further delay is introduced by the test set TX modem and the Selta remote RX modem.

For further details refer to the circuit diagram on page 41.

10.0 CONNECTING THE TEST SET

Communication between master and remote is interrupted by removing the M2 plug situated on the back connector plate of the remote. The remote's (Rx, Tx) modems are thus disconnected from the communication channel.

The test set may then be connected to the Selta remote via the M2 plug of the remote.

NB: -10 Volts from the remote's power supply is supplied to the test set interface card via the M2 plug.

11.0 LOADING/RUNNING THE SELTA TEST SET

To load and run the Selta test set do the following:

- (a) Load/run "TEST" from either Prog 1, Prog 2 cassettes.
- (b) Insert cassette with substation parameters.
- (c) Key in substation name then press enter key.
- (d) Press continue and then the enter key (cassette may be removed).

The program listing shown below is a simple short program called "TEST" that does all the necessary loading to run the Selta test set programs.

NB: Ensure that the substation name is entered correctly.

```
10 REM PROGRAM TO LOAD AND RUN
20 REM SELTA TEST SET PROGRAMS
30 CLS
40 PLOT 0,0: DRAW 0,175
50 PLOT 0,175: DRAW 255,0
60 PLOT 255,175: DRAW 0,-175
70 PLOT 255,0: DRAW -255,0
80 PRINT AT 2,13; INVERSE 1;"SELTA"
90 PRINT AT 3,12; INVERSE 1;"TEST SET"
100 PRINT AT 5,3;"LOADING THE FOLLOWING 3"
110 PRINT AT 6,3;"PROGRAMS:"
120 PRINT AT 7,3;"(1) selta*13."
130 PRINT AT 8,3;"(2) IPR*2."
140 PRINT AT 9,3;"(3) TELEC*."
150 PRINT AT 11,3;"ONCE LOADED, ENTER D/BASE"
160 PRINT AT 12,3;"OF REQUIRED SUB STATION"
170 PRINT AT 7,16; FLASH 1;" "
180 LOAD *"m";1;"selta*13" CODE
190 PRINT AT 7,16; FLASH 0;" "
200 PRINT AT 8,16; FLASH 1;" "
210 LOAD *"m";1;"IPR*2" CODE
220 PRINT AT 8,16; FLASH 0;" "
230 PRINT AT 9,16; FLASH 1;" "
240 LOAD *"m";1;"TELEC*" CODE
250 PRINT AT 9,16; FLASH 0;" "
260 PRINT AT 13,3;"INSERT D/BASE CASSETTE"
270 PRINT AT 14,3;"TYPE IN SUB STATION NAME"
280 INPUT " SUB STATION NAME:";a$
290 PRINT AT 15,3;"LOADING:"; FLASH 1;a$
300 LOAD *"m";1;a$ CODE
310 PRINT AT 15,11;a$
320 PRINT AT 16,3;"YOU MAY REMOVE CASSETTE."
330 PRINT AT 18,1;"TO RUN TEST SET,PRESS CONTINUE"
340 PRINT AT 19,3;"THEN PRESS ENTER KEY."
350 STOP
360 RANDOMIZE USR 40064
```


12.0 PROGRAM LISTING

The following is a brief explanation on the program contents.

12.1 "Selta * 13"; Locations 9C80H to A764H.

Is the main program and executes the following tasks.

- (a) Displays menu, data, prompts and detects key entries.
- (b) Moves data base to required locations.
- (c) Initialize memories, flags and the Z80PIO.
- (d) Converts/calculates analogue quantities and displays them on screen with sign.
- (e) Converts B.R.I. received data and displays it on screen as O, C, A.
- (f) Converts alarms received data and displays it on screen as T, F.
- (g) Accepts control entries with status and converts it into an appropriate code.

12.2 "IPR * 2"; Locations AC80H to AF59H.

This program is executed under control of the $\overline{\text{NMI}}$ and executes the following tasks.

- (a) Receives data from the remote and stores words in the appropriate memories.
- (b) Synchronizes the remote and resets the remote word counter at the required message length.
- (c) Sets up the remote control message, fetches control words from the look up table and sends the control message re-synchronizing the remote.
- (d) Controls the Full duplex communication between the remote and "test set".

12.3 "TELEC*"; Locations E000H to EOEFH.

Contains the look up table and stores TC and $\overline{\text{TC}}$ control words.

12.4 "SUBSTATION"; Locations F800H to FD90H.

DATA BASE The substation data base would be loaded into the machine, by selecting the required substation name.
NB: The relevant substation's information is stored on cassette in a predefined format. For further details see program listing.


```

■@9C80      0005      ORG  9C80H
0010 ;**** **** *****
0015 ;*MOV DATA BLOCK-OF-32BYTES-
0020 ;* FROM DATABASE-INFORMAT-
9C80 212DFE 0025 LD HL,0FE2DH
9C83 113FEF 0030 LD DE,0EF3FH
9C86 012000 0035 LD BC,0020H
9C89 EDB8 0040 LDDR
0045 ;**** **** *****
0050 ;*CLR LOC- EF00-EF1F-DISP-MEM
9C8B 3E00 0055 LD A,00H
9C8D 2100EF 0060 LD HL,0EF00H
9C90 0E20 0065 LD C,20H
9C92 77 0070 GIRO LD (HL),A
9C93 23 0075 INC HL
9C94 0D 0080 DEC C
9C95 20FB 0085 JR NZ,GIRO
0090 ;**** **** *****
0095 ;*ROU TINE STORE,+SIGN-IN-MEM
0100 ;* UNTIL-NMI-UPDATE..
9C97 3E2B 0105 LD A,2BH
9C99 21F8EE 0110 LD HL,0EEF8H
9C9C 0E08 0115 LD C,08H
9C9E 77 0120 GIR1 LD (HL),A
9C9F 23 0125 INC HL
9CA0 0D 0130 DEC C
9CA1 20FB 0135 JR NZ,GIR1
0140 ;**** **** *****
0145 ;*ROU TINE TO-INITIALIZE-Z80-
0150 ;* PIO- MODES-3&0-PORT-A+B
0155 ;* AND-ENABLE-NMI-INP
9CA3 3ECF 0160 LD A,0CFH
9CA5 D3DB 0165 OUT (0DBH),A
9CA7 3E80 0170 LD A,80H
9CA9 D3DB 0175 OUT (0DBH),A
9CAB 3EFE 0180 LD A,0FEH
9CAD D3DB 0185 OUT (0DBH),A
9CAF 3E07 0190 LD A,07H
9CB1 D3DB 0195 OUT (0DBH),A
9CB3 3E0F 0200 LD A,0FH
9CB5 D3FB 0205 OUT (0FBH),A
9CB7 3E00 0210 LD A,00H
9CB9 D3BB 0215 OUT (0BBH),A
9CBB 3E00 0220 LD A,00H
9CBD 32CDEF 0225 LD (0EFC0H),A
9CC0 32CAEF 0230 LD (0EFC0H),A
9CC3 32F6EF 0235 LD (0EFF6H),A
9CC6 3200F0 0240 LD (0F000H),A
9CC9 3201F0 0245 LD (0F001H),A
9CCC 322FF0 0246 LD (0F02FH),A
9CCF 3E80 0250 LD A,80H
9CD1 32B05C 0255 LD (5CB0H),A
9CD4 3EAC 0260 LD A,0ACH
9CD6 32B15C 0265 LD (5CB1H),A
9CD9 3E01 0270 LD A,01H
9CDB D37B 0275 OUT (07BH),A
0280 ;**** **** *****
0285 ;*INP MENU DISPLAYS,NAME,OPEN
0290 ;* CHAN,PRINT,MESSAGE
9CDD 0618 0295 MENU LD B,18H

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9CDF	CD440E	0300	CALL	0E44H
9CE2	3E02	0305	LD	A,02H
9CE4	CD0116	0310	CALL	1601H
9CE7	117EA2	0315	LD	DE,STAT
9CEA	011400	0320	LD	BC,14H
9CED	CD3C20	0325	CALL	203CH
9CF0	2100F8	0330	LD	HL,0F800H
9CF3	CDE49E	0335	CALL	DISP
9CF6	1192A2	0340	LD	DE,DAT
9CF9	019200	0345	LD	BC,92H
9CFC	CD3C20	0350	CALL	203CH
		0355	****	*****
		0360	PRNT	ENTER-SELECTED,NUM
		0365	MESSAGE-1,2,3,4.	
9CFF	1124A3	0370	LD	DE,DAT1
9D02	012100	0375	LD	BC,21H
9D05	CD3C20	0380	CALL	203CH
		0385	****	*****
		0390	INPT	FETCH-ROUT,STORES
		0395	KEY,DEPRESS,IN,MEM	
9D08	CDB010	0400	CALL	10B0H
9D0B	30FB	0405	JR	NC, TOP
9D0D	3200FF	0410	LD	(MEM), A
9D10	D7	0415	RST	0010H
		0420	****	*****
		0425	ROUT	ENTER,KEY-DETECT,&
		0430	RESTORE,PREV,INPUT	
9D11	CDB59E	0435	CALL	GET-K
9D14	3A00FF	0440	LD	A, (MEM)
		0445	****	*****
		0450	KEY	DEPRESSION-1,2,3,4
9D17	FE31	0455	CP	31H
9D19	CA459D	0460	JP	Z,BRI
9D1C	FE32	0465	CP	32H
9D1E	CAE29D	0470	JP	Z,ALARM
9D21	FE33	0475	CP	33H
9D23	CA769E	0480	JP	Z,ANAL
9D26	FE34	0485	CP	34H
9D28	CAEC9E	0490	JP	Z,DOWN1
9D2B	CDD59E	0495	CALL	MESS1
		0500	****	*****
		0505	KEY	CHECKING,EXIT/ENTR
		0510	KEY,DEPRESSIONS	
9D2E	CDB010	0515	CALL	10B0H
9D31	FE0D	0520	CP	0DH
9D33	CA3D9D	0525	JP	Z,DOWN2
9D36	FE65	0530	CP	65H
9D38	CAEC9E	0535	JP	Z,DOWN1
9D3B	20F1	0540	JR	NZ, AGAIN
		0545	****	*****
		0550	ROUT	5LINES, FROM, BOTTOM
9D3D	0605	0555	LD	B,5H
9D3F	CD440E	0560	CALL	0E44H
9D42	C3FF9C	0565	JP	UP1
		0570	****	*****
		0575	ROUT	TO-PRINT-PAGE-1
		0580	OF-BRI/CONTROLS	
9D45	0618	0585	LD	B,18H
9D47	CD440E	0590	CALL	0E44H
9D4A	2126F8	0595	LD	HL,0F826H

9D4D	CDE49E	0600	CALL	DISP
9D50	2185EF	0605	LD	HL,0EF85H
9D53	22BAEF	0610	LD	(0EFBAH),HL
9D56	CD0FA0	0615	CALL	ROUT
9D59	1196A3	0620	LD	DE,DAT3
9D5C	01E900	0625	LD	BC,0E9H
9D5F	CD3C20	0630	CALL	203CH
9D62	CDBD9E	0635	CALL	UP2
9D65	3A00FF	0640	LD	A,(MEM)
9D68	D7	0645	RST	0010H
9D69	CDB59E	0650	CALL	GET-K
9D6C	3A00FF	0655	LD	A,(MEM)
9D6F	FE4E	0660	CP	4EH
9D71	2820	0665	JR	Z,NEXT1
9D73	FE43	0670	CP	43H
9D75	CA47A1	0675	JP	Z,MESA
9D78	FE4D	0680	CP	4DH
9D7A	CADD9C	0685	JP	Z,MENU
9D7D	CDC69E	0690	CALL	MESS
9D80	CDB010	0695	AGA	CALL 10B0H
9D83	FE0D	0700	CP	0DH
9D85	CA459D	0705	JP	Z,BRI
9D88	FE65	0710	CP	65H
9D8A	CAEC9E	0715	JP	Z,DOWN1
9D8D	CD0FA0	0720	CALL	ROUT
9D90	C3809D	0725	JP	AGA
		0730	*****	*****
		0735	ROUT	TO-PRINT-PAGE-2
		0740		OF-BRI/CONTROLS
9D93	0615	0745	NEXT1	LD B,15H
9D95	CD440E	0750	CALL	0E44H
9D98	21ADF9	0755	LD	HL,0F9ADH
9D9B	CDE49E	0760	CALL	DISP
9D9E	2194EF	0765	LD	HL,0EF94H
9DA1	22BAEF	0770	LD	(0EFBAH),HL
9DA4	CD0FA0	0775	CALL	ROUT
9DA7	117FA4	0780	LD	DE,DAT4
9DAA	01AB00	0785	LD	BC,0ABH
9DAD	CD3C20	0790	CALL	203CH
9DB0	CDBD9E	0795	CALL	UP2
9DB3	3A00FF	0800	LD	A,(MEM)
9DB6	D7	0805	RST	0010H
9DB7	CDB59E	0810	CALL	GET-K
9DBA	3A00FF	0815	LD	A,(MEM)
9DBD	FE50	0820	CP	50H
9DBF	CA459D	0825	JP	Z,BRI
9DC2	FE43	0830	CP	43H
9DC4	CA47A1	0835	JP	Z,MESA
9DC7	FE4D	0840	CP	4DH
9DC9	CADD9C	0845	JP	Z,MENU
9DCC	CDC69E	0850	CALL	MESS
9DCF	CDB010	0855	AGA1	CALL 10B0H
9DD2	FE0D	0860	CP	0DH
9DD4	CA939D	0865	JP	Z,NEXT1
9DD7	FE65	0870	CP	65H
9DD9	CAEC9E	0875	JP	Z,DOWN1
9DDC	CD0FA0	0880	CALL	ROUT
9DDF	C3CF9D	0885	JP	AGA1
		0890	***	*****
		0895	ALRM	DISP-ROUTINE

	0900 ;*	PAGE-1-OF-2
9DE2 0618	0905 ALARM LD	B, 18H
9DE4 CD440E	0910 CALL	0E44H
9DE7 2133FB	0915 LD	HL, 0FB33H
9DEA CDE49E	0920 CALL	DISP
9DED 21A5EF	0925 LD	HL, 0EFA5H
9DF0 22BAEF	0930 LD	(0EFBAH), HL
9DF3 CDB4A0	0935 CALL	ARMS
9DF6 112AA5	0940 LD	DE, DAT5
9DF9 019400	0945 LD	BC, 94H
9DFC CD3C20	0950 CALL	203CH
9DFF CDBD9E	0955 CALL	UP2
9E02 3A00FF	0960 LD	A, (MEM)
9E05 D7	0965 RST	0010H
9E06 CDB59E	0970 CALL	GET-K
9E09 3A00FF	0975 LD	A, (MEM)
9E0C FE4D	0980 CP	4DH
9E0E CADD9C	0985 JP	Z, MENU
9E11 FE4E	0990 CP	4EH
9E13 CA2C9E	0995 JP	Z, ALAR1
9E16 CDC69E	1000 CALL	MESS
9E19 CDB010	1005 AGA2 CALL	10B0H
9E1C FE0D	1010 CP	0DH
9E1E CAE29D	1015 JP	Z, ALARM
9E21 FE65	1020 CP	65H
9E23 CAEC9E	1025 JP	Z, DOWN1
9E26 CDB4A0	1030 CALL	ARMS
9E29 C3199E	1035 JP	AGA2
	1040 ;****	**** *****
	1045 ;*	ALRM DISP-ROUTINE
	1050 ;*	PAGE-2-OF-2
9E2C 0615	1055 ALAR1 LD	B, 15H
9E2E CD440E	1060 CALL	0E44H
9E31 2138FC	1065 LD	HL, 0FC38H
9E34 CDE49E	1070 CALL	DISP
9E37 21AFEF	1075 LD	HL, 0EF AFH
9E3A 22BAEF	1080 LD	(0EFBAH), HL
9E3D CDB4A0	1085 CALL	ARMS
9E40 11BEA5	1090 LD	DE, DAT6
9E43 017D00	1095 LD	BC, 7DH
9E46 CD3C20	1100 CALL	203CH
9E49 CDBD9E	1105 CALL	UP2
9E4C 3A00FF	1110 LD	A, (MEM)
9E4F D7	1115 RST	0010H
9E50 CDB59E	1120 CALL	GET-K
9E53 3A00FF	1125 LD	A, (MEM)
9E56 FE50	1130 CP	50H
9E58 CAE29D	1135 JP	Z, ALARM
9E5B FE4D	1140 CP	4DH
9E5D CADD9C	1145 JP	Z, MENU
9E60 CDC69E	1150 CALL	MESS
9E63 CDB010	1155 AGA3 CALL	10B0H
9E66 FE0D	1160 CP	0DH
9E68 CA2C9E	1165 JP	Z, ALAR1
9E6B FE65	1170 CP	65H
9E6D CAEC9E	1175 JP	Z, DOWN1
9E70 CDB4A0	1180 CALL	ARMS
9E73 C3639E	1185 JP	AGA3
	1190 ;****	**** *****
	1195 ;*	ANAL -DISP-ROUTINE

	1200	;	*	8-ANALOGUES.
9E76 0618	1205	ANAL	LD	B, 18H
9E78 CD440E	1210		CALL	0E44H
9E7B 213DFD	1215		LD	HL, 0FD3DH
9E7E CDE49E	1220		CALL	DISP
9E81 CDFC9E	1225		CALL	ANSW
9E84 113BA6	1230		LD	DE, DAT7
9E87 018F00	1235		LD	BC, 8FH
9E8A CD3C20	1240		CALL	203CH
9E8D CDBD9E	1245		CALL	UP2
9E90 3A00FF	1250		LD	A, (MEM)
9E93 D7	1255		RST	0010H
9E94 CDB59E	1260		CALL	GET-K
9E97 3A00FF	1265		LD	A, (MEM)
9E9A FE4D	1270		CP	4DH
9E9C CADD9C	1275		JP	Z, MENU
9E9F CDC69E	1280		CALL	MESS
9EA2 CDB010	1285	AGA4	CALL	10B0H
9EA5 FE0D	1290		CP	0DH
9EA7 CA769E	1295		JP	Z, ANAL
9EAA FE65	1300		CP	65H
9EAC CAEC9E	1305		JP	Z, DOWN1
9EAF CDFC9E	1310		CALL	ANSW
9EB2 C3A29E	1315		JP	AGA4
	1320	;	****	*****
9EB5 CDB010	1325	GET-K	CALL	10B0H
9EB8 FE0D	1330		CP	0DH
9EBA 20F9	1335		JR	NZ, GET-K
9EBC C9	1340		RET	
	1345	;	****	*****
	1350	;	*INP	KEY ROUTINE.
9EBD CDB010	1355	UP2	CALL	10B0H
9EC0 30FB	1360		JR	NC, UP2
9EC2 3200FF	1365		LD	(MEM), A
9EC5 C9	1370		RET	
	1375	;	****	*****
	1380	;	*	ROUT CLEAR-5-LINES.
	1385	;	*	DISP-ERR-MESS.
9EC6 0605	1390	MESS	LD	B, 5H
9EC8 CD440E	1395		CALL	0E44H
9ECB 1145A3	1400		LD	DE, DAT2
9ECE 015100	1405		LD	BC, 51H
9ED1 CD3C20	1410		CALL	203CH
9ED4 C9	1415		RET	
	1420	;	****	*****
	1425	;	*	ROUT CLEAR-5-LINES.
	1430	;	*	DISP E/MESS-NO-FLASH
9ED5 0605	1435	MESS1	LD	B, 05H
9ED7 CD440E	1440		CALL	0E44H
9EDA 113CA7	1445		LD	DE, DAT10
9EDD 014000	1450		LD	BC, 40H
9EE0 CD3C20	1455		CALL	203CH
9EE3 C9	1460		RET	
	1465	;	****	*****
	1470	;	*	DISP ROUTINE-CHECKS
	1475	;	*	FOR-FFH-TO-END
9EE4 7E	1480	DISP	LD	A, (HL)
9EE5 23	1485		INC	HL
9EE6 FEFF	1490		CP	0FFH
9EE8 C8	1495		RET	Z

9EE9 D7	1500	RST	0010H
9EEA 18F8	1505	JR	DISP
	1510	;**** *****	
	1515	;* ROUT -TO-DISPLAY-END	
	1520	;* MESSAGE.	
9EEC 0618	1525	DOWN1 LD	B,18H
9EEE CD440E	1530	CALL	0E44H
9EF1 2110F8	1535	LD	HL,0F810H
9EF4 CDE49E	1540	CALL	DISP
9EF7 3E00	1545	LD	A,00H
9EF9 D39B	1550	OUT	(09BH),A
9EFB C9	1555	RET	
	1560	;**** *****	
	1565	;*FLT PONT ROUTINE-VARIABLES-	
	1570	;* -IN- EF10/11-ANS.EF40/41	
9EFC 3E00	1575	ANSW LD	A,00H
9EFE 3280EF	1580	LD	(0EF80H),A
9F01 DD2110EF	1585	LD	IX,0EF10H
9F05 DD4E00	1590	FPONT LD	C,(IX+00H)
9F08 DD4601	1595	LD	B,(IX+01H)
9F0B CD2B2D	1600	CALL	2D2BH
9F0E DD4E10	1605	LD	C,(IX+10H)
9F11 DD4611	1610	LD	B,(IX+11H)
9F14 CD2B2D	1615	CALL	2D2BH
9F17 EF	1620	RST	28H
9F18 04	1625	DEFB	04H
9F19 38	1630	DEFB	38H
9F1A DD4E20	1635	LD	C,(IX+20H)
9F1D DD4621	1640	LD	B,(IX+21H)
9F20 CD2B2D	1645	CALL	2D2BH
9F23 EF	1650	RST	28H
9F24 05	1655	DEFB	05H
9F25 27	1660	DEFB	27H
9F26 38	1665	DEFB	38H
9F27 CDA22D	1670	CALL	2DA2H
9F2A DD7130	1675	LD	(IX+30H),C
9F2D DD7031	1680	LD	(IX+31H),B
9F30 3A80EF	1685	LD	A,(0EF80H)
9F33 3C	1690	INC	A
9F34 3280EF	1695	LD	(0EF80H),A
9F37 FE08	1700	CP	08H
9F39 CA439F	1705	JP	Z,CONV
9F3C DD23	1710	INC	IX
9F3E DD23	1715	INC	IX
9F40 C3059F	1720	JP	FPONT
	1725	;**** *****	
	1730	;*RUT -TO- CONV-HEX-VAR-2BYTE	
	1735	;* EF40-41,TO,EF5D-60	
9F43 DD215DEF	1740	CONV LD	IX,0EF5DH
9F47 2140EF	1745	LD	HL,0EF40H
9F4A FDE5	1750	PUSH	IY
9F4C 3E00	1755	LD	A,00H
9F4E 3284EF	1760	LD	(0EF84H),A
9F51 FD21BF EF	1765	LD	IY,0EFBFH
9F55 FD360000	1770	SUB2 LD	(IY+00H),00H
9F59 3E00	1775	LD	A,00H
9F5B 3283EF	1780	LD	(0EF83H),A
9F5E 01E803	1785	LD	BC,03E8H
9F61 5E	1790	LD	E,(HL)
9F62 23	1795	INC	HL

9F63	56	1800	LD	D, (HL)
9F64	DD360000	1805	SUB1	LD (IX+00H), 00H
9F68	37	1810	SUB3	SCF
9F69	3F	1815		CCF
9F6A	EB	1820	EX	DE, HL
9F6B	ED42	1825	SBC	HL, BC
9F6D	DD3400	1830	INC	(IX+00H)
9F70	EB	1835	EX	DE, HL
9F71	30F5	1840	JR	NC, SUB3
9F73	3F	1845		CCF
9F74	EB	1850	EX	DE, HL
9F75	ED4A	1855	ADC	HL, BC
9F77	EB	1860	EX	DE, HL
9F78	3A83EF	1865	LD	A, (0EF83H)
9F7B	3C	1870	INC	A
9F7C	3283EF	1875	LD	(0EF83H), A
9F7F	DD3500	1880	DEC	(IX+00H)
9F82	016400	1885	LD	BC, 0064H
9F85	DD23	1890	INC	IX
9F87	3ABFEF	1895	LD	A, (0EFBFH)
9F8A	FE01	1900	CP	01H
9F8C	2807	1905	JR	Z, SUB4
9F8E	3A83EF	1910	LD	A, (0EF83H)
9F91	FE02	1915	CP	02H
9F93	20CF	1920	JR	NZ, SUB1
9F95	FD360001	1925	SUB4	LD (IY+00H), 01H
9F99	010A00	1930	LD	BC, 000AH
9F9C	3A83EF	1935	LD	A, (0EF83H)
9F9F	FE03	1940	CP	03H
9FA1	20C1	1945	JR	NZ, SUB1
9FA3	DD7300	1950	LD	(IX+00H), E
9FA6	DD23	1955	INC	IX
9FA8	23	1960	INC	HL
9FA9	3A84EF	1965	LD	A, (0EF84H)
9FAC	3C	1970	INC	A
9FAD	3284EF	1975	LD	(0EF84H), A
9FB0	FE08	1980	CP	08H
9FB2	20A1	1985	JR	NZ, SUB2
9FB4	FDE1	1990	POP	IY
9FB6	1E00	1995	LD	E, 00H
9FB8	215DEF	2000	LD	HL, 0EF5DH
		2005	****	**** *****
		2010	*ASC	CONV ROUT-EF5D/60-TO-ASC
		2015	;	* CHARS-FOR-DISPLAY
9FBB	7E	2020	ASCII	LD A, (HL)
9FBC	C630	2025		ADD 30H
9FBE	77	2030		LD (HL), A
9FBF	23	2035		INC HL
9FC0	1C	2040		INC E
9FC1	7B	2045		LD A, E
9FC2	FE20	2050		CP 20H
9FC4	20F5	2055		JR NZ, ASCII
		2060	****	**** *****
		2065	*PNT	ROUT TO-DISPLAY-CHARACTS
		2070	;	* NEXT-T0-ANALOGS
9FC6	21F8EE	2075		LD HL, 0EEF8H
9FC9	3E03	2080		LD A, 03H
9FCB	3281EF	2085		LD (0EF81H), A
9FCE	3E00	2090		LD A, 00H
9FD0	3283EF	2095		LD (0EF83H), A

9FD3	DD215DEF	2100	LD	IX,0EF5DH
9FD7	3E16	2105 UPW	LD	A,16H
9FD9	D7	2110	RST	0010H
9FDA	3A81EF	2115	LD	A,(0EF81H)
9FDD	D7	2120	RST	0010H
9FDE	3E1B	2125	LD	A,1BH
9FE0	D7	2130	RST	0010H
9FE1	7E	2135	LD	A,(HL)
9FE2	D7	2140	RST	0010H
9FE3	DD7E00	2145	LD	A,(IX+00H)
9FE6	D7	2150	RST	0010H
9FE7	DD7E01	2155	LD	A,(IX+01H)
9FEA	D7	2160	RST	0010H
9FEB	DD7E02	2165	LD	A,(IX+02H)
9FEE	D7	2170	RST	0010H
9FEF	DD7E03	2175	LD	A,(IX+03H)
9FF2	D7	2180	RST	0010H
9FF3	3A81EF	2185	LD	A,(0EF81H)
9FF6	3C	2190	INC	A
9FF7	3281EF	2195	LD	(0EF81H),A
9FFA	DD23	2200	INC	IX
9FFC	DD23	2205	INC	IX
9FFE	DD23	2210	INC	IX
A000	DD23	2215	INC	IX
A002	23	2220	INC	HL
A003	3A83EF	2225	LD	A,(0EF83H)
A006	3C	2230	INC	A
A007	3283EF	2235	LD	(0EF83H),A
A00A	FE08	2240	CP	08H
A00C	20C9	2245	JR	NZ,UPW
A00E	C9	2250	RET	
		2255	****	*****
		2260	;*BRI	ROUT 10,BITS,INTO,5MEMS
		2265	;*	DENOTES,STATE,BRKS
A00F	3E01	2266	ROUT	LD A,01H
A011	322FF0	2267	LD	(0F02FH),A
A014	1600	2270	LD	D,00H
A016	2185EF	2275	LD	HL,0EF85H
A019	DD2100EF	2280	LD	IX,0EF00H
A01D	1E00	2285	BIT1	LD E,00H
A01F	37	2290	SCF	
A020	3F	2295	CCF	
A021	3600	2300	BIT0	LD (HL),00H
A023	DDCB000E	2305	RRC	(IX+00H)
A027	CB1E	2310	RR	(HL)
A029	DDCB000E	2315	RRC	(IX+00H)
A02D	CB1E	2320	RR	(HL)
A02F	23	2325	INC	HL
A030	1C	2330	INC	E
A031	7B	2335	LD	A,E
A032	FE04	2340	CP	04H
A034	20EB	2345	JR	NZ,BIT0
A036	DD23	2350	INC	IX
A038	3600	2355	LD	(HL),00H
A03A	DDCB000E	2360	RRC	(IX+00H)
A03E	CB1E	2365	RR	(HL)
A040	DDCB000E	2370	RRC	(IX+00H)
A044	CB1E	2375	RR	(HL)
A046	DDCB0006	2380	RLC	(IX+00H)
A04A	DDCB0006	2385	RLC	(IX+00H)

A04E 23	2390	INC	HL
A04F 14	2395	INC	D
A050 DD23	2400	INC	IX
A052 7A	2405	LD	A, D
A053 FE06	2410	CP	06H
A055 20C6	2415	JR	NZ, BIT1
A057 3E00	2416	LD	A, 00H
A059 322FF0	2417	LD	(0F02FH), A
	2420	;**** *****	
	2425	;*BRI ROUT CONVERTS, 2BITS, OF	
	2430	;* DATA, INTO, SYMBOLS	
A05C 2185EF	2435	LD	HL, 0EF85H
A05F 1E00	2440	LD	E, 00H
A061 7E	2445	FUTH5	LD A, (HL)
A062 FE00	2450	CP	00H
A064 280C	2455	JR	Z, FUTH0
A066 FEC0	2460	CP	0C0H
A068 2808	2465	JR	Z, FUTH0
A06A FE80	2470	CP	80H
A06C 2808	2475	JR	Z, FUTH1
A06E FE40	2480	CP	40H
A070 2808	2485	JR	Z, FUTH2
A072 3641	2490	FUTH0	LD (HL), 41H
A074 1806	2495	JR	FUTH4
A076 3643	2500	FUTH1	LD (HL), 43H
A078 1802	2505	JR	FUTH4
A07A 364F	2510	FUTH2	LD (HL), 4FH
A07C 23	2515	FUTH4	INC HL
A07D 1C	2520	INC	E
A07E 7B	2525	LD	A, E
A07F FE1E	2530	CP	1EH
A081 20DE	2535	JR	NZ, FUTH5
	2540	;**** *****	
	2545	;*BRI ROUT PRINTS, A, O, C, CHARS	
	2550	;* ON, SCREEN, IN, PLACE	
A083 DD2ABAEF	2555	LD	IX, (0EFBAH)
A087 3E03	2560	LD	A, 03H
A089 3281EF	2565	LD	(0EF81H), A
A08C 3E00	2570	LD	A, 00H
A08E 3283EF	2575	LD	(0EF83H), A
A091 3E16	2580	FUTH8	LD A, 16H
A093 D7	2585	RST	0010H
A094 3A81EF	2590	LD	A, (0EF81H)
A097 D7	2595	RST	0010H
A098 3E1D	2600	LD	A, 1DH
A09A D7	2605	RST	0010H
A09B DD7E00	2610	LD	A, (IX+00H)
A09E D7	2615	RST	0010H
A09F 3A81EF	2620	LD	A, (0EF81H)
A0A2 3C	2625	INC	A
A0A3 3281EF	2630	LD	(0EF81H), A
A0A6 DD23	2635	INC	IX
A0A8 3A83EF	2640	LD	A, (0EF83H)
A0AB 3C	2645	INC	A
A0AC 3283EF	2650	LD	(0EF83H), A
A0AF FE0F	2655	CP	0FH
A0B1 20DE	2660	JR	NZ, FUTH8
A0B3 C9	2665	RET	
	2670	;**** *****	
	2675	;*ALM ROUT SPLITT, 2BYTE-10BIT	

	2680	;	*	INTO, 10MEM-BYTES.
A0B4 3E01	2681	ARMS	LD	A, 01H
A0B6 322FF0	2682		LD	(0F02FH), A
A0B9 1600	2685		LD	D, 00H
A0BB 21A5EF	2690		LD	HL, 0EFA5H
A0BE DD210CEF	2695		LD	IX, 0EF0CH
A0C2 1E00	2700	BET2	LD	E, 00H
A0C4 37	2705		SCF	
A0C5 3F	2710		CCF	
A0C6 3600	2715	BET0	LD	(HL), 00H
A0C8 DDCB000E	2720		RRC	(IX+00H)
A0CC CB1E	2725		RR	(HL)
A0CE 23	2730		INC	HL
A0CF 1C	2735		INC	E
A0D0 7B	2740		LD	A, E
A0D1 FE08	2745		CP	08H
A0D3 20F1	2750		JR	NZ, BET0
A0D5 DD23	2755		INC	IX
A0D7 3600	2760	BET1	LD	(HL), 00H
A0D9 DDCB000E	2765		RRC	(IX+00H)
A0DD CB1E	2770		RR	(HL)
A0DF 23	2775		INC	HL
A0E0 1C	2780		INC	E
A0E1 7B	2785		LD	A, E
A0E2 FE0A	2790		CP	0AH
A0E4 20F1	2795		JR	NZ, BET1
A0E6 DDCB0006	2800		RLC	(IX+00H)
A0EA DDCB0006	2805		RLC	(IX+00H)
A0EE 14	2810		INC	D
A0EF DD23	2815		INC	IX
A0F1 7A	2820		LD	A, D
A0F2 FE02	2825		CP	02H
A0F4 20CC	2830		JR	NZ, BET2
A0F6 3E00	2831		LD	A, 00H
A0F8 322FF0	2832		LD	(0F02FH), A
	2835	;	****	*****
	2840	;	*ALM	ROUT CONV, MEM, CONTENTS,
	2845	;	*	INTO, F-ALSE, T-RUE
A0FB 21A5EF	2850		LD	HL, 0EFA5H
A0FE 1E00	2855		LD	E, 00H
A100 7E	2860	GIU4	LD	A, (HL)
A101 FE00	2865		CP	00H
A103 2804	2870		JR	Z, GIU0
A105 FE80	2875		CP	80H
A107 2804	2880		JR	Z, GIU1
A109 3646	2885	GIU0	LD	(HL), 46H
A10B 1802	2890		JR	GIU3
A10D 3654	2895	GIU1	LD	(HL), 54H
A10F 23	2900	GIU3	INC	HL
A110 1C	2905		INC	E
A111 7B	2910		LD	A, E
A112 FE14	2915		CP	14H
A114 20EA	2920		JR	NZ, GIU4
	2925	;	****	*****
	2930	;	*ALM	PRNT ROUT, TO, DISPLAY,
	2935	;	*	CONDITIN, OF, ALARMS
A116 DD2ABAEF	2940		LD	IX, (0EFBAH)
A11A 3E02	2945		LD	A, 02H
A11C 3281EF	2950		LD	(0EF81H), A
A11F 3E00	2955		LD	A, 00H

A121	3283EF	2960	LD	(0EF83H), A
A124	3E16	2965	GIUS	LD A, 16H
A126	D7	2970	RST	0010H
A127	3A81EF	2975	LD	A, (0EF81H)
A12A	D7	2980	RST	0010H
A12B	3E1D	2985	LD	A, 1DH
A12D	D7	2990	RST	0010H
A12E	DD7E00	2995	LD	A, (IX+00H)
A131	D7	3000	RST	0010H
A132	3A81EF	3005	LD	A, (0EF81H)
A135	3C	3010	INC	A
A136	3281EF	3015	LD	(0EF81H), A
A139	DD23	3020	INC	IX
A13B	3A83EF	3025	LD	A, (0EF83H)
A13E	3C	3030	INC	A
A13F	3283EF	3035	LD	(0EF83H), A
A142	FE0A	3040	CP	0AH
A144	20DE	3045	JR	NZ, GIUS
A146	C9	3050	RET	
		3055	*****	*****
		3060	*CON	TROL ROUTINE.PROMPTS-&
		3065	*INP	UT- CONTROL/STATUS-O/C.
A147	0605	3070	MESA	LD B, 05H
A149	CD440E	3075	CALL	0E44H
A14C	11CAA6	3080	LD	DE, DAT8
A14F	016C00	3085	LD	BC, 6CH
A152	CD3C20	3090	CALL	203CH
A155	2108F0	3095	LD	HL, 0F008H
A158	DD210EF0	3100	LD	IX, 0F00EH
A15C	3E00	3105	LD	A, 00H
A15E	DD7700	3110	LD	(IX+00H), A
A161	CDBD9E	3115	COTR	CALL UP2
		3120	*****	*****
		3125	*CHE	CK- FOR-SECOND-KEY-DEP
		3130	;	* RESSION
A164	DD7E00	3135	LD	A, (IX+00H)
A167	FE02	3140	CP	02H
A169	2819	3145	JR	Z, COTR0
A16B	3A00FF	3150	LD	A, (MEM)
A16E	FE58	3155	CP	58H
A170	CA459D	3160	JP	Z, BRI
A173	FE30	3165	CP	30H
A175	DA61A1	3170	JP	C, COTR
A178	FE3A	3175	CP	3AH
A17A	D261A1	3180	JP	NC, COTR
A17D	D7	3185	RST	0010H
A17E	CDB3A1	3190	CALL	CURSO
A181	C398A1	3195	JP	COTR3
		3200	*****	*****
		3205	*CHE	CK- FOR-3RD-KEY-ENTRY-
		3210	;	* C, O, X, OR-OTHER-KEY
A184	3A00FF	3215	COTR0	LD A, (MEM)
A187	FE43	3220	CP	43H
A189	280C	3225	JR	Z, COTR2
A18B	FE4F	3230	CP	4FH
A18D	2808	3235	JR	Z, COTR2
A18F	FE58	3240	CP	58H
A191	CA459D	3245	JP	Z, BRI
A194	C361A1	3250	JP	COTR
A197	D7	3255	COTR2	RST 0010H

A198 3A00FF	3260	COTR3	LD	A, (MEM)
A19B 77	3265		LD	(HL), A
A19C 23	3270		INC	HL
A19D DD3400	3275		INC	(IX+00H)
A1A0 DD7E00	3280		LD	A, (IX+00H)
A1A3 FE03	3285		CP	03H
A1A5 20BA	3290		JR	NZ, COTR
	3295	;**** **** *****		
	3300	;*FET CH- ENTER-KEY-DEPRESSN		
A1A7 CDB010	3305	COTR1	CALL	10B0H
A1AA 30FB	3310		JR	NC, COTR1
A1AC FE0D	3315		CP	0DH
A1AE CABDA1	3320		JP	Z, CHANG
A1B1 18F4	3325		JR	COTR1
	3330	;**** **** *****		
	3335	;*ROU TIME TG-MOVE-CURSOR-RIG		
	3340	;* -HT, ONE-POSITION		
A1B3 1136A7	3345	CURSO	LD	DE, DAT9
A1B6 010600	3350		LD	BC, 06H
A1B9 CD3C20	3355		CALL	203CH
A1BC C9	3360		RET	
	3365	;**** **** *****		
	3370	;*CON VERS ION-KEY-ENTRY-ROUT		
	3375	;*INE FROM ASCII-TO-BINARY..		
A1BD DD210DF0	3380	CHANG	LD	IX, 0F00DH
A1C1 2108F0	3385		LD	HL, 0F008H
A1C4 7E	3390		LD	A, (HL)
A1C5 E60F	3395		AND	0FH
A1C7 320BF0	3400		LD	(0F00BH), A
	3405	;**** **** *****		
	3410	;*CHE CK- TENS-VALUE-FOR-0, 1		
	3415	;* 2, 3. (1ST-ENTRY).		
A1CA FE00	3420		CP	00H
A1CC 280F	3425		JR	Z, MENO0
A1CE FE01	3430		CP	01H
A1D0 2813	3435		JR	Z, MENO1
A1D2 FE02	3440		CP	02H
A1D4 2817	3445		JR	Z, MENO2
A1D6 FE03	3450		CP	03H
A1D8 281B	3455		JR	Z, MENO3
A1DA C347A1	3460		JP	MESA
	3465	;**** **** *****		
	3470	;*STO RE- SUBTRACTION-VALUE-		
	3475	;* OR CORRECTION-FACTOR.		
A1DD 3E00	3480	MENO0	LD	A, 00H
A1DF DD7700	3485		LD	(IX+00H), A
A1E2 C3FAA1	3490		JP	MENO4
A1E5 3E06	3495	MENO1	LD	A, 06H
A1E7 DD7700	3500		LD	(IX+00H), A
A1EA C3FAA1	3505		JP	MENO4
A1ED 3E0C	3510	MENO2	LD	A, 0CH
A1EF DD7700	3515		LD	(IX+00H), A
A1F2 C3FAA1	3520		JP	MENO4
A1F5 3E12	3525	MENO3	LD	A, 12H
A1F7 DD7700	3530		LD	(IX+00H), A
A1FA 3A0BF0	3535	MENO4	LD	A, (0F00BH)
	3540	;**** **** *****		
	3545	;*ADJ UST- 1ST-KEY-ENTRY-MOVE		
	3550	;*LEF T- ONE-PLACE.		
A1FD CB27	3555	SLA	A	

A1FF CB27	3560	SLA	A
A201 CB27	3565	SLA	A
A203 CB27	3570	SLA	A
A205 320BF0	3575	LD	(0F00BH), A
A208 23	3580	INC	HL
A209 7E	3585	LD	A, (HL)
A20A E60F	3590	AND	0FH
A20C 23	3595	INC	HL
A20D 23	3600	INC	HL
A20E B6	3605	OR	(HL)
A20F 77	3610	LD	(HL), A
	3615	;**** **** *****	
	3620	;*CHE CK- IF-KEY-ENTRY-IS-	
	3625	;*LAR GER- 31H-OR-SMALLER-01H	
A210 FE31	3630	CP	31H
A212 D247A1	3635	JP	NC, MESA
A215 FE01	3640	CP	01H
A217 DA47A1	3645	JP	C, MESA
A21A DD9600	3650	SUB	(IX+00H)
A21D CB27	3655	SLA	A
A21F 77	3660	LD	(HL), A
	3665	;**** **** *****	
	3670	;*CHE CK- IF-IT-IS-A-OPEN-OR	
	3675	;* CLOSE-COMMAND.	
A220 3A0AF0	3680	LD	A, (0F00AH)
A223 FE43	3685	CP	43H
A225 2804	3690	JR	Z, MEN05
A227 35	3695	DEC	(HL)
A228 C32DA2	3700	JP	MEN06
A22B 35	3705	MEN05 DEC	(HL)
A22C 35	3710	DEC	(HL)
	3715	;**** **** *****	
	3720	;*INI TIAL IZE-MEMORY-CONTENT	
	3725	;* WITH -CONTROL-WORDS.	
A22D 3E59	3730	MEN06 LD	A, 59H
A22F 320FF0	3735	LD	(0F00FH), A
A232 3E0F	3740	LD	A, 0FH
A234 3210F0	3745	LD	(0F010H), A
A237 3EA4	3750	LD	A, 0A4H
A239 3211F0	3755	LD	(0F011H), A
A23C 3E67	3760	LD	A, 67H
A23E 3212F0	3765	LD	(0F012H), A
A241 3E63	3770	LD	A, 63H
A243 3213F0	3775	LD	(0F013H), A
A246 3E1C	3780	LD	A, 1CH
A248 3214F0	3785	LD	(0F014H), A
A24B 3E00	3790	LD	A, 00H
A24D 3215F0	3795	LD	(0F015H), A
A250 3216F0	3800	LD	(0F016H), A
A253 3219F0	3805	LD	(0F019H), A
A256 321AF0	3810	LD	(0F01AH), A
A259 320CF0	3815	LD	(0F00CH), A
A25C 3E9C	3820	LD	A, 9CH
A25E 3217F0	3825	LD	(0F017H), A
A261 3E07	3830	LD	A, 07H
A263 3218F0	3835	LD	(0F018H), A
A266 3E59	3840	LD	A, 59H
A268 321BF0	3845	LD	(0F01BH), A
A26B 3E0F	3850	LD	A, 0FH
A26D 321CF0	3851	LD	(0F01CH), A

A270	3E01	3855	LD	A,01H	
A272	3200F0	3860	LD	(0F000H),A	
		3865	;**** *****		
		3870	;*CHE CK- TO-WHICH-PAGE-WE-		
		3875	;*ARE JUMP ING-TO.1ST-OR-2ND.		
A275	7E	3880	LD	A,(HL)	
A276	FE1E	3885	CP	1EH	
A278	D2939D	3890	JP	NC,NEXT1	
A27B	C3459D	3895	JP	BRI	
		3900	;**** *****		
		3905	;*BEG -OF- FIXED,DATA,BORDER		
		3910	;* AND,QUESTIONS		
A27E	16	3915	STAT	DEFB	16H
A27F	03	3920		DEFB	03H
A280	02	3925		DEFB	02H
A281	14	3930		DEFB	14H
A282	01	3935		DEFB	01H
A283		3940	DEFM	"STATION NAME."	
A290	14	3945		DEFB	14H
A291	00	3950		DEFB	00H
A292	16	3955	DAT	DEFB	16H
A293	06	3960		DEFB	06H
A294	00	3965		DEFB	00H
A295		3970	DEFM	"	*MENU*
A2B5		3975	DEFM	"	(1)BRI/CONT.
A2D5		3980	DEFM	"	(2)ALARMS.
A2F5		3985	DEFM	"	(3)ANALOGUES.
A315		3990	DEFM	"	(4)EXIT."
A324	16	3995	DAT1	DEFB	16H
A325	15	4000		DEFB	15H
A326	00	4005		DEFB	00H
A327		4010	DEFM	"ENTER SELECTED NUMBER."	
A33F	12	4015		DEFB	12H
A340	01	4020		DEFB	01H
A341	3E	4025		DEFB	3EH
A342	12	4030		DEFB	12H
A343	00	4035		DEFB	00H
A344	08	4040		DEFB	08H
FF00		4045	MEM	EQU	0FF00H
A345	16	4050	DAT2	DEFB	16H
A346	13	4055		DEFB	13H
A347	00	4060		DEFB	00H
A348	14	4065		DEFB	14H
A349	01	4070		DEFB	01H
A34A	12	4075		DEFB	12H
A34B	01	4080		DEFB	01H
A34C		4085	DEFM	"UPDATING"	
A354	12	4090		DEFB	12H
A355	00	4095		DEFB	00H
A356	14	4100		DEFB	14H
A357	00	4105		DEFB	00H
A358	0D	4110		DEFB	0DH
A359		4115	DEFM	"WRONG ENTRY TO TRY AGAIN PRESS (ENTER) OR (E)	
A387		4120	DEFM	" FOR EXIT."	
A391	12	4125		DEFB	12H
A392	01	4130		DEFB	01H
A393	3E	4135		DEFB	3EH
A394	12	4140		DEFB	12H
A395	00	4145		DEFB	00H
A396	16	4150	DAT3	DEFB	16H

A397 00	4155	DEFB 00H	
A398 03	4160	DEFB 03H	
A399	4165	DEFM "(DISPLAY) BRI./(CONTROLS)."	
A3B4 0D	4170	DEFB 0DH	
A3B5 0D	4175	DEFB 0DH	
A3B6	4180	DEFM "	BREAKERS.....STATE"
A3D6 0D	4185	DEFB 0DH	
A3D7	4190	DEFM "(01)"	
A3DB 0D	4195	DEFB 0DH	
A3DC	4200	DEFM "(02)"	
A3E0 0D	4205	DEFB 0DH	
A3E1	4210	DEFM "(03)"	
A3E5 0D	4215	DEFB 0DH	
A3E6	4220	DEFM "(04)"	
A3EA 0D	4225	DEFB 0DH	
A3EB	4230	DEFM "(05)"	
A3EF 0D	4235	DEFB 0DH	
A3F0	4240	DEFM "(06)"	
A3F4 0D	4245	DEFB 0DH	
A3F5	4250	DEFM "(07)"	
A3F9 0D	4255	DEFB 0DH	
A3FA	4260	DEFM "(08)"	
A3FE 0D	4265	DEFB 0DH	
A3FF	4270	DEFM "(09)"	
A403 0D	4275	DEFB 0DH	
A404	4280	DEFM "(10)"	
A408 0D	4285	DEFB 0DH	
A409	4290	DEFM "(11)"	
A40D 0D	4295	DEFB 0DH	
A40E	4300	DEFM "(12)"	
A412 0D	4305	DEFB 0DH	
A413	4310	DEFM "(13)"	
A417 0D	4315	DEFB 0DH	
A418	4320	DEFM "(14)"	
A41C 0D	4325	DEFB 0DH	
A41D	4330	DEFM "(15)"	
A421 0D	4335	DEFB 0DH	
A422 0D	4340	DEFB 0DH	
A423	4345	DEFM "TO DISP.NEXT PAGE PRESS (N)KEY,"	
A442 0D	4350	DEFB 0DH	
A443	4355	DEFM "FOR CONTRLS (C)KEY,MENU (M)KEY."	
A462 0D	4360	DEFB 0DH	
A463	4365	DEFM "THEN PRESS (ENTER)KEY."	
A479 12	4370	DEFB 12H	
A47A 01	4375	DEFB 01H	
A47B 3E	4380	DEFB 3EH	
A47C 12	4385	DEFB 12H	
A47D 00	4390	DEFB 00	
A47E 08	4395	DEFB 08H	
A47F 16	4400	DEFB 16H	DAT4
A480 03	4405	DEFB 03H	
A481 00	4410	DEFB 00H	
A482	4415	DEFM "(16)"	
A486 0D	4420	DEFB 0DH	
A487	4425	DEFM "(17)"	
A48B 0D	4430	DEFB 0DH	
A48C	4435	DEFM "(18)"	
A490 0D	4440	DEFB 0DH	
A491	4445	DEFM "(19)"	
A495 0D	4450	DEFB 0DH	

A496	4455	DEFM "(20)"
A49A 0D	4460	DEFB 0DH
A49B	4465	DEFM "(21)"
A49F 0D	4470	DEFB 0DH
A4A0	4475	DEFM "(22)"
A4A4 0D	4480	DEFB 0DH
A4A5	4485	DEFM "(23)"
A4A9 0D	4490	DEFB 0DH
A4AA	4495	DEFM "(24)"
A4AE 0D	4500	DEFB 0DH
A4AF	4505	DEFM "(25)"
A4B3 0D	4510	DEFB 0DH
A4B4	4515	DEFM "(26)"
A4B8 0D	4520	DEFB 0DH
A4B9	4525	DEFM "(27)"
A4BD 0D	4530	DEFB 0DH
A4BE	4535	DEFM "(28)"
A4C2 0D	4540	DEFB 0DH
A4C3	4545	DEFM "(29)"
A4C7 0D	4550	DEFB 0DH
A4C8	4555	DEFM "(30)"
A4CC 0D	4560	DEFB 0DH
A4CD 0D	4565	DEFB 0DH
A4CE	4570	DEFM "TO DISP.PREV.PAGE PRESS (P)KEY,"
A4ED 0D	4575	DEFB 0DH
A4EE	4580	DEFM "FOR CONTRLS (C)KEY,MENU (M)KEY."
A50D 0D	4585	DEFB 0DH
A50E	4590	DEFM "THEN PRESS (ENTER)KEY."
A524 12	4595	DEFB 12H
A525 01	4600	DEFB 01H
A526 3E	4605	DEFB 3EH
A527 12	4610	DEFB 12H
A528 00	4615	DEFB 00
A529 08	4620	DEFB 08H
A52A 16	4625 DAT5	DEFB 16H
A52B 00	4630	DEFB 00H
A52C 08	4635	DEFB 08H
A52D	4640	DEFM "ALARM-LISTING. STATE"
A544 0D	4645	DEFB 0DH
A545 0D	4650	DEFB 0DH
A546	4655	DEFM "(01)"
A54A 0D	4660	DEFB 0DH
A54B	4665	DEFM "(02)"
A54F 0D	4670	DEFB 0DH
A550	4675	DEFM "(03)"
A554 0D	4680	DEFB 0DH
A555	4685	DEFM "(04)"
A559 0D	4690	DEFB 0DH
A55A	4695	DEFM "(05)"
A55E 0D	4700	DEFB 0DH
A55F	4705	DEFM "(06)"
A563 0D	4710	DEFB 0DH
A564	4715	DEFM "(07)"
A568 0D	4720	DEFB 0DH
A569	4725	DEFM "(08)"
A56D 0D	4730	DEFB 0DH
A56E	4735	DEFM "(09)"
A572 0D	4740	DEFB 0DH
A573	4745	DEFM "(10)"
A577 0D	4750	DEFB 0DH

A578 16	4755	DEFB 16H	
A579 14	4760	DEFB 14H	
A57A 00	4765	DEFB 00H	
A57B	4770	DEFM "FOR NEXT PAGE PRESS (N)KEY.OR"	
A578 0D	4775	DEFB 0DH	
A599	4780	DEFM "(M)KEY FOR MENU,THEN(ENTER)KEY."	
A5B8 12	4785	DEFB 12H	
A5B9 01	4790	DEFB 01H	
A5BA 3E	4795	DEFB 3EH	
A5BB 12	4800	DEFB 12H	
A5BC 00	4805	DEFB 00H	
A5BD 08	4810	DEFB 08H	
A5BE 16	4815 DAT6	DEFB 16H	
A5BF 02	4820	DEFB 02H	
A5C0 00	4825	DEFB 00H	
A5C1	4830	DEFM "(11)"	
A5C5 0D	4835	DEFB 0DH	
A5C6	4840	DEFM "(12)"	
A5CA 0D	4845	DEFB 0DH	
A5CB	4850	DEFM "(13)"	
A5CF 0D	4855	DEFB 0DH	
A5D0	4860	DEFM "(14)"	
A5D4 0D	4865	DEFB 0DH	
A5D5	4870	DEFM "(15)"	
A5D9 0D	4875	DEFB 0DH	
A5DA	4880	DEFM "(16)"	
A5DE 0D	4885	DEFB 0DH	
A5DF	4890	DEFM "(17)"	
A5E3 0D	4895	DEFB 0DH	
A5E4	4900	DEFM "(18)"	
A5E8 0D	4905	DEFB 0DH	
A5E9	4910	DEFM "(19)"	
A5ED 0D	4915	DEFB 0DH	
A5EE	4920	DEFM "(20)"	
A5F2 0D	4925	DEFB 0DH	
A5F3 16	4930	DEFB 16H	
A5F4 14	4935	DEFB 14H	
A5F5 00	4940	DEFB 00H	
A5F6	4945	DEFM "FOR PREVIOUS PAGE PRESS (P)KEY."	
A615 0D	4950	DEFB 0DH	
A616	4955	DEFM "FOR MENU (M)KEY.THEN(ENTER)KEY."	
A635 12	4960	DEFB 12H	
A636 01	4965	DEFB 01H	
A637 3E	4970	DEFB 3EH	
A638 12	4975	DEFB 12H	
A639 00	4980	DEFB 00H	
A63A 08	4985	DEFB 08H	
A63B 16	4990 DAT7	DEFB 16H	
A63C 00	4995	DEFB 00H	
A63D 08	5000	DEFB 08H	
A63E	5005	DEFM "ANALOGUES-LISTING"	
A64F 0D	5010	DEFB 0DH	
A650 16	5015	DEFB 16H	
A651 02	5020	DEFB 02H	
A652 09	5025	DEFB 09H	
A653	5030	DEFM "NAME. VALUE."	
A66A 0D	5035	DEFB 0DH	
A66B	5040	DEFM "(1)"	
A66E 0D	5045	DEFB 0DH	
A66F	5050	DEFM "(2)"	

A672 0D	5055	DEFB 0DH
A673	5060	DEFM "(3)"
A676 0D	5065	DEFB 0DH
A677	5070	DEFM "(4)"
A67A 0D	5075	DEFB 0DH
A67B	5080	DEFM "(5)"
A67E 0D	5085	DEFB 0DH
A67F	5090	DEFM "(6)"
A682 0D	5095	DEFB 0DH
A683	5100	DEFM "(7)"
A686 0D	5105	DEFB 0DH
A687	5110	DEFM "(8)"
A68A 0D	5115	DEFB 0DH
A68B 16	5120	DEFB 16H
A68C 14	5125	DEFB 14H
A68D 00	5130	DEFB 00H
A68E	5135	DEFM "TO RETURN TO MENU PRESS (M)KEY."
A6AD 0D	5140	DEFB 0DH
A6AE	5145	DEFM "THEN PRESS (ENTER)KEY."
A6C4 12	5150	DEFB 12H
A6C5 01	5155	DEFB 01H
A6C6 3E	5160	DEFB 3EH
A6C7 12	5165	DEFB 12H
A6C8 00	5170	DEFB 00H
A6C9 08	5175	DEFB 08H
A6CA 16	5180 DAT8	DEFB 16H
A6CB 13	5185	DEFB 13H
A6CC 00	5190	DEFB 00H
A6CD	5195	DEFM "FOR CONTROLS ENTER SELECTED NUM"
A6EC 0D	5200	DEFB 0DH
A6ED	5205	DEFM "2DIGIT+OPEN/CLOSE O/C, THEN PRES"
A70C 0D	5210	DEFB 0DH
A70D	5215	DEFM "ENTER-KEY.ABORT PRESS XKEY()"
A72C 08	5220	DEFB 08H
A72D 08	5225	DEFB 08H
A72E 08	5230	DEFB 08H
A72F 08	5235	DEFB 08H
A730 12	5240	DEFB 12H
A731 01	5245	DEFB 01H
A732 3E	5250	DEFB 3EH
A733 12	5255	DEFB 12H
A734 00	5260	DEFB 00H
A735 08	5265	DEFB 08H
A736 12	5270 DAT9	DEFB 12H
A737 01	5275	DEFB 01H
A738 3E	5280	DEFB 3EH
A739 12	5285	DEFB 12H
A73A 00	5290	DEFB 00H
A73B 08	5295	DEFB 08H
A73C 16	5300 DAT10	DEFB 16H
A73D 14	5305	DEFB 14H
A73E 00	5310	DEFB 00H
A73F	5315	DEFM "WRONG ENTRY TO TRY AGAIN PRESS (ENTER) OR (E
A76D	5320	DEFM " FOR EXIT."
A777 12	5325	DEFB 12H
A778 01	5330	DEFB 01H
A779 3E	5335	DEFB 3EH
A77A 12	5340	DEFB 12H
A77B 00	5345	DEFB 00H
	5350	END

DAT10	A73C	DAT9	A736	DAT8	A6CA
DAT7	A63B	DAT6	A5BE	DAT5	A52A
DAT4	A47F	DAT3	A396	DAT2	A345
MEM	FF00	DAT1	A324	DAT	A292
STAT	A27E	MEN06	A22D	MEN05	A22B
MEN04	A1FA	MEN03	A1F5	MEN02	A1ED
MEN01	A1E5	MEN00	A1DD	CHANG	A1BD
CURSO	A1B3	COTR1	A1A7	COTR3	A198
COTR2	A197	COTR0	A184	COTR	A161
MESA	A147	GIU8	A124	GIU3	A10F
GIU1	A10D	GIU0	A109	GIU4	A100
BET1	A0D7	BET0	A0C6	BET2	A0C2
ARMS	A0B4	FUTH8	A091	FUTH4	A07C
FUTH2	A07A	FUTH1	A076	FUTH0	A072
FUTH5	A061	BIT0	A021	BIT1	A01D
ROUT	A00F	UPW	9FD7	ASCII	9FBB
SUB4	9F95	SUB3	9F68	SUB1	9F64
SUB2	9F55	CONV	9F43	FPONT	9F05
ANSW	9EFC	DOWN1	9EEC	DISP	9EE4
MESS1	9ED5	MESS	9EC6	UP2	9EBD
GET-K	9EB5	AGA4	9EA2	ANAL	9E76
AGA3	9E63	ALAR1	9E2C	AGA2	9E19
ALARM	9DE2	AGA1	9DCF	NEXT1	9D93
AGA	9D80	BRI	9D45	DOWN2	9D3D
AGAIN	9D2E	TOP	9D08	UP1	9CFF
MENU	9CDD	GIR1	9C9E	GIRO	9C92
#	5F15				


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■@AC80      0010      ORG 0AC80H
0020 ;**** **** *****
0030 ;*INP ROUT SERIALIZES-DATA-IN
0040 ;* EF00 -EF1F, UNDER-NMI
0050 ;* CONTROL
AC80 C5      0060      PUSH BC
AC81 DDE5    0070      PUSH IX
AC83 D5      0080      PUSH DE
AC84 FDE5    0090      PUSH IY
AC86 F3      0100      DI
AC87 3ACDEF  0110      LD A, (0EFCDH)
AC8A FE01    0120      CP 01H
AC8C 2828    0130      JR Z, SYNC
AC8E 3ECE    0140      LD A, 0CEH
AC90 32C4EF  0150      LD (0EFC4H), A
AC93 3ECF    0160      LD A, 0CFH
AC95 32C6EF  0170      LD (0EFC6H), A
AC98 3EEF    0180      LD A, 0EFH
AC9A 32C5EF  0190      LD (0EFC5H), A
AC9D 32C7EF  0200      LD (0EFC7H), A
ACA0 3E00    0210      LD A, 00H
ACA2 32C8EF  0220      LD (0EFC8H), A
ACA5 32CAEF  0230      LD (0EFC9H), A
ACA8 32CB EF  0240      LD (0EFCBH), A
ACAB 32CEEF  0250      LD (0EFC EH), A
ACAE 32CF EF  0260      LD (0EFCFH), A
ACB1 3E01    0270      LD A, 01H
ACB3 32CDEF  0280      LD (0EFCDH), A
ACB6 3ACBEF  0290 SYNC LD A, (0EFCBH)
ACB9 FE01    0300      CP 01H
ACBB 2824    0310      JR Z, SICK1
ACBD 2AC4EF  0320      LD HL, (0EFC4H)
ACC0 DD2AC6EF 0330      LD IX, (0EFC6H)
ACC4 DD7E00  0340      LD A, (IX+00H)
ACC7 FE1E    0350      CP 1EH
ACC9 C2AAAD  0360      JP NZ, SYCH
ACCC 7E      0370      LD A, (HL)
ACCD FEB2    0380      CP 0B2H
ACCF C2AAAD  0390      JP NZ, SYCH
0400 ;**** **** *****
0410 ;*SYC 1EB2 HAS-BEEN-DETECTED
0420 ;* NOW RECEIVE-16-WORDS
0430 ;* OF DATA-15-BITS-LONG
ACD2 3E01    0440      LD A, 01H
ACD4 32CB EF  0450      LD (0EFCBH), A
ACD7 3ED0    0460      LD A, 0D0H
ACD9 32C4EF  0470      LD (0EFC4H), A
ACDC 3ED1    0480      LD A, 0D1H
ACDE 32C6EF  0490      LD (0EFC6H), A
ACE1 2AC4EF  0500 SICK1 LD HL, (0EFC4H)
ACE4 DD2AC6EF 0510      LD IX, (0EFC6H)
ACE8 3AC8 EF  0520 SICK LD A, (0EFC8H)
ACEB FE0F    0530      CP 0FH
ACED 2003    0540      JR NZ, SYCH1
ACEF C3FCAC  0550      JP SICK5
ACF2 3AC8 EF  0560 SYCH1 LD A, (0EFC8H)
ACF5 3C      0570      INC A
ACF6 32C8 EF  0580      LD (0EFC8H), A
ACF9 C3AAAD  0590      JP SYCH
ACFC DDCB003E 0600 SICK5 SRL (IX+00H)

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AD00	CB1E	0610	RR	(HL)
AD02	3E00	0620	LD	A,00H
AD04	32C8EF	0630	LD	(0EFC8H),A
AD07	3AC4EF	0640	LD	A,(0EFC4H)
AD0A	3C	0650	INC	A
AD0B	3C	0660	INC	A
AD0C	32C4EF	0670	LD	(0EFC4H),A
AD0F	3AC6EF	0680	LD	A,(0EFC6H)
AD12	3C	0690	INC	A
AD13	3C	0700	INC	A
AD14	32C6EF	0710	LD	(0EFC6H),A
AD17	2AC4EF	0720	LD	HL,(0EFC4H)
AD1A	DD2AC6EF	0730	LD	IX,(0EFC6H)
AD1E	3ACAEF	0740	LD	A,(0EFC4H)
AD21	3C	0750	INC	A
AD22	32CAEF	0760	LD	(0EFC4H),A
AD25	FE10	0770	CP	10H
AD27	C2F2AC	0780	JP	NZ,SYCH1
		0790	****	*****
		0800	;-16	WORD HAVE-BEEN-RECEIVED
		0810	;	NOW CLEAR-COUNTERS-AND
		0820	;	FLAGS
AD2A	3E00	0830	LD	A,00H
AD2C	32CEEF	0840	LD	(0EFC4H),A
AD2F	32CFEF	0850	LD	(0EFC4H),A
AD32	32CAEF	0860	LD	(0EFC4H),A
		0870	****	*****
		0880	;*ROU	TINE FIND-SIGN-STORE-IT
		0890	;*...	TEST COINC-DISP-FLAG=1.
AD35	3A2FF0	0900	LD	A,(0F02FH)
AD38	FE01	0910	CP	01H
AD3A	CAB4AD	0920	JP	Z,RETU
AD3D	0600	0930	LD	B,00H
AD3F	21E0EF	0940	LD	HL,0EFE0H
AD42	DD21F8EE	0950	LD	IX,0EEF8H
AD46	CB46	0960	NUOV	BIT 0,(HL)
AD48	2004	0970	JR	NZ,POSIT
AD4A	3E2D	0980	LD	A,2DH
AD4C	1802	0990	JR	STOR
AD4E	3E2B	1000	POSIT	LD A,2BH
AD50	DD7700	1010	STOR	LD (IX+00H),A
AD53	23	1020	INC	HL
AD54	23	1030	INC	HL
AD55	DD23	1040	INC	IX
AD57	04	1050	INC	B
AD58	78	1060	LD	A,B
AD59	FE08	1070	CP	08H
AD5B	20E9	1080	JR	NZ,NUOV
		1090	****	*****
		1100	;*ROU	TINE TURN-AROUND-ANALOG
		1110	;*VAL	UES MSB-BECOMES-LSB.
		1120	;	AND SHIFTS-SIGN-OUT
AD5D	1600	1130	LD	D,00H
AD5F	21E0EF	1140	LD	HL,0EFE0H
AD62	DD21E1EF	1150	LD	IX,0EFE1H
AD66	0E00	1160	NOOVO	LD C,00H
AD68	0600	1170	LD	B,00H
AD6A	DDCB001E	1180	RR	(IX+00H)
AD6E	CB1E	1190	RR	(HL)
AD70	3E01	1200	LD	A,01H

AD72	DDA600	1210	AND	(IX+00H)
AD75	DD7700	1220	LD	(IX+00H),A
AD78	46	1230	LD	B,(HL)
AD79	CB18	1240	RR	B
AD7B	CB16	1250	RL	(HL)
AD7D	0C	1260	INC	C
AD7E	3E08	1270	LD	A,08H
AD80	B9	1280	CP	C
AD81	20F6	1290	JR	NZ,FINI
AD83	DDCB003E	1300	SRL	(IX+00H)
AD87	CB16	1310	RL	(HL)
AD89	DDCB0016	1320	RL	(IX+00H)
AD8D	14	1330	INC	D
AD8E	3E08	1340	LD	A,08H
AD90	BA	1350	CP	D
AD91	2809	1360	JR	Z,FINO
AD93	23	1370	INC	HL
AD94	23	1380	INC	HL
AD95	DD23	1390	INC	IX
AD97	DD23	1400	INC	IX
AD99	C366AD	1410	JP	NOOVO
		1420	****	*****
		1430	*MOV	DATA BLOCK-OF-32,BYTES.
AD9C	21EFEF	1440	LD	HL,0EFEFH
AD9F	111FEF	1450	LD	DE,0EF1FH
ADA2	012000	1460	LD	BC,0020H
ADA5	EDB8	1470	LDDR	
ADA7	C3B4AD	1480	JP	RETU
		1490	****	*****
		1500	*INP	ROUT INPUTS-DATA-FROM
		1510	*Z80.	PIO-AT-ADDRESS-09B
ADAA	DB9B	1520	SYCH	IN A,(09BH)
ADAC	CB07	1530	RLC	A
ADAE	DDCB001E	1540	RR	(IX+00H)
ADB2	CB1E	1550	RR	(HL)
		1560	****	*****
		1570	*INS	ERTE D-APPOX-5MSEC-DLY.
ADB4	0604	1580	LD	B,04H
ADB6	0EC0	1590	LD	C,0C0H
ADB8	0D	1600	DEC	C
ADB9	20FD	1610	JR	NZ,LOOP0
ADBB	05	1620	DEC	B
ADBC	20F8	1630	JR	NZ,LOOP1
		1640	****	*****
		1650	*FET	CH- AND-CHECK-SYNCH-
		1660	*CON	TROL -DUPLX-INIT-FLAGS.
ADBE	3ACBEF	1670	LD	A,(0EFCBH)
ADC1	FE01	1680	CP	01H
ADC3	C250AF	1690	JP	NZ,RETUN
ADC6	3A00F0	1700	LD	A,(0F000H)
ADC9	FE01	1710	CP	01H
ADCB	200A	1720	JR	NZ,DUPLX
ADCD	3AF6EF	1730	LD	A,(0EFF6H)
ADD0	FE01	1740	CP	01H
ADD2	2803	1750	JR	Z,DUPLX
ADD4	C385AE	1760	JP	CTROL
		1770	****	*****
		1780	*STA	RT- OF-FULL-DUPLX-ROUT
ADD7	3AF6EF	1790	LD	A,(0EFF6H)
ADDA	FE01	1800	CP	01H

ADDC	CA12AE	1810	JP	Z,MASTE
		1820	;**** *****	
		1830	;*INI TIAL IZE-FLAGS,COUNTERS	
		1840	;* AND- TYPE-OF-WORDS.	
ADDF	3EFF	1850	LD	A,0FFH
ADE1	32F8EF	1860	LD	(0EFF8H),A
ADE4	3E0B	1870	LD	A,0BH
ADE6	32F9EF	1880	LD	(0EFF9H),A
ADE9	3E59	1890	LD	A,59H
ADEB	32FAEF	1900	LD	(0EFFAH),A
ADEE	3E0F	1910	LD	A,0FH
ADF0	32FB EF	1920	LD	(0EFFBH),A
ADF3	3E01	1930	LD	A,01H
ADF5	32F6EF	1940	LD	(0EFF6H),A
ADF8	3E00	1950	LD	A,00H
ADFA	32F7EF	1960	LD	(0EFF7H),A
ADFD	32FCEF	1970	LD	(0EFFCH),A
AE00	3EF8	1980	LD	A,0F8H
AE02	32F2EF	1990	LD	(0EFF2H),A
AE05	3EF9	2000	LD	A,0F9H
AE07	32F4EF	2010	LD	(0EFF4H),A
AE0A	3EEF	2020	LD	A,0EFH
AE0C	32F3EF	2030	LD	(0EFF3H),A
AE0F	32F5EF	2040	LD	(0EFF5H),A
AE12	2AF2EF	2050	MASTE LD	HL,(0EFF2H)
AE15	DD2AF4EF	2060	LD	IX,(0EFF4H)
AE19	3AF7EF	2070	LD	A,(0EFF7H)
AE1C	FE0F	2080	CP	0FH
AE1E	2816	2090	JR	Z,MAST1
		2100	;**** *****	
		2110	;*STA RT- OF-O/P-EMPTY-WORDS	
		2120	;* SYNCH-WORD.	
AE20	3AF7EF	2130	SHIF0 LD	A,(0EFF7H)
AE23	3C	2140	INC	A
AE24	32F7EF	2150	LD	(0EFF7H),A
AE27	37	2160	SCF	
AE28	3F	2170	CCF	
AE29	DDCB001E	2180	RR	(IX+00H)
AE2D	CB1E	2190	RR	(HL)
AE2F	CB1F	2200	RR	A
AE31	D3BB	2210	OUT	(0BBH),A
AE33	C350AF	2220	JP	RETUN
		2230	;**** *****	
		2240	;*REL OAD- 0BFFH-EMPTY-WORD	
		2250	;* IN-EFF8H,EFF9H.	
AE36	3EFF	2260	MAST1 LD	A,0FFH
AE38	32F8EF	2270	LD	(0EFF8H),A
AE3B	3E0B	2280	LD	A,0BH
AE3D	32F9EF	2290	LD	(0EFF9H),A
AE40	3AFCEF	2300	LD	A,(0EFFCH)
		2310	;**** *****	
		2320	;* HAVE 0-14,EMPTY-WORDS.	
		2330	;* BEEN-SENT.	
AE43	FE0E	2340	CP	0EH
AE45	2824	2350	JR	Z,MAST2
AE47	FE0F	2360	CP	0FH
AE49	280F	2370	JR	Z,MAST3
AE4B	3AFCEF	2380	MAST4 LD	A,(0EFFCH)
AE4E	3C	2390	INC	A
AE4F	32FCEF	2400	LD	(0EFFCH),A

AE52	3E00	2410	LD	A, 00H
AE54	32F7EF	2420	LD	(0EFF7H), A
AE57	C320AE	2430	JP	SHIF0
	2440	****	****	*****
	2450	*ALL	WORD	S-SENT. CLEAR-MASTE
	2460	*		BIT, FLAGS, COUNTERS
AE5A	3E00	2470	MAST3 LD	A, 00H
AE5C	32F6EF	2480	LD	(0EFF6H), A
AE5F	32CDEF	2490	LD	(0EFC0H), A
AE62	32F7EF	2500	LD	(0EFF7H), A
AE65	32FCEF	2510	LD	(0EFFCH), A
AE68	C350AF	2520	JP	RETUN
	2530	****	****	*****
	2540	*INC	REME	NT-WORD-POINTERS-
	2550	*	AND	LOAD-IX, HL.
AE6B	3AF2EF	2560	MAST2 LD	A, (0EFF2H)
AE6E	3C	2570	INC	A
AE6F	3C	2580	INC	A
AE70	32F2EF	2590	LD	(0EFF2H), A
AE73	3AF4EF	2600	LD	A, (0EFF4H)
AE76	3C	2610	INC	A
AE77	3C	2620	INC	A
AE78	32F4EF	2630	LD	(0EFF4H), A
AE7B	2AF2EF	2640	LD	HL, (0EFF2H)
AE7E	DD2AF4EF	2650	LD	IX, (0EFF4H)
AE82	C34BAE	2660	JP	MAST4
	2670	****	****	*****
	2680	*ROU	TINE	CONTROLS-CHECK-FOR
	2690	*INI	TIAL	IZE-FLAG, INIT/MEM
	2700	*		&SET, INIT/FLAG
AE85	3A01F0	2710	CTROL LD	A, (0F001H)
AE88	FE01	2720	CP	01H
AE8A	CAD7AE	2730	JP	Z, TROLS
AE8D	3E00	2740	LD	A, 00H
AE8F	3202F0	2750	LD	(0F002H), A
AE92	3203F0	2760	LD	(0F003H), A
AE95	3E0F	2770	LD	A, 0FH
AE97	3204F0	2780	LD	(0F004H), A
AE9A	3E10	2790	LD	A, 10H
AE9C	3206F0	2800	LD	(0F006H), A
AE9F	3EF0	2810	LD	A, 0F0H
AEA1	3205F0	2820	LD	(0F005H), A
AEA4	3207F0	2830	LD	(0F007H), A
AEA7	DD2100E0	2840	LD	IX, 0E000H
AEAB	2178E0	2850	LD	HL, 0E078H
	2860	****	****	*****
	2870	*ADD	ROUT	INE-FETCH-CONTROL.
	2880	*	ADJU	ST-F00BH-LEFT/ONE.
AEAE	3A0BF0	2890	LD	A, (0F00BH)
AEB1	CB27	2900	SLA	A
AEB3	320BF0	2910	LD	(0F00BH), A
AEB6	ED4B0BF0	2920	LD	BC, (0F00BH)
AEBA	DD09	2930	ADD	IX, BC
AEBD	DD7E00	2940	LD	A, (IX+00H)
AEBF	3215F0	2950	LD	(0F015H), A
AEC2	DD7E01	2960	LD	A, (IX+01H)
AEC5	3216F0	2970	LD	(0F016H), A
AEC8	09	2980	ADD	HL, BC
AEC9	7E	2990	LD	A, (HL)
AECA	3219F0	3000	LD	(0F019H), A

AECD	23	3010	INC	HL
AECE	7E	3020	LD	A, (HL)
AECF	321AF0	3030	LD	(0F01AH), A
AED2	3E01	3040	LD	A, 01H
AED4	3201F0	3050	LD	(0F001H), A
AED7	2A04F0	3060	TROLS	LD HL, (0F004H)
AEDA	DD2A06F0	3070	LD	IX, (0F006H)
AEDE	3A02F0	3080	LD	A, (0F002H)
AEEl	FE0F	3090	CP	0FH
AEEl	2816	3100	JR	Z, TROL1
		3110	;**** **** *****	
		3120	;*OUT PUT- ROUT.TRANSMIT/DATA	
		3130	;* TO,REMOTE	
AEEl	3A02F0	3140	TROL0	LD A, (0F002H)
AEEl	3C	3150	INC	A
AEEl	3202F0	3160	LD	(0F002H), A
AEEl	37	3170	SCF	
AEED	3F	3180	CCF	
AEEl	DDCB001E	3190	RR	(IX+00H)
AEF2	CB1E	3200	RR	(HL)
AEF4	CB1F	3210	RR	A
AEF6	D3BB	3220	OUT	(0BBH), A
AEF8	C350AF	3230	JP	RETUN
		3240	;**** **** *****	
		3250	;*COU NTED -15BITS,RESTORE-	
		3260	;* 0BFF IN/MEM.CHECK-WORD.	
AEFB	3EFF	3270	TROL1	LD A, 0FFH
AEFD	320FF0	3280	LD	(0F00FH), A
AF00	3E0B	3290	LD	A, 0BH
AF02	3210F0	3300	LD	(0F010H), A
AF05	3A03F0	3310	LD	A, (0F003H)
AF08	FE07	3320	CP	07H
AF0A	2816	3330	JR	Z, TROL3
AF0C	FE01	3340	CP	01H
AF0E	3803	3350	JR	C, TROL4
AF10	C336AF	3360	JP	TROL2
		3370	;**** **** *****	
		3380	;*CLE AR- 15BIT-COUNTER-AND	
		3390	;*INC THE- WORD-COUNTER.	
AF13	3E00	3400	TROL4	LD A, 00H
AF15	3202F0	3410	LD	(0F002H), A
AF18	3A03F0	3420	LD	A, (0F003H)
AF1B	3C	3430	INC	A
AF1C	3203F0	3440	LD	(0F003H), A
AF1F	C3E5AE	3450	JP	TROL0
AF22	3E00	3460	TROL3	LD A, 00H
AF24	3200F0	3470	LD	(0F000H), A
AF27	3201F0	3480	LD	(0F001H), A
AF2A	3202F0	3490	LD	(0F002H), A
AF2D	3203F0	3500	LD	(0F003H), A
AF30	32CDEF	3510	LD	(0EFCDH), A
AF33	C350AF	3520	JP	RETUN
		3530	;**** **** *****	
		3540	;*INC WORD POINTERS-*2-LOAD-	
		3550	;* VALU E-INTO-HL, IX.	
AF36	3A04F0	3560	TROL2	LD A, (0F004H)
AF39	3C	3570	INC	A
AF3A	3C	3580	INC	A
AF3B	3204F0	3590	LD	(0F004H), A
AF3E	3A06F0	3600	LD	A, (0F006H)

AF41 3C	3610	INC A
AF42 3C	3620	INC A
AF43 3206F0	3630	LD (0F006H), A
AF46 2A04F0	3640	LD HL, (0F004H)
AF49 DD2A06F0	3650	LD IX, (0F006H)
AF4D C313AF	3660	JP TROL4
AF50 FDE1	3670	RETUN POP IY
AF52 D1	3680	POP DE
AF53 DDE1	3690	POP IX
AF55 C1	3700	POP BC
AF56 E1	3710	POP HL
AF57 F1	3720	POP AF
AF58 FB	3730	EI
AF59 ED45	3740	RETN
	3750	END
RETUN AF50	TROL2 AF36	TROL3 AF22
TROL4 AF13	TROL1 AEFB	TROL0 AEE5
TROLS AED7	CTROL AE85	MAST2 AE6B
MAST3 AE5A	MAST4 AE4B	MAST1 AE36
SHIF0 AE20	MASTE AE12	DUPLX ADD7
LOOP0 ADB8	LOOP1 ADB6	RETU ADB4
SYCH ADAA	FINO AD9C	FINI AD79
NOOV0 AD66	STOR AD50	POSIT AD4E
NUOV AD46	SICK5 ACFC	SYCH1 ACF2
SICK ACE8	SICK1 ACE1	SYNC ACB6
#	5F15	

E000	0010	ORG 0E000H
	0020	;**** **** *****
	0030	;*TO BE- USED,WITH-SELTA*13
	0040	;**** **** *****
	0050	;*CON TROL -TABLE,0,TO,59.TC.
	0060	; AND THE-INVERSE-TC.
E000 63	0070	DEFB 63H
E001 1C	0080	DEFB 1CH
E002 A3	0090	DEFB 0A3H
E003 40	0100	DEFB 40H
E004 23	0110	DEFB 23H
E005 55	0120	DEFB 55H
E006 23	0130	DEFB 23H
E007 7E	0140	DEFB 7EH
E008 C3	0150	DEFB 0C3H
E009 38	0160	DEFB 38H
E00A 43	0170	DEFB 43H
E00B 2D	0180	DEFB 2DH
E00C 43	0190	DEFB 43H
E00D 06	0200	DEFB 06H
E00E 83	0210	DEFB 83H
E00F 71	0220	DEFB 71H
E010 83	0230	DEFB 83H
E011 5A	0240	DEFB 5AH
E012 03	0250	DEFB 03H
E013 4F	0260	DEFB 4FH
E014 65	0270	DEFB 65H
E015 58	0280	DEFB 58H
E016 A5	0290	DEFB 0A5H
E017 04	0300	DEFB 04H
E018 25	0310	DEFB 25H
E019 11	0320	DEFB 11H
E01A 25	0330	DEFB 25H
E01B 3A	0340	DEFB 3AH
E01C C5	0350	DEFB 0C5H
E01D 7C	0360	DEFB 7CH
E01E 45	0370	DEFB 45H
E01F 69	0380	DEFB 69H
E020 45	0390	DEFB 45H
E021 42	0400	DEFB 42H
E022 85	0410	DEFB 85H
E023 35	0420	DEFB 35H
E024 85	0430	DEFB 85H
E025 1E	0440	DEFB 1EH
E026 05	0450	DEFB 05H
E027 0B	0460	DEFB 0BH
E028 69	0470	DEFB 69H
E029 7C	0480	DEFB 7CH
E02A A9	0490	DEFB 0A9H
E02B 20	0500	DEFB 20H
E02C 29	0510	DEFB 29H
E02D 35	0520	DEFB 35H
E02E 29	0530	DEFB 29H
E02F 1E	0540	DEFB 1EH
E030 C9	0550	DEFB 0C9H
E031 58	0560	DEFB 58H
E032 49	0570	DEFB 49H
E033 4D	0580	DEFB 4DH
E034 49	0590	DEFB 49H
E035 66	0600	DEFB 66H

E036 89	0610	DEFB 89H
E037 11	0620	DEFB 11H
E038 89	0630	DEFB 89H
E039 3A	0640	DEFB 3AH
E03A 09	0650	DEFB 09H
E03B 2F	0660	DEFB 2FH
E03C 71	0670	DEFB 71H
E03D 34	0680	DEFB 34H
E03E B1	0690	DEFB 0B1H
E03F 68	0700	DEFB 68H
E040 31	0710	DEFB 31H
E041 7D	0720	DEFB 7DH
E042 31	0730	DEFB 31H
E043 56	0740	DEFB 56H
E044 D1	0750	DEFB 0D1H
E045 10	0760	DEFB 10H
E046 51	0770	DEFB 51H
E047 05	0780	DEFB 05H
E048 51	0790	DEFB 51H
E049 2E	0800	DEFB 2EH
E04A 91	0810	DEFB 91H
E04B 59	0820	DEFB 59H
E04C 91	0830	DEFB 91H
E04D 72	0840	DEFB 72H
E04E 11	0850	DEFB 11H
E04F 67	0860	DEFB 67H
E050 66	0870	DEFB 66H
E051 2C	0880	DEFB 2CH
E052 A6	0890	DEFB 0A6H
E053 70	0900	DEFB 70H
E054 26	0910	DEFB 26H
E055 65	0920	DEFB 65H
E056 26	0930	DEFB 26H
E057 4E	0940	DEFB 4EH
E058 C6	0950	DEFB 0C6H
E059 08	0960	DEFB 08H
E05A 46	0970	DEFB 46H
E05B 1D	0980	DEFB 1DH
E05C 46	0990	DEFB 46H
E05D 36	1000	DEFB 36H
E05E 86	1010	DEFB 86H
E05F 41	1020	DEFB 41H
E060 86	1030	DEFB 86H
E061 6A	1040	DEFB 6AH
E062 06	1050	DEFB 06H
E063 7F	1060	DEFB 7FH
E064 6A	1070	DEFB 6AH
E065 08	1080	DEFB 08H
E066 AA	1090	DEFB 0AAH
E067 54	1100	DEFB 54H
E068 2A	1110	DEFB 2AH
E069 41	1120	DEFB 41H
E06A 2A	1130	DEFB 2AH
E06B 6A	1140	DEFB 6AH
E06C CA	1150	DEFB 0CAH
E06D 2C	1160	DEFB 2CH
E06E 4A	1170	DEFB 4AH
E06F 39	1180	DEFB 39H
E070 4A	1190	DEFB 4AH
E071 12	1200	DEFB 12H

E072 8A	1210	DEFB 8AH
E073 65	1220	DEFB 65H
E074 8A	1230	DEFB 8AH
E075 4E	1240	DEFB 4EH
E076 0A	1250	DEFB 0AH
E077 5B	1260	DEFB 5BH
	1270 ;****	**** *****
	1280 ;*CON	TROL -INVERSE-OF-TC-
E078 9C	1290	DEFB 9CH
E079 07	1300	DEFB 07H
E07A 5C	1310	DEFB 5CH
E07B 5B	1320	DEFB 5BH
E07C DC	1330	DEFB 0DCH
E07D 4E	1340	DEFB 4EH
E07E DC	1350	DEFB 0DCH
E07F 65	1360	DEFB 65H
E080 3C	1370	DEFB 3CH
E081 23	1380	DEFB 23H
E082 BC	1390	DEFB 0BCH
E083 36	1400	DEFB 36H
E084 BC	1410	DEFB 0BCH
E085 1D	1420	DEFB 1DH
E086 7C	1430	DEFB 7CH
E087 6A	1440	DEFB 6AH
E088 7C	1450	DEFB 7CH
E089 41	1460	DEFB 41H
E08A FC	1470	DEFB 0FCH
E08B 54	1480	DEFB 54H
E08C 9A	1490	DEFB 9AH
E08D 43	1500	DEFB 43H
E08E 5A	1510	DEFB 5AH
E08F 1F	1520	DEFB 1FH
E090 DA	1530	DEFB 0DAH
E091 0A	1540	DEFB 0AH
E092 DA	1550	DEFB 0DAH
E093 21	1560	DEFB 21H
E094 3A	1570	DEFB 3AH
E095 67	1580	DEFB 67H
E096 BA	1590	DEFB 0BAH
E097 72	1600	DEFB 72H
E098 BA	1610	DEFB 0BAH
E099 59	1620	DEFB 59H
E09A 7A	1630	DEFB 7AH
E09B 2E	1640	DEFB 2EH
E09C 7A	1650	DEFB 7AH
E09D 05	1660	DEFB 05H
E09E FA	1670	DEFB 0FAH
E09F 10	1680	DEFB 10H
E0A0 96	1690	DEFB 96H
E0A1 67	1700	DEFB 67H
E0A2 56	1710	DEFB 56H
E0A3 3B	1720	DEFB 3BH
E0A4 D6	1730	DEFB 0D6H
E0A5 2E	1740	DEFB 2EH
E0A6 D6	1750	DEFB 0D6H
E0A7 05	1760	DEFB 05H
E0A8 36	1770	DEFB 36H
E0A9 43	1780	DEFB 43H
E0AA B6	1790	DEFB 0B6H
E0AB 56	1800	DEFB 56H

E0AC	B6	1810	DEFB	0B6H
E0AD	7D	1820	DEFB	7DH
E0AE	76	1830	DEFB	76H
E0AF	0A	1840	DEFB	0AH
E0B0	76	1850	DEFB	76H
E0B1	21	1860	DEFB	21H
E0B2	F6	1870	DEFB	0F6H
E0B3	34	1880	DEFB	34H
E0B4	8E	1890	DEFB	8EH
E0B5	2F	1900	DEFB	2FH
E0B6	4E	1910	DEFB	4EH
E0B7	73	1920	DEFB	73H
E0B8	CE	1930	DEFB	0CEH
E0B9	66	1940	DEFB	66H
E0BA	CE	1950	DEFB	0CEH
E0BB	4D	1960	DEFB	4DH
E0BC	2E	1970	DEFB	2EH
E0BD	0B	1980	DEFB	0BH
E0BE	AE	1990	DEFB	0AEH
E0BF	1E	2000	DEFB	1EH
E0C0	AE	2010	DEFB	0AEH
E0C1	35	2020	DEFB	35H
E0C2	6E	2030	DEFB	6EH
E0C3	42	2040	DEFB	42H
E0C4	6E	2050	DEFB	6EH
E0C5	69	2060	DEFB	69H
E0C6	EE	2070	DEFB	0EEH
E0C7	7C	2080	DEFB	7CH
E0C8	99	2090	DEFB	99H
E0C9	37	2100	DEFB	37H
E0CA	59	2110	DEFB	59H
E0CB	6B	2120	DEFB	6BH
E0CC	D9	2130	DEFB	0D9H
E0CD	7E	2140	DEFB	7EH
E0CE	D9	2150	DEFB	0D9H
E0CF	55	2160	DEFB	55H
E0D0	39	2170	DEFB	39H
E0D1	13	2180	DEFB	13H
E0D2	B9	2190	DEFB	0B9H
E0D3	06	2200	DEFB	06H
E0D4	B9	2210	DEFB	0B9H
E0D5	2D	2220	DEFB	2DH
E0D6	79	2230	DEFB	79H
E0D7	5A	2240	DEFB	5AH
E0D8	79	2250	DEFB	79H
E0D9	71	2260	DEFB	71H
E0DA	F9	2270	DEFB	0F9H
E0DB	64	2280	DEFB	64H
E0DC	95	2290	DEFB	95H
E0DD	13	2300	DEFB	13H
E0DE	55	2310	DEFB	55H
E0DF	4F	2320	DEFB	4FH
E0E0	D5	2330	DEFB	0D5H
E0E1	5A	2340	DEFB	5AH
E0E2	D5	2350	DEFB	0D5H
E0E3	71	2360	DEFB	71H
E0E4	35	2370	DEFB	35H
E0E5	37	2380	DEFB	37H
E0E6	B5	2390	DEFB	0B5H
E0E7	22	2400	DEFB	22H

E0E8 B5	2410	DEFB 0B5H
E0E9 09	2420	DEFB 09H
E0EA 75	2430	DEFB 75H
E0EB 7E	2440	DEFB 7EH
E0EC 75	2450	DEFB 75H
E0ED 55	2460	DEFB 55H
E0EE F5	2470	DEFB 0F5H
E0EF 40	2480	DEFB 40H
	2490	END
#	5F15	

@@@F800

0000

ORG 0F800H

0005 ;**** *****

0006 ;*THE FOLL IS,KOEBERG,SYSTEM-

0007 ;* VARIABLE,INFORMATN

F800 16

0010 DEFB 16H

F801 03

0020 DEFB 03H

F802 10

0030 DEFB 10H

F803

0040 DEFM "KOEBERG 400A"

F80F FF

0050 DEFB 0FFH

F810 16

0060 DEFB 16H

F811 0B

0070 DEFB 0BH

F812 09

0080 DEFB 09H

F813 14

0090 DEFB 14H

F814 01

0100 DEFB 01H

F815

0110 DEFM "END OF PROGRAM"

F823 14

0120 DEFB 14H

F824 00

0130 DEFB 00H

F825 FF

0140 DEFB 0FFH

F826 16

0150 DEFB 16H

F827 03

0160 DEFB 03H

F828 04

0170 DEFB 04H

F829

0180 DEFM "400/132kV TRF 1 HV BK "

F840 16

0190 DEFB 16H

F841 04

0200 DEFB 04H

F842 04

0210 DEFB 04H

F843

0220 DEFM "400/132kV TRF 1 MV BK "

F85A 16

0230 DEFB 16H

F85B 05

0240 DEFB 05H

F85C 04

0250 DEFB 04H

F85D

0260 DEFM "400/132kV TRF 2 HV BK "

F874 16

0270 DEFB 16H

F875 06

0280 DEFB 06H

F876 04

0290 DEFB 04H

F877

0300 DEFM "400/132kV TRF 2 MV BK "

F88E 16

0320 DEFB 16H

F88F 07

0330 DEFB 07H

F890 04

0340 DEFB 04H

F891

0350 DEFM "AURORA 400kV FD.5 BK "

F8A8 16

0360 DEFB 16H

F8A9 08

0370 DEFB 08H

F8AA 04

0380 DEFB 04H

F8AB

0390 DEFM "AURORA 400kV FD.5 AUTSY"

F8C2 16

0400 DEFB 16H

F8C3 09

0410 DEFB 09H

F8C4 04

0420 DEFB 04H

F8C5

0430 DEFM "AURORA 400kV FD.5 RLOCK"

F8DC 16

0440 DEFB 16H

F8DD 0A

0450 DEFB 0AH

F8DE 04

0460 DEFB 04H

F8DF

0470 DEFM "MVLEI1 400kV FD.4 BK "

F8F6 16

0480 DEFB 16H

F8F7 0B

0490 DEFB 0BH

F8F8 04

0500 DEFB 04H

F8F9

0510 DEFM "MVLEI1 400kV FD.4 AUTSY"

F910 16

0520 DEFB 16H

F911 0C

0530 DEFB 0CH

F912 04

0540 DEFB 04H

F913

0550 DEFM "MVLEI1 400kV FD.4 RLOCK"

F92A 16

0560 DEFB 16H

F92B 0D

0570 DEFB 0DH

F92C 04	0580	DEFB 04H
F92D	0590	DEFM "400kV B/C NORTH(B) BK "
F944 16	0600	DEFB 16H
F945 0E	0610	DEFB 0EH
F946 04	0620	DEFB 04H
F947	0630	DEFM "400kV B/C NORTH(B) ATSY"
F95E 16	0640	DEFB 16H
F95F 0F	0650	DEFB 0FH
F960 04	0660	DEFB 04H
F961	0670	DEFM "400kV B/S 2 AUTSY-PROG "
F978 16	0680	DEFB 16H
F979 10	0690	DEFB 10H
F97A 04	0700	DEFB 04H
F97B	0710	DEFM "400kV B/S 2 BK "
F992 16	0720	DEFB 16H
F993 11	0730	DEFB 11H
F994 04	0740	DEFB 04H
F995	0750	DEFM "MVLEI2 400kV FD.3 BK "
F9AC FF	0760	DEFB 0FFH
F9AD 16	0780	DEFB 16H
F9AE 03	0790	DEFB 03H
F9AF 04	0800	DEFB 04H
F9B0	0810	DEFM "MVLEI2 400kV FD.3 AUTSY"
F9C7 16	0820	DEFB 16H
F9C8 04	0830	DEFB 04H
F9C9 04	0840	DEFB 04H
F9CA	0850	DEFM "MVLEI2 400kV FD.3 RCOUT"
F9E1 16	0860	DEFB 16H
F9E2 05	0870	DEFB 05H
F9E3 04	0880	DEFB 04H
F9E4	0890	DEFM "ACACIA1 400kV FD.2 BK "
F9FB 16	0900	DEFB 16H
F9FC 06	0910	DEFB 06H
F9FD 04	0920	DEFB 04H
F9FE	0930	DEFM "ACACIA1 400kV FD.2 ATSY"
FA15 16	0940	DEFB 16H
FA16 07	0950	DEFB 07H
FA17 04	0960	DEFB 04H
FA18	0970	DEFM "ACACIA1 400kV FD.2 ROUT"
FA2F 16	0980	DEFB 16H
FA30 08	0990	DEFB 08H
FA31 04	1000	DEFB 04H
FA32	1010	DEFM "400kV B/S 1 BK "
FA49 16	1020	DEFB 16H
FA4A 09	1030	DEFB 09H
FA4B 04	1040	DEFB 04H
FA4C	1050	DEFM "400kV B/S 1 AUTSY-PROG "
FA63 16	1060	DEFB 16H
FA64 0A	1070	DEFB 0AH
FA65 04	1080	DEFB 04H
FA66	1090	DEFM "ACACIA2 400kV FD.1 BK "
FA7D 16	1100	DEFB 16H
FA7E 0B	1110	DEFB 0BH
FA7F 04	1120	DEFB 04H
FA80	1130	DEFM "ACACIA2 400kV FD.1 ASYP"
FA97 16	1140	DEFB 16H
FA98 0C	1150	DEFB 0CH
FA99 04	1160	DEFB 04H
FA9A	1170	DEFM "ACACIA2 400kV FD.1 ROUT"
FAB1 16	1180	DEFB 16H

FAB2 0D	1190	DEFB 0DH	
FAB3 04	1200	DEFB 04H	
FAB4	1210	DEFM "400kV B/C SOUTH(A) BK	"
FACB 16	1220	DEFB 16H	
FACC 0E	1230	DEFB 0EH	
FACD 04	1240	DEFB 04H	
FACE	1250	DEFM "400kV B/C SOUTH(A) ASYP"	
FAE5 16	1260	DEFB 16H	
FAE6 0F	1270	DEFB 0FH	
FAE7 04	1280	DEFB 04H	
FAE8	1290	DEFM "400kV GEN.TRF1 HV BK	"
FAFF 16	1300	DEFB 16H	
FB00 10	1310	DEFB 10H	
FB01 04	1320	DEFB 04H	
FB02	1330	DEFM "400kV GEN.TRF2 HV BK	"
FB19 16	1340	DEFB 16H	
FB1A 11	1350	DEFB 11H	
FB1B 04	1360	DEFB 04H	
FB1C	1370	DEFM "SPARE....."	
FB32 FF	1380	DEFB 0FFH	
FB33 16	1400	DEFB 16H	
FB34 02	1410	DEFB 02H	
FB35 04	1420	DEFB 04H	
FB36	1430	DEFM "CARRIER TX ALARM	"
FB4D 16	1440	DEFB 16H	
FB4E 03	1450	DEFB 03H	
FB4F 04	1460	DEFB 04H	
FB50	1470	DEFM "CARRIER RX ALARM	"
FB67 16	1480	DEFB 16H	
FB68 04	1490	DEFB 04H	
FB69 04	1500	DEFB 04H	
FB6A	1510	DEFM "ALARM UNIT FAIL	"
FB81 16	1520	DEFB 16H	
FB82 05	1530	DEFB 05H	
FB83 04	1540	DEFB 04H	
FB84	1550	DEFM "CHGER DC PANEL& AC FAIL"	
FB9B 16	1560	DEFB 16H	
FB9C 06	1570	DEFB 06H	
FB9D 04	1580	DEFB 04H	
FB9E	1590	DEFM "50V DC CHGER FAIL	"
FBB5 16	1600	DEFB 16H	
FBB6 07	1610	DEFB 07H	
FBB7 04	1620	DEFB 04H	
FBB8	1630	DEFM "ACACIA GT TELE/IND.FAIL"	
FBCF 16	1640	DEFB 16H	
FBD0 08	1650	DEFB 08H	
FBD1 04	1660	DEFB 04H	
FBD2	1670	DEFM "ACACIA2 400kV FD1 ALM	"
FBE9 16	1680	DEFB 16H	
FBEA 09	1690	DEFB 09H	
FBEB 04	1700	DEFB 04H	
FBE C	1710	DEFM "ACACIA2 400kV FD.2 ALM	"
FC03 16	1720	DEFB 16H	
FC04 0A	1730	DEFB 0AH	
FC05 04	1740	DEFB 04H	
FC06	1750	DEFM "MVLEI2 400kV FD.3 ALM	"
FC1D 16	1760	DEFB 16H	
FC1E 0B	1770	DEFB 0BH	
FC1F 04	1780	DEFB 04H	
FC20	1790	DEFM "MVLEI1 400kV FD.4 ALM	"

FC37 FF	1795	DEFB 0FFH	
FC38 16	1800	DEFB 16H	
FC39 02	1810	DEFB 02H	
FC3A 04	1820	DEFB 04H	
FC3B	1830	DEFM "AURORA1 400kV FD.5 ALM	"
FC52 16	1840	DEFB 16H	
FC53 03	1850	DEFB 03H	
FC54 04	1860	DEFB 4H	
FC55	1870	DEFM "400kV B/C NORTH ALM	"
FC6C 16	1880	DEFB 16H	
FC6D 04	1890	DEFB 04H	
FC6E 04	1900	DEFB 04H	
FC6F	1910	DEFM "400kV B/C SOUTH ALM	"
FC86 16	1920	DEFB 16H	
FC87 05	1930	DEFB 05H	
FC88 04	1940	DEFB 04H	
FC89	1950	DEFM "400kV BUS-SECT1 ALM	"
FCA0 16	1960	DEFB 16H	
FCA1 06	1970	DEFB 06H	
FCA2 04	1980	DEFB 04H	
FCA3	1990	DEFM "400kV BUS-SECT2 ALM	"
FCBA 16	2000	DEFB 16H	
FCBB 07	2010	DEFB 07H	
FCBC 04	2020	DEFB 04H	
FCBD	2030	DEFM "400kV GEN.TRF1 ALM	"
FCD4 16	2040	DEFB 16H	
FCD5 08	2050	DEFB 08H	
FCD6 04	2060	DEFB 04H	
FCD7	2070	DEFM "400kV GEN.TRF2 ALM	"
FCEE 16	2080	DEFB 16H	
FCEF 09	2090	DEFB 09H	
FCF0 04	2100	DEFB 04H	
FCF1	2110	DEFM "400/132kv TRF1 ALM	"
FD08 16	2120	DEFB 16H	
FD09 0A	2130	DEFB 0AH	
FD0A 04	2140	DEFB 04H	
FD0B	2150	DEFM "400/132kv TRF2 ALM	"
FD22 16	2160	DEFB 16H	
FD23 0B	2170	DEFB 0BH	
FD24 04	2180	DEFB 04H	
FD25	2190	DEFM "SELTA OUTSTATION FAIL	"
FD3C FF	2200	DEFB 0FFH	
FD3D 16	2220	DEFB 16H	
FD3E 03	2230	DEFB 03H	
FD3F 03	2240	DEFB 03H	
FD40	2250	DEFM "ACACIA1 400kV FD.MW	"
FD57 16	2260	DEFB 16H	
FD58 04	2270	DEFB 04H	
FD59 03	2280	DEFB 03H	
FD5A	2290	DEFM "MVLEI 1&2 FD.....MW	"
FD71 16	2300	DEFB 16H	
FD72 05	2310	DEFB 05H	
FD73 03	2320	DEFB 03H	
FD74	2330	DEFM "ACACIA1 400kV FD.MVars	"
FD8B 16	2340	DEFB 16H	
FD8C 06	2350	DEFB 06H	
FD8D 03	2360	DEFB 03H	
FD8E	2370	DEFM "AURORA FD.....MW	"
FDA5 16	2380	DEFB 16H	
FDA6 07	2390	DEFB 07H	

FDA7 03	2400	DEFB 03H
FDA8	2410	DEFM "AURORA FD.....MVars "
FDBF 16	2420	DEFB 16H
FDC0 08	2430	DEFB 08H
FDC1 03	2440	DEFB 03H
FDC2	2450	DEFM "MVLEI 1&2 FD.....MVars "
FDD9 16	2460	DEFB 16H
FDDA 09	2470	DEFB 09H
Fddb 03	2480	DEFB 03H
FDDC	2490	DEFM "400kV STATION....VOLTS "
FDF3 16	2500	DEFB 16H
FDF4 0A	2510	DEFB 0AH
FDF5 03	2520	DEFB 03H
FDF6	2530	DEFM "400kV STAT/FREQ Hz..45 "
FE0D FF	2540	DEFB 0FFH
	2545 ;****	*****
	2547 ;*THE	FOLL DATA,IS,SCAL/FACTS
	2548 ;*	MULT &SCAL/FACTS,DEVIDE
FE0E 14	2550	DEFB 14H
FE0F 00	2560	DEFB 00H
FE10 14	2570	DEFB 14H
FE11 00	2580	DEFB 00H
FE12 06	2590	DEFB 06H
FE13 00	2600	DEFB 00H
FE14 14	2610	DEFB 14H
FE15 00	2620	DEFB 00H
FE16 06	2630	DEFB 06H
FE17 00	2640	DEFB 00H
FE18 0C	2650	DEFB 0CH
FE19 00	2660	DEFB 00H
FE1A 0C	2670	DEFB 0CH
FE1B 00	2680	DEFB 00H
FE1C 02	2690	DEFB 02H
FE1D 00	2700	DEFB 00H
FE1E 0A	2710	DEFB 0AH
FE1F 00	2720	DEFB 00H
FE20 0A	2730	DEFB 0AH
FE21 00	2740	DEFB 00H
FE22 0A	2750	DEFB 0AH
FE23 00	2760	DEFB 00H
FE24 0A	2770	DEFB 0AH
FE25 00	2780	DEFB 00H
FE26 0A	2790	DEFB 0AH
FE27 00	2800	DEFB 00H
FE28 0A	2810	DEFB 0AH
FE29 00	2820	DEFB 00H
FE2A 0A	2830	DEFB 0AH
FE2B 00	2840	DEFB 00H
FE2C 64	2850	DEFB 64H
FE2D 00	2860	DEFB 00H
	2870	END

5F15

13.0 FLOW CHARTS

The following is a brief explanation on the contents of the various flow charts.

Page 001 : Main body of the program, it takes care of the following:

- (a) Moves scaling factors to required locations.
- (b) Initializes Z80 P.I.O. and enables $\overline{\text{NMI}}$.
- (c) Displays prompts and detects key entry.
- (d) Jump to selected entry, or displays error message.
- (e) If exit is selected, it disables $\overline{\text{NMI}}$, displays "END OF PROGRAM".

Page 002 : B.R.I. page 1.

- (a) Displays breaker names and status on screen.
- (b) Displays prompts and detects key entry.
- (c) Jump to selected entry, or displays error message.
- (d) Updates 01 to 15 B.R.I. status on screen.
- (e) Allows selection of page 1 or page 2 of B.R.I. displays.

Page 003 : Alarm page 1.

- (a) Displays alarm names and status on screen (1 - 10).
- (b) Displays prompts and detects key entry.
- (c) Jumps to selected entry, or displays error message.
- (d) Updates alarm status on screen.
- (e) Allows selection of page 1 or page 2 of alarm display.

Page 004 : Analogues.

- (a) Displays analogue names, values and sign on screen.
- (b) Displays prompts and detects key entry.
- (c) Jumps to selected entry, or displays error message.
- (d) Updates analogue values.

Page 005 : B.R.I. page 2.

- (a) It is similar to page 002 only the parameters are changed.
- (b) Displays different prompts to the ones displayed on page 002.
- (c) Updates page 2, 16 - 30 B.R.I. status.

Page 006 : Control selection input routine.

- (a) Displays prompts and detects key entries.
- (b) Detects entry error and allows you to exit without executing a remote control.
- (c) Stores entries and proceeds to conversion routine.
(CHANG)

Page 007 : Control key entry conversion routine.

- (a) Detects entries 01 - 09, 10 - 19, 20 - 29, 30.
- (b) Selects appropriate subtrahend.
- (c) Converts entry into appropriate offset.
- (d) Initializes control memories.
- (e) Sets control flag.
- (f) Jumps to the required display page of B.R.I.

Page 008 : ALARM page 2.

- (a) It is similar to page 003 only the parameters are changed.
- (b) Displays different prompts to the ones displayed on page 003.
- (c) Updates page 2, 11 - 20 alarm status on screen.

Page 009 : 3 part B.R.I. conversion and display routine.

- (a) Takes the 12 bytes of B.R.I. status, removes the bit check and restores data in groups of 2 bits.
- (b) Converts the stored 30 groups of breaker status into an ASCII character. 0 = open, C = Close A = Anomally (fault condition).
- (c) Prints the breaker status next to the breaker names, selecting either page 1 or page 2.

Page 010 : 3 part alarm conversion and display routine.

- (a) Takes the 4 bytes of alarm inputs, removes the bit check and restores data as 20 single bits.
- (b) Converts the stored 20 bits into ASCII characters T = True, F = Fault.
- (c) Prints the alarm status next to the alarm names, selecting either page 1 or page 2 of data.

Page 011 : 3 part analogue routine.

- (a) Uses the Spectrum floating point calculator to convert the received binary counts into 8 x 2 byte values.
- (b) Converts the 8 x 2 bytes values into 8 x 4 bytes quantities.
- (c) Converts the 32 bytes into ASCII characters to be printed on the screen.
- (d) Prints the analogues values on the screen with sign.

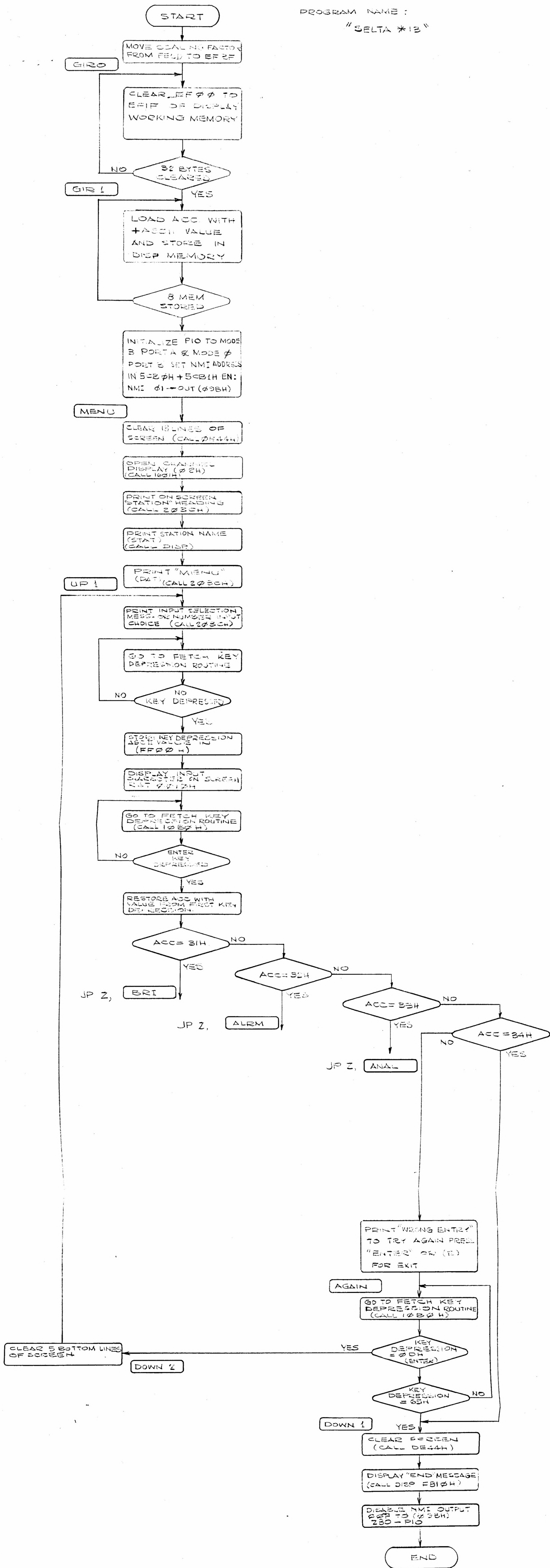
Page 012 : This routine is called IPR*2 and runs under the control of the NMI.

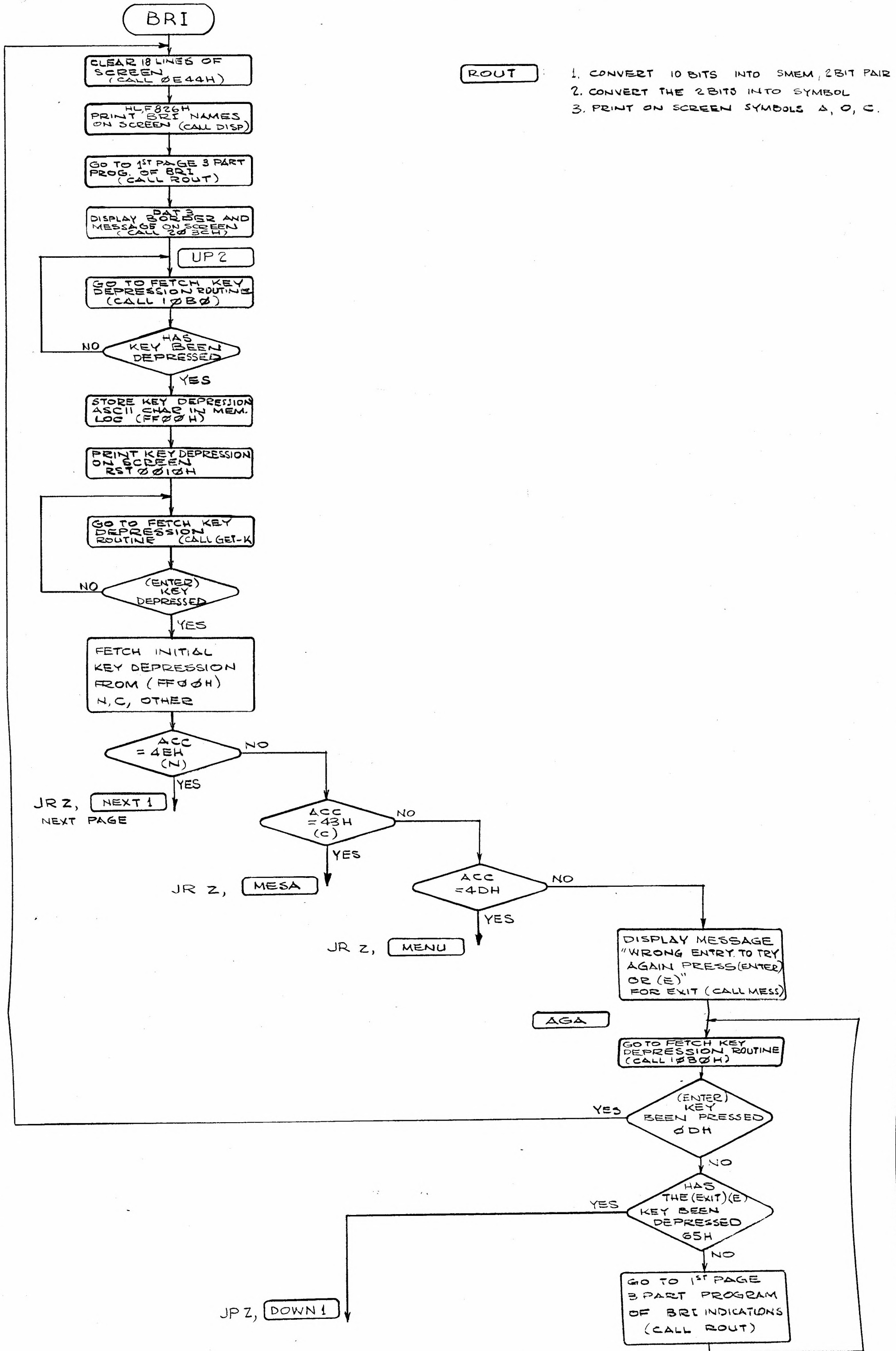
- (a) Searches for the synch word and check bits.
- (b) Receives the 16 words of useful information from the remote and stores them in 32 bytes of memory.
- (c) Takes care of the sign, aligns the received analogue quantity and turns it around so the M.S.B. becomes L.S.B.
- (d) Moves the received incoming data stored in the input serial data temporary store, to the display working memory.
- (e) Introduces approximately a 4 m/sec delay to the data sent to the remote.
- (f) Checks the control flag, the synch flag and the master initialize flag.
- (g) Transmits to the remote PVX empty words and a synchronizing word resetting the remote word counter at the correct word count.
- (h) Takes care of the display coincidence detection.
- (i) Returns to the main program until the next $\overline{\text{NMI}}$.

Page 013 : This routine is part of IPR*2 and transmits remote controls to the remote.

- (a) Checks the control flag and is synchronized to the transmitted data sent to the remote.
- (b) Sends SYNCH, PVX, TELEC, GTC, TC, $\overline{\text{GTC}}$, $\overline{\text{TC}}$, SYNCH words to the remote. The 1st synch word resets the remote word counter and so does the last enabling the remote to resume normal transmission.
- (c) Returns to the main program and is not executed again until the control flag is set again.

PROGRAM NAME :
"SELTA *12"

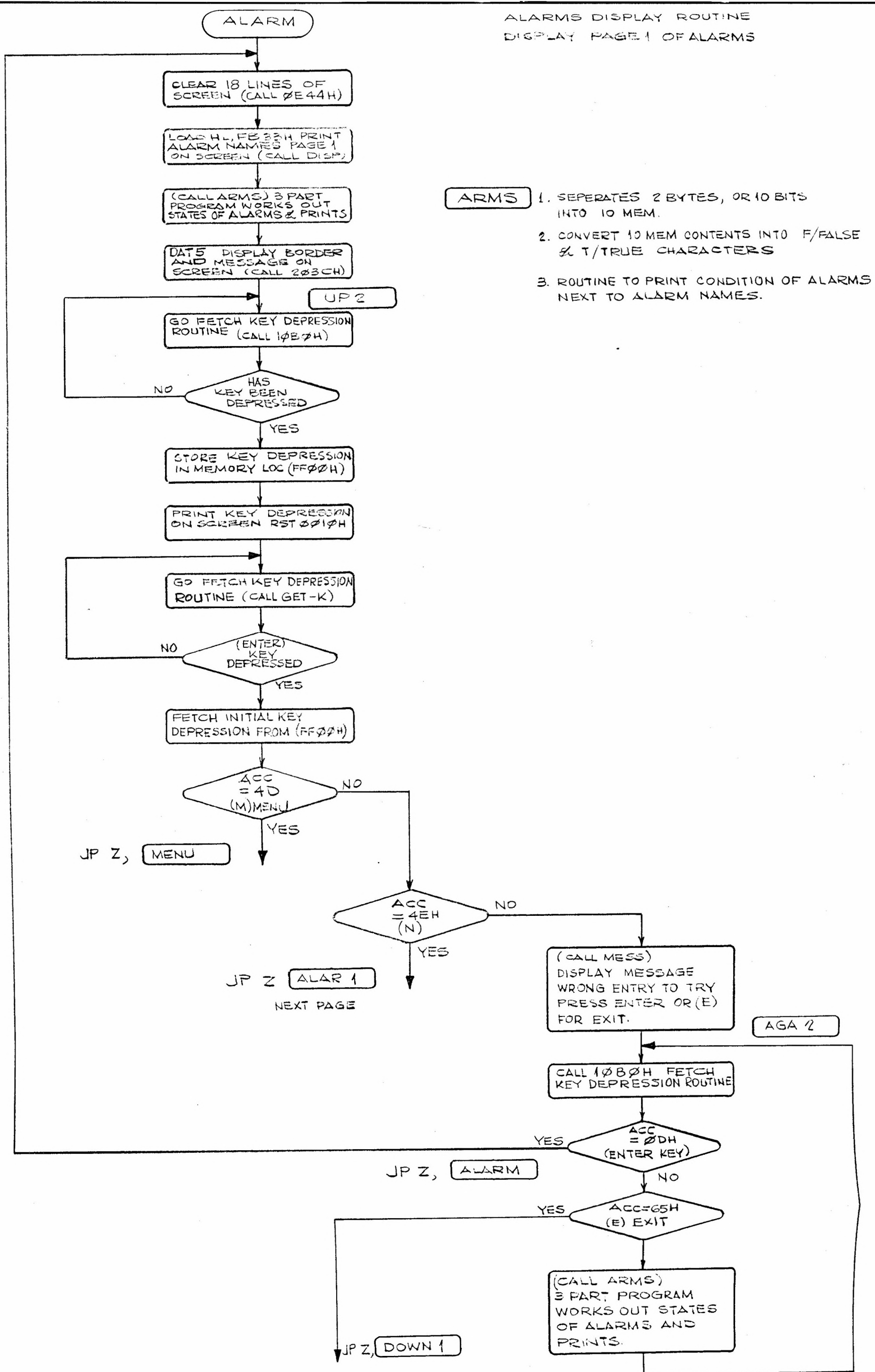


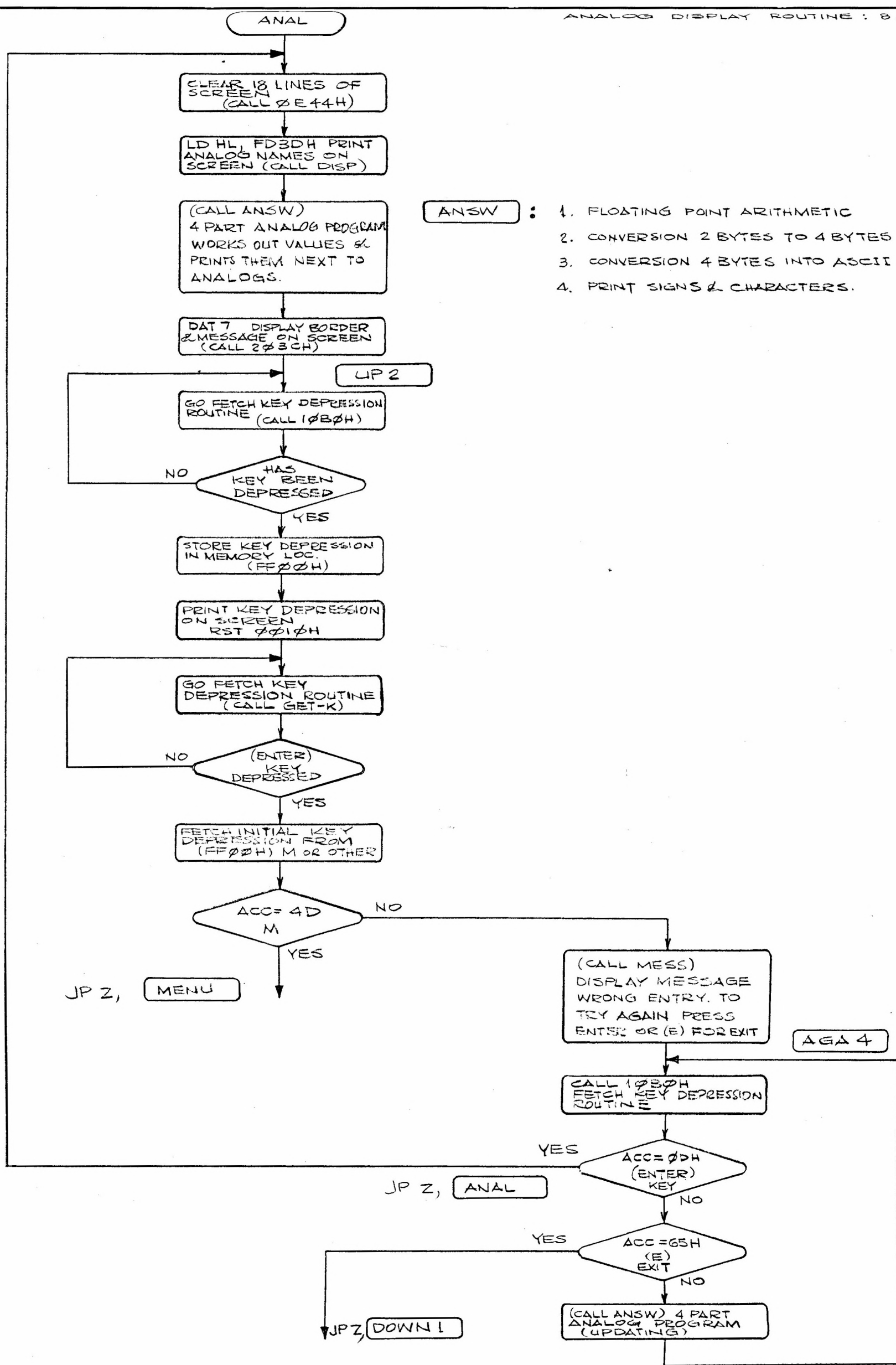


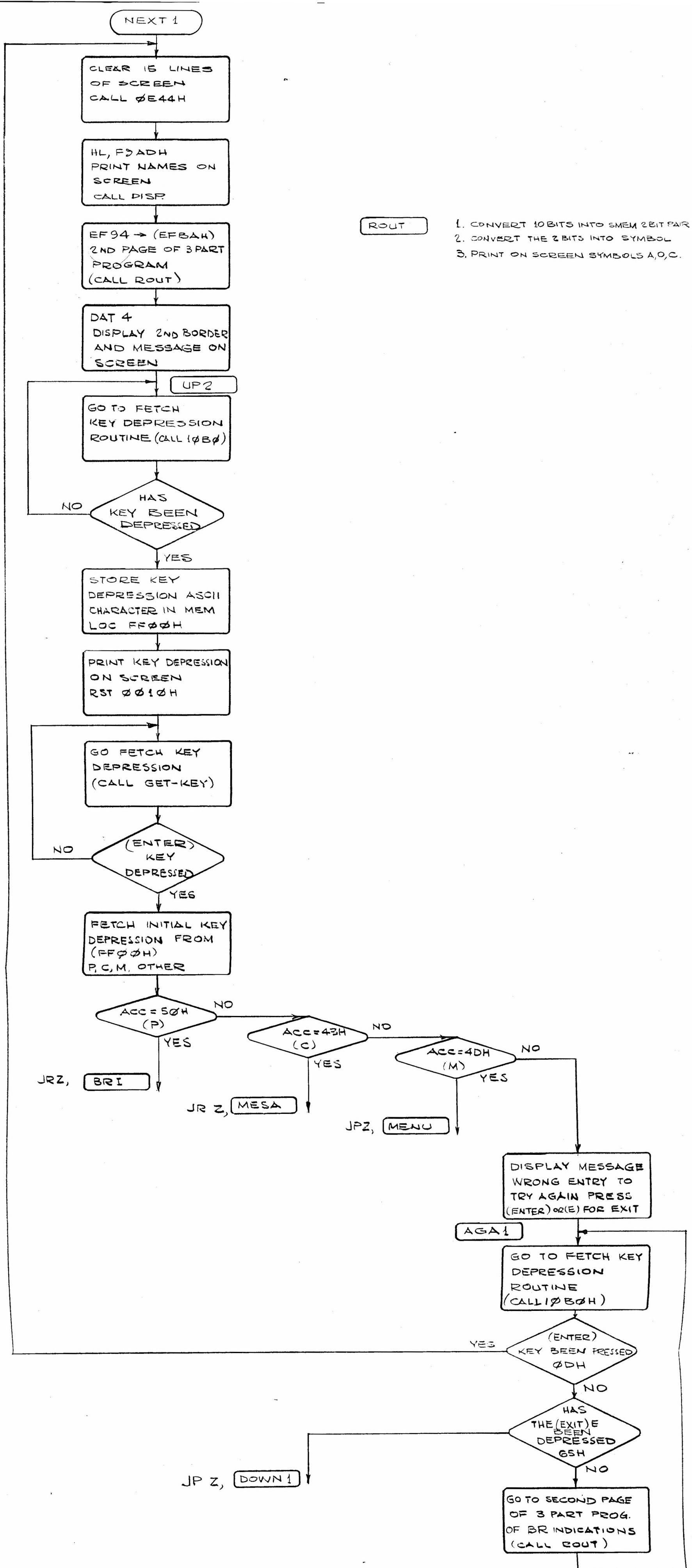
ROUT

1. CONVERT 10 BITS INTO SMEM, 2BIT PAIR
2. CONVERT THE 2BITS INTO SYMBOL
3. PRINT ON SCREEN SYMBOLS A, O, C.

AGA

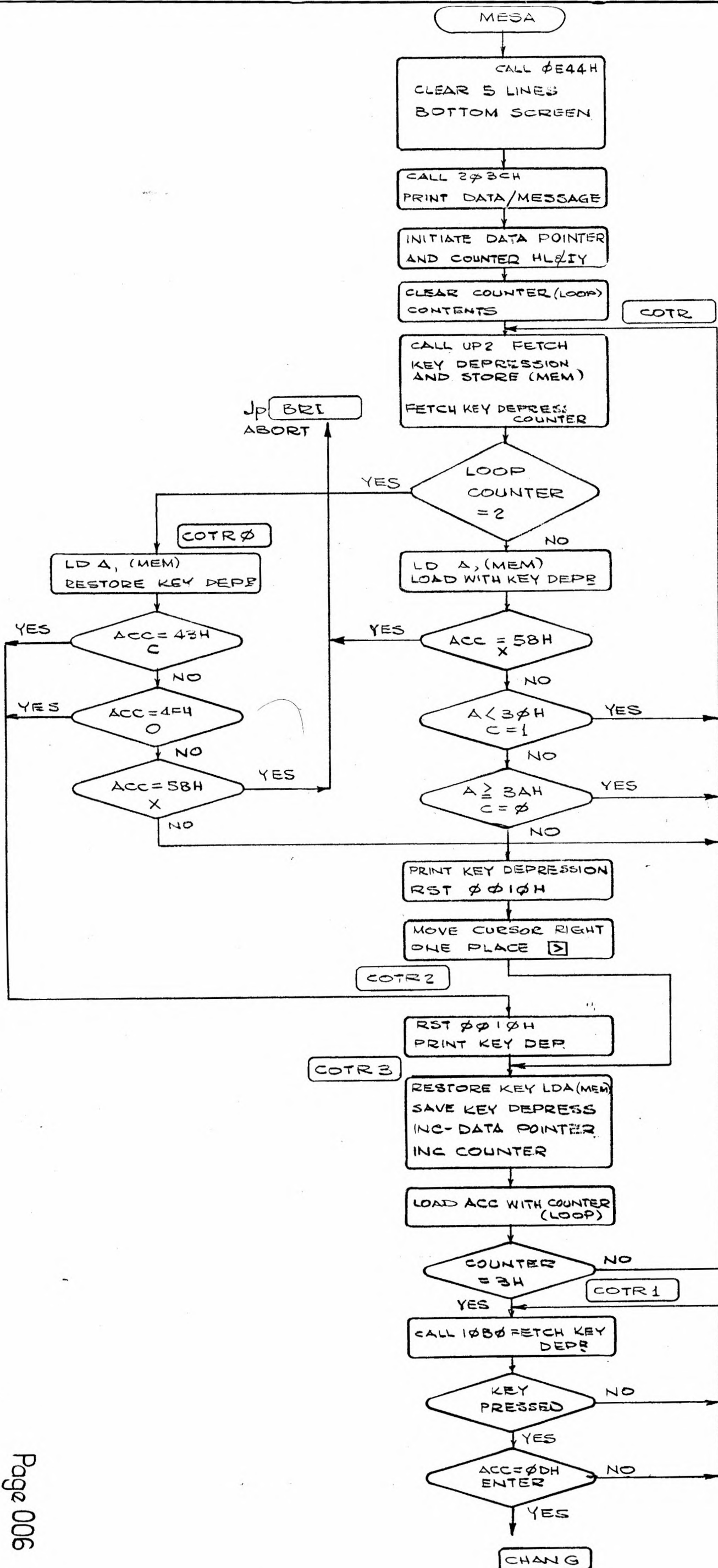


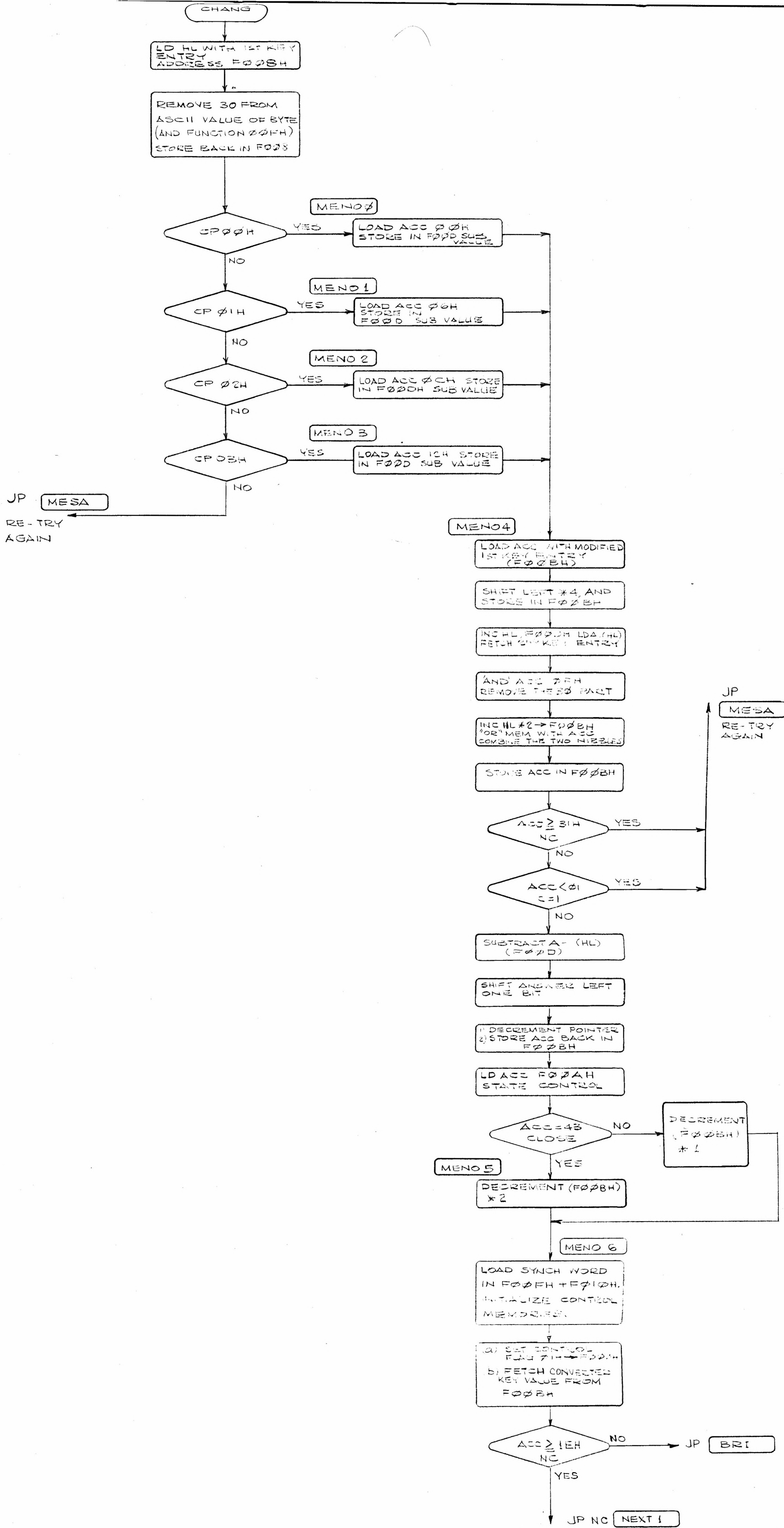


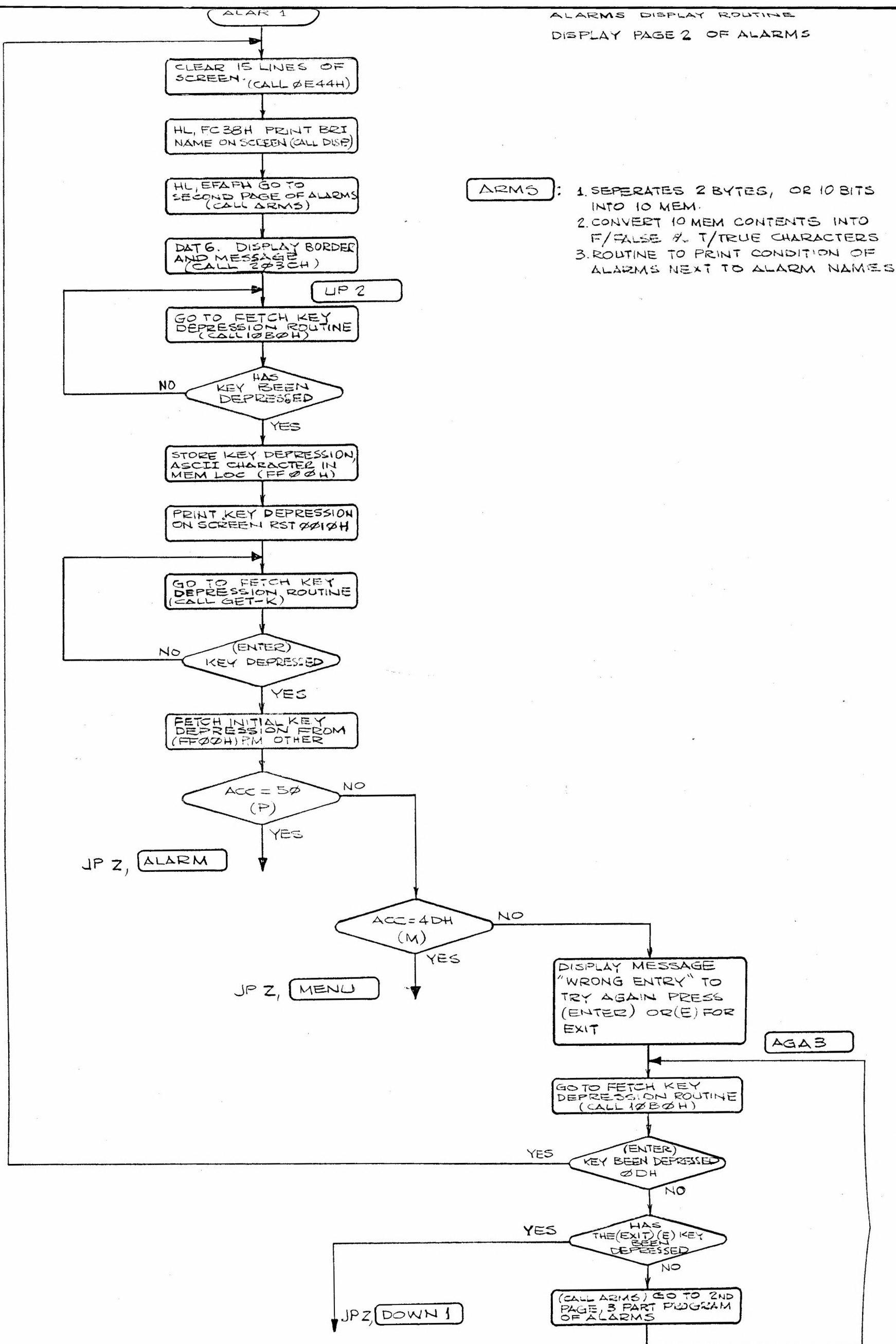


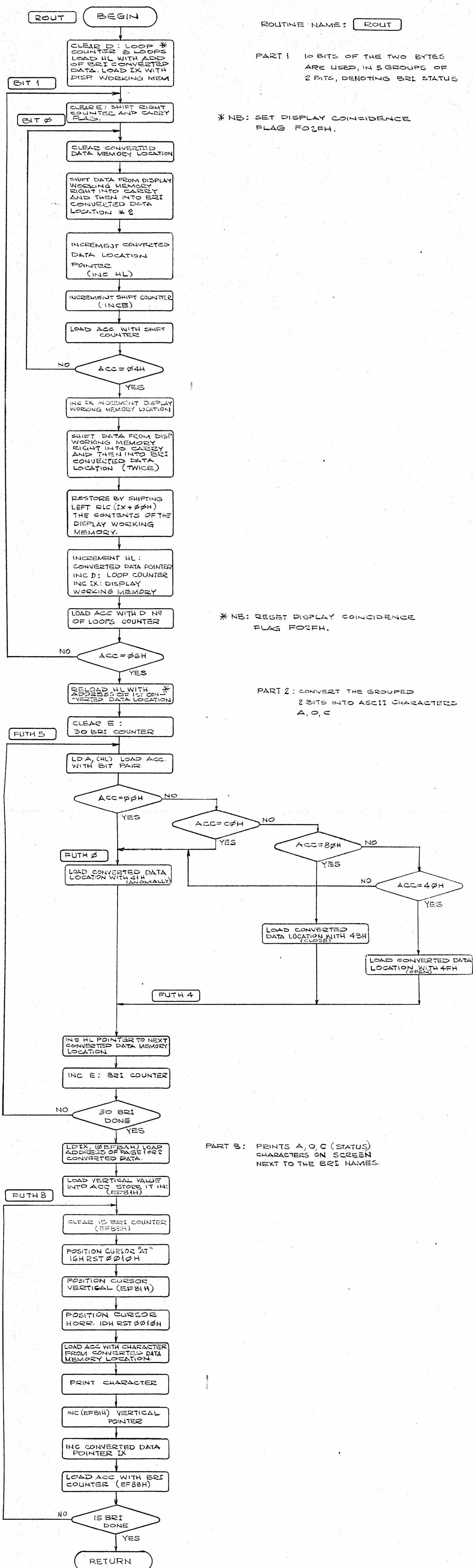
CONTROL INPUT ROUTINE

SELECT REQUIRED CONTROL NUMBER
AND STATE: O OR C OPEN/CLOSE





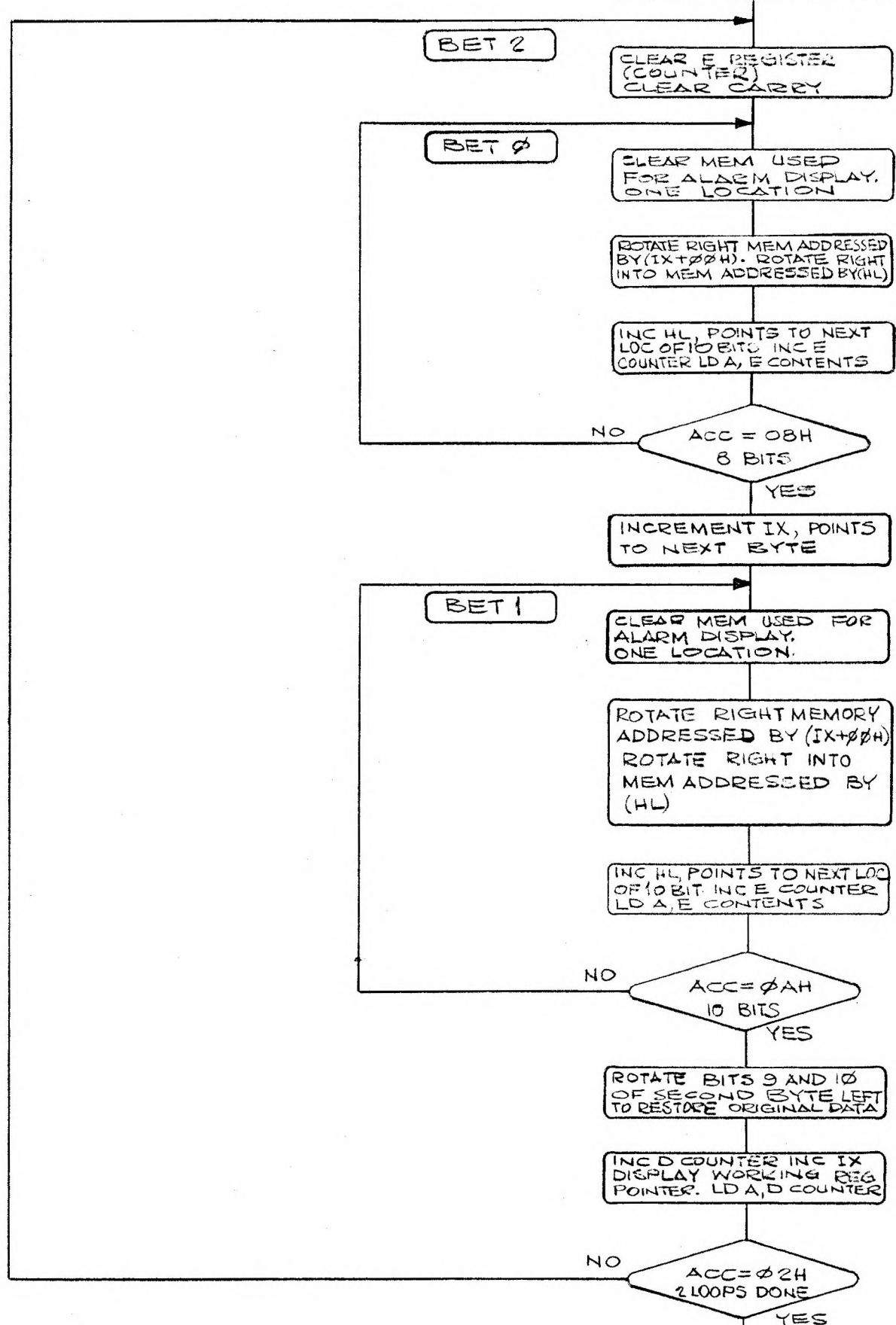




* N2: SET DISPLAY COINCIDENCE
FLAG F02FH

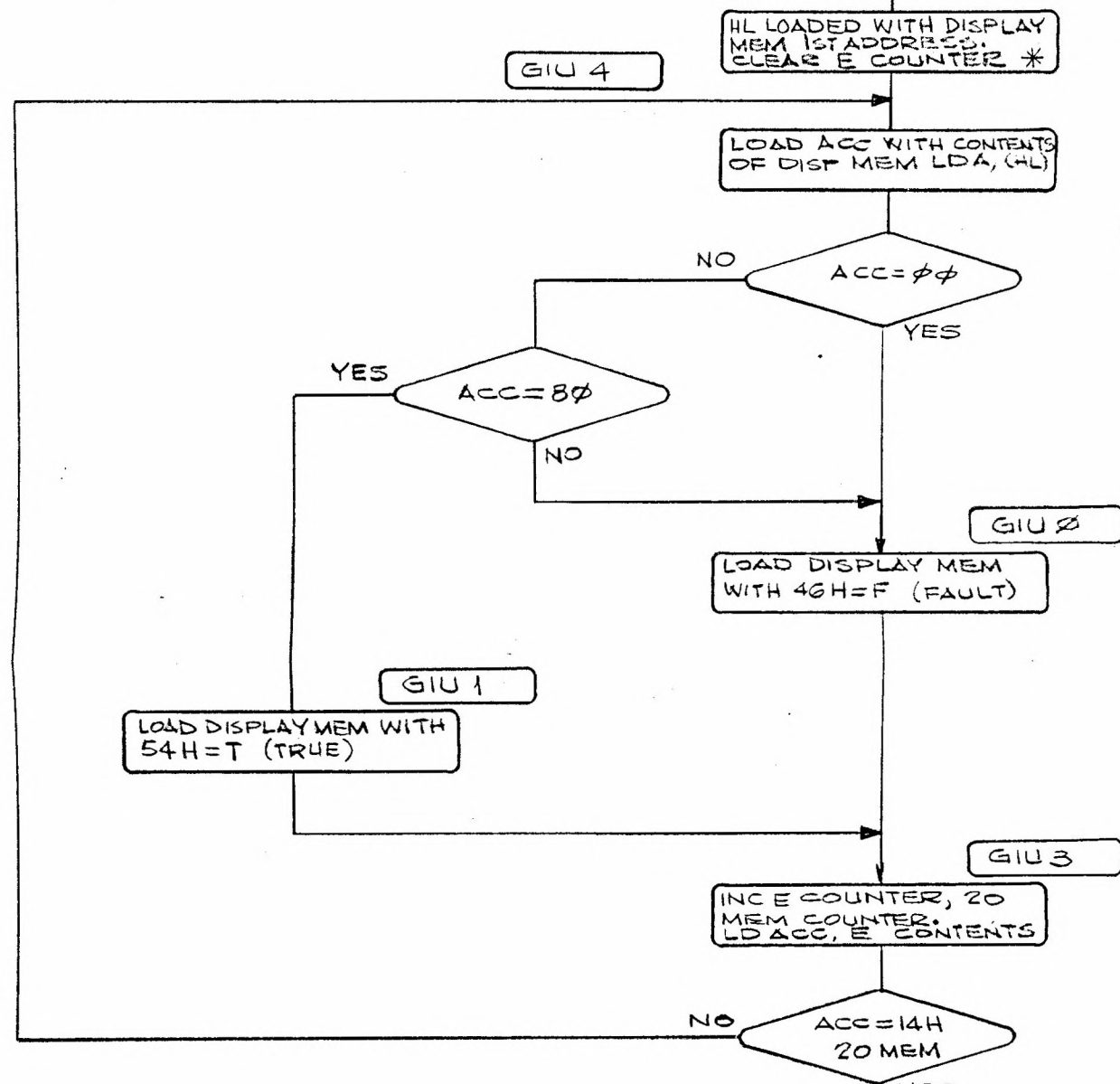
ARMED
BEGIN
CLEAR D REGISTER
LD HL, EFASH *
1ST LOCATION OF 10 BYTES
LDIX, EF0CH
1ST LOCAT ON OF 4BYTES
DISPLAY WORKING MEM

PART 1: SPLITS 10 BITS OF
2 BYTES INTO 10
MEMORY LOCATIONS

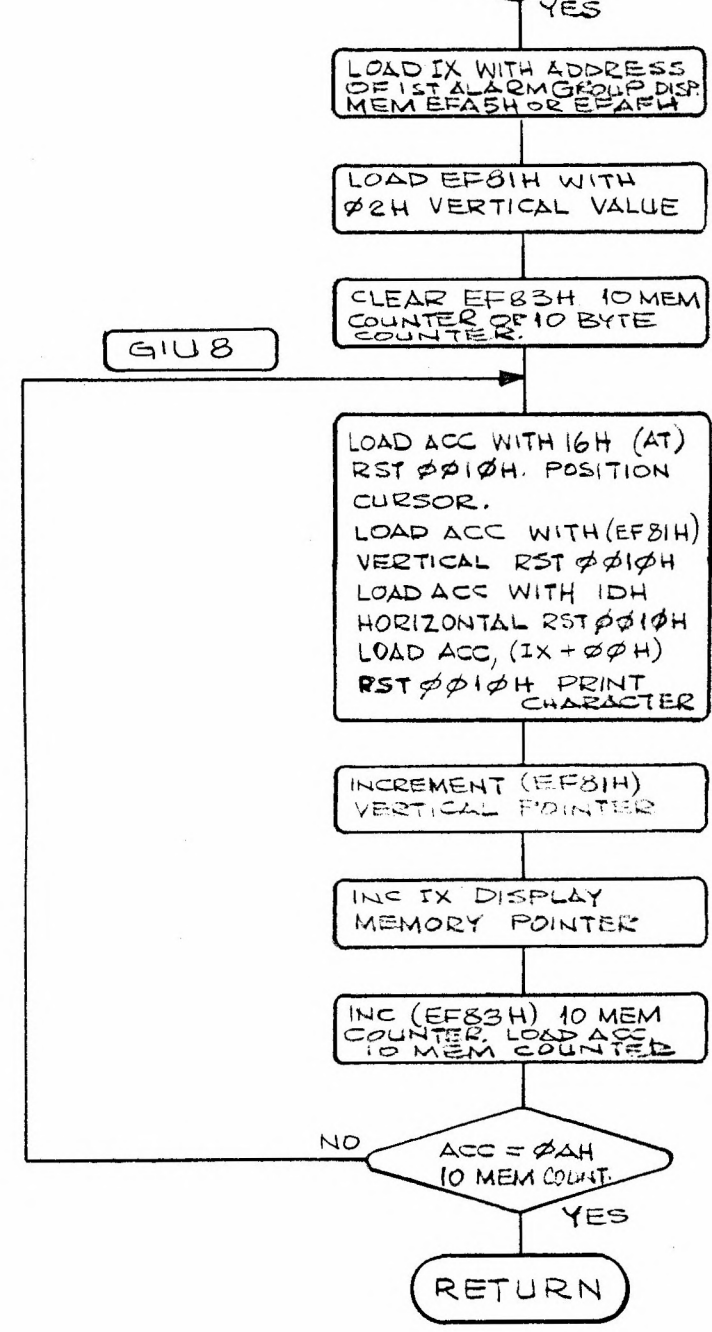


PART 2: CONVERTS DATA IN
THE 2 GROUPS OF
10 MEM INTO F/FALSE
T/TRUE CHARACTERS

* N3: RESET DISPLAY
COINCIDENCE
FLAG F02FH.



PART 3: PRINTS STATUS OF
ALARMS NEXT TO
ALARM NAMES.



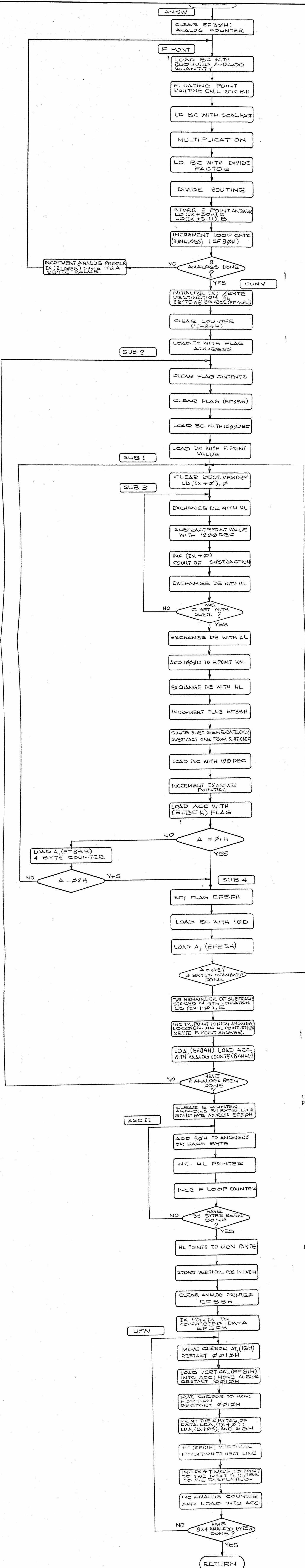
ANALOGUES FLOATING POINT ROUTINE

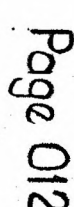
4 PART PROGRAM.
PART 1: FLOATING POINT
CALCULATOR ROUTINE
EF10 ~ EF1F RECEIVED BINARY VALUES
EF40 ~ EF4F PROCESSED DATA
EF5D ~ EF7C DISPLAY DATA

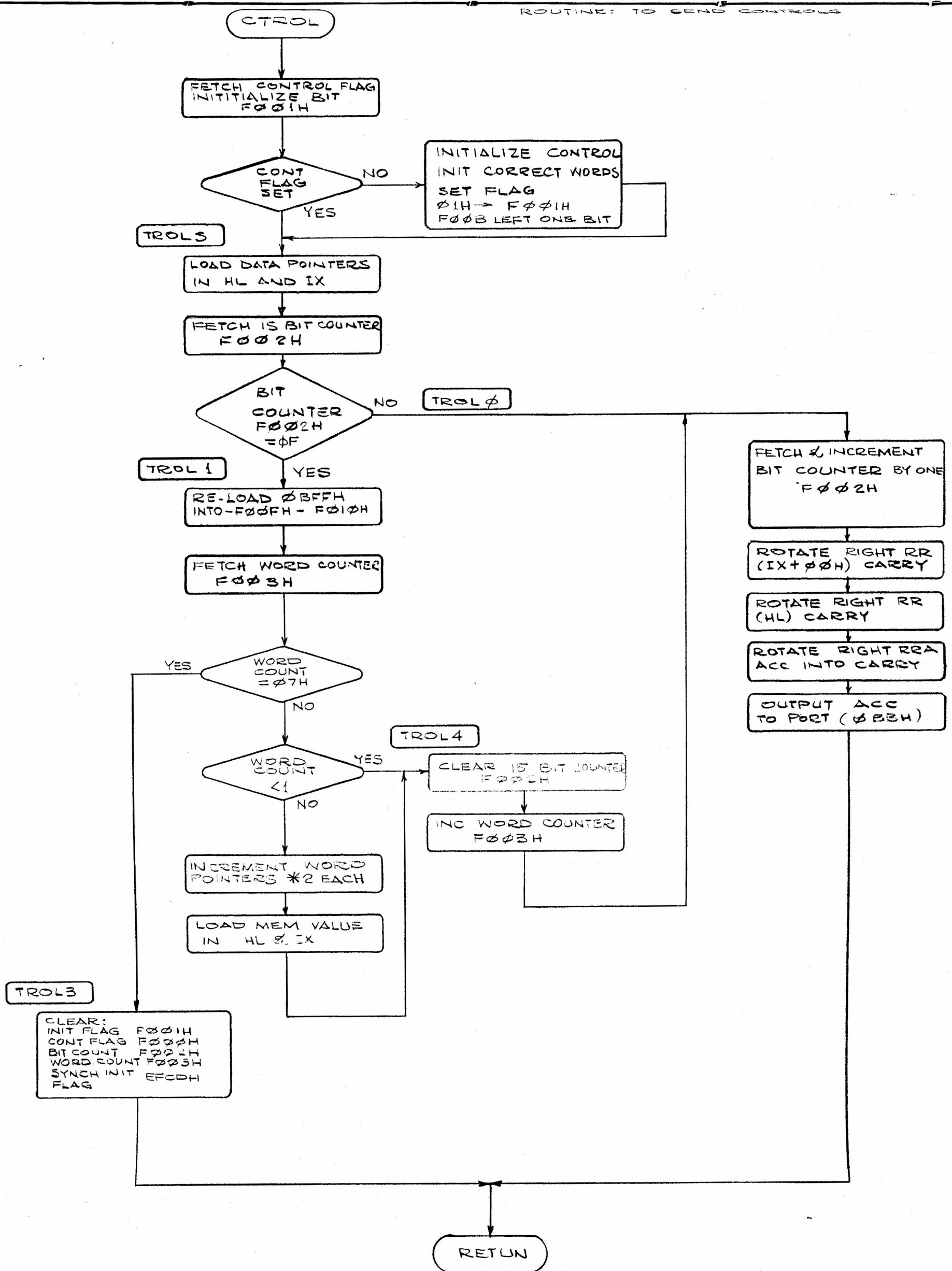
PART 2: CONVERT THE HEX
2 BYTE ANSWER INTO
4 BYTE VALUE

PART 3: CONVERT THE 8x4 BYTES
ANSWERS INTO ASCII
CHARACTERS FOR DISPLAY

PART 4: PRINT OUT ROUTINE
SIGN AND 4 BYTES
OF DATA.







14.0 INVESTIGATION, DEVELOPMENT APPROACH/CHANGES

The operation of the Selta remote was analyzed in great detail, a PM 3551A logic/timing analyzer was used to check timing details of the following signals:

- (a) Relationship between transmitted data and COS3 output strobe.
- (b) Relationship between transmitted data and received synch word.
- (c) Relationship between received data and COS 3 input strobe.
- (d) Timing relationship between control messages sent to the remote and transmitted data from the remote.

As stated earlier in the report a micro-based approach was used. The idea was to have a user friendly unit whose operation could be changed by making software modifications, this being much easier than making changes to a circuit board. Certain changes were made to the project. They are as follows:

- (a) Generation of $\overline{\text{NMI}}$ strobe pulses

In the original approach two $\overline{\text{NMI}}$ would be generated every 20m/sec, and additional hardware would have been used to simulate a "Status" register for the Z80 P.I.O., this register would flag the $\overline{\text{NMI}}$ for received data and the $\overline{\text{NMI}}$ for transmitted data.

The above was simplified by using only one $\overline{\text{NMI}}$ pulse to strobe incoming data, the "Status" register was discarded and a 4 m/sec software loop was used to delay the transmitted data to the remote.

- (b) Receiving and Transmitting data

The method of receiving/transmitting data was changed from an 8 bit approach to a 16 bit approach, this simplified the handling of received and transmitted data.

- (c) Sending of Remote Controls

The original approach was to send the following words:

- (i) 1 SYNCH WORD
- (ii) 9 PVX Words
- (iii) 1 TELEC word
- (iv) 1 GTC Word
- (v) 1 TC word

- (vi) 1 $\overline{\text{GTC}}$ word
- (vii) 1 $\overline{\text{TC}}$ word
- (viii) 1 SYNCH word

The above was changed slightly by sending only 1 PVX empty word, instead of 9 PVX words. The control time was decreased from 4.8 sec to 2.4 seconds. The control program was also shortened and simplified.

- (d) The design of the Interface card was changed from a circuit using various 555 timers to the present circuit.

In the original circuit synchronization would not be as good as the present method.

Synchronization was checked by the following methods.

- (i) A short routine was written to display the incoming data on the screen as "1" and "0".

The unit was allowed to run for a period of three hours, this is approximately 540 000 bits or 36 000 words. The bit pattern of the last message was checked and the data was correct.

- (ii) The incoming data was checked using a PM 3551A Logic/Timing analyzer on repetitive trigger, the $\overline{\text{NMI}}$ strobe pulse was always in the centre of the bit cell.

A better method was used to check the reliability of the incoming data, which will be explained later on.

- (e) Display coincidence detection flag.

The above flag had to be used for detecting coincidence between the data update occurring every 5.4 seconds in the program running under the control of the $\overline{\text{NMI}}$ and the program used to do calculation/-display. It was found that over a period of 1 hour an alarm status might give a wrong indication 2 or 3 times.

The coincidence flag prevents update to take place during the right shift occurring in the main body of the program "Selta*13".

15.0 RELIABILITY TESTS

(a) Controls:

A total of 250 controls were sent to the remote with a 100% execution, no controls were lost.

(b) Displayed data:

It was found that displayed data, alarms and B.R.I. but not analogue quantities would change at random on the screen. This would occur approximately 6 times in one hour lasting a total of 5.4 seconds.

It was found that the update transfer from the input serial data temporary store occurring every 5.4 seconds under the control of the NMI, would clash with a right shift of memory contents occurring in the ARMS and ROUT routines.

The program was changed and a display coincidence flag was inserted to overcome the above problem.

To check the reliability some small temporary changes were made to the program as follows:

- (i) Compare routine was inserted to compare the data of the input serial data temporary store memory and the previous update stored in the working display memory.
- (ii) A counter was initialized to count the number of changes if any, detected between the two memories.

The program was allowed to run for a total of 10.5 hours and the counter (FO2AH) contents were checked at the end of this time. No errors had been experienced, thus 100% accuracy in the reception of data is obtained between the Selta Test set and the remote.

- (iii) The test set was used with various remotes and cards were interchanged, no faulty operations were detected.

16.0 ATTAINMENT OF PROJECT OBJECTIVES

The unit displays breaker return indications, alarms and analogue values in a user friendly mode. It is capable of sending remote controls, is easy to maintain and reliable in it's operation.

Certain minor modifications had to be implemented to obtain the original set objectives.

All changes made contributed to a better operation of the test set.

17.0 SUGGESTIONS MADE FOR IMPROVING THE TEST SET.

- (a) Decimal point could be inserted in the displayed analogue quantities.
- (b) A routine displaying data received from the remote in binary form, could be included as part of the main program. This routine could be useful in determining transmission faults with the remote.
- (c) A short routine generating a square wave could be very useful for adjusting the mark/space ratio of the Rx modem.
- (d) A data recorder could be used in place of the micro drive.
- (e) Improvement to the input key detection routine.

A slight improvement could be made to the input routine by adding a key "filter".

Changes are as follows:

CHANGE TO:

LINE

400 Top Call IMPR
 LD A, (MEM)
 RST 0010H

CHANGE TO:

LINE

1355 Up 2 Call IMPR
 RET

ADD TO PROGRAM:

IMPR Call 10BOH
 JR NC, IMPR
 CP 2FH
 JP C, IMPR
 LD (MEM), A
 RET

APPENDIX

Table of Selta words (10 bits of data and their 5 check bits)	105
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Z80 P.I.O.	146
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TABLE OF POSSIBLE SELTA WORDS

The table on the following pages shows the following:

- (a) All the combinations possible with the 10 bits of data sent in a word, (without the 5 check bits). These are called BIT UTILI = USEFUL BITS.
- (b) The 5 bit check of the above 0-1023 combinations, called CODICE CICLICO = CYCLIC CODE.
- (c) The modified 5 bit check of the above 0-1023 combinations, different to the cyclic code if the 10 bits of data represents information. Called CODICE INFORMAZ = INFORMATION CODE.
- (d) The modified 5 bit check of the above 0-1023 combinations, different to the cyclic code if the 10 bits of data represents a service word. Called CODICE SERVIZIO = SERVICE CODE.

The given table was used to obtain our Control data words TC and $\overline{TC}$, stored in memory locations E000H to E0EFH.

NB: TC and $\overline{TC}$ are information words.

SYNCH and TELEC are service words.

GTC and $\overline{GTC}$ are information words.

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0000	: 0000000000	00	: 00000	04	: 00100	23	: 10111
0001	: 0000000001	21	: 10101	17	: 10001	02	: 00010
0002	: 0000000010	31	: 11111	27	: 11011	08	: 01000
0003	: 0000000011	10	: 01010	14	: 01110	29	: 11101
0004	: 0000000100	11	: 01011	15	: 01111	28	: 11100
0005	: 0000000101	30	: 11110	26	: 11010	09	: 01001
0006	: 0000000110	20	: 10100	16	: 10000	03	: 00011
0007	: 0000000111	01	: 00001	05	: 00101	22	: 10110
0008	: 0000001000	22	: 10110	18	: 10010	01	: 00001
0009	: 0000001001	03	: 00011	07	: 00111	20	: 10100
0010	: 0000001010	09	: 01001	13	: 01101	30	: 11110
0011	: 0000001011	28	: 11100	24	: 11000	11	: 01011
0012	: 0000001100	29	: 11101	25	: 11001	10	: 01010
0013	: 0000001101	08	: 01000	12	: 01100	31	: 11111
0014	: 0000001110	02	: 00010	06	: 00110	21	: 10101
0015	: 0000001111	23	: 10111	19	: 10011	00	: 00000
0016	: 0000010000	25	: 11001	29	: 11101	14	: 01110
0017	: 0000010001	12	: 01100	03	: 01000	27	: 11011
0018	: 0000010010	06	: 00110	02	: 00010	17	: 10001
0019	: 0000010011	19	: 10011	23	: 10111	04	: 00100
0020	: 0000010100	18	: 10010	22	: 10110	05	: 00101
0021	: 0000010101	07	: 00111	03	: 00011	16	: 10000
0022	: 0000010110	13	: 01101	09	: 01001	26	: 11010
0023	: 0000010111	24	: 11000	23	: 11100	15	: 01111
0024	: 0000011000	15	: 01111	11	: 01011	24	: 11000
0025	: 0000011001	26	: 11010	30	: 11110	13	: 01101
0026	: 0000011010	16	: 10000	20	: 10100	07	: 00111
0027	: 0000011011	05	: 00101	01	: 00001	18	: 10010
0028	: 0000011100	04	: 00100	00	: 00000	19	: 10011
0029	: 0000011101	17	: 10001	21	: 10101	06	: 00110
0030	: 0000011110	27	: 11011	31	: 11111	12	: 01100
0031	: 0000011111	14	: 01110	10	: 01010	25	: 11001

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0032	: 0000100000	07	: 00111	03	: 00011	16	: 10000
0033	: 0000100001	18	: 10010	22	: 10110	05	: 00101
0034	: 0000100010	24	: 11000	28	: 11100	15	: 01111
0035	: 0000100011	13	: 01101	09	: 01001	26	: 11010
0036	: 0000100100	12	: 01100	08	: 01000	27	: 11011
0037	: 0000100101	25	: 11001	29	: 11101	14	: 01110
0038	: 0000100110	19	: 10011	23	: 10111	04	: 00100
0039	: 0000100111	06	: 00110	02	: 00010	17	: 10001
0040	: 0000101000	17	: 10001	21	: 10101	06	: 00110
0041	: 0000101001	04	: 00100	00	: 00000	19	: 10011
0042	: 0000101010	14	: 01110	10	: 01010	25	: 11001
0043	: 0000101011	27	: 11011	31	: 11111	12	: 01100
0044	: 0000101100	26	: 11010	30	: 11110	13	: 01101
0045	: 0000101101	15	: 01111	11	: 01011	24	: 11000
0046	: 0000101110	05	: 00101	01	: 00001	18	: 10010
0047	: 0000101111	16	: 10000	20	: 10100	07	: 00111
0048	: 0000110000	30	: 11110	26	: 11010	09	: 01001
0049	: 0000110001	11	: 01011	15	: 01111	28	: 11100
0050	: 0000110010	01	: 00001	05	: 00101	22	: 10110
0051	: 0000110011	20	: 10100	16	: 10000	03	: 00011
0052	: 0000110100	21	: 10101	17	: 10001	02	: 00010
0053	: 0000110101	00	: 00000	04	: 00100	23	: 10111
0054	: 0000110110	10	: 01010	14	: 01110	29	: 11101
0055	: 0000110111	31	: 11111	27	: 11011	08	: 01000
0056	: 0000111000	08	: 01000	12	: 01100	31	: 11111
0057	: 0000111001	29	: 11101	25	: 11001	10	: 01010
0058	: 0000111010	23	: 10111	19	: 10011	00	: 00000
0059	: 0000111011	02	: 00010	06	: 00110	21	: 10101
0060	: 0000111100	03	: 00011	07	: 00111	20	: 10100
0061	: 0000111101	22	: 10110	18	: 10010	01	: 00001
0062	: 0000111110	28	: 11100	24	: 11000	11	: 01011
0063	: 0000111111	09	: 01001	13	: 01101	30	: 11110

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0064	: 0001000000	14	: 01110	10	: 01010	25	: 11001
0065	: 0001000001	27	: 11011	31	: 11111	12	: 01100
0066	: 0001000010	17	: 10001	21	: 10101	06	: 00110
0067	: 0001000011	04	: 00100	00	: 00000	19	: 10011
0068	: 0001000100	05	: 00101	01	: 00001	18	: 10010
0069	: 0001000101	16	: 10000	20	: 10100	07	: 00111
0070	: 0001000110	26	: 11010	30	: 11110	13	: 01101
0071	: 0001000111	15	: 01111	11	: 01011	24	: 11000
0072	: 0001001000	24	: 11000	28	: 11100	15	: 01111
0073	: 0001001001	13	: 01101	09	: 01001	26	: 11010
0074	: 0001001010	07	: 00111	03	: 00011	16	: 10000
0075	: 0001001011	18	: 10010	22	: 10110	05	: 00101
0076	: 0001001100	19	: 10011	23	: 10111	04	: 00100
0077	: 0001001101	06	: 00110	02	: 00010	17	: 10001
0078	: 0001001110	12	: 01100	08	: 01000	27	: 11011
0079	: 0001001111	25	: 11001	29	: 11101	14	: 01110
0080	: 0001010000	23	: 10111	19	: 10011	00	: 00000
0081	: 0001010001	02	: 00010	06	: 00110	21	: 10101
0082	: 0001010010	08	: 01000	12	: 01100	31	: 11111
0083	: 0001010011	29	: 11101	25	: 11001	10	: 01010
0084	: 0001010100	28	: 11100	24	: 11000	11	: 01011
0085	: 0001010101	09	: 01001	13	: 01101	30	: 11110
0086	: 0001010110	03	: 00011	07	: 00111	20	: 10100
0087	: 0001010111	22	: 10110	18	: 10010	01	: 00001
0088	: 0001011000	01	: 00001	05	: 00101	22	: 10110
0089	: 0001011001	20	: 10100	16	: 10000	03	: 00011
0090	: 0001011010	30	: 11110	26	: 11010	09	: 01001
0091	: 0001011011	11	: 01011	15	: 01111	28	: 11100
0092	: 0001011100	10	: 01010	14	: 01110	29	: 11101
0093	: 0001011101	31	: 11111	27	: 11011	08	: 01000
0094	: 0001011110	21	: 10101	17	: 10001	02	: 00010
0095	: 0001011111	00	: 00000	04	: 00100	23	: 10111

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0096	: 0001100000	09	: 01001	13	: 01101	30	: 11110
0097	: 0001100001	28	: 11100	24	: 11000	11	: 01011
0098	: 0001100010	22	: 10110	18	: 10010	01	: 00001
0099	: 0001100011	03	: 00011	07	: 00111	20	: 10100
0100	: 0001100100	02	: 00010	06	: 00110	21	: 10101
0101	: 0001100101	23	: 10111	19	: 10011	00	: 00000
0102	: 0001100110	29	: 11101	25	: 11001	10	: 01010
0103	: 0001100111	08	: 01000	12	: 01100	31	: 11111
0104	: 0001101000	31	: 11111	27	: 11011	08	: 01000
0105	: 0001101001	10	: 01010	14	: 01110	29	: 11101
0106	: 0001101010	00	: 00000	04	: 00100	23	: 10111
0107	: 0001101011	21	: 10101	17	: 10001	02	: 00010
0108	: 0001101100	20	: 10100	16	: 10000	03	: 00011
0109	: 0001101101	01	: 00001	05	: 00101	22	: 10110
0110	: 0001101110	11	: 01011	15	: 01111	28	: 11100
0111	: 0001101111	30	: 11110	26	: 11010	09	: 01001
0112	: 0001110000	16	: 10000	20	: 10100	07	: 00111
0113	: 0001110001	05	: 00101	01	: 00001	18	: 10010
0114	: 0001110010	15	: 01111	11	: 01011	24	: 11000
0115	: 0001110011	26	: 11010	30	: 11110	13	: 01101
0116	: 0001110100	27	: 11011	31	: 11111	12	: 01100
0117	: 0001110101	14	: 01110	10	: 01010	25	: 11001
0118	: 0001110110	04	: 00100	00	: 00000	19	: 10011
0119	: 0001110111	17	: 10001	21	: 10101	06	: 00110
0120	: 0001111000	06	: 00110	02	: 00010	17	: 10001
0121	: 0001111001	19	: 10011	23	: 10111	04	: 00100
0122	: 0001111010	25	: 11001	29	: 11101	14	: 01110
0123	: 0001111011	12	: 01100	08	: 01000	27	: 11011
0124	: 0001111100	13	: 01101	09	: 01001	26	: 11010
0125	: 0001111101	24	: 11000	28	: 11100	15	: 01111
0126	: 0001111110	18	: 10010	22	: 10110	05	: 00101
0127	: 0001111111	07	: 00111	03	: 00011	16	: 10000

#	BIT UTILI	#	CODICE	#	CODICE	#	CODICE	#
#		#	CICLICO	#	INFORMAZ.	#	SERVIZIO	#
#	DEC BIN	#	DEC BIN	#	DEC BIN	#	DEC BIN	#
#	0128 : 0010000000	#	28 : 11100	#	24 : 11000	#	11 : 01011	#
#	0129 : 0010000001	#	09 : 01001	#	13 : 01101	#	30 : 11110	#
#	0130 : 0010000010	#	03 : 00011	#	07 : 00111	#	20 : 10100	#
#	0131 : 0010000011	#	22 : 10110	#	18 : 10010	#	01 : 00001	#
#	0132 : 0010000100	#	23 : 10111	#	19 : 10011	#	00 : 00000	#
#	0133 : 0010000101	#	02 : 00010	#	06 : 00110	#	21 : 10101	#
#	0134 : 0010000110	#	08 : 01000	#	12 : 01100	#	31 : 11111	#
#	0135 : 0010000111	#	29 : 11101	#	25 : 11001	#	10 : 01010	#
#	0136 : 0010001000	#	10 : 01010	#	14 : 01110	#	29 : 11101	#
#	0137 : 0010001001	#	31 : 11111	#	27 : 11011	#	08 : 01000	#
#	0138 : 0010001010	#	21 : 10101	#	17 : 10001	#	02 : 00010	#
#	0139 : 0010001011	#	00 : 00000	#	04 : 00100	#	23 : 10111	#
#	0140 : 0010001100	#	01 : 00001	#	05 : 00101	#	22 : 10110	#
#	0141 : 0010001101	#	20 : 10100	#	16 : 10000	#	03 : 00011	#
#	0142 : 0010001110	#	30 : 11110	#	26 : 11010	#	09 : 01001	#
#	0143 : 0010001111	#	11 : 01011	#	15 : 01111	#	28 : 11100	#
#	0144 : 0010010000	#	05 : 00101	#	01 : 00001	#	18 : 10010	#
#	0145 : 0010010001	#	16 : 10000	#	20 : 10100	#	07 : 00111	#
#	0146 : 0010010010	#	26 : 11010	#	30 : 11110	#	13 : 01101	#
#	0147 : 0010010011	#	15 : 01111	#	11 : 01011	#	24 : 11000	#
#	0148 : 0010010100	#	14 : 01110	#	10 : 01010	#	25 : 11001	#
#	0149 : 0010010101	#	27 : 11011	#	31 : 11111	#	12 : 01100	#
#	0150 : 0010010110	#	17 : 10001	#	21 : 10101	#	06 : 00110	#
#	0151 : 0010010111	#	04 : 00100	#	00 : 00000	#	19 : 10011	#
#	0152 : 0010011000	#	19 : 10011	#	23 : 10111	#	04 : 00100	#
#	0153 : 0010011001	#	06 : 00110	#	02 : 00010	#	17 : 10001	#
#	0154 : 0010011010	#	12 : 01100	#	08 : 01000	#	27 : 11011	#
#	0155 : 0010011011	#	25 : 11001	#	29 : 11101	#	14 : 01110	#
#	0156 : 0010011100	#	24 : 11000	#	28 : 11100	#	15 : 01111	#
#	0157 : 0010011101	#	13 : 01101	#	09 : 01001	#	26 : 11010	#
#	0158 : 0010011110	#	07 : 00111	#	03 : 00011	#	16 : 10000	#
#	0159 : 0010011111	#	18 : 10010	#	22 : 10110	#	05 : 00101	#

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	EIN	DEC	EIN	DEC	EIN	DEC	EIN
0160	: 0010100000	27	: 11011	31	: 11111	12	: 01100
0161	: 0010100001	14	: 01110	10	: 01010	25	: 11001
0162	: 0010100010	04	: 00100	00	: 00000	19	: 10011
0163	: 0010100011	17	: 10001	21	: 10101	06	: 00110
0164	: 0010100100	16	: 10000	20	: 10100	07	: 00111
0165	: 0010100101	05	: 00101	01	: 00001	18	: 10010
0166	: 0010100110	15	: 01111	11	: 01011	24	: 11000
0167	: 0010100111	26	: 11010	30	: 11110	13	: 01101
0168	: 0010101000	13	: 01101	09	: 01001	26	: 11010
0169	: 0010101001	24	: 11000	23	: 11100	15	: 01111
0170	: 0010101010	18	: 10010	22	: 10110	05	: 00101
0171	: 0010101011	07	: 00111	03	: 00011	16	: 10000
0172	: 0010101100	06	: 00110	02	: 00010	17	: 10001
0173	: 0010101101	19	: 10011	23	: 10111	04	: 00100
0174	: 0010101110	25	: 11001	29	: 11101	14	: 01110
0175	: 0010101111	12	: 01100	08	: 01000	27	: 11011
0176	: 0010110000	02	: 00010	06	: 00110	21	: 10101
0177	: 0010110001	23	: 10111	19	: 10011	00	: 00000
0178	: 0010110010	29	: 11101	25	: 11001	10	: 01010
0179	: 0010110011	08	: 01000	12	: 01100	31	: 11111
0180	: 0010110100	09	: 01001	13	: 01101	30	: 11110
0181	: 0010110101	28	: 11100	24	: 11000	11	: 01011
0182	: 0010110110	22	: 10110	18	: 10010	01	: 00001
0183	: 0010110111	03	: 00011	07	: 00111	20	: 10100
0184	: 0010111000	20	: 10100	16	: 10000	03	: 00011
0185	: 0010111001	01	: 00001	05	: 00101	22	: 10110
0186	: 0010111010	11	: 01011	15	: 01111	28	: 11100
0187	: 0010111011	30	: 11110	26	: 11010	09	: 01001
0188	: 0010111100	31	: 11111	27	: 11011	08	: 01000
0189	: 0010111101	10	: 01010	14	: 01110	29	: 11101
0190	: 0010111110	00	: 00000	04	: 00100	23	: 10111
0191	: 0010111111	21	: 10101	17	: 10001	02	: 00010

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0192	: 0011000000	18	: 10010	22	: 10110	05	: 00101
0193	: 0011000001	07	: 00111	03	: 00011	16	: 10000
0194	: 0011000010	13	: 01101	09	: 01001	26	: 11010
0195	: 0011000011	24	: 11000	28	: 11100	15	: 01111
0196	: 0011000100	25	: 11001	29	: 11101	14	: 01110
0197	: 0011000101	12	: 01100	08	: 01000	27	: 11011
0198	: 0011000110	06	: 00110	02	: 00010	17	: 10001
0199	: 0011000111	19	: 10011	23	: 10111	04	: 00100
0200	: 0011001000	04	: 00100	00	: 00000	19	: 10011
0201	: 0011001001	17	: 10001	21	: 10101	06	: 00110
0202	: 0011001010	27	: 11011	31	: 11111	12	: 01100
0203	: 0011001011	14	: 01110	10	: 01010	25	: 11001
0204	: 0011001100	15	: 01111	11	: 01011	24	: 11000
0205	: 0011001101	26	: 11010	30	: 11110	13	: 01101
0206	: 0011001110	16	: 10000	20	: 10100	07	: 00111
0207	: 0011001111	05	: 00101	01	: 00001	18	: 10010
0208	: 0011010000	11	: 01011	15	: 01111	28	: 11100
0209	: 0011010001	30	: 11110	26	: 11010	09	: 01001
0210	: 0011010010	20	: 10100	16	: 10000	03	: 00011
0211	: 0011010011	01	: 00001	05	: 00101	22	: 10110
0212	: 0011010100	00	: 00000	04	: 00100	23	: 10111
0213	: 0011010101	21	: 10101	17	: 10001	02	: 00010
0214	: 0011010110	31	: 11111	27	: 11011	08	: 01000
0215	: 0011010111	10	: 01010	14	: 01110	29	: 11101
0216	: 0011011000	29	: 11101	25	: 11001	10	: 01010
0217	: 0011011001	08	: 01000	12	: 01100	31	: 11111
0218	: 0011011010	02	: 00010	06	: 00110	21	: 10101
0219	: 0011011011	23	: 10111	19	: 10011	00	: 00000
0220	: 0011011100	22	: 10110	18	: 10010	01	: 00001
0221	: 0011011101	03	: 00011	07	: 00111	20	: 10100
0222	: 0011011110	09	: 01001	13	: 01101	30	: 11110
0223	: 0011011111	28	: 11100	24	: 11000	11	: 01011

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
# 0224 :	0011100000	# 21 :	10101	# 17 :	10001	# 02 :	00010
# 0225 :	0011100001	# 00 :	00000	# 04 :	00100	# 23 :	10111
# 0226 :	0011100010	# 10 :	01010	# 14 :	01110	# 29 :	11101
# 0227 :	0011100011	# 31 :	11111	# 27 :	11011	# 08 :	01000
# 0228 :	0011100100	# 30 :	11110	# 26 :	11010	# 09 :	01001
# 0229 :	0011100101	# 11 :	01011	# 15 :	01111	# 28 :	11100
# 0230 :	0011100110	# 01 :	00001	# 05 :	00101	# 22 :	10110
# 0231 :	0011100111	# 20 :	10100	# 16 :	10000	# 03 :	00011
# 0232 :	0011101000	# 03 :	00011	# 07 :	00111	# 20 :	10100
# 0233 :	0011101001	# 22 :	10110	# 18 :	10010	# 01 :	00001
# 0234 :	0011101010	# 28 :	11100	# 24 :	11000	# 11 :	01011
# 0235 :	0011101011	# 09 :	01001	# 13 :	01101	# 30 :	11110
# 0236 :	0011101100	# 08 :	01000	# 12 :	01100	# 31 :	11111
# 0237 :	0011101101	# 29 :	11101	# 25 :	11001	# 10 :	01010
# 0238 :	0011101110	# 23 :	10111	# 19 :	10011	# 00 :	00000
# 0239 :	0011101111	# 02 :	00010	# 06 :	00110	# 21 :	10101
# 0240 :	0011110000	# 12 :	01100	# 08 :	01000	# 27 :	11011
# 0241 :	0011110001	# 25 :	11001	# 29 :	11101	# 14 :	01110
# 0242 :	0011110010	# 19 :	10011	# 23 :	10111	# 04 :	00100
# 0243 :	0011110011	# 06 :	00110	# 02 :	00010	# 17 :	10001
# 0244 :	0011110100	# 07 :	00111	# 03 :	00011	# 16 :	10000
# 0245 :	0011110101	# 18 :	10010	# 22 :	10110	# 05 :	00101
# 0246 :	0011110110	# 24 :	11000	# 28 :	11100	# 15 :	01111
# 0247 :	0011110111	# 13 :	01101	# 09 :	01001	# 26 :	11010
# 0248 :	0011111000	# 26 :	11010	# 30 :	11110	# 13 :	01101
# 0249 :	0011111001	# 15 :	01111	# 11 :	01011	# 24 :	11000
# 0250 :	0011111010	# 05 :	00101	# 01 :	00001	# 18 :	10010
# 0251 :	0011111011	# 16 :	10000	# 20 :	10100	# 07 :	00111
# 0252 :	0011111100	# 17 :	10001	# 21 :	10101	# 06 :	00110
# 0253 :	0011111101	# 04 :	00100	# 00 :	00000	# 19 :	10011
# 0254 :	0011111110	# 14 :	01110	# 10 :	01010	# 25 :	11001
# 0255 :	0011111111	# 27 :	11011	# 31 :	11111	# 12 :	01100

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0256	: 0100000000	13	: 01101	09	: 01001	26	: 11010
0257	: 0100000001	24	: 11000	28	: 11100	15	: 01111
0258	: 0100000010	18	: 10010	22	: 10110	05	: 00101
0259	: 0100000011	07	: 00111	03	: 00011	16	: 10000
0260	: 0100000100	06	: 00110	02	: 00010	17	: 10001
0261	: 0100000101	19	: 10011	23	: 10111	04	: 00100
0262	: 0100000110	25	: 11001	29	: 11101	14	: 01110
0263	: 0100000111	12	: 01100	08	: 01000	27	: 11011
0264	: 0100001000	27	: 11011	31	: 11111	12	: 01100
0265	: 0100001001	14	: 01110	10	: 01010	25	: 11001
0266	: 0100001010	04	: 00100	00	: 00000	19	: 10011
0267	: 0100001011	17	: 10001	21	: 10101	06	: 00110
0268	: 0100001100	16	: 10000	20	: 10100	07	: 00111
0269	: 0100001101	05	: 00101	01	: 00001	18	: 10010
0270	: 0100001110	15	: 01111	11	: 01011	24	: 11000
0271	: 0100001111	26	: 11010	30	: 11110	13	: 01101
0272	: 0100010000	20	: 10100	16	: 10000	03	: 00011
0273	: 0100010001	01	: 00001	05	: 00101	22	: 10110
0274	: 0100010010	11	: 01011	15	: 01111	28	: 11100
0275	: 0100010011	30	: 11110	26	: 11010	09	: 01001
0276	: 0100010100	31	: 11111	27	: 11011	08	: 01000
0277	: 0100010101	10	: 01010	14	: 01110	29	: 11101
0278	: 0100010110	00	: 00000	04	: 00100	23	: 10111
0279	: 0100010111	21	: 10101	17	: 10001	02	: 00010
0280	: 0100011000	02	: 00010	06	: 00110	21	: 10101
0281	: 0100011001	23	: 10111	19	: 10011	00	: 00000
0282	: 0100011010	29	: 11101	25	: 11001	10	: 01010
0283	: 0100011011	08	: 01000	12	: 01100	31	: 11111
0284	: 0100011100	09	: 01001	13	: 01101	30	: 11110
0285	: 0100011101	28	: 11100	24	: 11000	11	: 01011
0286	: 0100011110	22	: 10110	18	: 10010	01	: 00001
0287	: 0100011111	03	: 00011	07	: 00111	20	: 10100

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0288	: 0100100000	10	: 01010	14	: 01110	29	: 11101
0289	: 0100100001	31	: 11111	27	: 11011	08	: 01000
0290	: 0100100010	21	: 10101	17	: 10001	02	: 00010
0291	: 0100100011	00	: 00000	04	: 00100	23	: 10111
0292	: 0100100100	01	: 00001	05	: 00101	22	: 10110
0293	: 0100100101	20	: 10100	16	: 10000	03	: 00011
0294	: 0100100110	30	: 11110	26	: 11010	09	: 01001
0295	: 0100100111	11	: 01011	15	: 01111	28	: 11100
0296	: 0100101000	28	: 11100	24	: 11000	11	: 01011
0297	: 0100101001	09	: 01001	13	: 01101	30	: 11110
0298	: 0100101010	03	: 00011	07	: 00111	20	: 10100
0299	: 0100101011	22	: 10110	18	: 10010	01	: 00001
0300	: 0100101100	23	: 10111	19	: 10011	00	: 00000
0301	: 0100101101	02	: 00010	06	: 00110	21	: 10101
0302	: 0100101110	08	: 01000	12	: 01100	31	: 11111
0303	: 0100101111	29	: 11101	25	: 11001	10	: 01010
0304	: 0100110000	19	: 10011	23	: 10111	04	: 00100
0305	: 0100110001	06	: 00110	02	: 00010	17	: 10001
0306	: 0100110010	12	: 01100	08	: 01000	27	: 11011
0307	: 0100110011	25	: 11001	29	: 11101	14	: 01110
0308	: 0100110100	24	: 11000	28	: 11100	15	: 01111
0309	: 0100110101	13	: 01101	09	: 01001	26	: 11010
0310	: 0100110110	07	: 00111	03	: 00011	16	: 10000
0311	: 0100110111	18	: 10010	22	: 10110	05	: 00101
0312	: 0100111000	05	: 00101	01	: 00001	18	: 10010
0313	: 0100111001	16	: 10000	20	: 10100	07	: 00111
0314	: 0100111010	26	: 11010	30	: 11110	13	: 01101
0315	: 0100111011	15	: 01111	11	: 01011	24	: 11000
0316	: 0100111100	14	: 01110	10	: 01010	25	: 11001
0317	: 0100111101	27	: 11011	31	: 11111	12	: 01100
0318	: 0100111110	17	: 10001	21	: 10101	06	: 00110
0319	: 0100111111	04	: 00100	00	: 00000	19	: 10011

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0320	: 0101000000	03	: 00011	07	: 00111	20	: 10100
0321	: 0101000001	22	: 10110	18	: 10010	01	: 00001
0322	: 0101000010	28	: 11100	24	: 11000	11	: 01011
0323	: 0101000011	09	: 01001	13	: 01101	30	: 11110
0324	: 0101000100	08	: 01000	12	: 01100	31	: 11111
0325	: 0101000101	29	: 11101	25	: 11001	10	: 01010
0326	: 0101000110	23	: 10111	19	: 10011	00	: 00000
0327	: 0101000111	02	: 00010	06	: 00110	21	: 10101
0328	: 0101001000	21	: 10101	17	: 10001	02	: 00010
0329	: 0101001001	00	: 00000	04	: 00100	23	: 10111
0330	: 0101001010	10	: 01010	14	: 01110	29	: 11101
0331	: 0101001011	31	: 11111	27	: 11011	08	: 01000
0332	: 0101001100	30	: 11110	26	: 11010	09	: 01001
0333	: 0101001101	11	: 01011	15	: 01111	28	: 11100
0334	: 0101001110	01	: 00001	05	: 00101	22	: 10110
0335	: 0101001111	20	: 10100	16	: 10000	03	: 00011
0336	: 0101010000	26	: 11010	30	: 11110	13	: 01101
0337	: 0101010001	15	: 01111	11	: 01011	24	: 11000
0338	: 0101010010	05	: 00101	01	: 00001	18	: 10010
0339	: 0101010011	16	: 10000	20	: 10100	07	: 00111
0340	: 0101010100	17	: 10001	21	: 10101	06	: 00110
0341	: 0101010101	04	: 00100	00	: 00000	19	: 10011
0342	: 0101010110	14	: 01110	10	: 01010	25	: 11001
0343	: 0101010111	27	: 11011	31	: 11111	12	: 01100
0344	: 0101011000	12	: 01100	08	: 01000	27	: 11011
0345	: 0101011001	25	: 11001	29	: 11101	14	: 01110
0346	: 0101011010	19	: 10011	23	: 10111	04	: 00100
0347	: 0101011011	06	: 00110	02	: 00010	17	: 10001
0348	: 0101011100	07	: 00111	03	: 00011	16	: 10000
0349	: 0101011101	18	: 10010	22	: 10110	05	: 00101
0350	: 0101011110	24	: 11000	28	: 11100	15	: 01111
0351	: 0101011111	13	: 01101	09	: 01001	26	: 11010

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0352	: 0101100000	04	: 00100	00	: 00000	19	: 10011
0353	: 0101100001	17	: 10001	21	: 10101	06	: 00110
0354	: 0101100010	27	: 11011	31	: 11111	12	: 01100
0355	: 0101100011	14	: 01110	10	: 01010	25	: 11001
0356	: 0101100100	15	: 01111	11	: 01011	24	: 11000
0357	: 0101100101	26	: 11010	30	: 11110	13	: 01101
0358	: 0101100110	16	: 10000	20	: 10100	07	: 00111
0359	: 0101100111	05	: 00101	01	: 00001	18	: 10010
0360	: 0101101000	18	: 10010	22	: 10110	05	: 00101
0361	: 0101101001	07	: 00111	03	: 00011	16	: 10000
0362	: 0101101010	13	: 01101	09	: 01001	26	: 11010
0363	: 0101101011	24	: 11000	28	: 11100	15	: 01111
0364	: 0101101100	25	: 11001	29	: 11101	14	: 01110
0365	: 0101101101	12	: 01100	08	: 01000	27	: 11011
0366	: 0101101110	06	: 00110	02	: 00010	17	: 10001
0367	: 0101101111	19	: 10011	23	: 10111	04	: 00100
0368	: 0101110000	29	: 11101	25	: 11001	10	: 01010
0369	: 0101110001	08	: 01000	12	: 01100	31	: 11111
0370	: 0101110010	02	: 00010	06	: 00110	21	: 10101
0371	: 0101110011	23	: 10111	19	: 10011	00	: 00000
0372	: 0101110100	22	: 10110	18	: 10010	01	: 00001
0373	: 0101110101	03	: 00011	07	: 00111	20	: 10100
0374	: 0101110110	09	: 01001	13	: 01101	30	: 11110
0375	: 0101110111	28	: 11100	24	: 11000	11	: 01011
0376	: 0101111000	11	: 01011	15	: 01111	28	: 11100
0377	: 0101111001	30	: 11110	26	: 11010	09	: 01001
0378	: 0101111010	20	: 10100	16	: 10000	03	: 00011
0379	: 0101111011	01	: 00001	05	: 00101	22	: 10110
0380	: 0101111100	00	: 00000	04	: 00100	23	: 10111
0381	: 0101111101	21	: 10101	17	: 10001	02	: 00010
0382	: 0101111110	31	: 11111	27	: 11011	08	: 01000
0383	: 0101111111	10	: 01010	14	: 01110	29	: 11101

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0384	: 0110000000	17	: 10001	21	: 10101	06	: 00110
0385	: 0110000001	04	: 00100	00	: 00000	19	: 10011
0386	: 0110000010	14	: 01110	10	: 01010	25	: 11001
0387	: 0110000011	27	: 11011	31	: 11111	12	: 01100
0388	: 0110000100	26	: 11010	30	: 11110	13	: 01101
0389	: 0110000101	15	: 01111	11	: 01011	24	: 11000
0390	: 0110000110	05	: 00101	01	: 00001	18	: 10010
0391	: 0110000111	16	: 10000	20	: 10100	07	: 00111
0392	: 0110001000	07	: 00111	03	: 00011	16	: 10000
0393	: 0110001001	18	: 10010	22	: 10110	05	: 00101
0394	: 0110001010	24	: 11000	28	: 11100	15	: 01111
0395	: 0110001011	13	: 01101	09	: 01001	26	: 11010
0396	: 0110001100	12	: 01100	08	: 01000	27	: 11011
0397	: 0110001101	25	: 11001	29	: 11101	14	: 01110
0398	: 0110001110	19	: 10011	23	: 10111	04	: 00100
0399	: 0110001111	06	: 00110	02	: 00010	17	: 10001
0400	: 0110010000	08	: 01000	12	: 01100	31	: 11111
0401	: 0110010001	29	: 11101	25	: 11001	10	: 01010
0402	: 0110010010	23	: 10111	19	: 10011	00	: 00000
0403	: 0110010011	02	: 00010	06	: 00110	21	: 10101
0404	: 0110010100	03	: 00011	07	: 00111	20	: 10100
0405	: 0110010101	22	: 10110	18	: 10010	01	: 00001
0406	: 0110010110	28	: 11100	24	: 11000	11	: 01011
0407	: 0110010111	09	: 01001	13	: 01101	30	: 11110
0408	: 0110011000	30	: 11110	26	: 11010	09	: 01001
0409	: 0110011001	11	: 01011	15	: 01111	28	: 11100
0410	: 0110011010	01	: 00001	05	: 00101	22	: 10110
0411	: 0110011011	20	: 10100	16	: 10000	03	: 00011
0412	: 0110011100	21	: 10101	17	: 10001	02	: 00010
0413	: 0110011101	00	: 00000	04	: 00100	23	: 10111
0414	: 0110011110	10	: 01010	14	: 01110	29	: 11101
0415	: 0110011111	31	: 11111	27	: 11011	08	: 01000

BIT UTILI		CODICE		CODICE		CODICE	
CICLICO		INFORMAZ.		SERVIZIO			
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0416	: 0110100000	22	: 10110	18	: 10010	01	: 00001
0417	: 0110100001	03	: 00011	07	: 00111	20	: 10100
0418	: 0110100010	09	: 01001	13	: 01101	30	: 11110
0419	: 0110100011	28	: 11100	24	: 11000	11	: 01011
0420	: 0110100100	29	: 11101	25	: 11001	10	: 01010
0421	: 0110100101	08	: 01000	12	: 01100	31	: 11111
0422	: 0110100110	02	: 00010	06	: 00110	21	: 10101
0423	: 0110100111	23	: 10111	19	: 10011	00	: 00000
0424	: 0110101000	00	: 00000	04	: 00100	23	: 10111
0425	: 0110101001	21	: 10101	17	: 10001	02	: 00010
0426	: 0110101010	31	: 11111	27	: 11011	08	: 01000
0427	: 0110101011	10	: 01010	14	: 01110	29	: 11101
0428	: 0110101100	11	: 01011	15	: 01111	28	: 11100
0429	: 0110101101	30	: 11110	26	: 11010	09	: 01001
0430	: 0110101110	20	: 10100	16	: 10000	03	: 00011
0431	: 0110101111	01	: 00001	05	: 00101	22	: 10110
0432	: 0110110000	15	: 01111	11	: 01011	24	: 11000
0433	: 0110110001	26	: 11010	30	: 11110	13	: 01101
0434	: 0110110010	16	: 10000	20	: 10100	07	: 00111
0435	: 0110110011	05	: 00101	01	: 00001	18	: 10010
0436	: 0110110100	04	: 00100	00	: 00000	19	: 10011
0437	: 0110110101	17	: 10001	21	: 10101	06	: 00110
0438	: 0110110110	27	: 11011	31	: 11111	12	: 01100
0439	: 0110110111	14	: 01110	10	: 01010	25	: 11001
0440	: 0110111000	25	: 11001	29	: 11101	14	: 01110
0441	: 0110111001	12	: 01100	03	: 01000	27	: 11011
0442	: 0110111010	06	: 00110	02	: 00010	17	: 10001
0443	: 0110111011	19	: 10011	23	: 10111	04	: 00100
0444	: 0110111100	18	: 10010	22	: 10110	05	: 00101
0445	: 0110111101	07	: 00111	03	: 00011	16	: 10000
0446	: 0110111110	13	: 01101	09	: 01001	26	: 11010
0447	: 0110111111	24	: 11000	28	: 11100	15	: 01111

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0448	: 0111000000	31	: 11111	27	: 11011	08	: 01000
0449	: 0111000001	10	: 01010	14	: 01110	29	: 11101
0450	: 0111000010	00	: 00000	04	: 00100	23	: 10111
0451	: 0111000011	21	: 10101	17	: 10001	02	: 00010
0452	: 0111000100	20	: 10100	16	: 10000	03	: 00011
0453	: 0111000101	01	: 00001	05	: 00101	22	: 10110
0454	: 0111000110	11	: 01011	15	: 01111	28	: 11100
0455	: 0111000111	30	: 11110	26	: 11010	09	: 01001
0456	: 0111001000	09	: 01001	13	: 01101	30	: 11110
0457	: 0111001001	28	: 11100	24	: 11000	11	: 01011
0458	: 0111001010	22	: 10110	18	: 10010	01	: 00001
0459	: 0111001011	03	: 00011	07	: 00111	20	: 10100
0460	: 0111001100	02	: 00010	06	: 00110	21	: 10101
0461	: 0111001101	23	: 10111	19	: 10011	00	: 00000
0462	: 0111001110	29	: 11101	25	: 11001	10	: 01010
0463	: 0111001111	08	: 01000	12	: 01100	31	: 11111
0464	: 0111010000	06	: 00110	02	: 00010	17	: 10001
0465	: 0111010001	19	: 10011	23	: 10111	04	: 00100
0466	: 0111010010	25	: 11001	29	: 11101	14	: 01110
0467	: 0111010011	12	: 01100	08	: 01000	27	: 11011
0468	: 0111010100	13	: 01101	09	: 01001	26	: 11010
0469	: 0111010101	24	: 11000	28	: 11100	15	: 01111
0470	: 0111010110	18	: 10010	22	: 10110	05	: 00101
0471	: 0111010111	07	: 00111	03	: 00011	16	: 10000
0472	: 0111011000	16	: 10000	20	: 10100	07	: 00111
0473	: 0111011001	05	: 00101	01	: 00001	18	: 10010
0474	: 0111011010	15	: 01111	11	: 01011	24	: 11000
0475	: 0111011011	26	: 11010	30	: 11110	13	: 01101
0476	: 0111011100	27	: 11011	31	: 11111	12	: 01100
0477	: 0111011101	14	: 01110	10	: 01010	25	: 11001
0478	: 0111011110	04	: 00100	00	: 00000	19	: 10011
0479	: 0111011111	17	: 10001	21	: 10101	06	: 00110

BIT UTILI		CODICE CICLICO		CODICE INFORMAZ.		CODICE SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0480	: 0111100000	24	: 11000	28	: 11100	15	: 01111
0481	: 0111100001	13	: 01101	09	: 01001	26	: 11010
0482	: 0111100010	07	: 00111	03	: 00011	16	: 10000
0483	: 0111100011	18	: 10010	22	: 10110	05	: 00101
0484	: 0111100100	19	: 10011	23	: 10111	04	: 00100
0485	: 0111100101	06	: 00110	02	: 00010	17	: 10001
0486	: 0111100110	12	: 01100	08	: 01000	27	: 11011
0487	: 0111100111	25	: 11001	29	: 11101	14	: 01110
0488	: 0111101000	14	: 01110	10	: 01010	25	: 11001
0489	: 0111101001	27	: 11011	31	: 11111	12	: 01100
0490	: 0111101010	17	: 10001	21	: 10101	06	: 00110
0491	: 0111101011	04	: 00100	00	: 00000	19	: 10011
0492	: 0111101100	05	: 00101	01	: 00001	18	: 10010
0493	: 0111101101	16	: 10000	20	: 10100	07	: 00111
0494	: 0111101110	26	: 11010	30	: 11110	13	: 01101
0495	: 0111101111	15	: 01111	11	: 01011	24	: 11000
0496	: 0111110000	01	: 00001	05	: 00101	22	: 10110
0497	: 0111110001	20	: 10100	16	: 10000	03	: 00011
0498	: 0111110010	30	: 11110	26	: 11010	09	: 01001
0499	: 0111110011	11	: 01011	15	: 01111	28	: 11100
0500	: 0111110100	10	: 01010	14	: 01110	29	: 11101
0501	: 0111110101	31	: 11111	27	: 11011	08	: 01000
0502	: 0111110110	21	: 10101	17	: 10001	02	: 00010
0503	: 0111110111	00	: 00000	04	: 00100	23	: 10111
0504	: 0111111000	23	: 10111	19	: 10011	00	: 00000
0505	: 0111111001	02	: 00010	06	: 00110	21	: 10101
0506	: 0111111010	08	: 01000	12	: 01100	31	: 11111
0507	: 0111111011	29	: 11101	25	: 11001	10	: 01010
0508	: 0111111100	28	: 11100	24	: 11000	11	: 01011
0509	: 0111111101	09	: 01001	13	: 01101	30	: 11110
0510	: 0111111110	03	: 00011	07	: 00111	20	: 10100
0511	: 0111111111	22	: 10110	18	: 10010	01	: 00001

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0512	: 1000000000	26	: 11010	30	: 11110	13	: 01101
0513	: 1000000001	15	: 01111	11	: 01011	24	: 11000
0514	: 1000000010	05	: 00101	01	: 00001	18	: 10010
0515	: 1000000011	16	: 10000	20	: 10100	07	: 00111
0516	: 1000000100	17	: 10001	21	: 10101	06	: 00110
0517	: 1000000101	04	: 00100	00	: 00000	19	: 10011
0518	: 1000000110	14	: 01110	10	: 01010	25	: 11001
0519	: 1000000111	27	: 11011	31	: 11111	12	: 01100
0520	: 1000001000	12	: 01100	08	: 01000	27	: 11011
0521	: 1000001001	25	: 11001	29	: 11101	14	: 01110
0522	: 1000001010	19	: 10011	23	: 10111	04	: 00100
0523	: 1000001011	06	: 00110	02	: 00010	17	: 10001
0524	: 1000001100	07	: 00111	03	: 00011	16	: 10000
0525	: 1000001101	18	: 10010	22	: 10110	05	: 00101
0526	: 1000001110	24	: 11000	28	: 11100	15	: 01111
0527	: 1000001111	13	: 01101	09	: 01001	26	: 11010
0528	: 1000010000	03	: 00011	07	: 00111	20	: 10100
0529	: 1000010001	22	: 10110	18	: 10010	01	: 00001
0530	: 1000010010	28	: 11100	24	: 11000	11	: 01011
0531	: 1000010011	09	: 01001	13	: 01101	30	: 11110
0532	: 1000010100	08	: 01000	12	: 01100	31	: 11111
0533	: 1000010101	29	: 11101	25	: 11001	10	: 01010
0534	: 1000010110	23	: 10111	19	: 10011	00	: 00000
0535	: 1000010111	02	: 00010	06	: 00110	21	: 10101
0536	: 1000011000	21	: 10101	17	: 10001	02	: 00010
0537	: 1000011001	00	: 00000	04	: 00100	23	: 10111
0538	: 1000011010	10	: 01010	14	: 01110	29	: 11101
0539	: 1000011011	31	: 11111	27	: 11011	08	: 01000
0540	: 1000011100	30	: 11110	26	: 11010	09	: 01001
0541	: 1000011101	11	: 01011	15	: 01111	28	: 11100
0542	: 1000011110	01	: 00001	05	: 00101	22	: 10110
0543	: 1000011111	20	: 10100	16	: 10000	03	: 00011

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0544	: 1000100000	29	: 11101	25	: 11001	10	: 01010
0545	: 1000100001	08	: 01000	12	: 01100	31	: 11111
0546	: 1000100010	02	: 00010	06	: 00110	21	: 10101
0547	: 1000100011	23	: 10111	19	: 10011	00	: 00000
0548	: 1000100100	22	: 10110	18	: 10010	01	: 00001
0549	: 1000100101	03	: 00011	07	: 00111	20	: 10100
0550	: 1000100110	09	: 01001	13	: 01101	30	: 11110
0551	: 1000100111	28	: 11100	24	: 11000	11	: 01011
0552	: 1000101000	11	: 01011	15	: 01111	28	: 11100
0553	: 1000101001	30	: 11110	26	: 11010	09	: 01001
0554	: 1000101010	20	: 10100	16	: 10000	03	: 00011
0555	: 1000101011	01	: 00001	05	: 00101	22	: 10110
0556	: 1000101100	00	: 00000	04	: 00100	23	: 10111
0557	: 1000101101	21	: 10101	17	: 10001	02	: 00010
0558	: 1000101110	31	: 11111	27	: 11011	08	: 01000
0559	: 1000101111	10	: 01010	14	: 01110	29	: 11101
0560	: 1000110000	04	: 00100	00	: 00000	19	: 10011
0561	: 1000110001	17	: 10001	21	: 10101	06	: 00110
0562	: 1000110010	27	: 11011	31	: 11111	12	: 01100
0563	: 1000110011	14	: 01110	10	: 01010	25	: 11001
0564	: 1000110100	15	: 01111	11	: 01011	24	: 11000
0565	: 1000110101	26	: 11010	30	: 11110	13	: 01101
0566	: 1000110110	16	: 10000	20	: 10100	07	: 00111
0567	: 1000110111	05	: 00101	01	: 00001	18	: 10010
0568	: 1000111000	18	: 10010	22	: 10110	05	: 00101
0569	: 1000111001	07	: 00111	03	: 00011	16	: 10000
0570	: 1000111010	13	: 01101	09	: 01001	26	: 11010
0571	: 1000111011	24	: 11000	28	: 11100	15	: 01111
0572	: 1000111100	25	: 11001	29	: 11101	14	: 01110
0573	: 1000111101	12	: 01100	08	: 01000	27	: 11011
0574	: 1000111110	06	: 00110	02	: 00010	17	: 10001
0575	: 1000111111	19	: 10011	23	: 10111	04	: 00100

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0576	: 1001000000	20	: 10100	16	: 10000	03	: 00011
0577	: 1001000001	01	: 00001	05	: 00101	22	: 10110
0578	: 1001000010	11	: 01011	15	: 01111	28	: 11100
0579	: 1001000011	30	: 11110	24	: 11010	09	: 01001
0580	: 1001000100	31	: 11111	27	: 11011	08	: 01000
0581	: 1001000101	10	: 01010	14	: 01110	29	: 11101
0582	: 1001000110	00	: 00000	04	: 00100	23	: 10111
0583	: 1001000111	21	: 10101	17	: 10001	02	: 00010
0584	: 1001001000	02	: 00010	06	: 00110	21	: 10101
0585	: 1001001001	23	: 10111	19	: 10011	00	: 00000
0586	: 1001001010	29	: 11101	25	: 11001	10	: 01010
0587	: 1001001011	08	: 01000	12	: 01100	31	: 11111
0588	: 1001001100	09	: 01001	13	: 01101	30	: 11110
0589	: 1001001101	28	: 11100	24	: 11000	11	: 01011
0590	: 1001001110	22	: 10110	18	: 10010	01	: 00001
0591	: 1001001111	03	: 00011	07	: 00111	20	: 10100
0592	: 1001010000	13	: 01101	09	: 01001	26	: 11010
0593	: 1001010001	24	: 11000	28	: 11100	15	: 01111
0594	: 1001010010	18	: 10010	22	: 10110	05	: 00101
0595	: 1001010011	07	: 00111	03	: 00011	16	: 10000
0596	: 1001010100	06	: 00110	02	: 00010	17	: 10001
0597	: 1001010101	19	: 10011	23	: 10111	04	: 00100
0598	: 1001010110	25	: 11001	29	: 11101	14	: 01110
0599	: 1001010111	12	: 01100	08	: 01000	27	: 11011
0600	: 1001011000	27	: 11011	31	: 11111	12	: 01100
0601	: 1001011001	14	: 01110	10	: 01010	25	: 11001
0602	: 1001011010	04	: 00100	00	: 00000	19	: 10011
0603	: 1001011011	17	: 10001	21	: 10101	06	: 00110
0604	: 1001011100	16	: 10000	20	: 10100	07	: 00111
0605	: 1001011101	05	: 00101	01	: 00001	18	: 10010
0606	: 1001011110	15	: 01111	11	: 01011	24	: 11000
0607	: 1001011111	26	: 11010	30	: 11110	13	: 01101

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	EIN	DEC	EIN	DEC	EIN	DEC	EIN
0608	: 1001100000	19	: 10011	23	: 10111	04	: 00100
0609	: 1001100001	06	: 00110	02	: 00010	17	: 10001
0610	: 1001100010	12	: 01100	03	: 01000	27	: 11011
0611	: 1001100011	25	: 11001	29	: 11101	14	: 01110
0612	: 1001100100	24	: 11000	28	: 11100	15	: 01111
0613	: 1001100101	13	: 01101	09	: 01001	26	: 11010
0614	: 1001100110	07	: 00111	03	: 00011	16	: 10000
0615	: 1001100111	18	: 10010	22	: 10110	05	: 00101
0616	: 1001101000	05	: 00101	01	: 00001	18	: 10010
0617	: 1001101001	16	: 10000	20	: 10100	07	: 00111
0618	: 1001101010	26	: 11010	30	: 11110	13	: 01101
0619	: 1001101011	15	: 01111	11	: 01011	24	: 11000
0620	: 1001101100	14	: 01110	10	: 01010	25	: 11001
0621	: 1001101101	27	: 11011	31	: 11111	12	: 01100
0622	: 1001101110	17	: 10001	21	: 10101	06	: 00110
0623	: 1001101111	04	: 00100	00	: 00000	19	: 10011
0624	: 1001110000	10	: 01010	14	: 01110	29	: 11101
0625	: 1001110001	31	: 11111	27	: 11011	08	: 01000
0626	: 1001110010	21	: 10101	17	: 10001	02	: 00010
0627	: 1001110011	00	: 00000	04	: 00100	23	: 10111
0628	: 1001110100	01	: 00001	05	: 00101	22	: 10110
0629	: 1001110101	20	: 10100	16	: 10000	03	: 00011
0630	: 1001110110	30	: 11110	26	: 11010	09	: 01001
0631	: 1001110111	11	: 01011	15	: 01111	28	: 11100
0632	: 1001111000	28	: 11100	24	: 11000	11	: 01011
0633	: 1001111001	09	: 01001	13	: 01101	30	: 11110
0634	: 1001111010	03	: 00011	07	: 00111	20	: 10100
0635	: 1001111011	22	: 10110	18	: 10010	01	: 00001
0636	: 1001111100	23	: 10111	19	: 10011	00	: 00000
0637	: 1001111101	02	: 00010	06	: 00110	21	: 10101
0638	: 1001111110	08	: 01000	12	: 01100	31	: 11111
0639	: 1001111111	29	: 11101	25	: 11001	10	: 01010

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0640	1010000000	06	00110	02	00010	17	10001
0641	1010000001	19	10011	23	10111	04	00100
0642	1010000010	25	11001	29	11101	14	01110
0643	1010000011	12	01100	08	01000	27	11011
0644	1010000100	13	01101	09	01001	26	11010
0645	1010000101	24	11000	28	11100	15	01111
0646	1010000110	18	10010	22	10110	05	00101
0647	1010000111	07	00111	03	00011	16	10000
0648	1010001000	16	10000	20	10100	07	00111
0649	1010001001	05	00101	01	00001	18	10010
0650	1010001010	15	01111	11	01011	24	11000
0651	1010001011	26	11010	30	11110	13	01101
0652	1010001100	27	11011	31	11111	12	01100
0653	1010001101	14	01110	10	01010	25	11001
0654	1010001110	04	00100	00	00000	19	10011
0655	1010001111	17	10001	21	10101	06	00110
0656	1010010000	31	11111	27	11011	08	01000
0657	1010010001	10	01010	14	01110	29	11101
0658	1010010010	00	00000	04	00100	23	10111
0659	1010010011	21	10101	17	10001	02	00010
0660	1010010100	20	10100	16	10000	03	00011
0661	1010010101	01	00001	05	00101	22	10110
0662	1010010110	11	01011	15	01111	28	11100
0663	1010010111	30	11110	26	11010	09	01001
0664	1010011000	09	01001	13	01101	30	11110
0665	1010011001	28	11100	24	11000	11	01011
0666	1010011010	22	10110	18	10010	01	00001
0667	1010011011	03	00011	07	00111	20	10100
0668	1010011100	02	00010	06	00110	21	10101
0669	1010011101	23	10111	19	10011	00	00000
0670	1010011110	29	11101	25	11001	10	01010
0671	1010011111	08	01000	12	01100	31	11111

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0672	: 1010100000	01	: 00001	05	: 00101	22	: 10110
0673	: 1010100001	20	: 10100	16	: 10000	03	: 00011
0674	: 1010100010	30	: 11110	26	: 11010	09	: 01001
0675	: 1010100011	11	: 01011	15	: 01111	28	: 11100
0676	: 1010100100	10	: 01010	14	: 01110	29	: 11101
0677	: 1010100101	31	: 11111	27	: 11011	08	: 01000
0678	: 1010100110	21	: 10101	17	: 10001	02	: 00010
0679	: 1010100111	00	: 00000	04	: 00100	23	: 10111
0680	: 1010101000	23	: 10111	19	: 10011	00	: 00000
0681	: 1010101001	02	: 00010	06	: 00110	21	: 10101
0682	: 1010101010	08	: 01000	12	: 01100	31	: 11111
0683	: 1010101011	29	: 11101	25	: 11001	10	: 01010
0684	: 1010101100	28	: 11100	24	: 11000	11	: 01011
0685	: 1010101101	09	: 01001	13	: 01101	30	: 11110
0686	: 1010101110	03	: 00011	07	: 00111	20	: 10100
0687	: 1010101111	22	: 10110	18	: 10010	01	: 00001
0688	: 1010110000	24	: 11000	28	: 11100	15	: 01111
0689	: 1010110001	13	: 01101	09	: 01001	26	: 11010
0690	: 1010110010	07	: 00111	03	: 00011	16	: 10000
0691	: 1010110011	18	: 10010	22	: 10110	05	: 00101
0692	: 1010110100	19	: 10011	23	: 10111	04	: 00100
0693	: 1010110101	06	: 00110	02	: 00010	17	: 10001
0694	: 1010110110	12	: 01100	08	: 01000	27	: 11011
0695	: 1010110111	25	: 11001	29	: 11101	14	: 01110
0696	: 1010111000	14	: 01110	10	: 01010	25	: 11001
0697	: 1010111001	27	: 11011	31	: 11111	12	: 01100
0698	: 1010111010	17	: 10001	21	: 10101	06	: 00110
0699	: 1010111011	04	: 00100	00	: 00000	19	: 10011
0700	: 1010111100	05	: 00101	01	: 00001	18	: 10010
0701	: 1010111101	16	: 10000	20	: 10100	07	: 00111
0702	: 1010111110	26	: 11010	30	: 11110	13	: 01101
0703	: 1010111111	15	: 01111	11	: 01011	24	: 11000

BIT UTILI		CODICE	CODICE	CODICE
		CICLICO	INFORMAZ.	SERVIZIO
DEC	BIN	DEC BIN	DEC BIN	DEC BIN
0704	: 1011000000	08 : 01000	12 : 01100	31 : 11111
0705	: 1011000001	29 : 11101	25 : 11001	10 : 01010
0706	: 1011000010	23 : 10111	19 : 10011	00 : 00000
0707	: 1011000011	02 : 00010	06 : 00110	21 : 10101
0708	: 1011000100	03 : 00011	07 : 00111	20 : 10100
0709	: 1011000101	22 : 10110	18 : 10010	01 : 00001
0710	: 1011000110	28 : 11100	24 : 11000	11 : 01011
0711	: 1011000111	09 : 01001	13 : 01101	30 : 11110
0712	: 1011001000	30 : 11110	26 : 11010	09 : 01001
0713	: 1011001001	11 : 01011	15 : 01111	28 : 11100
0714	: 1011001010	01 : 00001	05 : 00101	22 : 10110
0715	: 1011001011	20 : 10100	16 : 10000	03 : 00011
0716	: 1011001100	21 : 10101	17 : 10001	02 : 00010
0717	: 1011001101	00 : 00000	04 : 00100	23 : 10111
0718	: 1011001110	10 : 01010	14 : 01110	29 : 11101
0719	: 1011001111	31 : 11111	27 : 11011	08 : 01000
0720	: 1011010000	17 : 10001	21 : 10101	06 : 00110
0721	: 1011010001	04 : 00100	00 : 00000	19 : 10011
0722	: 1011010010	14 : 01110	10 : 01010	25 : 11001
0723	: 1011010011	27 : 11011	31 : 11111	12 : 01100
0724	: 1011010100	26 : 11010	30 : 11110	13 : 01101
0725	: 1011010101	15 : 01111	11 : 01011	24 : 11000
0726	: 1011010110	05 : 00101	01 : 00001	18 : 10010
0727	: 1011010111	16 : 10000	20 : 10100	07 : 00111
0728	: 1011011000	07 : 00111	03 : 00011	16 : 10000
0729	: 1011011001	18 : 10010	22 : 10110	05 : 00101
0730	: 1011011010	24 : 11000	28 : 11100	15 : 01111
0731	: 1011011011	13 : 01101	09 : 01001	26 : 11010
0732	: 1011011100	12 : 01100	08 : 01000	27 : 11011
0733	: 1011011101	25 : 11001	29 : 11101	14 : 01110
0734	: 1011011110	19 : 10011	23 : 10111	04 : 00100
0735	: 1011011111	06 : 00110	02 : 00010	17 : 10001

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0736	: 1011100000	15	: 01111	11	: 01011	24	: 11000
0737	: 1011100001	26	: 11010	30	: 11110	13	: 01101
0738	: 1011100010	16	: 10000	20	: 10100	07	: 00111
0739	: 1011100011	05	: 00101	01	: 00001	18	: 10010
0740	: 1011100100	04	: 00100	00	: 00000	19	: 10011
0741	: 1011100101	17	: 10001	21	: 10101	06	: 00110
0742	: 1011100110	27	: 11011	31	: 11111	12	: 01100
0743	: 1011100111	14	: 01110	10	: 01010	25	: 11001
0744	: 1011101000	25	: 11001	29	: 11101	14	: 01110
0745	: 1011101001	12	: 01100	08	: 01000	27	: 11011
0746	: 1011101010	06	: 00110	02	: 00010	17	: 10001
0747	: 1011101011	19	: 10011	23	: 10111	04	: 00100
0748	: 1011101100	18	: 10010	22	: 10110	05	: 00101
0749	: 1011101101	07	: 00111	03	: 00011	16	: 10000
0750	: 1011101110	13	: 01101	09	: 01001	26	: 11010
0751	: 1011101111	24	: 11000	28	: 11100	15	: 01111
0752	: 1011110000	22	: 10110	13	: 10010	01	: 00001
0753	: 1011110001	03	: 00011	07	: 00111	20	: 10100
0754	: 1011110010	09	: 01001	13	: 01101	30	: 11110
0755	: 1011110011	28	: 11100	24	: 11000	11	: 01011
0756	: 1011110100	29	: 11101	25	: 11001	10	: 01010
0757	: 1011110101	08	: 01000	12	: 01100	31	: 11111
0758	: 1011110110	02	: 00010	06	: 00110	21	: 10101
0759	: 1011110111	23	: 10111	19	: 10011	00	: 00000
0760	: 1011111000	00	: 00000	04	: 00100	23	: 10111
0761	: 1011111001	21	: 10101	17	: 10001	02	: 00010
0762	: 1011111010	31	: 11111	27	: 11011	08	: 01000
0763	: 1011111011	10	: 01010	14	: 01110	29	: 11101
0764	: 1011111100	11	: 01011	15	: 01111	28	: 11100
0765	: 1011111101	30	: 11110	26	: 11010	09	: 01001
0766	: 1011111110	20	: 10100	16	: 10000	03	: 00011
0767	: 1011111111	01	: 00001	05	: 00101	22	: 10110

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0768	: 1100000000	23	: 10111	19	: 10011	00	: 00000
0769	: 1100000001	02	: 00010	06	: 00110	21	: 10101
0770	: 1100000010	08	: 01000	12	: 01100	31	: 11111
0771	: 1100000011	29	: 11101	25	: 11001	10	: 01010
0772	: 1100000100	28	: 11100	24	: 11000	11	: 01011
0773	: 1100000101	09	: 01001	13	: 01101	30	: 11110
0774	: 1100000110	03	: 00011	07	: 00111	20	: 10100
0775	: 1100000111	22	: 10110	18	: 10010	01	: 00001
0776	: 1100001000	01	: 00001	05	: 00101	22	: 10110
0777	: 1100001001	20	: 10100	16	: 10000	03	: 00011
0778	: 1100001010	30	: 11110	26	: 11010	09	: 01001
0779	: 1100001011	11	: 01011	15	: 01111	28	: 11100
0780	: 1100001100	10	: 01010	14	: 01110	29	: 11101
0781	: 1100001101	31	: 11111	27	: 11011	08	: 01000
0782	: 1100001110	21	: 10101	17	: 10001	02	: 00010
0783	: 1100001111	00	: 00000	04	: 00100	23	: 10111
0784	: 1100010000	14	: 01110	10	: 01010	25	: 11001
0785	: 1100010001	27	: 11011	31	: 11111	12	: 01100
0786	: 1100010010	17	: 10001	21	: 10101	06	: 00110
0787	: 1100010011	04	: 00100	00	: 00000	19	: 10011
0788	: 1100010100	05	: 00101	01	: 00001	18	: 10010
0789	: 1100010101	16	: 10000	20	: 10100	07	: 00111
0790	: 1100010110	26	: 11010	30	: 11110	13	: 01101
0791	: 1100010111	15	: 01111	11	: 01011	24	: 11000
0792	: 1100011000	24	: 11000	28	: 11100	15	: 01111
0793	: 1100011001	13	: 01101	09	: 01001	26	: 11010
0794	: 1100011010	07	: 00111	03	: 00011	16	: 10000
0795	: 1100011011	18	: 10010	22	: 10110	05	: 00101
0796	: 1100011100	19	: 10011	23	: 10111	04	: 00100
0797	: 1100011101	06	: 00110	02	: 00010	17	: 10001
0798	: 1100011110	12	: 01100	08	: 01000	27	: 11011
0799	: 1100011111	25	: 11001	29	: 11101	14	: 01110

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0800	: 1100100000	16	: 10000	20	: 10100	07	: 00111
0801	: 1100100001	05	: 00101	01	: 00001	18	: 10010
0802	: 1100100010	15	: 01111	11	: 01011	24	: 11000
0803	: 1100100011	26	: 11010	30	: 11110	13	: 01101
0804	: 1100100100	27	: 11011	31	: 11111	12	: 01100
0805	: 1100100101	14	: 01110	10	: 01010	25	: 11001
0806	: 1100100110	04	: 00100	00	: 00000	19	: 10011
0807	: 1100100111	17	: 10001	21	: 10101	06	: 00110
0808	: 1100101000	06	: 00110	02	: 00010	17	: 10001
0809	: 1100101001	19	: 10011	23	: 10111	04	: 00100
0810	: 1100101010	25	: 11001	29	: 11101	14	: 01110
0811	: 1100101011	12	: 01100	03	: 01000	27	: 11011
0812	: 1100101100	13	: 01101	09	: 01001	26	: 11010
0813	: 1100101101	24	: 11000	28	: 11100	15	: 01111
0814	: 1100101110	18	: 10010	22	: 10110	05	: 00101
0815	: 1100101111	07	: 00111	03	: 00011	16	: 10000
0816	: 1100110000	09	: 01001	13	: 01101	30	: 11110
0817	: 1100110001	28	: 11100	24	: 11000	11	: 01011
0818	: 1100110010	22	: 10110	18	: 10010	01	: 00001
0819	: 1100110011	03	: 00011	07	: 00111	20	: 10100
0820	: 1100110100	02	: 00010	06	: 00110	21	: 10101
0821	: 1100110101	23	: 10111	19	: 10011	00	: 00000
0822	: 1100110110	29	: 11101	25	: 11001	10	: 01010
0823	: 1100110111	08	: 01000	12	: 01100	31	: 11111
0824	: 1100111000	31	: 11111	27	: 11011	08	: 01000
0825	: 1100111001	10	: 01010	14	: 01110	29	: 11101
0826	: 1100111010	00	: 00000	04	: 00100	23	: 10111
0827	: 1100111011	21	: 10101	17	: 10001	02	: 00010
0828	: 1100111100	20	: 10100	16	: 10000	03	: 00011
0829	: 1100111101	01	: 00001	05	: 00101	22	: 10110
0830	: 1100111110	11	: 01011	15	: 01111	28	: 11100
0831	: 1100111111	30	: 11110	26	: 11010	09	: 01001

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0832	: 1101000000	25	: 11001	29	: 11101	14	: 01110
0833	: 1101000001	12	: 01100	08	: 01000	27	: 11011
0834	: 1101000010	06	: 00110	02	: 00010	17	: 10001
0835	: 1101000011	19	: 10011	23	: 10111	04	: 00100
0836	: 1101000100	18	: 10010	22	: 10110	05	: 00101
0837	: 1101000101	07	: 00111	03	: 00011	16	: 10000
0838	: 1101000110	13	: 01101	09	: 01001	26	: 11010
0839	: 1101000111	24	: 11000	28	: 11100	15	: 01111
0840	: 1101001000	15	: 01111	11	: 01011	24	: 11000
0841	: 1101001001	26	: 11010	30	: 11110	13	: 01101
0842	: 1101001010	16	: 10000	20	: 10100	07	: 00111
0843	: 1101001011	05	: 00101	01	: 00001	18	: 10010
0844	: 1101001100	04	: 00100	00	: 00000	19	: 10011
0845	: 1101001101	17	: 10001	21	: 10101	06	: 00110
0846	: 1101001110	27	: 11011	31	: 11111	12	: 01100
0847	: 1101001111	14	: 01110	10	: 01010	25	: 11001
0848	: 1101010000	00	: 00000	04	: 00100	23	: 10111
0849	: 1101010001	21	: 10101	17	: 10001	02	: 00010
0850	: 1101010010	31	: 11111	27	: 11011	08	: 01000
0851	: 1101010011	10	: 01010	14	: 01110	29	: 11101
0852	: 1101010100	11	: 01011	15	: 01111	28	: 11100
0853	: 1101010101	30	: 11110	26	: 11010	09	: 01001
0854	: 1101010110	20	: 10100	16	: 10000	03	: 00011
0855	: 1101010111	01	: 00001	05	: 00101	22	: 10110
0856	: 1101011000	22	: 10110	18	: 10010	01	: 00001
0857	: 1101011001	03	: 00011	07	: 00111	20	: 10100
0858	: 1101011010	09	: 01001	13	: 01101	30	: 11110
0859	: 1101011011	28	: 11100	24	: 11000	11	: 01011
0860	: 1101011100	29	: 11101	25	: 11001	10	: 01010
0861	: 1101011101	08	: 01000	12	: 01100	31	: 11111
0862	: 1101011110	02	: 00010	06	: 00110	21	: 10101
0863	: 1101011111	23	: 10111	19	: 10011	00	: 00000

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0864	: 1101100000	30	: 11110	26	: 11010	09	: 01001
0865	: 1101100001	11	: 01011	15	: 01111	28	: 11100
0866	: 1101100010	01	: 00001	05	: 00101	22	: 10110
0867	: 1101100011	20	: 10100	16	: 10000	03	: 00011
0868	: 1101100100	21	: 10101	17	: 10001	02	: 00010
0869	: 1101100101	00	: 00000	04	: 00100	23	: 10111
0870	: 1101100110	10	: 01010	14	: 01110	29	: 11101
0871	: 1101100111	31	: 11111	27	: 11011	08	: 01000
0872	: 1101101000	08	: 01000	12	: 01100	31	: 11111
0873	: 1101101001	29	: 11101	25	: 11001	10	: 01010
0874	: 1101101010	23	: 10111	19	: 10011	00	: 00000
0875	: 1101101011	02	: 00010	06	: 00110	21	: 10101
0876	: 1101101100	03	: 00011	07	: 00111	20	: 10100
0877	: 1101101101	22	: 10110	18	: 10010	01	: 00001
0878	: 1101101110	28	: 11100	24	: 11000	11	: 01011
0879	: 1101101111	09	: 01001	13	: 01101	30	: 11110
0880	: 1101110000	07	: 00111	03	: 00011	16	: 10000
0881	: 1101110001	18	: 10010	22	: 10110	05	: 00101
0882	: 1101110010	24	: 11000	28	: 11100	15	: 01111
0883	: 1101110011	13	: 01101	09	: 01001	26	: 11010
0884	: 1101110100	12	: 01100	08	: 01000	27	: 11011
0885	: 1101110101	25	: 11001	29	: 11101	14	: 01110
0886	: 1101110110	19	: 10011	23	: 10111	04	: 00100
0887	: 1101110111	06	: 00110	02	: 00010	17	: 10001
0888	: 1101111000	17	: 10001	21	: 10101	06	: 00110
0889	: 1101111001	04	: 00100	00	: 00000	19	: 10011
0890	: 1101111010	14	: 01110	10	: 01010	25	: 11001
0891	: 1101111011	27	: 11011	31	: 11111	12	: 01100
0892	: 1101111100	26	: 11010	30	: 11110	13	: 01101
0893	: 1101111101	15	: 01111	11	: 01011	24	: 11000
0894	: 1101111110	05	: 00101	01	: 00001	18	: 10010
0895	: 1101111111	16	: 10000	20	: 10100	07	: 00111

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0896	: 1110000000	11	: 01011	15	: 01111	28	: 11100
0897	: 1110000001	30	: 11110	26	: 11010	09	: 01001
0898	: 1110000010	20	: 10100	16	: 10000	03	: 00011
0899	: 1110000011	01	: 00001	05	: 00101	22	: 10110
0900	: 1110000100	00	: 00000	04	: 00100	23	: 10111
0901	: 1110000101	21	: 10101	17	: 10001	02	: 00010
0902	: 1110000110	31	: 11111	27	: 11011	08	: 01000
0903	: 1110000111	10	: 01010	14	: 01110	29	: 11101
0904	: 1110001000	29	: 11101	25	: 11001	10	: 01010
0905	: 1110001001	08	: 01000	12	: 01100	31	: 11111
0906	: 1110001010	02	: 00010	06	: 00110	21	: 10101
0907	: 1110001011	23	: 10111	19	: 10011	00	: 00000
0908	: 1110001100	22	: 10110	18	: 10010	01	: 00001
0909	: 1110001101	03	: 00011	07	: 00111	20	: 10100
0910	: 1110001110	09	: 01001	13	: 01101	30	: 11110
0911	: 1110001111	28	: 11100	24	: 11000	11	: 01011
0912	: 1110010000	18	: 10010	22	: 10110	05	: 00101
0913	: 1110010001	07	: 00111	03	: 00011	16	: 10000
0914	: 1110010010	13	: 01101	09	: 01001	26	: 11010
0915	: 1110010011	24	: 11000	28	: 11100	15	: 01111
0916	: 1110010100	25	: 11001	29	: 11101	14	: 01110
0917	: 1110010101	12	: 01100	08	: 01000	27	: 11011
0918	: 1110010110	06	: 00110	02	: 00010	17	: 10001
0919	: 1110010111	19	: 10011	23	: 10111	04	: 00100
0920	: 1110011000	04	: 00100	00	: 00000	19	: 10011
0921	: 1110011001	17	: 10001	21	: 10101	06	: 00110
0922	: 1110011010	27	: 11011	31	: 11111	12	: 01100
0923	: 1110011011	14	: 01110	10	: 01010	25	: 11001
0924	: 1110011100	15	: 01111	11	: 01011	24	: 11000
0925	: 1110011101	26	: 11010	30	: 11110	13	: 01101
0926	: 1110011110	16	: 10000	20	: 10100	07	: 00111
0927	: 1110011111	05	: 00101	01	: 00001	18	: 10010

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0928	: 1110100000	12	: 01100	08	: 01000	27	: 11011
0929	: 1110100001	25	: 11001	29	: 11101	14	: 01110
0930	: 1110100010	19	: 10011	23	: 10111	04	: 00100
0931	: 1110100011	06	: 00110	02	: 00010	17	: 10001
0932	: 1110100100	07	: 00111	03	: 00011	16	: 10000
0933	: 1110100101	18	: 10010	22	: 10110	05	: 00101
0934	: 1110100110	24	: 11000	28	: 11100	15	: 01111
0935	: 1110100111	13	: 01101	09	: 01001	26	: 11010
0936	: 1110101000	26	: 11010	30	: 11110	13	: 01101
0937	: 1110101001	15	: 01111	11	: 01011	24	: 11000
0938	: 1110101010	05	: 00101	01	: 00001	18	: 10010
0939	: 1110101011	16	: 10000	20	: 10100	07	: 00111
0940	: 1110101100	17	: 10001	21	: 10101	06	: 00110
0941	: 1110101101	04	: 00100	00	: 00000	19	: 10011
0942	: 1110101110	14	: 01110	10	: 01010	25	: 11001
0943	: 1110101111	27	: 11011	31	: 11111	12	: 01100
0944	: 1110110000	21	: 10101	17	: 10001	02	: 00010
0945	: 1110110001	00	: 00000	04	: 00100	23	: 10111
0946	: 1110110010	10	: 01010	14	: 01110	29	: 11101
0947	: 1110110011	31	: 11111	27	: 11011	08	: 01000
0948	: 1110110100	30	: 11110	26	: 11010	09	: 01001
0949	: 1110110101	11	: 01011	15	: 01111	28	: 11100
0950	: 1110110110	01	: 00001	05	: 00101	22	: 10110
0951	: 1110110111	20	: 10100	16	: 10000	03	: 00011
0952	: 1110111000	03	: 00011	07	: 00111	20	: 10100
0953	: 1110111001	22	: 10110	18	: 10010	01	: 00001
0954	: 1110111010	28	: 11100	24	: 11000	11	: 01011
0955	: 1110111011	09	: 01001	13	: 01101	30	: 11110
0956	: 1110111100	08	: 01000	12	: 01100	31	: 11111
0957	: 1110111101	29	: 11101	25	: 11001	10	: 01010
0958	: 1110111110	23	: 10111	19	: 10011	00	: 00000
0959	: 1110111111	02	: 00010	06	: 00110	21	: 10101

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0960	: 1111000000	05	: 00101	01	: 00001	18	: 10010
0961	: 1111000001	16	: 10000	20	: 10100	07	: 00111
0962	: 1111000010	26	: 11010	30	: 11110	13	: 01101
0963	: 1111000011	15	: 01111	11	: 01011	24	: 11000
0964	: 1111000100	14	: 01110	10	: 01010	25	: 11001
0965	: 1111000101	27	: 11011	31	: 11111	12	: 01100
0966	: 1111000110	17	: 10001	21	: 10101	06	: 00110
0967	: 1111000111	04	: 00100	00	: 00000	19	: 10011
0968	: 1111001000	19	: 10011	23	: 10111	04	: 00100
0969	: 1111001001	06	: 00110	02	: 00010	17	: 10001
0970	: 1111001010	12	: 01100	08	: 01000	27	: 11011
0971	: 1111001011	25	: 11001	29	: 11101	14	: 01110
0972	: 1111001100	24	: 11000	28	: 11100	15	: 01111
0973	: 1111001101	13	: 01101	09	: 01001	26	: 11010
0974	: 1111001110	07	: 00111	03	: 00011	16	: 10000
0975	: 1111001111	18	: 10010	22	: 10110	05	: 00101
0976	: 1111010000	28	: 11100	24	: 11000	11	: 01011
0977	: 1111010001	09	: 01001	13	: 01101	30	: 11110
0978	: 1111010010	03	: 00011	07	: 00111	20	: 10100
0979	: 1111010011	22	: 10110	18	: 10010	01	: 00001
0980	: 1111010100	23	: 10111	19	: 10011	00	: 00000
0981	: 1111010101	02	: 00010	06	: 00110	21	: 10101
0982	: 1111010110	08	: 01000	12	: 01100	31	: 11111
0983	: 1111010111	29	: 11101	25	: 11001	10	: 01010
0984	: 1111011000	10	: 01010	14	: 01110	29	: 11101
0985	: 1111011001	31	: 11111	27	: 11011	08	: 01000
0986	: 1111011010	21	: 10101	17	: 10001	02	: 00010
0987	: 1111011011	00	: 00000	04	: 00100	23	: 10111
0988	: 1111011100	01	: 00001	05	: 00101	22	: 10110
0989	: 1111011101	20	: 10100	16	: 10000	03	: 00011
0990	: 1111011110	30	: 11110	26	: 11010	09	: 01001
0991	: 1111011111	11	: 01011	15	: 01111	28	: 11100

BIT UTILI		CODICE		CODICE		CODICE	
		CICLICO		INFORMAZ.		SERVIZIO	
DEC	BIN	DEC	BIN	DEC	BIN	DEC	BIN
0992	1111100000	02	00010	06	00110	21	10101
0993	1111100001	23	10111	19	10011	00	00000
0994	1111100010	29	11101	25	11001	10	01010
0995	1111100011	08	01000	12	01100	31	11111
0996	1111100100	09	01001	13	01101	30	11110
0997	1111100101	28	11100	24	11000	11	01011
0998	1111100110	22	10110	18	10010	01	00001
0999	1111100111	03	00011	07	00111	20	10100
1000	1111101000	20	10100	16	10000	03	00011
1001	1111101001	01	00001	05	00101	22	10110
1002	1111101010	11	01011	15	01111	28	11100
1003	1111101011	30	11110	26	11010	09	01001
1004	1111101100	31	11111	27	11011	08	01000
1005	1111101101	19	01010	14	01110	29	11101
1006	1111101110	00	00000	04	00100	23	10111
1007	1111101111	21	10101	17	10001	02	00010
1008	1111110000	27	11011	31	11111	12	01100
1009	1111110001	14	01110	10	01010	25	11001
1010	1111110010	04	00100	00	00000	19	10011
1011	1111110011	17	10001	21	10101	06	00110
1012	1111110100	16	10000	20	10100	07	00111
1013	1111110101	05	00101	01	00001	18	10010
1014	1111110110	15	01111	11	01011	24	11000
1015	1111110111	26	11010	30	11110	13	01101
1016	1111111000	13	01101	09	01001	26	11010
1017	1111111001	24	11000	28	11100	15	01111
1018	1111111010	18	10010	22	10110	05	00101
1019	1111111011	07	00111	03	00011	16	10000
1020	1111111100	06	00110	02	00010	17	10001
1021	1111111101	19	10011	23	10111	04	00100
1022	1111111110	25	11001	29	11101	14	01110
1023	1111111111	12	01100	08	01000	27	11011

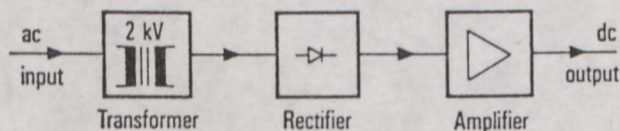


APPLICATION

Measuring transducers, as the name implies, measure and transduce the input measurand into a corresponding output signal. In the Ultrakust Measurtronic system the output is a standardised dc signal from a high impedance source and galvanically isolated from the input. This permits the connection of one or more readout systems, independent of burden, for local and/or remote measurement or telemetry, as well as paralleling for random summation of output signals independent of the paralleling burden.

MEAN VALUE MEASURING, RMS CALIBRATED
CURRENT AND VOLTAGE TRANSDUCER OPERATION

The Ultrakust Measurtronic transducers are fully solid state electronic transducers, requiring no auxilliary supply. However, transducers with live zero or suppressed zero require an auxilliary supply to maintain the live zero or suppression independent of the measured input. The transducers embody transformers, silicon transistors, high stability resistors, non electrolytic or long life electrolytic capacitors, all components being liberally rated to ensure high accuracy, long life and stability. A low voltage ac derived from either the built-in current or voltage transformer is rectified and electronically amplified, without a separate auxilliary supply, in a current compensation circuit so that the output current signal is maintained independent of the load burden or change in burden during operation. The output circuit is arranged for both current and voltage limitation so that the transducer can be run continuously with short circuited or open circuited output without damage to the transducer or the connected equipment.



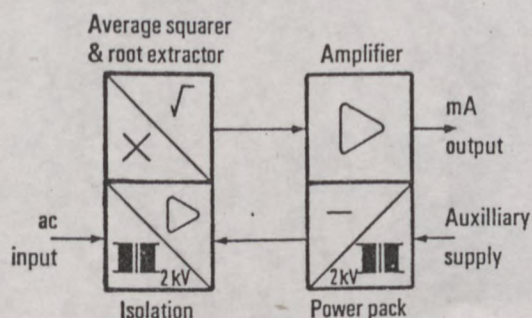
Schematic Arrangement.

Rectifier method for current and voltage transducer.

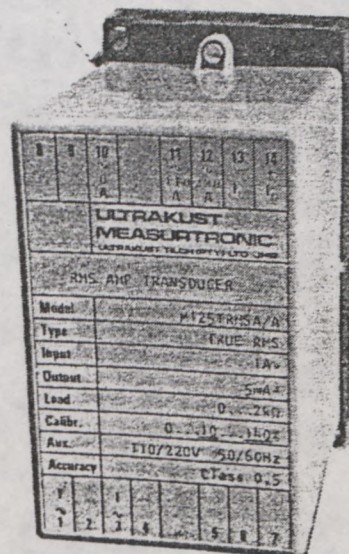
TRUE RMS TRANSDUCER OPERATION

The Ultrakust true rms transducer is a solid state device employing the principle of squaring, averaging and then extracting the square root of the signal to obtain the "Root Mean Square" of the input signal measured.

The computed signal is amplified to give a directly proportional dc output signal independent of the connected load and is circuited for both current and voltage limitation.

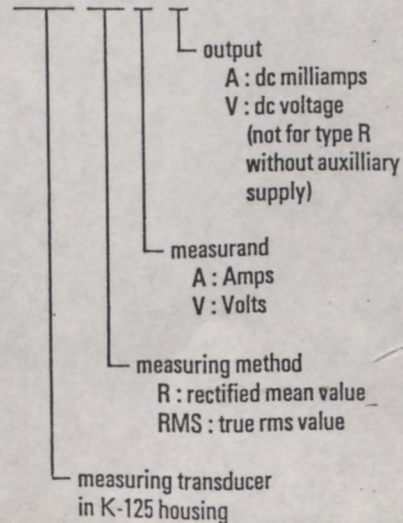


Schematic Arrangement

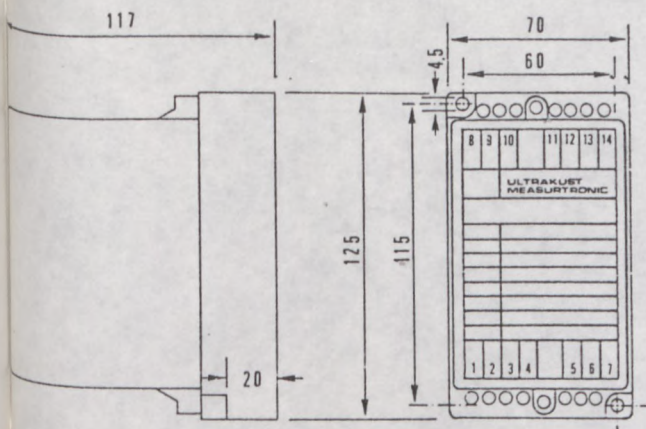


MODEL DESIGNATIONS

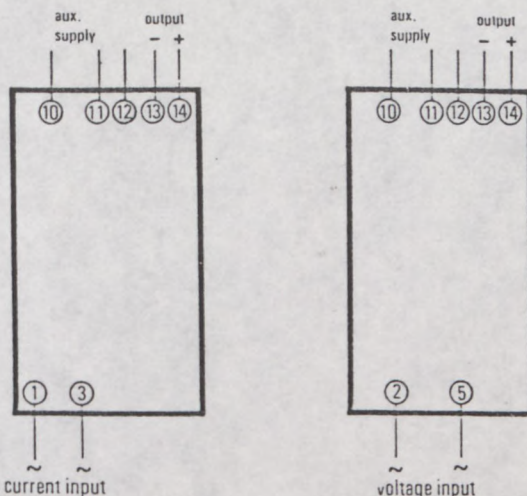
Eg., Model M125T RMS V / A



DIMENSIONS



CONNECTIONS



Dual auxiliary voltage is catered for into terminals as follows:

110V, 50/60 Hz : terminals 10 & 11
220V, 50/60 Hz : terminals 10 & 12

TECHNICAL DATA

Transducer Model	M125TRA/A	M125TRV/A	M125TRMSA/A	M125TRMSV/A
Measurand	Mean ac current RMS calibrated	Mean ac voltage RMS calibrated	True RMS ac current	True RMS ac voltage
Input	0...1 or 5A	0...110/√3, 110, 220 400, 500 or 600V	0...1 or 5A	0...110/√3, 110, 220 400, 500 or 600V
Overload	1.5x continuously 10x for 3 sec.	1.2x continuously 2x for 10 sec.	1.5x continuously 10x for 3 sec.	1.2x continuously 2x for 10 sec.
Input frequency	50 or 60 Hz	50 or 60 Hz	30...50...60...1 000 Hz	30...50...60...1 000 Hz
Frequency error		-	<0.3% over range	<0.3% over range
Input wave shape	sinusoidal	sinusoidal	arbitrary	arbitrary
Consumption	<1VA	<1VA for 5mA <2VA for 20mA	<0.3VA	<2mA
Output	0...5mA dc (other on request)	0...5mA dc (other on request)	0...5mA dc (other on request)	0...5mA dc (other on request)
Output burden voltage	10V eg., 2kΩ for 5mA	10V eg., 2kΩ for 5mA	10V eg., 2kΩ for 5mA	10V eg., 2kΩ for 5mA
Burden influence	<0.1%	<0.1%	<0.1%	<0.1%
Output ripple	<1% ptp	<1% ptp	<1% ptp	<1% ptp
Response time T80	200ms	200ms	200ms	200ms
Ambient temperature	-10...+60°C	-10...+60°C	-10...+60°C	-10...+60°C
Temperature influence	<0.2%/10°C	<0.2%/10°C	<0.2%/10°C	<0.2%/10°C
Accuracy class	1	1	0.5	0.5
Calibration accuracy range	0...10...140%	0...80...120%	0...10...140%	0...80...120%
Zero suppression range	only with aux. supply eg., 0/60...120%	only with aux. supply eg., 0/90...110%	on request eg., 0/60...120%	on request eg., 0/90...110%
Auxiliary supply	none, or 110/220V ± 20%, 50/60 Hz	none, or 110/220V ± 20%, 50/60 Hz	110/220V ± 20%, 50/60 Hz <4VA (other on request)	110/220V ± 20%, 50/60 Hz <4VA (other on request)
Insulation	2kV, 50 Hz	2kV, 50 Hz	2kV, 50 Hz	2kV, 50 Hz
Impulse withstand	5kV peak, 1/50us wave, 0.5 J	5kV peak, 1/50us wave, 0.5 J	5kV peak, 1/50us wave, 0.5 J	5kV peak, 1/50us wave, 0.5 J
Housing	Surface mounted hard plastic base with protected screw terminals for 2.5mm² conductors, with removable impact resistant grey plastic cover.			
Mass	0.6-0.7 kg	0.6-0.7 kg	0.8 kg	0.8 kg
Price	Extra price for: non-standard range live zero (eg., 4-20mA) suppressed zero (eg., 200-240V)			

MEASURTRONIC MODEL M125TW(VAR)

MT 1.4.6.2

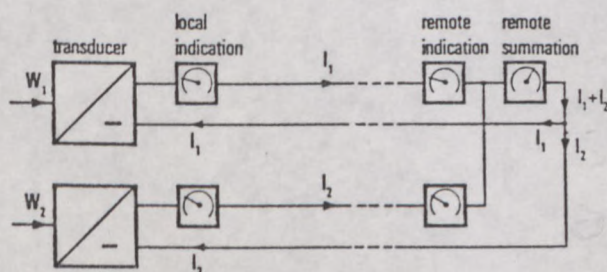
IN SURFACE MOUNTED HOUSING K-125

JULY, 1982

APPLICATION

Measuring transducers, as the name implies, measure and transduce the input measurand (single, two, two and a half or three wattmeter method) into a proportional output signal.

In the Ultrakust Measurtronic system, the output is a standardised dc signal from a high impedance source and galvanically isolated from the input. This permits the connection of one or more readout systems, independent of burden, for local and/or remote measurement or telemetry as well as the random summation of two or more measurands independent of the parallel burden. These features are of particular consequence in watt and var measurements where the multi wire power measuring circuit is converted to a two wire output telephone type circuit with substantial saving in cabling costs and instrument transformer rating where remote or multi readout measurements are made.

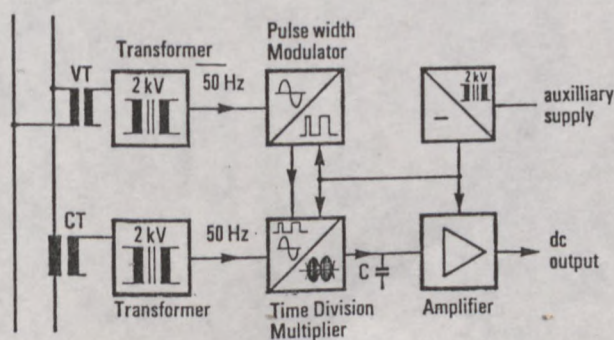


Multi readout and output summation arrangement.

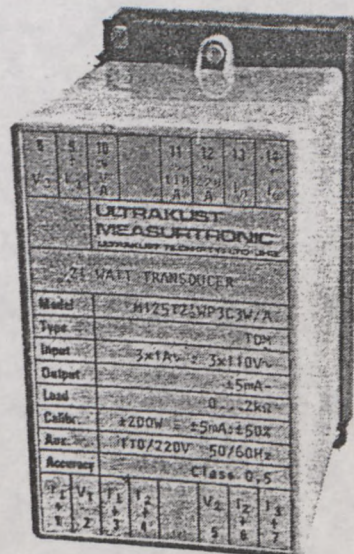
OPERATION

The Ultrakust Measurtronic transducers are fully solid state electronic transducers using C-MOS technology, IC amplifiers, silicon transistors, high stability resistors, long life capacitors and all components being liberally rated to ensure high accuracy, long life and stability.

The schematic diagram shows the arrangement for a single element watt measurement in which the transformer isolated voltage signal is pulse width modulated to chop the transformer isolated current signal to form a train of square wave pulses the height of which is proportional to the instantaneous current and the width proportional to the instantaneous voltage. The integral of this signal being the level of power measured is electronically amplified to give a dc output independent of the load and is circuited for both current and voltage limitation so that the transducer can be continuously energised with short circuited or open circuited output without damage to the transducer or connected equipment.



Schematic Arrangement



MODEL DESIGNATIONS

Eg. Model M125T 2 ½ W P 3C 3W/A

output
A : dc milliamps
V : dc voltage

voltage connections
2 : 2 wire
3 : 3 wire
4 : 4 wire

current connections
1 : 1 current circuit
2 : 2 current circuits
3 : 3 current circuits

type of measurement
S : single phase
P : polyphase

measurand
W : active power
VAR : reactive power

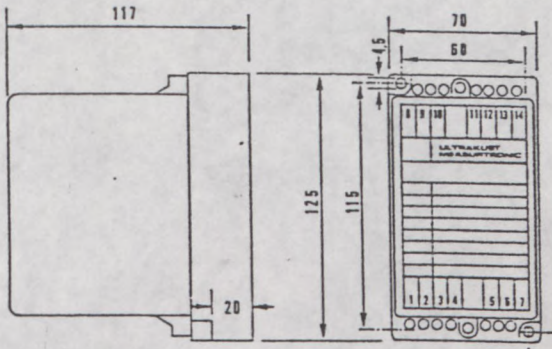
measuring method
1 : single wattmeter
2 : two wattmeter
2 ½ : two and a half wattmeter
3 : three wattmeter

Measuring transducer in K-125 housing

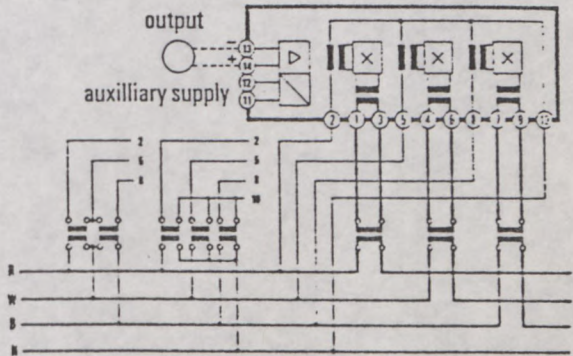
TECHNICAL DATA

Transducer Model	M125TW(VAR)
Measurand	active & reactive power
Calibration factor	as required
Input voltage	110/ $\sqrt{3}$, 110, 220, 380, 500 or 600V
Voltage overload	1,2x continuously 2x for 10 sec
Voltage path consumption	<0,5mA
Input current	1 or 5 A
Current overload	1,2x continuously 10x for 3 sec
Current path consumption	<0,2 VA
Input frequency	50/60 Hz
Output	-5 ... 0 ... +5 mA dc (20 mA or other on request)
Output limit cutoff	<2x I _n , or 18V
Output ripple	2% ptp
Output burden voltage	10V eg., 2k Ω for 5mA
Burden influence	<0,1%
Response time T80	200 ms
Permissible ambient	-10 ... +60°C
Temperature influence	<0,2%/10°C
Accuracy class	0,5
Auxilliary supply	110/220V, $\pm$ 20%, 50/60 Hz, <4VA (dc and other voltages on request)
Insulation	2 kV, 50 Hz, 1 minute
Impulse withstand	5 kV peak, 1/50us wave, 0,5J
Housing	Surface mounted hard plastic base with protected screw terminals for 2,5 mm ² conductors with removable impact proof grey plastic cover
Mass	0,6 - 0,8 kg

DIMENSIONS



CONNECTIONS



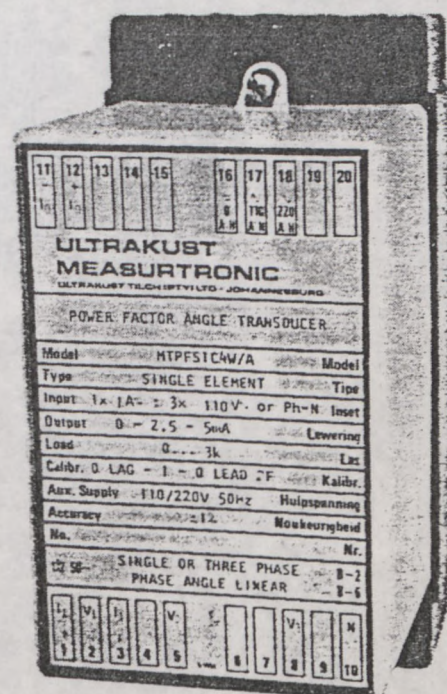
- Note: 1) The same external connection arrangement applies for both watt and var measurements. The appropriate phase shifting is arranged internally.
- 2) Single or 2 element transducers employ the same terminal numbering with the connected element terminals marked on the transducer name plate.
- 3) Dual auxilliary voltage (not for 3 elements method) is catered for into terminals as follows:
- 110V, 50/60Hz : terminals 10 & 11
220V, 50/60Hz : terminals 10 & 12

Method and Application	Measurand	Transducer Type	Price
1 element, single phase	WATT VAr	M125T1WS1C2W/A M125T1VAR1C2W/A	
1 element, 3 phase, 3 wire balanced load	WATT VAr	M125T1WP1C3W/A M125T1VAR1C3W/A	
2 element, 3 phase, 3 wire unbalanced load	WATT VAr	M125T2WP2C3W/A M125T2VAR2C3W/A	
2 1/2 element, 3 phase, 4 wire, unbalanced load	WATT VAr	M125T2 1/2 WP3C3W/A M125T2 1/2 VAR3C3W/A	
3 element, 3 phase, 4 wire, unbalanced load	WATT VAr	M125T3WP3C4W/A M125T3VAR3C3W/A	
Extra price for non standard range (e.g. live zero 4 ... 20mA)			

ULTRAKUST
INDUSTRIAL PROCESS INSTRUMENTATION

TECHNICAL DATA

Transducer Model	MTPFS1C4W/A-K182
Measurand	power factor angle
Range	- 180° ... 0 ... + 180° or part thereof, 30° minimum
Calibration zero	arbitrary
Characteristic	phase angle linear
Input current	1 or 5A
Current range	5...140%
Current overload	1,2x continuously 10x for 3 sec
Current path burden	0,2 VA
Input voltage	110/√3, 110, 220, 380, 500 or 600V
Voltage range	80 ... 120 %
Voltage overload	1,2x continuously 2x for 10 sec
Voltage path burden	4 mA
Input frequency	40 ... 50 ... 60 ... 600Hz
Input wave shape	arbitrary
Output	0 ... ± 5mA dc (20mA or other on request)
Output burden	10V eg., 2k Ω for 5mA
Burden influence	<0,1 %
Output burden voltage	2% ptp
Response time T80	200 ms
Ambient temperature	- 10 ... + 60°C
Temperature influence	<0,2%/10°C
Accuracy class	1
Auxilliary supply	110/220V ± 20%, 50/60 Hz (other on request)
Insulation	2kV, 50 Hz, 1 min.
Impulse withstand	5kV peak 1/50us wave, 0,5J
Housing	Surface mounted hard plastic base with protected screw terminals for 2,5 mm² conductor, with removable impact proof grey plastic cover
Mass	1,2 kg



APPLICATION

Measuring transducers, as the name implies, measure and transduce the input measurand into a proportional output signal. In the Ultrakust Measurtronic system, the output is a standardised dc signal from a high impedance source and galvanically isolated from the input. This permits the connection of one or more readout systems, independent of burden, for local and/or remote measurement or telemetry.

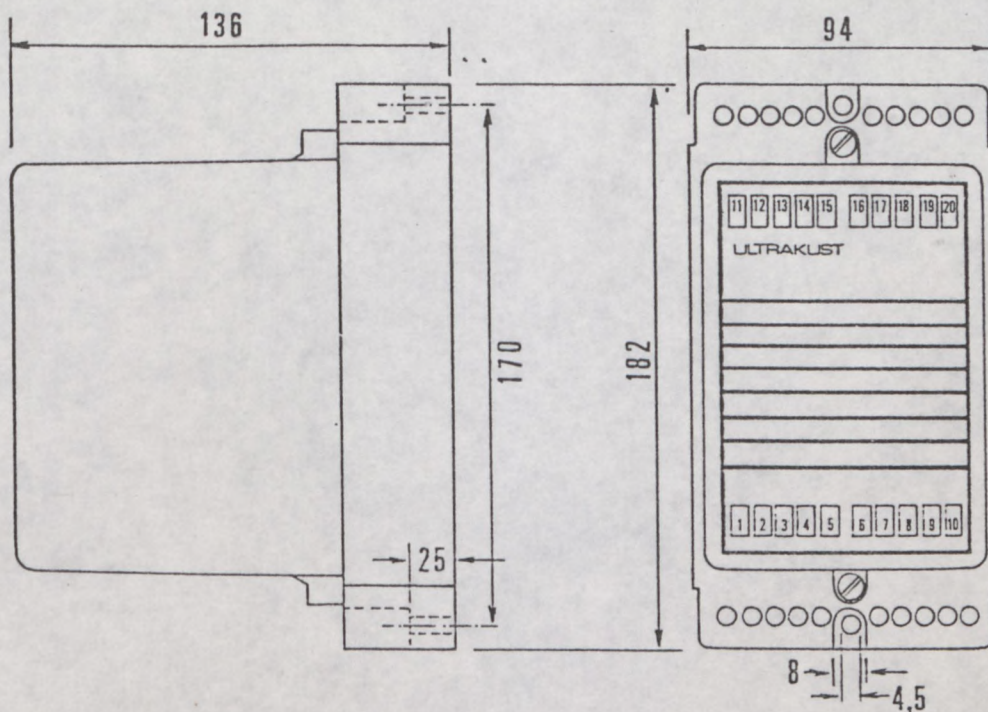
TRANSDUCER OPERATION

The Ultrakust Measurtronic power factor angle transducer is a solid state device using C-MOS logic and other high quality components. In the device the zero crossing between current and voltage, in one phase is measured to give an output proportional to the phase angle and with polarity dependent on leading or lagging phase angle. To achieve the arbitrary zero for calibration, a highly stabilised reference voltage is used to bias the output driver amplifier to the zero required for the calibration. The amplifier mA dc output current is directly proportional to the phase angle and independent of the connected load up to 10V dc voltage drop.

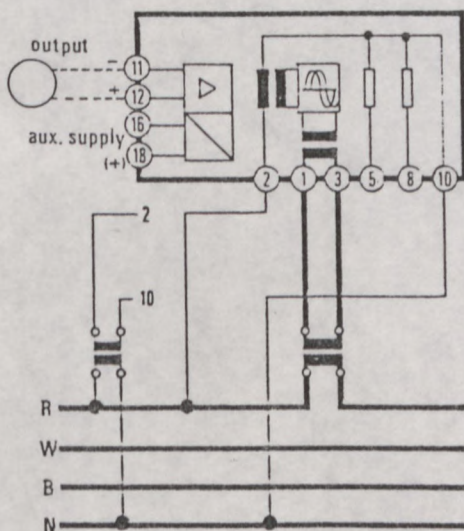
The amplifier output is circuited for both current and voltage limitation.

Also, with either or both the input current, voltage and or the auxilliary supply not being present, the transducer output will go to zero to clearly identify this fault condition.

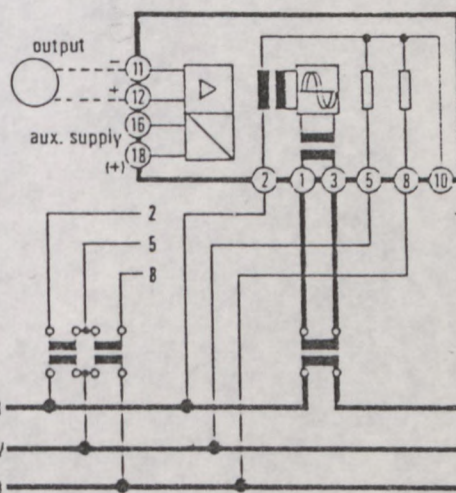
Price
Extra price for:
Non standard range
Live zero (eg., 4 - 20mA)



CONNECTIONS



Recommended Connections using phase-neutral volts.



Alternative Connections without neutral.

Star point created in all transducers.

Unbalance in system voltages leads to errors and thus the circuit on the left is recommended.

Note : Auxilliary Supply - see instrument name plate.

1 : (+) indicates polarity for dc auxilliary supply when called for.

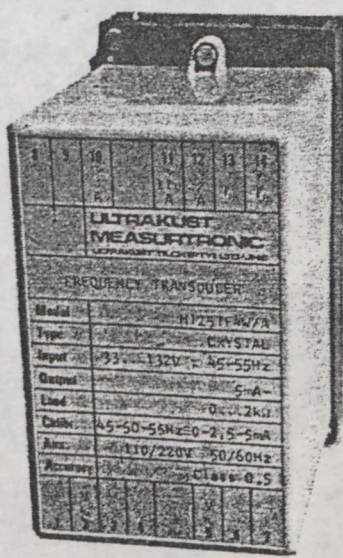
2 : Dual auxilliary voltage is catered for into terminals as follows:

110V, 50Hz: terminals 16 & 17

220V, 50Hz: terminals 16 & 18

TECHNICAL DATA

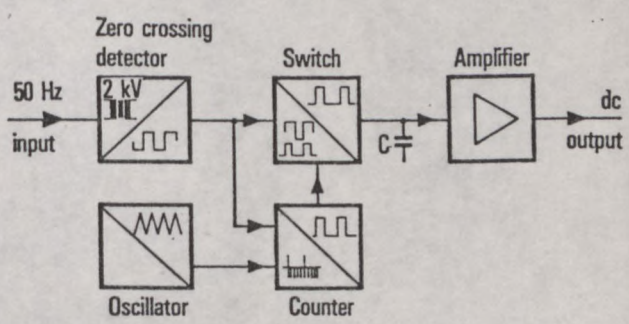
Transducer Model	M125TF2W/A M125TF4W/A (aux. supply)
Measurand	power frequency
Input voltage	110/√3, 110, 220, 380, 500 or 600V
Input voltage range	30...120%
Voltage overload	1,2x continuously 2x for 10 sec.
Input frequency	50 Hz nominal or 60 Hz
Range	45...50...55 Hz 48...50...52 Hz 49...50...51 Hz (other ranges on request)
Input wave shape	arbitrary
Consumption	<2mA
Output	0...5mA dc (20mA or other on request)
Output burden voltage	10V eg., 2kΩ for 5mA
Burden influence	<0,1%
Output ripple	<2% ptp
Response time T80	200 ms for 10 Hz span
Ambient temperature	−10... +60°C
Temperature influence	<0,2%/10°C
Accuracy class	0,5 (referred to range)
Auxilliary supply	110/220V ± 20%, 50/60 Hz <4VA (other on request)
Insulation	2 kV, 50 Hz, 1 min.
Impulse withstand	5 kV peak, 1/50us wave, 0,5J
Housing	Surface mounted hard plastic base with protected screw terminals for 2,5 mm² conductor with removable impact proof grey plastic cover.
Mass	0,6 kg



FREQUENCY TRANSDUCER OPERATION

The Ultrakust Measurtronic frequency transducer is a fully solid state crystal controlled frequency transducer either employing the measured voltage for its auxilliary supply or with a separate auxilliary supply source.

The ac measurand transformer isolated signal is applied to a zero crossing detector which gates a switch and a counter. The counter is fed from a crystal controlled oscillator and after a predetermined count the counter resets and returns the switch to its original state. The switch switches a constant voltage source to produce a train of pulses the height and width of which are constant but the period determined by the frequency measured. The integral of this zero suppressed signal is electronically amplified to give a proportional dc output signal independent of the connected load and is circuited for both output current and voltage limitation.



Schematic Arrangement.

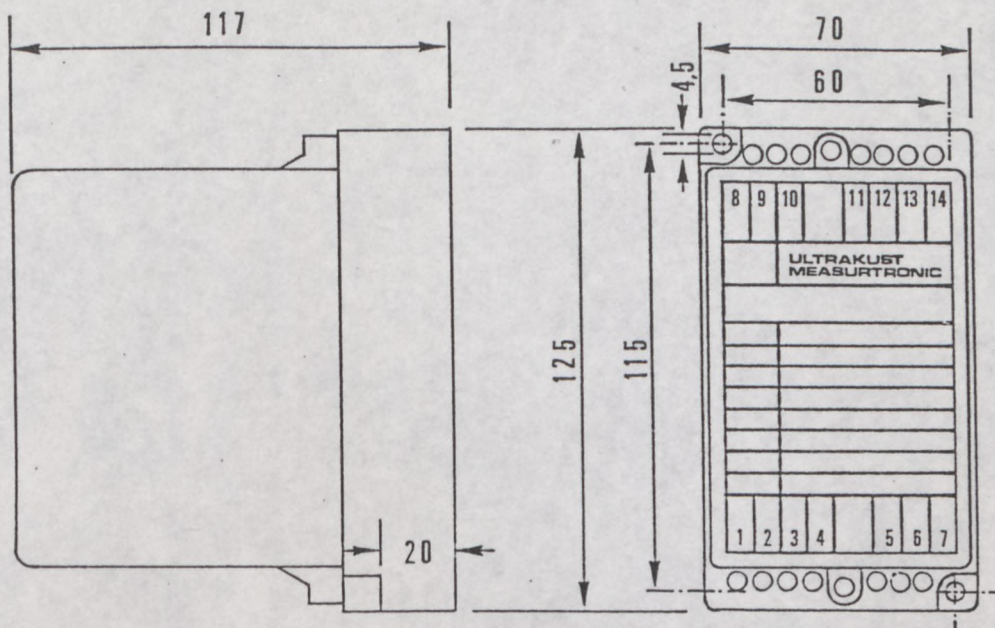
Crystal controlled frequency transducer.

Price

Extra price for:

Non standard range

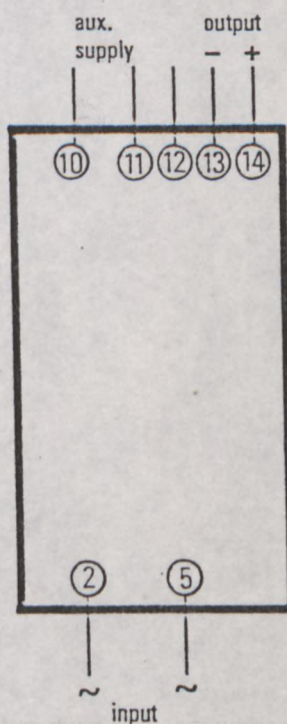
Live zero (eg., 4 - 20mA)



CONNECTIONS

Note: Auxilliary Supply—see instrument name plate.

1. For the 2 wire arrangement (no separate auxilliary supply), connection is to terminals 2 and 5 only.
The auxilliary transformer is connected internally to terminals 2 and 5 and is rated for the corresponding voltage.
2. Dual auxilliary voltage is catered for into terminals as follows:
110V, 50/60 Hz : terminals 10 & 11
220V, 50/60 Hz : terminals 10 & 12



Z80-PIO **2**

Technical Manual

1.0 INTRODUCTION

The Z-80 Parallel I/O (PIO) Circuit is a programmable, two port device which provides a TTL compatible interface between peripheral devices and the Z80-CPU. The CPU can configure the Z80-PIO to interface with a wide range of peripheral devices with no other external logic required. Typical peripheral devices that are fully compatible with the Z80-PIO include most keyboards, paper tape readers and punches, printers, PROM programmers, etc. The Z80-PIO utilizes N channel silicon gate depletion load technology and is packaged in a 40 pin DIP. Major features of the Z80-PIO include:

- Two independent 8 bit bidirectional peripheral interface ports with 'handshake' data transfer control
- Interrupt driven 'handshake' for fast response
- Any one of four distinct modes of operation may be selected for a port including:
 - Byte output
 - Byte input
 - Byte bidirectional bus (Available on Port A only)
 - Bit control mode
- All with interrupt controlled handshake
- Daisy chain priority interrupt logic included to provide for automatic interrupt vectoring without external logic
- Eight outputs are capable of driving Darlington transistors
- All inputs and outputs fully TTL compatible
- Single 5 volt supply and single phase clock are required.

One of the unique features of the Z80-PIO that separates it from other interface controllers is that all data transfer between the peripheral device and the CPU is accomplished under total interrupt control. The interrupt logic of the PIO permits full usage of the efficient interrupt capabilities of the Z80-CPU during I/O transfers. All logic necessary to implement a fully nested interrupt structure is included in the PIO so that additional circuits are not required. Another unique feature of the PIO is that it can be programmed to interrupt the CPU on the occurrence of specified status conditions in the peripheral device. For example, the PIO can be programmed to interrupt if any specified peripheral alarm conditions should occur. This interrupt capability reduces the amount of time that the processor must spend in polling peripheral status.

2.0 PIO ARCHITECTURE

A block diagram of the Z80-PIO is shown in Figure 2.0-1. The internal structure of the Z80-PIO consists of a Z80-CPU bus interface, internal control logic, Port A I/O logic, Port B I/O logic, and interrupt control logic. The CPU bus interface logic allows the PIO to interface directly to the Z80-CPU with no other external logic. However, address decoders and/or line buffers may be required for large systems. The internal control logic synchronizes the CPU data bus to the peripheral device interfaces (Port A and Port B). The two I/O ports (A and B) are virtually identical and are used to interface directly to peripheral devices.

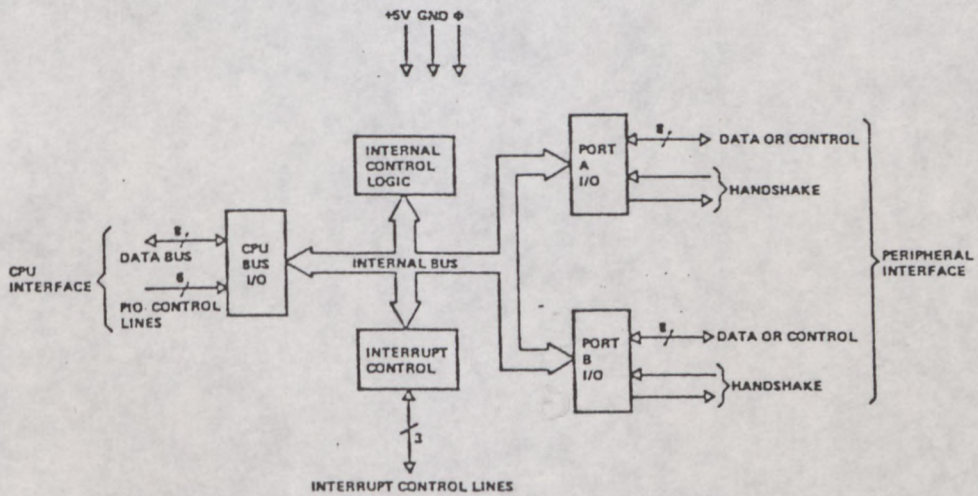


FIGURE 2.0-1
PIO BLOCK DIAGRAM

The Port I/O logic is composed of 6 registers with "handshake" control logic as shown in Figure 2.0-2. The registers include: an 8 bit data input register, an 8 bit data output register, a 2 bit mode control register, an 8 bit mask register, an 8 bit input/output select register, and a 2 bit mask control register.

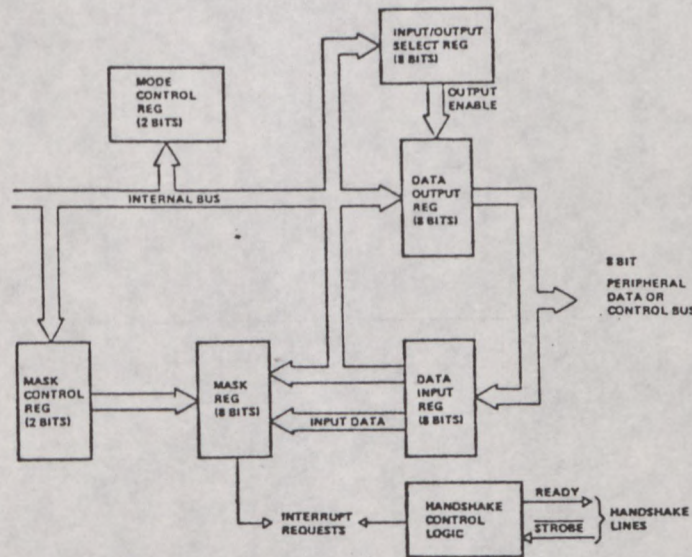


FIGURE 2.0-2
PORT I/O BLOCK DIAGRAM

The 2-bit mode control register is loaded by the CPU to select the desired operating mode (byte output, byte input, byte bidirectional bus, or bit control mode). All data transfer between the peripheral device and the CPU is achieved through the data input and data output registers. Data may be written into the output register by the CPU or read back to the CPU from the input register at any time. The handshake lines associated with each port are used to control the data transfer between the PIO and the peripheral device.

The 8-bit mask register and the 8-bit input/output select register are used only in the bit control mode. In this mode any of the 8 peripheral data or control bus pins can be programmed to be an input or an output as specified by the select register. The mask register is used in this mode in conjunction with a special interrupt feature. This feature allows an interrupt to be generated when any or all of the unmasked pins reach a specified state (either high or low). The 2-bit mask control register specifies the active state desired (high or low) and if the interrupt should be generated when *all* unmasked pins are active (AND condition) or when *any* unmasked pin is active (OR condition). This feature reduces the requirement for CPU status checking of the peripheral by allowing an interrupt to be automatically generated on specific peripheral status conditions. For example, in a system with 3 alarm conditions, an interrupt may be generated if any one occurs or if all three occur.

The interrupt control logic section handles all CPU interrupt protocol for nested priority interrupt structures. The priority of any device is determined by its physical location in a daisy chain configuration. Two lines are provided in each PIO to form this daisy chain. The device closest to the CPU has the highest priority. Within a PIO, Port A interrupts have higher priority than those of Port B. In the byte input, byte output or bidirectional modes, an interrupt can be generated whenever a new byte transfer is requested by the peripheral. In the bit control mode an interrupt can be generated when the peripheral status matches a programmed value. The PIO provides for complete control of nested interrupts. That is, lower priority devices may not interrupt higher priority devices that have not had their interrupt service routine completed by the CPU. Higher priority devices may interrupt the servicing of lower priority devices.

When an interrupt is accepted by the CPU in mode 2, the interrupting device must provide an 8-bit interrupt vector for the CPU. This vector is used to form a pointer to a location in the computer memory where the address of the interrupt service routine is located. The 8-bit vector from the interrupting device forms the least significant 8 bits of the indirect pointer while the I Register in the CPU provides the most significant 8 bits of the pointer. Each port (A and B) has an independent interrupt vector. The least significant bit of the vector is automatically set to a 0 within the PIO since the pointer must point to two adjacent memory locations for a complete 16-bit address.

The PIO decodes the RETI (Return from interrupt) instruction directly from the CPU data bus so that each PIO in the system knows at all times whether it is being serviced by the CPU interrupt service routine without any other communication with the CPU.

3.0 PIN DESCRIPTION

A diagram of the Z80-PIO pin configuration is shown in Figure 3.0-1. This section describes the function of each pin.

D_7-D_0	Z80-CPU Data Bus (bidirectional, tristate) This bus is used to transfer all data and commands between the Z80-CPU and the Z80-PIO. D_0 is the least significant bit of the bus.
B/A Sel	Port B or A Select (input, active high) This pin defines which port will be accessed during a data transfer between the Z80-CPU and the Z80-PIO. A low level on this pin selects Port A while a high level selects Port B. Often Address bit A_0 from the CPU will be used for this selection function.
C/D Sel	Control or Data Select (input, active high) This pin defines the type of data transfer to be performed between the CPU and the PIO. A high level on this pin during a CPU write to the PIO causes the Z-80 data bus to be interpreted as a <i>command</i> for the port selected by the B/A Select line. A low level on this pin means that the Z-80 data bus is being used to transfer data between the CPU and the PIO. Often Address bit A_1 from the CPU will be used for this function.
$\overline{CE}$	Chip Enable (input, active low) A low level on this pin enables the PIO to accept command or data inputs from the CPU during a write cycle or to transmit data to the CPU during a read cycle. This signal is generally a decode of four I/O port numbers that encompass port A and B, data and control.
Φ	System Clock (input) The Z80-PIO uses the standard Z-80 system clock to synchronize certain signals internally. This is a single phase clock.
$\overline{M1}$	Machine Cycle One Signal from CPU (input, active low) This signal from the CPU is used as a sync pulse to control several internal PIO operations. When $\overline{M1}$ is active and the $\overline{RD}$ signal is active, the Z80-CPU is fetching an instruction from memory. Conversely, when $\overline{M1}$ is active and $\overline{IORQ}$ is active, the CPU is acknowledging an interrupt. In addition, the $\overline{M1}$ signal has two other functions within the Z80-PIO. 1. $\overline{M1}$ synchronizes the PIO interrupt logic. 2. When $\overline{M1}$ occurs without an active $\overline{RD}$ or $\overline{IORQ}$ signal the PIO logic enters a reset state.
$\overline{IORQ}$	Input/Output Request from Z80-CPU (input, active low) The $\overline{IORQ}$ signal is used in conjunction with the B/A Select, C/D Select, $\overline{CE}$, and $\overline{RD}$ signals to transfer commands and data between the Z80-CPU and the Z80-PIO. When $\overline{CE}$, $\overline{RD}$ and $\overline{IORQ}$ are active, the port addressed by B/A will transfer data to the CPU (a read operation). Conversely, when $\overline{CE}$ and $\overline{IORQ}$ are active but $\overline{RD}$ is not active, then the port addressed by B/A will be written into from the CPU with either data or control information as specified by the C/D Select signal. Also, if $\overline{IORQ}$ and $\overline{M1}$ are active simultaneously, the CPU is acknowledging an interrupt and the interrupting port will automatically place its interrupt vector on the CPU data bus if it is the highest priority device requesting an interrupt.
$\overline{RD}$	Read Cycle Status from the Z80-CPU (input, active low) If $\overline{RD}$ is active a MEMORY READ or I/O READ operation is in progress. The $\overline{RD}$ signal is used with B/A Select, C/D Select, $\overline{CE}$, and $\overline{IORQ}$ signals to transfer data from the Z80-PIO to the Z80-CPU.

IEI	Interrupt Enable In (input, active high) This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
IEO	Interrupt Enable Out (output, active high) The IEO signal is the other signal required to form a daisy chain priority scheme. It is high only if IEI is high and the CPU is not servicing an interrupt from this PIO. Thus this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.
$\overline{\text{INT}}$	Interrupt Request (output, open drain, active low) When $\overline{\text{INT}}$ is active the Z80-PIO is requesting an interrupt from the Z80-CPU.
$A_0 - A_7$	Port A Bus (bidirectional, tristate) This 8 bit bus is used to transfer data and/or status or control information between Port A of the Z80-PIO and a peripheral device. A_0 is the least significant bit of the Port A data bus.
$\overline{\text{A STB}}$	Port A Strobe Pulse from Peripheral Device (input, active low) The meaning of this signal depends on the mode of operation selected for Port A as follows: 1) Output mode: The positive edge of this strobe is issued by the peripheral to acknowledge the receipt of data made available by the PIO. 2) Input mode: The strobe is issued by the peripheral to load data from the peripheral into the Port A input register. Data is loaded into the PIO when this signal is active. 3) Bidirectional mode: When this signal is active, data from the Port A output register is gated onto Port A bidirectional data bus. The positive edge of the strobe acknowledges the receipt of the data. 4) Control mode: The strobe is inhibited internally.
A RDY	Register A Ready (output, active high) The meaning of this signal depends on the mode of operation selected for Port A as follows: 1) Output mode: This signal goes active to indicate that the Port A output register has been loaded and the peripheral data bus is stable and ready for transfer to the peripheral device. 2) Input mode: This signal is active when the Port A input register is empty and is ready to accept data from the peripheral device. 3) Bidirectional mode: This signal is active when data is available in the Port A output register for transfer to the peripheral device. In this mode data is not placed on the Port A data bus unless $\overline{\text{A STB}}$ is active. 4) Control mode: This signal is disabled and forced to a low state.
$B_0 - B_7$	Port B Bus (bidirectional, tristate) This 8 bit bus is used to transfer data and/or status or control information between Port B of the PIO and a peripheral device. The Port B data bus is capable of supplying 1.5ma @ 1.5V to drive Darlington transistors. B_0 is the least significant bit of the bus.
$\overline{\text{B STB}}$	Port B Strobe Pulse from Peripheral Device (input, active low) The meaning of this signal is similar to that of $\overline{\text{A STB}}$ with the following exception: In the Port A bidirectional mode this signal strobes data from the peripheral device into the Port A input register.
B RDY	Register B Ready (output, active high) The meaning of this signal is similar to that of A Ready with the following exception: In the Port A bidirectional mode this signal is high when the Port A input register is empty and ready to accept data from the peripheral device.

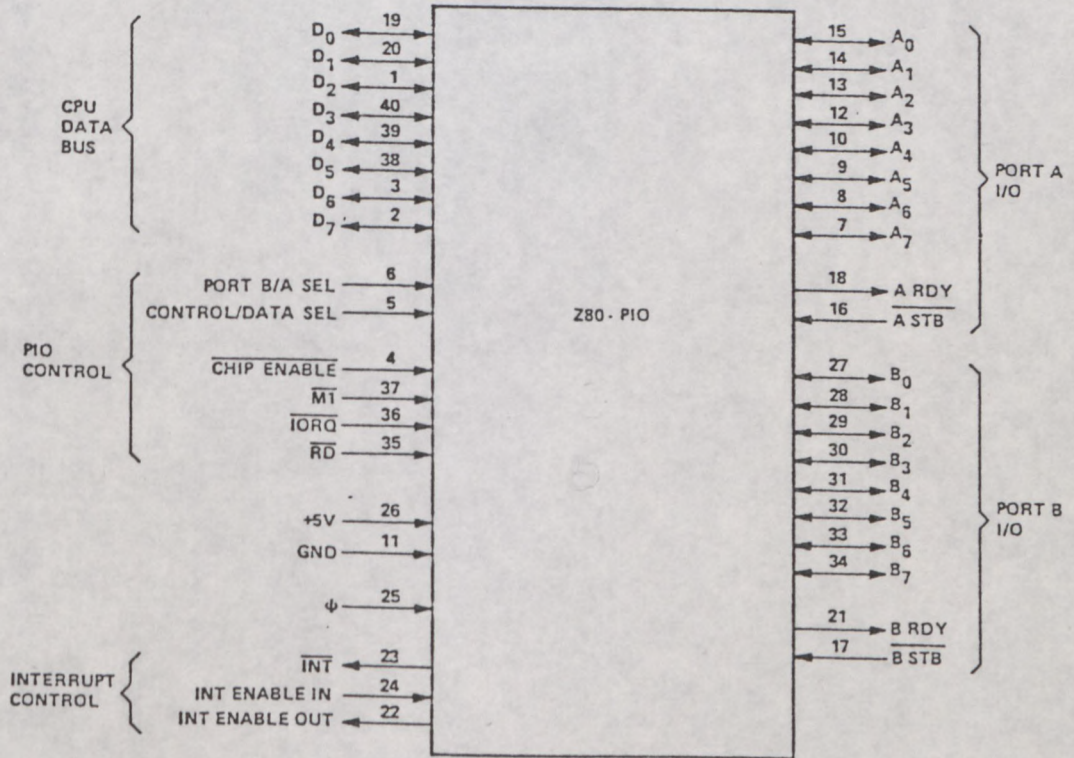


FIGURE 3.0-1
PIO PIN CONFIGURATION

4.0 PROGRAMMING THE PIO

4.1 RESET

The Z80-PIO automatically enters a reset state when power is applied. The reset state performs the following functions:

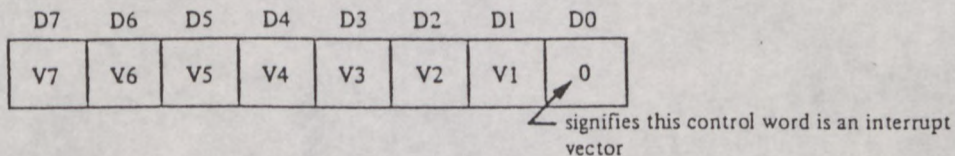
- 1) Both port mask registers are reset to inhibit all port data bits.
- 2) Port data bus lines are set to a high impedance state and the Ready "handshake" signals are inactive (low). Mode 1 is automatically selected.
- 3) The vector address registers are *not* reset.
- 4) Both port interrupt enable flip flops are reset.
- 5) Both port output registers are reset.

In addition to the automatic power on reset, the PIO can be reset by applying an $\overline{M1}$ signal without the presence of a $\overline{RD}$ or $\overline{IORQ}$ signal. If no $\overline{RD}$ or $\overline{IORQ}$ is detected during $\overline{M1}$ the PIO will enter the reset state immediately after the $\overline{M1}$ signal goes inactive. The purpose of this reset is to allow a single external gate to generate a reset without a power down sequence. This approach was required due to the 40 pin packaging limitation.

Once the PIO has entered the internal reset state it is held there until the PIO receives a control word from the CPU.

4.2 LOADING THE INTERRUPT VECTOR

The PIO has been designed to operate with the Z80-CPU using the mode 2 interrupt response. This mode requires that an interrupt vector be supplied by the interrupting device. This vector is used by the CPU to form the address for the interrupt service routine of that port. This vector is placed on the Z-80 data bus during an interrupt acknowledge cycle by the highest priority device requesting service at that time. (Refer to the Z80-CPU Technical Manual for details on how an interrupt is serviced by the CPU). The desired interrupt vector is loaded into the PIO by writing a control word to the desired port of the PIO with the following format:

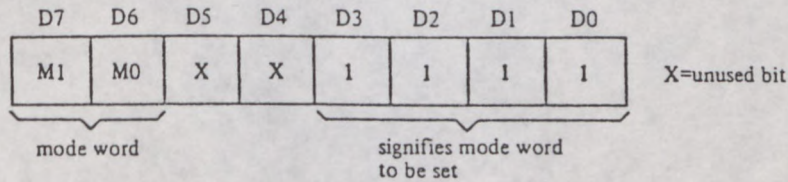


D0 is used in this case as a flag bit which when low causes V7 thru V1 to be loaded into the vector register. At interrupt acknowledge time, the vector of the interrupting port will appear on the Z-80 data bus exactly as shown in the format above.

4.3 SELECTING AN OPERATING MODE

Port A of the PIO may be operated in any of four distinct modes: Mode 0 (output mode), Mode 1 (input mode), Mode 2 (bidirectional mode), and Mode 3 (control mode). Note that the mode numbers have been selected for mnemonic significance; i.e. 0=Out, 1=In, 2=Bidirectional. Port B can operate in any of these modes except Mode 2.

The mode of operation must be established by writing a control word to the PIO in the following format:



Bits D7 and D6 from the binary code for the desired mode according to the following table:

D7	D6	Mode
0	0	0 (output)
0	1	1 (input)
1	0	2 (bidirectional)
1	1	3 (control)

Bits D5 and D4 are ignored. Bits D3-D0 must be set to 1111 to indicate "Set Mode".

Selecting Mode 0 enables any data written to the port output register by the CPU to be enabled onto the port data bus. The contents of the output register may be changed at any time by the CPU simply by writing a new data word to the port. Also the current contents of the output register may be read back to the Z80-CPU at any time through the execution of an input instruction.

With Mode 0 active, a data write from the CPU causes the Ready handshake line of that port to go high to notify the peripheral that data is available. This signal remains high until a strobe is received from the peripheral. The rising edge of the strobe generates an interrupt (if it has been enabled) and causes the Ready line to go inactive. This very simple handshake is similar to that used in many peripheral devices.

Selecting Mode 1 puts the port into the input mode. To start handshake operation, the CPU merely performs an input read operation from the port. This activates the Ready line to the peripheral to signify that data should be loaded into the empty input register. The peripheral device then strobes data into the port input register using the strobe line. Again, the rising edge of the strobe causes an interrupt request (if it has been enabled) and deactivates the Ready signal. Data may be strobed into the input register regardless of the state of the Ready signal if care is taken to prevent a data overrun condition.

Mode 2 is a bidirectional data transfer mode which uses all four handshake lines. Therefore only Port A may be used for Mode 2 operation. Mode 2 operation uses the Port A handshake signals for output control and the Port B handshake signals for input control. Thus, both A RDY and B RDY may be active simultaneously. The only operational difference between Mode 0 and the output portion of Mode 2 is that data from the Port A output register is allowed on to the port data bus only when A STB is active in order to achieve a bidirectional capability.

Mode 3 operation is intended for status and control applications and does not utilize the handshake signals. When Mode 3 is selected, the next control word sent to the PIO must define which of the port data bus lines are to be inputs and which are outputs. The format of the control word is shown below:

D7	D6	D5	D4	D3	D2	D1	D0
I/O ₇	I/O ₆	I/O ₅	I/O ₄	I/O ₃	I/O ₂	I/O ₁	I/O ₀

If any bit is set to a one, then the corresponding data bus line will be used as an input. Conversely, if the bit is reset, the line will be used as an output.

During Mode 3 operation the strobe signal is ignored and the Ready line is held low. Data may be written to a port or read from a port by the Z80-CPU at any time during Mode 3 operation. When reading a port, the data returned to the CPU will be composed of input data from port data bus lines assigned as inputs plus port output register data from those lines assigned as outputs.

4.4 SETTING THE INTERRUPT CONTROL WORD

The interrupt control word for each port has the following format:

D7	D6	D5	D4	D3	D2	D1	D0
Enable Interrupt	AND/ OR	High/ Low	Masks follows	0	1	1	1

used in Mode 3 only
signifies interrupt control word

If bit D7=1 the interrupt enable flip flop of the port is set and the port may generate an interrupt. If bit D7=0 the enable flag is reset and interrupts may not be generated. If an interrupt is pending when the enable flag is set, it will then be enabled onto the CPU interrupt request line. Bits D6, D5, and D4 are used only with Mode 3 operation. However, setting bit D4 of the interrupt control word during any mode of operation will cause any pending interrupt to be reset. These three bits are used to allow for interrupt operation in Mode 3 when any group of the I/O lines go to certain defined states. Bit D6 (AND/OR) defines the logical operation to be performed in port monitoring. If bit D6=1, an AND function is specified and if D6=0, an OR function is specified. For example, if the AND function is specified, all bits must go to a specified state before an interrupt will be generated while the OR function will generate an interrupt if any specified bit goes to the active state.

Bit D5 defines the active polarity of the port data bus line to be monitored. If bit D5=1 the port data lines are monitored for a high state while if D5=0 they will be monitored for a low state.

If bit D4=1 the next control word sent to the PIO must define a mask as follows:

D7	D6	D5	D4	D3	D2	D1	D0
MB ₇	MB ₆	MB ₅	MB ₄	MB ₃	MB ₂	MB ₁	MB ₀

Only those port lines whose mask bit is zero will be monitored for generating an interrupt.

5.0 TIMING

5.1 OUTPUT MODE (MODE 0)

Figure 5.0-1 illustrates the timing associated with Mode 0 operation. An output cycle is always started by the execution of an output instruction by the CPU. A $\overline{WR}^*$ pulse is generated by the PIO during a CPU I/O write operation and is used to latch the data from the CPU data bus into the addressed port's (A or B) output register. The rising edge of the $\overline{WR}^*$ pulse then raises the Ready flag after the next falling edge of Φ to indicate that data is available for the peripheral device. In most systems the rising edge of the Ready signal can be used as a latching signal in the peripheral device if desired. The Ready signal will remain active until: (1) a positive edge is received from the strobe line indicating that the peripheral has taken the data, or (2) if already active, Ready will be forced low $1\frac{1}{2}$ Φ cycles after the leading edge of $\overline{IORQ}$ if the port's output register is written into. Ready will return high on the first falling edge of Φ after the trailing edge of $\overline{IORQ}$. This guarantees that Ready is low when port data is changing. The Ready signal will not go inactive until a falling edge occurs on the clock (Φ) line. The purpose of delaying the negative transition of the Ready signal until after a negative clock transition is that it allows for a very simple generation scheme for the strobe pulse. By merely connecting the Ready line to the Strobe line, a strobe with a duration of one clock period will be generated with no other logic required. The positive edge of the strobe pulse automatically generates an $\overline{INT}$ request if the interrupt enable flip flop has been set and this device is the highest priority device requesting an interrupt.

If the PIO is not in a reset state, the output register may be loaded before mode 0 is selected. This allows the port output lines to become active in a user defined state.

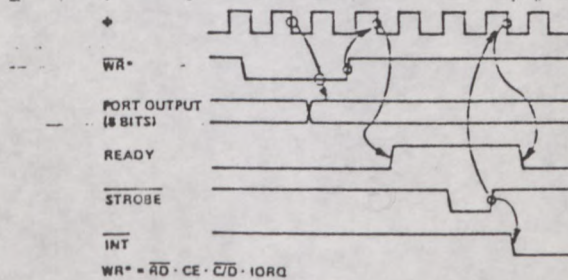


FIGURE 5.0-1
MODE 0 (OUTPUT) TIMING

5.2 INPUT MODE (MODE 1)

Figure 5.0-2 illustrates the timing of an input cycle. The peripheral initiates this cycle using the strobe line after the CPU has performed a data read. A low level on this line loads data into the port input register and the rising edge of the strobe line activates the interrupt request line ($\overline{INT}$) if the interrupt enable is set and this is the highest priority requesting device. The next falling edge of the clock line (Φ) will then reset the Ready line to an inactive state signifying that the input register is full and further loading must be inhibited until the CPU reads the data. The CPU will in the course of its interrupt service routine, read the data from the interrupting port. When this occurs, the positive edge from the CPU $\overline{RD}$ signal will raise the Ready line with the next low going transition of Φ , indicating that new data can be loaded into the PIO. If already active, Ready will be forced low one and one-half Φ periods following the leading edge of $\overline{IORQ}$ during a read of a PIO port. If the user strobes data into the PIO only when Ready is high, the forced state of Ready will prevent input register data from changing while the CPU is reading the PIO. Ready will go high again after the trailing edge of the $\overline{IORQ}$ as previously described.

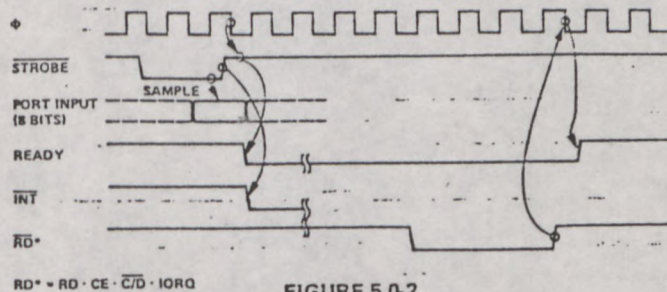


FIGURE 5.0-2
MODE 1 (INPUT) TIMING

5.3 BIDIRECTIONAL MODE (MODE 2)

This mode is merely a combination of Mode 0 and Mode 1 using all four handshake lines. Since it requires all four lines, it is available only on Port A. When this mode is used on Port A, Port B must be set to the Bit Control Mode. The same interrupt vector will be returned for a Mode 3 interrupt on Port B and an input transfer interrupt during Mode 2 operation of Port A. Ambiguity is avoided if Port B is operated in a polled mode and the Port B mask register is set to inhibit all bits.

Figure 5.0-3 illustrates the timing for this mode. It is almost identical to that previously described for Mode 0 and Mode 1 with the Port A handshake lines used for output control and the Port B lines used for input control. The difference between the two modes is that, in Mode 2, data is allowed out onto the bus only when the A strobe is low. The rising edge of this strobe can be used to latch the data into the peripheral since the data will remain stable until after this edge. The input portion of Mode 2 operates identically to Mode 1. Note that both Port A and Port B must have their interrupts enabled to achieve an interrupt driven bidirectional transfer.

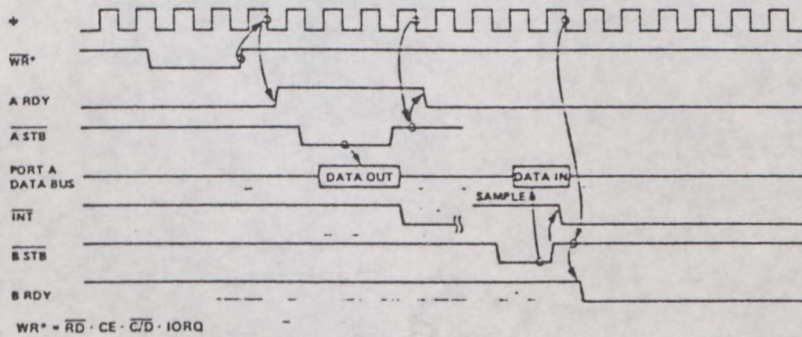


FIGURE 5.0-3
PORT A, MODE 2 (BIDIRECTIONAL) TIMING

The peripheral must not gate data onto a port data bus while $A\ STB$ is active. Bus contention is avoided if the peripheral uses $B\ STB$ to gate input data onto the bus. The PIO uses the $B\ STB$ low level to latch this data. The PIO has been designed with a zero hold time requirement for the data when latching in this mode so that this simple gating structure can be used by the peripheral. That is, the data can be disabled from the bus immediately after the strobe rising edge.

5.4 CONTROL MODE (MODE 3)

The control mode does not utilize the handshake signals and a normal port write or port read can be executed at any time. When writing, the data will be latched into output registers with the same timing as Mode 0. $A\ RDY$ will be forced low whenever Port A is operated in Mode 3. $B\ RDY$ will be held low whenever Port B is operated in Mode 3 unless Port A is in Mode 2. In the latter case, the state of $B\ RDY$ will not be affected.

When reading the PIO, the data returned to the CPU will be composed of output register data from those port data lines assigned as outputs and input register data from those port data lines assigned as inputs. The input register will contain data which was present immediately prior to the falling edge of $\overline{RD}$. See Figure 5.0-4.

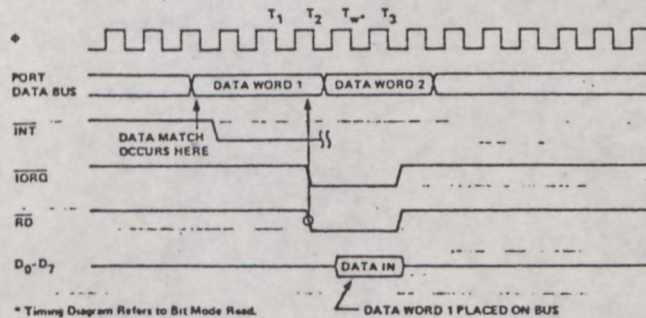


FIGURE 5.0-4

An interrupt will be generated if interrupts from the port are enabled and the data on the port data lines satisfies the logical equation defined by the 8-bit mask and 2-bit mask control registers. Another interrupt will not be generated until a change occurs in the status of the logical equation. A Mode 3 interrupt will be generated only if the result of a Mode 3 logical operation changes from false to true. For example, assume that the Mode 3 logical equation is an "OR" function. An unmasked port data line becomes active and an interrupt is requested. If a second unmasked port data line becomes active concurrently with the first, a new interrupt will not be requested since a change in the result of the Mode 3 logical operation has not occurred.

If the result of a logical operation becomes true immediately prior to or during $\overline{M1}$, an interrupt will be requested after the trailing edge of $\overline{M1}$.

6.0 INTERRUPT SERVICING

Some time after an interrupt is requested by the PIO, the CPU will send out an interrupt acknowledge ($\overline{M1}$ and $\overline{IORQ}$). During this time the interrupt logic of the PIO will determine the highest priority port which is requesting an interrupt. (This is simply the device with its Interrupt Enable Input high and its Interrupt Enable Output low). To insure that the daisy chain enable lines stabilize, devices are inhibited from changing their interrupt request status when $\overline{M1}$ is active. The highest priority device places the contents of its interrupt vector register onto the Z80 data bus during interrupt acknowledge.

Figure 6.0-1 illustrates the timing associated with interrupt requests. During $\overline{M1}$ time, no new interrupt requests can be generated. This gives time for the Int Enable signals to ripple through up to four PIO circuits. The PIO with IEI high and IEO low during $\overline{INTA}$ will place the 8-bit interrupt vector of the appropriate port on the data bus at this time.

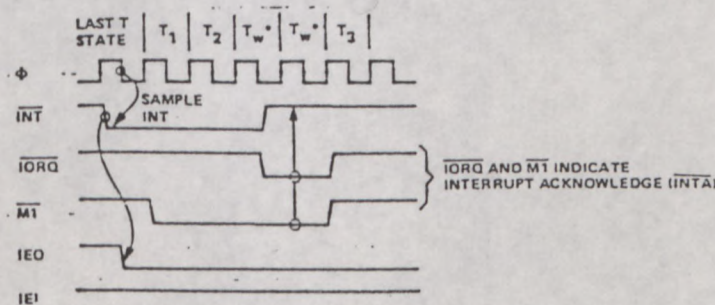


FIGURE 6.0-1
INTERRUPT ACKNOWLEDGE TIMING

If an interrupt requested by the PIO is acknowledged, the requesting port is 'under service'. $\overline{IEO}$ of this port will remain low until a return from interrupt instruction (RETI) is executed while $\overline{IEI}$ of the port is high. If an interrupt request is not acknowledged, $\overline{IEO}$ will be forced high for one $\overline{M1}$ cycle after the PIO decodes the opcode 'ED'. This action guarantees that the two byte RETI instruction is decoded by the proper PIO port. See Figure 6.0-2.

Figure 6.0-3 illustrates a typical nested interrupt sequence that could occur with four ports connected in the daisy chain. In this sequence Port 2A requests and is granted an interrupt. While this port is being serviced, a higher priority port (1B) requests and is granted an interrupt. The service routine for the higher priority port is completed and a RETI instruction is executed to indicate to the port that its routine is complete. At this time the service routine of the lower priority port is completed.

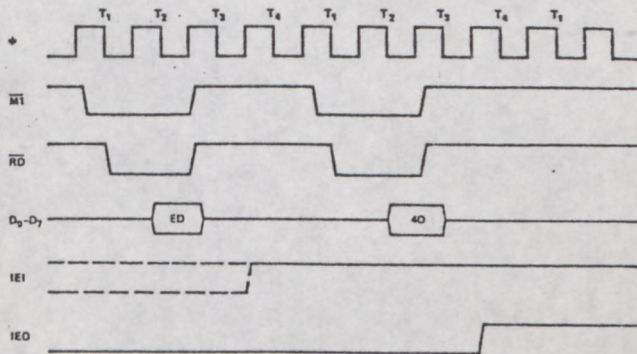


FIGURE 6.0-2
RETURN FROM INTERRUPT CYCLE

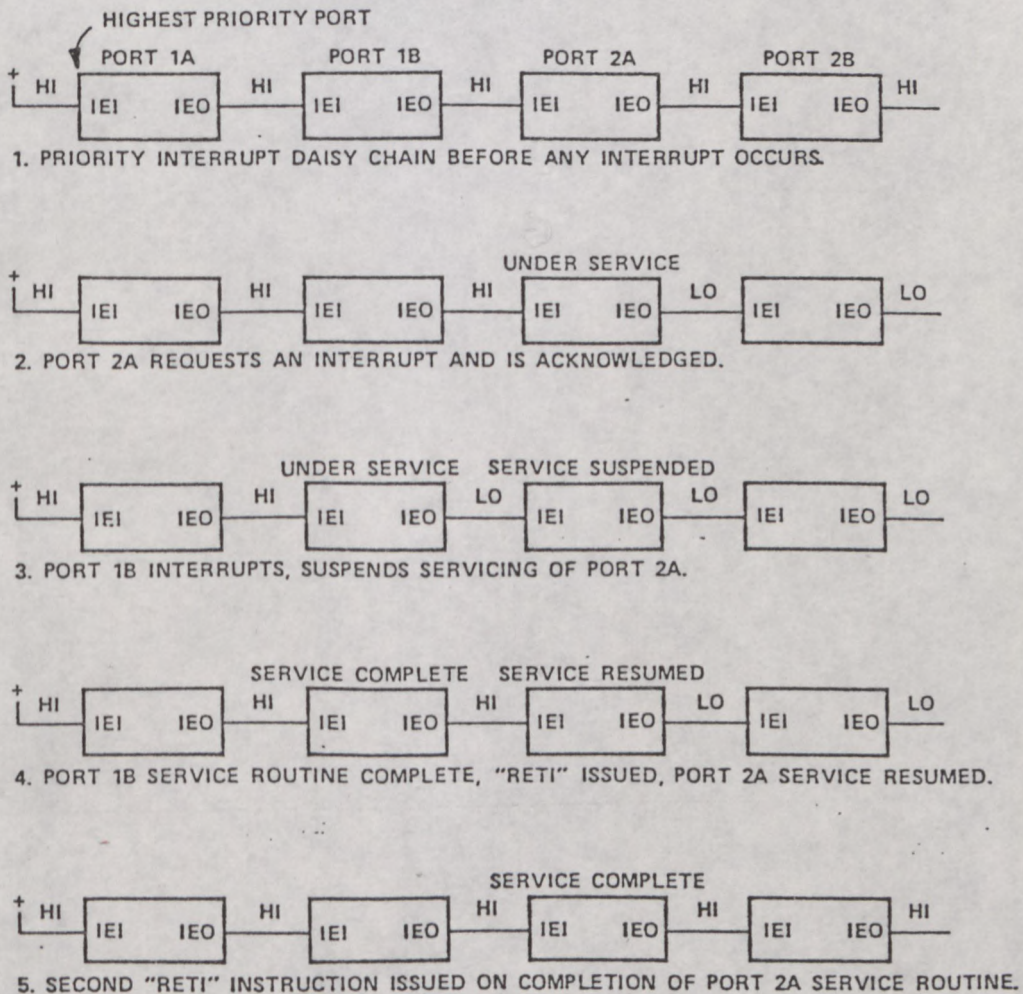


FIGURE 6.0-3
DAISY CHAIN INTERRUPT SERVICING

7.0 APPLICATIONS

7.1 EXTENDING THE INTERRUPT DAISY CHAIN

Without any external logic, a maximum of four Z80-PIO devices may be daisy chained into a priority interrupt structure. This limitation is required so that the interrupt enable status (IEO) ripples through the entire chain between the beginning of $\overline{M1}$, and the beginning of $\overline{IORQ}$ during an interrupt acknowledge cycle. Since the interrupt enable status cannot change during $\overline{M1}$, the vector address returned to the CPU is assured to be from the highest priority device which requested an interrupt.

If more than four PIO devices must be accommodated, a "look-ahead" structure may be used as shown in Figure 7.0-1. With this technique more than thirty PIO's may be chained together using standard TTL logic.

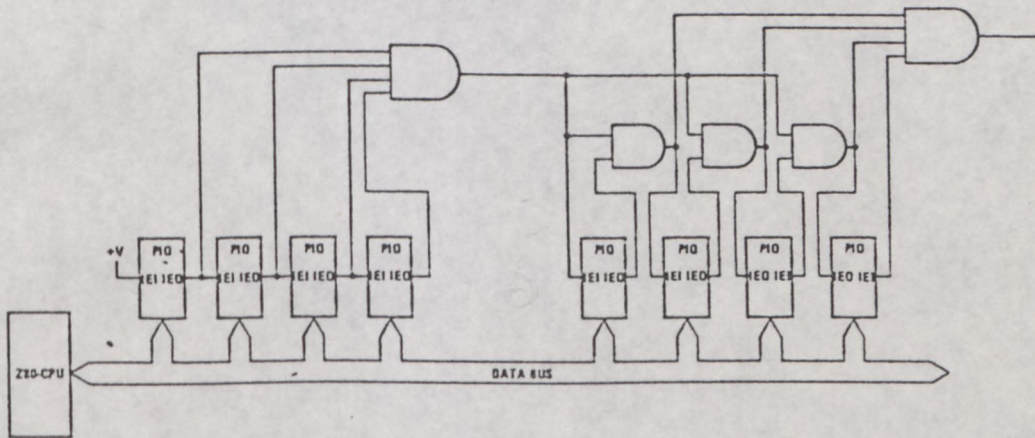


FIGURE 7.0-1
A METHOD OF EXTENDING THE INTERRUPT PRIORITY DAISY CHAIN

7.2 I/O DEVICE INTERFACE

In this example, the Z80-PIO is connected to an I/O terminal device which communicates over an 8 bit parallel bidirectional data bus as illustrated in Figure 7.0-2. Mode 2 operation (bidirectional) is selected by sending the following control word to Port A:

D7	D6	D5	D4	D3	D2	D1	D0
1	0	X	X	1	1	1	1

Mode Control

7.3 CONTROL INTERFACE

A typical control mode application is illustrated in Figure 7.0-3. Suppose an industrial process is to be monitored. The occurrence of any abnormal operating condition is to be reported to a Z80-CPU based control system. The process control and status word has the following format:

D7	D6	D5	D4	D3	D2	D1	D0
Special Test	Turn On Power	Power Failure Alarm	Halt Processing	Temp. Alarm	Turn Heaters On	Pressurize System	Pressure Alarm

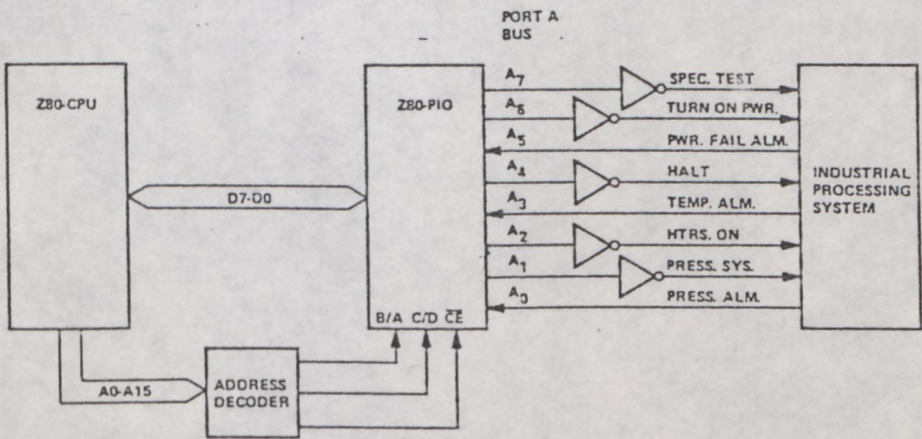


FIGURE 7.0-3
CONTROL MODE APPLICATION

The PIO may be used as follows. First Port A is set for Mode 3 operation by writing the following control word to Port A.

D7	D6	D5	D4	D3	D2	D1	D0
1	1	X	X	1	1	1	1

Whenever Mode 3 is selected, the next control word sent to the port must be an I/O select word. In this example we wish to select port data lines A5, A3 and A0 as inputs and so the following control word is written:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1

Next the desired interrupt vector must be loaded (refer to the CPU manual for details);

D7	D6	D5	D4	D3	D2	D1	D0
V7	V6	V5	V4	V3	V2	V1	0

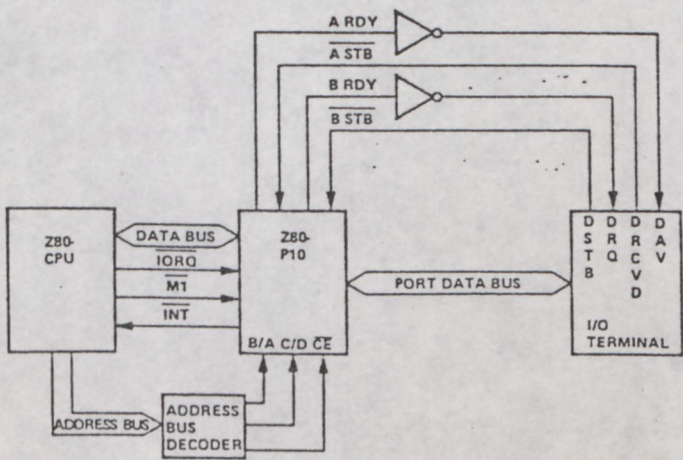


FIGURE 7.0-2
EXAMPLE I/O INTERFACE

Next, the proper interrupt vector is loaded (refer to CPU Manual for details on the operation of the interrupt).

D7	D6	D5	D4	D3	D2	D1	D0
V7	V6	V5	V4	V3	V2	V1	0

Interrupts are then enabled by the rising edge of the first $\overline{M1}$ after the interrupt mode word is set unless that $\overline{M1}$ defines an interrupt acknowledge cycle. If a mask follows the interrupt mode word, interrupts are enabled by the rising edge of the first $\overline{M1}$ following the setting of the mask.

Data can now be transferred between the peripheral and the CPU. The timing for this transfer is as described in Section 5.0.

An interrupt control word is next sent to the port:

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	1	1	1
Enable Interrupts	OR Logic	Active High	Mask Follows	Interrupt control			

The mask word following the interrupt mode word is:

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	0	1	1	0

Selects A5, A3 and A0 to be monitored

Now, if a sensor puts a high level on line A5, A3, or A0, an interrupt request will be generated. The mask word may select any combination of inputs or outputs to cause an interrupt. For example, if the mask word above had been:

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	0

then an interrupt request would also occur if bit A7 (Special Test) of the output register was set.

Assume that the following port assignments are to be used:

$E0_H$ = Port A Data

$E1_H$ = Port B Data

$E2_H$ = Port A Control

$E3_H$ = Port B Control

All port numbers are in hexadecimal notation. This particular assignment of port numbers is convenient since A_0 of the address bus can be used as the Port B/A Select and A_1 of the address bus can be used as the Control/Data Select. The Chip Enable would be the decode of CPU address bits A_7 thru A_2 (1110 00). Note that if only a few peripheral devices are being used, a Chip Enable decode may not be required since a higher order address bit could be used directly.

8.0 PROGRAMMING SUMMARY

8.1 LOAD INTERRUPT VECTOR

V7	V6	V5	V4	V3	V2	V1	0
----	----	----	----	----	----	----	---

8.2 SET MODE

M1	M0	X	X	1	1	1	1
----	----	---	---	---	---	---	---

M ₁	M ₀	Mode
0	0	Output
0	1	Input
1	0	Bidirectional
1	1	Bit Control

When selecting Mode 3, the next word must set the I/O Register:

I/O ₇	I/O ₆	I/O ₅	I/O ₄	I/O ₃	I/O ₂	I/O ₁	I/O ₀
------------------	------------------	------------------	------------------	------------------	------------------	------------------	------------------

I/O = 1 Sets bit to Input

I/O = 0 Sets bit to Output

8.3 SET INTERRUPT CONTROL

Int Enable	AND/ OR	High/ Low	Mask Follows	0	1	1	1
---------------	------------	--------------	-----------------	---	---	---	---

Used in Mode 3 only

If the "mask follows" bit is high, the next control word written to the port must be the mask:

MB ₇	MB ₆	MB ₅	MB ₄	MB ₃	MB ₂	MB ₁	MB ₀
-----------------	-----------------	-----------------	-----------------	-----------------	-----------------	-----------------	-----------------

MB = 0, Monitor bit

MB = 1, Mask bit from being monitored

Also, the interrupt enable flip flop of a port may be set or reset without modifying the rest of the interrupt control word by using the following command:

Int Enable	X	X	X	0	0	1	1
---------------	---	---	---	---	---	---	---

9.0 ELECTRICAL SPECIFICATIONS

9.1 ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Specified operating range.
Storage Temperature	-65° C to +150° C
Voltage On Any Pin With Respect To Ground	-0.3 V to +7 V
Power Dissipation	.6 W

Note: All AC and DC characteristics remain the same for the military grade parts except I_{CC} .

$I_{CC} = 130 \text{ mA. MAX}$

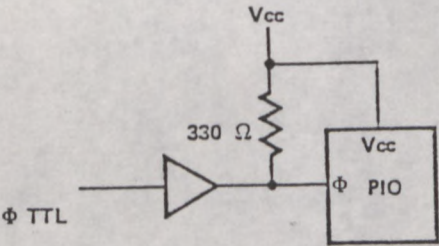
***Comment**
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9.2 D.C. CHARACTERISTICS

TA = 0° C to 70° C, Vcc = 5 V ± 5% unless otherwise specified

Symbol	Parameter	Min.	Max.	Unit	Test Condition
V _{ILC}	Clock Input Low Voltage	-0.3	0.45	V	I _{OL} = 1.8 mA I _{OH} = 250 μA T _C = 400 n sec V _{IN} = 0 to Vcc V _{OUT} = 2.4 to Vcc V _{OUT} = 0.4 V 0 ≤ V _{IN} ≤ Vcc V _{OH} = 1.5 V R _{EXT} = 390 Ω Port B Only
V _{IHC}	Clock Input High Voltage	Vcc-2	Vcc	V	
V _{IL}	Input Low Voltage	-0.3	0.8	V	
V _{IH}	Input High Voltage	2.0	Vcc	V	
V _{OL}	Output Low Voltage		0.4	V	
V _{OH}	Output High Voltage	2.4		V	
I _{CC}	Power Supply Current		70	mA	
I _{LI}	Input Leakage Current		10	μA	
I _{LOH}	Tri-State Output Leakage Current in Float		10	μA	
I _{LOL}	Tri-State Output Leakage Current in Float		-10	μA	
I _{LD}	Data Bus Leakage Current in Input Mode		±10	μA	
I _{OH(1)}	Darlington Drive Current	1.5		mA	

9.3 CLOCK DRIVER



An external pull-up resistor of 330 Ω will meet all A.C. and D.C. clock requirements.

9.4 A.C. CHARACTERISTICS

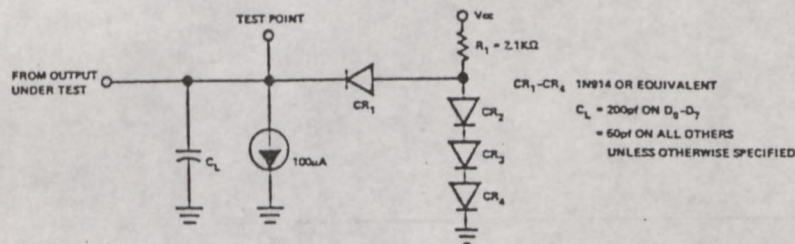
TA = 0° C to 70° C, Vcc = +5 V ± 5%, unless otherwise noted

Signal	Symbol	Parameter	Min.	Max.	Unit	Comments
Φ	t_c	Clock Period	.4	[1]	μ sec	[1] $t_c = t_w(\Phi H) + t_w(\Phi L) + t_r + t_f$
	$t_w(\Phi H)$	Clock Pulse Width, Clock High	180	2000	nsec	
	$t_w(\Phi L)$	Clock Pulse Width, Clock Low	180	2000	nsec	
	t_r, t_f	Clock Rise and Fall Times		30	nsec	
D ₀ -D ₇	$t_{HW}(D)$	Data Hold Time During Write Cycle	0		nsec	
	$t_{HR}(D)$	Data Hold Time From Rising Edge of $\overline{RD}$ During M1 Cycle	0		nsec	
	$t_{DR}(D)$	Data Output Delay During Read Cycle		430	nsec	
	$t_{DI}(D)$	Data Output Delay During INTA		[2]	nsec	
	$t_F(D)$	Delay to Floating Bus During Read Cycle		160	nsec	
	$t_S(D)$	Data Setup Time to Rising Edge of $\overline{IORQ}$ During Write Cycle	200		nsec	
	$t_{\Phi}(D)$	Data Setup Time to Rising Edge of Clock During M1 Cycle	50		nsec	
A ₀ -A ₇ , B ₀ -B ₇	$t_H(PD)$	Port Data Hold Time From Rising Edge of $\overline{STROBE}$	0		nsec	Mode 1
	$t_S(PD)$	Port Data Setup Time to Rising Edge of $\overline{STROBE}$	260		nsec	Mode 1
	$t_{DS}(PD)$	Port Data Output Delay From Falling Edge of $\overline{STROBE}$		230	nsec	Mode 2
	$t_F(PD)$	Delay to Floating Port Data Bus From Rising Edge of $\overline{STROBE}$	200		nsec	Mode 2
	$t_{DI}(PD)$	Port Data Stable From Rising Edge of $\overline{IORQ}$ During Write Cycle		200	nsec	Mode 0
B/A, C/D, $\overline{CE}$	$t_H(CS)$	Control Signal Hold Time From Rising Edge of $\overline{IORQ}$	0		nsec	
	$t_S(CS)$	Control Signal Setup Time to Falling Edge of $\overline{IORQ}$	30		nsec	
A $\overline{STB}$, B $\overline{STB}$	$t_w(ST)$	Pulse Width, $\overline{STROBE}$	150		nsec	Mode 0 or 1
			[3]		nsec	Mode 2 Output [3] $t_w(ST) > t_S(PD)$
$\overline{INT}$	$t_D(IT)$	$\overline{INT}$ Delay Time From Rising Edge of $\overline{STROBE}$		490	nsec	Mode 0, 1 or 2
	$t_D(IT3)$	$\overline{INT}$ Delay Time From Data Match During Mode 3 Operation		420	nsec	Mode 3
IEI	$t_S(IEI)$	Setup Time Of IEI Prior To $\overline{IORQ}$ During Interrupt Acknowledge	0		nsec	
IEO	$t_{DL}(IO)$	IEO Delay Time From Falling Edge of IEI		210	nsec	
	$t_{DH}(IO)$	IEO Delay Time From Rising Edge of $\overline{RD}$ During RETI		$1.5t_c + 500$	nsec	
	$t_{DM}(IEO)$	Delay Time From Falling Edge of $\overline{M1}$ To Falling Edge of IEO		310	nsec	
A RDY or B RDY	$t_{DH}(RY)$	READY Response Time From Rising Edge of $\overline{IORQ}$		$t_c + 460$	nsec	
	$t_{DL}(RY)$	READY Response Time From Rising Edge of $\overline{STROBE}$		$t_c + 400$	nsec	

[2] 380 ns for C_L = 100pF; 410 ns for C_L = 200pF

[4] $2.5 t_c > (N-2)t_{DL}(IO) + t_{DM}(IEO) + t_s(IEI) + \text{TTL buffer delay, if any}$
where N = number of PIO's in daisy chain

Output load circuit.



9.5 CAPACITANCE

TA = 25° C, f = 1 MHz

Symbol	Parameter	Max.	Unit	Test Condition
C_Φ	Clock Capacitance	10	pF	Unmeasured Pins Returned to Ground
C_{IN}	Input Capacitance	5	pF	
C_{OUT}	Output Capacitance	10	pF	

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