DEDICATED UNIVERSAL MICROCOMPUTER SYSTEM

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Cape Technikon
Kaapse Technikon

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DEDICATED UNIVERSAL MICROCOMPUTER SYSTEM FOR THE DEPARTMENT OF MECHANICAL ENGINEERING OF THE UNIVERSITY OF STELLENBOSCH.

C.P. WALSER

Dedicated Universal Microcomputer System for the Department of Mechanical Engineering of the University of Stellenbosch.

C.P. WALSER.

This report will be handed in to comply partially for the Diploma in Technology at the School for Electrical Engineering at the

CAPE TECHNIKON.

Handed in on 13 June 1988.

DECLARATION.

This report has been generated only by myself and compiled from the literature as shown in the appendix.

The opinions expressed in this report is explicitly my own and not necessarly that of the Cape Technikon.

ACKNOWLEDGEMENTS.

I would like to thank the following people for their assistance in materialising this report.

1. The Department for Mechanical Engineering of the University of Stellenbosch for giving me the opportunity to do this project.

2. Mr E. Terblanche of the University of Stellenbosch for his support and guidance.

3. Mr C. Rudolf of the Cape Technikon for his help, guidance and encouragement.

4. Mr N. Beute and P. Kleinhans of the Cape Technikon for their help and support in the abscence of Mr C. Rudolf.

INDEX.

INTRODUCTION.

The Department of Mechanical Engineering at the University of Stellenbosch developed the need for an intelligent controller for their well equiped laboratories. The system had to be dedicated only to their mechanical laboratories, but with universal characteristics, to adapt the system for a number of applications on various experiments.

The system had to be:

1. Universal to fit most experiments.
2. Programmable.
3. Fast control system.
4. Dedicated to one experiment at a time.
5. Long control time intervals.
6. Reliable system which can withstand harsh electrical interference.

The microprocessor, with its ability to perform a wide variety of different functions and being programmable was the answer. It could be obtained at low cost and coupled via suitable

interface circuits to a wide variety of external devices.

A small Motorola MEK6802D3 microprocessor kit was already available at the Department for Mechanical Engineering of the University of Stellenbosch.

It was decided to upgrade this system and use it as the central processor.

The following specifications were compiled:

1. ASCII keyboard input, video monitor and printer output.

2. Editor, Debugger and Assembler programs must be on ROM.

3. RS 232 cassette tape recorder.

4. Real Time Clock for date and time monitoring up to three weeks or longer for control applications.

5. 32k RAM memory with battery backup and power fail detection for fast data storage in the event of a power failure.

6. All programs had to be developed for control applications over long control intervals. An Eprom programmer was required to obtain reliable program loading and

functioning.

7. Eight analog to digital converters for multi channel monitoring. Input voltage ±15v, ±0,5% accuracy. This allowed for an eight bit converter giving 0,4% accuracy.
It must be interfaced with a M6802.
TTL compatible.
Three state data output port.
Clock must be faster than 0,8MHz for fast conversion.

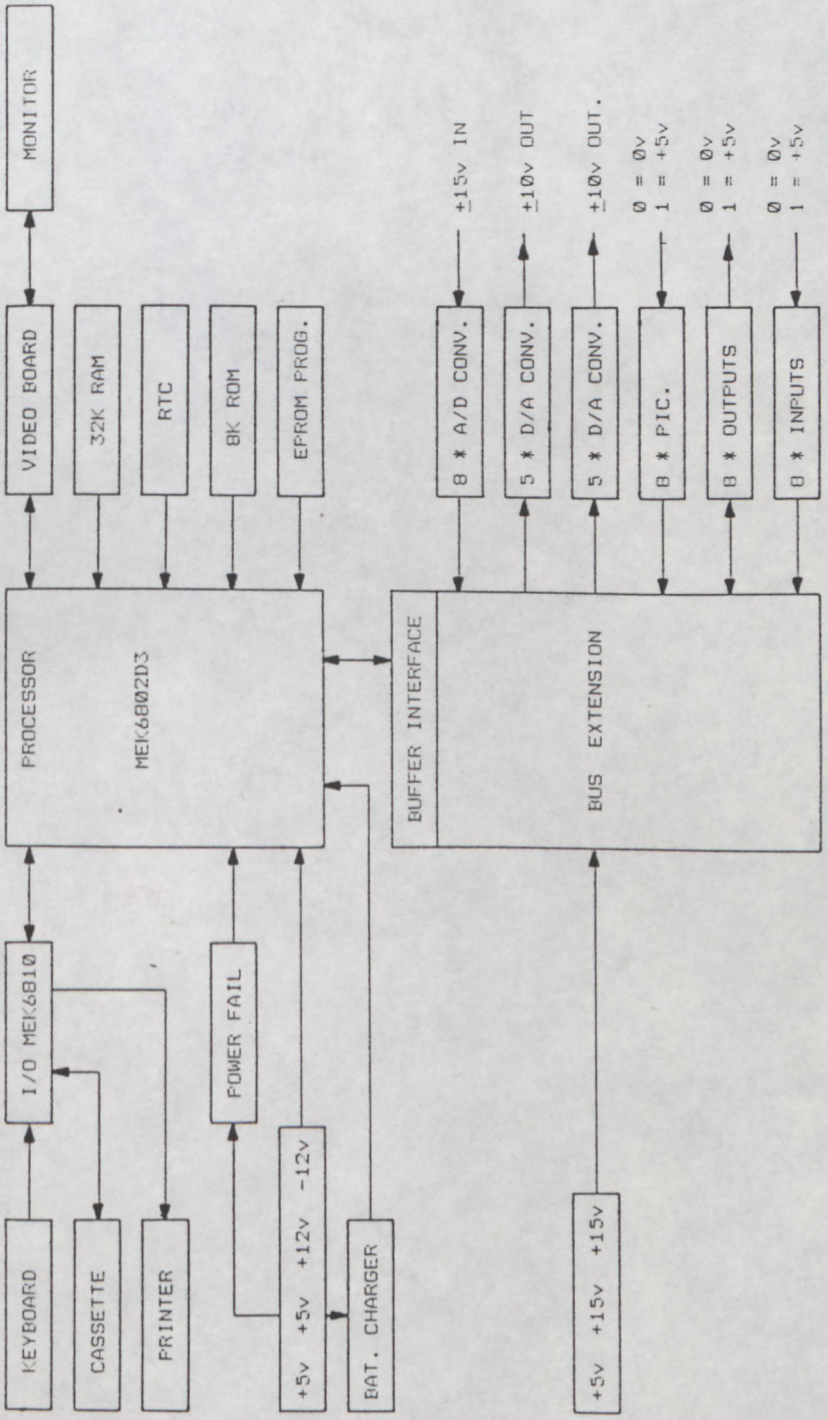
8. Ten digital to analog converters for multi channel control.
Output voltage ±10v, ±1mA current source.
Accuracy ±1%.
Settling time of 1ms.

9. Eight logical input lines and eight logical output lines must be available for turning devices ON and OFF. These lines will mostly drive relays to interface with the control systems.

10. Eight channel priority interrupt controller for the monitoring of important events in a control enviroment.
TTL compatible.

FIG. 1, display the block diagram of this universal microcomputer design.

FIG1. SYSTEM BLOCK DIAGRAM.



The following objectives had to be obtained in the documentation of this report:

1. The University of Stellenbosch requires a complete faultfinding and maintenance manual for the total system.

   This resulted in writing a complete manual for each card designed. Each of these manuals contain the basic design information and all data sheets of the hardware for the use of repair tradesman or technicians. Seven of these manuals were written and are refered to the APPENDIX in each section of this report.

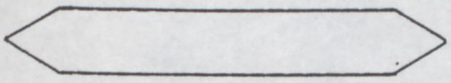
2. The idea was also to make this report useful for lecture purposes.

   This resulted that many basic concepts were incorporated into the APPENDIX of every card designed. However, this main report does not contain the very basic concepts.

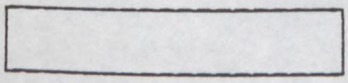
3. This report does not contain the complete circuit diagrams and PCB information, but these topics are contained in the APPENDIX of each card.

4. Every APPENDIX of each card was kept separate from one another to achieve easy access to the relative information that could be required.

5. The following two symbols simplified the flow charts so that more information could be fitted onto a single page.



Decision making instruction symbol.



Any other operational instruction.

1. THE MICROCOMPUTER SYSTEM.

The MEK6802D3 Motorola single board computer was the basic building block for the whole universal computer system. The MEK6802D3 has the following features.

1. 256 Bytes of user RAM.

2. 128 Bytes of ROM containing the operating system.

3. 2k ROM containing the debugger, D3BUG.

4. I/O port accessible through a 16 pin socket.

5. Supports eight levels of memory paging.

6. System bus allows expansion.

The MEK6802D3 with its limited capabilities was upgraded to a much more powerful system. The expansion boards already available from the University of Stellenbosch were the following.

1. MEK6810 input/output module. This board supported the RS232 interface for the printer and the 300 baud Kansas City Standard for the audio cassette interface.

2. MEK68R2M programmable CRT interface for the video monitor.

3. MEK68RR RAM ROM card to help in upgrading the system.

The following designs were attempted and constructed to upgrade this universal controller to a powerful laboratory control instrument.

1. Extension rack buffer card.

2. EPROM programmer for 2716 and 2732 EPROM's.

3. Real Time Clock, keeping track of date and time.

4. 32k Fast RAM memory with battery backup in the event of power failures and Power Fail Detector.

5. 16k EPROM for control program storage.

6. 8 Channel A/D converters.

7. 10 Channel D/A converters.

8. 8 Logic level input lines.

9. 8 Logic level output lines.

10. 8 Logic level priority interrupt controller lines.

The microprocessor was first tested as a single board computer and then gradually upgraded to the expanded system as mentioned.

The system is housed inside two standard 19 inch sliding cabinets. The processor related cards are housed in the top rack and the interface cards to the control device inside the second rack. Each rack is supplied with its own power supply as shown in FIG 2 .

1.1 GENERAL INFORMATION.

All the technical design and operation features of this section are contained in the seperate appendix called **MICROPROCESSOR.**

This appendix supplies:

1. Background to the designs.

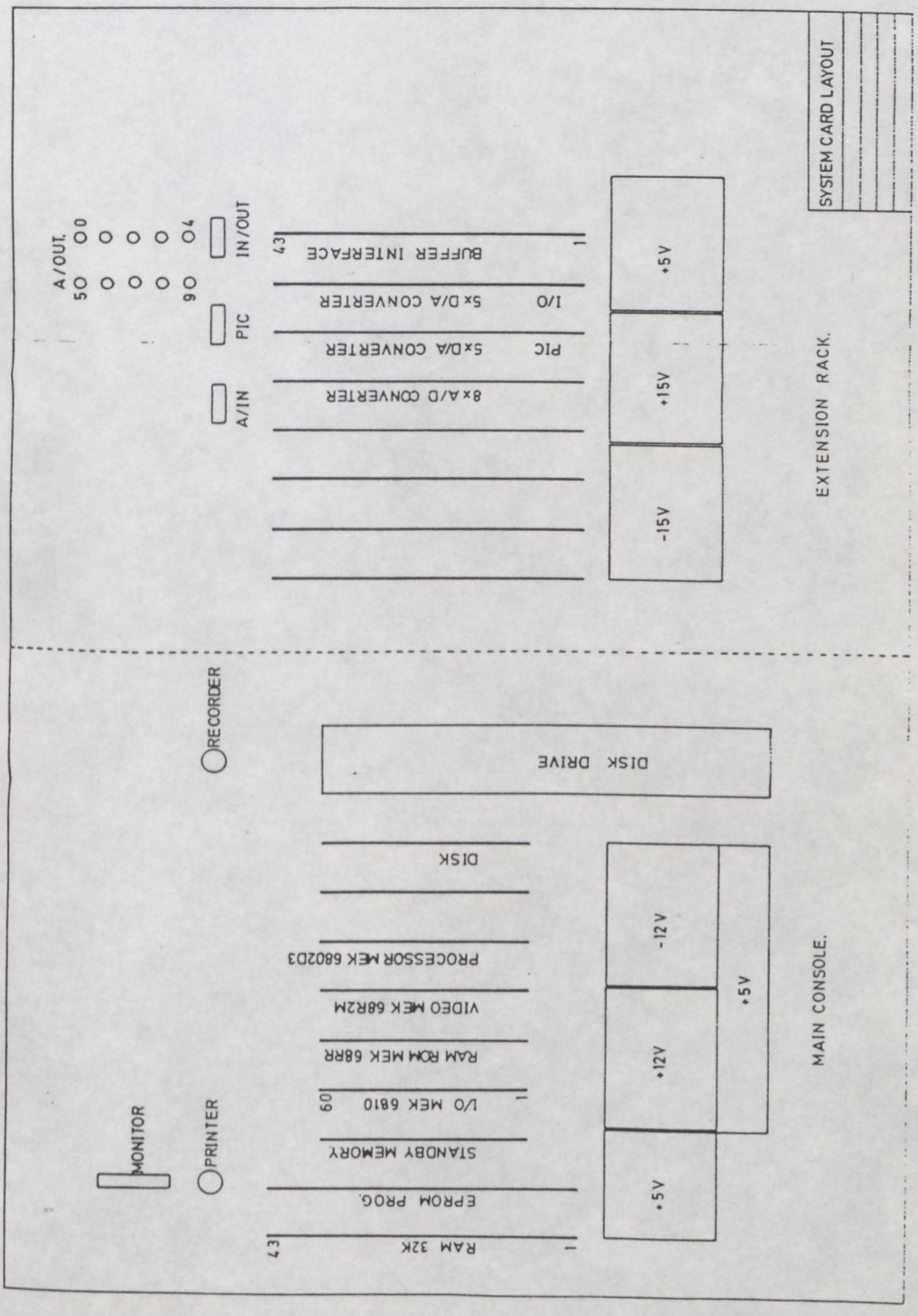
2. Complete design and circuit diagrams.

3. Wire wrap boards.

4. Test programs with flow charts and program listings.

5. All data sheets on the components used in the design.

FIG 2. SYSTEM CARD LAYOUT.



2. THE MEMORY SYSTEM.

The following features are incorporated into the design:

1. Parallel addressing for fast memory access.

2. 32k RAM memory.

3. Common 2k RAM for the use on all the memory pages of the system.

4. Battery standby power for all memory cards. CMOS design for low power dissipation.

5. 16k EPROM memory for the use of storing application programs reliably in the system.

6. Memory address decoding should be easy to change when necessary.

The following memory locations are used by the system.

On system page "ZERO".

RAM	$0000	to	$3FFF	16k
EPROM	$4000	to	$5FFF	8k
RAM	$6000	to	$7FFF	8k
RAM	$A000	to	$BFFF	8k
EPROM	$C000	to	$DFFF	8k

The RAM memory for common use on all memory pages:

RAM	$81FF	to	$87FF	2k

This whole design is done with wire wrapping technique for easy_ address decoder change when required.

2.1 SYSTEM MEMORY MAP.

The memory map of the MEK6802D3 was used and adapted for the total control system. All the memory addresses are indicated on the memory map in FIG. 3 and FIG. 4 .

The main feature of this design is the eight memory page system.

FIG 3. SYSTEM MEMORY MAP.

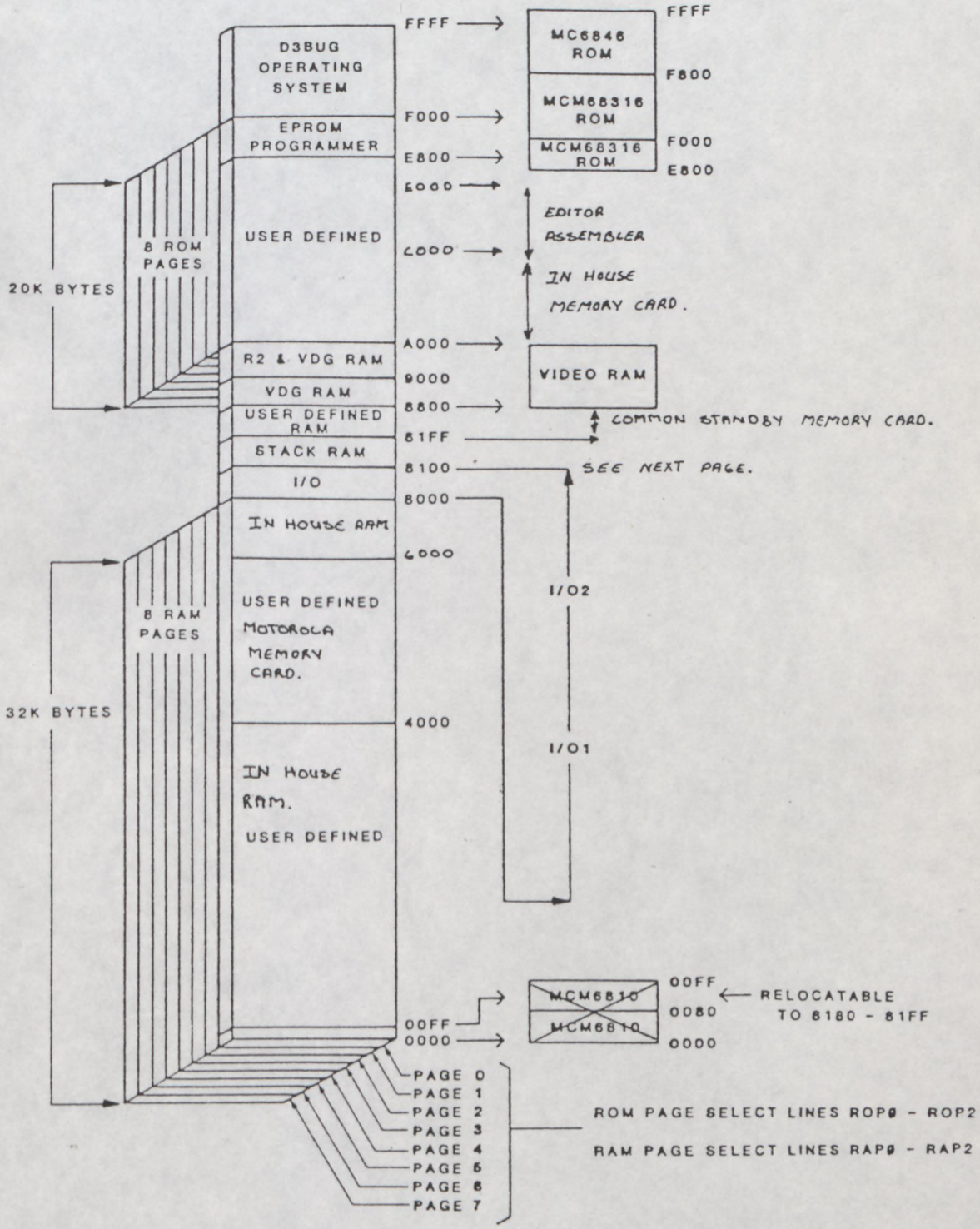
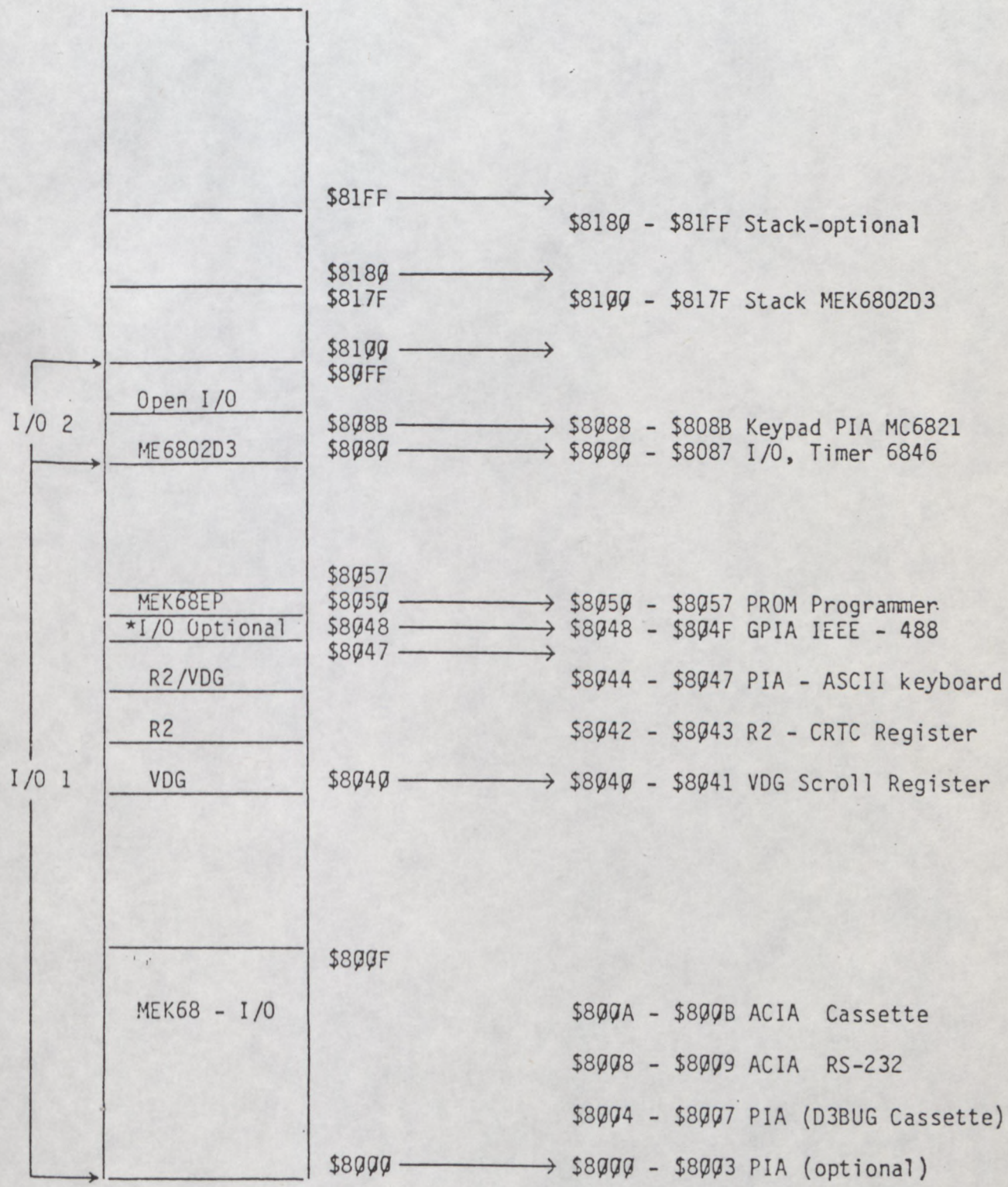


FIG 4. SYSTEM MEMORY MAP.



2.2 MEMORY BLOCK DIAGRAM.

The block diagram, FIG. 5 illustrates the basic design of the two memory cards.

The main function of the 32k RAM card is to store the control data compiled by the system, while the common memory is used by all the memory pages in the system.

2.3 MEMORY PERFORMANCE.

Memory access time is within 300ns and the standby current with an applied voltage of 2,4v is 5µA/IC.

Thus the total current drain is:

$$5*20 = 100\mu A.$$

The NI-CAD cell is a 0,6Ah battery giving a storage time of:

$$0,6/100*10^{-6} = 6000h$$

Changeover to battery power occurs already on a supply voltage of +4v. This characteristic allows for continuous power on the memory circuits.

FIG 5. MEMORY BLOCK DIAGRAMS.

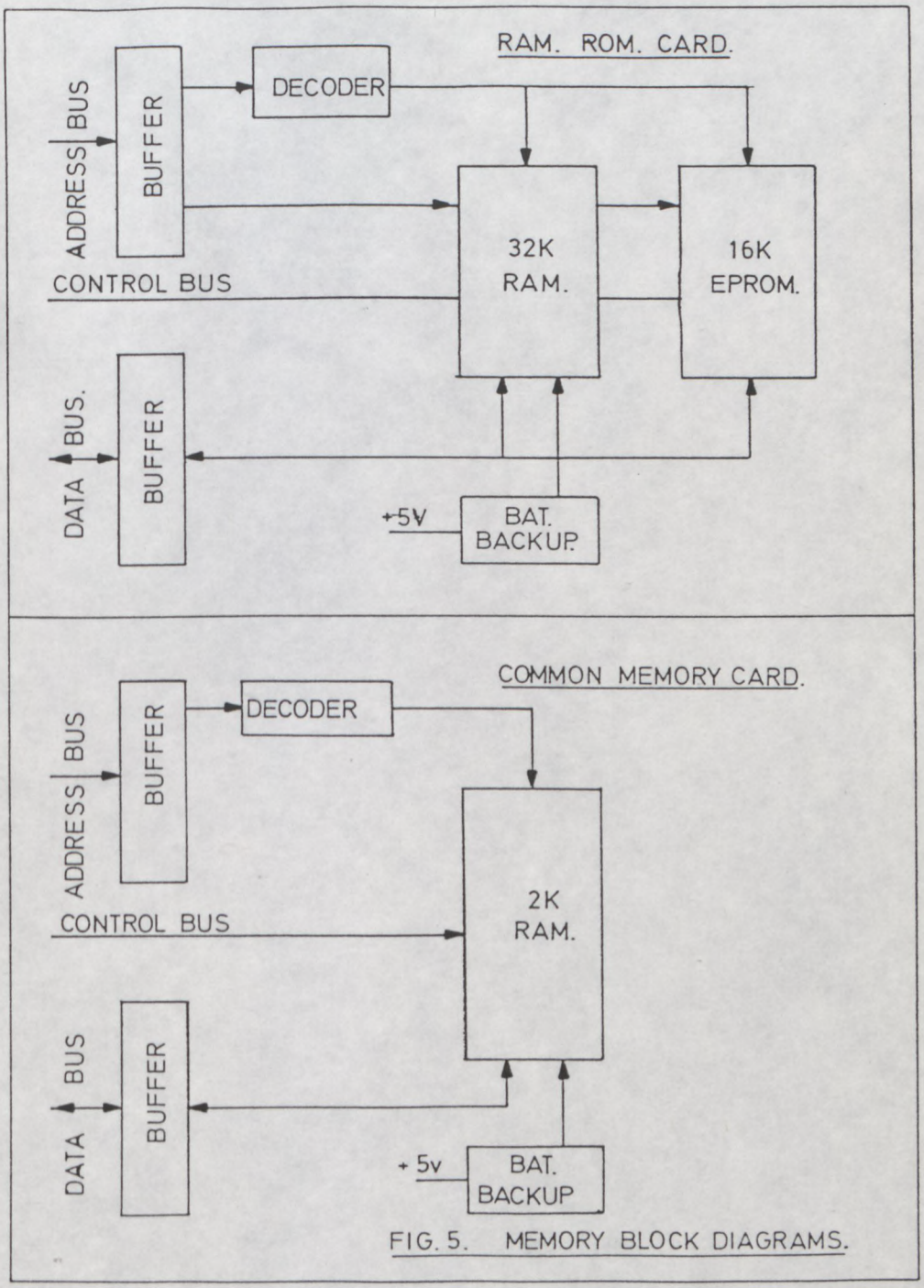


FIG. 5. MEMORY BLOCK DIAGRAMS.

2.4 MEMORY TEST PROGRAM.

The unique features of this program are:

1. Test the specified memory locations.

2. Indicate the faulty memory positions on the screen.

3. Handles memory selection on all eight memory pages.

4. Very user-friendly.

The program operates in the following sequence:

1. The program loads a byte into the first memory location.

2. Reads the location and varifies its contents.

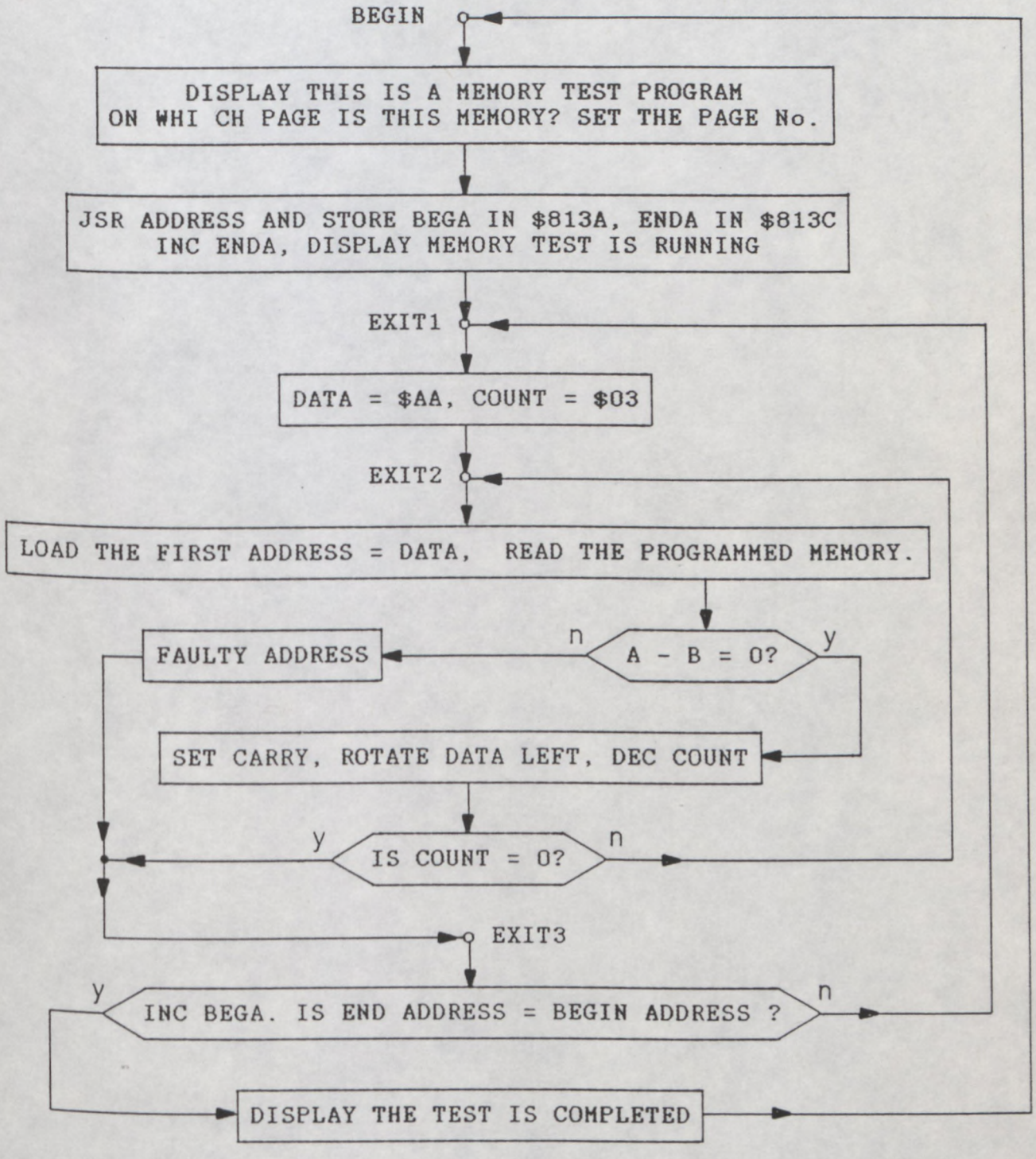
3. Sets the carry and rotates the contents.

4. Reads the location and varifies its contents.

5. This procedure repeates itself three times before proceeding to the next memory location.

The next page illustrates the detailed flow chart of the test program.

2.4.1 FLOW CHART OF THE MEMORY TEST PROGRAM.



2.5 GENERAL INFORMATION.

All the technical design and operation of this section are contained in the seperate appendix called

32k RAM MEMORY AND 16k EPROM MEMORY MODULE.

2k COMMON PAGE RAM MEMORY MODULE.

This appendix supplies:

1. Background to the designs.

2. Complete design and circuit diagrams.

3. Wire wrap boards.

4. Test programs with flow charts and program listings.

5. All data sheets on the components used in the design.

NB. It is recommended to refer always to this document.

The index of the memory modules is listed on the following page.

2.5.1 MEMORY APPENDIX INDEX.

32K RAM MEMORY AND 16K EPROM MEMORY MODULE.

2K COMMON PAGE RAM MEMORY MODULE.

3. EPROM PROGRAMMER.

The main application of the microcomputer project will be in long time-control systems. It is also important to perform repeated operations of a particular application. This is the reason for incorporating an EPROM programmer into the total system. Provision has been made for the programmer to offload programs into EPROMS which can be accessed from sockets provided for this purpose.

This EPROM programmer can only operate on the 2716 and the 2732 EPROM's.

The following table states the main features introduced into this programmer. It can perform all stated functions for the 2716 and 2732 EPROM'S.

3.1 PROGRAM FEATURES.

1. It can read an EPROM in any one of the EPROM INPUT sockets and produce an EPROM copy of that program. Even copies for different computer systems can be produced.

2. A written program, any where in memory, can be loaded into a buffer area and then stored into an EPROM.

3. A program-listing of the contents of an EPROM or a program in the buffer area can be obtained on the system printer. It is not a disassembler but only states the memory position and the mnemonic hexadecimal code.

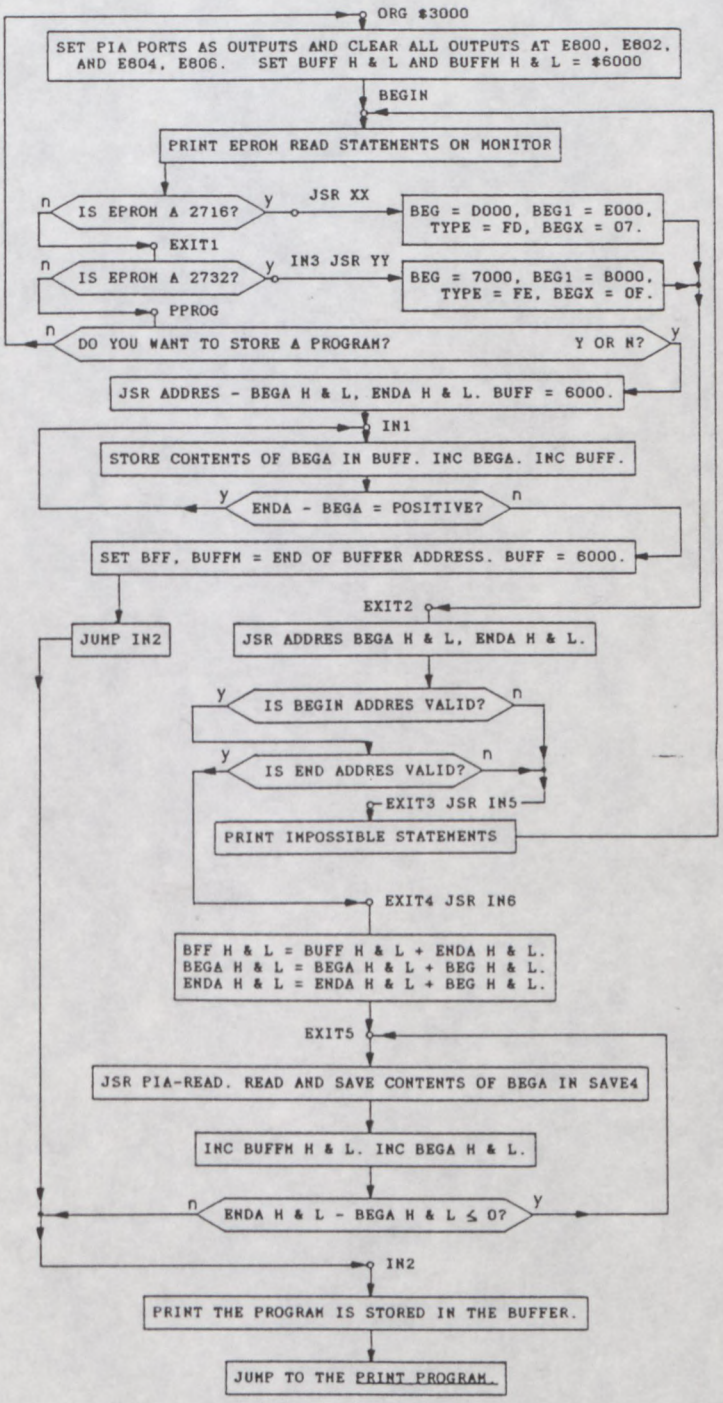
4. Parts of a program can also be listed on the printer.

5. During programming of an EPROM any faulty EPROMS will be clearly indicated on the monitor screen. The program will verify the contents of the EPROM while been programmed.

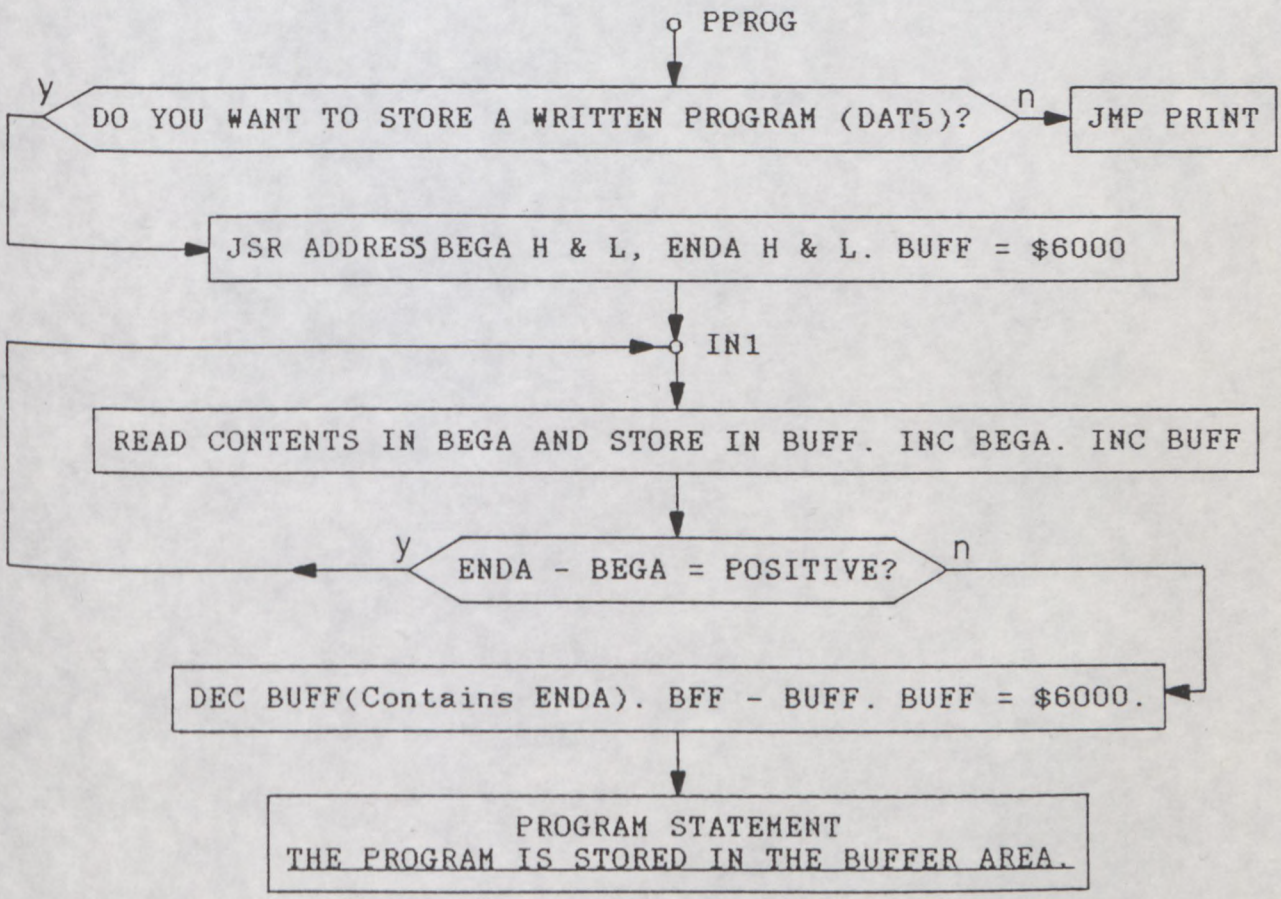
6. Impossible address specifications for a particular EPROM will be checked by the program and also indicated on the monitor screen.

7. The program is very intelligent and user-friendly.

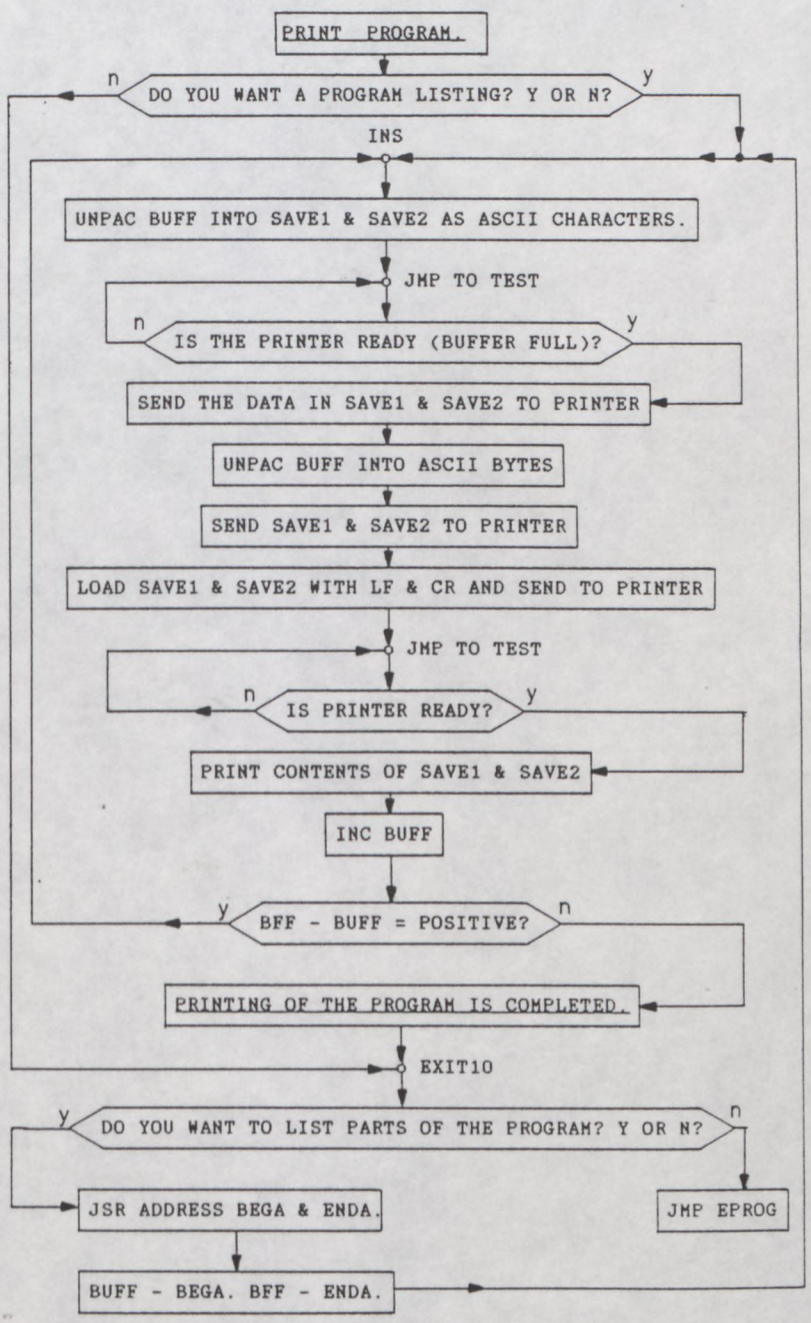
3.1.1 FLOW CHART FOR THE EPROM READ OPERATION.



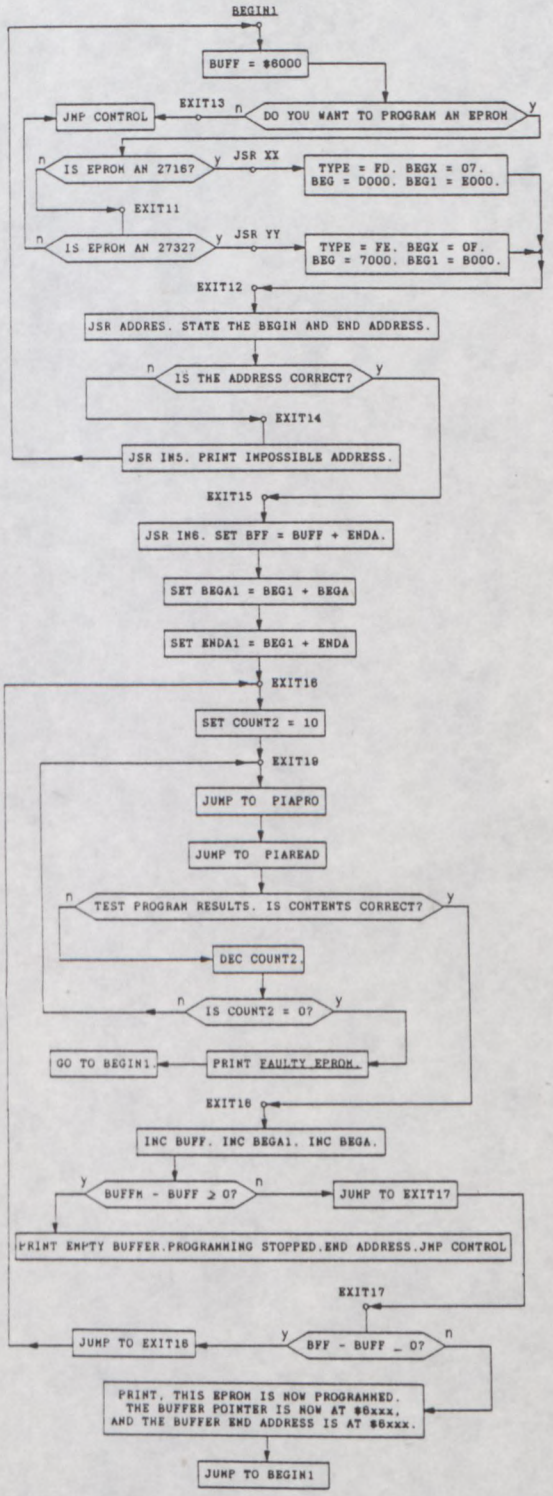
3.1.2 FLOW CHART TO STORE A PROGRAM INTO THE BUFFER AREA.



3.1.3 FLOW CHART OF PROGRAM PRINT ROUTINE.



3.1.4 FLOW CHART TO PROGRAM AN EPROM.



3.2 GENERAL INFORMATION.

All the technical design and operation of this section are contained in the seperate appendix called

THE REAL TIME CLOCK.

THE EPROM PROGRAMMER.

This appendix supplies:

1. Background to the designs.

2. Complete design and circuit diagrams.

3. Wire wrap boards.

4. Test programs with flow charts and program listings.

5. All data sheets on the components used in the design.

NB. It is recommended to refer always to this document.

The index of the module is listed on the following page.

3.3 EPROM APPENDIX INDEX.

SYSTEM REAL TIME CLOCK AND EPROM PROGRAMMER.

SYSTEM REAL TIME CLOCK.

THE EPROM PROGRAMMER.

4. REAL TIME CLOCK.

Real time clocks are important devices in computers and microcomputer systems. It is important in all control applications to control a system and to keep track of the time involved. An oven must be kept at a constant temperature for a number of hours, or a motor must run for a number of minutes. These applications all need a real time clock to keep track of the time.

A number of these integrated circuits are today available. Some of the very popular IC's are the MSM5832 from OKI Semiconductor Inc. and the MC146818 from Motorola. All are low power, high speed and high density CMOS IC's. These characteristics are important for the system to keep track of the time during power down periods. Battery backup must then be supplied.

The Motorola MC146818 was used for this application. The IC contains 12 registers, 50 bytes of low power static RAM, a complete time of day clock with alarm and one hundred year calender, a programmable periodic interrupt and square wave generater. The square wave generater is very accurate and is used for program interrupt systems.

The main features of this device are:

1. Internal time base and oscillator.

2. Counts seconds, minutes, and hours.

3. Counts date, month, and year.

4. 12 or 24 Hour clock.

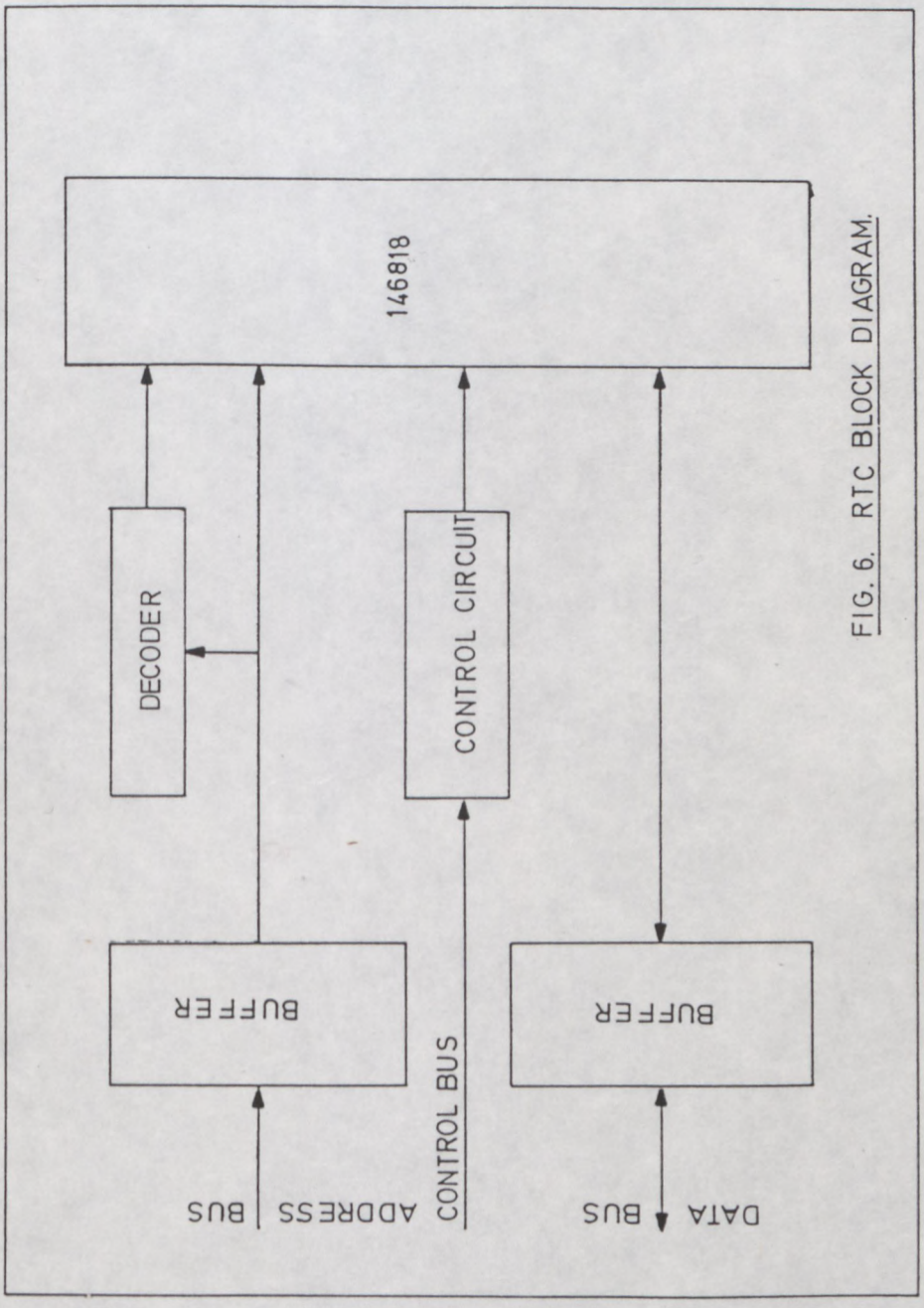
5. Microprocessor bus compatible.

6. Bus compatible interrupt signal.

4.1 THE REAL TIME CLOCK BLOCK DIAGRAM.

The following block diagram in FIG. 6 illustrates the basic design of this module.

FIG 6. THE REAL TIME CLOCK BLOCK DIAGRAM.



4.2 PROGRAM OPERATION OF THE REAL TIME CLOCK.

The MC146818 consists of 50 general purpose RAM bytes, 10 RAM bytes which normally contain the time, calender, alarm data, four control and status bytes. All 64 bytes are directly readable and writable by the processor program except register C and register D,which are read only. Bit 7 of register A , and the high order bit of the seconds byte are read only.

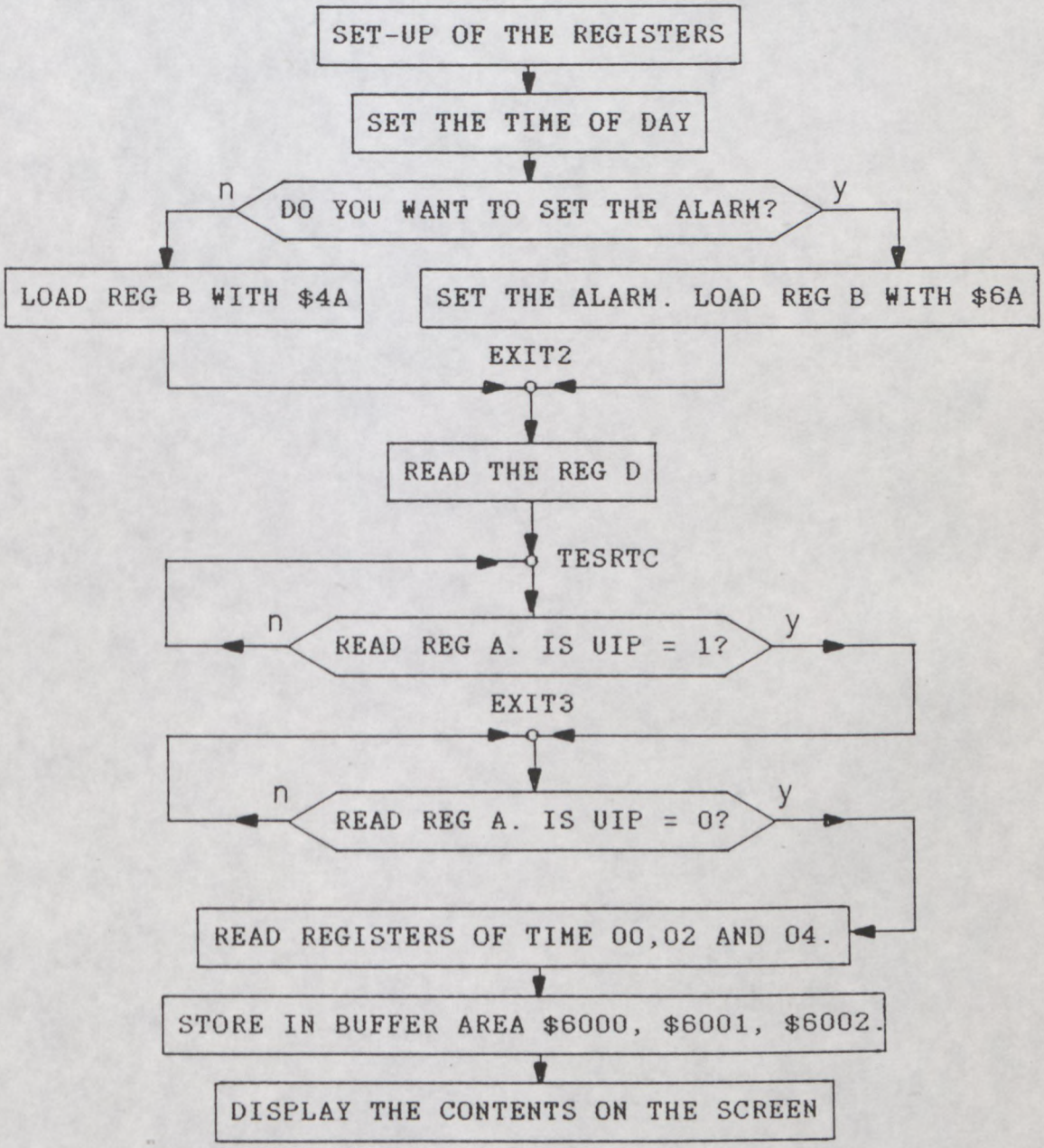
The processor obtains time and calender information by reading the appropriate locations. The first step in the program is to JSR SETREG, which loads REG $0B with $CA. This loads the SET bit to one and allows the processor to update the RTC registers. Register 0A is also loaded with $0F.

The IC is now ready for initialization of the internal registers. JSR TIMDAY loads the buffer at address $6000 with the time of the day and JSR STOTIM offloads the time in the buffer into the registers of the real time clock.

The subroutine JSR DMY sets the day, month and year in the following format DD-MM-YY-D. This is DAY-MONTH-YEAR-WEEK DAY. SUNDAY = 1 and 7 = SATURDAY for WEEK DAY. This information is then stored in the buffer area and JSR STODAY offloads this data into the registers of the real time clock.

The following routine is to set the alarm section of the real time clock. Bit 5 of register $0B must be set to 1, to activate the alarm circuit. Register $0C must be read to monitor the flags.

4.3 PROGRAM FLOW CHART OF THE REAL TIME CLOCK.



4.4 GENERAL INFORMATION.

The technical design and operation of this section are contained in the seperate appendix called

THE REAL TIME CLOCK.

THE EPROM PROGRAMMER.

This appendix supplies:

1. Background to the designs.

2. Complete design and circuit diagrams.

3. Wire wrap boards.

4. Test programs with flow charts and program listings.

5. All data sheets on the components used in the design.

NB. It is recommended to refer always to this document.

The index of the module is listed on the following page.

4.5 REAL TIME CLOCK APPENDIX INDEX.

SYSTEM REAL TIME CLOCK AND EPROM PROGRAMMER.

SYSTEM REAL TIME CLOCK.

5. POWER FAIL DETECTOR.

This circuit senses the +5v power supply. If the voltage drops to a value of +4,7v, the NMI line of the processor will be activated to interrupt the system.

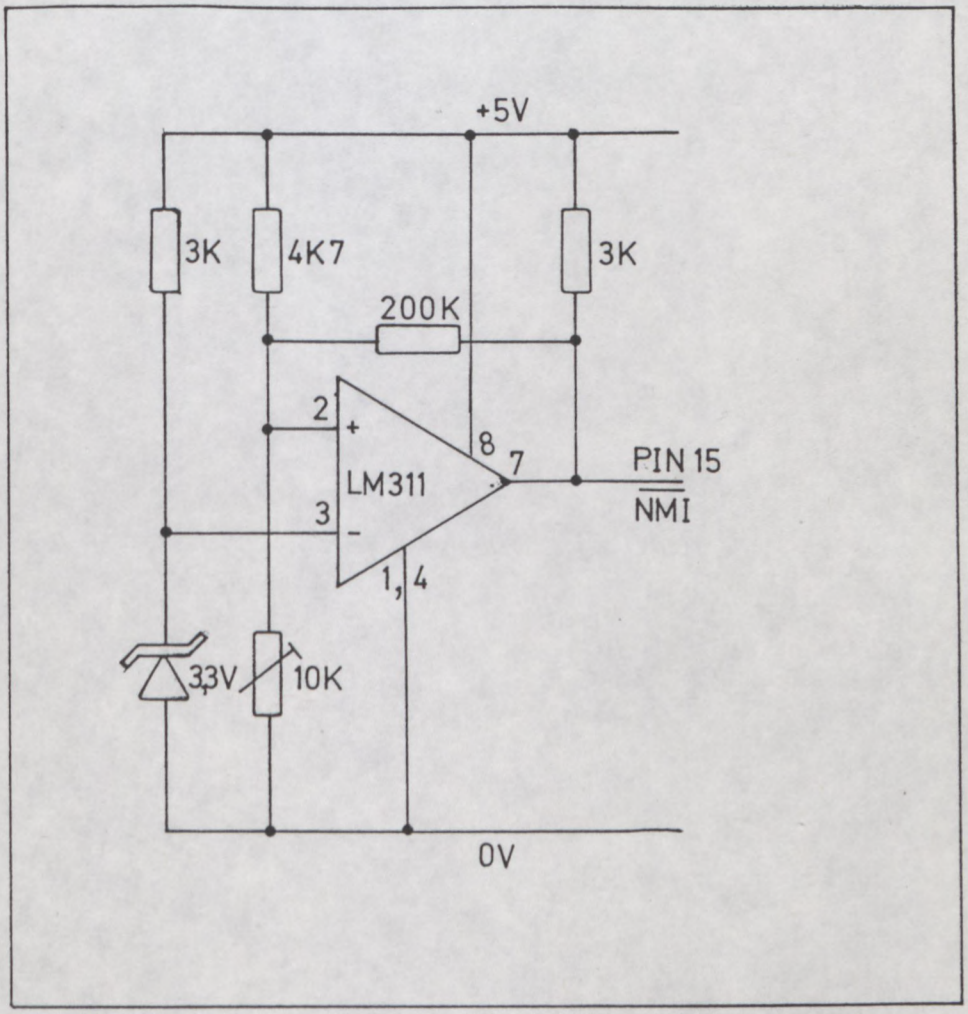
FIG. 7 illustrates the circuit diagram and the discharge curve of the +5v power supply.

The discharge rate of the supply is equal to 10ms/0,5v.

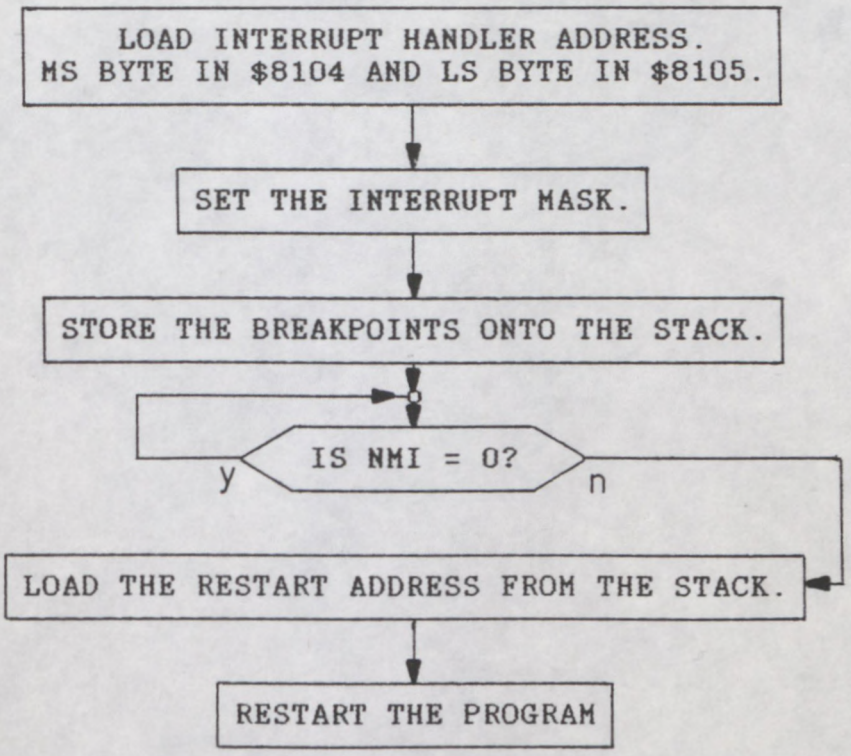
This brings the number of program steps allowed during a 10ms interval equal to 10ms/2us = 5000 program steps.

A power-fail interrupt handler should thus not be longer than 5000 program steps.

FIG. 7 POWER FAIL DETECTOR CIRCUIT DIAGRAM.



5.1 TEST PROGRAM FLOW CHART FOR THE POWER FAIL DETECTOR.



5.2 PROGRAM LISTING FOR THE POWER FAIL DETECTOR.

```
---
PAGE  001  TEST
0001                                NAM   TEST
0002                                OPT   M
0003                                OPT   O
0004                                OPT   L
0005                                OPT   NOP
0006                                OPT   NOS
0007                                OPT   NOG
0008        F156      OUTCHR        EQU   $F156
0009 3000                           ORG   $3000
0010 3000 8E A100 MAIN              LDS   £$A100
0011 3003 86 40                     LDAA  £$40
0012 3005 B7 8104                   STAA  $8104
0013 3008 86 00                     LDAA  £$00
0014 300A B7 8105                   STAA  $8105
0015 300D 20 F1                     BRA   MAIN
0016 4000                           ORG   $4000
0017 4000 01        INTR            NOP
0018 4001 01                        NOP
0019 4002 01                        NOP
0020 4003 86 30                     LDAA  £$30
0021 4005 BD F156                   JSR   OUTCHR
0022 4008 01                        NOP
0023 4009 01                        NOP
0024 400A 3B                        RTI
0025                                END

TOTAL ERRORS 00000
```

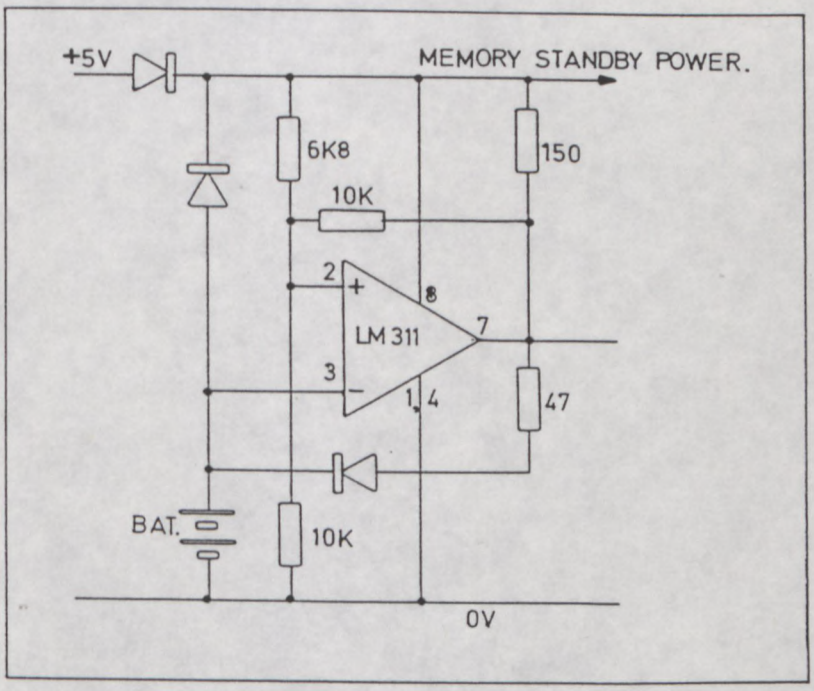
6. NI-CAD BATTERY CHARGER.

Two NI-CAD penlight cells are used for the memory power back-up system.

The circuit has been desiged with a 0,53v hysteresis.

The batteries will be charged to a 2,5v value and only recharged when the battery voltage reaches 1,87v. This allows for a long battery lifetime.

FIG. 8. NI-CAD CHARGER CIRCUIT DIAGRAM.



7. BUFFER INTERFACE.

The interconnection between the main console and the extension rack is long, because each console is mounted on slides for easy access to the console interiors. This necessitates the buffer driver board. This board occupies the first position in the extension rack. It facilitates reliable communications between the extension rack and the main console. The buffer has a fanout of 20 and can handle 20 boards having TTL LS specifications. The extension rack can house another 7 boards, assuring reliable operation.

Components on boards are placed as closely as possible to the bus connector to reduce lead lenghts.

All boards are decoupled from the power distribution network using capacitive decoupling networks. TTL logic gates generate switching transients and 0,01uF to 0,1uF are used to suppress these transients. The capacitors are soldered as close as possible to the IC's power supply input pins.

The bus driver/receiver's exhibit some hysteresis and help eliminate any noise picked up on the buses.

7.1 GENERAL INFORMATION.

The technical design and operation of this section are contained in the seperate appendix called

EXTENSION RACK BUFFER INTERFACE CARD.

This appendix supplies:

1. Background to the designs.

2. Complete design and circuit diagrams.

3. Wire wrap boards.

4. Test programs with flow charts and program listings.

5. All data sheets on the components used in the design.

NB. It is recommended to refer always to this document.

The index of the module is listed on the following page.

7.2 EXTENSION RACK BUFFER INTERFACE CARD APPENDIX INDEX.

EXTENSION RACK BUFFER INTERFACE CARD.

8. INTERFACING THE INPUT/OUTPUT LINES.

The following specifications were obtained for the INPUT/OUTPUT line buffer card.

1. Eight INPUT channels
2. Eight OUTPUT channels
3. Input and output must be TTL compatible.
4. Interrupt control is not required.

From these specifications it was decided to use a MC6821P peripheral interface adapter (PIA). The A port is used for the 8 output channels and port B is used for the 8 input channels. The PIA is ideal for this kind of application. From specification it was not necessary to design anything more than a very simple I/O system. However, this same design could easily be upgraded to a polled I/O or even a double handshaking I/O system. Only a few conductors must be added to the wire wrap card.

8.1 SUMMARY OF THE PIA REGISTERS.

Registers used for the output lines;

$1000 OUTPUT REGISTER A, and the address of DDR B.

$1001 CONTROL REGISTER A.

Rgisters used for the input lines;

$1002 OUTPUT REGISTER B, and the address of DDR B.

$1003 CONTROL REGISTER B.

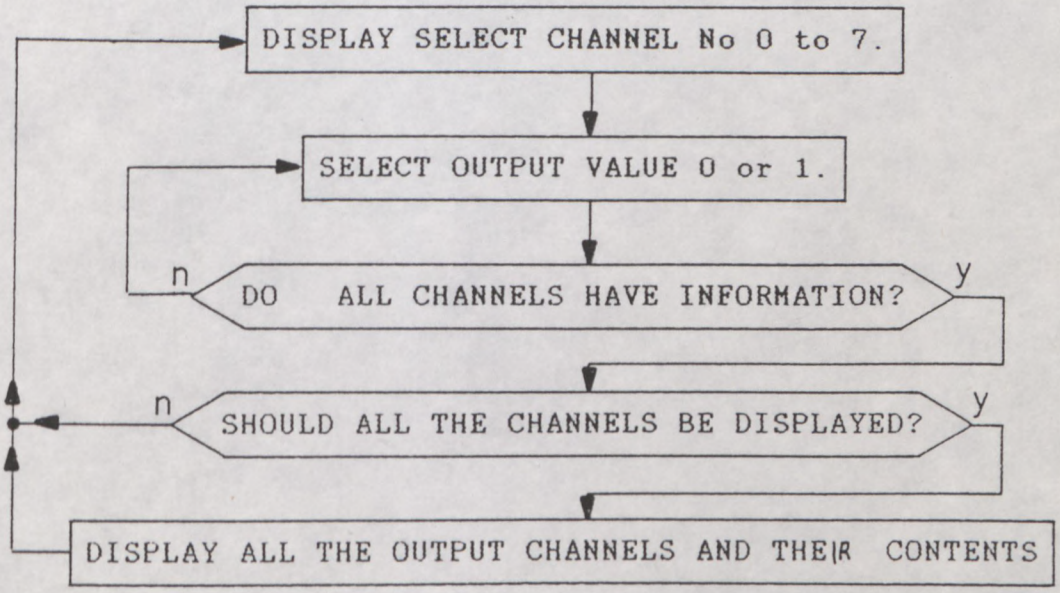
8.2 TEST PROGRAM FOR EIGHT OUTPUT LINES.

A test program was developed for these output lines and can be used to test the channels for faultfinding or even as a subroutine in larger control programs
The program was developed to be user-friendly and performs the following tasks.

1. It will display channel select options.
2. It will respond by asking the value of 0 or 1 that must be transmitted to the output port.
3. It will also read the output port and display the contents on the screen if required.

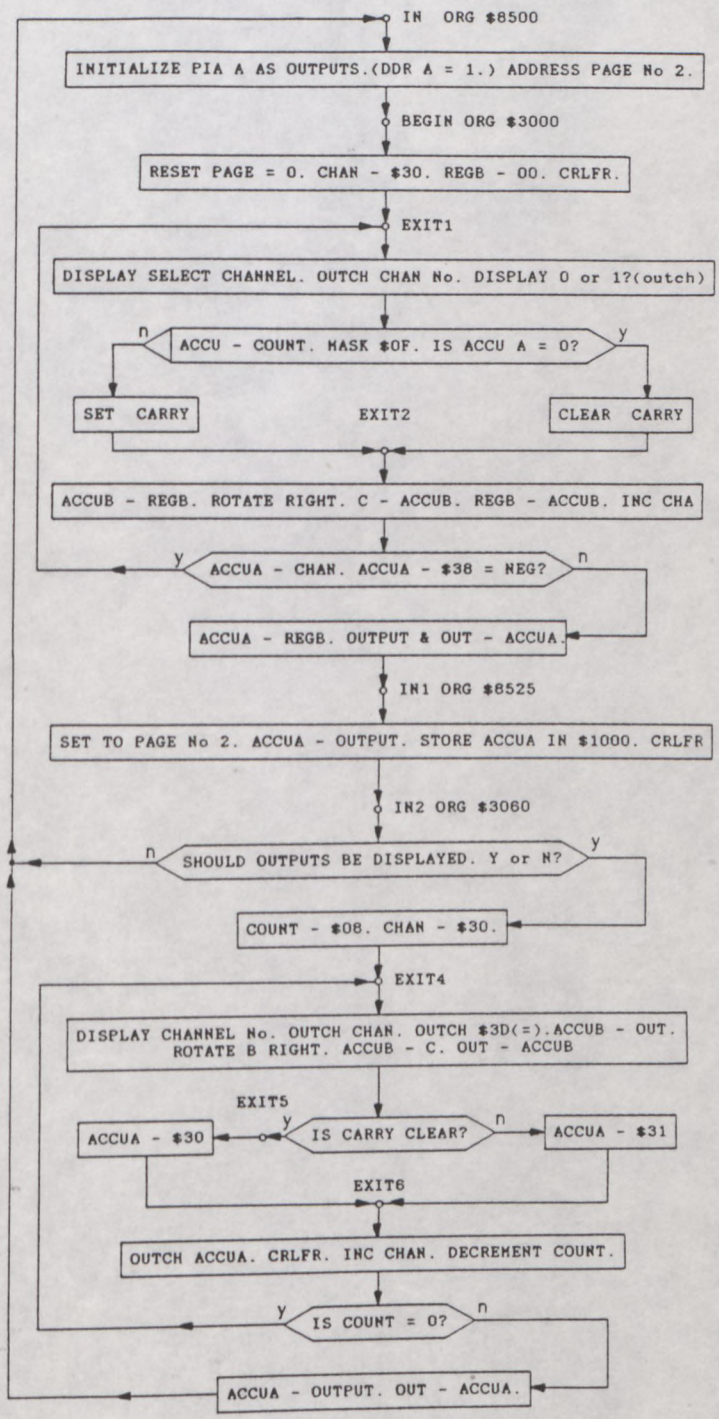
The following short flowchart indicates this operation.

8.3 TEST PROGRAM OPERATION PRINCIPLE.



5.4 COMPLETE FLOW CHART OF THE TEST PROGRAM.

EIGHT OUTPUT LINES. CARD No2 ADDRESSES $1000, $1001



8.5 TEST PROGRAM FOR THE EIGHT INPUT PORT.

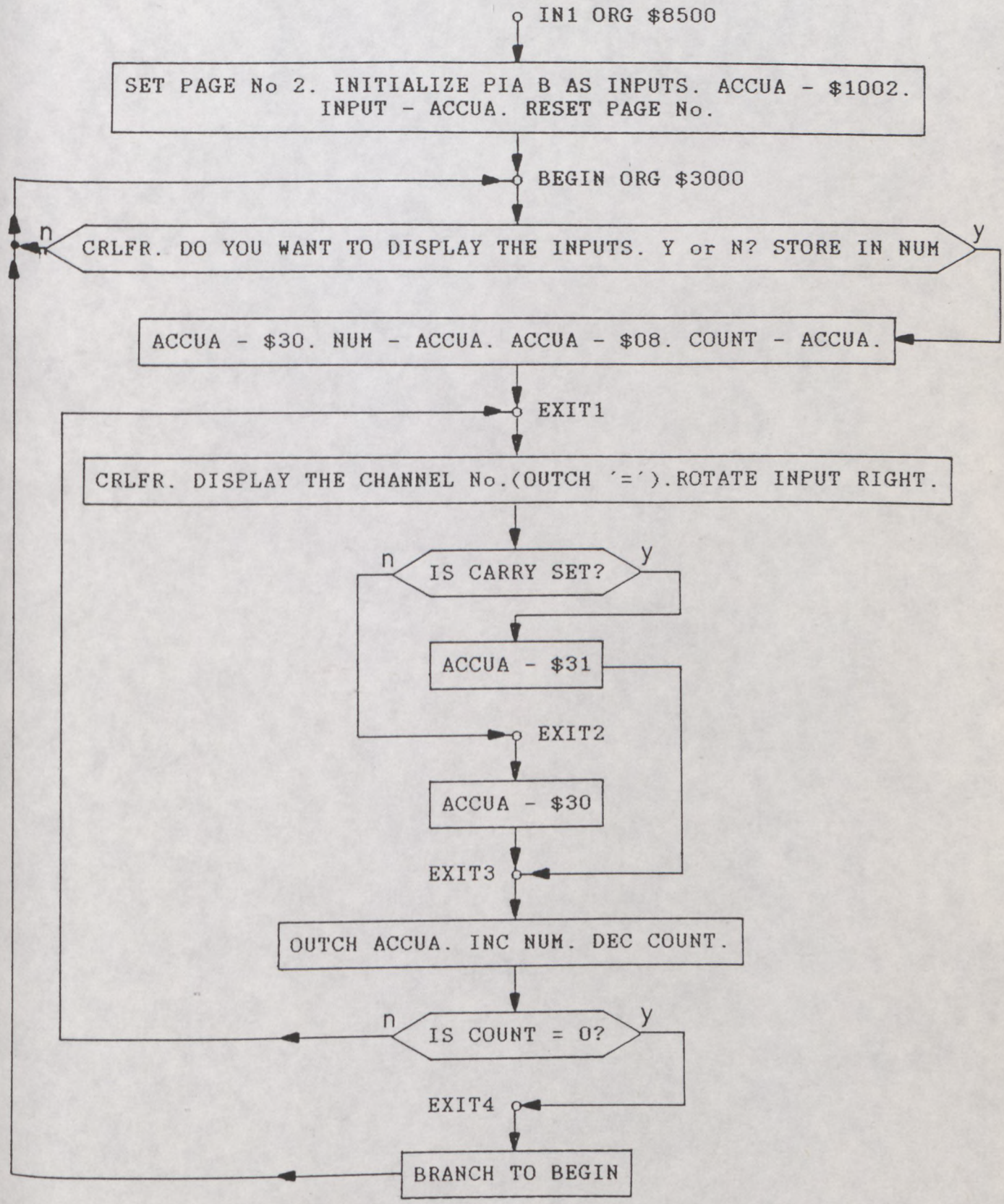
A test program was developed for this eight-input port. The program is user-friendly, programmed in ASSEMBLER language and will perform the following tasks.

1. It will ask whether the inputs must be displayed. Yes or NO?
2. If yes, it will display the channel number and the contents.

   0v = 0 and +5v = 1.

The flow chart for this program is shown on the following pages.

8.6 FLOW CHART OF THE EIGHT-CHANNEL INPUT PORT.



8.7 GENERAL INFORMATION.

The technical design and operation of this section are contained in the separate appendix called

INTERFACING INPUT/OUTPUT LINES TO THE MICROCOMPUTER.

EIGHT CHANNEL INPUT/OUTPUT PORT.

This appendix supplies:

1. Background to the designs.

2. Complete design and circuit diagrams.

3. Wire wrap boards.

4. Test programs with flow charts and program listings.

5. All data sheets on the components used in the design.

NB. It is recommended to refer always to this document.

The index of the module is listed on the following page.

8.8 INTERFACING INPUT/OUTPUT LINES TO THE MICROCOMPUTER.

APPENDIX INDEX.

9. PRIORITY INTERRUPT CONTROLLER.

The system is an EIGHT LEVEL PRIORITY VECTORED INTERRUPT SYSTEM.

FIG 9 illustrates the operating principle of this EIGHT LEVEL PRIORITY VECTORED INTERRUPT CONTROLLER.

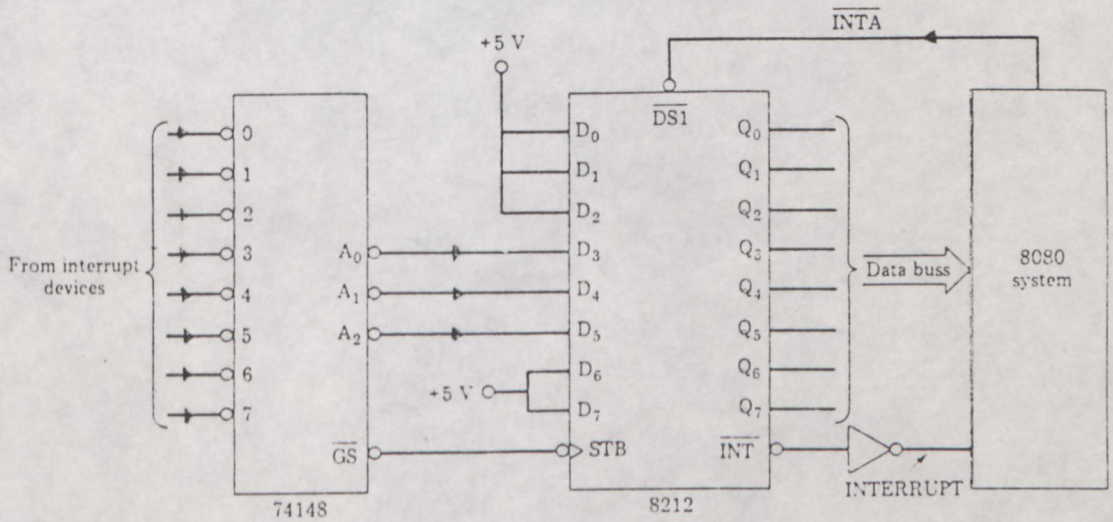


FIG 9. Eight level priority vectored interrupt.

For example, if line 5 goes LOW, the computer will read the value 11 010 111, or D7 in hexadecimal.
All the possible sevice routine addresses are:

	CHANNEL No.	ADDRESS
LOWEST PRIORITY	0	FF00
	1	F700
	2	EF00
	3	E700
	4	DF00
	5	D700
	6	CF00
HIGHEST PRIORITY	7	C700

This illustrates the power of this simple circuit. Each service routine must fit into the memory space. From FF00 to F700 are 2048 program steps. This amount of memory space should be enough for most application programs neaded for the system.

9.1 TEST PROGRAM FOR THE PIC.

A test program was developed for this PIC and can be used to test the channels for faultfinding or even as a subroutine in larger control programs.

The program was developed to be user-friendly and will do the following tasks.

1. It will check the input lines for any interrupts.
2. It will respond by displaying the interrupted channel input and will also ask if all channels should be displayed.
3. It will display the contents on the screen if required.

The following short flowchart indicates this operation.

PIC TEST PROGRAM OPERATING PRINCIPLE.

The PIA A must be set as as INPUT PORT.

PIA B as an INPUT PORT.

IRQA must go LOW when CA1 gets interrupted.

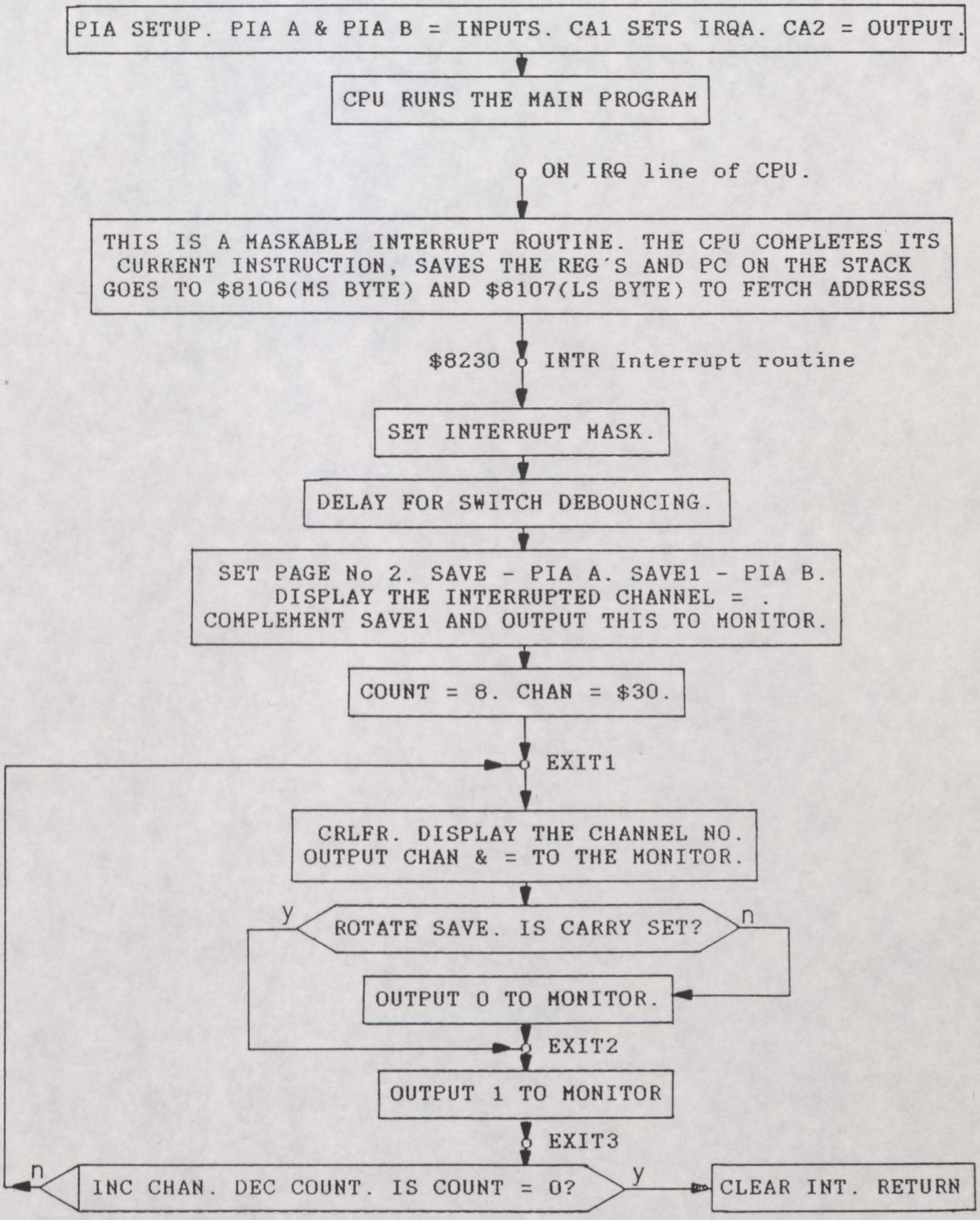
CA2 must generate a LOW on the CPU READ cycle, but must return to HIGH after the READ cycle.

This can be achieved by;

1. Load 00 into the Control reg A & B to select DDR's.
2. Write 00 into the DDR's to select PIA A & B as inputs.
3. Load $2D into Control reg A and $04 into B.

When interrupted the CPU completes its current instruction, saves the registers and PC on the stack. The PC will be loaded with the contents of $8106(MS BYTE) and $8107(LS BYTE), the address of the service routine. This routine displays the interrupted channel No and requests if the contents of the inputs should be displayed. After completion of this task, the CPU returns to the main program.

8.2 FLOW CHART FOR THE PIC TEST PROGRAM.



8.3 GENERAL INFORMATION.

All the technical design and operation of this section are contained in the seperate appendix called

INTERFACING INPUT/OUTPUT LINES TO THE MICROCOMPUTER.

EIGHT CHANNEL INPUT/OUTPUT PORT.

EIGHT INPUT CHANNEL PRIORITY INTERRUPT CONTROLLER.

This appendix supplies:

1. Background to the designs.

2. Complete design and circuit diagrams.

3. Wire wrap boards.

4. Test programs with flow charts and program listings.

5. All data sheets on the components used in the design.

NB. It is recommended to refer always to this document.

The index of the module is listed on the following page.

8.4 EIGHT INPUT CHANNEL PIC APPENDIX INDEX.

SECTION ON THE PRIORITY INTERRUPT CONTROLLER.

10. A/D CONVERTER.

The following specifications were laid down for this A/D converter.

1. Accuracy ± 0,5%
2. Input voltage ± 15v ± 0,5%

From these specifications the following characteristics were defined:

1. Eight bits will give an overall accuracy of 0,8%.
2. It must be interfaced to a M6800.
3. TTL compatible.
4. Three state data output port.
5. Fast conversion cycle.
6. Bipolar (Offset binary) operation mode.
7. Clock must be faster than 0,8MHZ.

IC SELECTED. The A/D from Analog Devices AD7581 complied to all these specifications. It has the following features.

Eight bit resolution.

On chip 8*8 dual port memory.

No missed code over full temperature range.

Interface directly to M6800.

CMOS and TTL compatible.

Three state data drivers.

Fast conversion. Max clock frequency 1,6MHZ.

See the index to find the data sheet on the AD7581.

10.1 CIRCUIT OPERATION

The AD7581 is a complete converter on its own and simplified the design of the interface. The IC is however designed to operate on a 0v to ±10v input voltage. The specification for this interface is however ±15v. For this reason OPAMP divider circuits are provided on all eight input channels. The 15v input voltage is divided to 5v by the input and feedback resistors.

INPUT CIRCUIT. The OP AMPS in the input circuit are LM324 quad operational amplifiers. These OP AMPS feature high stability, temperature compensation, compatiblity with TTL, low input bias current, low input offset voltage and offset current. These features accomplish an overall accuracy for the converter of better than 1%. See index for data sheet on the LM324. Gain calibration is set by the Rv (100K) multiturn trimpots.

The inputs are connected to edge connecter J1 and are numbered from CH0 TO CH7. Each channel has a unique address ranging from $3000 to $3007.

PAGE SELECTOR AND ADDRESS DECODER. This circuit selects the PAGE No 2 and decodes all the addresses $3xxx. This generates the chip select.

10.2 PROGRAM OPERATING PRINCIPLE.

The converter operates in the OFFSET BINARY mode.

Thus;

1 1 1 1 1 1 1 1 --- +5v (-15v)

1 0 0 0 0 0 0 0 --- 0v (0v)

0 0 0 0 0 0 0 0 --- -5v (+15v)

The general structure of the program is to convert the digital data to:

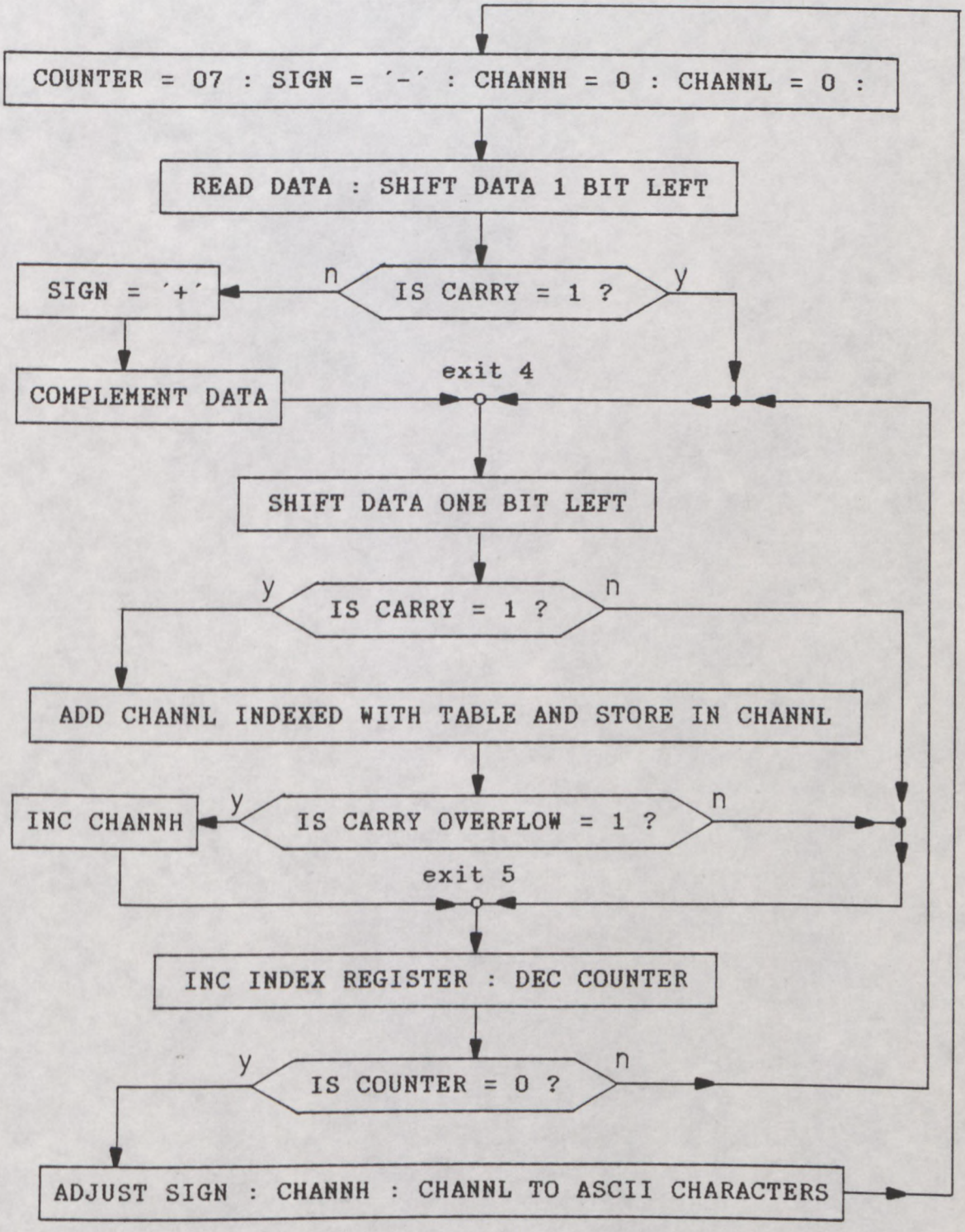
SIGN CHANNH CHANNL (Every location a 8 - bit word.)

SIGN -- indicates whether the value is positive or negative.
CHANNH -- stores 01 when value is 14.9v
CHANNL -- stores 49 when value is 14.9v

The seven bit code represents a decimal value of 14,9 .
Therefore a table was generated to adjust the binary value before being displayed on the monitor.

Table holds: 75, 38, 19, 09, 05, 02, 01, 00
The sum equals 149 giving an accuracy of 1/149 = 0,6%

The following short flowchart explains the operating principle.



10.3 A/D CONVERTER TEST PROGRAM.

A test program was developed for this A/D converter. The program is desiged to be user-friendly and to perform the following tasks.

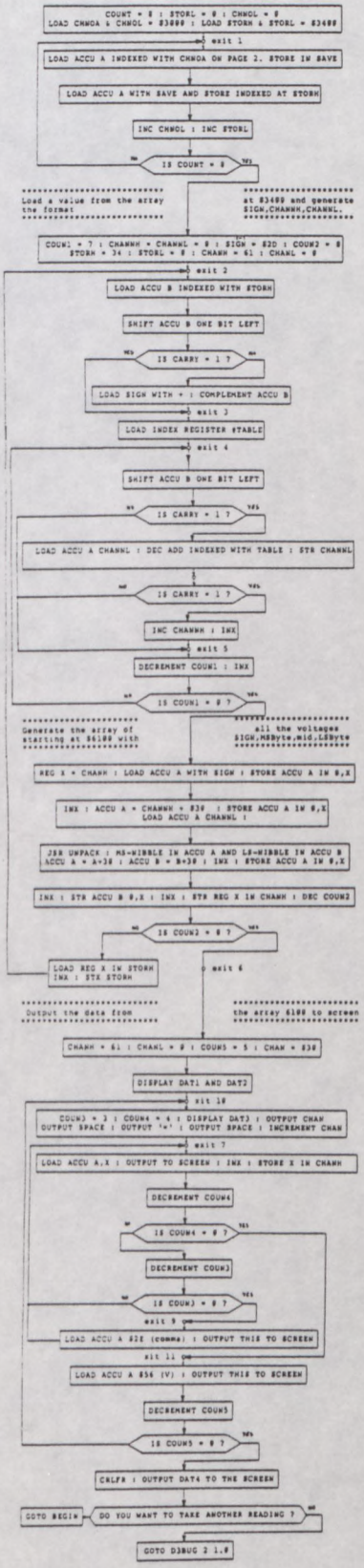
1. Display the function and its location in the system extension rack.
2. It reads the data on the seven analog input channels and stores the data in a memory array.
3. The data array will be converted into ASCII format and also adjusted to carry the ASCII equivalent number of the voltage read by the specific channel no.
4. Then the table will be send to the monitor in the following format.

   Example.

CHANNEL NO 0 = +12,7V
CHANNEL NO 1 = -05,3V
CHANNEL NO 2 = +03.3V

The following page illustrates the flow chart for this test program.

10.4 TEST PROGRAM FLOW CHART.



10.5 GENERAL INFORMATION.

The technical design and operation of this section are contained in the seperate appendix called

INTERFACING ANALOG AND DIGITAL SYSTEMS.

THE ANALOG TO DIGITAL CONVERTER.

This appendix supplies:

1. Background to the designs.

2. Complete design and circuit diagrams.

3. Wire wrap boards.

4. Test programs with flow charts and program listings.

5. All data sheets on the components used in the design.

NB. It is recommended to refer always to this document.

The index of the module is listed on the following page.

10.6 THE ANALOG TO DIGITAL CONVERTER APPENDIX INDEX.

11. D/A CONVERTER.

A D/A converter with the following specifications had to be designed.

1. A general multi-purpose system for experiments in the laboratories of the Department for Mechanical Engineering at the University of Stellenbosch.
2. Accuracy ± 10%.
3. Output voltage ± 10V ± 1mA.
4. Ten channels.

The Department for Mechanical Engineering stripped a computer system and a number of MODEL 411 D/A converters were made available. It was decided to use these modules in the proposed system in order to stay within the limited budget available.

MODEL 411 D/A CONVERTER. This model uses high quality wire wound resistors in all critical places to guarantee that the module is monotonic over it's full operating temperature range. The converter uses a BINARY WEIGHTED resistor network with a high stability temperature compensated OP AMP. The voltage output settling time is 20/us. The current settling time is 300ns. This makes the current output mode desirable for high speed operations.
An internal reference is included, but provisions are made for an external reference source.

Features of the MODEL 411 D/A CONVERTER.

TEN BIT CONVERTER. Accuracy 1/1024. Better 0,1%

Bipolar operation ± 10V output.

Maximum offset voltage ± 5mV.

Low overall temperature accuracy of 20 ppm/ C.

Output current is low, -1mA to +1mA.

Disadvantage: The module should not be overloaded and the modules should be well buffered by amplifiers.

11.1 CIRCUIT OPERATION.

The circuit consists of ten D/A converters and is housed on two separate cards. These cards are CARD No 2 and CARD No 3 in the EXTENSION RACK. The outputs are connected via a 3M 50 way flat cable and ends as BNC plugs on the rear panel of the EXTENSION RACK. The channels are numbered from channel No 0 to channel No 9

The channels are addressed in the following format in the EXTENSION RACK:

CHANNEL No.	CARD No.	PAGE No.	ADDRESS No.
0	2	2	$1004, $1005
1	2	2	$1006, $1007
2	2	2	$1008, $1009
3	2	2	$100A, $100B
4	2	2	$100C, $100D
5	3	2	$2004, $2005
6	3	2	$2006, $2007
7	3	2	$2008, $2009
8	3	2	$200A, %200B
9	3	2	$200C, $200D

11.2 PROGRAM OPERATING PRINCIPLE.

The DAC 411 is connected in a BIPOLAR OFFSET MODE. The output will generate:

+Vmax equals +10V and is 0 0 0000 0000
+0V is 0 0 1111 1111
-0V is 1 1 0000 0000
-Vmax equals -10V and is 1 1 1111 1111

Any value will thus be displayed in a nine bit format. The sign will be added after the integer value has been generated.
(1 1111 1111) = (513)

Thus 10,00V = 513 and is 0,513 BIT/V.

The input format is +10,00V.
This value will be stored at locations
SIGN MSB LSB3 LSB2 LSB1.

The ASCII part of the values will be masked out before being stored into the above storage positions. Once in this format the generating of the binary value will start.
A table for binary values has been developed and is shown in the next table

DIGIT VALUE	MSB	LSB3	LSB2	LSB1
0	0000	0000	0000	0000
1	01FF	0033	0005	0001
2		0067	000A	0001
3		009A	000F	0002
4		00CD	0015	0002
5		0101	001A	0003
6		0134	001F	0003
7		0167	0026	0004
8		019A	0029	0004
9		01CE	002E	0005

Example: When a value like +3,56V has been accepted the program will add the following values:

SIGN	MSB	LSB3	LSB2	LSB1
+	0	3 ,	5	6

SIGN 0000

MSB 0000

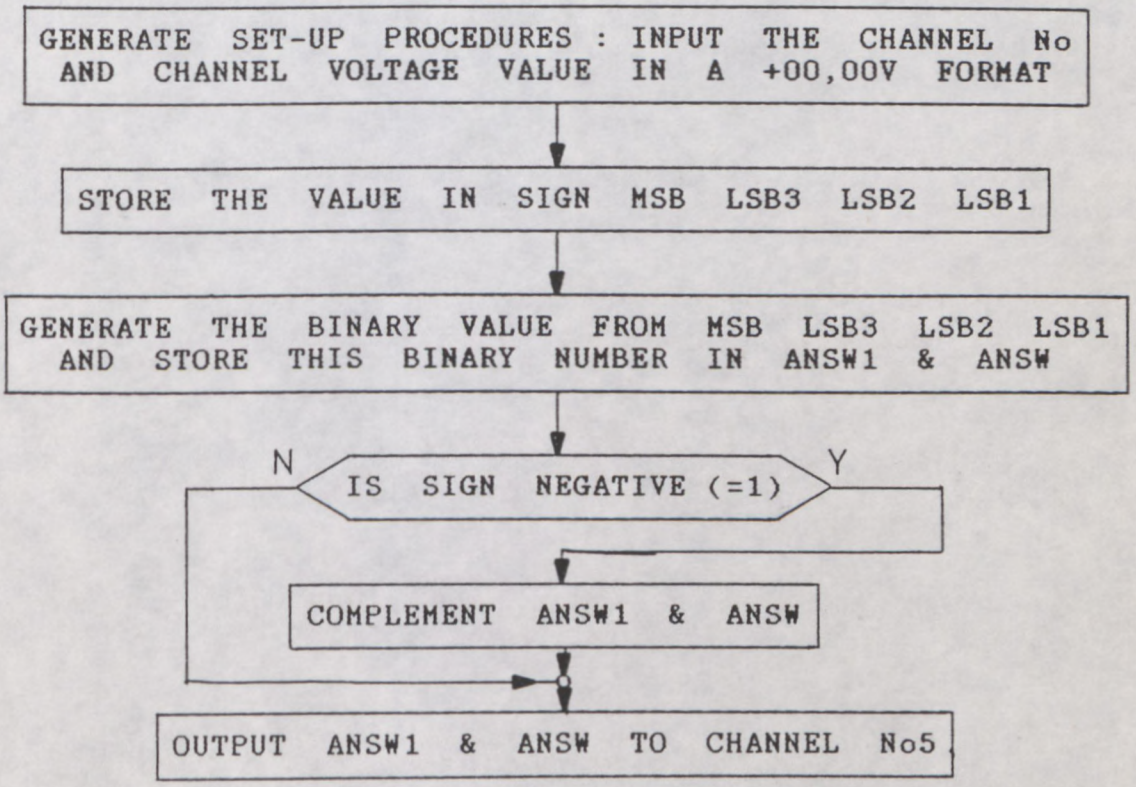
LSB3 009A

LSB2 001A

LSB1 0003

00B7 This value is stored into ANSW1 and ANSW (LS BYTE).This binary number is then transmitted to the D/A output channel.

The following short flowchart indicates the D/A operation.



11.3 D/A CONVERTER TEST PROGRAM.

This program was developed to be user-friendly and will perform the task in the following manner;

1. It will display the following message on the monitor:

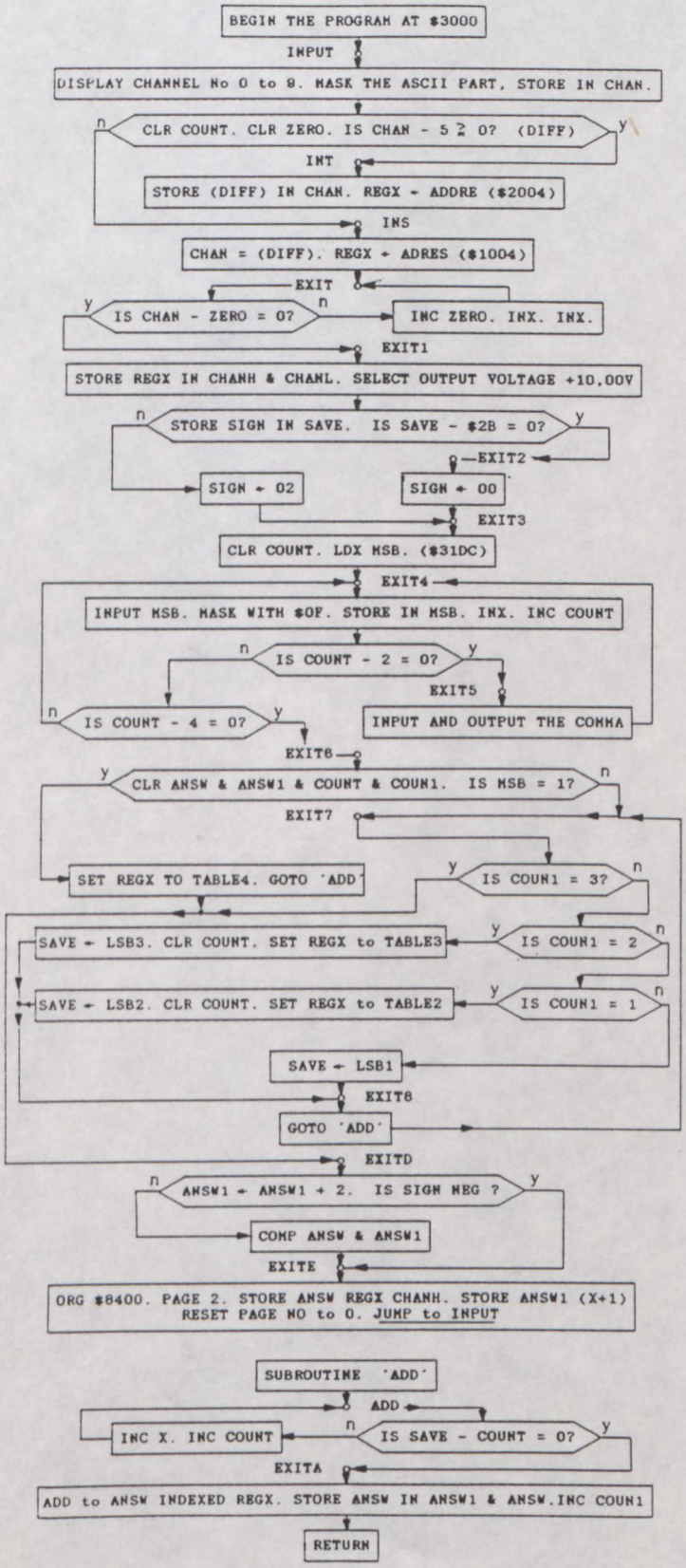
   SELECT THE CHANNEL No 0 TO 9.

2. After the operator replies to the channel number request, the program will ask for the output channel voltage value on the monitor:

   SELECT THE OUTPUT VOLTAGE IN THE FORMAT +10,00V

The following page illustrates the flow chart for this test program.

11.4 D/A CONVERTER TEST PROGRAM FLOW CHART.



11.5 GENERAL INFORMATION.

The technical design and operation of this section are contained in the seperate appendix called

INTERFACING DIGITAL AND ANALOG SYSTEMS.

THE DIGITAL TO ANALOG CONVERTER.

This appendix supplies:

1. Background to the designs.

2. Complete design and circuit diagrams.

3. Wire wrap boards.

4. Test programs with flow charts and program listings.

5. All data sheets on the components used in the design.

NB. It is recommended to refer always to this document.

The index of the module is listed on the following page.

11.6 D/A CONVERTER APPENDIX INDEX.

1.

12. APPLICATION OF THE UNIVERSAL MICROCOMPUTER SYSTEM.

12.1 INTRODUCTION.

The system was applied to one application in the laboratories of the Department for Mechanical Engineering of the University of Stellenbosch.

The application involved the intelligent control of a Photoelastic Oven Temperature Controller. This was attempted because numerous requests to the supplier of this oven in the USA, to improve the controller of their product was in vain.

Although this is a relative small application of the microcomputer, it emphasises the power available to the user.

12.2 PHOTOELASTIC OVEN TEMPERATURE CONTROLLER PROJECT.

The oven, as supplied by Photolastic Inc in Malvern, Pensilvania, USA, is equipped with a Partlow Recorder controller. The control point is determined by a cam-follower which rides the edge of a revolving cam. This cam must be cut specifically for a desired temperature curve.

A temperature limit of 5°C is set to operate above the selected temperature of the cam.

This controller, as supplied by Photolastic Inc, suffers from a number of shortcomings. Some of these are:

1. The temperature control accuracy is only $\pm$ 10°C.

2. A different cam has to be cut for every dissimilar temperature curve.

This oven is used extensively in testing strain gauge-devices. It was essential to drastically improve the accuracy of temperature control and the way to simulate the revolving cam.

An in-depth study of the system and controller led to the following solutions.

1. By using a Microcor Digital Controller the temperature control accuracy was improved to $\pm$ 0,5°C.

2. The revolving cam was replaced by the universal microcomputer system. A few minor changes were introduced to this system to achieve a very sophisticated control system.

The following text describes the complete design and modifications made to the system to accomodate the functions required.

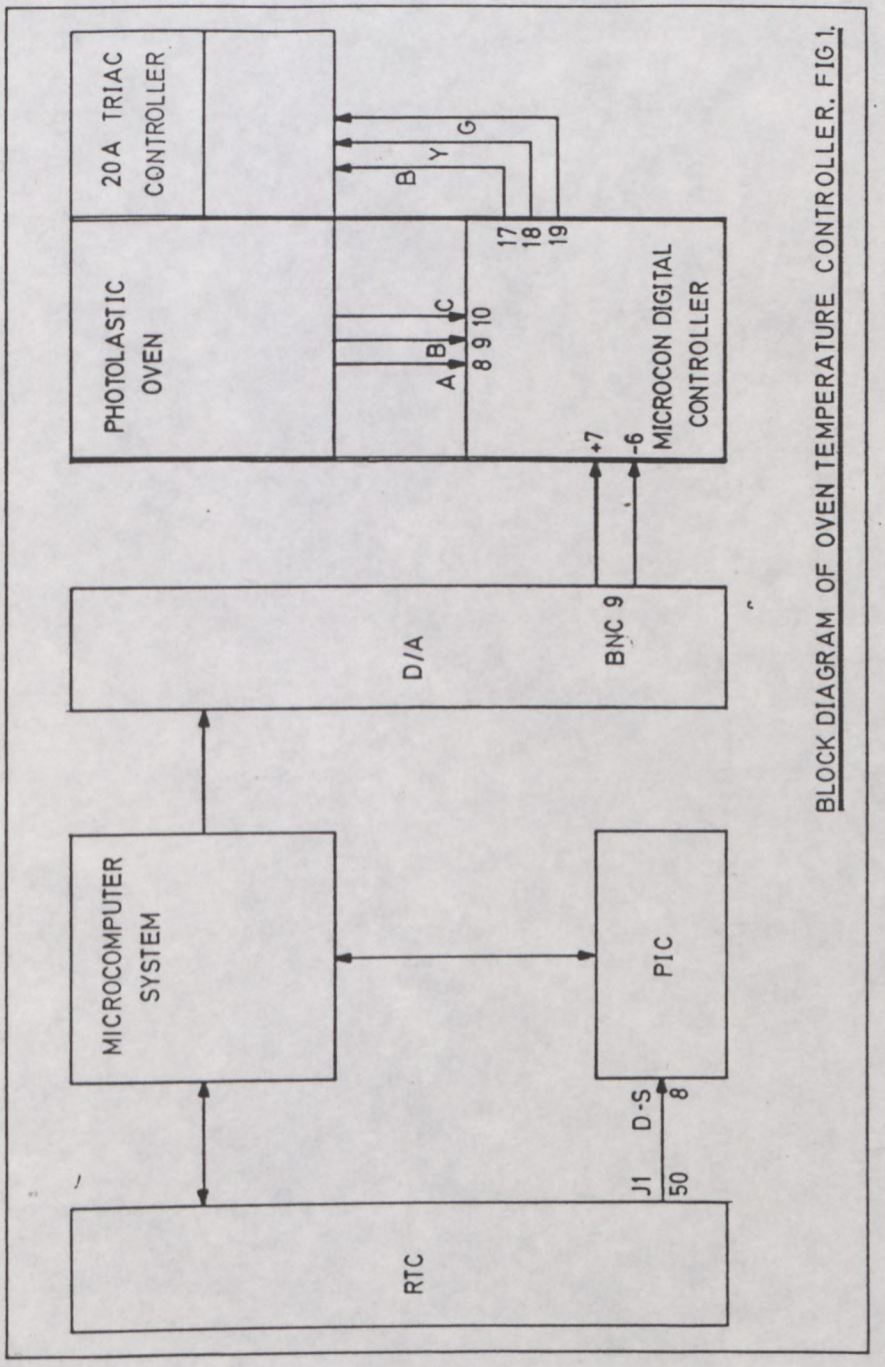
The block diagram of the control system is shown in FIG 10. The previous documents of the total microcomputer system must be studied to understand this document. The heart of the controller is the microcomputer system. This microcomputer controls:

1. Calender and clock.
2. D/A converter which feeds an analog signal to the Microcor Digital Controller, 0v = 0°C and +5v = 200°C.

The microcomputer is also coupled to the calender and real time clock, which interrupts the priority interrupt controller every 6 seconds. This in turn interrupts the control program to send a new analog temperature value to the Microcor Digital Controller.

The program resides in EPROM at memory location $5000.

FIG. 10 BLOCK DIAGRAM OF OVEN CONTROLLER.



12.3 PROGRAM OPERATING PRINCIPLE.

The hardware connection to the oven was a relative easy task. This illustrated the flexibility of the microcomputer system. However, the programming of the system was the major task.

The control program is stored on magnetic tape and on EPROM inside the system. This allows for easy and fast operation of the control program. The program resides at memory location $5000. A magnetic tape copy is available to allow easy change or modifications.

The control program addresses the D/A converter, the RTC and the PIC inside the system. It consists of two main sections.

1. The RTC setup and control part and
2. The oven temperature control section.

When the real time clock setup procedure is completed, the RTC will stay in this mode as long as the mains supply is on and the battery backup power is available.

Once the real time clock has been set up, restarting of the program can take place from memory position $5150. The user specifies the hourly increment from 0 to 200°C. Every hour interval must start from ambient temperature to a maximum of 200° C. The control program computes a ten-bit binary value for the

temperature every 6 seconds and outputs this value to the Microcor Digital Controller which activates the solid state relay.

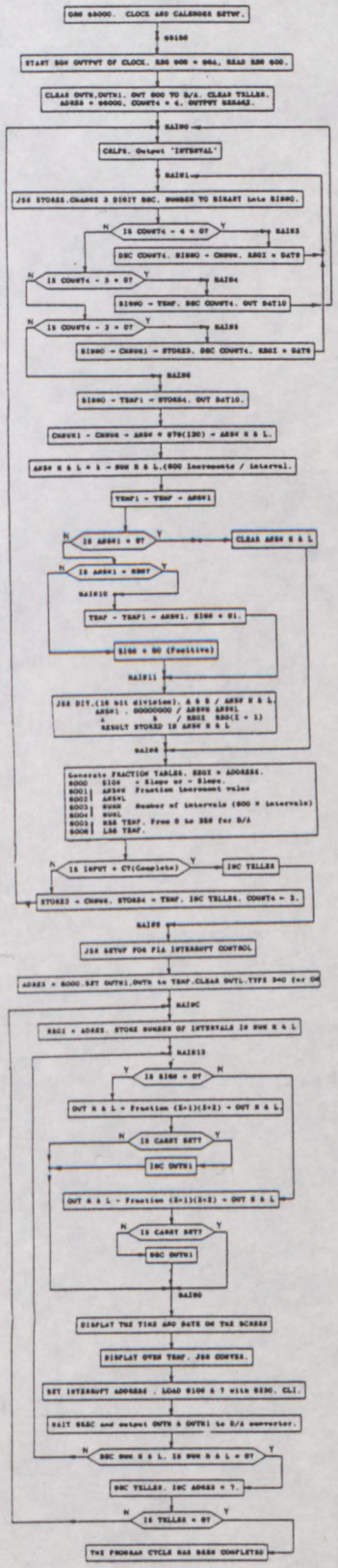
The microcomputer computes a linear function between specified intervals.

During the input operation of the interval and temperature values, the microcomputer calculates all the necessary increment values and data. These values are stored in a buffer area residing from memory position $6000. Every interval requires seven memory positions. Thus for a maximum value of 200 temperature values, this buffer will grow to 200 * 7 = 1400 bytes.(From $6000 to $6578)

Once the interval values are entered, the system waits for an interrupt occuring every 6 seconds, on which it will output a calculated value for the D/A converter. During this period the program displays the day, time, date and temperature of the oven on the monitor screen. A new screen display is generated every 6 seconds.

Program completion will be displayed on the monitor. All screen information is left on the screen as operator information. This following page illustrates a detailed flow chart of the control program.

12.4 OVEN TEMPERATURE CONTROLLER PROGRAM FLOW CHART.



12.5 GENERAL INFORMATION.

The technical design and operation of this section are contained in the seperate appendix called

PHOTOELASTIC TEMPERATURE OVEN CONTROLLER.

This appendix supplies:

1. Background to the designs.

2. Complete design and circuit diagrams.

3. Wire wrap boards.

4. Test programs with flow charts and program listings.

5. All data sheets on the components used in the design.

NB. It is recommended to refer always to this document.

The index of the module is listed on the following page.

12.6 OVEN TEMPERATURE CONTROLLER APPENDIX INDEX.

13. CONCLUSION.

The easy way in which the system adapted to the hardware specifications of the photoelatic oven emphasized the flexibility of the microcomputer system.

The software program offered an intelligent solution to the cam control problem and resulted in excellent performance.

The time, date and temperature is displayed every 6 seconds on the screen. This feature offers excellent monitor possibilities.

The main advantage of the system is its programability. The larger the investment in the software for a particular application, the better the overall performance.

The application program of the oven temperature controller can be vastly expanded to accommodate many extra features. Eight strain gauge signals, 16 condition indicaters plus 8 priority inputs and many other signals can all be monitored and introduced to a larger control sytem. The hardware is already available!

This system was already handed to the University of Stellenbosch in June 1987. Since then it operated faultless. The local agent and a representative for PHOTOLASTIC visited Stellenbosch during September 1987 and showed great interest in this system.

13.1 TEST EXAMPLES.

The following two pages show the results obtained from two different test runs. It can be seen that the graphs show very precise control. However, these graphs were drawn using the existing built-in PARTLOW recorder. Replacing this recorder with a high quality one will produce even better results.

Both these tests were performed over a total of 24 hours.

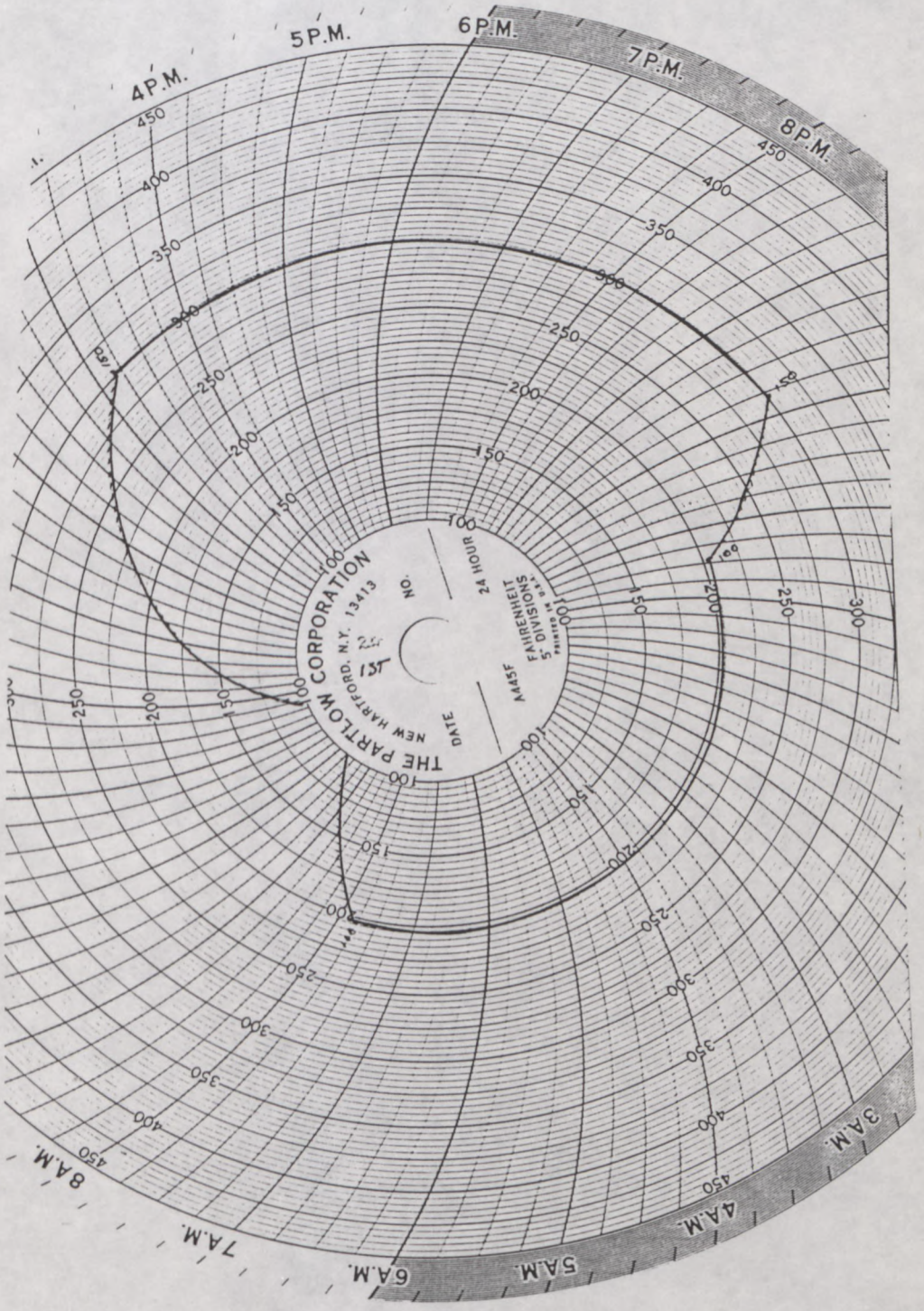
The first test followed the following temperature curves;

The first interval was after 3 hours	to 150°C.
second interval after 6,5 hours	at 150°C.
third interval after 1,5 hours	to 100°C.
fourt interval after 8,5 hours	at 100°C.
the last interval for 4,5 hours	to room temperature.

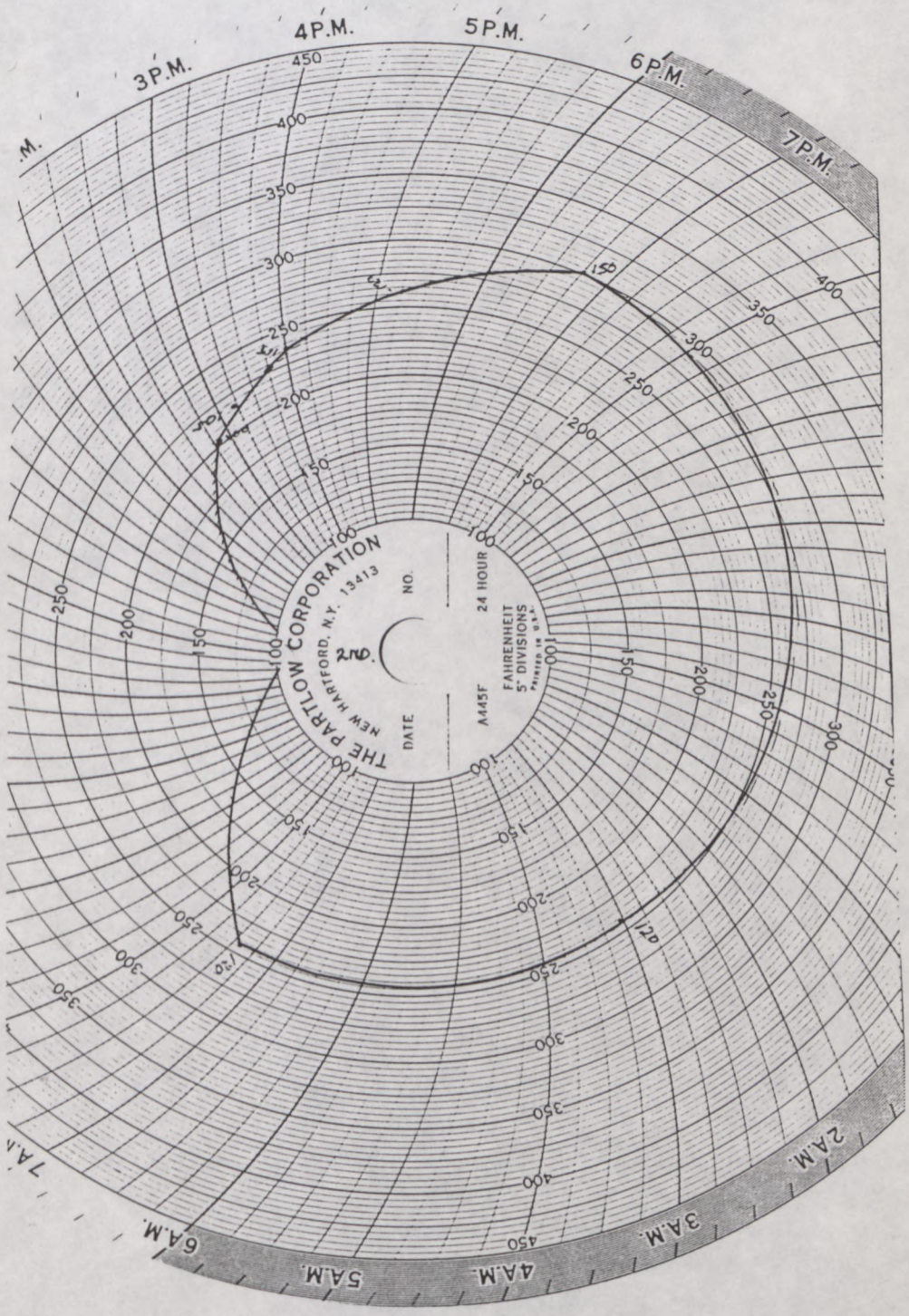
The program computes the exact linear temperature value, and displays the temperature on the screen. The non-linear sections of the curve on the Partlow recorder is caused by pen friction and the crude design of the Partlow recorder.

The second test run produced similar results.

THE FIRST TEST RUN.



THE SECOND TEST RUN.



14. REFERENCES.

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