An analogue controlled switch-mode power system for a CubeSat

by

Gavin Alexander Mutch

Thesis presented in fulfilment of the requirements for the degree of Magister Technologiae in Electrical Engineering at the Cape Peninsula University of Technology

Department of Electrical Engineering,
Cape Peninsula University of Technology

Supervisor: Dr. R.H. Wilkinson

April 2013

Declaration

I, Gavin Alexander Mutch, declare that the contents of this thesis represent my own unaided work, and that the thesis has not previously been submitted for academic examination towards any qualification. Furthermore, it represents my own opinions and not necessarily those of the Cape Peninsula University of Technology.

Signature: .....

G.A. Mutch

Date: .....

Copyright © 2013 Cape Peninsula University of Technology
All rights reserved.

Abstract

The power system is essentially one of the most critical subsystems to any satellite, without some form of power system a satellite would simply cease to function. The research within these pages investigates the areas pertaining to satellite power systems with the main focus towards the CubeSat platform. The end objective of this research was the development of a reliable analogue based switch-mode power system for a CubeSat.

The research began with an investigation into the CubeSat platform, the space environment and a basic overview of a satellite and its systems. The research then focussed on satellite power systems, focussing primarily on satellite power system topologies and switch-mode power systems. Various components and concepts surrounding the satellite power system were investigate and included the photovoltaic (PV) solar cell, batteries, satellite power system topologies, protection concepts and typical CubeSat power systems. The final part of the literature review included research into typical CubeSat power systems.

The space environment complicates the design of satellite systems. The developed electrical power system harnessed electrical power from a PV solar panel by means of a fractional open-circuit voltage (FOCV) based maximum power point tracker (MPPT) with the use of a SEPIC DC-DC converter. The use of a SEPIC DC-DC converter allowed the system to operate at a greater efficiency than could be expected from linear designs. The requirement for an efficient system was important as the heat generated by the power system could bring rise to dissipation issues, resulting in over-heating of various components. The design took into account component sizing, as larger components would be more prone to damage during the high accelerations and vibrations associated with being launched into space. The use of a MPPT allowed the power system to better utilise the available PV solar panel power, by maintaining the PV solar panel near its optimum operating voltage. The design slid between MPPT and voltage regulation to harness as much power as possible while not over-charging the Lithium polymer battery. The power system consisted of battery under-voltage protection as well as over-current protection for the attached payloads and satellite subsystems.

The SEPIC DC-DC converter was selected over other SMPS topologies, as this topology could be used in a 1U and 3U CubeSat with a wide variety of PV solar panel cell configurations. The benefits of this SMPS topology are due to the SEPIC DC-DC converter's ability to produce an output voltage greater than, less than or equal to the input voltage (National Semiconductor, 2008; Texas Instruments, 2008*a*). This, along with the operation of the FOCV based MPPT, allowed the power system to be very flexible. The designed FOCV based MPPT could be pre-set

to differing PV solar cell technologies due to the adjustable ratio between the maximum power point voltage, V_{mpp}, and the open-circuit voltage, V_{oc} of the PV solar panel. It was decided not to select a Buck or Boost DC-DC converter based power system as this would limit the flexibility of the system. Additionally, the SEPIC DC-DC converter brings with it the ability to isolate the input and output voltage upon shut down. This isolation is due to the SEPIC DC-DC converter's coupling capacitor and this topologies operation as described by National Semiconductor (2008) and Texas Instruments (2008*a*).

The prototype was versatile allowing a wide variety of PV solar cell technologies to be used. The wide operating voltage of the prototype allowed the design to be connected to a series or parallel combination of solar cells with an operating voltage of 3 V to 20 V. The power handling capability of the prototype per solar panel channel allows the design to be applied to a 1 U or 3 U CubeSat given that the channel did not exceed 10 W. All components of the prototype operated without fault, effectively charging the Li-poly battery safely while protecting payloads and subsystems. The SEPIC DC-DC converter utilised by the MPPT achieved an efficiency of 71 % under full load and with an input voltage of 10 V.

Acknowledgements

I would like to express my sincere gratitude to the following people and organisations:

- My supervisor Dr. Richardt Wilkinson for his guidance, support and interest in my work.
- The Centre for Instrumentation Research (CIR) and the French South African Institute of Technology (F'SATI) staff and students for their assistance and interest in my work.
- Prof. Gerhard de Jager, Jacques Wheeler and Prof. van Zyl for their support.
- My fellow research friends Charl Jooste, Jason Quibell and Jean Bester for their encouragement and suggestions towards my work.
- My family and friends for their motivation and encouragement.
- Everyone who took an interest in my work.

The financial aid of the National Research Foundation (NRF) IRDP programme and the National Research Foundation (NRF) through F'SATI towards this research project is acknowledged. Opinions expressed and the conclusions arrived at in this thesis are those of the author and not necessarily to be attributed to the NRF, F'SATI, CPUT or the CIR.

Contents

List of Figures

List of Tables

List of Abbreviations

Acronyms and abbreviations

AC	Alternating current
BCR	Battery charge regulator
BCDR	Battery charge/discharge regulator
BDR	Battery discharge regulator
BJT	Bipolar junction transistor
CC	Constant-current
CCM	Continuous-conduction mode
CIR	Centre for Instrumentation Research
COTS	Commercially off the shelf
CPUT	Cape Peninsula University of Technology
CV	Constant-voltage
CVCM	Collected Volatile Condensable Material
DC	Direct current
DCM	Discontinuous-conduction mode
DET	Direct energy transfer
DoD	Depth-of-discharge
DST	Department of Science and Technology
DTC	Dead-time control
ESIEE	École Supérieure d'Ingénieurs en Électronique et Électrotechnique
EMC	Electromagnetic compatibility
EMF	Electromotive force
EMI	Electromagnetic interference
EoC	End-of-charge
EPS	Electrical power subsystem
ESA	European Space Agency

FOCV	Fractional open-circuit voltage
F'SATI	French South African Institute of Technology
GaAs	Gallium Arsenide
Ge	Germanium
GM	Gain margin
IC	Integrated circuit
ISIS	Innovative Solutions In Space
I-V	Current-voltage relationship
LDO	Low-dropout regulator
LEO	Low Earth orbit
Li-ion	Lithium-ion
Li-poly	Lithium-ion polymer
MLCC	Mulit-layer ceramic capacitor
MOSFET	Metal-oxide-semiconductor field-effect transistor
MPP	Maximum power point
MPPT	Maximum power point tracking or maximum power point tracker
NiMH	Nickel-metal hydride
NRF	National Research Foundation
OBC	On-board computer
OCP	Over current protection
Op Amp	Operational amplifier
P&O	Perturb and observe
PCB	Printed circuit board
PCM	Power conditioning module
PDM	Power distribution module
PM	Phase margin
P-POD2	Poly-Pico Orbital Deployer version 2
PPT	Power point tracker
PV	Photovoltaic
P-V	Power-voltage relationship
PWM	Pulse width modulation

RBF	Remove before flight
S&H	Sample and hold
SCP	Short-circuit protection
SSDL	Stanford University's Space and Systems Development Laboratory
SEPIC	Single-ended primary inductance converter
SEL	Single event latch-up
SEU	Single event upset
Si	Silicon
SMPS	Switch-mode power system or switch-mode power supply
SoC	State-of-charge
S^3R	Sequential switching shunt regulator
TI	Texas Instruments
TML	Total Mass Loss
UTJ	Ultra triple junction

Chapter 1

Introduction

1.1 Background

The Ten-Year Innovation Plan of the Department of Science and Technology (DST), which is projected to be completed in 2018, was initiated to help drive South Africa's transformation towards a knowledge-based economy. The DST chose to focus on five grand challenge areas, these areas being the "Farmer" to "Pharma" value chain to strengthen the bio-economy, space science and technology, energy security, global change science with a focus on climate change and human and social dynamics (Department of Science and Technology, n.d.).

The Cape Peninsula University of Technology (CPUT) under the French South African Institute of Technology (F'SATI) Satellite Systems Engineering programme and in collaboration with École Supérieure d'Ingénieurs en Électronique et Électrotechnique (ESIEE) in Paris are offering a dual Master's degree using the CubeSat platform as a means to train students in satellite technology. The primary focus of F'SATI is the development of human capacity in the area of space science and technology and in so doing are aiding the DST in their Ten-Year Innovation Plan (Anon, n.d.).

The CubeSat platform standard aids in the education and training of students in real-world satellite systems and plans to help in the advancement of the aerospace industry. This has created a growing interest in the CubeSat standard by universities, organisations and governments for experimental projects as mentioned by Puig-Suari *et al.* (2008:1). This can be seen in how the CubeSat is fast becoming one of the most launched satellite platforms in history (Clark *et al.*, 2008:1).

The electrical power system (EPS) is one of the most critical subsystems to any satellite, without some form of electrical power system a satellite would simply cease to function. One of the most common causes of CubeSat mission failure is due to the failure of the power system. Purchasing a power system from a recognised manufacturer with many years of experience in the space arena is often impractical as this can bring additional, unwanted cost to building a CubeSat as mentioned by Clark *et al.* (2008:1). This brings about the need for a cost effective, yet reliable CubeSat power system for CPUT's Satellite Systems Engineering programme. To achieve this research must be done in the field of satellite power systems especially with concern to CubeSats.

Switch-mode power supplies are known for their high efficiencies and have the ability to produce an output voltage larger than, smaller than or equal in magnitude to their input voltage. This high efficiency and flexibility in input and output voltage give switch-mode power supplies a great advantage over linear based power supplies especially where only low levels of power are available, such as is the case with a CubeSat.

1.2 Statement of research problem

There is growing interest in the CubeSat platform as well as a growing need for a reliable, efficient and cost effective power system for these nano-satellites. This project is aimed at filling this need through the investigation and design of a reliable analogue based switch-mode power supply (SMPS) for use in a CubeSat, by considering various topologies and methods of power conversion used in satellites. The close proximity of different systems within the satellite increases the likelihood of electromagnetic compatibility (EMC) issues that could create instability or damage to susceptible subsystems; this creates a further need for some investigation into reducing EMC issues concerned with SMPSes.

1.3 Project objective

The primary objective of this project is the design of a functioning satellite power system for use in a CubeSat. This designed power system should have the potential to be used in future F'SATI space missions. Additionally this project is aimed towards increasing the knowledge base of F'SATI, the Centre for Instrumentation Research (CIR) and CPUT in the area of satellite power systems.

In order to achieve this objective the following research questions have significant importance:

- What are the required specifications for the power system?
- Which is the best power system topology to meet the requirements?
- What methods could be used in improving the reliability of the power system?
- What switch-mode DC-DC converters will be required in the design of the power system?
- What must be considered in the design of the power system in order to reduce possible EMC issues?

1.4 Research and design methodology

In order to answer the research questions and meet the primary objective the following research and design methodology will be followed:

- Investigate various satellite power system topologies.
- Investigate different switch-mode converter topologies used in satellite power systems.
- Investigate different methods of improving reliability.
- Determine the satellite power system specifications required for the CubeSat.
- Design, simulate and construct a prototype power system for use in a CubeSat.
- Perform tests in order to determine if the power system meets the specifications required.

1.5 Delineation of the research

In the thesis the research will focus primarily on different satellite power system topologies and switch-mode converter topologies required in designing a functioning satellite power system for use in a CubeSat. Some of the research will be on avoiding possible EMC issues involved with SMPS in an attempt to increase reliability of the satellite system as a whole as possible electromagnetic interference (EMI) emitted from the power system could damage or interfere with neighbouring satellite subsystems.

1.6 Significance and contributions of the research

The purpose of this study was to increase the knowledge of F'SATI, CIR and CPUT in the field of satellite electrical power systems as well as design an EPS that could later be implemented on a CubeSat in future F'SATI space missions. The power system is a key component to a functioning satellite, and as such there was a need to better understand this system, the environment it inhabits, and what is expected from a satellite system with concern to features and performance. The research investigates many facets of satellite power systems and resulted in the development of a functioning power system that could later be adapted for use in a CubeSat space mission.

Different DC-DC converter topologies were researched and the SEPIC DC-DC converter later chosen as the converter in which the EPS would be based upon. The developed satellite EPS relied on the SEPIC DC-DC converter SMPS topology utilising two control loops. These control loops are utilised separately depending on the operation mode of the developed EPS. The control loops maintain the PV solar panel voltage at its maximum power voltage, or regulate the battery voltage at its maximum charge voltage of 8.2 V. The selection of the appropriate control loop is governed by the power required in charging the battery and operating payloads. Accomplishing this design required research into feedback control loops, their compensation and various methods of PV solar panel maximum power point tracking (MPPT) techniques. This research provided

a better understanding of the analogue control of SMPS and the operation of differing MPPT techniques, such as perturb and observe (P&O) and fractional open-circuit voltage (FOCV). The knowledge gained in SMPS control and MPPT techniques can be applied both to terrestrial and space electrical power systems.

Additionally, this research could also bring about a financial benefit as an EPS could be developed within CPUT rather than by an external company or organisation for future satellite missions. The knowledge gained in this study could be applied to the design of future CubeSat EPS systems by CPUT and F'SATI. The ability to produce its own hardware would give CPUT more flexibility in the design of future missions as custom systems could be developed. A good understanding of the satellite EPS is fundamental to the success of a satellite mission as the EPS is critical to the operation of a satellite.

1.7 Thesis outline

The structure of the remainder of this document is as follows:

- **Chapter 2** introduces the CubeSat concept and standard, a general overview of a satellite and its subsystems, and describes the expected space environment, along with the damage this environment inflict on satellites. The aspects covered in this chapter include the requirements of the CubeSat standard and the damage that can be inflicted onto satellites by radiation, temperature, pressure, acceleration and vibration. This chapter also encompasses various aspects of satellite power systems, such as satellite power system topologies, switch-mode power systems and covers a brief overview of typical CubeSat power systems.

- **Chapter 3** focuses on the prototype design and verification of a CubeSat power system and the reasoning behind the decisions made during the design process.

- **Chapter 4** covers the testing and evaluation of the designed prototype.

- **Chapter 5** concludes and summarises this document. In this chapter recommendations as well as proposed future work are discussed.

Chapter 2

The CubeSat platform

2.1 Introduction

This chapter introduces the CubeSat as a satellite platform along with the basic blocks associated with any satellite. This chapter illustrates where the difficulties associated with designing a satellite system lie, along with the importance of the power system. The satellite electrical power system comprises of a few main components, these components are essential to the operation of the power system and are discussed in detail later in this chapter.

Initially the CubeSat project began as a collaboration between two professors, Prof. Jordi Puig-Suari at the California Polytechnic State University in San Luis Obispo and Prof. Bob Twiggs at Stanford University's Space and Systems Development Laboratory (SSDL). The purpose of the CubeSat project is to provide a standard for the design of nano-satellites. This standard was intended to reduce costs and development time, increasing accessibility to space, and sustain the frequency of launches. The main objective of the CubeSat programme was to provide access to space for small payloads (Munakata *et al.*, 2009:5).

A CubeSat is a 10cm x 10cm x 10cm satellite cube having a mass of up to 1.33 kg and typically manufactured from 7075 or 6061 aluminium. CubeSats are available in multiples of this single unit. In the case of a triple CubeSat, a 3U, the satellite has a dimension of 10cm x 10cm x 30cm and has a mass of up to 4.0 kg (Munakata *et al.*, 2009:5).

The CubeSat satellite platform has been used in many satellite missions with a wide variety of payloads and mission goals as shown by Thomsen (2009). Examples of these missions include the testing of commercially off the shelf (COTS) components, scientific missions and amateur radio missions.

The CubeSat satellite platform standard has many requirements. The power system might hinder the satellite's compliance with this standard in the following areas (Munakata *et al.*, 2009:9–11):

- The total stored chemical energy on a CubeSat shall not exceed 100 Watt-Hours.
- No hazardous materials shall be used on a CubeSat.
- The out-gassing limits of the standard.
- No electronics shall be active during launch to prevent any electrical or RF interference with the launch vehicle and primary payloads.
- The CubeSat shall include a 'Remove Before Flight' (RBF) pin or launch with batteries fully discharged. The RBF shall cut all power to the satellite when inserted into the satellite.
- The CubeSat shall include at least one deployment switch. This switch shall be located on the designated rail standoff to completely turn off power to the satellite once actuated. This shall turn off all systems including real-time clocks.

The out-gassing limits of the standard require that the materials used shall have a Total Mass Loss (TML) $\leq 1.0\%$ and have a Collected Volatile Condensable Material (CVCM) $\leq 0.1\%$ as described in Munakata *et al.* (2009:8).

The CubeSat satellite platform subsystems resembles that of any satellite, with the mission governing the required subsystems of the satellite. The satellite and its various subsystems are required to withstand the hostile space environment, along with the stresses involved during launch. These stresses bring added complexity to the design of the satellite.

2.2 The space environment

2.2.1 Radiation

In space there are two kinds of radiation that significantly affect satellites, electromagnetic radiation and particle radiation. Most of this radiation comes from the Sun, but radiation from the cosmos and the Earth's magnetic field are also of some importance to orbiting spacecraft. The particle radiation found in the Earth's magnetic field is essentially particle radiation that has been caught in the Earth's magnetic field (Alminde *et al.*, 2001:21). This radiation moves around the Earth in broad belts, known as the Van Allen Belts. Electromagnetic and particle radiation can bombard a satellite, and for this reason satellite electronics need some resilience to this radiation. Radiation is known to cause logic device errors, when high energy particles hit a device problems can occur in two possible ways. The first occurs when a high energy particle shoots through the device material leaving an ionised path. This ionised path acts as a short-circuit between individual parts/layers of the device. The second cause occurs when a high energy particle hits an atom with enough energy to split it. The individual parts of the

atom will then each trace a path of ionised particles through the device material (Alminde *et al.*, 2001:21).

This phenomenon can cause a Single Event Upset (SEU) or Single Event Latch-up (SEL) to occur. A SEU can change digitally stored data or cause a gate to *open* or *close* unexpectedly. A SEL is caused when this phenomenon causes physical damage to the device, this event has the potential to affect other devices, for example bus contention which occurs when various devices attempt to force different voltages on a fixed point. This could lead to the damage of multiple devices and not just the device affected by the SEL (Alminde *et al.*, 2001:21).

2.2.1.1 Radiation damage to photovoltaic solar cells

"Different charged particles in the space environment have significantly different energy levels due to their different masses and velocities" as stated by Patel (2005:169). The heavier particles cause more damage for a given energy. Different charged particles having the same energy levels cause different damaging effects on the short-circuit current, I_{sc}, and the open-circuit voltage, V_{oc}, of PV solar cells (Patel, 2005:169). This damaging effect changes the characteristics and power generating capability of PV solar cells.

2.2.2 Temperature and pressure

Generally CubeSats are expected to operate within Low Earth Orbit (LEO). At these altitudes the atmosphere is very thin and can be considered a vacuum in practical terms. Care must be taken in choosing components that operate in this vacuum environment as those consisting of volatile materials can be prone to evaporation (out-gassing). The transfer of heat within a satellite can cause problems if not properly considered, as the vacuum only permits heat to be transferred through heat conduction and heat radiation. This limited heat transfer ability may bring rise to heat dissipation issues within the satellite, as such the power system must be constructed such that as little heat as possible is produced(Alminde *et al.*, 2001:22).

The maximum expected temperature range for electronics within a CubeSat in LEO is between $-40°$ C and $85°$ C as mentioned by Obland *et al.* (2002). This corresponds closely with Connolly (2000:5) with a predicted maximum operating temperature in LEO for the Poly-Pico Orbital Deployer 2 (P-POD2) at $-40°$ C to $80°$ C.

2.2.3 Acceleration and vibration

While a satellite is in orbit there are no externally induced vibrations, and acceleration (gravity) is far less than on Earth as stated by Alminde *et al.* (2001:22). However, during the launch there are strong vibrations and high levels of acceleration (Alminde *et al.*, 2001:22). This high acceleration requires the satellite to withstand up to 16g of acceleration (Obland *et al.*, 2002). To reduce the risk of components breaking off during the high acceleration of launch, tall and heavy components should be avoided, as well as mechanical components such as potentiometers (Alminde *et al.*, 2001:22).

2.3 Overview of a satellite

The requirements of a satellite's mission are largely governed by the subsystems that are to be found on the satellite. The systems within a satellite are classified into two groups, namely the payload systems and the bus systems. Figure 2.1 illustrates the typical systems associated with a satellite (Patel, 2005:3). Many of these systems fall outside the scope of the research as the main focus is on the EPS. It is still important to note the systems that are present on satellites, as the majority of these systems are dependant on the EPS for their operation.

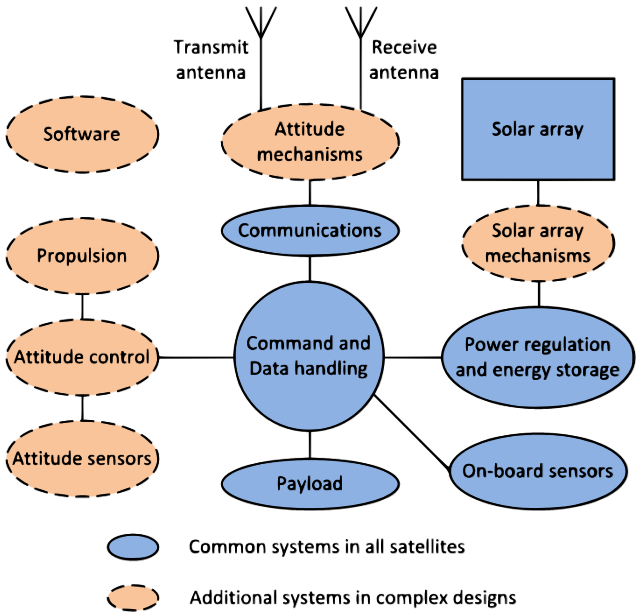

Figure 2.1: Satellite systems redrawn from Patel (2005:3)

The EPS comprises of "the solar array, solar array drive, battery, battery charge and discharge regulators, bus voltage regulator, load switching, fuses, and the distribution harness" as stated by Patel (2005:5). "This system generates, stores, conditions, controls, and distributes power within the specified voltage band to all bus and payload equipment" as stated by Patel (2005:5).

2.4 Satellite power systems

The only external source of energy available in space is solar radiation, as such any spacecraft power system not using solar energy must be able to carry its own source of energy. These sources can include fuel cells, nuclear or chemical fuel (Patel, 2005:40). The main types of energy sources found typically on a CubeSat are batteries and/or photovoltaic (PV) solar cells as stated by Bettex (2010).

A block diagram illustrating the basic components of a spacecraft power system can be seen in Figure 2.2. These basic components consist of the primary energy source, energy conversion, power regulation and control, rechargeable energy storage, power distribution and protection, and power utilised by loads such as payloads and other systems on the spacecraft (Patel, 2005:40). McDermott (2008:407) produced a similar breakdown of a spacecraft EPS in order to determine the requirements for the hardware, software and interfaces for each of these basic components.

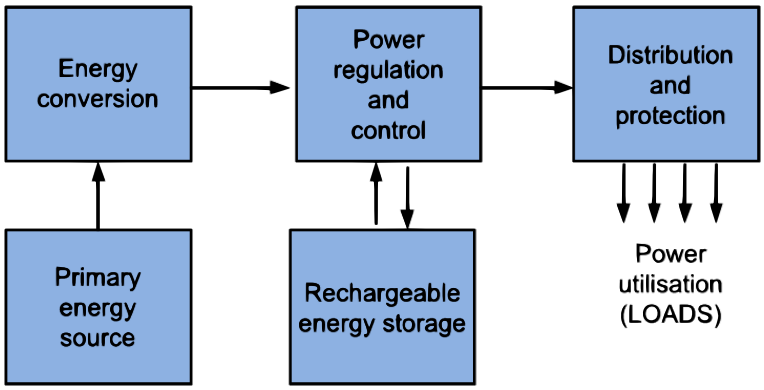

Figure 2.2: Spacecraft power system components redrawn from Patel (2005:40)

The typical top-level functions a spacecraft EPS might be expected to perform are listed as follows, taken from McDermott (2008:407):

- Supply a continuous source of electrical power to spacecraft loads during the mission life.
- Control and distribute electrical power to the spacecraft.
- Support power requirements for average and peak electrical load.
- Provide converters for AC and regulated DC power buses, if required.
- Provide command and telemetry capability for EPS health and status, as well as control by ground station or other autonomous system.
- Protect the spacecraft payload against failures within the EPS.
- Suppress transient bus voltages and protect against bus faults.

Some of these functions are not required of a CubeSat electrical power system, but the basic concepts still apply.

2.4.1 Photovoltaic solar cells

PV solar cells convert solar radiation from the sun into electrical power used in charging batteries and powering electrical loads. The primary energy source seen in Figure 2.2 constitutes the solar radiation while the energy conversion is done through the use of the PV solar cells. The literature within this section investigates PV solar cells as they are one of the main sources of energy typically found on the CubeSat (Bettex, 2010). The basic principle of operation of a PV solar cell is investigated along with a brief overview of different PV solar cell technologies.

2.4.1.1 Basic principle of operation of a photovoltaic solar cell

The basic principle of operation of the basic PV solar cell is based on the photovoltaic effect. According to this effect an open-circuit voltage is generated across a p-n junction when it is exposed to light. This light is typically in the form of solar radiation in the case of a PV solar cell. This open-circuit voltage leads to the flow of electric current if a resistive load is connected across it completing the circuit (Maini & Agrawal, 2011:145–146).

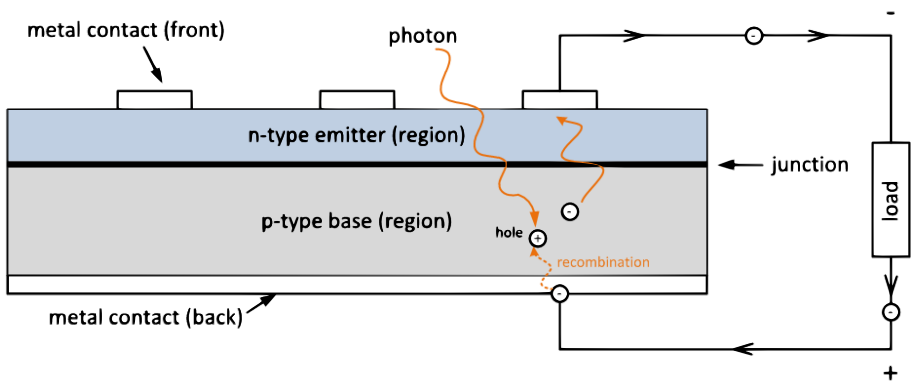

Figure 2.3: Basic principle of a photovoltaic solar cell redrawn from Maini & Agrawal (2011:148) and Flipsen (2005:25)

The energy of a beam of sunlight contains photons, when these photons hit the cell the energy of the photons frees electron-hole pairs. Each photon with enough energy will free an electron, resulting in a positively charged hole. Under the influence of the electric field at the metal contact the free electron will be sent to the n-side of the PV cell while the hole is sent towards the p-side. When a conductive path is formed between the two sides electrons will flow through this path in an attempt to meet and recombine with the holes. The cell voltage is due to the electric field found at the metal contacts while the flow of electrons constitutes the current, resulting in the power produced by the cell (Flipsen, 2005:26). An illustration of this can be seen in Figure 2.3 redrawn from Maini & Agrawal (2011:148) and Flipsen (2005:25).

The voltage and current drawn from a solar cell has a non-linear dependency on one another (Alminde *et al.*, 2001:173). The amount of power being generated by a solar cell is dependant on several external influences. These include the intensity of the light illuminating the cell, the temperature of the cell and the incidence angle at which light hits the cell (Liedholm, 2010:3). Figure 2.4 illustrates a typical solar array current-voltage (I-V) characteristic curve, and illustrates how temperature plays a role in the performance of a PV solar cell (Clark *et al.*, 2008:2).

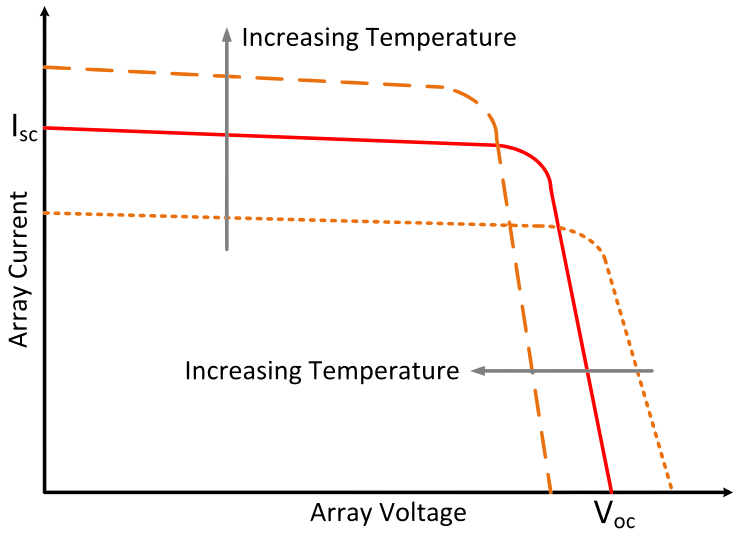

Figure 2.4: Solar array characteristic redrawn from Clark *et al.* (2008:2)

The power output of the cell is voltage dependant, this voltage dependency implies that the choice of the operating voltage is very important in extracting the highest usable power from the solar cell. This dependency is illustrated in Figure 2.5 by the power-voltage (P-V) characteristic curve redrawn from Liedholm (2010:3). The voltage found at the maximum power point (MPP), known as V_{mpp}, is dependant on the external influences that affect the power generating capability of the cell. These influences may result in a varying V_{mpp}, the solution to this problem is to employ a maximum power point tracker (MPPT) as mentioned by Liedholm (2010:3). Many MPPT techniques exist of which some of the more commonly used ones are discussed later in Section 2.4.4.

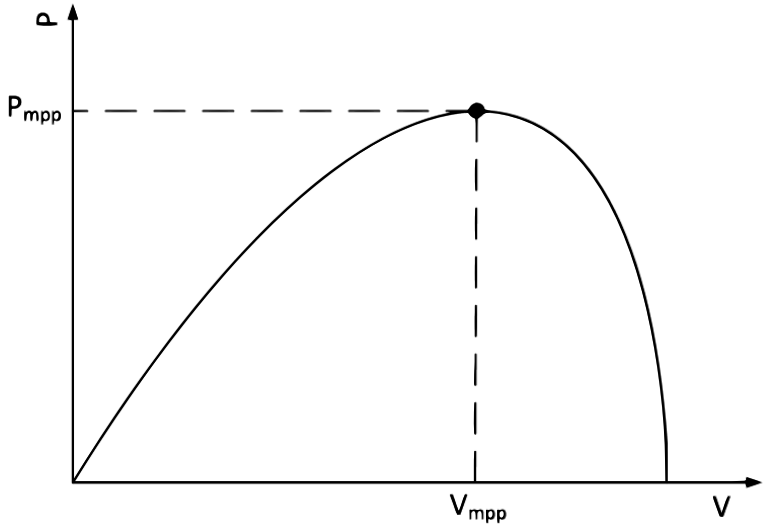

Figure 2.5: Typical power-voltage curve for a photovoltaic cell redrawn from Liedholm (2010:3)

There are a large number of equivalent circuits available that attempt to characterise the behaviour of PV solar cells. Most of these equivalent circuits are variations of the basic single diode model as stated by (Liedholm, 2010:3). Figure 2.6 shows one of the versions of the single diode model redrawn from Liedholm (2010:4) and Patel (2005:142). This model is characterised by Equation 2.4.1.

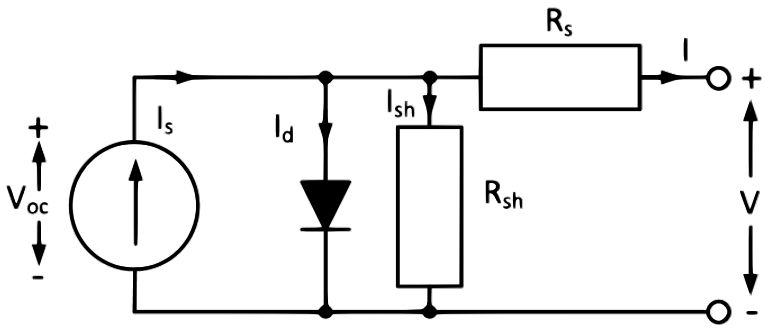

Figure 2.6: Single diode equivalent circuit for a photovoltaic cell redrawn from Liedholm (2010:4) and Patel (2005:142)

$$I = I_s - I_d - \frac{V_{oc}}{R_{sh}} \tag{2.4.1}$$

The PV solar cell acts much like a constant-current source shunted by a perfect diode. The parameters of the equivalent circuit are as follows: R_s represents the series resistance in the cell which inhibits the flow of current. This resistance is mainly due to the resistivity of the cell material. R_{sh} represents the shunt resistance, which takes into account the leakage current across the junction of the PV solar cell. This resistance is dependant on the purity of the material, the contact resistance and the depth of the p-n junction. This parameter, R_{sh}, is inversely proportional to the leakage current to ground. The PV solar cell's efficiency decreases with temperature as the magnitude of the diode current and the resistances of R_s and R_{sh} vary with temperature. In the equivalent circuit the current delivered to the load is the difference between the source current (photo current), I_s, and the sum of the diode-, I_d, and shunt I_{sh} currents. The open-circuit voltage, V_{oc}, can be determined when there is no output current, i.e. $I = 0$. V_{oc} is given by Equation 2.4.2, and the diode current is given by the classical diode current expression seen in Equation 2.4.3 (Patel, 2005:141–142).

$$V_{oc} = V + IR_s \tag{2.4.2}$$

$$I_d = I_0 \left[e^{\frac{qV_{oc}}{AKT}} - 1 \right] \tag{2.4.3}$$

The parameters associated with Equation 2.4.3 are:

I_0 represents the diode saturation(dark) current.
q = electron charge = $0.1592 \cdot 10^{-18}$ C.
A = curve fitting constant
K = Boltzmann's constant = $1.38 \cdot 10^{-23}$ J/K
T = absolute temperature, in kelvin (K).

Shading of PV solar cells results in a substantial loss of the cell's power generating capability. As can be seen from Figure 2.6, a PV solar cell functions as a current source with a parallel diode. Shading of a solar cell results in reduced current in that cell. If this cell is placed in series with other cells, operating under full illumination, the excess current from these cells will drive the shaded cell's 'diode' into reverse bias and eventually into breakdown operation. Diodes under breakdown operation no longer impede the flow of current in their reverse direction. Operating the 'diode' in reverse bias can result in heating of the 'diode' and possibly damage the PV solar cell. Additionally, partially shaded PV solar cells can result in a PV solar panel exhibiting several local maximum power points in their P-V characteristic. This can complicate the process of locating and tracking the MPP (Liedholm, 2010:5).

2.4.1.2 Photovoltaic solar cell technologies

Differing PV solar cell technologies exist, each with different properties. The sunlight wavelength spectrum is very important as not all energy absorbed by the PV solar cell is converted into electricity. Various cell technologies have differing operating wavelengths and as such photons with longer wavelengths are unable to generate hole-electron pairs required in the energy conversion process. These photons pass through the p-n junction of the solar cell and are absorbed at the bottom of the cell, causing heat to be generated. The majority of solar radiation lies within the 0.4 μm to 1.1 μm wavelengths (Patel, 2005:137).

The conversion efficiency of a PV solar cell is defined as (Patel, 2005:137):

$$\eta = \frac{\text{electrical power output}}{\text{solar power impinging the cell}} \tag{2.4.4}$$

Theoretical maximum energy conversion efficiencies for germanium (Ge), silicon (Si) and gallium arsenide (GaAs) are 16%, 24% and 29% respectively. Some of the major types of PV solar cell technologies are Single-Crystal Silicon, Gallium Arsenide (GaAs), Semicrystalline and Polycrystalline, Thin Film, Amorphous and Multi-Junction (Patel, 2005:137–141).

2.4.2 Batteries

Energy storage, such as batteries, are an integral part of a satellite's EPS. Any satellite that uses PV solar cells as a source of electrical power requires a means of storing energy for peak power demands and eclipse periods during the satellite's orbit. A battery consists of individual cells connected in series, where the number of required cells is determined by the required bus voltage (McDermott, 2008:418). As mentioned by Toorian *et al.* (2008:5), the most commonly flown batteries on the CubeSat platform are Lithium-ion (Li-ion) and nickel-metal hydride (NiMH) batteries, of which Li-ion are the more widely used due to their high energy densities. Batteries form the "Rechargeable energy storage" component of a spacecraft power system as illustrated in Figure 2.2.

Batteries operate due to the voltaic process (Flipsen, 2005:53). A galvanic or voltaic cell consists of two dissimilar electrodes immersed in a conducting material, such as a liquid electrolyte or fused salt. When these two electrodes are connected by a conductor, such as a wire, current will flow. At the surface of the separation between the metal and the electrolyte solution a difference in electrical potential is present. The electromotive force (EMF) of the cell is then equal to the sum of the two electrode potentials (Crompton, 2000:3).

Different types of batteries are available, single-use (primary) and rechargeable (secondary) batteries. In general, primary batteries have a few advantages over secondary batteries.

The advantages of primary batteries as stated by Flipsen (2005:53) are:

- larger energy density (Wh/kg) and specific energy (Wh/l).
- less subject to self-discharge, in other words have a longer shelf-life.
- larger power-per-use.
- the initial costs are lower.

The major disadvantage to primary batteries is they are not rechargeable whereas secondary batteries are rechargeable. Secondary batteries convert chemical energy into electrical energy during discharge. During charging of the battery electrical energy is converted into chemical energy. This process can be repeated for thousands of cycles. The satellite's orbital parameters determine the number of charge/discharge cycles the batteries have to support during the mission life (McDermott, 2008:419–420).

Figure 2.7 illustrates a typical charge-discharge characteristic of a spacecraft's energy-storage system. A flat discharge curve extends through most of the battery's capacity, it is desirable to have minimal overcharge. Battery cells may become unbalanced if their electrical characteristics are not matched. This causes stress that could degrade the batteries. This added stress on the batteries could lead to premature failure of the EPS (McDermott, 2008:418).

The depth-of-discharge (DoD) of a battery is simply the percentage of total battery storage capacity removed during a discharge period. Higher percentages of DoD result in a shorter battery life (McDermott, 2008:420).

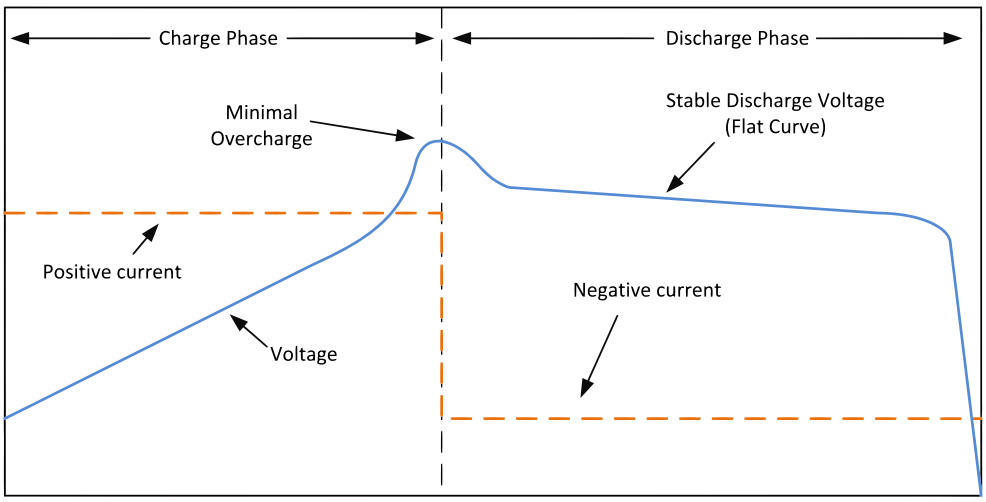

Figure 2.7: Battery charge/discharge profile redrawn from McDermott (2008:419)

2.4.2.1 Charge and discharge rate

The rate at which a battery is charged or discharged is often expressed in relation to its capacity known as the C-rate. This rate equates to a charge or discharge current which can be expressed through Equation 2.4.5 (Microchip, 2004:3).

$$I = M \cdot C_n \tag{2.4.5}$$

Where:

I represents the charge or discharge current in A.
M is a multiple or fraction of C.
C is a numerical value of the rated capacity in Ah.
n is the time in hours at which C is declared.

2.4.2.2 Lithium-ion voltage range

Over-charging Li-ion cells can lead to sudden destruction of the cell, similarly excessive discharge can decompose the anode causing copper shunts to form. This decomposition permanently hampers the performance of the Li-ion battery (Microchip, 2004:4). The usable voltage range for Li-ion battery chemistries can be seen in Figure 2.8.

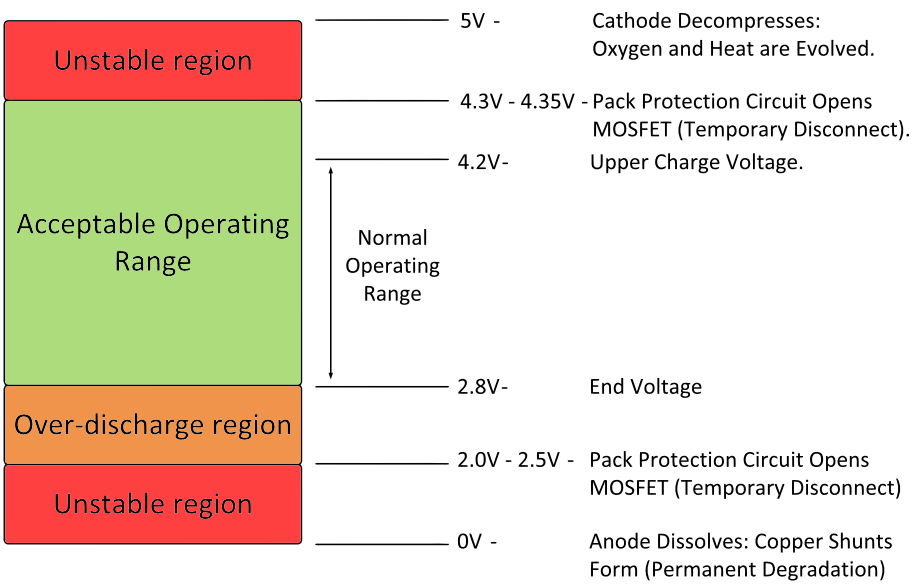

Figure 2.8: Lithium-ion cell voltage range redrawn from Microchip (2004:4)

Typically the Li-ion battery is only discharged to 3 V per cell and has a nominal voltage of 3.6 V for Li-ion or 3.7 V for lithium-ion polymer (Li-poly). Li-ion and Li-poly have similar charging processes. Li-ion and Li-poly are in fact so similar concerning the charge process that the same charge algorithms can be applied to both types of cells (Buchmann, 2001:61,86).

2.4.2.3 Lithium-ion charging

The preferred charging method of Li-ion battery chemistries is a constant-current (CC), constant-voltage (CV) method consisting of three stages. These three stages are trickle charge, fast or bulk charge and constant-voltage (Microchip, 2004:4).

The first stage, the trickle charge stage, is only used to restore deeply depleted cells. The cell is charged with a maximum constant-current at 0.1 C when the cell voltage is below 2.8 V. The second stage, the fast charge stage, charges the cell at a rate of less than 1.0 C while the final stage, the constant-voltage stage, is initiated when the cell reaches its end-of-charge (EoC) voltage of 4.2 V (Microchip, 2004:4).

2.4.2.4 Lithium-ion temperature range

Li-ion batteries are typically charged within the temperature range of 0° C to 45° C as stated by Microchip (2004:7) and Sony (n.d.:55). Charging Li-ion batteries outside this range can cause mechanical breakdown or venting of the battery due to an increase of pressure brought on by heating. This may lead to hampered performance of the battery or a reduction in the battery's life expectancy (Microchip, 2004:7). It is also recommended by Sony (n.d.:55) that Li-ion batteries be discharged within the temperature range of −20° C to 60° C.

2.4.3 Satellite power system topologies

The power regulation and control component of the satellite power system comprises of a few functional blocks, these blocks are typically the solar array regulator(s), battery charge regulators (BCRs) and battery discharge regulators (BDRs) (O' Sullivan, 1994). Some designs combine the BCR and BDR forming one functional block, the battery charge/discharge regulator (BCDR).

There are an extensive variety of power system topologies used by satellites. Clark & Lopez (2006:1) point out the following as the most commonly used satellite power system topologies:

- Direct Energy Transfer (DET) with battery bus.
- DET with regulated bus.
- Maximum Power Point Tracking (MPPT) with battery bus.

These topologies can be placed into two main groups, the DET and the non-DET topologies. The MPPT topologies rely on a regulator placed in series with the solar array and the load. This series regulator is typically a switch-mode DC-DC converter whereas in the DET topologies a shunt regulator is typically placed in parallel with the solar arrays and load (McDermott, 2008:426).

2.4.3.1 Direct energy transfer with battery bus

DET with battery bus is one of the simplest configurations and is most commonly selected for its low mass benefit when compared to other topologies. This topology consists of only a solar array regulator and no SMPS elements. This simple and small design allows this topology to have a low mass while having a seemingly cost-effective design. The low cost and low mass of this topology makes it seemingly desirable, but there are disadvantages to its use as mentioned by Clark & Lopez (2006:2–3). Figure 2.9 illustrates a simplified diagram of a DET with battery bus. In typical applications a shunt regulator is added to prevent over-charging of the battery.

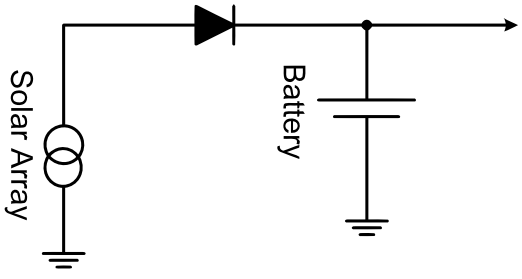

Figure 2.9: DET with battery bus redrawn from Clark *et al.* (2008:2)

The major drawback of this topology is the highest efficiency achieved by the solar array is only when the battery is fully charged and the panels are at their maximum temperature (Clark *et al.*, 2008:2). This major drawback makes this topology unsuitable for most missions as the amount

of power available is limited, and by increasing the size of the solar array to meet the power requirements of the satellite the overall mass of the satellite is increased.

2.4.3.2 Direct energy transfer with regulated bus

The European Space Agency (ESA) favours the DET with regulated bus approach, and as such it is the most commonly used power system topology in European spacecraft (Clark *et al.*, 2008:2). This topology is similar to the DET with the addition of a BCDR used to avoid battery overcharge and regulates the bus voltage to other subsystems. Figure 2.10 illustrates a block diagram of such a system redrawn from Maini & Agrawal (2011:144).

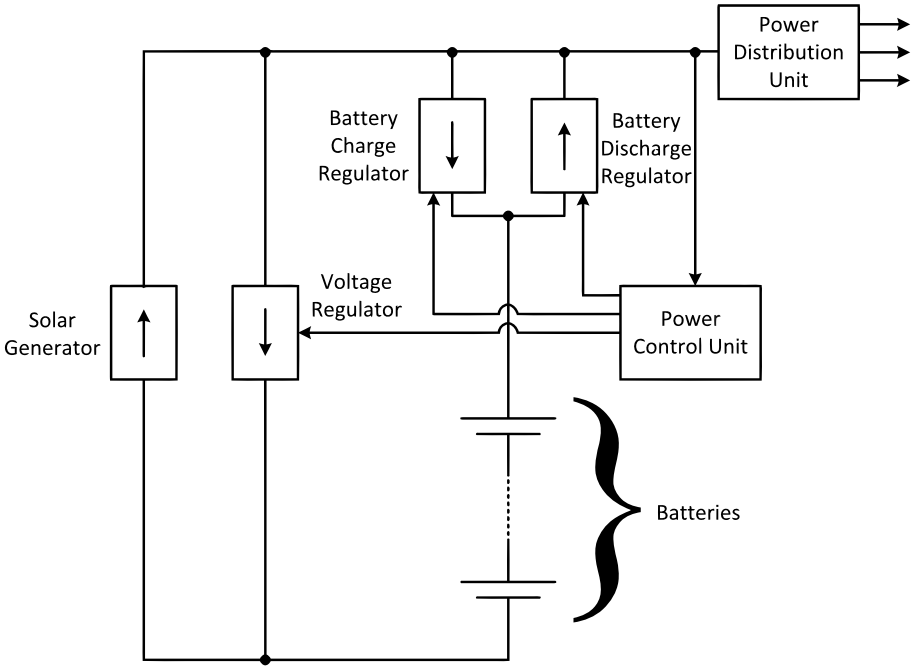

Figure 2.10: Basic block schematic of a solar energy driven power system redrawn from Maini & Agrawal (2011:144)

2.4.3.3 The sequential switching shunt regulator

The sequential switching shunt regulator (S^3R) is essentially a 'non-dissipative' shunt regulator and was first introduced and patented by D. O'Sullivan and A. Weinberg of ESTEC. The main qualities of the S^3R as mentioned by Perol (1998:79) are:

- Simplicity
- Modularity
- Stability

A schematic of the S^3R redrawn from Perol (1998:79) and O' Sullivan & Weinberg (1977:127) can be observed in Figure 2.11. As the shunt is merely a switch to bus or ground, the solar array voltage is always defined. These defined voltage levels are the bus voltage or zero. The modularity is realised through the use of multiples of the same design (C1–Cn), each of which

has the same weight and play the same role. The bang-bang operation of control of the S^3R defines the output voltage ripple and gives the system its stability (Perol, 1998:79).

This topology operates by bringing PV solar panels into play when required by electrical loads. As more power is required and the bus voltage begins to drop more switches are opened supplying more electrical power to the loads. The major benefit of this topology is a reduced power consumption in comparison with other DET methods, this is due to the switching operation of the shunts.

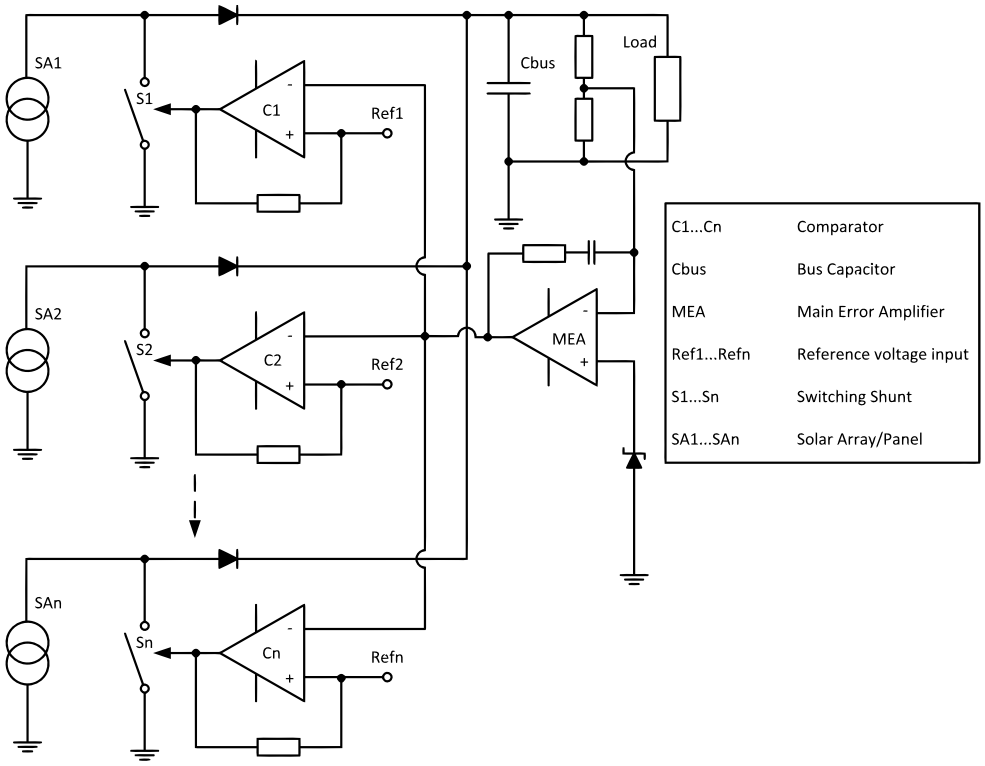

Figure 2.11: Sequential switching shunt regulator (S^3R) redrawn from Perol (1998:79) and O' Sullivan & Weinberg (1977:127)

This system is essentially a form of DET and as such has the same drawback as the DET topologies in terms of having the highest efficiency from the solar array when the batteries are fully charged and the panels are at their maximum temperature (Clark & Lopez, 2006:3).

2.4.3.4 Maximum power point tracking with battery bus

The MPPT topology operates by setting the solar array voltage to a point of maximum power, the power from this system charges the battery and supplies power to the bus during sunlit periods. When the battery has reached its EoC state the MPPT fixes the battery charge voltage allowing the battery current to naturally drop to a trickle charge level (Clark & Lopez, 2006:3). Figure 2.12 shows a simplified MPPT with battery bus topology.

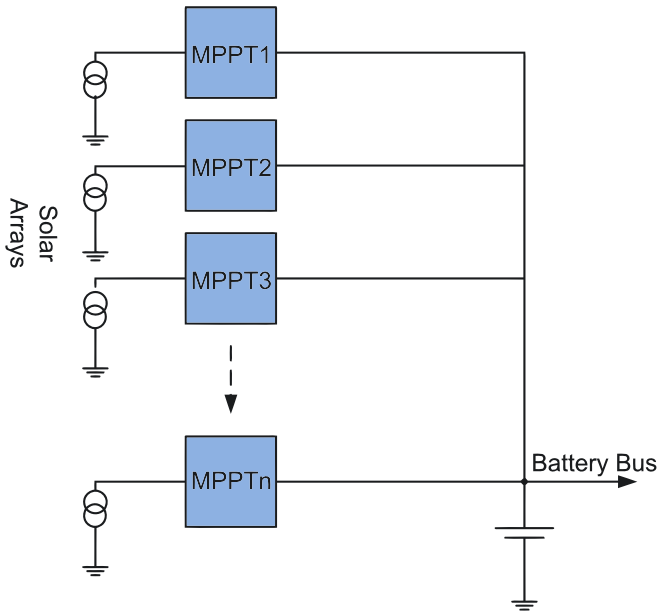

Figure 2.12: MPPT with battery bus redrawn from Clark *et al.* (2008:3)

"The ideal topology for CubeSats and miniature spacecraft is the MPPT with battery bus system" as stated by Clark *et al.* (2008:3). Numerous MPPT techniques exist of which the fractional open-circuit voltage (FOCV) and Perturb and Observe (P&O) based techniques are mentioned in Section 2.4.4.

2.4.4 Maximum power point tracking techniques

There are several MPPT techniques, these techniques consist of analogue and digital methods of control. Certain techniques favour different control methods (Esram & Chapman, 2007). Some of the more commonly used techniques are explained in subsequent sections.

2.4.4.1 Perturb and observe MPPT technique

The P&O process works through perturbation of the system through increasing or decreasing the solar array's operating voltage and observing the impact it plays on the solar array's output power (Pongratananukul, 2005:31). The solar array's operating voltage is perturbed with every MPPT cycle, as soon as the maximum power point (MPP) is reached the voltage of the array will oscillate around the ideal V_{mpp}. Figure 2.13 along with Table 2.1, redrawn from Pongratananukul (2005:32), help to illustrate the operation of the P&O method of MPPT.

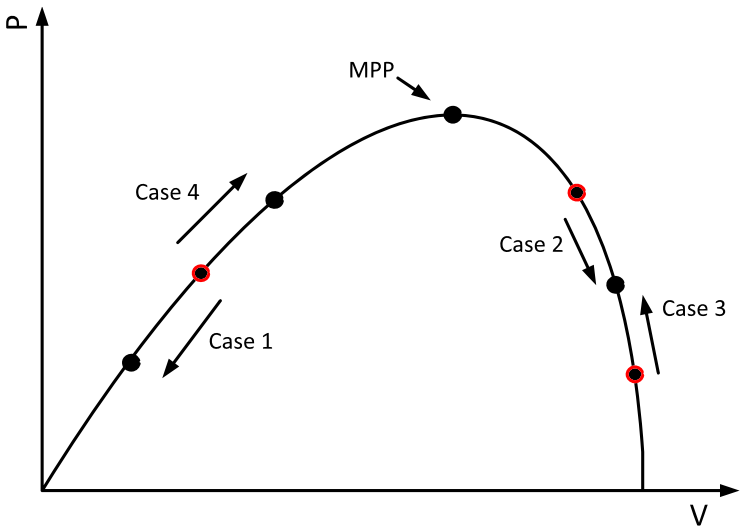

Figure 2.13: Perturb and observe control action redrawn from Pongratananukul (2005:32)

Table 2.1: Perturb and observe control action.

Case	dP	dV	Action
1	< 0	< 0	+
2	< 0	> 0	-
3	> 0	< 0	-
4	> 0	> 0	+

The fundamental principle behind P&O involves measuring the solar panel voltage and current while perturbing the panel's operating voltage. The power received at the current operating voltage is compared with the power received at a previously measured operating voltage. If the power received at the current voltage is higher than the previously measured voltage the perturbation to the operating voltage continues in the same direction as the previous perturbation. If the power received is less than that previously measured the perturbation will take place in the opposite direction. The "Action" seen in Table 2.1 denotes whether the operating voltage of the PV solar panel should be increased or decreased in an attempt to locate the MPP. When used in conjunction with a switch-mode power converter, changing of the operating voltage is done indirectly by changing the duty-cycle of the power converter. Changing the duty-cycle of the power converter affects the amount of current drawn from the PV solar panel thereby altering its operating voltage. This method of locating the MPP is often referred to as hill-climbing (Liedholm, 2010:6).

2.4.4.2 Fractional open-circuit voltage

The FOCV based MPPT technique relies on a specific solar array voltage corresponding to the maximum power point. This voltage shows a linear dependence to the open-circuit voltage of the

solar array, for varying irradiation and temperature levels. The relationship between the open-circuit voltage, V_{oc}, and the maximum power point voltage, V_{mpp}, is illustrated by Equation 2.4.6 (Ahmad & Kim, 2009:713).

$$V_{mpp} = M_v \cdot V_{oc} \tag{2.4.6}$$

In Equation 2.4.6 M_v is the voltage factor used in illustrating the linear dependance between V_{oc} and V_{mpp}. This factor is typically in the range 0.7 - 0.8 and is dependant on the characteristics of the solar panel (Ahmad & Kim, 2009:713).

To operate a solar panel at the MPP using this technique the actual panel voltage, V_{pv}, is compared with a reference voltage, V_{ref}. This reference voltage corresponds with the maximum power point voltage, V_{mpp}. The comparison of these two signals, V_{pv} and V_{ref}, results in an error signal used in operating a SMPS's pulse width modulator (PWM). The processing of this error signal in turn leads to $V_{pv} = V_{ref}$. The open-circuit voltage, V_{oc}, is usually sampled with the solar panel disconnected from the load. The fraction of this voltage corresponding to the V_{mpp} is sampled and held to function as V_{ref} for the converter's control loop (Ahmad & Kim, 2009:713).

2.5 Switch-mode power systems

2.5.1 Linear and switch-mode power supplies

Regulated linear and switch-mode DC power supplies are needed in a wide range of applications in electronics. Most power supplies are designed to meet at least one of the following requirements as stated by Mohan *et al.* (2003:301). These requirements are:

- **Regulated output.** The output voltage must be held constant within a specified tolerance for changes within a specific range in the input voltage and the output loading.
- **Isolation.** The output may be required to be electrically isolated from the input.
- **Multiple outputs.** There may be multiple outputs (positive and negative) that may differ in their voltage and current ratings. Such outputs may be isolated from each other.

Regulated linear power supplies have the ability to produce a very high quality output voltage and are best suited to applications where a low power level is required (Czarkowski, 2001:211). The main electronic device or devices within these supplies operate in their linear region, and act much like an *adjustable resistor*, where the difference between the input voltage and the desired output voltage can be found across the device as stated by Czarkowski (2001:211) and Mohan *et al.* (2003:301).

This *adjustable resistor* characteristic limits the magnitude of output voltage of the linear power supply to a magnitude smaller than that of the input voltage (Czarkowski, 2001:211). Operating

electronic devices such as MOSFETs or BJTs in this region can cause a significant amount of power loss, making them impractical in many applications where a high level of power or efficiency is required as mentioned by Czarkowski (2001:211) and Mohan *et al.* (2003:301).

Regulated switch-mode power supplies widely use DC-DC switch-mode converters in their operation (Mohan *et al.*, 2003:161). These converters use power electronic semiconductor switches which can be in either an *on* or *off* state. In these states very little power is dissipated as there is a low voltage across the switch when a high current flows or a high voltage across the switch when a low current flows. Modern semiconductor switches can switch at a high rate allowing for compact designs as small filters and transformers can be used. Switch-mode DC-DC converters have an advantage over linear regulators in the sense that they are capable of stepping-up or stepping-down a voltage depending on the topology used (Czarkowski, 2001:211–212). There are various converters available that can be used in SMPS consisting of isolated and non-isolated converter topologies.

Some of the non-isolated topologies are:

- Buck converter
- Boost converter
- Buck-boost converter
- Ćuk converter
- SEPIC converter
- Zeta converter
- Charge-pump converter

Some of the isolated topologies are:

- Flyback converter
- Ring choke converter
- Half-forward converter
- Forward converter
- Weinberg converter
- Resonant forward converter
- Push-pull converter
- Half-bridge converter
- Full-bridge converter
- Resonant, zero voltage switched (ZVS) converter
- Isolated Ćuk converter

2.5.2 Switch-mode converter topologies

The number of switch-mode topologies available is numerous. This section covers some of the more basic switch-mode topologies that are commonly used in the CubeSat platform, i.e., the Buck-, Boost-, Buck-Boost- and Single-Ended Primary Inductance Converter (SEPIC). The use

of these converter topologies are mentioned in the designs described by Strain (2010*a*), Strain (2010*b*), GomSpace (2011), Day (2004) and Jordan (2006).

2.5.2.1 Buck converter

The Buck DC-DC converter produces an average output voltage that is lower than its input voltage. Figure 2.14 illustrates a Buck converter with a purely resistive load R_{LOAD}. The Buck converter consists of a DC input voltage source V_s, a controlled switch Q, diode D, filter inductor L and filter capacitor C (Czarkowski, 2001:213). The average output voltage can be calculated in terms of the switch duty-cycle as seen in Equation 2.5.1 and Equation 2.5.2 (Mohan *et al.*, 2003:164–166).

$$V_o = \frac{1}{T_s}\int_0^{T_s} v_0(t)\,\mathrm{d}t = \frac{1}{T_s}\left(\int_0^{t_{on}} V_s\,\mathrm{d}t + \int_{t_{on}}^{T_s} 0\,\mathrm{d}t\right) = \frac{t_{on}}{T_s}V_s = DV_s \tag{2.5.1}$$

$$\frac{V_o}{V_s} = D \tag{2.5.2}$$

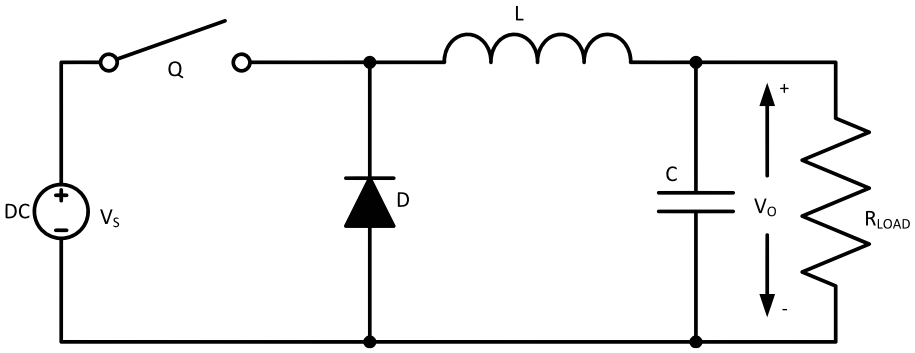

Figure 2.14: Buck converter circuit

The converter is referred to as being in continuous conduction mode (CCM) when the converter's inductor current is never zero for any period of time. In Figure 2.14 it can be seen that when switch Q is *on* the diode D is in reverse bias. When the switch Q is *off* the diode is in forward bias and conducts to support an uninterrupted current in the inductor. When the output current is low and the inductor's current drops to zero the converter is referred to as being in discontinuous conduction mode (DCM). CCM is preferred as the semiconductor switches and passive components are better utilised resulting in a greater efficiency from the converter (Czarkowski, 2001:213–214).

The value of the inductance that determines the boundary between CCM and DCM can be calculated with Equation 2.5.3, where f is the switching frequency of the switch and R_{load} is the load assuming that the load is purely resistive. For values of $L > L_b$ the converter operates in CCM, and for values of $L < L_b$ the converter operates in DCM (Czarkowski, 2001:214).

$$L_b = \frac{(1-D)R_{load}}{2f} \tag{2.5.3}$$

The current through the inductor i_L under CCM consists of a DC component, the output current, and a triangular AC component. The majority of the AC current component flows through the filter capacitor as the current i_c. This current, i_c, causes a small voltage ripple at the DC output voltage. To limit this output ripple voltage, V_r, to a certain magnitude, the filter capacitor capacitance must be larger than that determined through Equation 2.5.4. V_r is stated as a peak-peak voltage in Equation 2.5.4 (Czarkowski, 2001:214).

$$C_{min} = \frac{(1-D)V_o}{8V_r L f^2} \tag{2.5.4}$$

The switching waveforms associated with an ideal Buck converter can be seen in Figure 2.15 and are redrawn from Texas Instruments (2008*b*) and Czarkowski (2001:213).

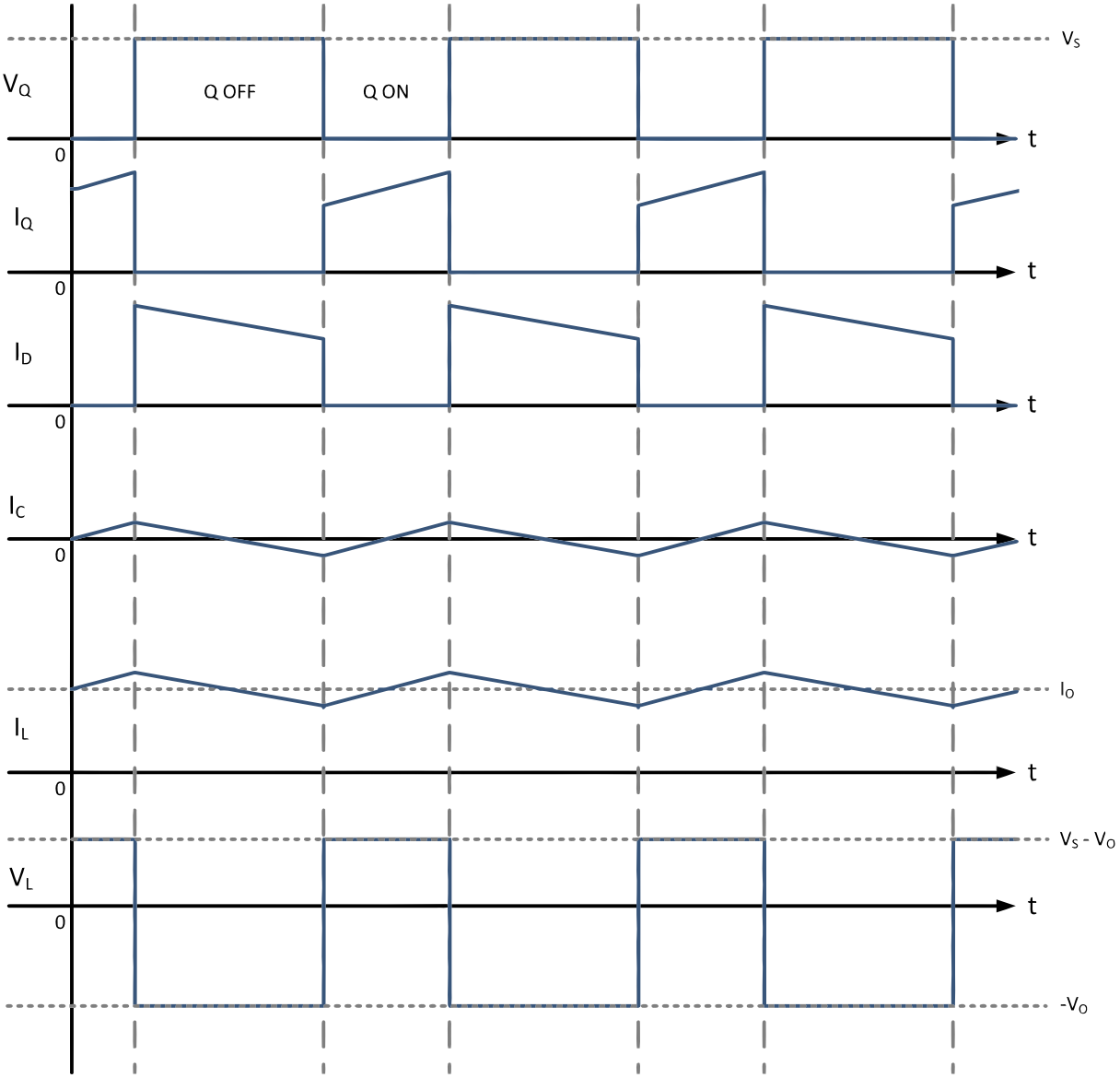

Figure 2.15: Buck switching waveforms redrawn from Texas Instruments (2008*b*) and Czarkowski (2001:213)

2.5.2.2 Boost converter

The Boost DC-DC converter produces an average output voltage that is greater than its input voltage. Figure 2.16 illustrates a Boost converter with a purely resistive load R_{LOAD}. The Boost converter consists of a DC input voltage source V_s, a controlled switch Q, diode D, inductor L and filter capacitor C (Czarkowski, 2001:215). When the switch is *on* the output stage is isolated due to the reverse bias of the diode, D, and the inductor, L, receives energy from the supply. During this time current is supplied to the load, R_{LOAD}, from the filter capacitor, C. When the switch is *off* the stored energy in the inductor as well as energy from the supply is supplied to the output stage (Mohan *et al.*, 2003:172).

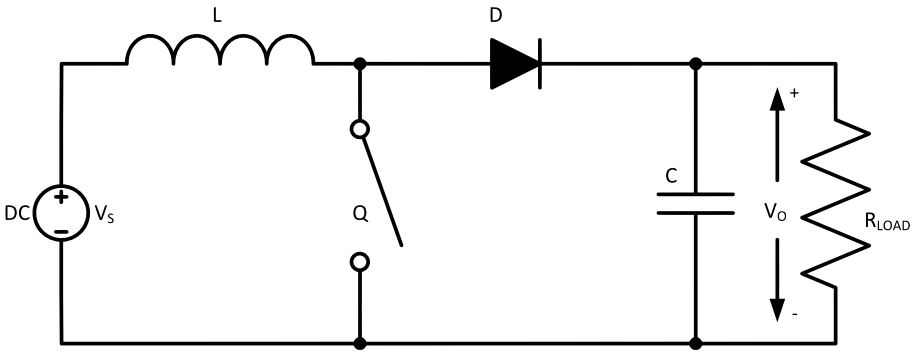

Figure 2.16: Boost converter circuit

Faraday's law can be used to determine Equation 2.5.5 relating to the Boost inductor. This leads to the DC voltage transfer function for the Boost converter as described by Equation 2.5.6 (Czarkowski, 2001:216).

$$V_s DT = (V_o - V_s)(1 - D)T \tag{2.5.5}$$

$$\frac{V_o}{V_s} = \frac{1}{1 - D} \tag{2.5.6}$$

The Boost converter operates in CCM under the condition that $L > L_b$. The Boost converter's inductor boundary value, L_b, can be determined by Equation 2.5.7. The operation of the Boost converter results in a discontinuity in the output current to the R-C output stage. This discontinuous current requires the output filter capacitor found in the Boost converter to be larger than that found in the Buck converter. This larger filter capacitor is required to supply current to the load when the switch is *on* and the diode is in reverse bias. The minimum value of capacitor that can be used to achieve a specific output ripple voltage, V_r, needs to be larger than that calculated using Equation 2.5.8 (Czarkowski, 2001:216).

$$L_b = \frac{(1 - D)^2 D R_{load}}{2f} \tag{2.5.7}$$

$$C_{min} = \frac{DV_o}{V_r R_{load} f} \tag{2.5.8}$$

The switching waveforms associated with an ideal Boost converter operating in CCM can be seen in Figure 2.17 and are redrawn from Texas Instruments (2008*b*) and Czarkowski (2001:216).

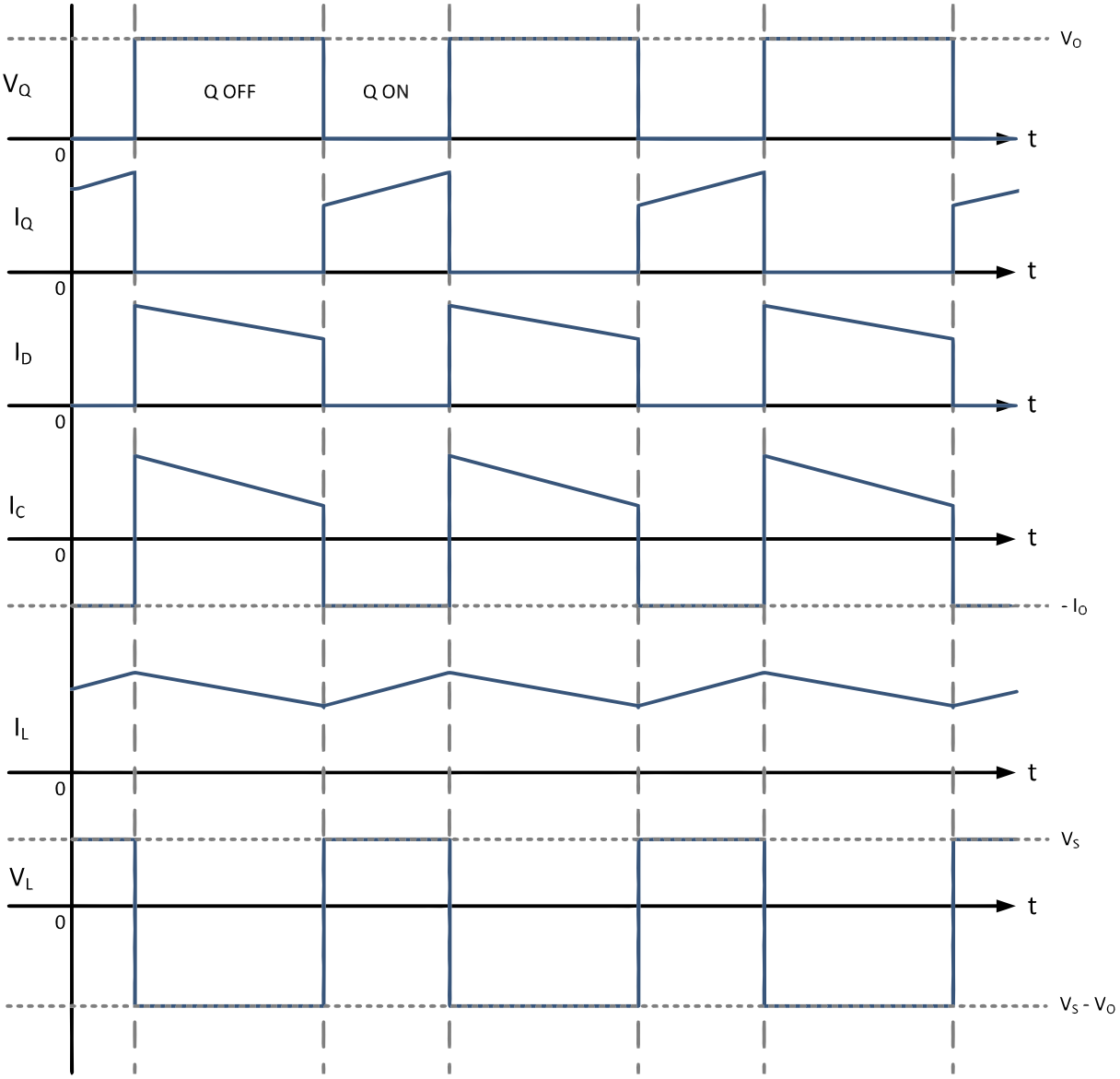

Figure 2.17: Boost switching waveforms redrawn from Texas Instruments (2008*b*) and Czarkowski (2001:216)

The operation of an ideal Boost converter operating in steady-state CCM is best explained through the observation of Figures 2.16 and 2.17. During the time interval in which the switch, Q, is *on* the diode, D, is essentially placed in parallel to the load in reverse bias, halting all flow of current through the diode. In this state the inductor, L, is placed in parallel to the input voltage source, V_s, causing the current through the inductor to increase at a rate of $\frac{di_L}{dt} = \frac{V_s}{L}$ (Maniktala, 2006:30). This current, I_L, is the only current flowing through the the switch, Q, during its *on-state*. The load, R_{LOAD}, during this time interval is supplied current from the output capacitor, C.

During the switch's *off-state* the energy stored in the inductor, L, along with some energy from the input voltage source, V_s is released through the diode to the output capacitor, C, and the

load, R_{LOAD} (Maniktala, 2006:55). In this state the diode, D, is forced into forward bias due to the sum of the potential formed across the inductor, L, and the input voltage source, V_s.

This results in energy being stored in the inductor, L, while the switch, Q, is *on* and energy being released by the inductor to the capacitor, C, and load, R_{LOAD} when the switch, Q, is *off*.

2.5.2.3 Buck-Boost converter

The main application of the Buck-Boost DC-DC converter is in regulated DC power supplies where a negative polarity output voltage is desired with respect to the input voltage (Mohan *et al.*, 2003:178). The output voltage in magnitude can be either greater than or less than the input voltage. Under steady-state operation the output-to-input conversion ratio, seen in Equation 2.5.9, is the product of the conversion ratio of the Buck converter and the conversion ratio of the Boost converter. Given that both the Buck converter and Boost converter are operated at the same duty-cycle. A Buck-Boost DC-DC converter can be seen in Figure 2.18 (Mohan *et al.*, 2003:178).

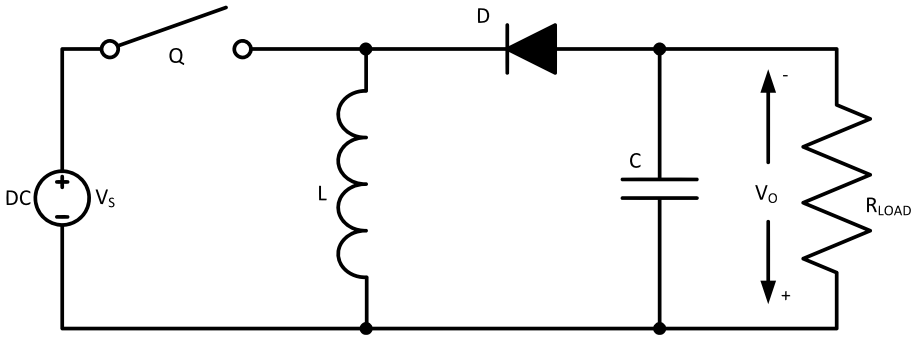

Figure 2.18: Buck-Boost converter circuit

$$\frac{V_o}{V_s} = D\,\frac{1}{1-D} \tag{2.5.9}$$

When the switch, Q, is *on* the inductor current rises and the diode is in reverse bias. When the switch, Q, is *off* the diode provides a path for the inductor current to flow. The value of the inductor that determines the mode of operation of the converter is determined through Equation 2.5.10. The structure of the output stage of the Buck-Boost converter is similar to that of the Boost converter and as such the filter capacitor can be calculated by using Equation 2.5.8 (Czarkowski, 2001:217).

$$L_b = \frac{(1-D)^2 R_{load}}{2f} \tag{2.5.10}$$

The switching waveforms associated with an ideal Buck-Boost converter operating in CCM can be seen in Figure 2.19 and are redrawn from Texas Instruments (2008*b*) and Czarkowski (2001:217). In Figure 2.19 V_o is defined as negative, and as such the switch, Q, must be able to handle a drain-source voltage of at least $V_s + |V_o|$.

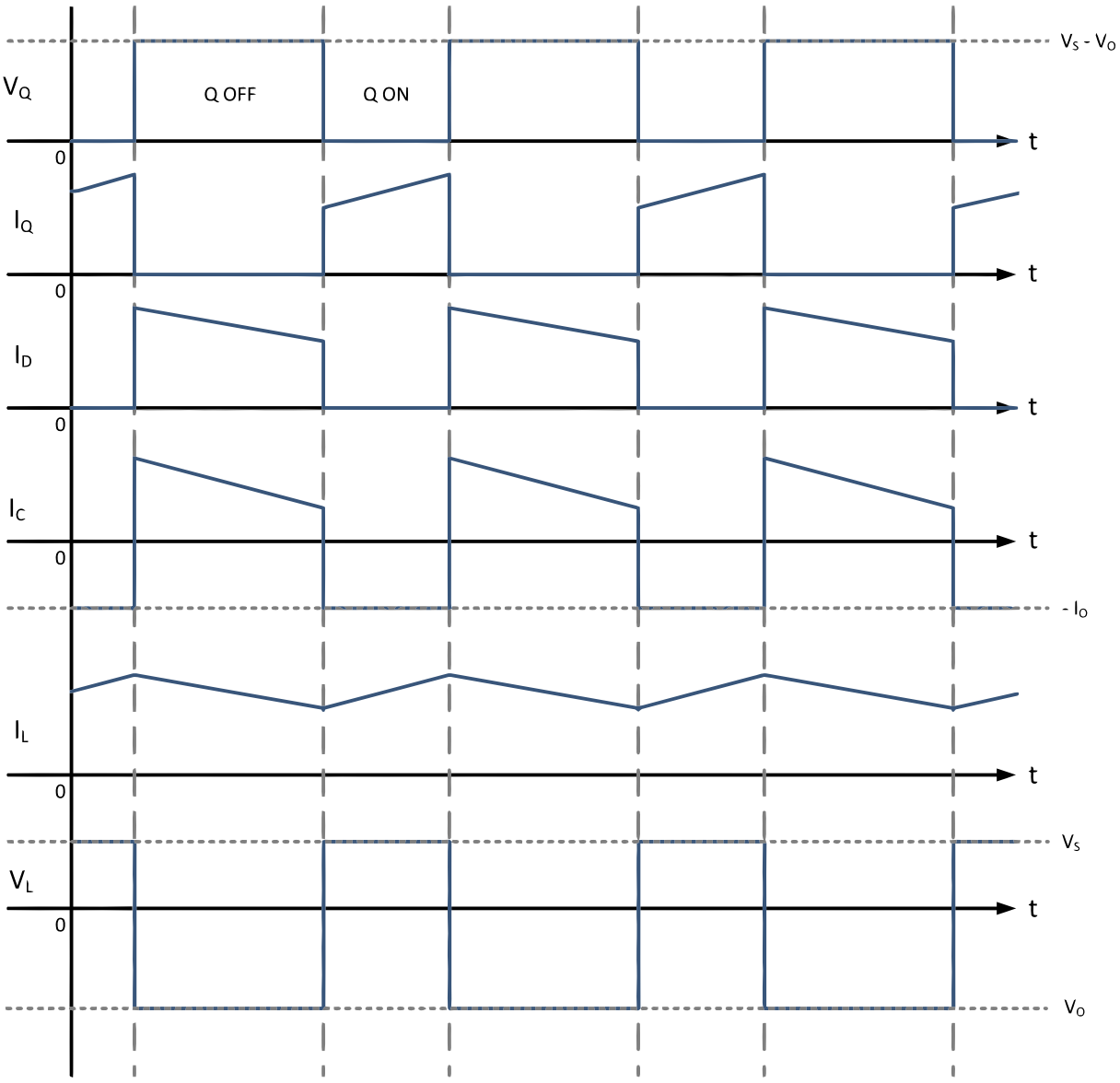

Figure 2.19: Buck-Boost switching waveforms redrawn from Texas Instruments (2008*b*) and Czarkowski (2001:217)

The operation of an ideal Buck-Boost converter operating in steady-state CCM can be explained through the observation of Figures 2.18 and 2.19. As with the Boost converter energy is stored in the inductor, L, and released to the output capacitor, C, and the load, R_{LOAD}. During the time interval in which the switch, Q, is *on* the diode, D, is reverse biased disconnecting the output capacitor, C, and the load, R_{LOAD} from the rest of the circuit. This state results in the inductor, L, being placed in parallel to the input voltage source, V_s, and the current in the inductor to increase at a rate of $\frac{di_L}{dt} = \frac{V_s}{L}$ (Maniktala, 2006:30). The load, R_{LOAD}, during this time receives current from the output capacitor, C.

During the switch's *off-state* the inductor, L, releases its stored energy into the output capacitor, C, and the load, R_{LOAD}, through the diode, D.

2.5.2.4 SEPIC converter

The SEPIC DC-DC converter is similar to the Ćuk but provides a positive output voltage and can operate with an input voltage less than or greater than the output voltage. Figure 2.20 illustrates this converter's topology. The SEPIC can be designed to operate with coupled inductors or non-coupled inductors. The coupled design allows the SEPIC converter to occupy a smaller footprint while allowing the use of half the inductance value required in a non-coupled design. Additionally the coupled SEPIC converter design allows the same inductor ripple current magnitude as the non-coupled inductor design while using half the inductance value (National Semiconductor, 2008; Texas Instruments, 2008*a*).

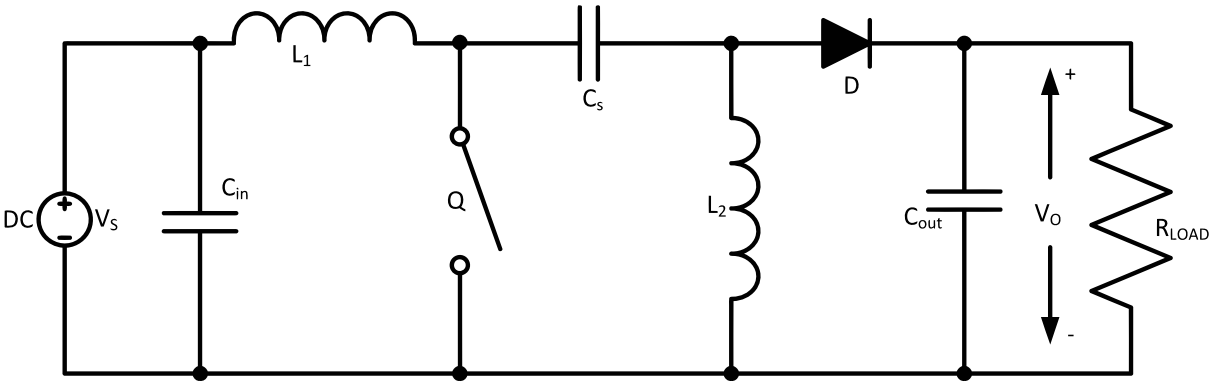

Figure 2.20: SEPIC converter circuit

The ideal DC voltage transfer function for the SEPIC converter is included as Equation 2.5.11 with the ideal switching waveforms associated with this converter under CCM shown in Figure 2.21 redrawn from Texas Instruments (2008*b*) and National Semiconductor (2008).

$$\frac{V_o}{V_s} = \frac{D}{1-D} \tag{2.5.11}$$

The operation of an ideal SEPIC converter operating in steady-state CCM can be described with the aid of Figures 2.20 and 2.21. It can be observed that the input to the SEPIC converter, consisting of the switch, Q, and inductor L_1, has similarities to that of a Boost converter. The SEPIC converter stores energy in inductors L_1 and L_2 and later passes this energy to the load, R_{LOAD}.

During the interval in which the switch, Q, is *on* the first inductor, L_1, is charged by the source, V_s, and the second inductor, L_2, is charged by the capacitor, C_s. No energy is supplied to the output capacitor, C_{out}, at this time. In this state C_s is in parallel to inductor, L_2, and the load, R_{LOAD}, is isolated from the the rest of the circuit by the diode, D. During this time the load, R_{LOAD}, is only supplied current from the output capacitor, C_{out} (Ridley, 2006:14).

When the switch, Q, is *off* the first inductor, L_1, charges the capacitor, C_s, and also provides current to the load. The second inductor, L_2, is also connected to the load at this time supplying some of the load current (Ridley, 2006:14).

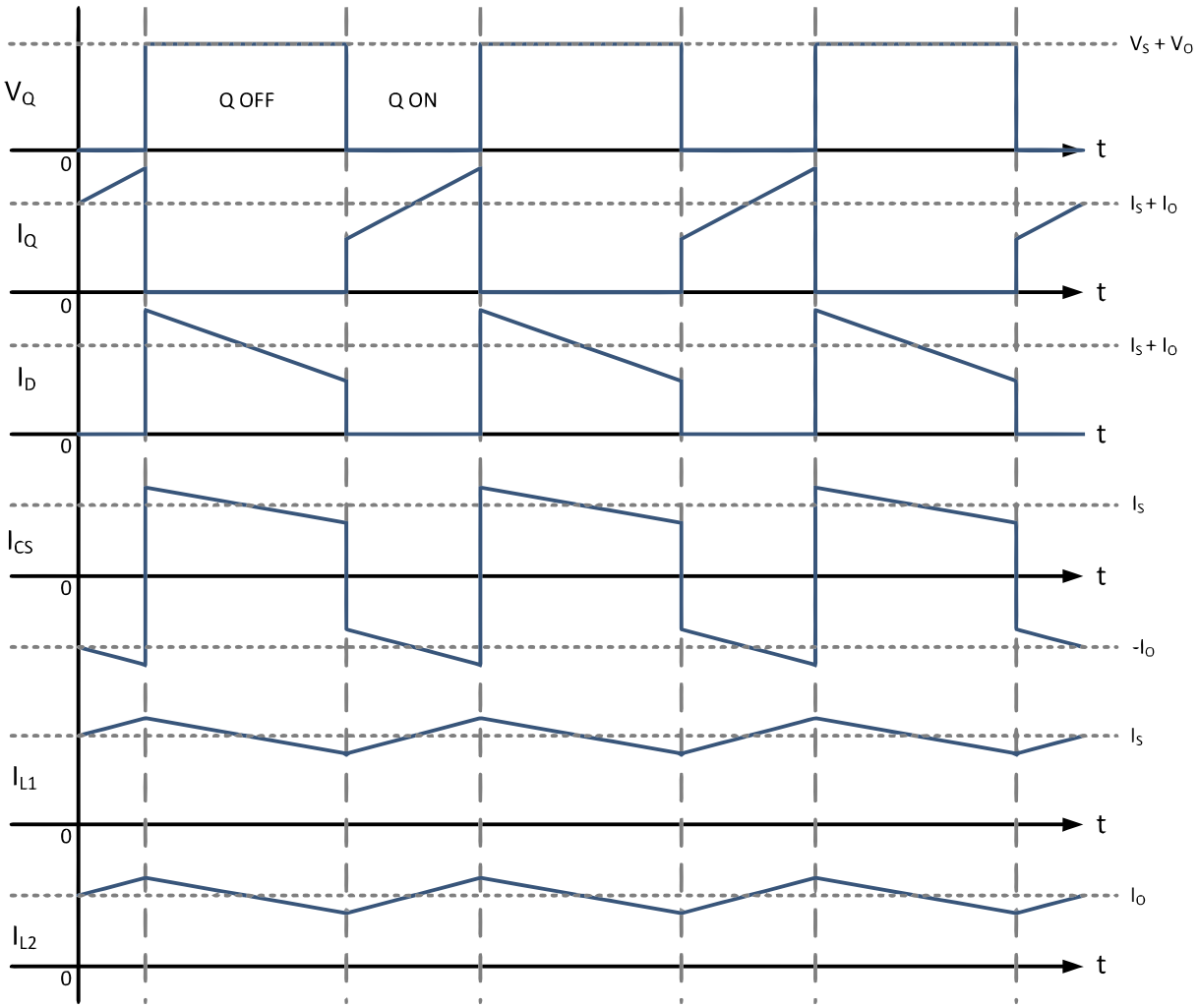

Figure 2.21: SEPIC switching waveforms redrawn from Texas Instruments (2008*b*) and National Semiconductor (2008)

The SEPIC DC-DC converter brings with it the ability to isolate the input and output voltage upon shut down. This isolation is due to the SEPIC DC-DC converter's coupling capacitor and this topologies operation as described by National Semiconductor (2008) and Texas Instruments (2008*a*). The coupling capacitor, C_s, blocks the direct DC path between the input and the output of the SEPIC DC-DC converter.

2.5.3 Power losses

The higher the switching frequency of the DC-DC converter the larger the switching losses of the converter, this is due to the transition of the switch or switches from an *on-state* to an *off-state* and vice versa. The higher operating frequency requires a higher number of switch state changes per second, increasing the number of transitions per second (Maniktala, 2006:205).

The motivation for using switching in modern power converters is "by switching the transistor, either the voltage across the transistor is close to zero, or the current through it is close to zero, and therefore the dissipation cross-product "$V \times I$" is also almost zero" as stated by Maniktala

(2006:213), this however does not hold true during the switching transitions. Unlike switching losses, the conduction losses of the switch or switches are independent of the frequency, however the losses are dependant on the duty-cycle at which the switches are operated (Maniktala, 2006:213).

2.5.4 Control of switch-mode DC-DC converters

Switch-mode DC-DC converters utilise a switch or switches to 'convert' a DC voltage to another DC voltage. The average output voltage of a switch-mode converter is controlled by the *on* and *off* duration of the switch or switches. The ratio of the *on* time and the sum of the *on* and *off* time is typically referred to as the duty ratio or duty-cycle, D. One of the more commonly used methods of varying the duty-cycle is through the use of pulse width modulation (PWM). Typically PWM is generated by comparing a signal-level control voltage, $v_{control}$, with a repetitive waveform, v_{st}, as can be seen in Figure 2.22 redrawn from Mohan *et al.* (2003:163). The control voltage signal is generated by amplifying the difference/error between the actual output voltage and the desired output voltage (Mohan *et al.*, 2003:162).

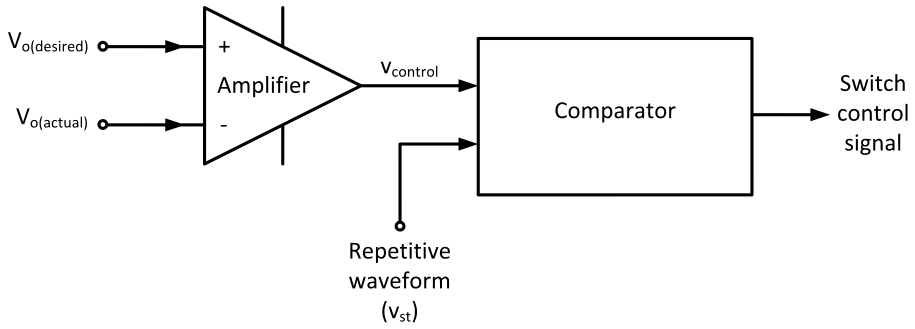

Figure 2.22: Pulse width modulator block diagram redrawn from Mohan *et al.* (2003:162)

Typically the frequency of the PWM is kept constant and is chosen to be in the order of a few kilohertz to a few hundred kilohertz. This frequency is established by the repetitive waveform, v_{st}, which is usually a ramping triangular or sawtooth waveform. The amplified error signal varies very slowly with time relative to the switching frequency. When this error signal is greater than the repetitive waveform the switch control signal goes high, causing the switch to turn *on* (Mohan *et al.*, 2003:163). The duty-cycle can be expressed in terms of $v_{control}$ and the peak of the carrier $\widehat{V}_{st}$ as can be seen in Equation 2.5.12.

$$D = \frac{t_{on}}{T_s} = \frac{v_{control}}{\widehat{V}_{st}} \tag{2.5.12}$$

Switch-mode DC-DC converter can operate in two modes of operation, namely continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM). These modes have significantly different characteristics. A converter may be expected to operate in both these modes and as such the control should take this into consideration (Mohan *et al.*, 2003:163).

2.5.5 Feedback and control loops

It is desirable for most DC-DC converters to have a tightly regulated output rail voltage. This regulated output rail voltage should maintain its integrity during input voltage and load current variations. If a constant duty-cycle converter were to be used, any variation in the input voltage of the converter would result in a variation occurring at the output voltage due to a constant duty-cycle and varying input voltage. Variations in output current would also result in variations of output voltage as losses in the switch and other components would vary with the current variation (Zhang, 2010).

Through the use of negative feedback the duty-cycle of the switches associated with DC-DC converters can be automatically adjusted as necessary to obtain a desired output voltage with a high level of accuracy regardless of variations in the output current and input voltage (Erickson & Maksimović, 2004:331).

The two most commonly used closed loop feedback control methods for PWM DC-DC converters rely on voltage-mode control and current-mode control Czarkowski (2001:221). Block diagrams illustrating these control methods can be seen in Figure 2.23 and Figure 2.24 respectively and are redrawn from Czarkowski (2001:221).

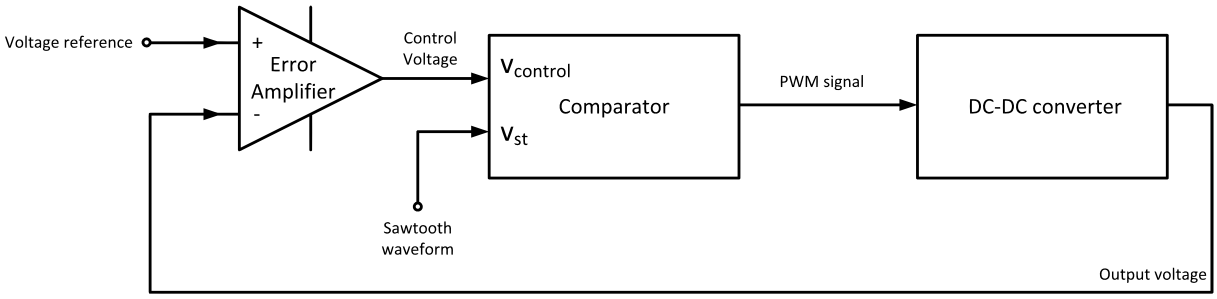

Figure 2.23: Voltage-mode DC-DC converter control redrawn from Czarkowski (2001:221)

A major advantage to voltage-mode control is it is simple to implement in hardware. The error amplifier in a voltage-mode control scheme produces a difference voltage, the control voltage ($v_{control}$), from the output voltage and a reference voltage. This control voltage is then compared to a constant amplitude sawtooth or triangular waveform, v_{st}. This produces the PWM used in controlling the switches of the DC-DC converter. The duty-cycle of the PWM is directly dependant on the control voltage. Voltage-mode regulation can provide good load regulation, however line regulation is delayed as variations in the input voltage must first be observed at the output voltage before they can be corrected by this form of control (Czarkowski, 2001:221).

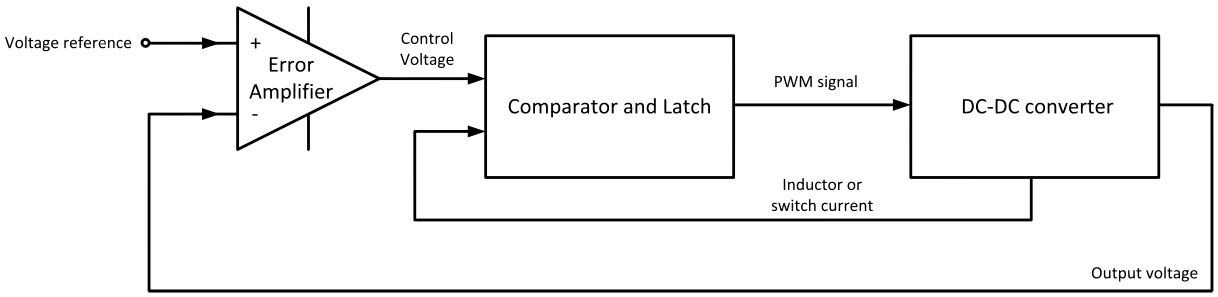

Figure 2.24: Current-mode DC-DC converter control redrawn from Czarkowski (2001:221)

In current-mode control an additional inner control loop feeds back an inductor current signal. This current signal is converted to an analogue voltage and is compared to the control voltage as a replacement to the sawtooth or triangular waveform. Replacing the sawtooth waveform used in voltage-mode control with a current signal causes the converter to take on some characteristics of a current source. These characteristics alter the dynamic behaviour of the converter (Czarkowski, 2001:221).

Figure 2.25 shows a practical application of voltage-mode control of a DC-DC converter where a fraction, α, of the output voltage, V_{out}, is compared against the reference voltage V_{ref}. This closes a loop from the output of the converter to the input, hence the term *feedback loop*. This feedback loop causes the controller to try to maintain equality between α and the reference, giving rise to Equation 2.5.13. The output signal feeds back to the inverting input of the operational amplifier. The frequency response of the error amplifier is affected by the compensation network formed around Z_f, the error amplifier feedback impedance, and R_{upper} seen in Figure 2.25. The purpose of the compensation network is to adjust the frequency response of the converter such that the converter is stable once operated in a closed loop (Basso, 2008:241).

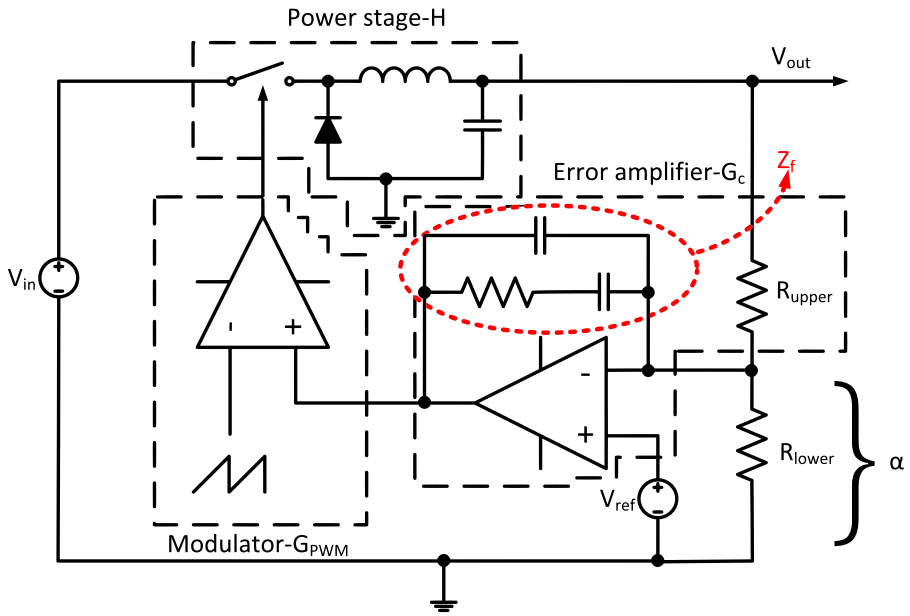

Figure 2.25: Switch-mode power converter operating in closed loop mode redrawn from Basso (2008:242)

$$V_{out} = \frac{V_{ref}}{\alpha} \tag{2.5.13}$$

A simplified representation of the converter seen in Figure 2.25 is shown in Figure 2.26 with the loop gain of the system represented by Equation 2.5.14, where $G(s) = G_c(s)G_{PWM}$.

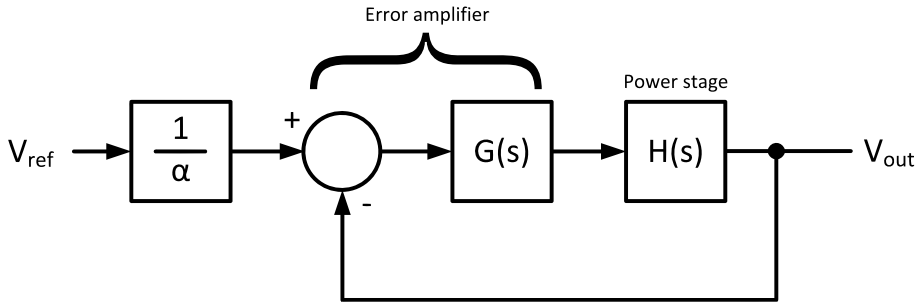

Figure 2.26: Simplified representation of the switch-mode power converter operating in closed loop mode

$$T(s) = H(s)G_c(s)G_{PWM} \tag{2.5.14}$$

2.5.5.1 Switch-mode power supply stability criteria

The feedback system takes a portion of the output variable and compares it to a stable reference voltage, this then further amplifies the error between these signals generating the error control

signal used in performing the corrective action required by the converter as mentioned in Section 2.5.5. This control action opposes the variation observed at the output of the converter by means of *negative feedback*. As the frequency of the variation increases, the converter's output stage $H(s)$ introduces delays and decreases the gain of the converter. A case might arise where the delay is significant enough as to allow a past control signal to propagate through the system and arrive in phase with the output signal at the output, in this case both signals reinforcing each other. This reinforcement forms a *positive feedback* oscillator which is not the intent of a switch-mode power supply (Basso, 2008:247).

The general rule for determining if a system is stable is "The closed loop phase shall never exceed 330° of lag whenever the gain of the closed loop system is greater than 1 (or 0 dB)" as stated by Brown (2001:205). A total phase lag of 315° is typically used as a minimum, while any closer to 360° would constitute a *metastable* system (Brown, 2001:205).

The phase margin (PM) is the safety margin of the closed loop phase at a gain of 0 dB. Brown (2001:205) mentioned that the phase should never exceed 330° of lag where the closed loop system gain is greater than 1. This lag would consist of the phase shift brought on by the power stage of the converter and the compensation circuit. If the phase of the closed loop system were to be 330° at the 0 dB crossover point, this would constitute a PM of 30°. Clarifying the statement by Brown (2001:205) a typical total phase lag of 315°, typically a PM of 45°, would be used. However, Basso (2008:247) highly recommends designs to utilise 70° to 80° phase margins as they offer good stability while maintaining a fast non-ringing response. A practical method of measuring the phase margin of a converter is illustrated by LeCroy (nd). According to Basso (2008:247), some textbooks refer to the PM from -180° to the phase at the 0 dB cross-over point. This can be seen in Warwick (1996:151) where the phase margin is determined through observing the required phase lag from the input to the output of the plant, referred to in the context of a switch-mode converter as the power stage. In such a case the PM is derived from the phase difference between the input and output of the system at a frequency where the loop has unity gain (Warwick, 1996:151). Basso (2008:247) mentions that both these methods lead to the same interpretation. This is due to the overall goal of designing a stable system and reducing the possibility of oscillation due to positive feedback. The open loop phase margin needs to be determined in order to decide whether compensation is required, and if so what type of compensation is required. Once the compensation is designed the closed loop phase margin should be verified in order to determine whether the closed loop system is stable. This can be seen in work by Zhihao & Xiaobo (2009) which shows phase margins for both an uncompensated and compensated system. Zero PM at above or below the 0 dB point offers *conditional stability*. The stability is conditional as an increase or decrease in the gain of the system while maintaining the same phase plot could cause the phase margin to drop to zero at the gain crossover point. The gain margin (GM) is the gain required, through increase or decrease, for the system to become unstable. If the gain were to increase by the gain margin the system would become unstable (Basso, 2008:247–248).

The intent of a power supply is not to create an oscillator. In order to overcome this, compensation is used. Compensation design consists of shaping the correction circuit $G_c(s)$, consisting of the compensation network and the error amplifier, such that (Brown, 2001:205):

- There exists sufficient phase difference between the error and output signal at the 0 dB crossover point.
- $G_c(s)$ offers a high gain value in the DC portion of the magnitude plot, this reduces static error, reduces the output impedance and improves input line rejection.

2.5.5.2 Selecting a crossover frequency and phase margin

Many factors govern the selection of a crossover frequency. Typically where a resonant LC network in the power stage is not present, a crossover frequency of 10% to 20% of the switching frequency can be chosen. Selecting a crossover frequency that is too high can result in noise pickup and lead to instability of a converter even if the design shows adequite PM and GM (Basso, 2008:249–250).

The PM of a closed loop converter governs the transient response of the converter. If the PM is too small, high output voltage ringing can occur due to a high response rate. Inversely if the PM is too large the response and recovery of the output voltage of the converter is slowed down Basso (2008:248–249).

There is a relationship between the PM of a second-order closed loop system and the quality coefficient, Q, of its transfer function. A second-order closed loop system with a Q of 0.5 leads to a critically-damped converter with a PM of 76°. A critically damped converter combines a good response speed and lack of overshoot. Due to this, Basso (2008:248–249) recommends a PM of 70° be attempted in designs with a worst case of 45°.

As previously mentioned the PM of a closed loop converter governs the response of the converter, thus the recovery time from an output voltage undershoot is dependant on the phase margin at the crossover frequency. Additional factors to the output undershoot voltage level have to be considered when a crossover frequency is selected for a closed loop DC-DC converter. Such factors could be the peaking of LC networks located in the power stage of converters which is due to resonance. Selecting a crossover frequency too close to this resonant frequency, f_0, could bring about stability issues when operating converters with voltage-mode control. These stability issues are due to the phase lag brought on at this location. In such a case a crossover frequency, f_c, should be selected for at least three times the resonant frequency, f_0 according to Basso (2008:250).

The specific output voltage undershoot level of a closed loop DC-DC converter can be determined through the observation of the converter's output impedance. The approximate output impedance of a closed loop DC-DC converter can be determined through the observation of its output capacitor impedance at the crossover frequency. This allows the approximate output

voltage undershoot level, V_p, during an output transient step, ΔI_{out}, to be determined through the use of Equation 2.5.15 (Basso, 2008:249).

$$V_p \approx \frac{\Delta I_{out}}{C_{out} 2\pi f_c} \tag{2.5.15}$$

Where:

C_{out} is the output capacitor in F
f_c is the crossover frequency in Hz
ΔI_{out} is the output transient step in A
V_p is the output voltage undershoot level in V

Equation 2.5.15 only holds true when the output capacitor's ESR is less than the reactance of C_{out} at the crossover frequency f_c. This condition is expressed by Equation 2.5.16 (Basso, 2008:249–250).

$$ESR_{C_{out}} \leq \frac{1}{2\pi f_c C_{out}} \tag{2.5.16}$$

2.5.5.3 Compensation networks

Improving stability of a switch-mode converter requires shaping the compensation circuit, $G_c(s)$, such as to provide a closed loop system with sufficient phase margin at the selected crossover point as well as a high DC gain. There are several compensation circuits that can be used in improving the stability of a switch-mode converter. These compensation circuits work by inserting poles and zeros into the closed loop response of the converter to increase or decrease the gain and phase of the closed loop response. Usually a phase boost is required at the crossover frequency in order to obtain a usable phase margin (Basso, 2008:250).

Type 1, type 2, type 2a, type 2b and type 3 compensation networks are discussed in subsections 2.5.5.4 to 2.5.5.8. The compensation networks are illustrated in Figures 2.27 to 2.35 using an ideal operational amplifier (Op Amp) with an open-loop gain of 60 dB. Figures 2.27 to 2.35 were used from Basso (2008:255–261) and re-simulated with the use of LTSpice® from Linear Technology.

2.5.5.4 Type 1 compensation

Type 1 compensation, seen in Figure 2.27, is essentially an active integrator circuit with the transfer function seen as Equation 2.5.17. The Bode plot for this type of compensation can be seen in Figure 2.28 (Basso, 2008:255–256).

$$G_c(s) = \frac{1}{sR_1C_1} \tag{2.5.17}$$

The gain of type 1 compensation rolls off at a rate of -20 dB/decade while the phase plot stays flat at 90° due to the −180° phase shift brought on by the inverting configuration of the Op Amp and an additional −90° brought on by the pole at the origin. This equates to a phase shift of −270° or +90° as seen in Figure 2.28 (Basso, 2008:255–256).

In DC analysis this type of amplifier configuration fixes the gain to the open loop gain of the amplifier, as the capacitor C_1 is seen as an open circuit, fixing the gain to 60 dB. Looking at Figure 2.27 in terms of AC, as the frequency rises the impedance of C_1 decreases causing the closed loop gain of the amplifier to drop at a rate of -20 dB/decade. R_{lower} does not play any role in the AC response of the amplifier configuration as the inverting pin can be treated as a virtual ground. However, R_1 and R_{lower} are both needed in selecting the required output voltage of a switch-mode converter (Basso, 2008:256).

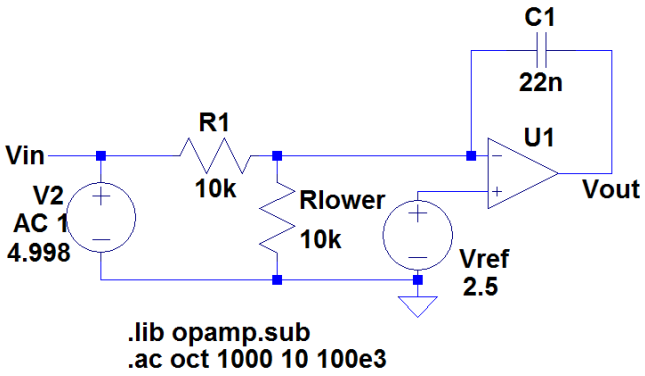

Figure 2.27: Type 1 compensation amplifier

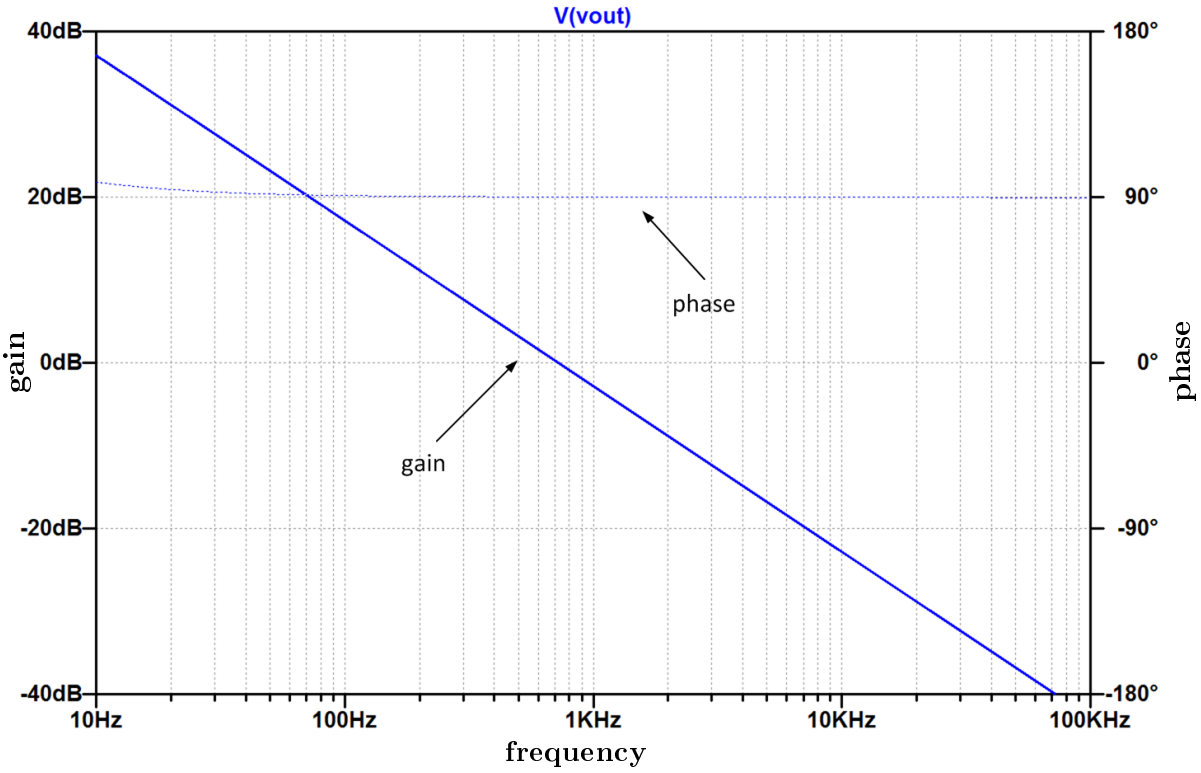

Figure 2.28: Type 1 compensation bode plot

2.5.5.5 Type 2 compensation

The type 2 compensation amplifier's response consists of an integrator and a zero-pole pair and can be used in increasing the phase margin of a closed loop system at a desired crossover frequency. A type 2 compensation amplifier can be seen in Figure 2.29 with the related bode plot in Figure 2.30. The transfer function of this type of compensation amplifier is included as Equation 2.5.18 (Basso, 2008:257).

$$G_c(s) = \frac{1 + sR_2C_1}{sR_1(C_1 + C_2)\left(1 + sR_2\frac{C_1C_2}{C_1+C_2}\right)} \tag{2.5.18}$$

Using Equation 2.5.18 the poles and zeros shown in Equation 2.5.19 to Equation 2.5.21 can be determined.

$$\omega_z = \frac{1}{R_2C_1} \tag{2.5.19}$$

$$\omega_{p1} = \frac{1}{R_1(C_1 + C_2)} \tag{2.5.20}$$

$$\omega_{p2} = \frac{1}{R_2\left(\frac{C_1C_2}{C_1+C_2}\right)} \tag{2.5.21}$$

If $C_2 << C_1$ Equation 2.5.21 can be simplified to Equation 2.5.22.

$$\omega_{p2} = \frac{1}{R_2 C_2} \tag{2.5.22}$$

The phase boost, an increase in phase, occurs between the zero-pole pair (ω_z and ω_{p2}). The distance between this zero and pole determines the amount of phase boost this type of compensation can deliver. The peak of this boost is located at the geometric mean value between this zero and pole (Basso, 2008:257).

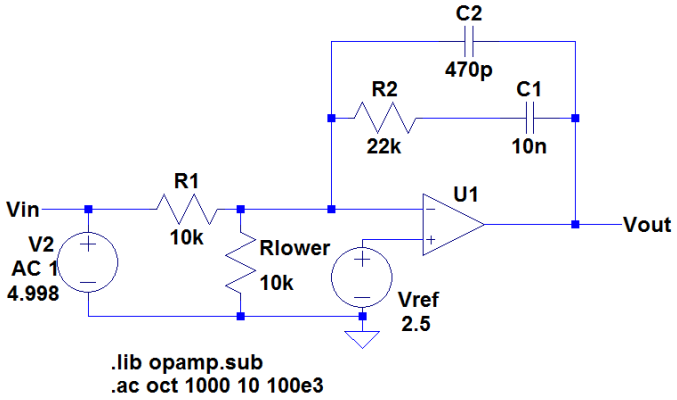

Figure 2.29: Type 2 compensation amplifier

Similarly to type 1 compensation this type of amplifier configuration produces an open loop gain when analysed in terms of DC. Equation 2.5.20 defines the pole at the origin. This pole causes the gain to roll off at a slope of -1 or at a rate of -20 dB/decade from the origin as the frequency is increased. The zero defined by Equation 2.5.19 causes the phase to increase and the slope to increase from -20 dB/decade to 0 dB/decade. The effect of the zero can be seen in Figure 2.30 at approximately 1 kHz. This zero continues to act as the frequency is increased until the final pole begins to affect the gain and phase of the system. The final pole effectively counteracts the previous zero bringing the phase back down to 90° and the gain to a slope of -20 dB/decade. The effect of this final pole can be seen after 10 kHz in Figure 2.30 (Basso, 2008:257–258).

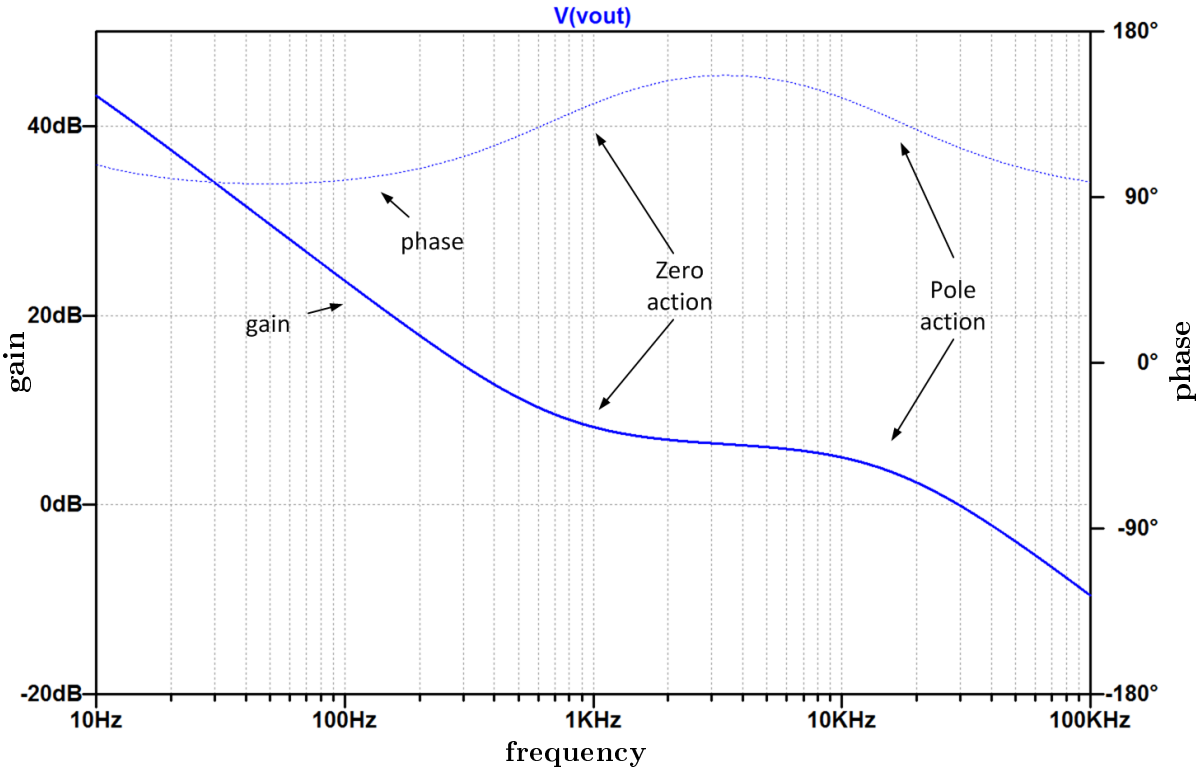

Figure 2.30: Type 2 compensation bode plot

2.5.5.6 Type 2a compensation

The type 2a compensation amplifier is similar to the type 2 with the exception of the removal of C_2. This type of compensation eliminates the high-frequency pole associated with the type 2 compensator. The transfer function of this type of compensation is included as Equation 2.5.23 with the zero and pole described by Equation 2.5.24 and Equation 2.5.25 respectively (Basso, 2008:258–259).

$$G_c(s) = \frac{1 + sR_2C_1}{sR_1C_1} \tag{2.5.23}$$

$$\omega_z = \frac{1}{R_2C_1} \tag{2.5.24}$$

$$\omega_p = \frac{1}{R_1C_1} \tag{2.5.25}$$

As with the type 1 and 2 compensator analysing the DC response of this amplifier configuration results in the open loop gain of the Op Amp. This type of compensation is merely an adaptation of type 2 compensation with the removal of C_2. In removing C_2 the high-frequency pole is removed resulting in a system only exhibiting a pole at the origin and a zero. The pole at the origin causes a slope of -20 dB/decade between the origin and the zero with a phase shift of 90°. As the frequency is increased the zero begins to affect the response of the amplifier, causing the

slope of the gain to increase to 0 dB/decade and a phase boost by 90° resulting in a phase of 180° (Basso, 2008:258–259).

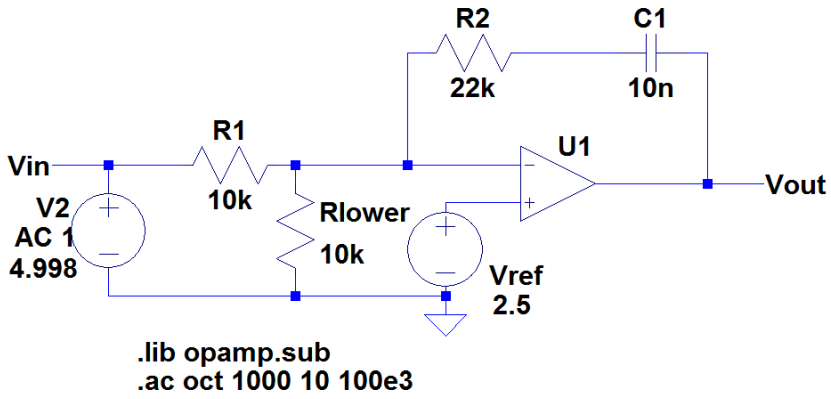

Figure 2.31: Type 2a compensation amplifier

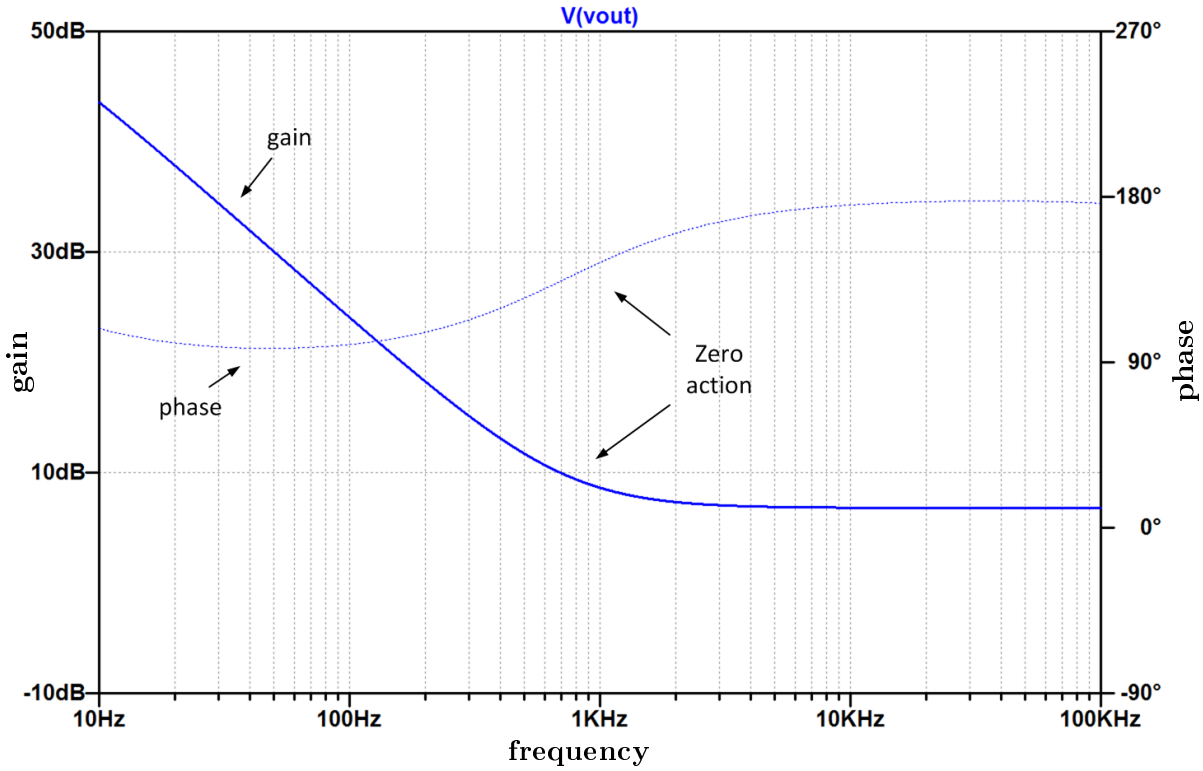

Figure 2.32: Type 2a compensation bode plot

2.5.5.7 Type 2b compensation

The type 2b compensation amplifier, seen in Figure 2.33, offers a flat gain given by R_1 and R_2 until the pole introduced by C_1 comes into effect as can be seen in the bode plot in Figure 2.34. The transfer function of this compensation amplifier is given by Equation 2.5.26 and the location of the pole is defined by Equation 2.5.27 (Basso, 2008:259–260).

$$G_c(s) = \frac{R_2}{R_1}\frac{1}{1+sR_2C_1} \tag{2.5.26}$$

$$\omega_p = \frac{1}{R_2C_1} \tag{2.5.27}$$

The DC gain of this amplifier configuration is governed by R_1 and R_2 and remains relatively flat in the frequency domain from the origin until the pole begins to affect the amplifier's response. The pole causes the gain to decrease at a slope of -20 dB/decade and the phase to decrease by 0° from 180° (Basso, 2008:259–260).

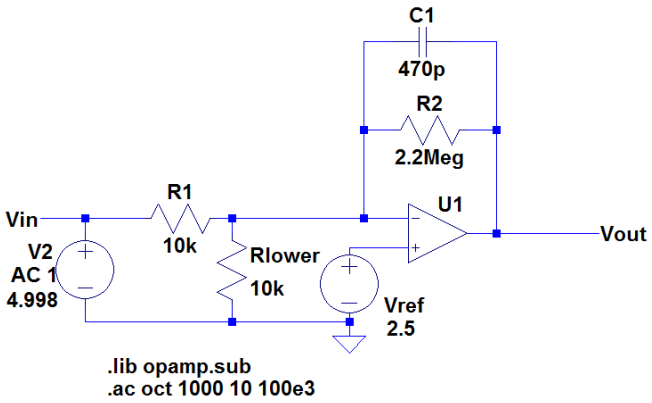

Figure 2.33: Type 2b compensation amplifier

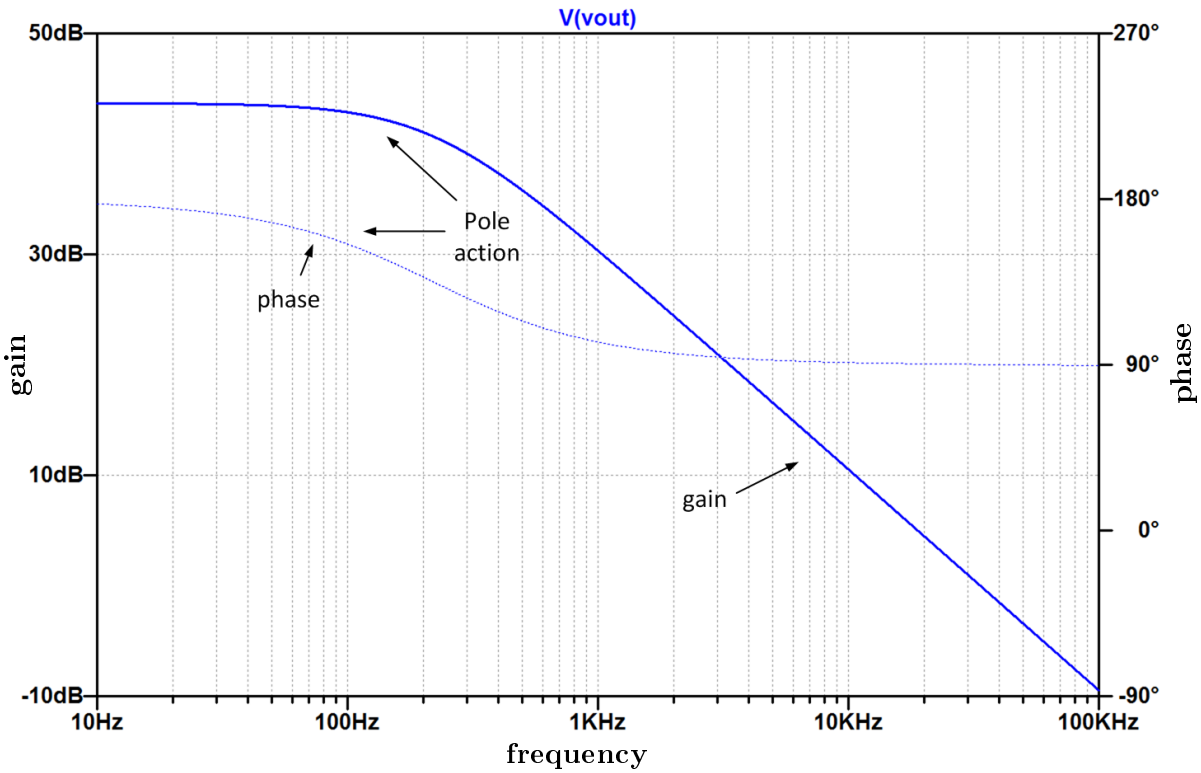

Figure 2.34: Type 2b compensation bode plot

2.5.5.8 Type 3 compensation

The type 3 compensation amplifier configuration is used where a large phase boost is required, such is usually the case with switch-mode converters operating in constant conduction mode (CCM) and voltage-mode operation having a second-order response. The type 3 compensation amplifier's response consists of a pole at the origin and two coincident zero-pole pairs. This amplifier configuration can be seen in Figure 2.35 with the bode plot in Figure 2.36. The transfer function for this type of compensation is given by Equation 2.5.28 and the poles and zeros are described in Equation 2.5.29 to Equation 2.5.33 assuming $C_2 << C_1$ and $R_3 << R_1$ (Basso, 2008:261–262).

$$G_c(s) = \frac{sR_2C_1 + 1}{sR_1(C_1 + C_2)\left(1 + sR_2\frac{C_1C_2}{C_1+C_2}\right)} \frac{sC_3(R_1 + R_3) + 1}{(sR_3C_3 + 1)} \tag{2.5.28}$$

$$\omega_{z1} = \frac{1}{R_2C_1} \tag{2.5.29}$$

$$\omega_{z2} = \frac{1}{R_1C_3} \tag{2.5.30}$$

$$\omega_{p0} = \frac{1}{R_1C_1} \tag{2.5.31}$$

$$\omega_{p1} = \frac{1}{R_3C_3} \tag{2.5.32}$$

$$\omega_{p2} = \frac{1}{R_2C_2} \tag{2.5.33}$$

As with the type 1, 2 and 2a compensators the DC gain of this amplifier configuration is that of the open loop gain of the Op Amp. In terms of AC response this amplifier configuration has a -20 dB/decade slope from the origin towards the double zero. As the double zero begins to affect the response of the amplifier with an increase in frequency the slope of the gain increases two fold resulting in a slope of +20 dB/decade. This double zero pair also introduces a phase boost. As the frequency is increased the double pole begins to affect the amplifier's response causing the slope of the gain to return to -20 dB/decade and the phase to drop back to 90° (Basso, 2008:261-262).

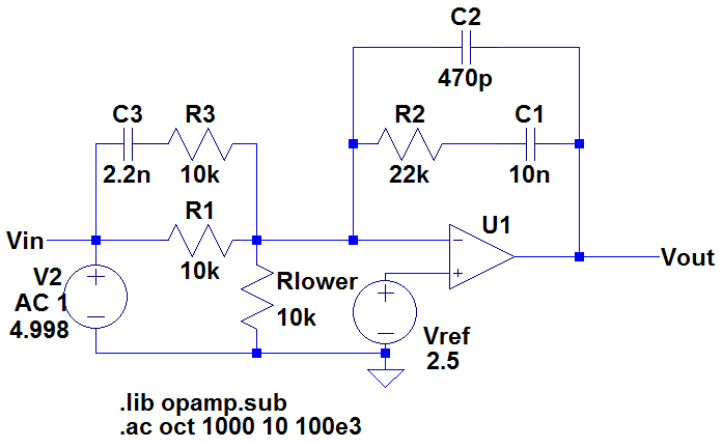

Figure 2.35: Type 3 compensation amplifier

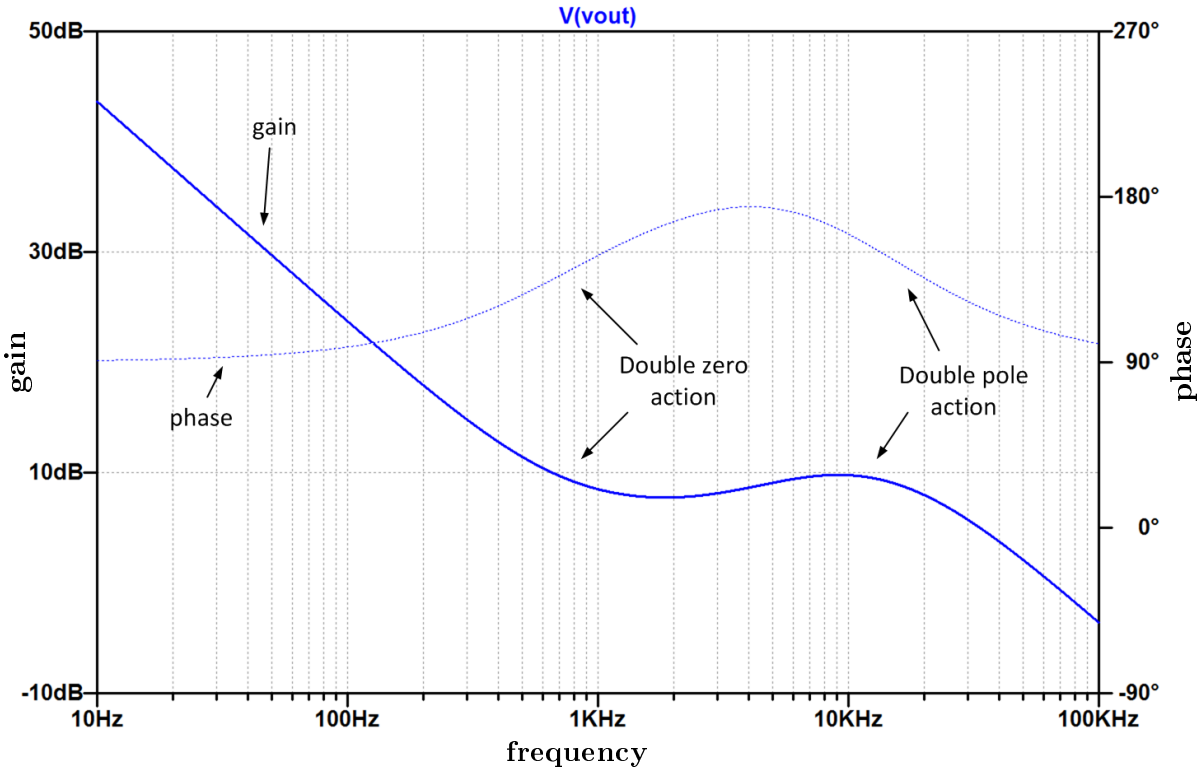

Figure 2.36: Type 3 compensation amplifier bode plot

As can be seen by this section there is a wide variety of compensation amplifier designs that can be employed to improve the response and stability of a SMPS. Table 2.2 is a short summary of the various compensation amplifier configurations including a guide to selecting the correct amplifier type for a variety of SMPS designs as described by Basso (2008:262).

Table 2.2: Selecting the correct amplifier type as described by Basso (2008:262)

Compensation type	Characteristics	Typical use
Type 1	• No phase boost. • Brings about the largest overshoot in the presence of a sudden load change.	In applications where the power stage phase shift is small, such as where a gain roll off far from the resonant frequency of a second-order filter is desired.
Type 2	• Phase boost between a zero-pole pair.	This is the most widely used compensation type, and works with power stages that lag down to $-90°$ and where the phase boost brought on by the output capacitor's ESR must be cancelled.
Type 2a	• Phase boost due to single zero. • Majority of the phase boost is in the high-frequency domain.	Used in similar applications to the type 2 compensator but when the output capacitor's ESR can be neglected. Such a case could be where the zero created by the ESR of the output capacitor is relegated to the high-frequency domain.
Type 2b	• The DC gain is flat until the high-frequency pole starts to act. • Majority of the phase boost is in the low-frequency domain.	This type of amplifier includes a proportionality term that can reduce the under- or overshoot conditions and can improve transient response. This amplifier configuration has a reduced DC gain compared to the other type 2 amplifiers producing a larger static error.
Type 3	• Introduces a double zero and double pole producing a significant phase boost.	This amplifier configuration is used where the phase shift brought by the power stage of a converter can reach $-180°$.

2.5.6 Electromagnetic compatibility

Electromagnetic compatibility (EMC) is defined as "the ability of equipment or systems to share the same electromagnetic environment" as stated by Maniktala (2006:334). Compatible devices should operate acceptably without inducing or experiencing interference from other devices. Devices emitting Electromagnetic Interference (EMI) are classified as culprits, while devices susceptible to EMI are classified as victims. The EMI/EMC "Tree" depicting the various aspects

of EMC can be seen in Figure 2.37.

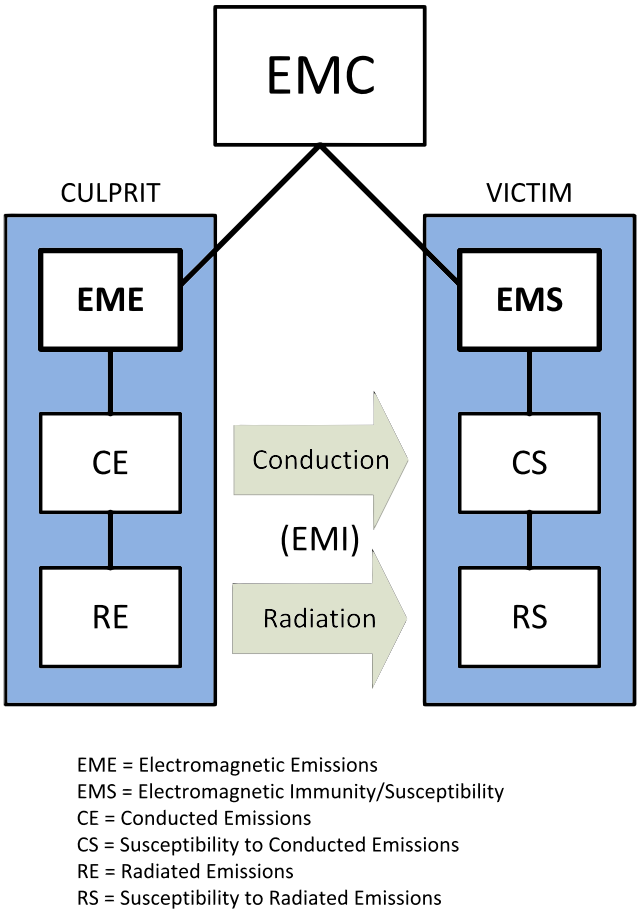

Figure 2.37: The EMI/EMC "Tree" redrawn from Maniktala (2006:326)

When several electronic or electrical systems are packed in very close proximity such as on board aircraft, ships, satellites and other vehicles EMC could be problematic. The location of these electronic or electrical systems may be such that susceptible systems may be in close proximity to powerful emitters. To prevent this special precautions need to be taken in order to maintain electromagnetic compatibility between these various systems (Williams, 2001:15).

For all electromagnetic waves there is a basic relationship connecting their wavelength λ, their frequency f and the speed of the wave u in the medium of propagation. This relationship is given by Equation 2.5.34 (Maniktala, 2006:328). The speed u is precisely the speed of light, called 'c', and has the value of 3×10^8 m/s for a wave propagating in free space, as stated by Griffiths (2008:376) and Maniktala (2006:328). A simpler form of Equation 2.5.34 can be seen in Equation 2.5.35 (Maniktala, 2006:328).

$$\lambda = \frac{u}{f} \tag{2.5.34}$$

$$\lambda_{meters} = \frac{300}{f_{MHz}} \tag{2.5.35}$$

If a conductor has a dimension close to $\lambda/4$, it can end up radiating or receiving, the corresponding frequency effectively. This is the basic principle behind a radio antenna (Maniktala, 2006:329). An antenna can be considered a complex RLC network that exhibits inductive reactance at some frequencies and capacitive reactance at others. At a specific frequency, the resonant frequency, both these reactances are equal in magnitude but opposite in sign causing them to cancel each other. An antenna has its best efficiency at this resonant frequency. A half-wave antenna is the shortest resonant antenna length. Shorter wavelength antennas can resonant at harmonic frequencies, this principle is commonly used with quarter-wave whip antennas (Linx Technologies, 2012:4). However, if an antenna is shorter than or much longer than the 'optimum' of $\lambda/4$, the antenna can still be quite effective, and as such an antenna should not be judged merely by its length (Maniktala, 2006:329). As stated by Maniktala (2006:329) an antenna can still be quite effective down to less than $\lambda/10$.

Whenever an electric field, E-field, varies with time it produces a magnetic field, H-field, and vice versa as showed by Maxwell. Both E-fields and H-fields appear simultaneously when there is a time variance in either a magnetic or electric source. Some distance away these fields combine to form an electromagnetic wave. A charged capacitor has an associated E-field present in the space between its plates, as there is no current flow there is no expected H-field. However, when the capacitor is charging/discharging there is a current passing through the capacitor, so during this time there is both an E-Field and an H-field. A coil passing a steady current forms an associated H-field and no E-field. As the current through the coil varies the H-field is accompanied by an E-field constituting the magnetic field in the vicinity of the coil, and forming an electromagnetic wave a certain distance away from the coil. This is why EMI is of major concern with SMPS, as both these situations do occur repetitively during the operation of a switch-mode converter (Maniktala, 2006:329–330).

2.5.6.1 Board layout

A switching transition occurs when the state of a switch changes from an on-state to an off-state or vice versa. These state transitions typically last less than 100 ns, and are responsible for most of the noise present on traces found on a converter printed circuit board (PCB). The smaller the transition time, the more severe the possible consequences of noise. This noise has little to do with the switching frequency of the converter itself. Close attention must be given to troublesome or 'critical traces' of the converter's PCB. This requires an understanding of the flow of power related currents in the converter (Maniktala, 2006:239–240).

During a switching transition the current flowing in certain trace sections has to suddenly *stop*, and in others the current has to suddenly *start*. These trace sections are identified as the 'critical traces'. At these traces a very high di/dt is created during every switching transition which ends up creating small voltage spikes across them due to the parasitic inductance of PCB traces and the relationship $v = Ldi/dt$ (Maniktala, 2006:240). Figure 2.38 illustrates the identified 'critical traces' for three DC-DC converters redrawn from Maniktala (2006:241).

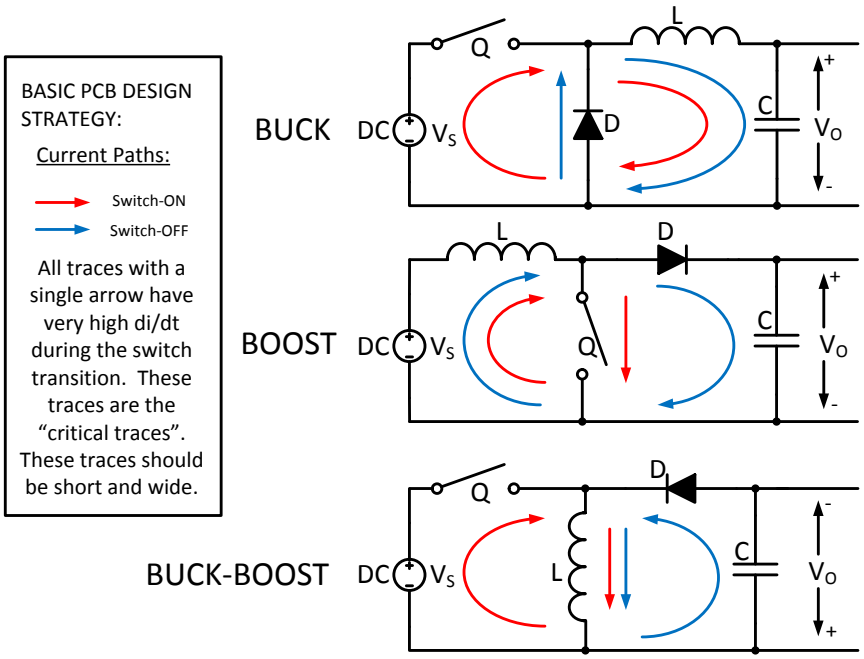

Figure 2.38: Critical trace sections for three topologies redrawn from Maniktala (2006:241)

These voltage spikes, caused by the high di/dt, not only cause performance issues due to their interaction with the supply and output of the converter, but can also infiltrate the control section of a converter causing it to behave unpredictably. Good local decoupling of the control section should be attempted in order to alleviate unpredictable behaviour of the control circuitry (Maniktala, 2006:242).

The electromagnetic field caused by inductors can infiltrate nearby circuits and sensitive traces causing issues, due to this very reason it is a good idea to use 'shielded inductors' thereby reducing EMI. If it is not possible to use 'shielded inductors' the inductors should be positioned away from sensitive areas such as ICs and the feedback traces (Maniktala, 2006:242).

Increasing the width of certain traces can be counter-productive, as any conductor with a varying voltage, irrespective of the current it may be carrying can become an E-field antenna if its dimensions are large enough. As such the only node that qualifies for copper filling is the ground node or plane. All other nodes including the input supply rail can start radiating because of the high frequency noise riding on them. Making large planes also increases the probability of that plane picking up noise from nearby traces and components through inductive and capacitive coupling (Maniktala, 2006:244).

With multi-layer boards it is common practice to fill one layer with ground, preferably this layer should be immediately below the power components/traces. This ground plane helps with thermal management, reduces inductance by imaging itself directly under the signal path, and causes a general reduction in noise/EMI through capacitive coupling. Ground planes are not perfect and may end up behaving as slot antennas in terms of EMI. This may occur if the ground

plane is partitioned in odd ways to create thermal islands or to route other traces (Maniktala, 2006:246).

The feedback signal trace is usually the only feedback trace to consider. If this trace picks up noise through capacitive or inductive coupling. Induced noise on the feedback trace can lead to slightly offset output voltages, and in extreme yet rare cases, even instability or device failure. A method in which to minimise noise pick-up is to keep the feedback trace as short as possible and keep the trace away from noise or field sources such as the switch, diode and inductor (Maniktala, 2006:246–247).

2.6 Protection concepts used in spacecraft power systems

One of the more critical features of any reliable power system design is the use of protection. The omission of such a feature is often only recognised after a failure event has occurred, and in spacecraft applications this could be catastrophic. Protection in a spacecraft power system should be such that any single failure will not produce a degradation of performance below the mission requirements during the lifetime of the spacecraft mission. Spacecraft power systems require a high level of reliability while maintaining a fail-safe protection scheme which should ensure quick isolation of any fault. Other spacecraft systems or commands from ground stations for protection should not be relied upon. Therefore, it is necessary to contain all critical protection within the power or energy sources of the spacecraft (Levins, 1991:157).

In general CubeSats use limited or no built-in redundancy as stated by Clyde Space (n.d.). The lack of redundancy within a CubeSat is typically due to mass, power and size constraints as well as the added complexity of the circuitry. It is still important to review the protection concepts used in spacecraft power systems as it may be possible to incorporate at least some of the concepts that are used on other spacecraft.

Solar array designs should incorporate series diodes to isolate sections of the solar array, as short-circuit failures can propagate from one array section to another. When mounting solar cells they should be satisfactorily isolated from ground as breakdown of the insulation layer can cause loss of solar array power due to the short-circuiting to ground of solar array strings (Levins, 1991:158).

Batteries are seldom fully redundant in spacecraft as their weight typically accounts for 15% to 20% of a spacecraft's dry mass. The battery management system should automatically protect batteries and cells against failures. These failures include open-circuit failures, under-voltage, over-voltage, over-temperature and/or pressure. Total loss of a battery due to open-circuit cell failure can be avoided through the use of relays or bypass diodes in parallel with each cell in the battery (Levins, 1991:158).

Solar array regulation is achieved either by means of a shunt regulator or series regulator. Shunt regulation involves shunting excess power from the spacecraft power bus, while series regulation involves blocked excess power from entering the spacecraft's power bus. A diagram illustrating a protected shunt regulator can be seen in Figure 2.39, redrawn from Levins (1991:158). A

permanent *on* or *off* state failure of a shunt or series regulator could result in a loss of solar power or in a bus over-voltage. Series redundant switches can be used as a means of protection for *on* state failures whereas additional redundant regulators can be used as protection against *off* state failures. When a non-dissipative shunt configuration is used, such as the S^3R, two diodes are required. These diodes are to required to prevent the power bus from short-circuiting when the dump switch is *on* in an instance where one of the diodes may have failed in an *on* state. Dissipative shunt configurations only require the use of a single diode. The use of a series regulator requires the use of a series diode to protect the regulating transistor from a solar array string short-circuit (Levins, 1991:158–159).

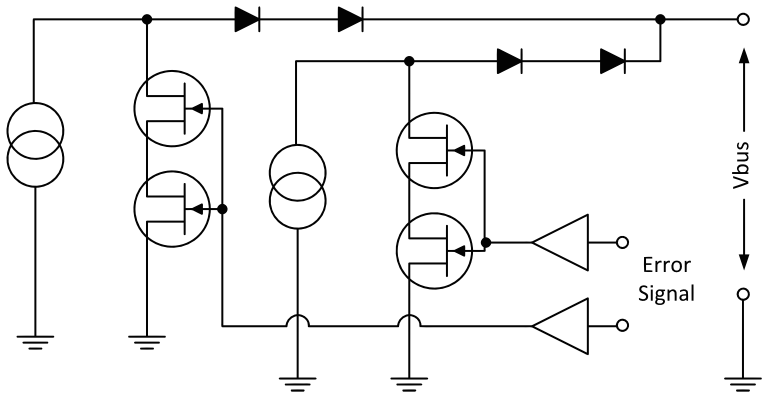

Figure 2.39: Protected shunt regulator redrawn from Levins (1991:158)

BCRs and BDRs should protected against failures which could produce a bus over-voltage, a bus short-circuit or a battery to bus short-circuit and in doing so must maintain the bus voltage within specification. Many different regulator topologies are used in satellite power systems. The protection, isolation and redundancy concepts utilised with these different regulator topologies is numerous. Conceptual circuits for a Boost regulator and Buck regulator are shown in Figure 2.40 and Figure 2.41 respectively. To protect these regulators against failure two control transistors and two series diodes are required. In order to provide full redundant protection the control transistors should have independent control electronics. Regulator topologies that include input current limiting protection in their designs are preferred for space applications as they offer a comprehensive protection against current surges and overloads (Levins, 1991:159).

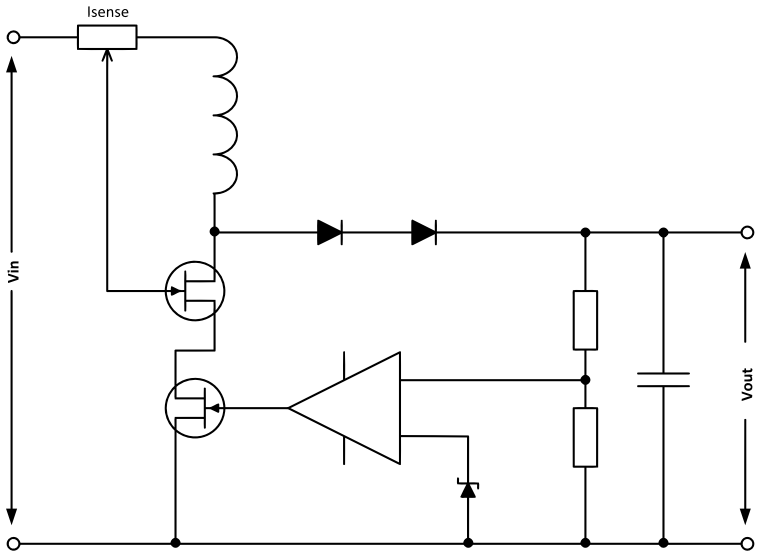

Figure 2.40: Protected Boost regulator redrawn from Levins (1991:159)

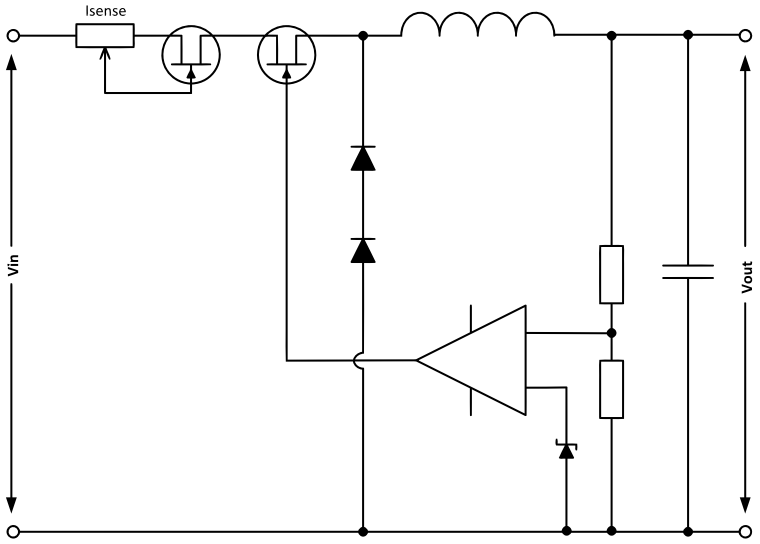

Figure 2.41: Protected Buck regulator redrawn from Levins (1991:159)

2.7 Typical CubeSat power systems

As with larger satellites, the subsystems developed for the CubeSat platform are somewhat tailored to a specific mission and the mission's requirements. Companies such as GomSpace, Clyde Space, Pumpkin and Innovative Solutions In Space (ISIS) are some of the companies currently developing and/or reselling generic and on customer request specialised "kits" or "parts" for the CubeSat platform.

GomSpace manufactures EPSes for 1U, 2U and 3U CubeSats. Their EPS P-series is a fully analogue system with the exception of a microcontroller for digital interfacing and maximum power point tracking. The EPS is designed to operate with triple junction PV solar cells with up to 2 solar cells in a series string. The electrical power from the cells is used to charge the battery

with the use of a Boost regulator. The EPS has under-voltage and over-voltage protection for the battery. The distribution comprises of two regulated power buses operating at +3.3 V and +5 V capable of delivering 5 A and 4 A respectively. The P11-models consist of a single MPPT capable of handling 10 W of PV power conversion at an average input efficiency of 93%, while the P31-models have 3 independant MPPT channels capable of handling 10 W each allowing up to 30 W of input power in total from the solar array. Each of these MPPT channels relies on a Boost DC-DC converter to handle the electrical power conversion. The EPS was designed to be operated on a "box" satellite with each MPPT channel connected to a pair of solar panels on opposite sides of the satellite (GomSpace, 2011:2–4).

The EPS manufactured by Pumpkin under the CubeSat Kit™ name was designed primarily for terrestrial use, typical applications for this kit are demonstrations, terrestrial testing and balloon missions. Though this EPS was not designed for space missions many functions found on this kit are present on space qualified EPSes as one of the applications of this kit is for terrestrial testing, and as such some of its features are relevant. This EPS operates with two or four 1500 mAh iPod® Li-poly rechargeable batteries. This EPS supplies an unregulated battery bus, a +5 V regulated bus and a +3.3 V regulated bus to the subsystems within a CubeSat. As the EPS is linear instead of switch-mode, no switching noise is present on the output voltage rails. This EPS includes an auto-resetting over-current trip fuse on the battery, the +5 V bus and the +3.3 V bus. Solar cells, if used in conjunction with this EPS, are connected directly to the V_{BATT} terminal on the EPS as an external source to charge the battery (Pumpkin inc., 2009:1–8). This method of charging would constitute a DET topology.

Clyde Space have developed numerous CubeSat electrical power systems, two of these systems are their 1U EPS and their FleXible EPS. The Clyde Space 1U EPS was designed to operate with a 10 Wh or 20 Wh Li-ion battery and was designed to operate on a 1U CubeSat. The solar panels for this EPS are connected in the same configuration as the P31-model manufactured by GomSpace. In this configuration only one panel per pair of solar panels is directly illuminated by the sun while the other panel is only illuminated through albedo from the Earth. This EPS sources power from the solar panels through three BCRs capable of handling 3 W of power each at 10 V maximum. Each BCR has an in-built MPPT which relies on a SEPIC DC-DC converter to handle electrical power conversion. Each SEPIC DC-DC converter has a typical efficiency of 79% at an input voltage of 6 V and with the EPS under full load. The MPP sampling is done ever 2.5 s. The battery voltage is conditioned to +5 V and +3.3 V and able to source 2.5 A per bus through the use of Buck converters operating at 480 kHz. The battery bus, +5 V bus and +3.3 V bus have over-current protection, an over-current event is reset approximately every 600 ms while the test period for measuring the current is in the range of 30 ms to 60 ms. The Clyde Space 1U EPS has battery under-voltage protection which shuts down the supply buses in the event that the battery voltage drops below ∼6.2 V, the supply buses are re-activated when the battery voltage exceeds ∼7 V (Strain, 2010*a*).

The Clyde Space FleXible EPS has four "large" and two "small" BCRs and was designed to be operated on a CubeSat or compatible nano-satellite. As with the 1U EPS each of these BCRs has a built-in MPPT. The "large" BCRs are capable of handling 8 W at a maximum voltage of

25 V each, while the "small" BCRs can handle 3 W at a maximum voltage of 10 V. The solar panel configuration for this EPS is such that four pairs of 6-8 cell panels not exceeding 8 W per pair, and two pairs of 2 cell panels not exceeding 3 W per pair can be mounted on the satellite (Strain, 2010*b*:12). Clyde Space uses Spectrolab Ultra Triple Junction (UTJ) cells on their solar panels (Clyde Space, 2009). The EPS through a power conditioning module (PCM) and power distribution module (PDM) supply the unregulated battery bus, regulated +5 V and +3 V buses. The 8 W BCRs utilise a Buck DC-DC converter and claims 90% efficiency at an input voltage of 16.5 V and under full load, while the 3 W BCRs utilise a SEPIC DC-DC converter and claims 79% efficiency at an input voltage of 6 V and under full load. The PCM and PDM specifications between the Flexible EPS and 1U EPS are identical. The PCM supplies +5 V and +3.3 V at 2.5 A from Buck converters operating at 480 kHz. The over-current protection in the PDM resets approximately every 600 ms with a test period ranging from 30 ms to 60 ms (Strain, 2010*b*).

2.8 Summary

It is evident from this chapter that the space environment is a harsh place for electronics. The design of a reliable satellite requires significant thought as the effects of this environment can seriously affect the subsystems within the satellite. It was established in this chapter that the CubeSat is expected to operate at a maximum temperature range of $-40°$ C to $85°$ C. This large temperature range, along with the reduced ability to transfer heat due to the vacuum, requires the EPS and other subsystems to dissipate as little power as possible. Additionally some form of thermal management would be required as the maximum expected operating temperature range for the CubeSat in LEO is outside the batteries' maximum operating temperature ranges of $-20°$ C to $60°$ C when discharging and $0°$ C to $45°$ C when charging.

It was also found in this chapter that the EPS has to protect other subsystems within the satellite from destructive SELs through protecting the power bus from over-current situations. Due to the strong vibrations and high levels of acceleration during launch, tall and heavy components are to be avoided along with mechanical components such as potentiometers that can be affected by vibration.

This chapter investigated the components and concepts of satellite power systems. The components and concepts of the satellite EPS that are covered include electrical power sources, satellite power system topologies, switch-mode power supply topologies, protection concepts and typical CubeSat power systems.

In this chapter the control aspects of SMPS needed to maintain a stable, regulated output voltage are investigated. Additionally, the importance of board layout is investigated, in an attempt to reduce EMI between various components and subsystems within the CubeSat.

Though CubeSats typically use limited or no built-in redundancy, simple protection concepts could be applied to the CubeSat such as battery under-voltage and over-voltage protection. The theory behind PV solar cells as a primary energy source was investigated, as well as Li-ion batteries as a secondary energy source. The different satellite power system topologies such as

DET and MPPT along with a couple of the MPPT techniques such as the FOCV and P&O were also investigated.

This chapter concludes with a short summary of typical CubeSat power systems produced by companies such as GomSpace, ClydeSpace and Pumpkin to serve as a guide in designing a satellite power system. Items of interest consist of the types of DC-DC converters utilised by these manufacturers, their efficiencies, power handling, input voltage ranges and EPS topologies utilised by these manufacturers.

The knowledge gained in this chapter lead to the design of the prototype seen in Chapter 3.

Chapter 3

Prototype design and verification

3.1 Introduction

In this section the operation of the various components of the designed EPS prototype will be described in greater detail along with the design of some of the sections of the EPS. Figure 3.1 illustrates a block diagram of the designed CubeSat EPS with its main components. This block diagram shows the main flow of power through the EPS and gives a broad overview of how the different control signals interface between the different components of the EPS.

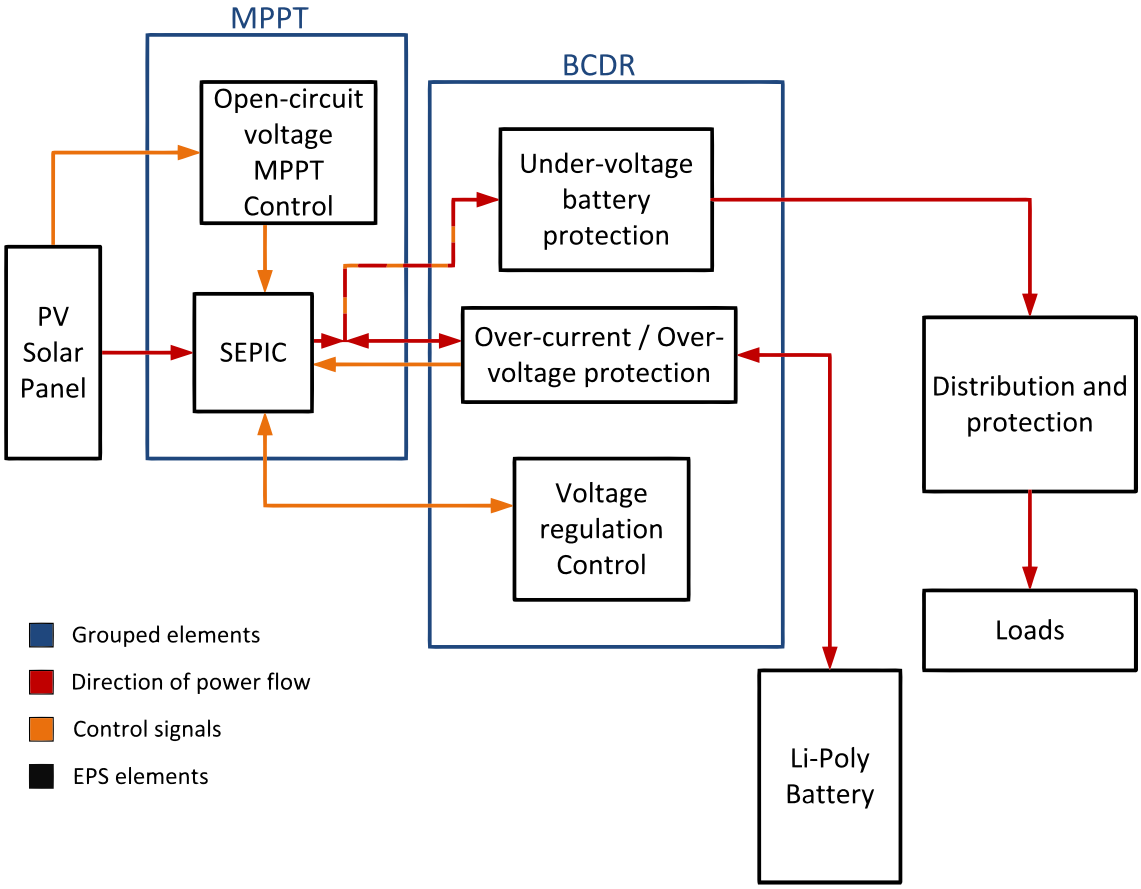

Figure 3.1: Proof of concept prototype block diagram

The primary energy source of the designed prototype is the Sun, using PV solar cells, placed in panels, this energy is converted to electrical energy for use by the satellite. The designed EPS is capable of accepting PV solar cells of various technology types. The system was designed to be as versatile as possible allowing for future progress in solar cell technology as well as accepting various technologies that currently exist.

The electrical energy from the PV solar panel is extracted by the MPPT through the SEPIC DC-DC converter. This allows the energy from the PV solar panel to be utilised as efficiently as possible. The power delivered by the SEPIC DC-DC converter flows through the over-current and over-voltage protection circuitry to the battery. In the event that either the over-current or over-voltage protection engages, the SEPIC DC-DC converter is shut down halting the flow of power from the PV solar panel. Once the battery voltage reaches the constant charge voltage stage of its charge cycle, the voltage regulation control loop becomes active regulating the battery bus to approximately 8.2 V.

The battery bus voltage is constantly monitored as an indication of the state-of-charge (SoC) of the Li-poly battery. In the event that the battery voltage drops to approximately 6.2 V the loads are disconnected in an attempt to protect the battery. The loads are kept disconnected from the EPS until the battery voltage has reached approximately 7.4 V. At this point the loads are reconnected supplying the satellite with power.

Power supplied to loads, such as payloads and other subsystems, is supplied through the distribution. The distribution monitors the current flowing to the loads and disconnects the appropriate load in the event too much current is drawn by the load. The loads are reconnected for a short duration in which the current is measured once again. If the fault is no longer present power is resupplied to the load, if the fault is still present the load is disconnected once again. The distribution also includes a logic level input allowing loads to be manually disconnected by an OBC or other digital system. This allows some subsystems to be powered down when they are not needed and thereby conserving precious energy that could rather be used by other loads or to charge the battery.

3.2 Design considerations

As there is no known mission as of yet for the proposed EPS design it was decided that a generic design be considered. The author chose to go about designing a FOCV based MPPT using a SEPIC DC-DC converter and supplying the battery bus to the EPS loads. The decision for this method of MPPT was due to the relative simplicity of design through analogue means while still achieving a usable efficiency out of the solar panels. The use of a SEPIC DC-DC converter allows the output voltage to be greater than or smaller than the input voltage. This gives the user of the EPS some freedom in how they would like to configure the solar array on the CubeSat. The use of a SEPIC DC-DC converter allows the EPS to be connected to the solar array of a 1U or 3U CubeSat with the solar cells connected in series or parallel depending on the satellite's mission requirements. A variety of PV solar cell technologies could be used as the PV solar panel voltage could be below or above the battery voltage. As the design is a proof of concept design

a single solar array input channel was designed.

Implementing the design in practice could require multiple channels to be used with the CubeSat EPS. Each MPPT channel could use a different DC-DC converter topology depending on the requirements of the mission. The use of a SEPIC DC-DC converter allows the CubeSat to be fully deactivated during launch by disconnecting the battery from the EPS as the SEPIC DC-DC converter would isolate the PV solar panels from the rest of the satellite. This could be implemented through the use of a deployment switch as stated in the CubeSat standard (see Chapter 2.1). Three MPPTs could be used on a CubeSat similar to GomSpace with each MPPT connected to a pair of PV solar panels on opposite sides of the satellite (see Section 2.7).

Two Li-poly cells placed in series form the battery, this allows for a larger usable voltage to be supplied to the loads in this battery bus system. Using a battery bus allows the addition of low-dropout (LDO) linear regulators or switch-mode converters to supply additional bus voltages if required. If the Li-poly cells were to be placed in parallel the option of using LDOs would be difficult as the battery voltage would be in the order of 3 V - 4 V, which is particularly low. Under-voltage battery protection was designed into the EPS to protect the battery from excessive discharge. The design was such that in the event that the battery voltage drops below 6.2 V the battery bus attached to the distribution is disconnected until the battery voltage reaches 7.4 V (the nominal battery voltage). The minimum operating voltage of 6.2 V was chosen to allow some headroom over the minimum normal cell voltage of the Li-poly battery. This headroom of approximately 200 mV gives the circuit some safety margin. This safety margin allows for some battery cell voltage imbalance to occur. Batteries with similar cell characteristics should be chosen to help reduce the chance of over-charging or over-discharging brought on by an imbalance in the cells.

The SEPIC DC-DC converter operates with two control loops, a control loop used for MPPT as well as an output voltage control loop. The MPPT control loop aids in extracting the maximum power from the solar panels when maximum power is required, while the output voltage control loop is used to regulate the output voltage to the battery charge voltage of 8.2 V. These two control loops work together to allow the battery to charge as fast as possible while not exceeding the battery's maximum charge voltage. In the event multiple MPPT channels are utilised the same voltage control loop could be utilised with all the MPPTs, but each channel would need its own MPPT control loop. The use of a single voltage control signal for all MPPT DC-DC converters is subject to the stability of the converter used, and as such having multiple DC-DC converters of the same design is beneficial. If differing SMPS converter topologies are utilised it may be possible to rely on a single voltage control signal given that stability is kept with each of the converters. If the voltage control loop was not present the MPPT would continue to extract as much power as possible from the solar array causing the battery voltage to exceed the maximum rated charge voltage of the batteries, and possibly damaging the battery and the circuitry of the EPS.

The design incorporates an emergency over-voltage and over-current shut down used in the battery charging section of the circuit. In the unlikely event that the reference voltage used in generating the error signal used in controlling the SEPIC DC-DC converter drifts excessively, or

a regulation fault of the converter occurs, the PWM signal of the DC-DC converter is abruptly pulled to ground dropping the output voltage. Similarly if the current charging the battery is excessive the PWM of the DC-DC converter is abruptly pulled to ground dropping the output voltage and in turn dropping the current flowing into the battery. In the event that the solar array cannot deliver enough power to charge the battery at a rate larger than 1.0 C the over-current battery protection could be omitted. The emergency over-voltage and over-current serves as a crude form of protection for the battery in the event that there is a fault with the control circuitry brought on by an SEL or drifting caused by temperature changes or ageing of the components. If the SEPIC DC-DC converter's main switch was subject to an SEL and the PV solar panel terminals were to be shorted through the SEPIC converter's inductor the output diode would isolate the short from the battery. During such an event power could still be harnessed from the remaining MPPT circuits.

The power distribution consists of an over-current protection (OCP) latch. Multiples of these latches could be utilised in the distribution of a CubeSat, each protecting a critical subsystem or payload within the satellite. The designed OCP consists of a MAX4374 current amplifier and serves as a resettable fuse "tripping" when a set current limit is exceeded. The current limit designed into the proof of concept design was set to 300mA. The proof of concept distribution OCP can be shut down remotely through a logic level input, this allows specific loads to be turned on and off by an on-board computer (OBC) or other digital systems. This current limit is easily adjusted through the selection of the appropriate resistor values.

A summary of the EPS prototype specifications can be seen in Table 3.1.

Table 3.1: EPS prototype specifications

Prototype topology specifications		
Parameter	**Requirement**	**Reasoning**
Circuit type	Analogue	Note 1
Topology type	FOCV MPPT with battery bus	Note 2
Prototype input specifications		
Parameter	**Requirement**	**Reasoning**
PV input voltage range	V_{mpp} **voltage:** 3 V - 20 V **Maximum** V_{oc}**:** 25 V	Note 3
Maximum input power	10 W	Note 4
Prototype energy storage specifications		
Parameter	**Requirement**	**Reasoning**
Battery type	Li-poly	Note 5
Output voltage	8.2 V	Note 6
Battery under-voltage threshold	6.2 V	Note 7
Prototype output specifications		
Parameter	**Requirement**	**Reasoning**
Output power	Mission specific	Note 8
Payload OCP	Adjustable	Note 9

Note 1: Improved reliability as there is no possibility of SEUs (See Section 2.2.1).

Note 2: MPPT for more efficient power extraction from the PV array (See Section 2.4.4 and 2.4.1.1). Battery bus for versatility and simplicity.

Note 3: Typical examples of CubeSat PV solar panels include the Clyde Space 1U CubeSat solar panel with a V_{mpp} of 4.02 V at its maximum rated temperature (Clyde Space, 2009). This PV solar panel consists of 2 Spectrolab UTJ PV solar cells. The Clyde Space 3U CubeSat solar panel consists of a series string of 8 UTJ solar cells and has a V_{mpp} of 19.54 V at its minimum rated temperature. The EPS has to be able to handle a V_{oc} of over 21.46 V for one of these 8 cell solar panels (Clyde Space, 2009). The GomSpace P-Series has a minimum PV solar panel input voltage of 3.7 V GomSpace (2011). The Clyde Space FleXible EPS has a minimum input voltage of 3.5 V for their 3 W SEPIC based MPPT and a maximum input voltage of 25 V for their 8 W Buck based MPPT (Strain, 2010*b*). This illustrates the PV input voltage range that could be expected of a CubeSat EPS. Using such a large PV input voltage range allows for a myriad of solar cell configurations, either in series or in parallel, and allows many different PV solar cell technologies to be used.

Note 4: The Clyde Space 3U CubeSat side panel can deliver 7.29 W at BOL at 28° C (Clyde Space, 2009). The Clyde Space FleXible EPS can handle an input power of up to 8 W while the GomSpace P-Series can handle an input power of up to 10 W (GomSpace, 2011; Strain, 2010*b*).

This illustrates the amount of power a CubeSat EPS could be expected to handle per PV input channel.

Note 5: Li-ion and Li-poly battery chemistries are commonly used with CubeSat power systems due to their high energy densities (See Section 2.4.2).

Note 6: A battery consisting of two Li-poly batteries allows the use of LDOs for distributed voltages or SMPS for a variety of bus voltages. Two Li-poly cells in series constitutes a charge voltage of 8.4 V (See Section 2.4.2.2). The use of 8.2 V allows for some cell imbalance as this reduces the likelihood of either cell being charged above 4.2 V.

Note 7: Typically a Li-ion or Li-poly battery is discharged to a cell voltage of 3 V (See Section 2.4.2.2). Having a battery consisting of two cells constitutes a minimum voltage of 6 V. 6.2 V was chosen to allow for some cell imbalance as well as giving the 5 V housekeeping LDO some voltage headroom for regulation. The 5 V housekeeping LDO is important in maintaining the safe operation of the power system. If the battery voltage were to drop too low the 5 V housekeeping LDO would cease to regulate and the voltage supplied to various components of the power systems would be negatively affected.

Note 8: This is specific to a mission, as there is no stated mission for the EPS there is no obvious required output power. It is beneficial for the EPS to be as efficient as possible, hence the need for the use of SMPS over a linear based power system. This requirement would need to be determined once a mission for the EPS is established.

Note 9: This is specific to the current requirements of the payloads used in a specific mission. A configurable OCP was required as to allow for different loads.

3.3 Photovoltaic solar panel

In order to simulate the designed EPS a PV solar cell model was required, using the single diode equivalent circuit seen in Figure 2.6 and the specifications of UTJ solar cells from Spectrolab along with the specifications of the solar panels developed by Clyde Space an approximate model seen in Figure 3.2 was developed (Spectrolab, 2008; Clyde Space, 2009; Intusoft, 2005). The power system was designed to operate with a variety of PV solar cell technologies requiring the PV solar cell model used to have a realistic P-V curve, though the model itself did not have to perfectly match any particular PV solar cell as the power system was designed to accept PV solar panels with a variety of P-V characteristics.

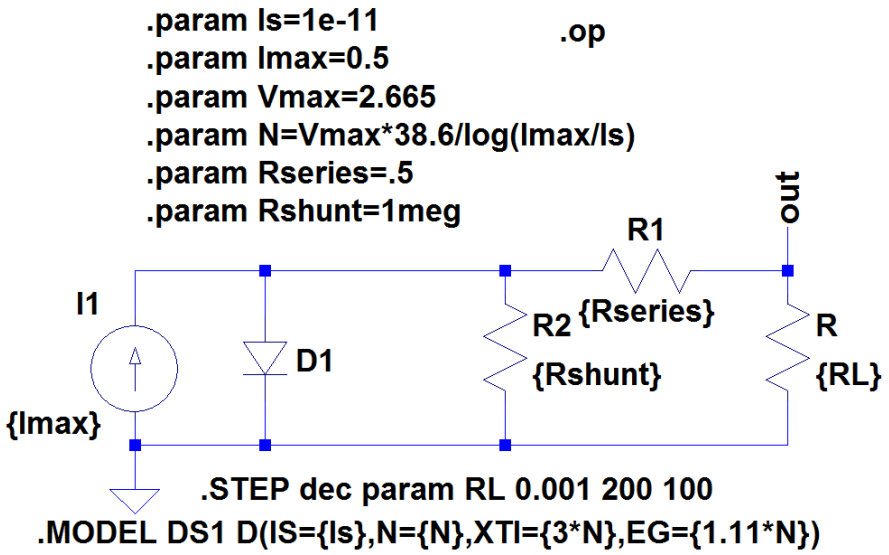

Figure 3.2: Solar cell model used in simulations

Using the PV solar cell model seen in Figure 3.2 the I-V and P-V curves seen in Figure 3.3 were simulated. This simulated cell was used in all subsequent simulations where a PV solar cell was required.

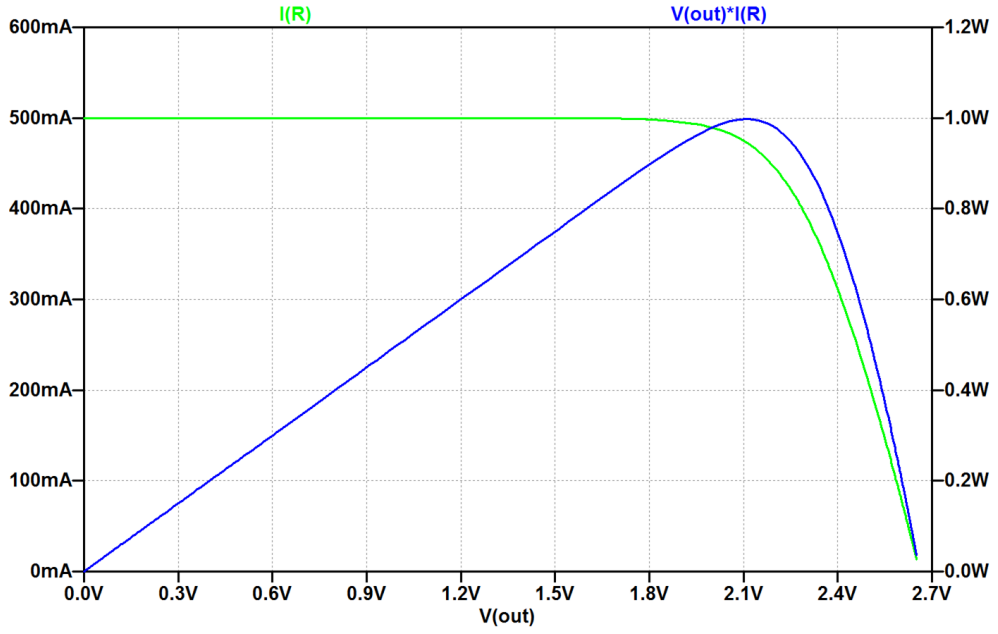

Figure 3.3: I-V and P-V curves of simulated solar cell model

3.4 Housekeeping

The EPS circuitry requires specific voltages and timers in order to function correctly. It was decided to operate the circuitry at 5 V as this allowed more freedom in the selection of components. Operating the circuitry at 5 V required a low-dropout voltage regulator (LDO) to

be used. This requirement is due to the minimum battery voltage of approximately 6 V when the battery is fully discharged. Using a 5 V supply allowed the designer to use a TL5001A PWM controller from Texas Instruments (TI). This component is readily available, operates from 3.6 V to 40 V at switching frequencies up to 500 kHz and can withstand the predicted $-40°$ C to $85°$ C maximum temperature range a CubeSat could be expected to operate in (Texas Instruments, 2002). Using an integrated PWM IC allowed for a more compact and simplified design. The use of a 5 V supply allowed logic level MOSFETs to be switched on *harder* than would be the case with a lower gate voltage such as 3.3 V. The larger the voltage applied to the gate of a MOSFET the lower the on-state resistance, and hence it was beneficial to have as large a voltage as possible across the gates in an attempt to reduce the power losses in the MOSFETs. The minimum voltage of the timers used in the circuitry was 4.5 V and as such a supply voltage much lower than 5V could not be used. The design of the PWM circuitry is discussed in greater detail in Section 3.6.1.

The LDO chosen was an LM1117I-ADJ from National Semiconductor due to its low dropout voltage (typically 1.1V at 100mA) and large operating temperature range ($-40°$ C to $125°$ C) (National Semiconductor, 2006). The adjustable version of this LDO was chosen as it allowed the designer to modify the prototype circuit if required. If the dropout voltage of the LDO was significantly larger than expected the regulated voltage could be reduced within the limits of the connected circuitry.

The design of the LDO was based upon the basic adjustable LDO voltage regulator shown in Figure 3.4 using the LM1117 taken from National Semiconductor (2006:9).

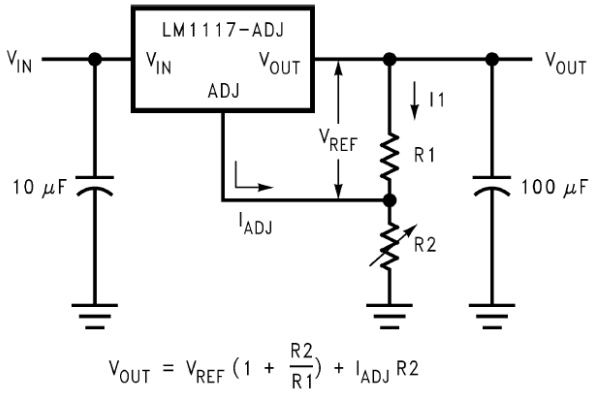

Figure 3.4: LM1117 basic adjustable regulator taken from National Semiconductor (2006:9)

The values from the datasheet required to calculate the components are shown in Table 3.2

Table 3.2: Required parameters for LM1117 Design

Symbol	Parameter	Typical Value
V_{REF}	Reference Voltage	1.25V
I_{ADJ}	Adjust terminal current	60μA

Equation 3.4.1 was used in determining the component values associated with Figure 3.4. R1 was determined for an output voltage of 5 V with a 10 kΩ resistor chosen for R2. The chosen E12 series resistor for R1 can be seen parentheses after the calculated value.

$$\begin{aligned} V_{OUT} =& V_{REF}(1 + \frac{R2}{R1}) + I_{ADJ}R2 \\ \therefore R1 =& \frac{R2}{\left(\frac{V_{OUT} - I_{ADJ}R2}{V_{REF}} - 1\right)} \\ R1 =& \frac{10k\Omega}{\left(\frac{5V - 60\mu A \cdot 10k\Omega}{1.25V} - 1\right)} \\ =& 3.9683k\Omega\,(3.9k\Omega) \end{aligned} \tag{3.4.1}$$

Throughout the design reference voltages were required. One of these reference voltages was used by the compensation amplifier in generating the error signal required in controlling the DC-DC converter. Another reference voltage is used in the battery under-voltage protection circuitry. These reference voltages have a voltage of 2.5 V and use a TL431 precision programmable reference IC. Initially the circuit was designed to use a simple resistor based voltage divider used in conjunction with a buffer to form the reference voltages. It was later decided to replace one of the resistors in the divider with the TL431. The replacement was undertaken due to the concern that the 5 V LDO might not regulate affectively as the battery discharges and the input voltage of the LDO drops towards 6 V. The SOT-23-3 package was chosen as it was possible to directly replace the resistor initially used in the voltage divider with the device with no alterations to the prototype board designs. The basic circuit used for all voltage references can be seen in Figure 3.5.

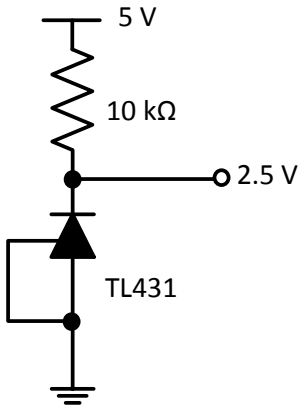

Figure 3.5: Basic 2.5 V reference voltage

The timers within the EPS control the sample and hold (S&H) circuitry, disconnecting the solar panel from the EPS and resetting any "tripped" over-current protected bus lines in the distribution. To achieve a compact design a simple 555 astable circuit was used. This astable

circuit provides the timed interval between successive MPP samples. The 555 was connected to two monostable 555 circuits used in setting the pulse widths used in disconnecting the solar panel and triggering the S&H. The two monostable circuits were implemented on a single 556 to further reduce the size of the circuit.

Figure 3.6 and Figure 3.7 show different configurations of the 555 used in the EPS for timing taken from Texas Instruments (2010:9-11). The 555 operating in astable mode was used for global timing across the EPS driving the two monostable 555s integrated into a single 556 IC.

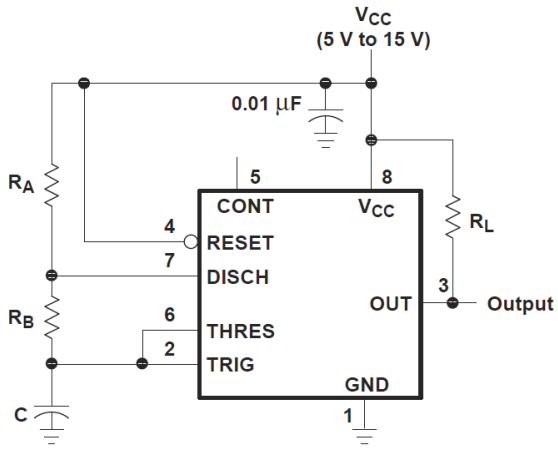

Figure 3.6: Generic 555 astable circuit taken from Texas Instruments (2010:9)

The pulse width was unimportant in the astable design as this timing circuit would be driving the two monostable timers used in setting the appropriate pulse widths. Equation 3.4.2 shows the calculations involved in selecting the component values with a $10\mu F$ capacitor used for C and a $100k\Omega$ resistor used for R_A. The calculations shown in Equation 3.4.2 relate to a period of approximately 2.5s. The chosen E12 resistor value for R_B can be seen in parentheses after the calculated value.

$$\begin{aligned} period =& 0.693(R_A + 2R_B)C \\ \therefore R_B =& \frac{1}{2}\left(\frac{period}{0.693C} - R_A\right) \\ =& \frac{1}{2}\left(\frac{2.5s}{0.693 \cdot 10\mu F} - 100k\Omega\right) \\ =& 130.3752k\Omega\,(150k\Omega) \end{aligned} \tag{3.4.2}$$

The two monostable timers were designed to output a 15 ms and 30 ms pulse. These pulses control the S&H control and the DTC respectively. Figure 3.7 shows a generic 555 monostable circuit, Equation 3.4.3 corresponds to the S&H timer, while Equation 3.4.4 corresponds to the DTC timer. It was decided to use a 100nF capacitor for C in the S&H and DTC timer. The chosen E12 resistor values for both the 15 ms and 30 ms timers can be seen in parentheses after the calculated values.

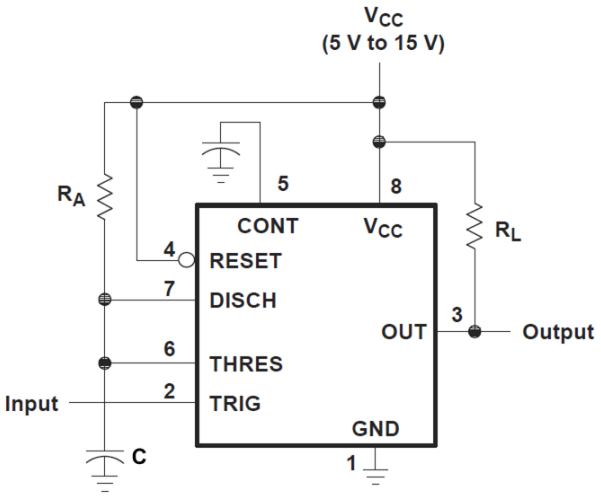

Figure 3.7: Circuit for 555 monostable operation taken from Texas Instruments (2010:10)

15 ms sample timer:

$$\begin{aligned} t_w &= 1.1 R_A C \\ \therefore R_A &= \frac{t_w}{1.1C} \\ R_A &= \frac{15ms}{1.1 \cdot 100nF} \\ R_A &= 136.3636k\Omega \, (150k\Omega) \end{aligned} \tag{3.4.3}$$

30 ms shut down timer:

$$\begin{aligned} t_w &= 1.1 R_A C \\ \therefore R_A &= \frac{t_w}{1.1C} \\ R_A &= \frac{30ms}{1.1 \cdot 100nF} \\ R_A &= 272.7273k\Omega \, (270k\Omega) \end{aligned} \tag{3.4.4}$$

Selecting a resistor value of 150 kΩ for R_A associated with the 15 ms timer results in a calculated pulse width of approximately 16.5 ms, and the selection of a resistor value for R_A associated with the 30 ms timer results in a calculated pulse width of approximately 29.7 ms. Additionally, the tolerances of R_A and C could cause an additional error in the expected pulse widths. The accuracy of the timers is not essential, and as such the discrepancy between the desired and calculated pulse widths is acceptable.

3.5 Maximum power point tracking

The MPPT utilised an analogue FOCV based MPPT method of control in combination with a SEPIC DC-DC converter. Figure 3.8 illustrates a simplified block diagram of the employed

MPPT method of control. The operation of this circuit is fairly simple. The MPP voltage of the solar panel, V_{mpp}, is achieved through the method described in Section 2.4.4.2.

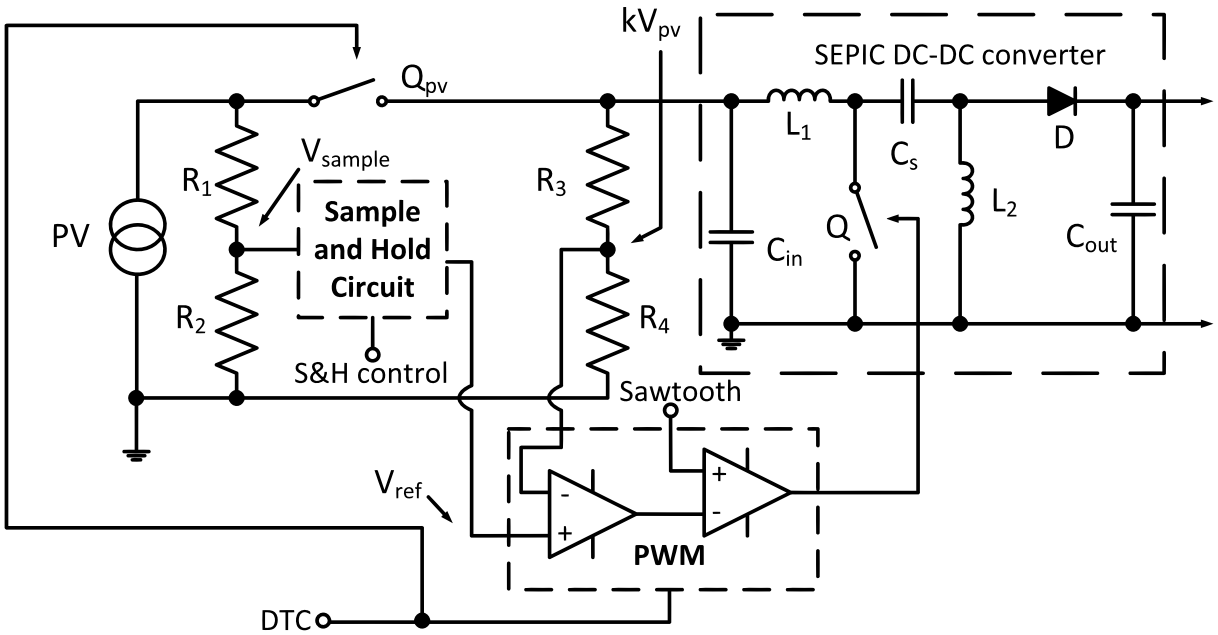

Figure 3.8: MPPT block diagram

The MPPT control circuit was initially designed to sample V_{mpp} approximately every second. Once it was established that the MPPT was functioning correctly the timing was altered to approximately 2.5 s which is similar to that of Clyde Space (Strain, 2010*a*:16). The design of these timers is covered in Section 3.4. The period between samples was increased as sampling too frequently would result in a greater loss in power from the sampled PV solar panel. A period between samples of 2.5 s was chosen as this has been proven successful by Clyde Space in their designs and was decided as a good starting point for the MPPT design. The simplicity of the design allowed the timing interval between successive samples to be adjusted with relative ease. If the satellite is expected to have a high roll/tumble rate this interval can be shortened through the selection of the appropriate timing capacitor and/or resistors (see Section 3.4). The main advantage of sampling the MPP more frequently, is any changes in the capability of the solar cell to produce power are sampled more frequently resulting in better MPPT. The major disadvantage of sampling more frequently is whenever a sample is taken the solar panel is disconnected from the EPS halting the flow of power from the solar panel.

When MPP sampling is initiated the state of the dead-time control (DTC) pin is changed. This leads to the solar panel being disconnected from the SEPIC DC-DC converter and the PWM signal controlling the SEPIC DC-DC converter to be shut down. The SEPIC DC-DC converter is disabled to reduce the possibility of induced noise from the converter being sampled by the S&H circuit. Disconnecting the solar panel allows for the approximate scaled open-circuit voltage of the solar panel, V_{sample}, to be measured through the resistor based voltage divider, R1 and R2, connected to the S&H circuit.

The voltage divider connected to the S&H, R1 and R2 in Figures 3.8 and 3.9, was designed to scale V_{oc} to a usable level for use by the error amplifier seen in the PWM stage of Figure 3.8. This voltage divider includes the voltage ratio factor between V_{oc} and V_{mpp} such that $V_{sample} = kM_vV_{oc}$. The voltage divider network requires the use of resistors with a large resistance. By having a large resistance, the solar panel is not excessively loaded, maintaining the solar panel at a voltage approximately that of V_{oc}. Once the solar panel is disconnected the S&H circuit is enabled, thereby sampling V_{sample}. The sampled voltage, V_{sample}, is essentially kV_{mpp} due to the relationship $V_{mpp} = M_vV_{oc}$ (see Section 2.4.4.2).

Figure 3.9 shows a simplified illustration of the voltage dividing resistor networks used in the MPPT circuit in Figure 3.8. The voltage divider represented by R1 and R2 is used during the sampling of the scaled maximum power point voltage, kV_{mpp}. The voltage divider represented by R3 and R4 is used in measuring the scaled operating voltage of the solar panel, kV_{pv}. The voltage drop across the MOSFET switch can be considered negligible if the MOSFET has an on-state resistance, $R_{DS(ON)}$, which is significantly small or in the event the current sourcing capability of the solar panel is small.

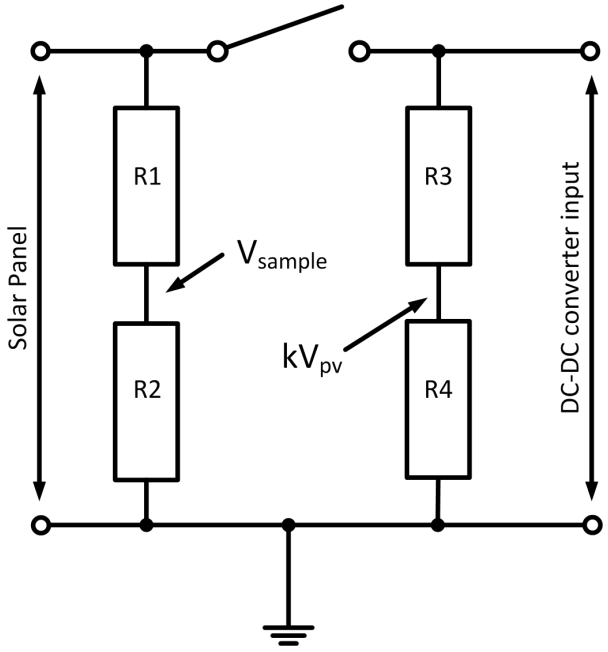

Figure 3.9: Simplified MPPT sample and reference voltage divider

The decision was taken to scale the measured voltages, V_{sample} and kV_{pv}, such that these voltages never exceed 4 V at a maximum solar panel voltage of 20 V. The supply for the operational amplifiers used in measuring the scaled voltages was 5V, and as such a lower voltage than 5V was selected as a starting point. If the divider networks were designed to operate at a lower voltage issues may have been encountered if lower voltage solar panels were used due to noise. The maximum input voltage that the MPPT circuitry was designed to operate at was 20V, choosing a value for R4 of $100k\Omega$, a value for R3 was calculated through the use of Equation 3.5.1.

$$
\begin{aligned}
kV_{pv} &\approx V_{pv}\left(\frac{R4}{R3+R4}\right) \\
\therefore R3 &\approx R4\left[\frac{V_{pv}}{kV_{pv}}-1\right] \\
R3 &\approx 100k\Omega\left[\frac{20V}{4V}-1\right] \\
R3 &\approx 400k\Omega\ (390k\Omega) \\
\text{and } k &\approx \left(\frac{R4}{R3+R4}\right) \approx 0.2041
\end{aligned}
\tag{3.5.1}
$$

This results in V_{pv} being scaled by a factor of 0.2041

Choosing $R1 = R3$ and $R2 = R4$ equates to a voltage factor, M_v, of 1. The designer chose to use a potentiometer in the place of R2, allowing M_v to be adjusted from 0 to 1 for testing purposes.

The basic S&H circuit can be seen in Figure 3.10. During the sampling period the switch seen in Figure 3.10 is closed. Both operational amplifiers act as buffers exhibiting a high input impedance and a low output impedance. The first buffer located between V_{sample} and the *switch* follows the scaled solar panel voltage. During sampling the switch is closed resulting in the capacitor charging to this scaled solar panel voltage. During this time the solar panel is also disconnected from the EPS resulting in the capacitor charging to $kM_vV_{oc} = kV_{mpp}$. Once sampling has completed the *switch* is once again disconnected, resulting in the capacitor "holding" the previously sampled voltage. The buffer situated between the *switch* and V_{ref} acts as a high impedance load to the capacitor resulting in the capacitor's voltage dropping extremely gradually over time. The output of this buffer, V_{ref}, is later used in the MPPT control as it closely approximates kV_{mpp}.

Once the sampling process is completed, the solar panel is reconnected to the SEPIC DC-DC converter and the PWM driving the converter is re-enabled. The error amplifier within the PWM section compares the previously stored $V_{sample} = kV_{mpp}$, with the current scaled solar panel voltage, kV_{pv}. If kV_{pv} is larger than kV_{mpp}, the duty-cycle is increased, thereby drawing more current from the solar panel and dropping V_{pv}. If the solar panel voltage is below the MPP voltage, the duty-cycle is reduced, thereby reducing the current drawn from the solar panel and allowing the solar panel voltage to increase towards the MPP voltage. Controlling the DC-DC converter in this manner causes the solar array voltage to oscillate around the MPP voltage in an attempt to produce $V_{pv} = V_{mpp}$.

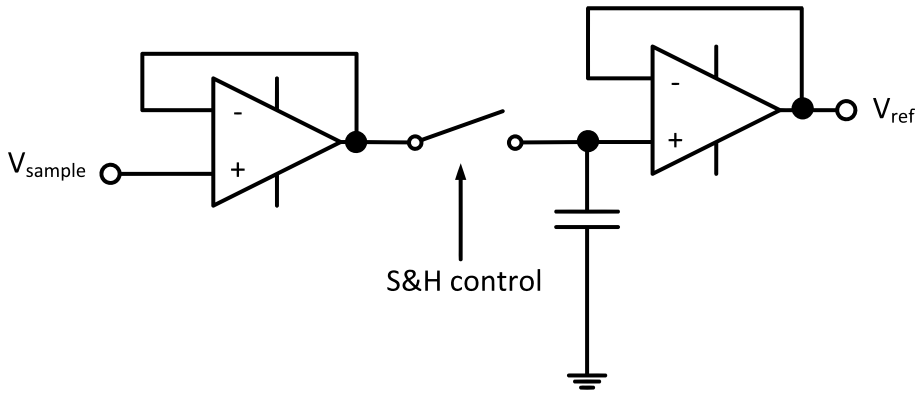

Figure 3.10: Sample and hold circuit

Figure 3.11 shows the circuit used in simulating the designed MPPT with no output voltage regulation. The current drawn from the solar panel is proportional to the duty-cycle and thus this circuit could be applied to a variety of DC-DC converters, such as a Buck or Boost converter. In Figure 3.11 a SEPIC DC-DC converter was used with two solar cells. The solar cell used in this simulation corresponds with Figure 3.2 and Figure 3.3. The sinusoidal voltage source simulates a slow change in voltage of the solar panel. Such a voltage fluctuation in practical terms could represent a change in the temperature of the solar panel. The time between samples illustrated in Figure 3.11 and Figure 3.12 has been reduced to 20 ms in an attempt to better illustrate the working of the MPPT to the reader. This is due to the small sampling period relative to the period between MPP samples. Additionally, scaling the timing significantly reduced the simulation time.

The basic operation of Figure 3.11 relies on M2 periodically disconnecting the solar panel depicted by V2 and the two PV solar cells. During this time the approximate scaled maximum power point voltage, kV_{mpp}, of this solar panel is sampled with the use of R2, R5, U2, U5, C3 and U4. When the solar panel is reconnected this sampled voltage, $V_{(Vref)}$, is compared to the scaled solar panel voltage, $kV_{(Vpv)}$. If the solar panel is operating at a voltage larger than $V_{(Vref)}$ the error signal, V_{error}, controlling the PWM is increased thereby increasing the duty cycle of the main switch, M1. In doing so more current is drawn from the solar panel resulting in the solar panel voltage dropping. If the solar panel is operating at a voltage less than $V_{(Vref)}$ the error signal, V_{error}, is reduced resulting in less current being drawn from the solar panel. This results in the solar panel voltage increasing. In this manner the solar panel voltage is controlled to oscillate around the maximum power point voltage resulting in the maximum power being extracted from the solar panel. In this basic configuration the output voltage is not regulated and the system will always attempt to extract maximum power from the solar panel. If little current is drawn from the output of the SEPIC DC-DC converter, this circuit would still attempt to extract the maximum power from the solar panel, resulting in a large output voltage. Similarly, a load drawing a large current would result in a low output voltage.

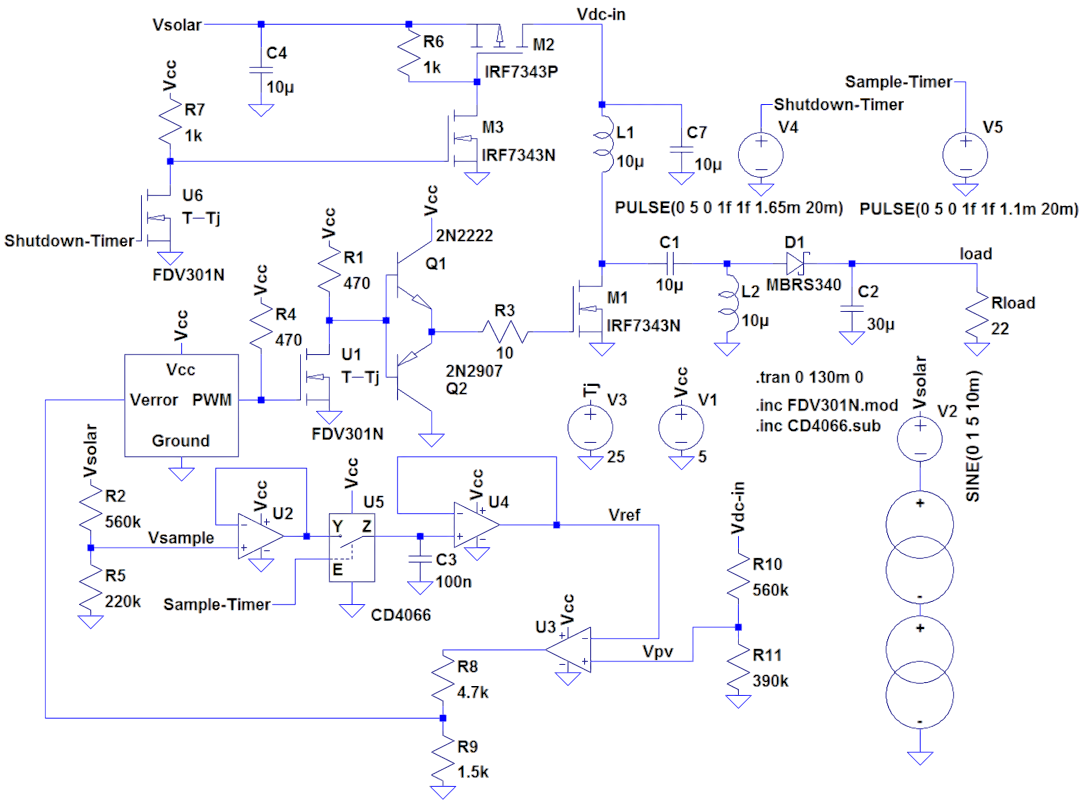

Figure 3.11: Fractional open-circuit MPPT schematic

In Figure 3.12 the solar panel voltage, $V(vsolar)$, is illustrated. As can be seen in Figure 3.12 the solar panel voltage is rising between sample periods, this is due to the sinusoidal source placed in series with the PV solar cells thereby emulating a change in PV solar cell temperature. It can be observed that the solar panel voltage is noticeably larger during the sample time, this larger voltage is the open-circuit solar panel voltage, V_{oc}. In Figure 3.12 it can also be seen that during the sampling time when the PWM is shut down and the solar panel is disconnected that output voltage,$V(load)$, begins to drop. When the solar panel is disconnected no power is transferred to the load and as such it is advantageous to sample the MPP voltage over the shortest possible time. In practice the battery would hold the output voltage during the sampling period.

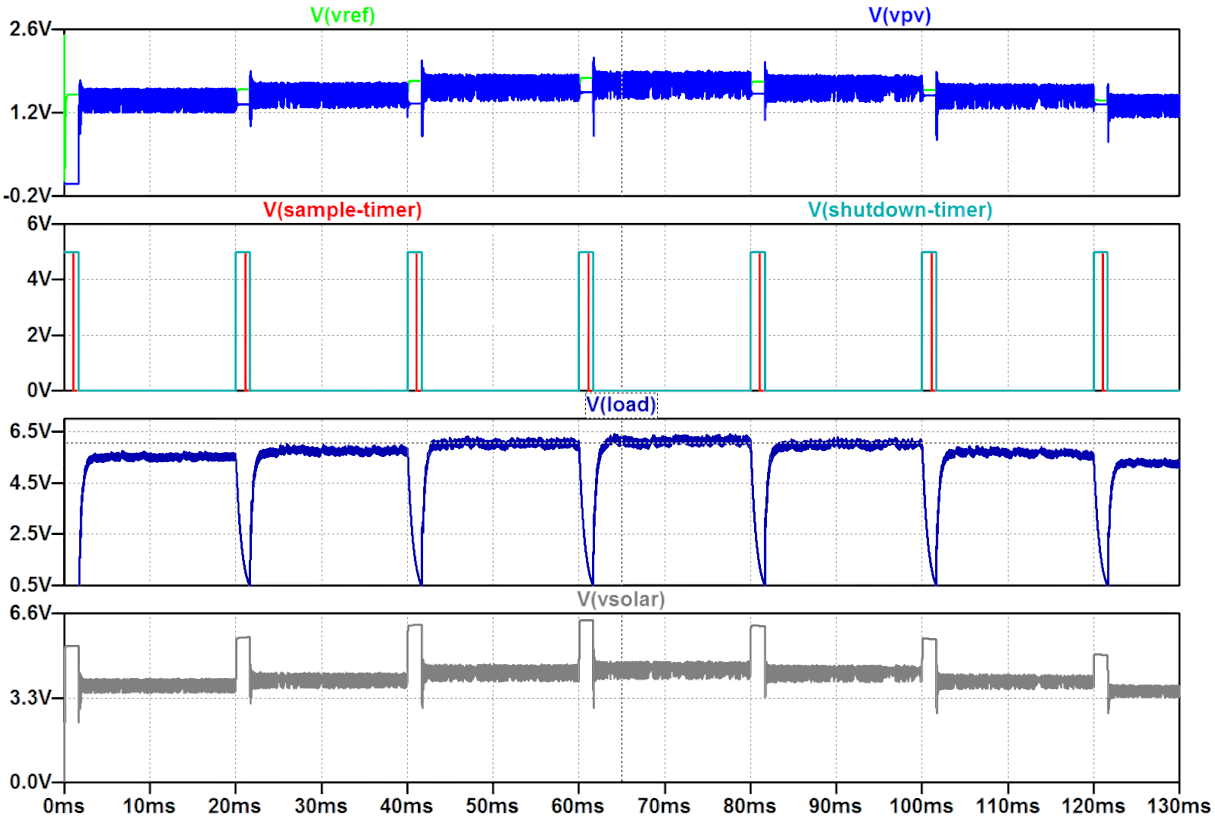

Figure 3.12: Fractional open-circuit MPPT simulation results

3.6 Battery charge/discharge regulator

The BCDR consists of all the battery protection components. These components include the battery over-discharge and over-charge protection circuitry. These elements will be discussed in a subsequent section along with the SEPIC DC-DC converter as its design is based upon the voltage regulation requirements of the BCR.

3.6.1 SEPIC DC-DC converter

The voltage-mode control loop controlling the SEPIC DC-DC converter regulates the battery bus voltage in order to prevent over-charging of the battery. The voltage control loop is only active when the EPS is in voltage regulation mode and attempts to keep the output voltage of the DC-DC converter regulated to 8.2 V. The DC-DC converter was designed using the design procedure set out by National Semiconductor (2008) and with the aid of MATLAB®. The script used in the design of the SEPIC DC-DC converter can be seen in Appendix C.1. The calculated values for the basic SEPIC DC-DC converter as seen in Figure 2.20 can be seen in Table 3.3. The chosen components for the SEPIC DC-DC converter can be seen in Table 3.4. The converter was designed for an input voltage range of 3V to 20V, this voltage allows for a PV solar panel to consist of a series or parallel combination of solar cells. Due to the design limitations of the SEPIC DC-DC converter, an attached solar panel cannot exceed 10 W per MPPT channel at any given time.

Two 10W solar panels may be connected to a single channel, provided only one of the channels is directly illuminated at any given time. Operating two solar panels on a single MPPT can be accomplished through mounting the solar panels on opposite sides of the satellite. This results in only one solar panel being illuminated directly by the Sun while the solar panel on the opposite side of the satellite is only exposed to albedo. This is the same "box" satellite configuration that GomSpace uses with their P-Series EPS GomSpace (2011:2–4). Exceeding the operating voltage or power rating of the MPPT may lead to the SEPIC DC-DC converter being damaged. The SPB9345136UH1 Li-poly battery cells from Enertech International were used merely for testing and are not space rated. These cells have a maximum charge voltage of 4.2 V per cell, a nominal operating voltage of 3.7 V and a capacity of 4.4 Ah. This equates to a battery with a nominal voltage of 7.4 V with a maximum charge voltage of 8.4 V (Enertech International, 2007). The designer chose to be cautious and charge the battery to a voltage of 8.2 V. This voltage was the output voltage used in the design of the SEPIC DC-DC converter's voltage control loop. The use of 8.2 V allows for some cell voltage imbalance to occur, as the design does not incorporate any form of cell balancing. These voltage specifications are comparable to the batteries and power systems developed by Clyde Space as seen in Clyde Space (2011), Strain (2010*a*) and Strain (2010*b*).

Table 3.3: Calculated SEPIC components

Component Designator	**Calculated Component Specifications**
L1	8.365 μH $\Delta I_L = 1.33$ A $I_{L(peak)} = 4.24$ A
L2	8.365 μH $\Delta I_L = 1.33$ A $I_{L(peak)} = 1.46$ A
Cs	10 μF 20 V Operating Voltage
Cout	22 μF ESR $<$ 35.9 $m\Omega$ 8.2 V Operating Voltage
D	28.2 V Reverse Voltage $I_{D(AVE)} = 1.22$ A

Table 3.4: Chosen SEPIC components

Component Designator	Chosen Component Specifications
L1	Shielded SMD 10 μH DCR $\approx$ 29 $m\Omega$ 5.4 A Maximum DC Current
L2	Shielded SMD 10 μH DCR $\approx$ 29 $m\Omega$ 5.4 A Maximum DC Current
Cs	Tantalum 10 μF ESR $\approx$ 270 $m\Omega$ 50 V Maximum Operating Voltage
Cout	Multilayer ceramic capacitors (MLCC) 3 x 10 μF in parallel ESR $\approx$ 15 $m\Omega$ each 25 V Maximum Operating Voltage
D	MBRS340T3 Schottky diode 40 V Maximum Reverse Voltage 3 A Maximum Average Forward Current 0.5 V Maximum Forward Voltage Drop

The chosen switching device for the SEPIC DC-DC converter was an IRF7343 MOSFET from International Rectifier driven by a Zetek Semiconductors ZXTC2062E6 medium power complementary pair of NPN and PNP transistors in the same configuration as the NPN and PNP push-pull circuit seen driving the main *switch*, the N-channel MOSFET of the IRF7343, in Figure 3.11. The designer chose to use a discrete driver to minimise component count and keep the circuit as simple as possible. The MOSFET was selected for its low on-state resistance, power handling capability and high junction operating temperature. The gate threshold voltage is low, 1V, on this logic level device, allowing the device to be switched on *hard* with a relatively low gate voltage. This MOSFET was driven with a gate voltage of approximately 5 V peak to peak from the ZXTC2062E6 push-pull pair.

The calculated power losses in the primary switching devices found in the SEPIC DC-DC converter can be seen in Table 3.5. These losses were calculated with the aid of the Matlab® script seen in Appendix C.1. These losses are for the converter under full-load with the minimum input voltage of 3 V and maximum input current while operating in CCM.

Table 3.5: 200 kHz SEPIC converter switching element power losses.

Switching Component	Power Dissipated
IRF7343	320 mW
MBRS340	610 mW

Driving the SEPIC DC-DC converter is the TL5001 based PWM incorporating an internal triangle wave oscillator with a minimum voltage of approximately 0.7 V and a maximum of approximately 1.3 V. The TL5001 has its own internal error amplifier and reference. This caused some problems as an independent error amplifier was required. The MPPT uses a scaled MPP voltage, V_{sample}, as a reference and compares this reference voltage to an instantaneous scaled solar panel voltage, V_{pv}. Hence, it was not possible to use a fixed voltage reference as the reference shifts with every MPP voltage sample. Using an external error amplifier allows for the internal reference voltage to be bypassed. This also allowed the circuitry required in sliding between MPPT and voltage regulation mode to be implemented.

Figure 3.13 illustrates the designed PWM circuit. JP1 and the attached passive circuit were used in testing the PWM. Closing the jumper, JP1, allows testing of the PWM through the adjustment of R5. During normal operation the jumper JP1 is left open allowing the PWM to be controlled by the error signal generated by the compensation amplifier used in the feedback system. The internal error amplifier was bypassed by connecting the error signal directly to the compensation (COMP) pin of the TL5001A and pulling the feedback (FB) pin to ground. An external error amplifier was used instead of the internal error amplifier along with a 2.5 V reference and a type 3 compensation network as seen in Figure 3.16 by the closed loop SEPIC DC-DC converter small-signal model.

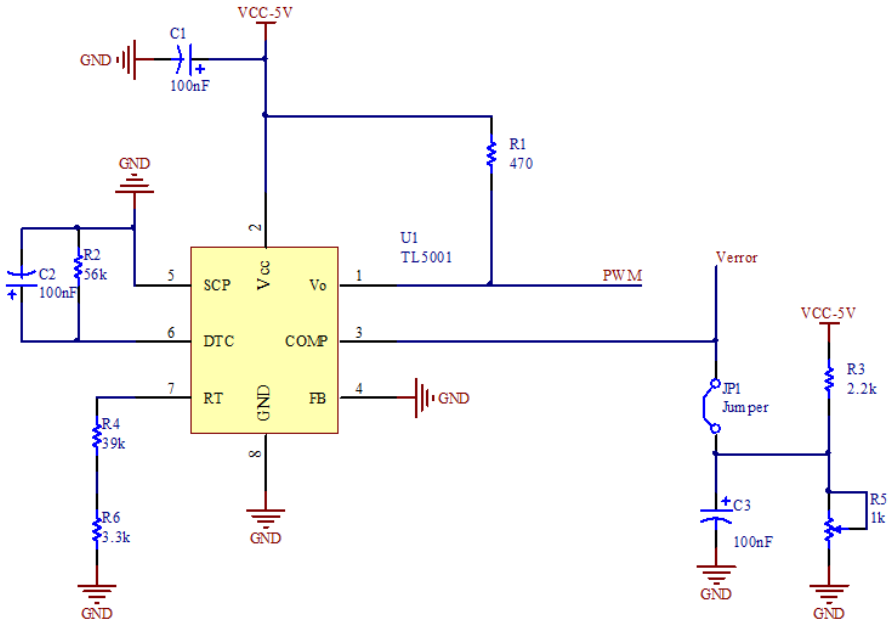

Figure 3.13: TL5001A PWM design

The oscillating frequency verses timing resistance graph found in the datasheet in conjunction with the application information supplied by Texas Instruments (2002:13) resulted in a value of ≈ 43 kΩ being selected for the timing resistor. This timing resistor is represented by R4 and R6 in Figure 3.13. The Short-circuit protection was disabled by pulling the short-circuit protection (SCP) pin of the TL5001A to ground. The use of a 100 nF in parallel to a 56 kΩ resistor

connected between the dead-time control (DTC) pin and ground allows for an approximate 90% duty-cycle (Texas Instruments, 2002:17). The duty-cycle had to be limited as at 100% duty the DC-DC converter would essentially short out the input voltage causing the DC-DC converter to fail.

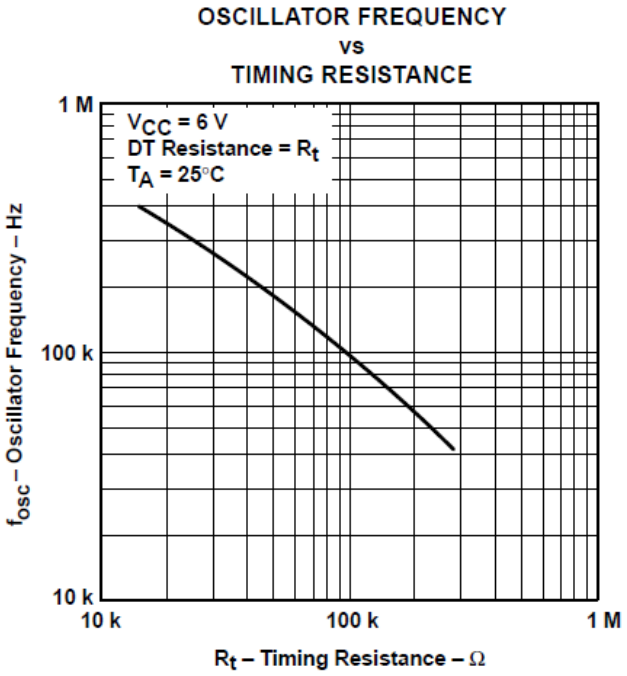

Figure 3.14: TL5001 timing resistor graph taken from Texas Instruments (2002:13)

3.6.2 Voltage control loop implementation

The voltage control loop regulates the output voltage of the SEPIC DC-DC converter to the constant charge voltage of the battery, approximately 8.2 V. This control loop is only active when the EPS is not in MPPT mode. It is critical that the SEPIC DC-DC converter be stable. This required the design of compensation to be used in the feedback loop. This designed compensation will be discussed in Section 3.6.3.

There are two different control signals required in controlling the SEPIC DC-DC converter, namely the voltage regulation control signal and the MPPT control signal. These signals both need to control the PWM signal, in order to increase or decrease the duty-cycle of the SEPIC DC-DC converter. The MPPT control mode of the SEPIC DC-DC converter needed to take priority over the voltage regulation mode during times of peak power demand and the voltage regulation mode needed to take priority when the battery went into constant-voltage charge mode. Figure 3.15 illustrates the simple solution to the problem.

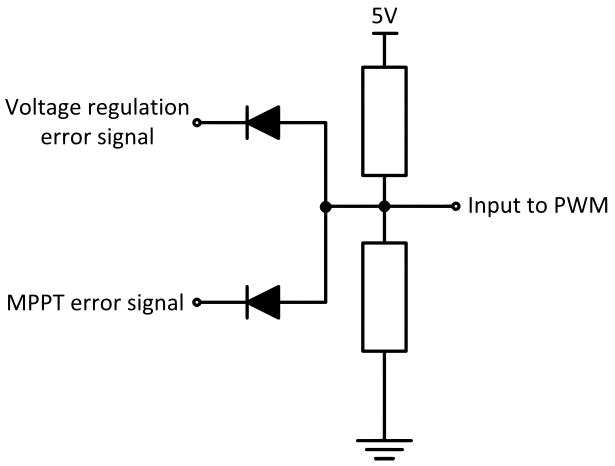

Figure 3.15: Error signal switch-over circuit

In Figure 3.15, the two error signals are connected to a simple voltage divider. This voltage divider limits the output voltage of the error signals to approximately 1.5 V, the upper limit of the TL5001A PWM IC. The diodes are pulled low by the error signals to control the PWM. If the error signals were to rise above 1.5 V, the diodes would go into reverse bias resulting in the input to the PWM circuit being held in place at 1.5 V. The lower of the two error signal voltages will pull their connected diode into forward bias, this results in the lower error signal voltage being passed onto the input of the PWM. Schottky diodes were needed for their low forward voltage drop. The resistors used in the voltage divider had sufficient resistance, as to keep the forward current of the diodes low and thus resulting in a low forward voltage drop. Essentially, whichever error signal requires the DC-DC converter to produce a lower output voltage, controls the duty-cycle produced by the TL5001A PWM IC.

3.6.3 Voltage regulation control

An external error amplifier was used along with the TL5001A PWM IC. Type 3 compensation was used in an attempt to shape the response of the SEPIC DC-DC converter bringing about a stable system capable of handling a wide range of input voltages and varying loads. A simple voltage-mode control scheme was employed due to its simplicity in hardware implementation.

The small-signal model used in the design of the SEPIC DC-DC converter can be seen in Figure 3.16 and was derived from Basso (2008:209–210). The component values for the SEPIC DC-DC converter were calculated through the MATLAB® script seen in Appendix C.1. The component values for the power stage in Figure 3.16 where physically measured from the chosen components with an impedance analyser. The voltage-mode control PWM switch model employed in the small-signal model was originally developed for PSpice by Basso (2008) but was later redeveloped by Charles Denton for LTSpice® and employed in the design of the SEPIC DC-DC converter (Basso, 2012). The PWM is modelled as a gain stage and is proportional to the triangular waveform within the PWM. The error amplifier was modelled as the actual Op Amp used. The highest voltage limit is set to 1.5 V as this is the limit imposed by the TL5001

and by the voltage feed-point between MPPT error signal and the voltage regulation error signal. The small-signal model used has the capability of operating in both CCM and DCM.

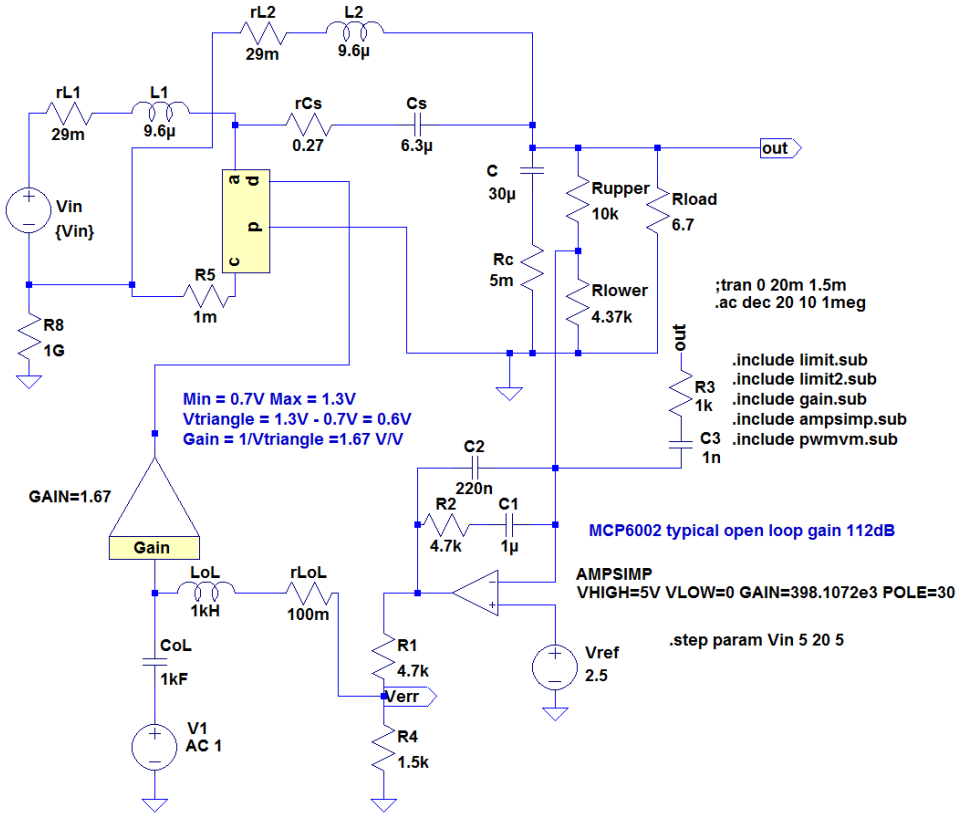

Figure 3.16: Small-signal model of designed SEPIC DC-DC converter.

As can be seen in Figure 3.17 the system could become unstable upon closing the loop if compensation was not employed. This is due to a 180° phase shift brought on by the power stage of the converter while still having a gain of over 0 dB. This instability is present with all simulated supply voltages and is due to the resonance peaks located at approximately 10 kHz and 15 kHz. Closing the feedback loop under such a condition would produce positive feedback and cause possible oscillation of the output of the converter. Figure 3.17 is the response of the duty-cycle to output voltage of the SEPIC DC-DC converter operating at its maximum power handling capability of 10 W and with a supply voltage of 5 V, 10 V, 15 V and 20 V.

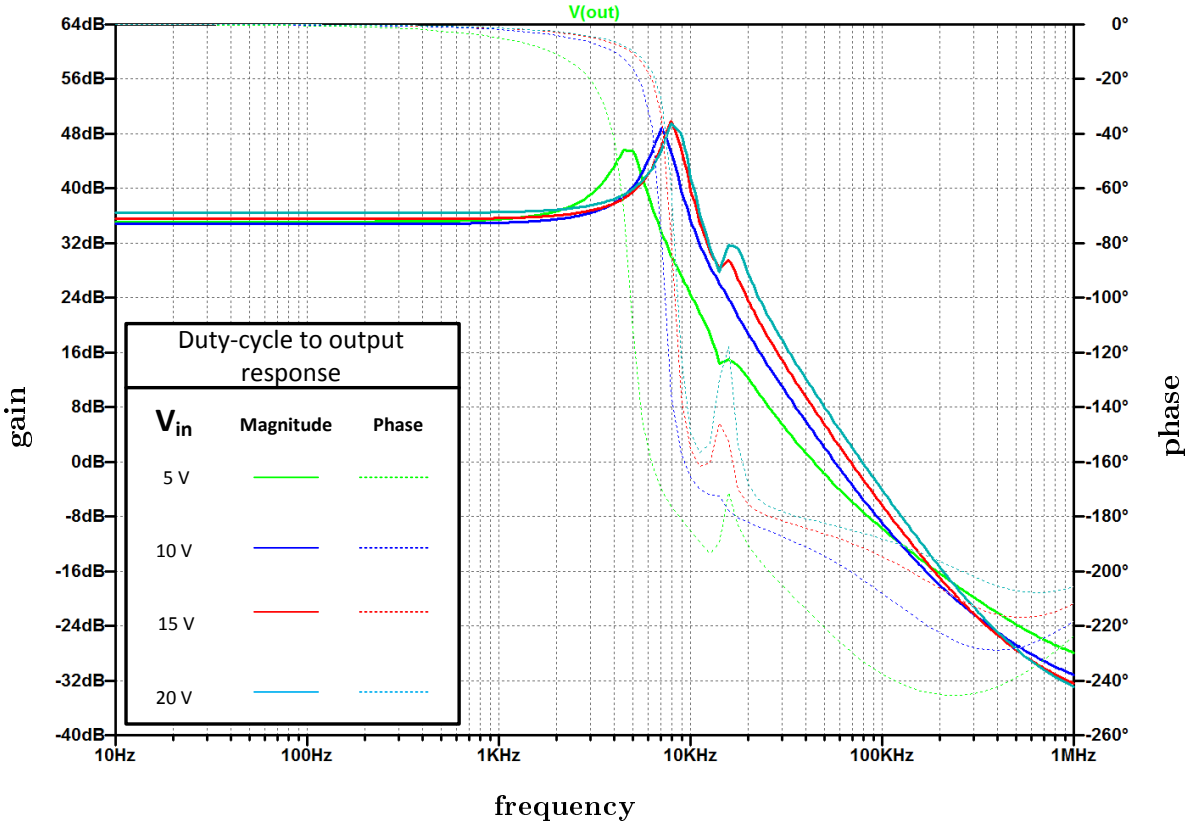

Figure 3.17: SEPIC DC-DC converter duty-cycle to output response (100% power)

Figure 3.18 is the response of the duty-cycle to output voltage of the SEPIC DC-DC converter operating at 50% of its maximum power handling capability with a supply voltage of 5 V, 10 V, 15 V and 20 V. It can be seen in Figure 3.18 that the duty-cycle to output voltage response of the converter with a supply voltage of 10 V, 15 V and 20 V differs significantly to the response of the duty-cycle to output voltage of the converter with a 5 V supply voltage. The duty-cycle to output voltage response of the converter with a 10 V, 15 V and 20 V supply voltage illustrates the response of the converter operating in DCM, while the duty-cycle to output voltage response of converter with a 5 V supply voltage illustrates the response of the converter operating under CCM.

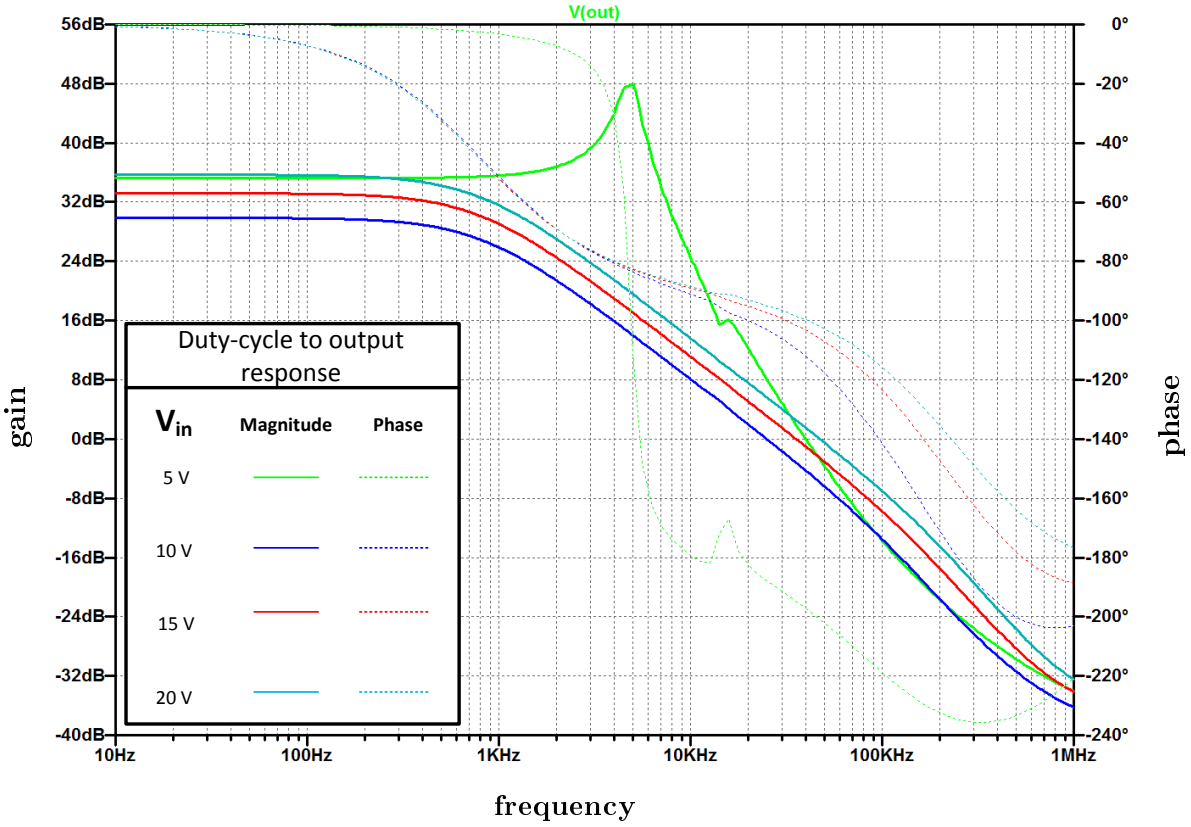

Figure 3.18: SEPIC DC-DC converter duty-cycle to output response (50% power)

The phase shift brought on by the power stage reaches $-180°$ as seen in Figure 3.17 and Figure 3.18, therefore type 3 compensation was chosen as a means to improve the stability of the closed loop system. The K Factor method as explained by Basso (2008:263–277) was used in calculating the required component values for this type of compensation.

The calculated component values can be seen in Table 3.6, the script used in calculating these values can be seen in Appendix C.2. The designed cut-off frequency was chosen to be 45 kHz. This was due the suggestion by (Basso, 2008:250) to place the crossover frequency at, at least three times the resonant frequency. The highest resonant frequency is located at ≈15 kHz and hence 45 kHz was chosen.

Table 3.6: Calculated compensation components.

Designator	Calculated Value	Selected Value
Rupper	10 kΩ	10 kΩ
R2	13.3975 Ω	10 Ω
R3	176.3809 Ω	220 Ω
C1	2.0052 μF	2.2 μF
C2	35.3678 nF	33 nF
C3	2.6399 nF	2.7 nF

Figure 3.19 shows the closed loop response of the SEPIC DC-DC converter at 100% of its rated output power. The simulated closed loop system response over the input voltage range and at 100% of the converter's rated output power had a worst case phase margin, PM, of approximately 100° at 1 kHz and a worst case gain margin, GM, of 3 dB at 5 kHz, 7 kHz and 8 kHz. The lack of gain margin is later remedied in Section 4.7 through a redesign of the SEPIC DC-DC converter.

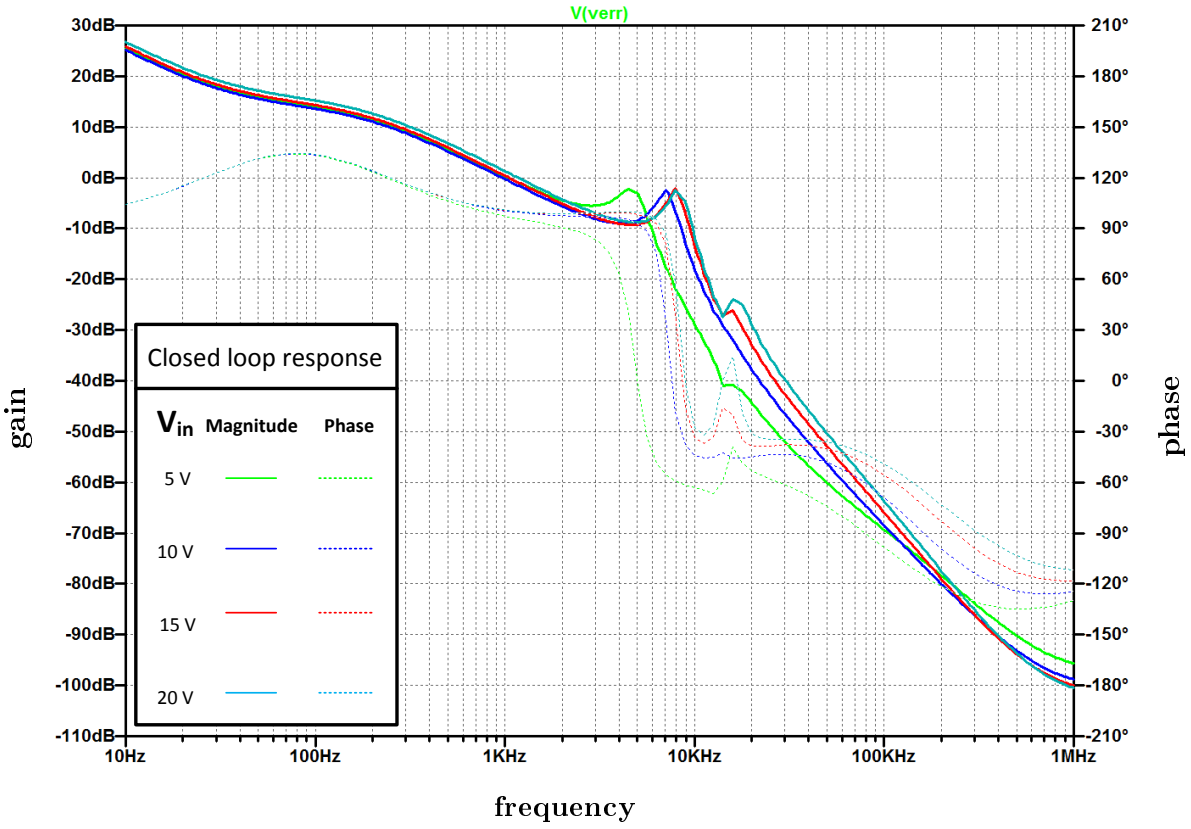

Figure 3.19: SEPIC DC-DC converter closed loop response with selected values (100% power)

Figure 4.22 shows the closed loop response of the converter at 50% of its rated output power. The simulated closed loop system response over the input voltage range and at 50% of the converter's rated output power had a worst case phase margin, PM, of 80° at 450 Hz with minimal gain margin, GM, at 4 kHz. The minimal gain margin could cause conditional stability issues with the SEPIC DC-DC converter. This issue is later remedied in Section 4.7 through a redesign of the SEPIC DC-DC converter.

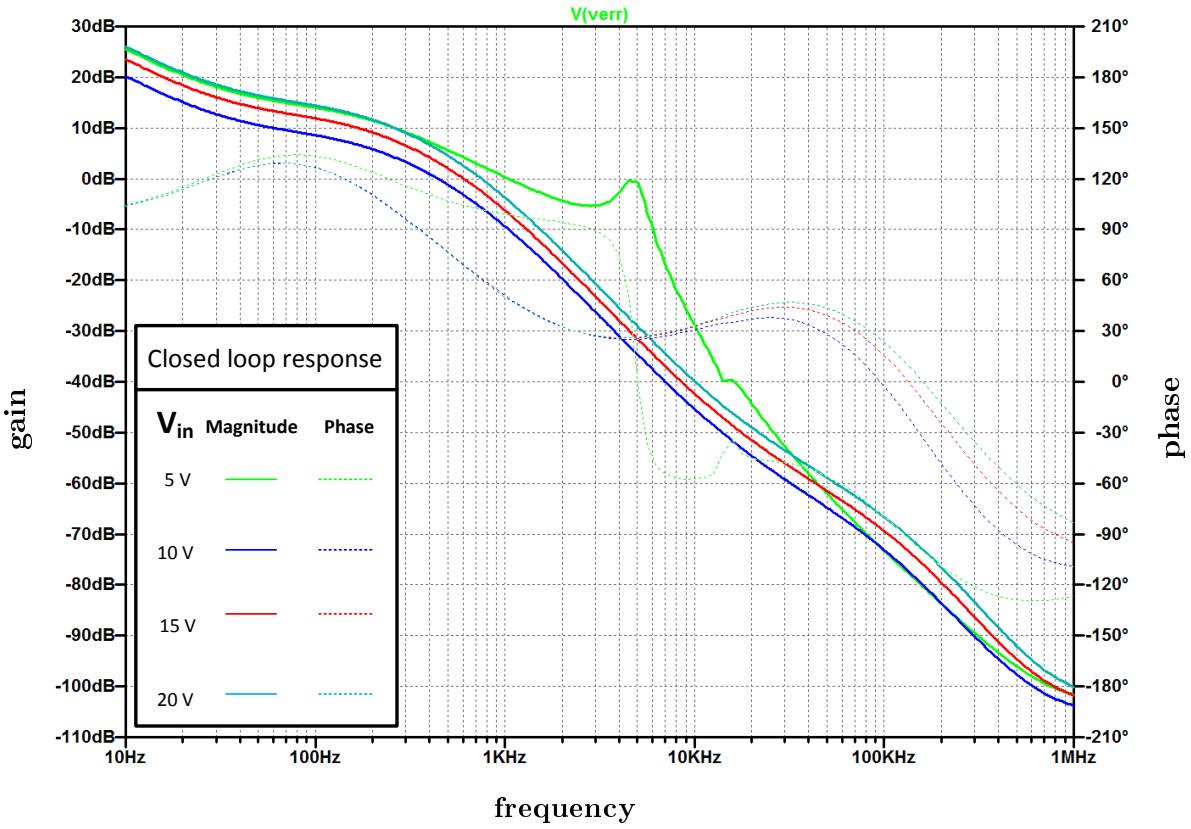

Figure 3.20: SEPIC DC-DC converter closed loop response with selected values (50% power)

The simulated cut-off frequency was lower than expected but acceptable as a high frequency response was not required. The design has excessive PM, but this is also acceptable as the response of the system did not need to be fast as the primary goal of the converter was to charge the Li-poly battery. The battery would serve as a large reservoir of energy aiding the converter in the supplying of current to loads.

3.6.4 Battery under-voltage protection

Battery under-voltage protection assists in increasing the longevity of the Li-poly battery. The minimum operating voltage per cell of a Li-poly battery is approximately 3 V, as such a two cell battery would have a minimum operating voltage of 6V (see Section 2.4.2.2). The nominal operating voltage per cell of the Li-poly battery is 3.7 V, resulting in the two cell battery having a nominal operating voltage of 7.4 V. The battery under-voltage protection consists of a simple operational amplifier circuit configured as a Schmitt trigger, with the upper and lower limits designed approximately to these limits. If the battery voltage drops below the lower threshold of approximately 6.2 V the EPS loads are disconnected until the battery returns to its nominal voltage due to charging from the solar array. The 200 mV headroom above 6 V allows for a slight voltage imbalance in the two battery cells to occur and gives the housekeeping LDO extra headroom to prevent drop-out from occurring. Once the battery is approximately at the

rated nominal voltage of 7.4 V, the EPS loads are reconnected to the system. If enough power is available from the solar array, the battery will continue to charge until the constant charge voltage limit of 8.2 V is reached.

The battery under-voltage protection circuit can be seen in Figure 3.21. The P-Channel MOSFETs within Q3 and Q4 are connected in parallel thereby sharing the current supplied to the loads. Connecting the P-Channel MOSFETs in this manner reduces the losses in each MOSFET. The two N-Channel MOSFETs are cascaded in order to form a level shift circuit required in driving the P-Channel MOSFETs. In the prototype circuit R30 was later replaced with the TL431 voltage reference IC. R24 and R26 scale the output voltage from the SEPIC DC-DC converter to an acceptable level for the MCP6002 operational amplifiers and to a voltage that coincides with the threshold voltage levels for the Schmitt trigger.

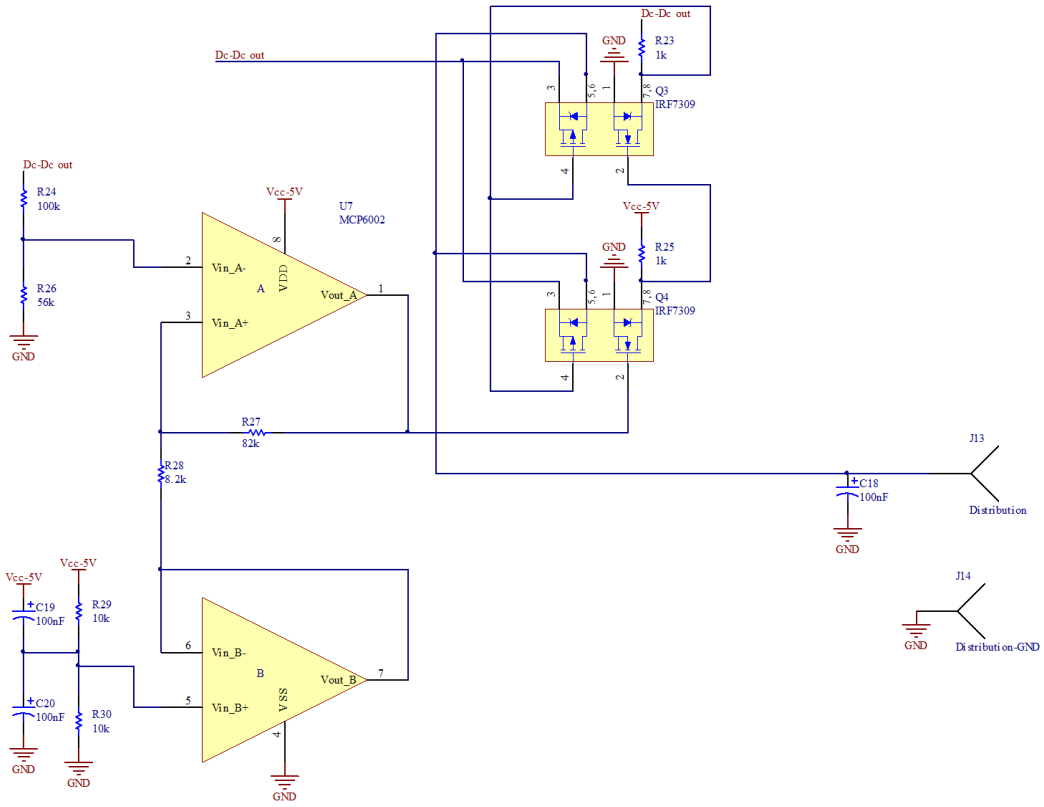

Figure 3.21: Hysteresis based battery under-voltage protection design

The Schmitt trigger operate with a 5V single supply and a reference voltage of 2.5 V. The operational amplifier used can supply an output voltage that is extremely close to the supply voltage. This causes the input voltage range for the Schmitt trigger to fall symmetrically around 2.5 V. Due to the symmetry of the circuit the reference voltage of 2.5 V can be treated as a virtual ground potential for simplicity. The designed upper and lower voltage thresholds for the battery under-voltage protection are designed for 7.4 V and 6.2 V respectively. It is required to scale the mean voltage point between these two voltages, 6.8 V, such that it coincides with the 2.5 V reference voltage used by the Schmitt trigger. The scaling was done through the use of R24 and R26 and is derived using Equation 3.6.1.

$$V_{R26} = V_{DC-DC(out)} \cdot \left(\frac{R26}{R26 + R24} \right) \tag{3.6.1}$$

Using Equation 3.6.1 and using a 100 kΩ resistor for R24 a value for R26 can be calculated as seen in Equation 3.6.2

$$\begin{aligned} V_{DC-DC(out)} =& V_{R26} \cdot \left(\frac{R24 + R26}{R26} \right) \\ \therefore R26 =& \frac{R24}{\left(\frac{V_{DC-DC(out)}}{V_{R26}} \right) - 1} \\ =& \frac{100k\Omega}{\left(\frac{6.8V}{2.5V} \right) - 1} \\ =& 58.1395k\Omega \ (56k\Omega) \end{aligned} \tag{3.6.2}$$

The difference between the unscaled mean voltage, 6.8 V and the unscaled threshold voltages is $\pm 0.6\ V$. Due to the scaling brought on by R24 and R25 this difference is scaled as seen in Equation 3.6.3. The threshold voltages are therefore 0.2154 V greater than and less than the 2.5 V reference voltage. Using the virtual ground this equates to a voltage of $\pm 0.2154\ V$ for the threshold voltages seen at the negative input of the operational amplifier.

$$\begin{aligned} V_{in-} &= \pm\, 0.6V \cdot \left(\frac{R26}{R24 + R26} \right) \\ &= \pm\, 0.6V \cdot \left(\frac{56k\Omega}{100k\Omega + 56k\Omega} \right) \\ &= 0.2154V \end{aligned} \tag{3.6.3}$$

The voltage located at the positive input of the operational amplifier defines the trigger level voltages of the Schmitt trigger. The approximate maximum and minimum output voltage of the operational amplifier is 5 V and 0 V respectively in reference to the true ground potential of the circuit, or 2.5 V and -2.5 V with reference to the virtual ground produced by the reference voltage. This leads to Equation 3.6.4 if referring to the virtual ground as a reference, where V_{out} is the output voltage of the operational amplifier.

$$V_{trigger} = V_{out} \cdot \left(\frac{R28}{R27 + R28} \right) \tag{3.6.4}$$

Manipulating Equation 3.6.4 and selecting a value of $82k\Omega$ for R27 the value for R28 can be calculated as seen in Equation 3.6.5.

$$\begin{aligned} R28 =& \frac{R27}{1 - \frac{V_{trigger}}{Vout}} \cdot \left(\frac{V_{trigger}}{V_{out}} \right) \\ R28 =& \frac{82k\Omega}{1 - \frac{0.2154V}{2.5V}} \cdot \left(\frac{0.2154V}{2.5V} \right) \\ =& 7.7312k\Omega \ (8.2k\Omega) \end{aligned} \tag{3.6.5}$$

3.6.5 Battery over-charge protection

The battery over-charge protection was initially designed to shut down the PWM of the SEPIC DC-DC converter in the event that a problem was encountered with the voltage regulation capability of the converter or in the event that the current used in charging the battery was excessive. This protection was based around a MAX4374FEUB+ current amplifier IC. The SPB9345136UH1 cells used in the battery have a maximum charge current of 8.8 A or 2.0C and a standard charge current of 4.4 A or 1.0C (Enertech International, 2007).

The SEPIC DC-DC converter has a maximum rating of 10 W and a designed minimum output voltage of approximately 6 V due to the battery under-voltage protection. In a satellite application, three MPPT circuits would be employed. The use of three MPPT circuits allows for the possibility of 30 W to be delivered to the battery, with an ideal DC-DC converter having no losses and the EPS powering no loads. Under this extreme and unrealistic case, the total battery charge current would be approximately 5 A. Depending on the batteries used in the CubeSat mission, the over-current protection may be required, especially if a C-rate below 1.0C is to be achieved during the fast charge stage of charging the battery (see Section 2.4.2.3). It is recommended to set the charge limit of the battery to 1.0C if the power supplied by the PV solar panel is large enough to charge the battery at an excessive rate. The designed prototype EPS is unable to reach 1.0C and as such a current limit of 300 mA (0.07C) was selected for testing. This protection, once tested, could be disabled as having this protection in place would significantly increase the time the battery takes to charge.

The battery over-voltage protection should only engage if the voltage regulation of the SEPIC DC-DC converter drifts due to ageing or damage. This form of protection abruptly shuts down the SEPIC DC-DC converter in the event that the battery voltage exceeds 8.6 V. This voltage was chosen as 4.3 V and is the upper limit, allowing for normal operation of Li-ion based cells (see Section 2.4.2.2). In the prototype, this limit was made adjustable allowing the voltage threshold to be finely tuned. In a final design, it is recommended that fixed values are used, due to problems that may occur during launch due to vibration (see Section 2.2.3).

Figure 3.22 shows the schematic for the designed protection. The batteries used in testing the prototype have a 1 C rating of 4400 mA. This was significantly more than the single channel MPPT could deliver and as such testing at this rate was impossible. To test this form of protection the same over-current protection design as seen in Section 3.7 was utilised. The current limit of the design was set to 300 mA as a proof of concept for missions that may require such protection. The over-current protection was later disabled as it was not required for this prototype design.

The selected MAX4374FEUB+ IC measures the voltage across R8, amplifies this voltage by 50 V/V and outputs this voltage to pin 2 (Out). This output voltage can then be compared to an internal 0.6 V reference if desired. The voltage measured across R8 is directly proportional to the current flowing through R8, and as such the output of this IC is directly related to the current measured. Selecting the appropriate resistor values for R15 and R17 and utilising one of the internal open-collector output comparators allowed the PWM error signal to be pulled low in

the event too much current flowed through R8. The design incorporated over-voltage protection through a similar means, except without the use of the internal amplifier. The output voltage of the DC-DC converter is scaled and measured against the internal 0.6 V reference. In the event that this scaled voltage exceeds 0.6 V the PWM output signal is grounded. The reset pin was pulled to ground thereby disabling the latching capability of the current amplifier IC. The over-voltage protection can be altered by adjusting R7. The chosen over-voltage protection limit for the design was 8.6 V as this voltage is higher than the voltage regulation limit and coincides with the maximum cell voltage of 4.3 V per cell for Li-ion battery chemistries.

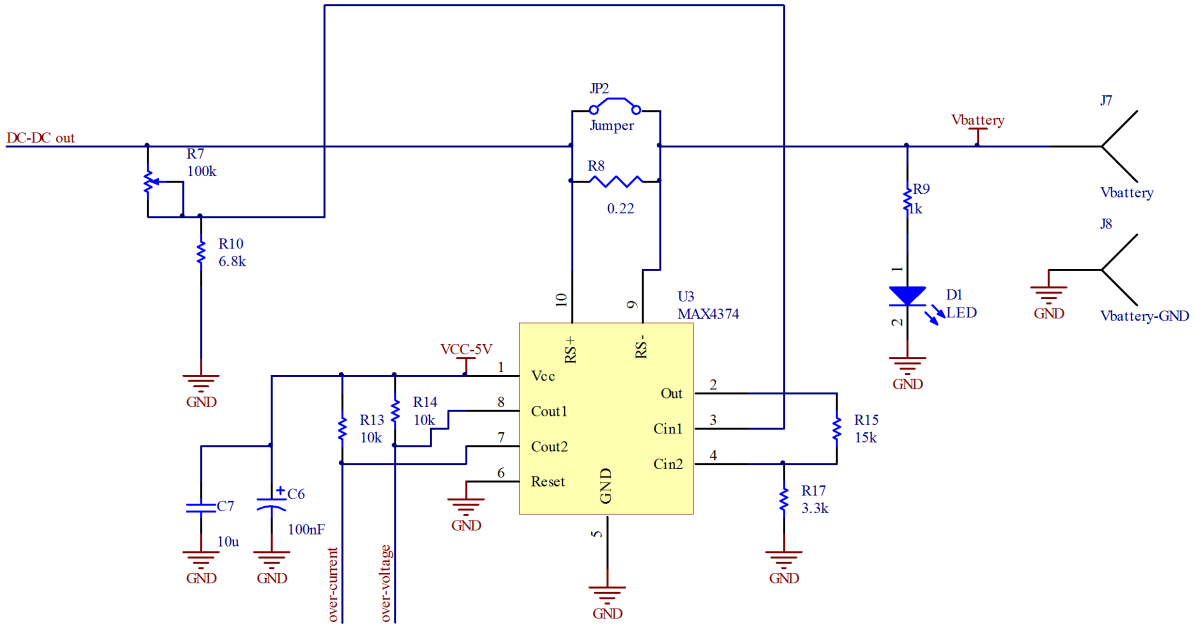

Figure 3.22: MAX4374 over-current design

A fixed value for R7 can be calculated through the use of Equation 3.6.6 bearing in mind that the comparator compares the input voltage to a reference voltage of 0.6 V. This resulted in the selection of a $100k\Omega$ potentiometer for R7.

$$\begin{aligned} V_{R10} &= V_{(DC-DCout)} \cdot \left(\frac{R10}{R7 + R10} \right) \\ \therefore R7 &= R10 \cdot \left(\frac{V_{(DC-DCout)}}{V_{R10}} - 1 \right) \\ &= 6.8k\Omega \cdot \left(\frac{8.6V}{0.6V} - 1 \right) \\ &= 90.67k\Omega \end{aligned} \tag{3.6.6}$$

The MAX4374FEUB+ has a voltage gain of 50 V/V and allows for a maximum differential voltage across the sense resistor, located between RS+ and RS-, of ± 0.3 V. Closing JP2 effectively shorts out R8 and allows the over-current protection circuit to be bypassed if necessary. Using a sense resistor of 0.22 Ω brings about a differential voltage of 66 mV at 300 mA, well

within the ± 300 mV absolute maximum voltage rating. At the absolute maximum differential voltage of ± 300 mV across the sense resistor a maximum current of 1.3 A can flow. If a larger current is required a smaller resistor value for R8 is required.

At a 300 mA current limit and having a differential voltage of 66 mV the MAX4374FEUB+ produces an output voltage of 3.3 V (66 mV × 50 V/V = 3.3 V) at pin 2 (Out). The internal comparators are connected to a 0.6 V reference voltage, this requires the output voltage of 3.3 V to be attenuated to 0.6 V. This is done through the use of R15 and R17 in Figure 3.22

3.7 Distribution

The distribution consists of a simple over-current latch, based around a MAX4374FEUB+ IC and was designed to "trip" when a current exceeding 300mA was supplied to a load. This current limit can be pre-set to a required current limit depending on the required maximum current rating of the load. Setting the current limit is done through the replacement of two resistors. This latch is reset by the same timer as the MPPT and as such any adjustment of the MPPT interval directly alters the period between two consecutive resets of the latch. During the period at which the reset pin on the MAX4374FEUB+ is low, equating to a reset of the latch, the current limiting operation of the circuit is not operational. After this period, if the load draws more than the set limit of 300mA, the circuit will disconnect the load from the EPS. Due to the operation of the latch, if a load is continuously drawing excessive current, the EPS will only be delivering power to the load for the short duration in which the MAX4374FEUB+ is reset. During the remaining period in which the MAX4374FEUB+ is not reset, the load will be disconnected from the EPS. Depending on the final CubeSat configuration the distribution might consist of multiple current latches connected to different output rail voltages or even individual payloads.

The over-current protection circuitry in the distribution was designed to disconnect attached loads when a current exceeding 300 mA was supplied. The MAX4374FEUB+ has a voltage gain of 50 V/V and allows for a maximum differential voltage across the sense resistor, located between RS+ and RS-, of ± 0.3 V. The basic distribution circuit can be seen in Figure 3.23. Closing JP1 allows the protection circuit to be bypassed if necessary.

JP2 and JP3 were used during testing and were used to emulate timing signals if the distribution was to be tested separately from the control circuit board.

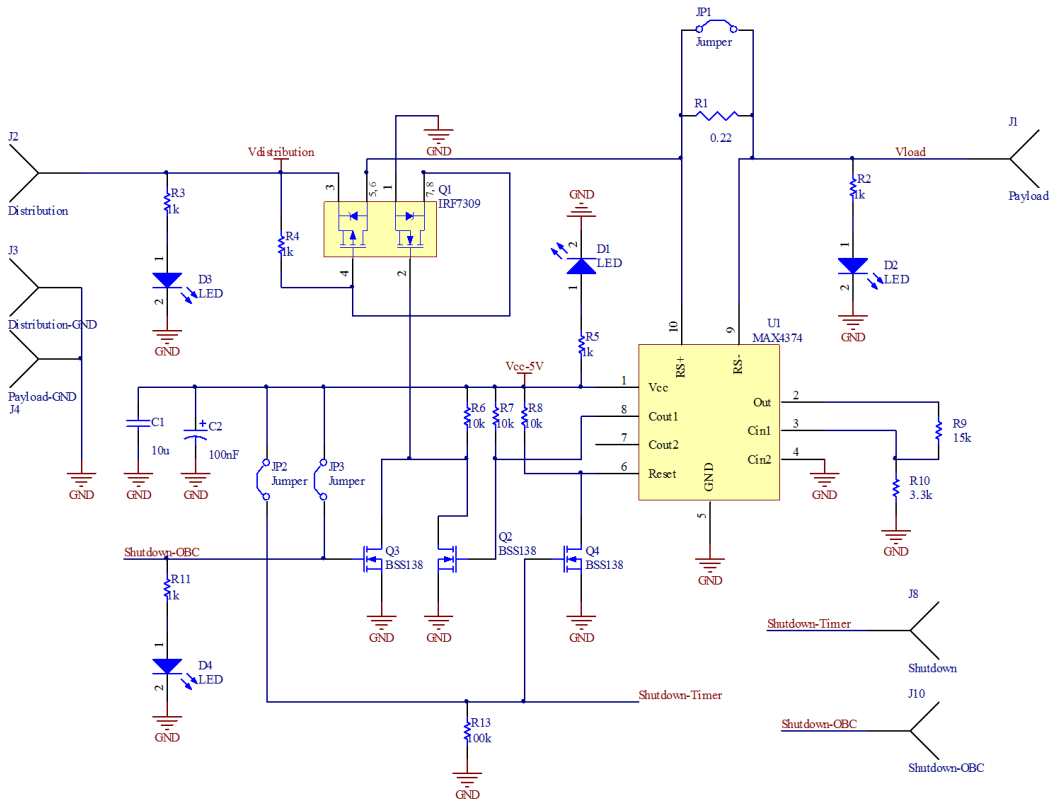

Figure 3.23: MAX4374 over-current design

Using a sense resistor of 0.22 Ω brings about a differential voltage of 66 mV at 300 mA, well within the ± 300 mV absolute maximum voltage rating. At the absolute maximum differential voltage of ± 300 mV across the sense resistor a maximum current of 1.3 A can be supplied to loads. The over-current protection can be bypassed through the use of JP1 which effectively shorts out the shunt resistor.

At the 300 mA current limit and having a differential voltage of 66 mV the MAX4374FEUB+ produces an output voltage of 3.3 V (66 mV × 50 V/V = 3.3 V). The internal comparators are connected to a 0.6 V reference voltage, this requires the output voltage of 3.3 V to be attenuated to 0.6 V. This is done through the use of R9 and R10 in Figure 3.23.

3.8 Summary

This chapter discussed the design considerations and thought processes involved in the design of the prototype EPS. The designed prototype EPS consisted of a single channel SEPIC DC-DC converter based FOCV MPPT, with over- and under-voltage battery protection, and over-current protection.

The design of the various EPS sections were discussed in great detail. These sections related to the PV solar panel model, housekeeping, maximum power point tracker, battery charge/discharge regulator and distribution circuitry.

Chapter 4

Experimental evaluation

4.1 Introduction

The prototype EPS consists of three prototype circuit boards seen in Figure 4.1. The indicated areas of the prototype test boards can be seen in Table 4.1. Once the construction of the various boards was completed, testing commenced. This section covers the results of these tests, the testing procedures and the modifications that were required in order to improve the performance of the EPS. This section ends with the results of the final testing. During all testing with the exception of the final tests, a DC bench power supply was used in place of the PV solar panel.

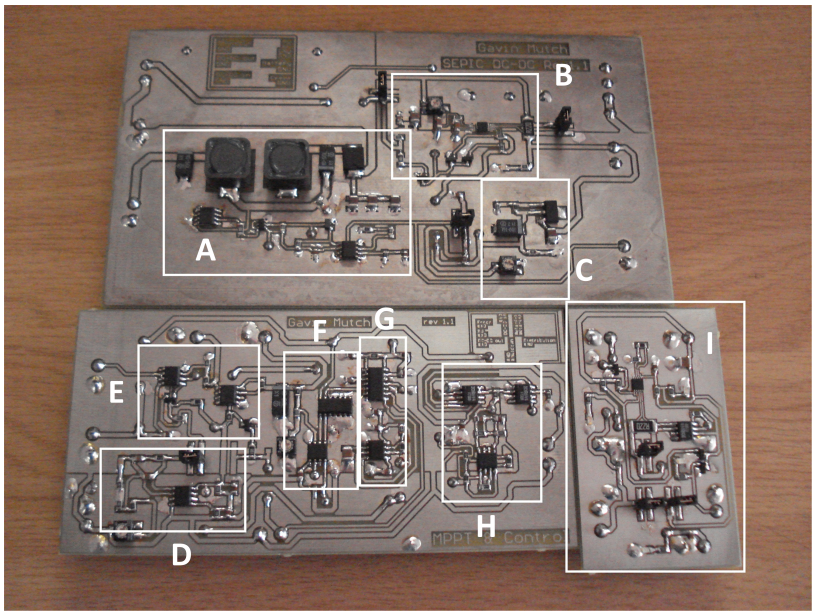

Figure 4.1: Photograph of the three prototype test circuits.

Table 4.1: Indicated areas of the prototype test boards

Indicated Area	Description
A	SEPIC DC-DC converter.
B	Battery over-voltage and over-current protection.
C	5V housekeeping voltage regulator.
D	SEPIC DC-DC converter voltage control loop compensator.
E	MPPT excluding F and G.
F	Sample and hold.
G	555 and 556 timers.
H	Battery under-voltage protection including MOSFET switches.
I	Distribution (Current latched switch circuit).

4.2 Photovoltaic solar panel

The PV solar panel was only used towards the end of the testing of the EPS prototype circuit. The PV solar panel consisted of a series array of 10 silicon based solar cells each having an open-circuit voltage of approximately 0.5 V, giving the solar panel a total V_{oc} of approximately 5 V. The initial I-V measurements required in locating V_{mpp} of the PV solar panel can be seen in Appendix B. The solar panel was placed directly in front of a light box, which in turn was connected to a DC power supply allowing for the intensity of the light illuminating the solar panel to be adjusted. Figure 4.2 is a photograph of the PV solar panel used during testing along with the light box used in illuminating the cells. Adjusting the DC power supply allowed for testing of the MPPT, as the light box would change the intensity of the light illuminating the PV solar cells as well as the temperature of the cells. More accurate measurement of the performance of the solar panel were recorded with the use of an oscilloscope and a variable resistor connected to the PV solar panel as a load. This test rig allowed the power from the PV solar panel to be visually monitored with the aid of the oscilloscope's math function as the load was adjusted. This made locating the maximum power point relatively easy. Disconnecting the PV solar panel broke the circuit, allowing for V_{oc} to be measured and the MPP voltage factor, M_v, to be calculated.

Though M_v did shift slightly with different light intensities and temperatures, the maximum power point voltage, V_{mpp}, was found to lie at approximately 75% of the open-circuit voltage, V_{oc}, leading to $M_v \approx 0.75$.

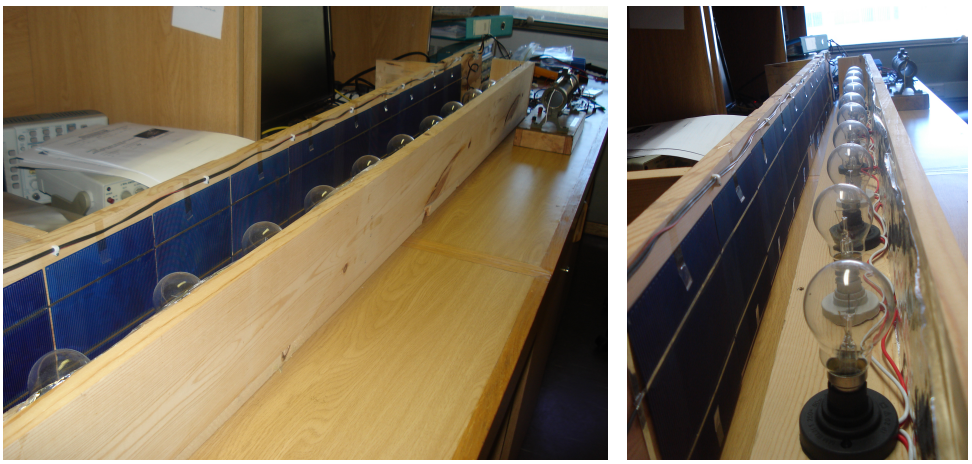

Figure 4.2: PV solar panel used during testing

4.3 Housekeeping

The housekeeping circuitry, though simple, is a highly important part of the prototype EPS. The EPS will function with inaccurate timers but will cease to function if the timers fail to operate or if the supplied voltage from the LDO is outside the operating voltages of the control circuitry within the EPS. The lowest recommended voltage that the control circuitry can operate at is 4.5 V, while the maximum recommended voltage is 6.0 V. The accuracy of the reference voltages are important, as a drift in the voltage of these reference voltage ICs could cause the output voltage of the SEPIC DC-DC converter to drift, resulting in batteries that are over or under-charged. A reference voltage IC was used in setting the mid-point voltage of the hysteresis voltage band in which the battery operates. A drift in this voltage could result in the under-voltage battery protection not engaging at the correct voltage. Tests are done in Sections 4.3.1, 4.3.2 and 4.3.3. These tests verify that the LDO, reference voltage ICs and timers are functioning acceptably for the EPS.

4.3.1 Low dropout linear regulator

The LDO was tested within the designed battery voltage range of 6.2 V to 8.2 V and functioned better than expected. All sections of the EPS were connected, allowing the control circuitry to act as a load to the LDO. A bench power supply was connected in place of the battery, with the solar panel input and EPS output disconnected. The minimum drop-out voltage, the difference in potential between the input voltage and output voltage, is typically 1.10 V and has a maximum potential difference of 1.20 V at an output of 100 mA (National Semiconductor, 2006). The output voltage of the LM1117 LDO was measured during normal operating conditions and was proven to operate below the expected minimum input voltage, 6.2 V, as can be seen in Table 4.2. As can be seen in Table 4.2, the LDO is still capable of supplying approximately 5 V with an input voltage of 6.033 V. When an input voltage lower than this was used, the output voltage would drop dramatically illustrating that the dropout voltage for the LDO in this circuit was approximately 6 V. Though the output voltage regulation at this low input voltage is sufficient, the circuit was never expected to operate under such conditions as the lowest designed battery

voltage is 6.2 V. The LDO drives the control circuitry for the entire EPS, but supplies no power to external loads. As the battery voltage is never expected to drop below 6.2 V, the LDO is expected to function effectively under all conditions.

Table 4.2: Measured LM1117 LDO input and output voltages.

Input voltage	Output voltage
6.118 V	5.014 V
8.209 V	5.019 V
6.033 V	4.989 V

4.3.2 Timers

The timers were tested with a bench power supply connected to the battery input of the EPS, and with the solar panel input and EPS output disconnected. The timers operate the S&H circuitry required for the operation of the MPPT. Though the period between samples is unimportant to the operation of the circuit, the timing does have an effect on the efficiency of the MPPT and how quickly the MPPT responds to a change in the maximum power point voltage. The timers are designed to supply two pulses with a period of 2.5 s. These pulses are used in the operation of the MPPT and the distribution. These two pulses are triggered simultaneously and have designed pulse widths of 15 ms and 30 ms respectively. The 15 ms pulse triggers the sampling of the S&H circuit while the 30 ms pulse is used in disconnecting the PV solar panel from the MPPT used in measuring the open-circuit voltage of the PV solar panel as well as triggering a reset of the current latch used in the distribution section of the EPS. Figure 4.3 shows the measured period of 1.7 s between each timed pulse. Figure 4.4 shows the pulse widths of the two timer output voltage signals. These pulse widths were measured to be approximately 30 ms and 20 ms respectively.

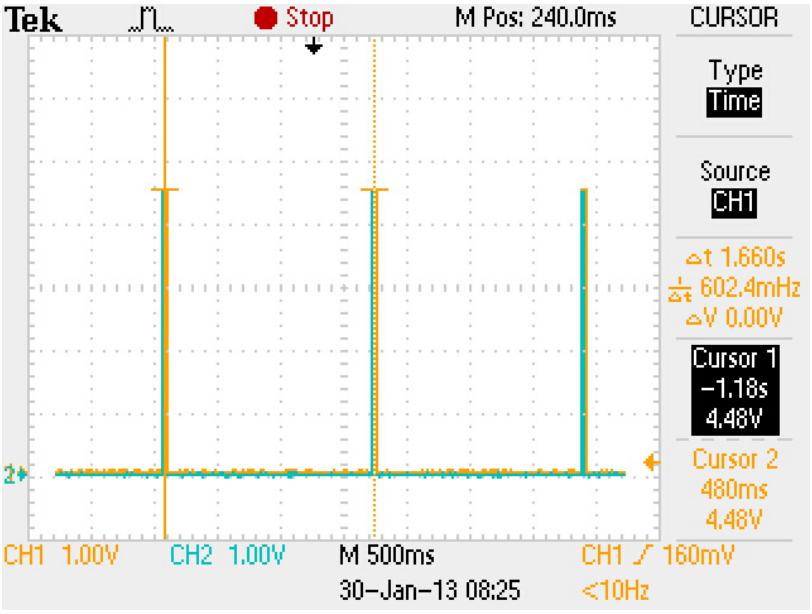

Figure 4.3: 1.7 s interval between the shutdown and the sample & hold timer

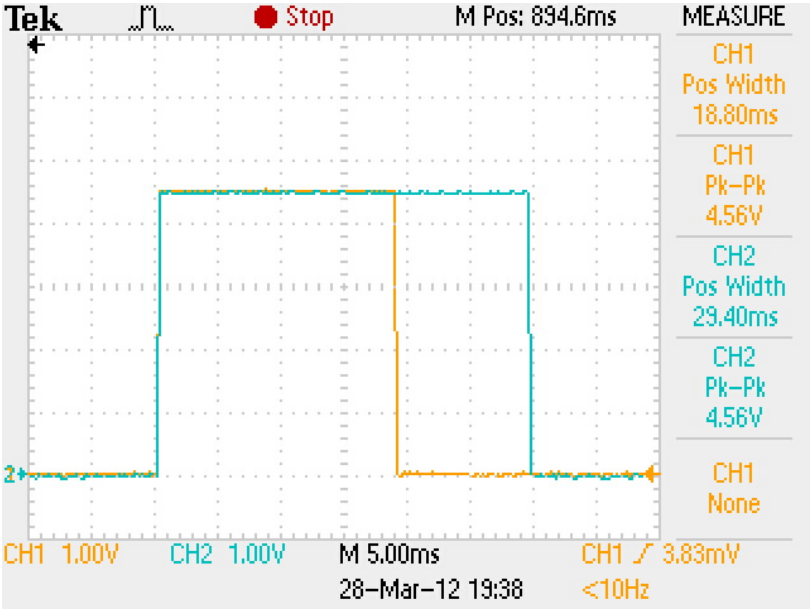

Figure 4.4: Shutdown timer and the sample & hold timer pulse widths

Table 4.3 compares the designed and the measured pulses in terms of width and period. It can be seen that the period between pulses is significantly different to the designed. This merely makes the MPPT track the MPP more frequently, thereby following the MPP more effectively. The downside to tracking the MPP more frequently, is a reduction in efficiency as the PV solar panel is disconnected more frequently within a given time window. This inaccuracy could be due to capacitor and resistor tolerances.

Table 4.3: Comparison of designed and measured timers.

Parameter	Designed	Measured	Error
Period between pulses	2.5 s	1.7 s	32%
Shutdown timer period	30 ms	29.4 ms	2%
Sample & Hold timer period	15 ms	18.8 ms	25%

4.3.3 Reference voltages

The reference voltage ICs were used in the battery under-voltage protection as well as the control of the SEPIC DC-DC converter to generate an error signal. To test the reference voltage ICs a bench power supply was connected to the battery input of the EPS, while the solar panel input and the EPS load output were disconnected. Initially a voltage divider across the LDO was used as a voltage reference but it was later decided to replace one of the resistors in the divider with a TL431 voltage reference IC. Using the independent voltage references instead of the LDO allows for the output voltage of the LDO to drift or ripple slightly without influencing the performance of other circuitry. Table 4.4 shows the measured reference voltages.

Table 4.4: Measured reference voltages.

Location	Designed reference voltage	Measured reference voltage	Error
SEPIC DC-DC converter error amplifier	2.5 V	2.448 V	2%
Battery under-voltage protection	2.5 V	2.451 V	2%

4.4 Maximum power point tracking

Initial testing of the MPPT lead to the discovery that when a large current is drawn from the solar panel, input inaccuracies in the measurement of V_{pv} occur. This inaccuracy is due to a drop in potential across the switch that connects the solar panel to the EPS. The on-state resistance of this MOSFET switch causes this inaccuracy. It was observed that this MOSFET switch could be bypassed, as the SEPIC DC-DC converter isolates the input from the output when the PWM is shut down. If other DC-DC converters are used, it may not be possible to bypass this switch. An example of a DC-DC converter where this may be an issue is the Boost converter, as during shut down the input is connected to the output via an inductor and a diode. If V_{oc} is above the output voltage during the sampling period, current will flow from the PV solar panel to the battery, thereby giving an inaccurate V_{oc} measurement and hence an inaccurate V_{mpp}. Figure 4.5 shows the input voltage to the MPPT, the solar panel voltage. It can be seen in Figure 4.5 that the input voltage increases during the sampling of the open-circuit voltage. Figure 4.6 illustrates the MPPT input voltage (Channel 1) and the output voltage of the MPPT across the Li-poly battery (Channel 2). Figures 4.5 and 4.6 are both recorded with the solar panel input to the EPS connected to a bench power supply, set to a voltage of 5 V and with current limiting set to 2 A. The factor, M_v, between the V_{oc} and V_{mpp} was adjusted to approximately 0.75 in Figures 4.5 and 4.6.

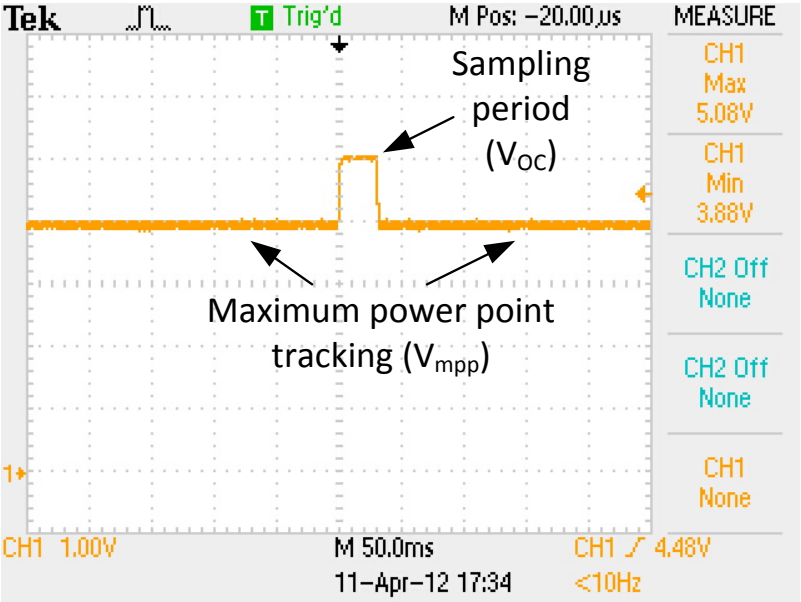

Figure 4.5: Sampled open-circuit voltage

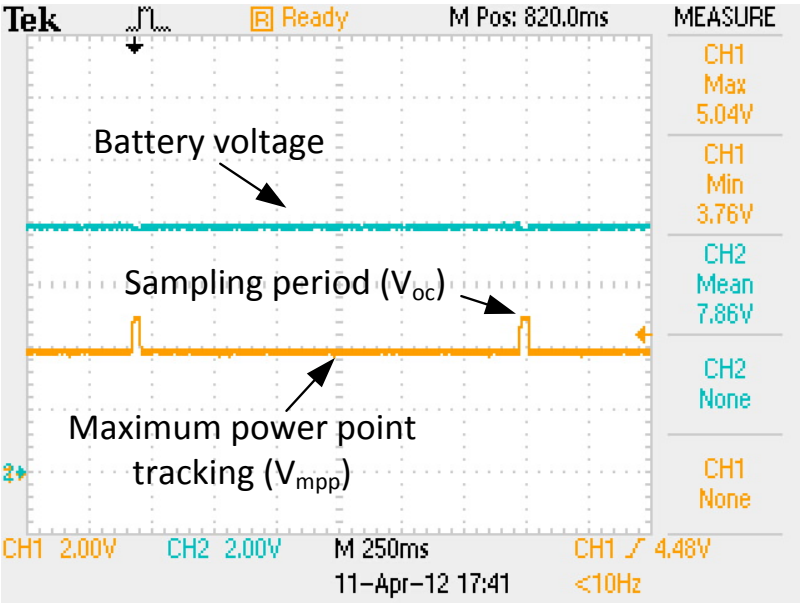

Figure 4.6: Sampled open-circuit voltage and battery voltage during MPPT mode

Figure 4.7 illustrates the solar panel voltage (Channel 1). It can be seen in Figure 4.7 that the transition from an MPPT mode of control to voltage regulation mode of control has begun. The output voltage of the MPPT across the Li-poly battery is illustrated as Channel 2. In Figure 4.7 M_v was set to approximately 0.8. The solar panel voltage is above the set MPPT voltage of 4 V during the period in which the MPPT is in voltage regulation mode and during the period in which the solar panel open-circuit voltage is measured. During the period in which the open-circuit voltage is measured the battery voltage drops as there is no incoming power from the solar panel. Once the solar panel is reconnected the circuit enters MPPT mode for a

short duration to bring the battery voltage up to the charge level as quickly as possible. Once the charge voltage is reached the circuit enters voltage regulation mode until the open-circuit voltage is measured allowing the battery voltage to drop below the regulated battery voltage once again. This crossover period from MPPT to voltage regulation mode happened over a period of minutes and did not take long to complete.

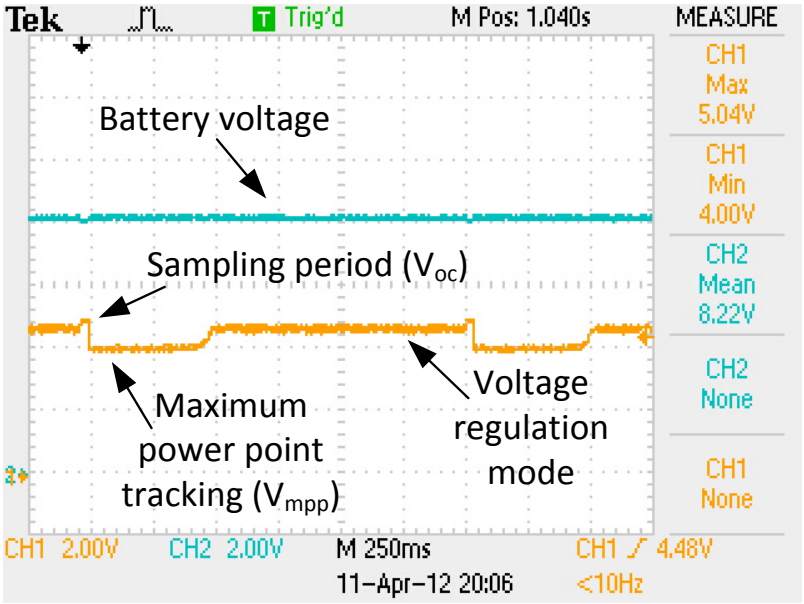

Figure 4.7: Sampled open-circuit voltage and battery voltage while sliding between modes

Eventually the circuit remains in voltage control regulation mode and does not enter MPPT control mode until more power is drawn from the EPS than the EPS can deliver. Figure 4.8 illustrates the solar panel voltage (Channel 1) when the Li-poly battery voltage (Channel 2) has settled to the charge voltage, thereby keeping the circuit primarily in voltage regulation mode, except during the period in which the open-circuit voltage of the solar panel was measured.

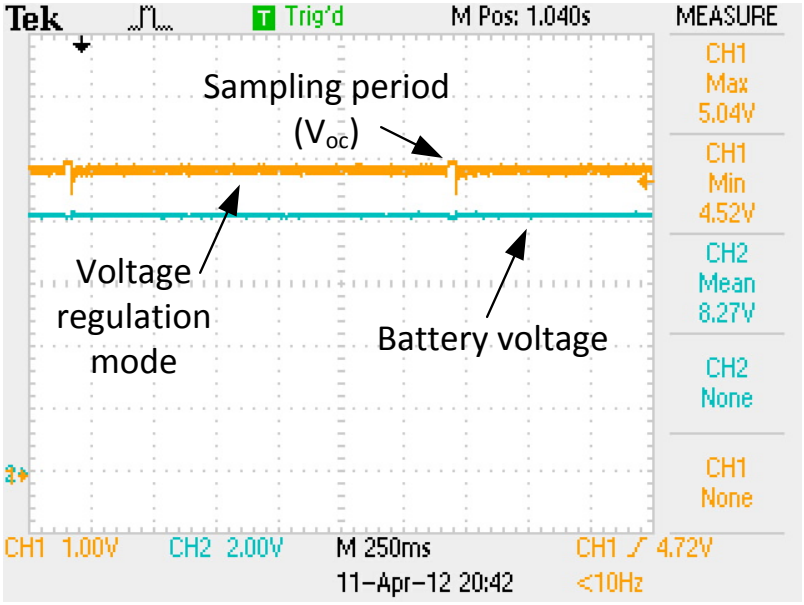

Figure 4.8: Sampled open-circuit voltage and battery voltage during voltage regulation mode

4.4.1 Sample and hold

A simple method of testing the S&H circuit was devised. All the prototype boards were connected with the exception of the distribution board. A bench power supply was connected to the MPPT input. The lack of load causes the EPS to operate in voltage regulation mode as only a small amount of power was required. The waveforms seen in Figures 4.9 and 4.10 were generated through observing the input voltage and the output voltage of the S&H circuit. The ramping input voltage waveform was generated through adjustment of the MPPT fraction adjustment potentiometer used in adjusting the ratio between the maximum power point voltage and the open-circuit voltage of the PV solar panel. This test was done for a dropping input voltage as seen in Figure 4.9 as well as a rising input voltage as seen in Figure 4.10.

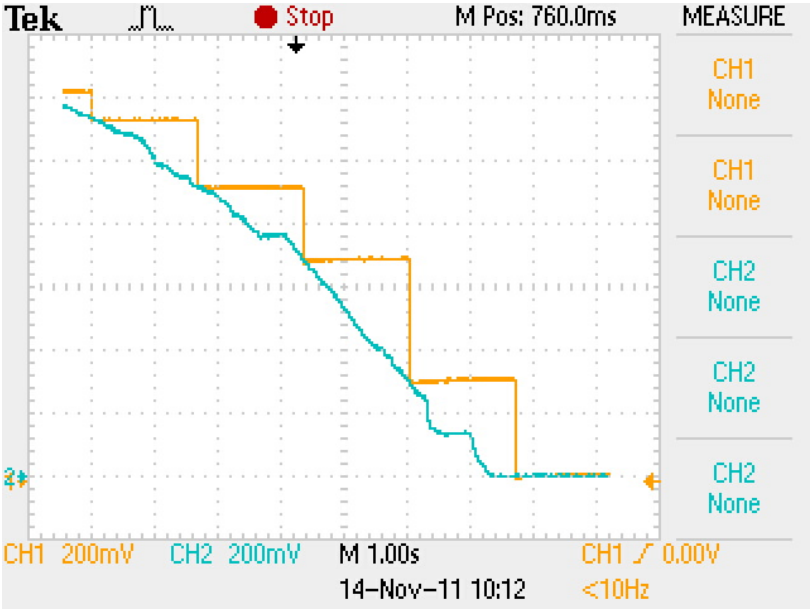

Figure 4.9: Dropping S&H test

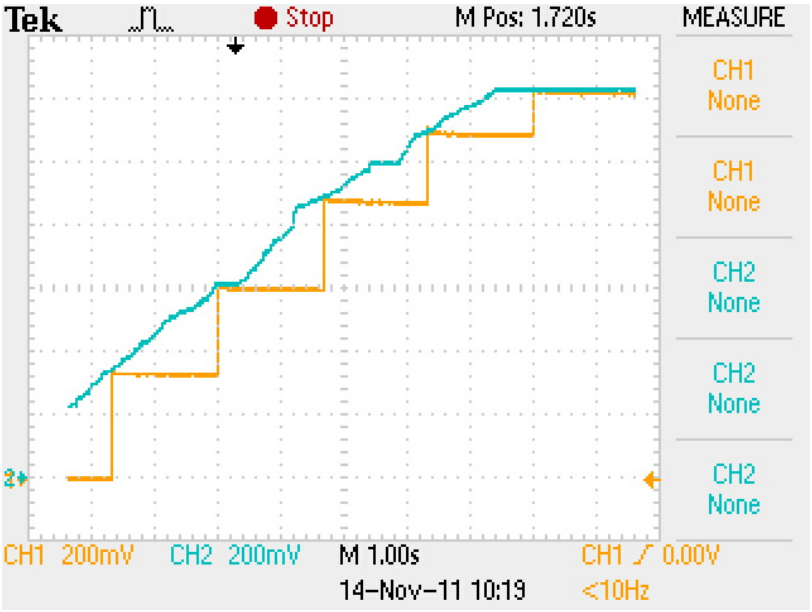

Figure 4.10: Rising S&H test

It can be seen in Figures 4.9 and 4.10 that the S&H circuitry operates adequately with no noticable drooping or drifting of the output voltage.

4.5 Battery charge/discharge regulator

The testing done in this section comprised primarily of the SEPIC DC-DC converter, the PWM required in its operation and the battery under-voltage protection.

4.5.1 Pulse width modulator

Testing of the PWM was achieved through the use of the SEPIC DC-DC converter circuit board only and manually adjusting the reference voltage signal to the PWM with the on-board test potentiometer. The converter circuit board was connected to a bench power supply at the battery input for this test, with the voltage regulated to 5 V by the housekeeping LDO. The design operated as expected at a frequency of approximately 200 kHz as can be seen in Figures 4.11 and 4.12. Initially the reference voltage for the PWM was set such that the PWM produces a pulse train with a duty-cycle of approximately 50% as can be seen in Figure 4.11.

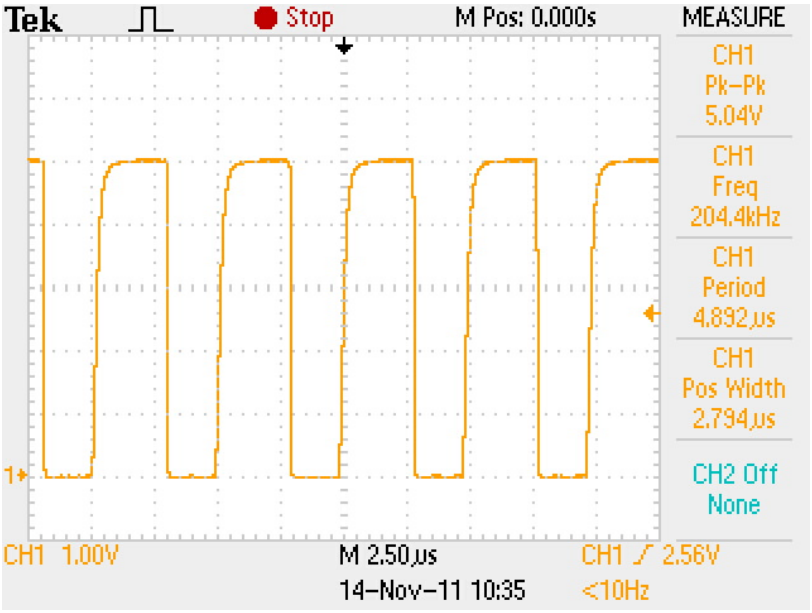

Figure 4.11: 200 kHz PWM at a duty-cycle of approximately 50%

Further testing was done to determine the maximum duty-cycle the PWM could deliver. The result of this can be seen in Figure 4.12. It was determined through the oscilloscope measurement shown in Figure 4.12 that the maximum duty-cycle achievable was approximately 85%.

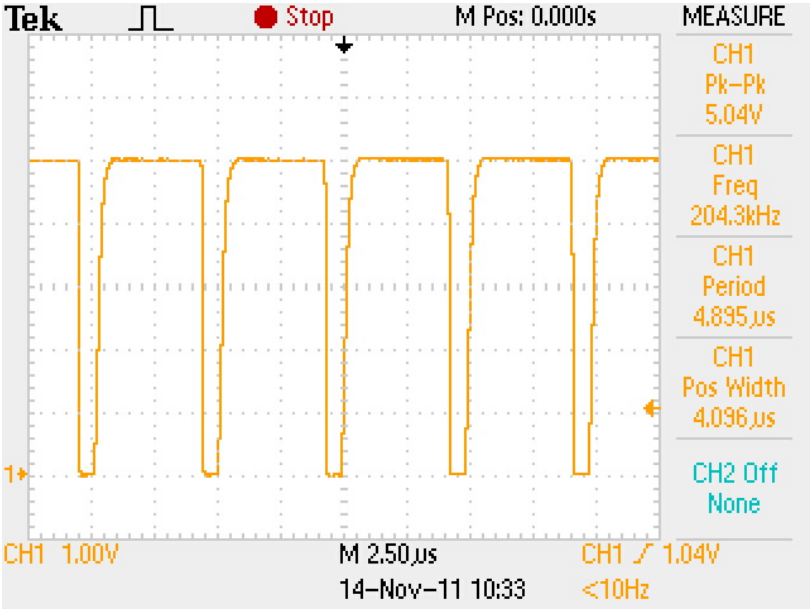

Figure 4.12: 200 kHz PWM at maximum duty-cycle

The output voltage of the discrete MOSFET driver that drives the gate of the main switch of the SEPIC DC-DC converter was measured and can be seen in Figure 4.13.

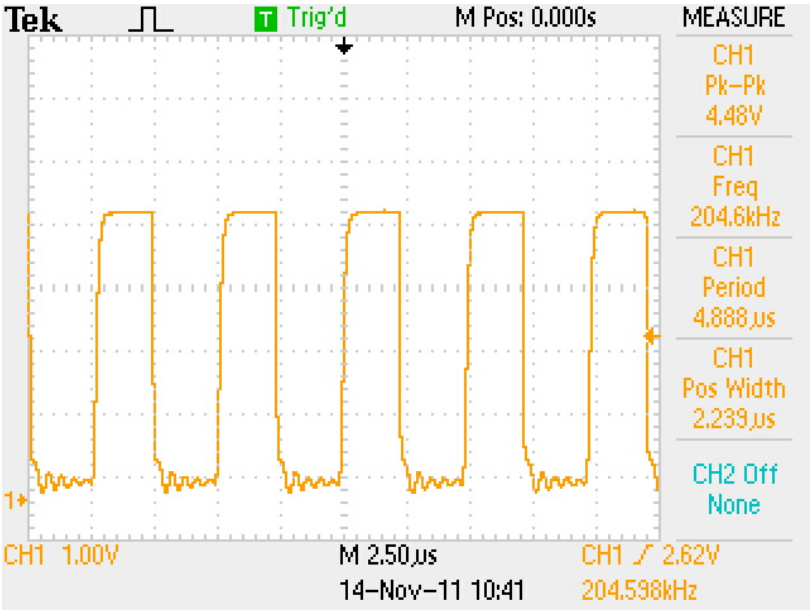

Figure 4.13: 200 kHz SEPIC N-channel MOSFET gate voltage

It was observed in Figure 4.13 that there was a small voltage ripple, or ringing, present on the MOSFET gate while the MOSFET is in an off-state, though this did not seem to detrimentally affect the operation of the circuit. This ringing could be due to gate capacitive and inductive parasitics along with inductance brought on by the PCB track linking the gate to

the driver. These parasitic elements could be forming a resonant tank as mentioned by Fairchild Semiconductor (1998) and causing the oscillation.

4.5.2 SEPIC DC-DC converter

A 1000 μF capacitor was used in place of the battery and no load connected to the EPS. This meant that the quiescent power consumption of the EPS could be measured. In this state all the power supplied by the DC-DC converter would be supplied to the LDO and any subsequent electronics connected. An insignificant amount of current would be sourced by the converter to overcome the leakage current of the capacitor replacing the battery. The power lost due to the leakage current of the capacitor was insignificant in comparison to the power used by the DC-DC converter and the control electronics. As the leakage current was insignificant it was neglected in the measurements. A 0.1Ω resistor was placed in series with the solar panel input of the MPPT circuit allowing for quick and easy measurement of the input current flowing into the EPS. This measurement was done by measuring the voltage drop across the resistor and calculating the current flowing through it. The shut down input terminal of the SEPIC DC-DC converter board was tied to ground and the input of the S&H circuit set as high as possible, thereby disabling the MPPT operating mode of the EPS and locking the EPS into voltage regulation mode.

The control circuit was measured to draw approximately 15 mA and consume approximately 75 mW. The EPS quiescent power consumption with no load attached and all the EPS parts connected resulted in the consumption seen in Table 4.5.

Table 4.5: Measured EPS quiescent power consumption.

Measured input voltage	Measured input current	Measured power
2.996 V	193 mA	578.23 mW
4.925 V	121 mA	595.92 mW
9.87 V	68 mA	671.16 mW
14.97 V	55 mA	823.35 mW
19.93 V	50 mA	996.5 mW

The efficiency of the SEPIC DC-DC converter was measured and shown in Appendix A. Issues were encountered with the SEPIC DC-DC converter with a 3 V input and heavy loading on the output. This was thought to be due to the very high duty-cycle required to supply the required power at 8.2 V. The efficiency of the SEPIC DC-DC converter was measured with an input voltage of 3 V to 20 V and with an output load of 2 W to 8 W. The SEPIC DC-DC converter was designed for a maximum input power of 10 W, as such the 3 V input voltage final efficiency test was not done as to protect the prototype from damage (see Appendix A). It was observed that the efficiency of the SEPIC DC-DC converter lay in the 60% to 70% range under many of the tests.

4.5.3 Battery under-voltage protection

In this test the SEPIC DC-DC converter and control prototype boards were connected together with the distribution test board omitted. A bench power supply and a resistive load was connected as well as a 1000 μF capacitor to emulate a battery. The current and voltage settings of the bench power supply were such that the available power to the MPPT was less than the power required by the load. To protect the Li-poly battery from damage, the capacitor was initially used until the function of the protection was verified to work. In this test, the battery voltage dropped until the under-voltage protection threshold was reached. At this voltage the load is disconnected allowing the capacitor to charge towards the regulated charge voltage of 8.2 V. Once the capacitor reaches the nominal voltage of the battery, the load is reconnected. As the input power to the EPS was lower than the required output power, the capacitor voltage began to drop once again. This test can be seen by the waveform illustrated in Figure 4.14. This waveform shows the voltage observed at the load. It can be seen in Figure 4.14 that a lower threshold of 6.28 V was achieved with an upper threshold of 7.24 V.

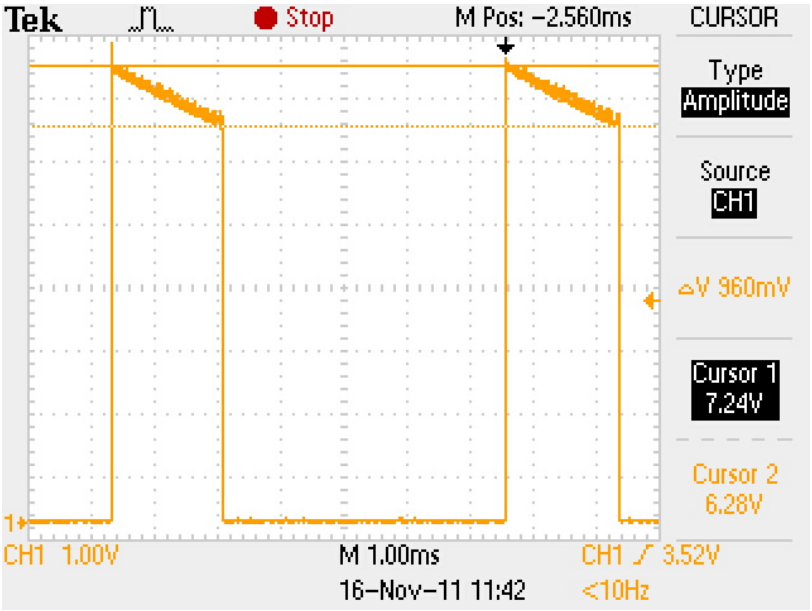

Figure 4.14: Battery under-voltage protection limits

Table 4.6 shows the measured and designed upper and lower voltage threshold limits used in the battery under-voltage protection.

Table 4.6: Battery upper and lower thresholds.

Parameter	Designed	Measured	Error
Lower threshold	6.2 V	6.28 V	2%
Upper threshold	7.4 V	7.24 V	2%

Though the thresholds achieved are outside the designed 6.2 V and 7.4 V limits, these voltage levels are still acceptable and provide the battery with adequate under-voltage protection.

4.5.4 Battery over-charge protection

The emergency battery over-voltage and over-current protection consisted of a MAX4374 and was tested and operated adequately. The over-voltage protection was successfully adjusted within a range of 8 V to 10 V and was later set to 8.6 V. The over-current battery protection though designed to trip at 300 mA was measured to trip at approximately 345 mA. As a proof of concept the design operated adequately, though in a final design the adjustment of the trip current may need to be adjusted such that the current limit is set to 1.0 C of the Li-poly battery used. In this test a current significantly lower than 1.0 C was used as the single channel MPPT could not deliver enough current to charge the battery at a current larger than $\frac{P_{MPP}}{V_{batMin}} = \frac{10W}{6V} = 1.67\ A$ which equates to a C-rate of 0.38 C.

The over-voltage protection tests were done with a 1000 μF capacitor replacing the battery as not to damage the Li-poly battery due to excessive charge voltage. The over-current tests were done with the Li-poly battery attached and the batteries slightly discharged. The voltage across the sense resistor was then measured and the current flowing into the battery determined. The measured voltage across the 0.22 Ω sense resistor was 76 mV concluding that a current of approximately 345 mA was flowing into the battery. The battery over-voltage and over-current protection disabled the MOSFET gate driver used in switching the SEPIC DC-DC converter switch. A far more elegant solution would be to pull the error signal supplying the PWM low, thereby shutting down the PWM in that manner. This was only realised during testing of the EPS.

4.6 Distribution

The three prototype test boards were connected together as the 5 V rail from the SEPIC DC-DC converter board and the timing from the control board are required to operate the distribution board. A fixed resistive load of 8 Ω was connected to the output of the distribution board and a bench power supply was connected to the input of the distribution board. The input voltage of the bench power supply was then increased gradually while the current through the load at the output was measured. The input voltage was increased until the current through the load reached the over-current limit. Once the current through the load exceeds the over-current limit, the load is disconnected, stopping flow of current to the load. In this manner, the maximum current can be measured just before the load is disconnected and the over-current limit can be determined. Initial testing showed the current limit to be approximately 300 mA which coincides with the designed limit of 300 mA. This value can easily be changed through the adjustment of a voltage divider connected to the output voltage of the MAX4374FEUB+. The same test was then done with a 39 Ω load achieving the same result.

4.7 Modifications to the prototype circuit

The prototype circuit operated as expected except in terms of efficiency. The prototype struggled operating at low input voltages when loaded. This was thought to be due to the poor efficiency of the designed SEPIC DC-DC converter and the limited duty-cycle of the PWM. Some simple additions were added to the typical SEPIC DC-DC converter topology illustrated in Figure 2.20 and 3.8 in an attempt to rectify these issues. An additional MOSFET was placed in parallel to the SEPIC DC-DC converter's MOSFET switch, Q. This had the benefit of lowering the effective on-state resistance of the switch thereby reducing power losses in the SEPIC DC-DC converter. Additionally the operating frequency of the PWM was reduced from 200 kHz to 100 kHz reducing switching losses in the MOSFET and core losses in the inductors. The coupling capacitor located between the two inductors, Cs, in the SEPIC DC-DC converter was replaced with multi-layer ceramic capacitors (MLCCs) with a lower ESR than the tantalum originally used. The MLCCs used in replacing the tantalum coupling capacitor, Cs, had a measured ESR of approximately 15mΩ. By comparison, the tantalum originally used in the place of Cs had a measured ESR of approximately 270 $m\Omega$.

The initial PWM circuit can be seen in Figure 3.13, modifying the PWM circuit to operate at 100 kHz rather than 200 kHz required the timing resistance to be changed to approximately 100 kΩ, as illustrated by the timing graph seen in Figure 3.14. This was achieved by changing R4 to 100 kΩ, resulting in a timing resistance of 103.3 kΩ. Making this modification requires a new resistor value for R2, the dead-time control resistor. This resistor, R2, controls the maximum duty-cycle of the DC-DC converter. The value for R2 was calculated with Equation 4.7.1 for a maximum duty-cycle of 90% (Texas Instruments, 2002:4).

$$\begin{aligned} R_{DT} = R2 =& (R_t + 1250)[D(V_{oscMAX} - V_{oscMIN}) + V_{oscMIN}] \\ R2 =& (103.3k\Omega + 1250)[0.9(1.3V - 0.7V) + 0.7V] \\ R2 =& 129.642\ k\Omega \\ & (180k\ k\Omega // 470\ k\Omega = 130.1538\ k\Omega) \end{aligned} \tag{4.7.1}$$

Additional modifications were done to the prototype, including the addition of a MOSFET in parallel to the MOSFET used in disconnecting the solar panel from the EPS, represented as Q_{PV} in Figure 3.8. This modification reduced the significance that the voltage drop across the MOSFET played in the operation of the MPPT as the on-state resistance was effectively halved. Though this modification was done, the MOSFET used in disconnecting the solar panel was eventually bypassed as it was determined unnecessary for the operation of the circuit with a SEPIC DC-DC converter. Though this switch was bypassed the electronics was kept in place as other DC-DC converter topologies could be used later if needed.

The power losses in the SEPIC DC-DC converter switching elements were recalculated for 100 kHz with the use of Appendix C.1 and can be seen in Table 4.7.

Table 4.7: 100 kHz SEPIC converter switching element power losses.

Switching Component	Power Dissipated
IRF7343	258 mW
MBRS340	610 mW

The modified PWM output voltage signal can be seen at a duty-cycle of 50% in Figure 4.15 and at a duty-cycle of roughly 90% in Figure 4.16

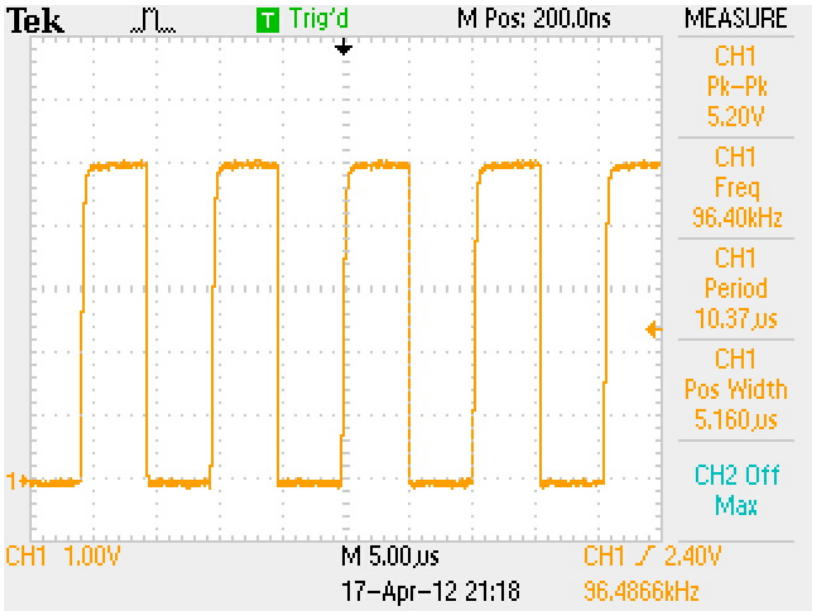

Figure 4.15: 100 kHz PWM at 50% duty-cycle

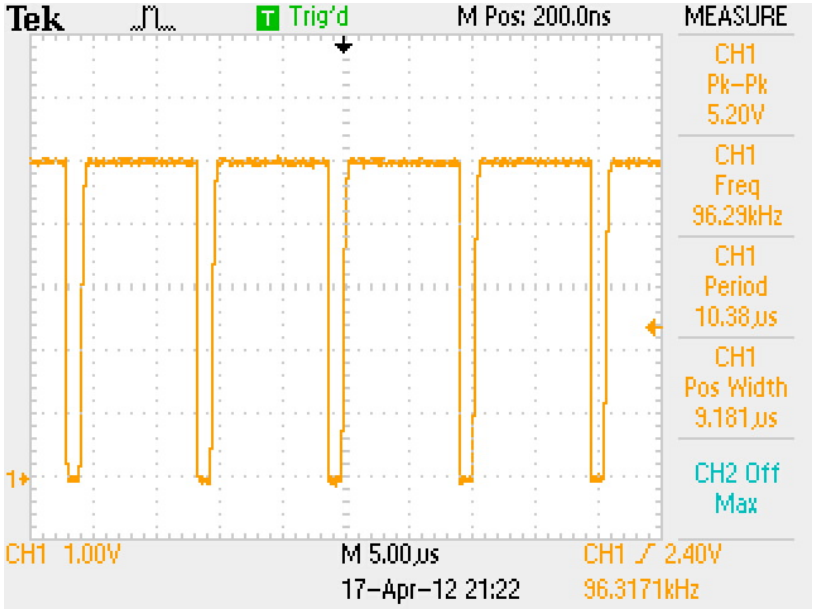

Figure 4.16: 100 kHz PWM at maximum duty-cycle

Figure 4.17 shows the SEPIC DC-DC converter's MOSFET gate voltage with the PWM operating at a 50% duty-cycle.

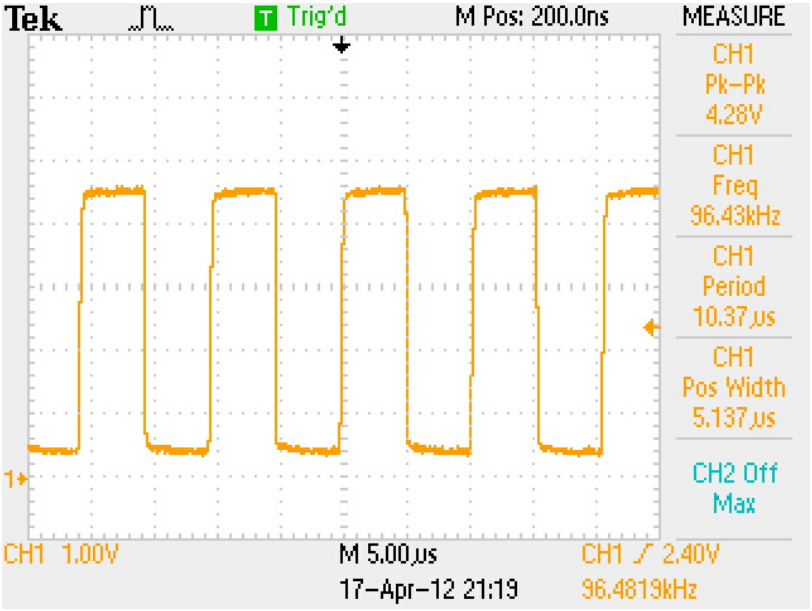

Figure 4.17: 100 kHz SEPIC N-channel MOSFET gate voltage

Changing the coupling capacitor, Cs, of the SEPIC DC-DC converter, alters the response of the power stage of the converter, as such the stability criteria for the converter had to be verified with the design. The new small-signal model used in the design of the SEPIC DC-DC converter can be seen in Figure 4.18.

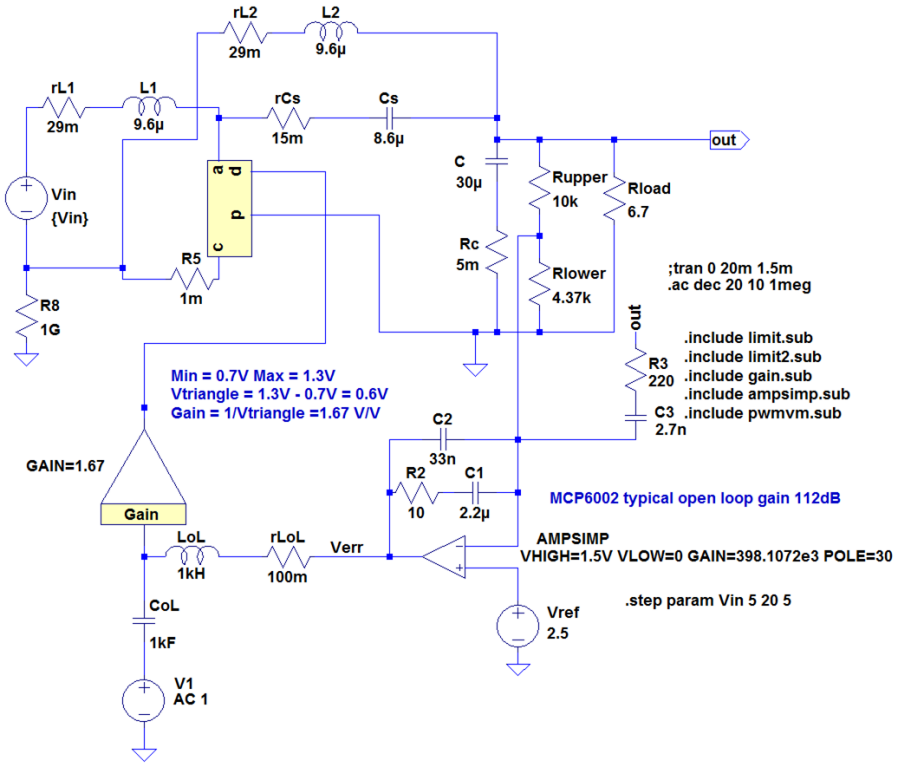

Figure 4.18: Small-signal model of designed SEPIC DC-DC converter.

As can be seen in Figure 4.19 the system could become unstable upon closing the loop if compensation was not employed. This is due to a 180° phase shift brought on by the power stage of the converter while still having a gain of over 0 dB. Closing the feedback loop under such a condition would produce positive feedback and cause possible oscillation of the output of the converter.

Figure 4.19 is the response of the power stage of the SEPIC DC-DC converter operating at its maximum power handling capability of 10 W and with a supply voltage of 5 V, 10 V, 15 V and 20 V.

Figure 4.20 is the response of the duty-cycle to output voltage of the SEPIC DC-DC converter operating at 50% of its maximum power handling capability with a supply voltage of 5 V, 10 V, 15 V and 20 V.

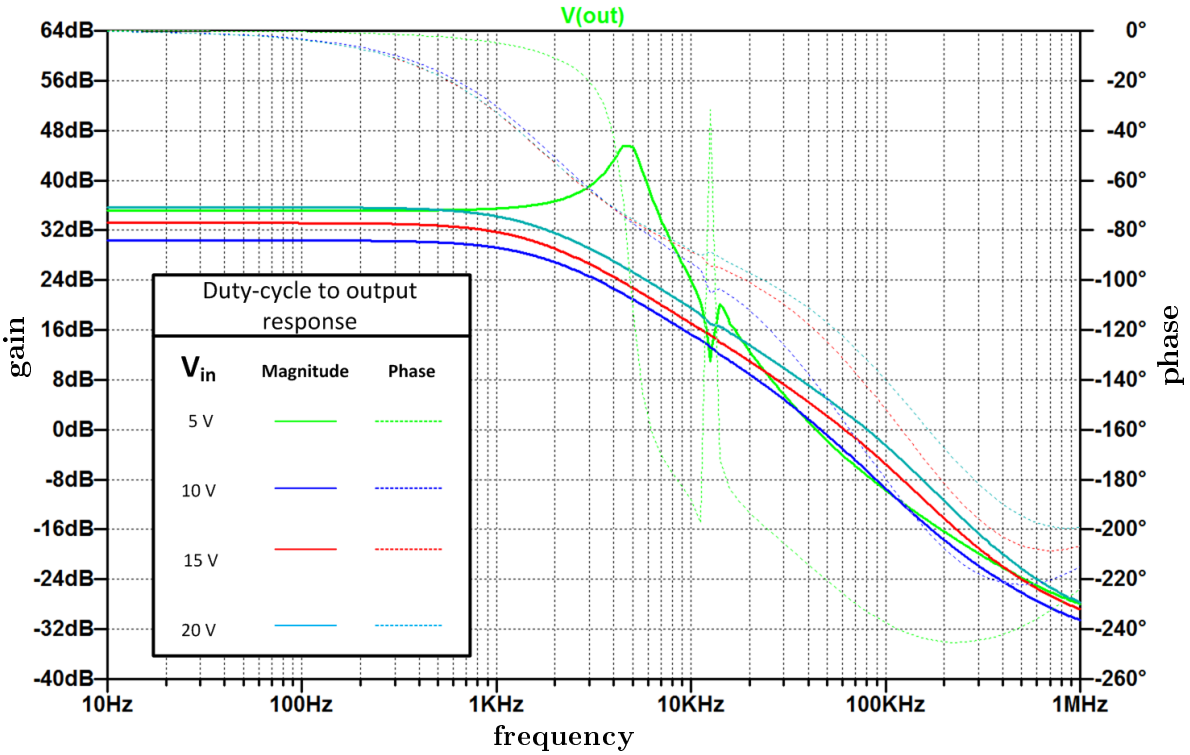

Figure 4.19: SEPIC DC-DC converter duty-cycle to output response (100% power)

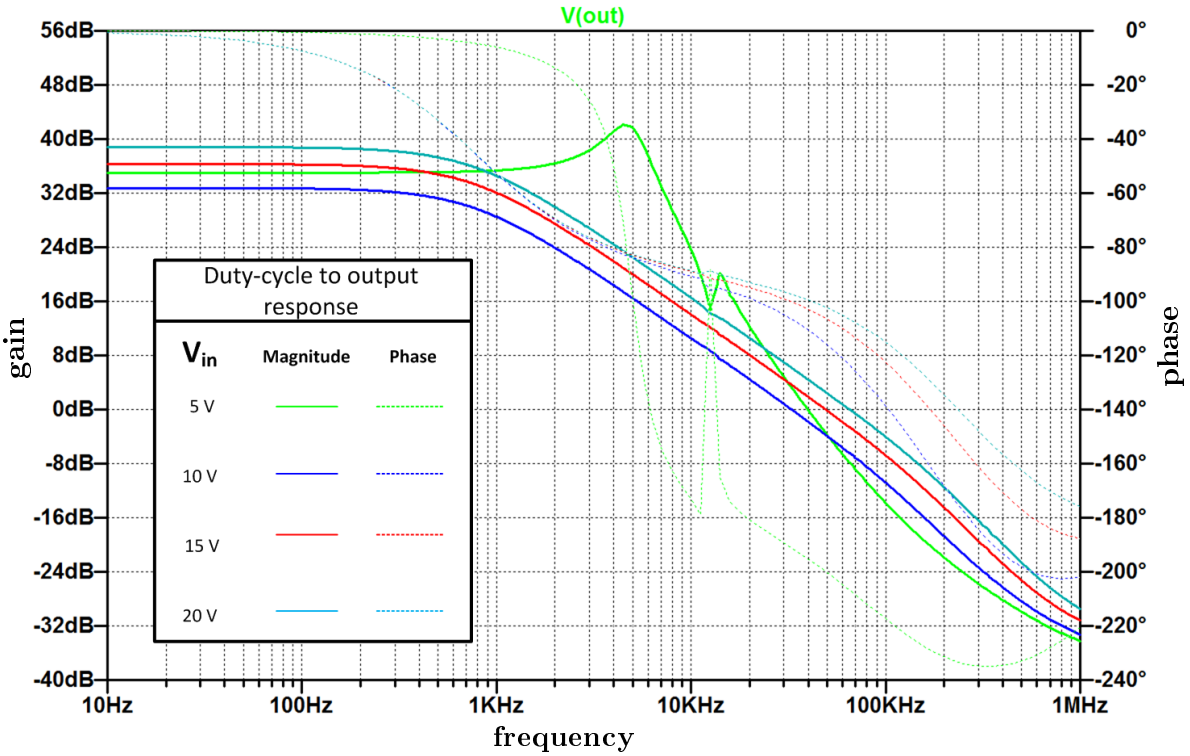

Figure 4.20: SEPIC DC-DC converter duty-cycle to output response (50% power)

The phase shift brought on by the power stage reaches −180° as seen in Figure 4.19 and Figure 4.20, therefore type 3 compensation was chosen as a means to improve the stability of the closed loop system, as was the 200 kHz design.

Figure 4.22 shows the closed loop response of the SEPIC DC-DC converter at 100% of its rated output power using the same compensation network used in the 200 kHz design. The simulated closed loop system response over the input voltage range and at 100% of the converter's rated output power had a worst case phase margin, PM, of 85° at 250 Hz and a worst case gain margin, GM, of 45 dB at 80 kHz.

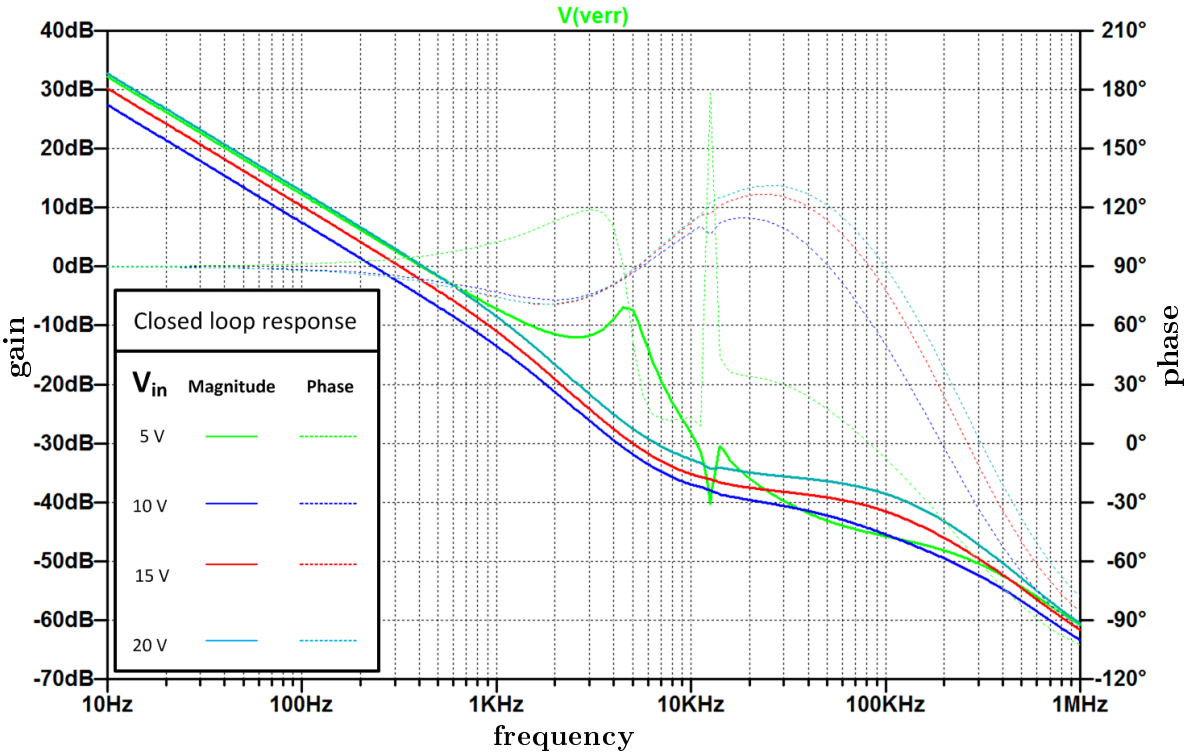

Figure 4.21: SEPIC DC-DC converter closed loop response with selected values (100% power)

Figure 4.22 shows the closed loop response of the converter at 50% of its rated output power. The simulated closed loop system response over the input voltage range and at 50% of the converter's rated output power had a worst case phase margin, PM, of 75° at 300 Hz and a worst case gain margin, GM, of 51 dB at 125 kHz.

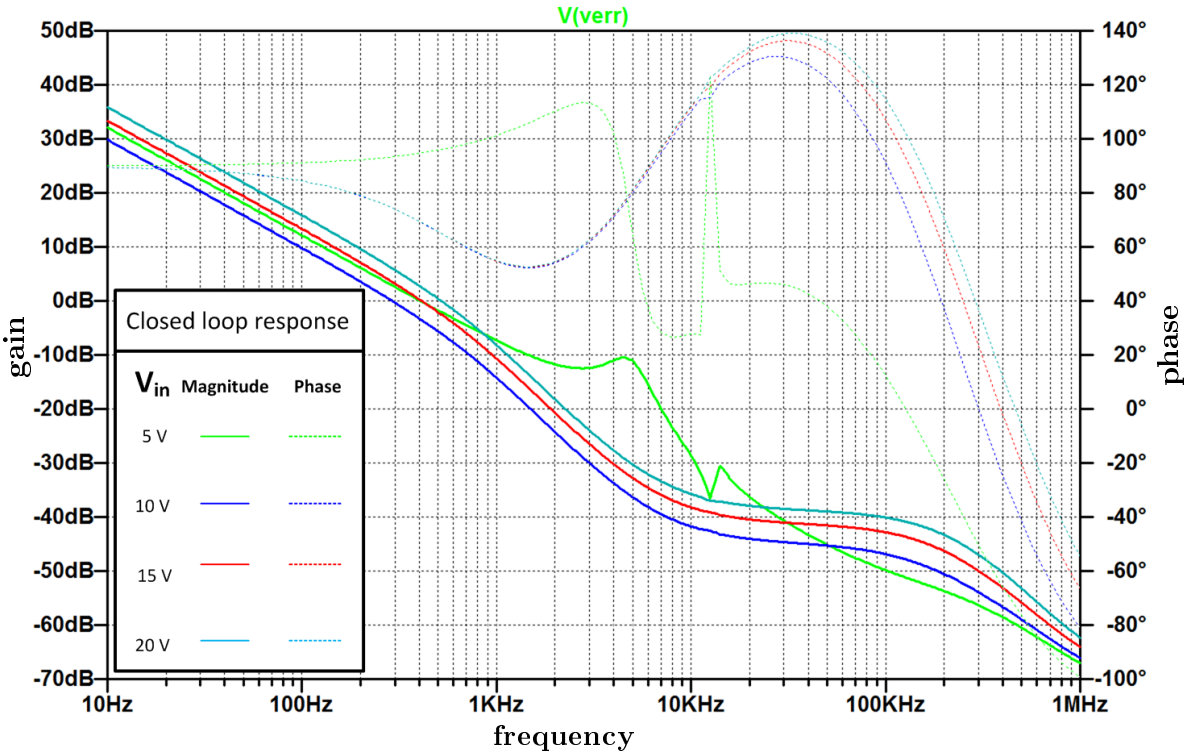

Figure 4.22: SEPIC DC-DC converter closed loop response with selected values (50% power)

The simulated cut-off frequency was lower than expected but acceptable as a high frequency response was not required. The design has excessive PM, but this is also acceptable as the response of the system did not need to be fast as the primary goal of the converter was to charge the Li-poly battery.

It was shown through these simulations that the previously designed compensation would work with the modifications made the EPS circuitry. Therefore, there was no need to change the design of the compensation.

4.8 Final results

The final EPS prototype circuit operating with a 100 kHz SEPIC converter was fully tested. This section pertains to the results of the final tests that were done. Many of the tests previously done in Section 4.1 were not redone as the modifications to the circuit would not have altered the results.

It was determined previously that the PV solar panel used during testing had a V_{mpp} at approximately 75% of V_{oc}. The MPPT circuit samples the open-circuit voltage, V_{oc}, of the PV solar array every 1.7 s and in doing so disconnects the PV solar panel from the EPS for a period of 30 ms. The operation of the various MPPT parts was previously verified in Section 4.1. Figure 4.23 and Figure 4.24 show the solar panel voltage, V_{pv}, while the MPPT is operational. During this test the intensity of the light illuminating the solar panel was increased and decreased

through the use of the DC power supply connected to the light box. This increased and decreased the amount of available current to the EPS. Increasing the intensity of the light also increased the temperature of the solar panel, thereby changing the open-circuit voltage.

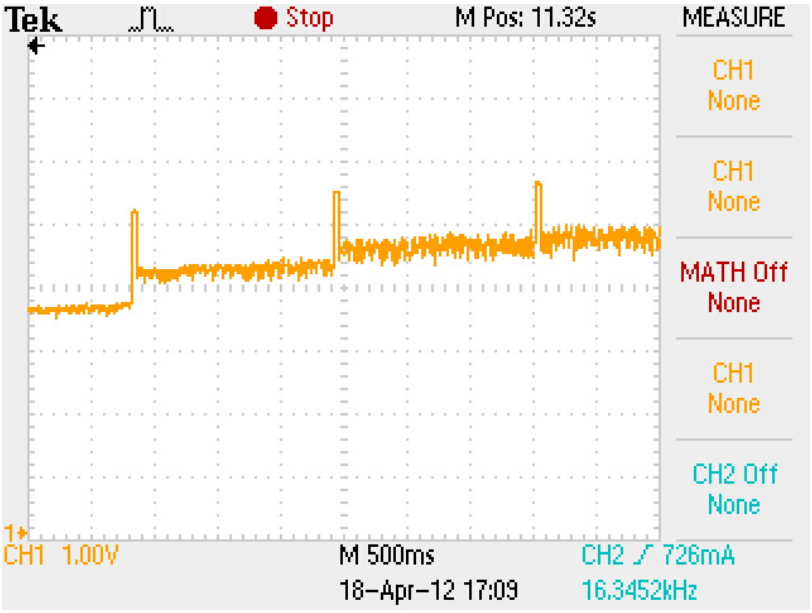

Figure 4.23: MPPT solar panel voltage rising

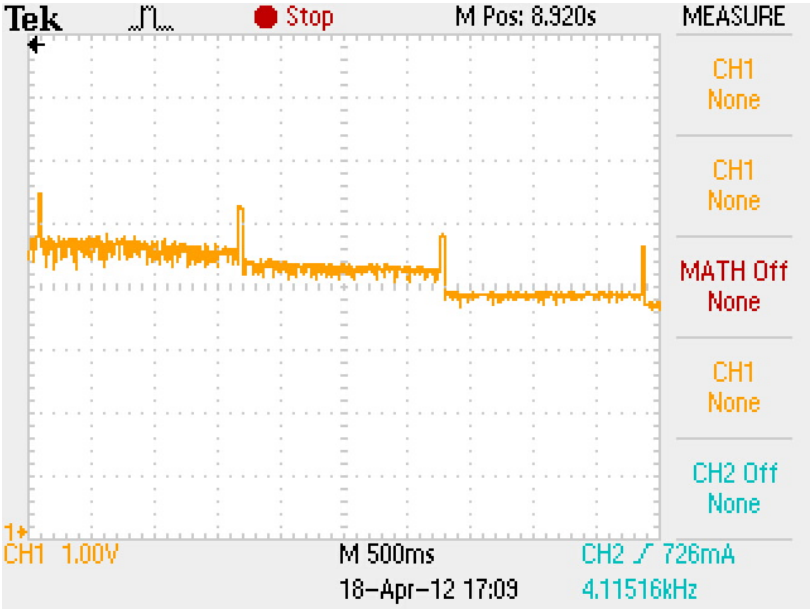

Figure 4.24: MPPT solar panel voltage dropping

It was observed during testing that using a large capacitor at the input to the EPS allowed the MPPT to better track V_{mpp} as the input voltage did not swing as far from the maximum power point. This was due to filtering, an increase in this capacitance allowed a more steady stream of current to be drawn from the solar panel.

The modified SEPIC DC-DC converter had an average efficiency of 65% and a peak efficiency of 71% whereas the initial design had a average efficiency of 62% and a peak efficiency of 69%. The measured efficiencies can be seen in Appendix A for both the initial prototype design and the modified prototype design. This is not a true reflection of the SEPIC DC-DC converter by itself as power had to be supplied to the control circuit board, the LDO and protection circuits within the SEPIC DC-DC converter prototype board. Therefore the efficiencies stated above are the minimum expected from the SEPIC DC-DC converter.

The quiescent power consumption of the modified EPS with no load and drawing power from the PV solar array input can be seen in Table 4.8.

Table 4.8: Measured modified EPS quiescent power consumption.

Measured input voltage	Measured input current	Measured power
3.055 V	183 mA	559.065 mW
5.050 V	113 mA	570.65 mW
10.00 V	64 mA	640 mW
14.94 V	52 mA	776.88 mW
20.04 V	48 mA	961.92 mW

Table 4.9 shows the quiescent power consumed with only the battery connected and no power flowing from the PV solar panel.

Table 4.9: Quiescent battery power consumption.

Battery voltage	Battery current	Measured power
7.37 V	50 mA	368.5 mW
7.58 V	48.9 mA	370.66 mW
8.18 V	51.2 mA	418.82 mW

The ability of the MPPT to effectively maintain the ratio between V_{mpp} and V_{oc} over the various PV solar input voltages was measured and can be seen in Table 4.10. Though M_v did drift, the amount of drift is not substantial over such a large voltage test range.

Table 4.10: Prototype EPS M_v drift test

Effective V_{oc}	Effective V_{mpp}	Calculated M_v
20.03 V	15.15 V	0.7564
15.01 V	11.42 V	0.7608
9.91 V	7.58 V	0.7649
5.09 V	3.98 V	0.7819

The final results of the tests done in Section 4.1 and this Section for the EPS have been summarised in Table 4.11. The notes associated with Table 4.11 are as follows.

Note 1: The battery charge over-current protection was disabled during normal operation as it reduced the charge rate of the battery and was not necessary for a single MPPT channel as the single channel could not produce an output current exceeding 4.4 A. The over-current protection did function, though it is advised for future designs that the error signal to the PWM be pulled to ground instead of disabling the MOSFET gate driver. The over-current protection limit can be adjusted by changing two resistors located at the comparator input of the MAX4374 (see Section 3.6.5).

Note 2: The battery over-voltage protection was built to be adjustable and tested within a voltage range of 8 V to 10 V and functioned as needed. In a final EPS design, it is advised that fixed resistor values are used such as was calculated in Section 3.6.5. The battery over-voltage protection was set to 8.6 V, as the maximum permissible voltage that Li-ion or Li-poly based battery chemistries should operate at is 4.3 V per cell (see Section 2.4.2.2). This voltage is large enough as not to affect the operation of the regulation of the SEPIC DC-DC converter to 8.2 V. It was observed that using the 1000 μF capacitor instead of the battery resulted in some over-shoot in the output voltage when the EPS was subjected to a large load-step. When the batteries were connected instead of the capacitor this over-shoot was significantly suppressed and the over-voltage protection did not need to engage.

Note 3: The over-current protection used in protecting the battery bus that supplies the loads and payloads was tested and disconnected the loads successfully when a current exceeding approximately 300 mA was drawn by the load. The distribution was tested separately to the EPS through the use of a fixed resistive load at the output of the distribution. The current flowing through the load was measured and the input voltage slowly increased until current flowing into the load stopped. The maximum current measured before the load was disconnected was approximately 300 mA. This current limit can be easily adjusted through the selection of resistors placed at the comparator input of the MAX4374 or by selecting an appropriate sense resistor (see Section 3.7).

Table 4.11: Summary of results

PV solar panel V_{oc}/V_{mpp} ratio	
M_v	≈ 0.75

LDO measurements	
Input voltage	**Output voltage**
6.118 V	5.014 V
8.209 V	5.019 V
6.033 V	4.989 V

Reference voltages			
Location	**Designed reference voltage**	**Measured reference voltage**	**Error**
SEPIC DC-DC converter error amplifier	2.5 V	2.447 V	2%
Battery under-voltage protection	2.5 V	2.451 V	2%

Battery under-voltage protection thresholds			
Parameter	**Designed**	**Measured**	**Error**
Lower threshold	6.2 V	6.28 V	2%
Upper threshold	7.4 V	7.24 V	2%

MPPT timers			
Parameter	**Designed**	**Measured**	**Error**
Sample period	2.5 s	1.7 s	32%
Shut down duration	30 ms	29.4 ms	2%
S&H duration	15 ms	18.8 ms	25%

SEPIC DC-DC converter	
Condition	**Efficiency**
10 V input voltage with the EPS under maximum load	71%
Input voltage	**Output voltage**
3 V - 20 V	≈ 8.2 V

Battery over-charge protection			
Parameter	**Designed**	**Measured**	**Comment**
Over-current	300 mA	345 mA (76 mV/0.22Ω)	Note 1
Over-voltage	adjustable	8 V - 10 V (set to 8.6 V)	Note 2

Distribution			
Parameter	**Designed**	**Measured**	**Comment**
Payload over-current protection	300 mA	≈ 300 mA	Note 3

4.9 Summary

This chapter pertained to the evaluation of the EPS prototype circuit. During testing issues were encountered, these issues were overcome through modification of the circuit. The efficiency of the circuit was lower than expected but later improved through the replacement of the SEPIC DC-DC converter's coupling capacitor and the reduction of its switching frequency from 200 kHz to 100 kHz. These modifications are stated in this chapter and the final results after modification are supplied. The prototype EPS functioned as intended though differences between the designed and practical implementation of the EPS existed. Though there were differences these differences did not affect the operation of the EPS in a negative manner.

Chapter 5

Conclusions

5.1 Summary and conclusions

The main objective of the project was to design, build and test a functioning power system for a future CubeSat mission and in doing so broaden the knowledge of F'SATI and the CIR in the area of satellite power systems. To complete this objective a literature review of various aspects of satellite power systems was done. Upon completion of the literature review an engineering prototype was designed and built. The requirements for the prototype were determined through the research covered in Chapter 2 and specifically in Section 2.4. The requirements were later summarised for the design in Chapter 3. The literature review covered topics outside of satellite power systems, namely that of SMPS, board layout, EMC and the stability of SMPS in a closed loop. The literature reviewed within the SMPS topics aided in the understanding of SMPS and the design of an efficient power system capable of regulating its own output voltage in a stable and safe manner. This stable, safe SMPS in turn was used to charge the Li-poly battery.

The CubeSat standard including its origins and how this standard affects the design of an EPS was investigated. Following this an overview of the various components within a satellite was discussed. This lead to the understanding of the various components within an EPS. These various components were further researched in order to design and fully understand the satellite EPS. The parts of interest within a satellite EPS include the solar array, battery, battery charge and discharge regulators, load switching and fuses. These components are used in generating, storing, conditioning, controlling and distributing power to all bus and payload equipment within the satellite.

PV solar cells were discussed as the primary energy source for the satellite. It became apparent through the literature that there are many influencing factors that affect the amount of electrical power that can be drawn from a PV solar cell/panel. Due to the non-linear dependency of the current and voltage to one another, and the aforementioned influencing factors the maximum power that the PV solar cell/panel can source is not constant. It was discovered that an MPPT would be an effective means of compensating for these influencing factors allowing more energy to be harvested from the PV solar panel.

Batteries are an integral part of a satellite operating with PV solar panels as a source of electrical

power. Batteries store energy for peak power demand and during times of eclipse. The batteries discussed for a CubeSat mission are Li-ion battery chemistries as they are more commonly flown than NiMH due to their high energy densities. The operating voltage range of Li-ion and Li-poly batteries are discussed as well as the CC/CV charging algorithm used in charging these batteries. The literature reviewed concerning Li-ion batteries defines the operating temperature range as 0° C to 45° C during charging and defined the minimum and maximum voltage limits of the battery in order to safely operate the battery with the prototype EPS. It was discovered that these voltage limits are 3 V for the minimum operating voltage and 4.2 V for the maximum operating voltage per cell. The thermal limitation of the Li-ion battery chemistries would have to be addressed through means of thermal control. This can be done actively through the use of heaters or passively through the use of insulation materials.

Four EPS topologies were investigated, namely the DET with battery bus, DET with regulated bus, S^3R and MPPT with battery bus. The DET topologies and the S^3R have the drawback of receiving the highest efficiency from the the solar array when the battery is fully charged and when the solar panels are at their maximum temperature. This drawback makes these topologies less suited to CubeSat missions where the amount of power and mass is limited. Two MPPT techniques were discussed, namely P&O and FOCV. The FOCV based MPPT was chosen as the method of MPPT for the EPS prototype due to its simplicity in analogue design. The use of an MPPT allows for extraction of energy from the PV solar panels with greater efficiency than the DET EPS topologies.

Protection concepts used in spacecraft power systems were investigated, though CubeSats generally use limited or no built-in redundancy due to mass, power and size constraints. The addition of simple components such as diodes can be used to better protect the EPS from failure while maintaining a simple robust design. EPSes manufactured by GomSpace, Clyde Space and Pumpkin are briefly discussed illustrating the EPS requirements that may be expected for future F'SATI space missions. The requirement for flexibility in the designed EPS prototype brought about the decision to attempt a design capable of accepting solar panels from many of these manufacturers while also having the capability to accept a myriad of PV solar cell technologies.

The space environment is a harsh place for a CubeSat and its electronics and as such was discussed. Radiation can cause problems with electronics due to SEUs and SELs. These problems were discussed along with how charged particles in space having significantly different energy levels cause different amounts of damage. This damage can cause different damaging effects to the I_{sc} and V_{oc} of PV solar cells. The CubeSat can be expected to operate in an environment where temperatures could range from $-40°$ C to 85° C and where the atmosphere is so thin it can be considered a vacuum. In this vacuum out-gassing of components can occur. The vacuum also brings about thermal issues due to limited heat transfer. Heat within a vacuum can only be transferred through conduction and heat radiation, not through convection. The use of tall heavy components has to be avoided due to the vibration and acceleration experienced by a satellite during launch. This section reassures the decision for the prototype to use an analogue means of control. This allowed the design to avoid the issue of SEUs that can afflict digital systems.

A large portion of the literature review consists of SMPS and related topics such as EMC and board layout. The benefits of SMPS over linear power systems was investigated as well as various SMPS topologies that could be used with the CubeSat EPS prototype. Typical SMPS topologies used in CubeSat power systems were determined in Section 2.7. Typical SMPS used by CubeSat EPS manufacturers includes the Boost, Buck and SEPIC DC-DC converters (Strain, 2010*b*; GomSpace, 2011). These topologies are discussed along with the Buck-Boost converter. The SEPIC DC-DC converter was chosen as the DC-DC converter to be used with the EPS. This converter topology was chosen due to its ability to accept an input voltage larger than or smaller than its output voltage. This gives the EPS prototype some flexibility when it comes to configuring the PV solar panels.

The control of DC-DC converters was thoroughly explored, mainly in the area of voltage-mode control. Feedback and control loops are discussed as a stable regulated voltage is required for the constant-voltage charge stage of the Li-poly battery once the EPS has switched away from MPPT control mode. The stability criteria for switch-mode power supplies were discussed and how compensation networks can better shape the closed loop frequency response of the system in order to improve the stability and the transient response of the closed loop system. Type 1, 2, 2a, 2b and type 3 compensation networks were discussed and tips supplied on selecting the correct type of compensation for differing SMPS power stage frequency responses.

EMC was discussed as the final EPS has the possibility of interfering with other subsystems within the CubeSat due to their close proximity. Correct board layout procedures were investigated as to reduce noise and interference between various parts of the SMPS. Noise and interference such as this could be created by electromagnetic fields generated by inductors. This interference could infiltrate sensitive signal lines such as those used in control, resulting in unexpected and possibly unstable operation of the SMPS. Instability of the SMPS could result in damage to the SMPS and possibly other subsystems within the satellite.

Having completed the literature review, consisting of the various aspects surrounding a satellite EPS, the design of the prototype commenced. The designed EPS prototype relied on purely analogue circuitry, improving reliability as the EPS could avoid SEUs brought on by radiation in the space environment. The EPS employed a FOCV based MPPT with battery bus allowing for a simple design while still harvesting energy from the PV solar panel with greater efficiency than a DET system.

A single MPPT channel was designed as a proof of concept. In a CubeSat mission the EPS could be used in a "box" layout incorporating three MPPT channels and connecting each channel to a PV solar panel on opposite sides of the CubeSat similar to GomSpace (2011). The designed MPPT proved to function well and track V_{mpp} effectively for a single MPPT channel. Initially, the prototype employed a solar panel disconnect MOSFET switch used during the sampling of V_{oc}. This was later abandoned as the SEPIC DC-DC converter essentially disconnected the PV solar panel from the EPS when disabled. Using the SEPIC DC-DC converter as the sole PV solar panel switch improved the accuracy in tracking V_{mpp}. The PV solar panel disconnect MOSFET switch brought about losses when large currents were drawn from the PV solar panel. These losses created inaccuracies in the measurement of the PV solar panel voltage while the SEPIC

DC-DC converter was active.

The EPS was able to accept a V_{mpp} from 3 V to 20 V with a maximum V_{oc} of 25 V. This would allow for a series string of 2 to 8 Spectralab UTJ solar cells to be used given that the maximum power available from the string did not exceed 10 W. This same design could handle various parallel combinations of PV solar cells given the power did not exceed 10 W. The ratio between V_{mpp} and V_{oc}, M_v, of the connected PV solar panels could easily be adjusted through the selection of resistor values. The design employed a control scheme that slid between MPPT and voltage regulation control depending on the power required by the satellite payloads and subsystems. The decision was taken to use a two cell Li-poly battery to supply power to payloads and subsystems. This allowed the design to be more flexible for future missions.

The EPS required a SEPIC DC-DC converter to handle the large input voltage range from the PV solar panel. The measured efficiency of the SEPIC DC-DC converter was 71% with an input voltage of 10 V and with the EPS under full load. This is comparable to the 3 W SEPIC DC-DC converters used by Clyde Space in their power systems. Clyde Space claims 79% efficiency from their SEPIC based MPPT with a 6 V input and their EPS under full load (Strain, 2010*a*,*b*).

The SEPIC DC-DC converter regulates effectively to 8.2 V as required for the constant-voltage charge state of the Li-poly battery once the EPS has switched from MPPT mode to voltage regulation mode. The battery under-voltage protection was satisfactory though it operated in a slightly narrower band than originally designed. The payloads are connected to the EPS when the battery voltage exceeds 7.24 V and disconnected when the battery voltage drops to 6.28 V. The originally designed thresholds were 6.2 V and 7.4 V.

The adjustable OCP located at the distribution, required to protect payloads from over-current, was tested and functioned as designed. The distributed bus could be switched through a logic level input. Testing of this logic level input was done with a simple jumper. This logic level input could be controlled by an OBC or another digital system within the CubeSat in a final mission. The OCP was able to automatically reset itself with the aid of a timed signal from the control board. The tested distribution board was set to trip at 300 mA and functioned flawlessly.

In closing the EPS performed adequately though the efficiency of the DC-DC converter could be improved upon. The EPS effectively harnessed the maximum power from the PV solar panel charging the battery and powering loads. The payload OCP protection performed perfectly disconnecting loads if excessive current was drawn from the EPS, while the battery under-voltage protection operated in a safe manner protecting the battery from over-discharge. The EPS slides seamlessly between MPPT mode and voltage regulation mode. Once the battery is sufficiently charged the EPS safely regulates the battery voltage to 8.2 V.

5.2 Problems encountered

During the design of the prototype EPS it was difficult to locate an Op Amp that had a high input impedance, rail-to-rail output voltage swing and that could operate at the battery voltage. The high input impedance was required by the S&H circuitry as an Op Amp with too low an input

impedance would result in the sampled voltage drooping thereby creating inaccuracies in the MPPT. The rail-to-rail output voltage made the design of the battery under-voltage protection circuitry simpler. The Microchip MCP6002 Op Amps chosen were the only components used in the EPS that could not operate at the battery voltage. This required the inclusion of some form of voltage regulation for the battery bus voltage. It was decided to use an LDO to regulate this voltage, the addition of this component would result in a slightly higher power dissipation, affecting the overall efficiency of the design. An LDO was chosen over a small SMPS due to its simplicity. Additionally, this LDO was not expected to source much current, resulting in a low level of power dissipation from the LDO. It was decided that the benefits of a small SMPS where insubstantial in comparison to using an LDO at such low power levels.

The first major problem encountered with the EPS prototype during testing was due to the PV solar panel disconnect MOSFET switch. This switch caused inaccuracies in the tracking of the maximum power point due to V_{pv} measurement errors. Using the SEPIC DC-DC converter as the PV solar panel disconnect switch proved more successful in tracking V_{mpp}. It is perceived by the author that this approach should work with a Buck DC-DC converter, though the MPPT was not tested with a Buck DC-DC converter as there was no need. The large input voltage range required the EPS to use a SEPIC DC-DC converter.

Initially it was observed that the PV solar panel voltage, V_{pv}, fluctuated significantly around the maximum power point voltage, V_{mpp}, when the SEPIC DC-DC converter was in MPPT mode. This fluctuation in voltage was reduced through the addition of a larger capacitor at the input of the EPS. The addition of more capacitance filtered the current drawn from the PV solar panel and steadied V_{pv} bringing it closer to V_{mpp}.

The emergency over-voltage and over-current protection used in protecting the battery from over-charging operated with no major issues. It was noticed that abruptly pulling the PWM to ground in an attempt to disable the DC-DC converter worked but produced an audible switching noise when this protection engaged. This protection system under normal conditions has no need to operate, but when tested did operate as expected. To alleviate the audible switching noise a 10 μF capacitor was added from both comparator inputs of the MAX4374 to ground in an attempt to reduce the rate at which the output of the comparators switched through a reduction in the rate at which the sensed voltage fluctuated. A better solution would be to pull the error signal to ground, this would cause the PWM to ramp down more gracefully as opposed to the abrupt forcing of the PWM output signal to ground. This would also maintain the switching frequency instead of introducing unexpected switching frequencies into the converter.

A method of incorporating voltage-mode control as well as MPPT tracking had to be developed. Though the final solution was simple it took some thought in bypassing the TL5001A's internal error amplifier and integrating the slide control between voltage regulation mode control and MPPT control modes.

5.3 Proposed future work and recommendations

Many improvements could be made to the designed EPS, some of these improvements are listed below:

- Coupled inductors could be used with the SEPIC converter to reduce the converter's physical footprint.
- More research could be done into current-mode control as this may improve the frequency and transient response of the SEPIC converter's control.
- Once a mission is defined and the configuration of the solar panels is known a Buck or Boost converter could be used instead of the SEPIC converter. The benefit to using either of these converters over a SEPIC converter is a reduction in component count, improved simplicity, a more compact design and possibly a more efficient system. The improvement in efficiency would be more noticeable with the use of synchronous converters.
- Voltage regulators could be placed before the distribution as to supply a regulated voltage to various subsystems as opposed to the battery bus voltage being distributed. The voltages that could be distributed would depend on the mission, but as seen in Chapter 2 +5 V and +3.3 V are common on CubeSat EPSes.
- Cell balancing of the battery could be implemented in order to better improve the longevity of the battery, though research would have to be done as to whether this is necessary, as this would depend on the lifespan of the specific CubeSat mission.
- Operational amplifiers with a wider operating voltage range could be used as a replacement to the MCP6002 used in the control circuitry. This would allow the control circuitry to operate at the battery voltage eliminating the need for the LDO. Eliminating the LDO simplifies the design, reduces the size of the design and reduces the power consumption of the EPS.
- The duration in which V_{oc} is sampled and the SEPIC DC-DC converter is disconnected could be reduced in an attempt to increase the efficiency of the MPP as during this time no power is supplied to the battery or loads from the PV solar array.

Bibliography

Ahmad, J. & Kim, H. 2009. A voltage based maximum power point tracking for low power and low cost photovoltaic applications. In *World Academy of Science, Engineering and Technology*, volume 60, pages 712–715.
Available at: `http://www.waset.org/journals/waset/v60/v60-121.pdf`

Alminde, L., Bisgaard, M., Gudmundsson, F., Kejser, C., Koustrup, T., Lodberg, C. & Viscor, T. 2001. *Power Supply for the AAU CubeSat.*
Available at: `http://www.cubesat.auc.dk/dokumenter/psu.pdf [12 January 2011]`

Anon. n.d. *French South African Institute of Technology.*
Available at: `http://iac2011.com/space-south-africa/fsati [8 September 2011]`

Basso, C.P. 2008. *Switch-mode Power Supplies: SPICE Simulations and Practical Designs.* New York: McGraw Hill.

Basso, C.P. 2012. Spice. Online.
Available at: `http://cbasso.pagesperso-orange.fr/Spice.htm [19 March 2012]`

Bettex, M. 2010. *Powering cube satellites: An electric propulsion technology for miniature satellites aims to give them more mobility and may eventually allow them to take on deep-space missions.*
Available at: `http://web.mit.edu/newsoffice/2010/cubesat-01115.html [4 November 2010]`

Brown, M. 2001. *Power Supply Cookbook.* 2nd edition. Massachusetts: Newnes.

Buchmann, I. 2001. *Batteries in a Portable World: a handbook on rechargeable batteries for non-engineers.* British Columbia: Cadex Electronics Inc.

Clark, C. & Lopez, A. 2006. Power system challenges for small satellite missions. In *Proceedings of the 2006 Small Satellites, Systems and Services Symposium, D. Danesy, Ed. The Netherlands: ESA.*

Clark, C., Strain, A. & Lopez Mazarias, A. 2008. A high performance, very low cost power system for microspacecraft. In *Eighth European Space Power Conference*, pages 1–11.

Clyde Space. 2009. *Small satellite solar panels.*
Available at: `http://www.clyde-space.com/documents/22625 [09 September 2013]`

Clyde Space. 2011. *Space Qualified Batteries.*
Available at: `http://www.clyde-space.com/documents/2381 [1 September 2011]`

Clyde Space. n.d. *Some useful information about CubeSats.*
Available at: `http://www.clyde-space.com/cubesat/som_useful_info_about_cubesats [12 October 2011]`

Connolly, R. 2000. *The P-POD Payload Planner's Guide.*
Available at: `http://www.cubesat.auc.dk/documents/planners_guide.pdf`
`[24 January 2011]`

Crompton, T. 2000. *Battery Reference Book.* 3rd edition. Newnes.

Czarkowski, D. 2001. *Power Electronics Handbook*, chapter 13, pages 211–223. California: Academic Press.

Day, C.A. 2004. The design of an efficient, elegant, and cubic pico-satellite electronics system. Master's thesis, California Polytechnic State University.

Department of Science and Technology. n.d. *The Ten-Year Plan for Science and Technology.*
Available at: `http://www.dst.gov.za/publications-policies/strategies-reports/...`
`...The%20Ten-Year%20Plan%20for%20Science%20and%20Technology.pdf [10 October 2011]`

Enertech International. 2007. *Specifications of Product: Rechargeable Li-ion Polymer Battery Model : SPB9345136UH1 (4.4Ah).* Online.
Available at: `http://www.ener1korea.com/eng/product/pdf/SPB9345136UH1.pdf`
`[10 April 2012]`

Erickson, R.W. *&* Maksimović, D. 2004. *Fundamentals of Power Electronics.* New York: Kluwer Academic Publishers.

Esram, T. *&* Chapman, P. 2007. Comparison of photovoltaic array maximum power point tracking techniques. In *IEEE Transactions on Energy Convervation*, volume 22, pages 439–449.

Fairchild Semiconductor. 1998. *Application Bulletin AB-9: Suppressing MOSFET Gate Ringing in Converters: Selection of a Gate Resistor.* Online.
Available at: `http://hmin.tripod.com/als/ccs/docs/pdf/Fairchild_AB-9.pdf`
`[4 October 2012]`

Flipsen, S. 2005. Alternative power sources for portables & wearables. Master's thesis, Delft University of technology.

GomSpace. 2011. *Datasheet for NanoPower P11u,P31u,P31u-S.*
Available at: `http://www.gomspace.com/documents/GS-DS-NANOPOWER-3.0.3.pdf`
`[14 September 2011]`

Griffiths, D.J. 2008. *Introduction to Electrodynamics.* 3rd edition. California: Pearson Benjamin Cummings.

Intusoft. 2005. *Modelling Solar Cells.*
Available at: `http://www.intusoft.com/nlhtm/nl78.htm [20 October 2011]`

Jordan, F. 2006. *SwissCube: Phase A - Electrical Power System (EPS) Final Report.*
Available at: `http://ctsgepc7.epfl.ch/03%20-%20Power%20system/...`
`...S3-B-EPS-1-1-Electrical_Power_System.pdf [14 October 2011]`

LeCroy, T. nd. Lab 748: Measuring phase margin. Online.
Available at: `http://cdn.teledynelecroy.com/files/appnotes/lab748.pdf [ 31 July 2013]`

Levins, D. 1991. Protection concepts used in spacecraft power systems. In *European Space Power Conference.*

Liedholm, E. 2010. Tracking the maximum power point of solar panels: A digital implementation using only voltage measurements. Master's thesis, Chalmers University of Technology.
Available at: `http://publications.lib.chalmers.se/records/fulltext/125967.pdf` `[18 January 2011]`

Linx Technologies. 2012. Application note an-00500 - antennas: Design, application and performance. Online.
Available at: `http://www.linxtechnologies.com/resources/documents/an-00500.pdf` `[25 October 2012]`

Maini, A.K. *&* Agrawal, V. 2011. *Satellite Technology: Principles and Applications.* 2nd edition. John Wiley and Sons Ltd.

Maniktala, S. 2006. *Switching Power Supplies A to Z.* Massachusetts: Newnes.

McDermott, J. 2008. *Space Mission Analysis and Design*, chapter 11, pages 407–427. 3rd edition. New York: Springer and Hawthorne: Microcosm Press.

Microchip. 2004. An947 - power management in portable applications: Charging lithium-ion/lithium-polymer batteries. Online.
Available at: `http://ww1.microchip.com/downloads/en/AppNotes/00947a.pdf [23 April 2012]`

Mohan, N., Undeland, T. *&* Robbins, W. 2003. *Power Electronics: Converters, Applications and Design.* 3rd edition. New Jersey: John Wiley and Sons Ltd.

Munakata, R., Lan, W., Hutputanasin, A. *&* Lee, S. 2009. Cubesat design specifications (cds) rev. 12. Technical Report, California Polytechnic State University.

National Semiconductor. 2006. *LM1117/LM1117I 800mA Low-Dropout Linear Regulator.*
Available at: `http://www.national.com/ds/LM/LM1117.pdf [19 October 2011]`

National Semiconductor. 2008. *Designing A SEPIC Converter.*
Available at: `http://www.national.com/an/AN/AN-1484.pdf [24 October 2011]`

O' Sullivan, D. 1994. Space power electronics - design drivers. *ESA Journal*, 18:1–23.

O' Sullivan, D. *&* Weinberg, A. 1977. The sequential switching shunt regulator s^3r. In *Proceedings of the Third ESTEC Spacecraft Power Conditioning Seminar*, pages 123–131. ESTEC.

Obland, M., Klumpar, D.M., Kirn, S., Hunyadi, G., Jepsen, S. *&* Larsen, B. 2002. Power subsystem design for the montana earth orbiting pico-explorer (merope) cubesat-class satellite. In *Aerospace Conference Proceedings, 2002. IEEE.*
Available at: `http://www.ssel.montana.edu/merope/abstracts/F197_2.pdf [21 January 2011]`

Patel, M. 2005. *Spacecraft Power Systems.* Florida: CRC Press.

Perol, P. 1998. Another look at the sequential switching shunt regulator. In *Proceedings of the Fifth European Space Power Conference*, pages 79–84.

Pongratananukul, N. 2005. Analysis and simulation tools for solar array power systems. Ph.D. thesis, University of Central Florida.

Puig-Suari, J., Chin, A., Coelho, R., Nugent, R. *&* Munakata, R. 2008. The cubesat: The picosatellite standard for research and education. In *AIAA SPACE 2008 Conference & Exposition.*
Available at: `http://www.cubesat.org/images/More_Papers/cps2008.pdf [2 November 2010]`

Pumpkin inc. 2009. Cubesat kit™linear eps: Rechargeable electrical power system for cubesat kit bus. Available at: `http://www.cubesatkit.com/docs/datasheet/DS_CSK_Linear_EPS_711-00338-D.pdf [26 September 2011]`

Ridley, R. 2006. Analyzing the sepic converter. *Power System Design Europe*, page 14.

Sony. n.d. Lithium ion rechargeable batteries: Technical handbook. Online. Available at: `http://www.sony.com.cn/products/ed/battery/download.pdf [23 May 2012]`

Spectrolab. 2008. *28.3% Ultra Triple Junction (UTJ) Solar Cells.* Available at: `http://www.spectrolab.com/DataSheets/TNJCell/utj3.pdf [18 October 2011]`

Strain, A. 2010*a*. *User Manual: CubeSat 1U Electronic Power System and Batteries: CS-1UEPS2-NB/-10/-20.* Available at: `http://www.clyde-space.com/documents/1819 [12 October 2011]`

Strain, A. 2010*b*. *User Manual: FleXible Electronic PowerSystem: CS-XUEPS2-41/-42.* Available at: `http://www.clyde-space.com/documents/1820 [12 October 2011]`

Texas Instruments. 2002. *TL5001, TL5001A Pulse-width-modulation control circuits.* Available at: `http://www.ti.com/lit/ds/symlink/tl5001a.pdf [19 October 2011]`

Texas Instruments. 2008*a*. *Designing DC/DC converters based on SEPIC topology.* Available at: `http://focus.ti.com/lit/an/slyt309/slyt309.pdf [24 October 2011]`

Texas Instruments. 2008*b*. *Power Supply Topologies.* Available at: `http://www.ti.com/lit/sg/sluw001d/sluw001d.pdf [14 October 2011]`

Texas Instruments. 2010. *NA555, NE555, SA555, SE555.* Available at: `http://www.ti.com/lit/ds/slfs022h/slfs022h.pdf [20 October 2011]`

Thomsen, M. 2009. *Michael's List of CubeSat Satellite Missions.* Available at: `http://mtech.dk/thomsen/space/cubesat.php [13 February 2013]`

Toorian, A., Diaz, K. *&* Lee, S. 2008. The cubesat approach to space access. In *Aerospace Conference, 2008 IEEE.*

Warwick, K. 1996. *An introduction to control systems.* Singapore: World Scientific Publishing.

Williams, T. 2001. *EMC for Product Designers.* 3rd edition. Oxford: Newnes.

Zhang, D. 2010. *Switching Power Supply Control Fundamentals.* Available at: `http://www.national.com/AU/design/courses/190/ [24 February 2011]`

Zhihao, Y. *&* Xiaobo, W. 2009. Photovoltaic system based on constant voltage mppt. In *Power and Energy Engineering Conference,2009. APPEC 2009. Asia-Pacific.*

Appendices

Appendix A

Measured efficiency of the EPS prototype

The efficiency of the EPS was measured with the Li-Poly battery replaced by the 1000μF capacitor, $C_{storage}$, used in Section 4.5.2. This would simplify the measurement of the efficiency of the DC-DC converter as the capacitor would charge quickly to the regulated output voltage, and also discharge quickly if the battery bus voltage was pulled down by excessive current draw by loads or circuitry. An example where this could be an issue would be when the battery is not fully charged, and testing were to be done. The power delivered by the EPS would be used in charging the battery as well as powering the EPS loads. The power would have to be measured at the input to the EPS, the output to the battery and the output to the loads. The capacitor would merely draw current until it reached the operating voltage of the loads currently drawing current. Similarly this would occur with the battery, but the time one would have to wait for this to occur would be significantly longer when using the battery.

A shunt resistor of 0.1 Ω, R_{shunt}, was placed in series with a bench power supply and connected to the solar panel input of the EPS. Connected to the output of the EPS was a 33 Ω, 5 W resistor, R_{load}. This load would draw approximately 2 W at 8.2 V for every 33 W resistor placed in parallel at the load. This resulted in tests for an output power of 2 W, 4 W, 6 W and 8 W. An illustration of this test setup can be seen in Figure A.1.

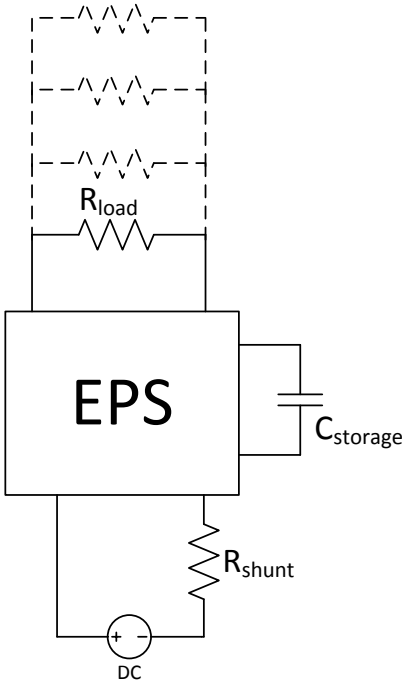

Figure A.1: Efficiency measurement setup

During testing the RMS voltage across the resistor at the input, R_{shunt}, was determined with an oscilloscope, along with the RMS input voltage located at the terminals of the PV solar panel input. The voltage across R_{shunt} was used to determine the input current to the EPS, this along with the voltage measured at the terminals of the PV solar panel input was used to determine the input power of the EPS. Similarly the voltage found at the output across R_{load} was used to determine the output power of the EPS, using the load resistance to calculate the output power.

The bench power supply was set to test the EPS with an input voltage of 3 V, 5 V, 10 V, 15 V and 20 V for the unmodified and modified EPS designs. Resulting in Tables A.1 to A.10.

Table A.1: Initial EPS efficiency at 3 V input.

V_{IN} [V]	I_{IN} [A]	P_{IN} [W]	V_{OUT} [V]	I_{OUT} [A]	P_{OUT} [W]	η [%]
2.97	1.12	3.32	8.18	0.24	2.00	60.15
3.09	2.16	6.67	8.18	0.49	4.01	60.11
3.00	4.55	13.63	7.67	0.63	4.86	35.67

Table A.2: Modified EPS efficiency at 3 V input.

V_{IN} [V]	I_{IN} [A]	P_{IN} [W]	V_{OUT} [V]	I_{OUT} [A]	P_{OUT} [W]	η [%]
3.06	1.04	3.18	8.21	0.25	2.01	63.31
3.14	1.92	6.03	8.21	0.49	4.04	66.95
3.14	2.90	9.09	8.28	0.68	5.62	61.81

Table A.3: Initial EPS efficiency at 5 V input.

V_{IN} [V]	I_{IN} [A]	P_{IN} [W]	V_{OUT} [V]	I_{OUT} [A]	P_{OUT} [W]	η [%]
4.91	0.68	3.34	8.15	0.24	1.98	59.35
4.72	1.24	5.85	8.13	0.49	3.96	67.62
4.63	1.74	8.06	8.10	0.67	5.42	67.31
4.46	2.84	12.66	8.14	0.96	7.80	61.60

Table A.4: Modified EPS efficiency at 5 V input.

V_{IN} [V]	I_{IN} [A]	P_{IN} [W]	V_{OUT} [V]	I_{OUT} [A]	P_{OUT} [W]	η [%]
5.08	0.62	3.15	8.20	0.24	2.01	63.78
4.95	1.20	5.94	8.22	0.49	4.05	68.11
4.93	1.61	7.94	8.21	0.67	5.52	69.61
5.02	2.30	11.55	8.23	0.97	7.97	69.02

Table A.5: Initial EPS efficiency at 10 V input.

V_{IN} [V]	I_{IN} [A]	P_{IN} [W]	V_{OUT} [V]	I_{OUT} [A]	P_{OUT} [W]	η [%]
9.88	0.34	3.36	8.18	0.24	2.00	59.46
4.82	0.61	5.99	8.18	0.49	4.01	66.89
9.79	0.82	8.03	8.18	0.68	5.53	68.89
9.68	1.17	11.33	8.18	0.96	7.87	69.51

Table A.6: Modified EPS efficiency at 10 V input.

V_{IN} [V]	I_{IN} [A]	P_{IN} [W]	V_{OUT} [V]	I_{OUT} [A]	P_{OUT} [W]	η [%]
9.99	0.33	3.30	8.13	0.24	1.97	59.85
9.95	0.59	5.87	8.12	0.49	3.95	67.25
9.98	0.78	7.78	8.12	0.67	5.40	69.43
10.08	1.10	11.09	8.19	0.96	7.89	71.17

Table A.7: Initial EPS efficiency at 15 V input.

V_{IN} [V]	I_{IN} [A]	P_{IN} [W]	V_{OUT} [V]	I_{OUT} [A]	P_{OUT} [W]	η [%]
14.94	0.24	3.59	8.18	0.24	2.00	55.71
14.89	0.41	6.10	8.17	0.49	4.00	65.47
14.86	0.55	8.17	8.17	0.68	5.52	67.50
14.78	0.78	11.53	8.16	0.96	7.83	67.95

Table A.8: Modified EPS efficiency at 15 V input.

V_{IN} [V]	I_{IN} [A]	P_{IN} [W]	V_{OUT} [V]	I_{OUT} [A]	P_{OUT} [W]	η [%]
14.97	0.23	3.44	8.18	0.24	2.00	58.01
14.95	0.41	6.13	8.20	0.49	4.03	65.69
14.96	0.54	8.08	8.19	0.68	5.54	68.62
15.09	0.77	11.62	8.17	0.96	7.85	67.58

Table A.9: Initial EPS efficiency at 20 V input

V_{IN} [V]	I_{IN} [A]	P_{IN} [W]	V_{OUT} [V]	I_{OUT} [A]	P_{OUT} [W]	η [%]
19.91	0.19	3.78	8.18	0.24	2.00	52.80
19.87	0.33	6.56	8.17	0.49	4.00	60.96
19.84	0.43	8.53	8.18	0.68	5.53	64.82
19.80	0.60	11.88	8.16	0.96	7.83	65.94

Table A.10: Modified EPS efficiency at 20 V input.

V_{IN} [V]	I_{IN} [A]	P_{IN} [W]	V_{OUT} [V]	I_{OUT} [A]	P_{OUT} [W]	η [%]
20.00	0.19	3.80	8.18	0.24	2.00	52.56
19.97	0.32	6.39	8.11	0.49	3.94	61.63
19.94	0.42	8.37	8.08	0.67	5.40	64.43
19.92	0.59	11.75	8.04	0.95	7.60	64.71

Appendix B

Measured PV current-voltage characteristic

The PV solar panel was connected in series to a fixed 0.1 Ω shunt resistor and a high power variable resistor. One channel of an oscilloscope was connected across the PV solar panel with the ground connected to the side with the fixed resistor. A second oscilloscope channel was connected across the fixed resistor. An illustration of this can be seen in Figure B.1, where both channels of the oscilloscope use a common ground and measure point A and B.

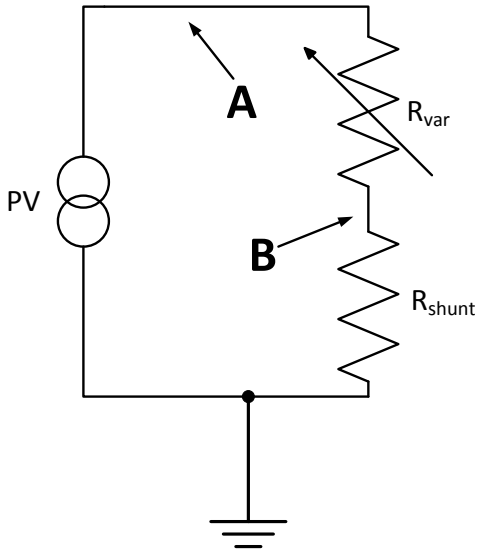

Figure B.1: PV solar panel MPP measurement

The voltage located at B is directly proportional to the current flowing through it, Ohms law. Thus the product of the voltage located at A and the voltage located at B is directly proportional to the power delivered by the PV solar panel. Using the maths function of the oscilloscope allows a visual representation of the power delivered by the PV solar panel but at $\frac{1}{10}$ the value. Through adjustment of the variable resistor, and the use of the oscilloscope, the maximum power delivered by the PV solar panel can be located. In this manner measurements can be done quickly relating

to power, current and voltage. The open-circuit voltage of the PV solar panel can be located by disconnecting the fixed and variable resistors, located at point B, and measuring the voltage from point A to ground.

Table B.1: I-V characteristic with the light box at 170 V.

Current [A]	2.00	1.85	1.61	1.40	1.18	1.02	0.80	0.61	0.41	0.20
Voltage [V]	3.06	3.78	4.03	4.18	4.31	4.41	4.52	4.61	4.71	4.80
Power [W]	6.11	6.99	6.49	5.84	5.10	4.48	3.61	2.81	1.91	0.97
V_{OC} **[V]**	5.02									
M_v	0.75									

Table B.2: I-V characteristic with the light box at 150 V.

Current [A]	1.50	1.32	1.11	0.90	0.71	0.50	0.31	0.20
Voltage [V]	2.70	3.79	4.15	4.33	4.46	4.50	4.70	4.76
Power [W]	4.05	4.98	4.60	3.88	3.16	2.30	1.43	0.95
V_{OC} **[V]**	5.02							
M_v	0.76							

Table B.3: I-V characteristic with the light box at 130 V.

Current [A]	1.05	0.90	0.80	0.72	0.60	0.50	0.41	0.30	0.21
Voltage [V]	0.26	3.95	4.12	4.30	4.43	4.51	4.58	4.67	4.73
Power [W]	0.27	3.55	3.28	3.09	2.64	2.27	1.87	1.40	0.97
V_{OC} **[V]**	4.84								
M_v	0.82								

Table B.4: I-V characteristic with the light box at 100 V.

Current [A]	0.50	0.45	0.40	0.35	0.30	0.25	0.20
Voltage [V]	0.15	3.43	3.87	4.07	4.22	4.38	4.65
Power [W]	0.076	1.54	1.56	1.43	1.27	1.09	0.92
V_{OC} **[V]**	4.88						
M_v	0.79						

Appendix C

SEPIC DC-DC converter MATLAB® scripts

This Appendix contains the MATLAB scripts used in calculating the SEPIC DC-DC converter components as well as the components required in the design of the compensation.

The SEPIC DC-DC converter script located in Section C.1 requires the selection of values for under the "SEPIC converter specs section" and "Switch specs" sections commented in the code. Upon running the script the outputs are displayed in the terminal window.

The SEPIC DC-DC converter compensation script calculates the required component values for Type 3 compensation. The values that need specifying are Gfc, fc, PM and PS. Descriptions of these variables can be seen in comments in the script. This script also sends it's output to the terminal window.

C.1 SEPIC DC-DC converter MATLAB® script

```
%% SEPIC DC-DC converter design calculations
% Author: Gavin Mutch

format short eng;
clear all;
close all;
clc;

%% SEPIC converter specs

fsw = 200e3;          %[Hz] switching frequency
VinMIN=3;             %[V] Minimum input voltage (1U solar panel voltage)
VinMAX=20;            %[V] Maximum input voltage (3U solar panel voltage)
Pout=10;              %[W] Maximum output power
Vout=8.2;             %[V] Designed output voltage, same as 2 x 4.1V Li-Po cells
Vripple=0.05*Vout;    %[V] Peak-to-peak output voltage ripple
Cs=10e-6;
```

```
Vd=0.5;             %[V] Diode forward bias volt-drop

%SEPIC design

Iout=Pout/Vout              %[A] Output current
Iin=Iout*(Vout/VinMIN)      %[A] Average input current

Dmax=(Vout+Vd)/(VinMIN+Vout+Vd)   %[%] Maximum duty ratio
Dmin=(Vout+Vd)/(VinMAX+Vout+Vd)   %[%] Minimum duty ratio

delta_Il=0.4*Iin           %[A] peak-to-peak inductor ripple current

L=(VinMIN/(delta_Il*fsw))*Dmax    %[H] Inductor value for L1 & L2
L1=L
L2=L

I_L1_pk=Iout*((Vout+Vd)/VinMIN)*(1+0.4/2)  %[A] Peak current for L1
I_L2_pk=Iout*(1+0.4/2)                     %[A] Peak current for L2

V_Cs_max=VinMAX                            %[V] Maximum voltage of Cs
I_Cs_rms=Iout*sqrt((Vout+Vd)/(VinMIN))     %[A] RMS current through Cs
delta_V_Cs=(Iout*Dmax)/(Cs*fsw)            %[V] voltage ripple across Cs

I_Cout_rms=Iout*sqrt((Vout+Vd)/VinMIN)     %[A] RMS current for Cout
Cout_ESR=(Vripple*0.5)/(I_L1_pk+I_L2_pk)   %[ohm] Maximum ESR for Cout
Cout=(Iout*Dmax)/(Vripple*0.5*fsw)         %[F] Output filter capacitance

I_Cin_rms=delta_Il/sqrt(12)                %[A] Input current RMS current

%% Switch specs [IRF7343]

Rds=0.065;  %[ohm] on state resistance of switch
Qgd=10e-9;  %[C] Gate-Drain "Miller Charge"

%Predicted gate current using 470 ohm pull up from PWM and ZXC2062E6 as
%driver
Rpullup=470;
Vsupply=5;
Ipullup=Vsupply/Rpullup;
hfe=100;

%[A] Gate drive current
Ig=Ipullup*hfe;

%% Switch design

%[A] pk switch current
I_Q1_pk=I_L1_pk+I_L2_pk;
%[A] RMS switch current
I_Q1_rms=Iout*sqrt(((Vout+VinMIN+Vd)*(Vout+Vd))/(VinMIN^2));

%[W] power dissipated by the switch
```

```
P_Q1=I_Q1_rms*Rds*Dmax+(VinMIN+Vout)*I_Q1_pk*((Qgd*fsw)/Ig)

%[V] reverse breakdown voltage of diode
Vrd=VinMAX+Vout

%[W] Power dissipated by the diode
Pdiode=Iout*Vd

%[V] Maximum switch voltage
Vq1=VinMAX+Vout
```

C.2 SEPIC DC-DC converter compensation MATLAB® script

```
%% Author: Gavin Mutch
% Compensation Design for Type 3 amplifier using k-factor method from
% Switch-mode power supplies: SPICE Simulations and Practical Designs
% by C. Basso

format short eng;
close all;
clear all;
clc;

%% Parameters required to calculate component values

%Gain required in dB, IE if gain at desired crossover
%frequency is -18dB, 18dB is required.
Gfc=-40;

%Desired crossover frequency in Hz
fc=45e3;

%Desired Phase at crossover frequency in degrees
PM=70;

%Open-loop phase shift at crossover frequency in degrees
PS=-230;

%% Component values

Boost=PM-PS-90;                     %[degrees] Required boost by amplifier
k=(tan(deg2rad((Boost/4)+45)))^2;   %k-factor
G=10^(Gfc/20);                      %[V/V] required Gain in V/V

R1=10e3                             %[ohm] R1 is also refered to as Rupper
C2=1/(2*pi*fc*G*R1)                 %[F]
C1=C2*(k-1)                         %[F]
R2=sqrt(k)/(2*pi*fc*C1)             %[ohm]
R3=R1/(k-1)                         %[ohm]
C3=1/(2*pi*fc*sqrt(k)*R3)           %[F]
```

Appendix D

Prototype schematics

See attached CD-ROM for schematics in PDF format.

The schematics are located under "./Schematics - PDF/".
Within this directory the following sub-directories exist, each containing schematics of a different prototype board. These sub-directories are located at:

./Schematics - PDF/Control/
./Schematics - PDF/DC-DC/
./Schematics - PDF/Distribution/

Directory "./Schematics - PDF/Control/" contains the following schematics:

batteryUndervoltage.pdf	This file contains the battery under voltage protection circuit schematic.
Compensation.pdf	This file contains the feedback compensation circuit schematic.
MPPT.pdf	This file contains the basic elements required for the MPPT, excluding the timers and sample and hold.
SandH.pdf	This file contains the sample and hold circuit schematic.
Timers.pdf	This file contains the circuit schematics of the timers used in driving the MPPT, along with the resettable over current protection.

Directory "./Schematics - PDF/DC-DC/" contains the following schematics:

PWM.pdf	This file contains the PWM, LDO, over voltage and over current battery protection circuit schematics.
SEPIC.pdf	This file contains the basic SEPIC converter circuit schematic.

Directory "./Schematics - PDF/Distribution/" contains the following schematics:

Distribution.pdf	This file contains the distribution over current protection.

Appendix E

Component datasheets

See attached CD-ROM for component datasheets.

The datasheets are located under "./datasheets/".
Within this directory the following sub-directories exist, each containing a category of component types. These sub-directories are located at:

./datasheets/Batteries/
./datasheets/BJTs/
./datasheets/Current amplifiers/
./datasheets/Diodes/
./datasheets/LDOs/
./datasheets/MOSFETs/
./datasheets/Opamps/
./datasheets/PWM/
./datasheets/Timers/

Appendix F

PCB Gerbers and NC drill files

See attached CD-ROM for PCB Gerber files.

The Gerber and NC drill files used in producing the PCBs are located under "./PCB Gerbers/". Within this directory the following sub-directories exist, each containing a different prototype board. These sub-directories are located at:

./PCB Gerbers/PCB-ControlRev1_1/
./PCB Gerbers/PCB-DCDCrev1_1/
./PCB Gerbers/PCB-DistributionRev1_1/