Cape Peninsula
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Development of a multi-cell inverter topology for driving nonlinear piezoelectric load.

by

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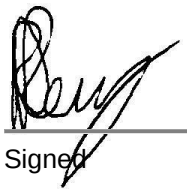
DECLARATION

I, Rory Adriaan Pentz, declare that the contents of this dissertation represent my own unaided work, and that the dissertation has not to my knowledge previously been submitted for academic examination towards any qualification. Furthermore, it represents my own opinions and not necessarily those of the Cape Peninsula University of Technology.



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ABSTRACT

This report presents the design and development of a five cell multicell inverter for driving a piezoelectric load. The multicell inverter was chosen for this application as it became evident that it would be more suitable for driving piezoelectric transducers due to its high apparent switching frequency. The multicell inverter was designed using DirectFET's as this type of FET has a high current switching ability in a very small package. A positive and negative bootstrap power supply was incorporated in the design to reduce the number of supplies to power the gate drive circuits of the multicell inverter.

Three compensation networks were designed and constructed to investigate which one would transfer the most energy to the piezoelectric transducer. It was also important to investigate whether these compensation networks were able to reduce the harmonic content produced by the multicell inverter. This is necessary in order to excite the transducer correctly. It was found that the Q-Matching compensation network reduced the harmonic content applied to the load the most. Experiments were also conducted to determine if the advantage of the apparent frequency of the multicell inverter would mean that the piezoelectric load could be driven directly with the multicell inverter without any damage to the transducer. It was however required to increase the applied apparent power to the transducer to compensate for the reactive component of the load in order to melt the plastic which was used as the load to the transducer.

Experiments were conducted to determine if the charge on the cell capacitors of the multicell inverter would stay balanced while driving a non linear load such as a piezoelectric transducer. The results showed that the voltages stayed balanced when driving the piezoelectric transducer.

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GLOSSARY

Abbreviations

AC	: Alternating Current
DC	: Direct Current
BVD	: Butterworth-Van Dyke
f	: frequency
FET	: Field Effect Transistor
Hz	: Hertz
kHz	: kilo Herts
MHz	: Mega Hertz
I_{THD}	: Total harmonic distortion contained within the current
Q-factor	: Quality Factor
PCB	: Printed circuit board
P.F.	: Power factor
PSpice	: Simulation Program for Integrated Circuit Emphasis
PWM	:Pulse Width Modulation
PZT	: Lead zircon ate titanate is a form of piezoelectric ceramic material
SPWM	: Sinusoidal Pulse Width Modulations
V_{THD}	: Total harmonic distortion contained within the voltage

Symbols

A	: area of the piezoelectric transducer
A_{con}	*:* area of the copper conductor
A_e	: the effective area of the core
A_w	: the winding window
B	: Susceptance
B_{max}	: the maximum flux density
β	: the peak current ($I \times \sqrt{2}$)
C_k	: the cell capacitance
C_M	: the compliance of the oscillating body
C_O	: clamped static capacitance of the piezoceramics
C_P	: capacitor connected in parallel with transducer to reduce the impedance.
C_S	: The series capacitor used in Q-Matching
C_1	: the motional mass of the mechanical oscillating circuit
C_2	: the sum of C_P and C_O
D	: the duty cycle
E	: Voltage
F	: Force
f_a	: Anti-resonant frequency of the piezoelectric transducer
f_r	: Mechanical resonant frequency of the piezoelectric transducer

f_m : the frequency of maximum admittance

f_n : the frequency where the admittance is a minimum

f_O : the frequency of the output signal

f_p : the parallel resonance frequency

f_r : resonance frequency

f_s : the series resonance frequency of the motional arm where the conductance is a maximum

f_{sw} : the switching frequency

f_1 and f_2 : are the point where the conductance is half the value of G_{MAX}

G : Conductance

G_C : clamped conductance

G_{MAX} : the conductance of the motional arm

h_x : piezoelectric constant

I : Current

I_{AVG} : Average current flow

I_{cbs} : the Bootstrap capacitor leakage current

I_{dc} : the output dc current

l_g : is the length of the air gap

I_{peak} : Peak current

I_{qbs} : the quiescent current for the high-side driver

I_O : Output current

I_p : the primary current of the transformer

I_s : and secondary current of the transformer

Kc : the copper fill factor

k : number of (variable)

k_{eff} : electromechanical coupling coefficient

L : the inductance of the inductor

L_1 : the stiffness of the mechanical oscillating circuit

L_s : Series compensation inductor

L_P : Parallel compensation inductor

M : the motional inductance giving a measure of mass

N : Transformer ratio

N_p : the primary turns ratio of the transformer

N_s : the secondary turns ratio of the transformer

ρ : Density

p : number of cells

P : Power

P_D : the power being dissipated

P_{con} : conduction losses

P_{rr} : reverse recovery losses

P_{sw} : the switching losses

P_T : the total power dissipation

Q_g : the total gate charge required by the MOSFET

Q_{GD} : Gate charge between the gate and drain of a FET

Q_{GS} : Gate charge between the gate and source of a FET

Q_{ls} : the level shift charge required per cycle

Q_m : mechanical Q-factor

Q_{rr} : the reverse recovery charge

$R_{DS(on)}$: the resistance between drain and source when the FET is on

R_g : Gate resistance

R_M : the mechanical impedance

R_S : Source resistance

R_P : the resistance of the load or equal to R_1

R_1 : the dissipative power losses of the piezoelectric load

R_θ : the thermal resistance

$R_{\theta(h\text{-}a)}$: thermal resistance of heat sink-to-ambient

$R_{\theta(c\text{-}h)}$: thermal resistance of case-to-heat sink

$R_{\theta(j\text{-}a)}$: thermal resistance from junction to ambient

$R_{\theta(j\text{-}c)}$: thermal resistance of junction-to-case

T_a : ambient temperature

T_C : Curie temperature

T_c : The maximum case temperature

ΔT : the temperature deference

t : thickness on the transducer

t_{off} : the turn off time

t_{on} : the turn on time

t_{SW} : the switching time which is the inverse of the switching frequency

V_{CC} : the supply voltage applied to the gate drive IC

V_{cell} : the voltage across the switching device

V_{Ck} : Voltage across cell capacitor

ΔV_{Ck} : the capacitor ripple voltage

V_d : Input voltage for the multicell inverter

V_{dc} : Supply voltage

V_f : the forward voltage drop across the bootstrap diode

V_{gate} : the maximum voltage the gate drive circuit will produce

$V_{GS(th)}$: the maximum gate-to-source threshold voltage required to turn on the MOSFET

V_{LS} : the volt drop across the low-side FET

V_{min} : the minimum voltage between pins V_B and V_S of the gate drive IC

V_p : the primary voltage of the transformer

V_O : The output voltage

V_{ripple} : ripple voltage

V_s : the secondary voltage of the transformer

V_S : Source voltage

v : Velocity

Y	: Admittance
Z_L	: Impedance of the load
Z_O	: Characteristic acoustic impedance
Z_P	: Impedance seen from the primary side of the transformer
α	: the transformation ratio
ε^s	: camped permittivity
ω	: angular frequency
μ_i	: the permeability of the copper
μ_0	: the permeability of free space
λ	: Wavelength
δ	: the skin depth
σ	: the conductivity of copper
Φ	: the phase-shift between the control signals

CHAPTER ONE

Introduction

1.1 Background

Ultrasound includes all acoustical energy that is not part of the audible range of a human being. The maximum upper audible range is 20 kHz and this value deteriorates as the age of an individual increases. This results in ultrasonic applications using frequencies above 20 kHz. Ultrasonic industries have increased considerably; they include medical diagnostics, atomisation of liquids, welding of plastics and metals, food and liquid processing and cleaning. (Kuttruff, 2013, p. 637) The equipment used in ultrasonic application, uses piezoelectric transducers to produce the acoustic energy needed to perform the work.

Piezoelectric material is among the most commonly used material to produce ultrasonic transducers. This material generates a potential difference when pressure is applied to the material. The inverse processes also occurs when a potential is applied, the shape of the material changes. As this phenomenon can be used to change electrical energy into acoustical energy, the material is used to produce transducers. The characteristics of piezoelectric transducer change with reference to resonant frequency, Q-factor and impedance, with the change of applied power and the load to the transducer. (Green, 2002, p. 110) The problem about changing resonance frequency with different power levels is not considered in this thesis. This dynamic behaviour of the load must be addressed in order to transfer maximum energy to the transducer. The impedance of the piezoelectric transducer contains a capacitive reactive component, it's important to attend to this problem in order to transfer maximum energy to the transducer. (Green, 2002, p. 110)

Many of the ultrasonic applications require high power. Most high power electronic circuits generate harmonics in their own right. Piezoelectric transducers have different resonant modes and only one mode should be excited at a time as exciting different modes at the same time can cause physical damage to the transducer (Ferroperm, 2006). When a piezoelectric transducer is driven by a source using PWM, the source doesn't only produce the fundamental frequency to stimulate the transducer but the output signal of the source also contains harmonics at multiples of the switching frequency. (Wilkinson, et al., 2003, p. 1309) These harmonics can stimulate other resonant modes at the same time while the mechanical resonant mode of the transducer is stimulated and could cause spurious modes. These spurious modes will cause the transducer to be excited incorrectly and can lead to its destruction. (Ferroperm, 2006)

1.2 Problem statement

There is an increasing need to drive high power transducers which require switching devices that can handle a high product of voltage and current. These switching devices normally have high conduction losses, low switching speeds, and high cost (Meynard, 1997, p. 356).

Multilevel inverter topologies are used to overcome this problem by placing switching devices in series, thereby reducing the required voltage rating of the individual switch (Molepo, 2003, p. 11). Switching devices with lower blocking voltages normally have lower conduction losses and high switching speeds (Meynard, 1997, p. 356).

There are mainly five types of multilevel inverter topologies (Wilkinson, 2004, p. 2):

- The plain series connected pseudo multilevel topology.
- The neutral-point-clamped multilevel topology.
- The multicell topology.
- The series-stacked multilevel topology.
- The cascaded multilevel topology

The multicell topology has an added advantage that the control signals applied to the switching devices can be phase-shifted in order to achieve a high apparent switching frequency with a frequency of the product of the number of cells and the switching frequency (Meynard, 1997, p. 356). Therefore the harmonic spectrum obtained from the multicell inverter will have a fundamental frequency with a value of the reference signal and the first significant harmonic situated at the point of the apparent frequency. This high apparent frequency will result in less distortion being produced due to a reduction of the overlapping of side-band harmonics. The high apparent frequency will also reduce the need for a large output filter as the cut-off frequency of the low-pass filter can be chosen at a much higher frequency compared to the conventional switch mode topologies. (Wilkinson, 1997, p. 14).

The output signal of the Multicell inverter contains unwanted harmonics due to the nature of switch-mode topologies. These harmonics need to be reduced as these harmonics can stimulate other resonant modes while the mechanical resonant mode is excited. Traditionally a low-pass filter will be used to filter out these unwanted harmonics and help to reduce distortion of the output signal (Wilkinson, 1997, p. 4). This method of filter design does not work effectively in this situation because the impedance of the piezoelectric load changes as applied power increases. This will cause a mismatch of impedances between the load and the source and will result in inefficient transfer of power. (Horowitz, 2005, p. 5).

Interfacing a piezoelectric transducer to a source presents the following two main challenges:
Traditional methods of impedance matching, of which the π- and T-matching networks are well known (Young, 1994, p. 190), have high insertion losses which will result in large energy losses within the impedance matching network and cannot be used in this application (Bell, 2008, p. 715). Impedance matching with impedance matching transformers is also an option, but due to the impedance of the transducer changes will still result in some degree of mismatch (Boylestad, 1994, p. 940). An alternative method would involve the implementation of a resonant filter, like Q-Matching, which also incorporates a type of impedance matching (Bruyn, 2003, p. 31) (Smith, 2006, p. 129).

At the mechanical resonant frequency of the piezoelectric transducer the model of the transducer reduces to a capacitive reactive component in parallel with a resistive component. This capacitive component is due to the clamped static capacitance of the piezoceramics of the transducer. (Prokic, 2004) In order to transfer maximum energy this capacitive reactive component must be eliminated by introducing an inductive reactive component so that the piezoelectric transducer can react as a resistive load. The one method is by placing an inductor in parallel with the transducer and the other method is by placing an inductor in series with the transducer. (J van Randeraat, 1968, p. 101)

1.3 Objectives of the research

The first objective of this research was to design and construct a five-cell multicell inverter which was used to drive a piezoelectric load. The five-cell multicell inverter was constructed using DirectFET's as the switching devices. These DirectFET's have advantages that lend them to being used for switching applications. This inverter has ten switching devices requiring its own isolated power supply, as each driving circuit is situated at a different ground potential. With the implementation of bootstrap power supplies, only a positive and a negative bootstrap circuit is needed instead of ten independently isolated circuits.

The second objective of this research was to examine three types of compensation networks, series compensation inductor, parallel compensation inductor and Q-matching in order to reduce the harmonic content of the output from switch-mode topologies while ensuring maximum transfer of energy.

A further objective was to determine if the voltages across the cell capacitors stay balanced as the piezoelectric load is driven by the multicell inverter. This could be a problem as the piezoelectric transducer doesn't behave like a load with a resistive impedance but also contains a capacitive reactive component. This reactive component will result in that some of the applied energy to the load will be reflected back to the source and this would imply that the source must absorb this energy. This absorbing of the reflected energy might cause the cell capacitors to deviate to voltage level other than that which the theory states. This would result in the increase of distortion of the output signal resulting in the production of unwanted harmonics.

The last objective was to examine if the piezoelectric transducer could be driven without any compensation network, only relying on the line impedance of the wires connecting the transducer to the inverter, as the first harmonic is situated at 1.5MHz with the driving signal at 22.1 kHz.

With the main objectives of this project introduced, the following research questions are significant:

- Which compensation network will result in the best energy transfer while driving a piezoelectric load?
- Which compensation network will reduce the harmonic content of the output signal?
- While driving a non-linear piezoelectric load, will the voltages of the cell capacitors still balance naturally?

- Can the piezoelectric transducer be driven by a multicell inverter without a filter while exciting only the mechanical resonant mode?

1.4 Research methodology

A literature research was done on different types of multilevel inverters. This led to further investigation of the multicell inverter as this typology presented the best advantages in order to drive a piezoelectric transducer. Information on how piezoelectric material behaves allowed the generation of an electrical model of a piezoelectric load for simulation purposes. Investigation on filter design revealed why the behaviour of the piezoelectric material did not permit the use of a traditional low pass filter for effective power transfer. Two different types of compensation networks were identified that would "cancel" the capacitive reactive component of the piezoelectric transducer's impedance which would promote more efficient power transfer. A third compensation network that was evaluated is a type of resonant filter that also incorporate a form of impedance matching.

A multicell inverter, using DirectFET's as switching devices, with a positive and a negative bootstrap power supply and the three compensation networks, was constructed. A comparison of these three compensation networks was made to establish which one performed the best in terms of transferring the most energy to the load while reducing the harmonic content produced by the multicell inverter. The piezoelectric transducer was also driven by the multicell inverter to establish if it could be driven without any filtering of the harmonics produced by the multicell inverter. The voltages of the cell capacitors and the time it took to charge to their stable values were compared to the theoretical values and results obtained from simulations.

1.5 Delineation of the research

This research was based around driving a piezoelectric transducer, model MPI-20 kHz-3 kW (502/932R, Branson Converter), with a mechanical resonant frequency of 22.1 kHz, with a five-cell multicell inverter. The controller (developed as part of another Masters project) for the multicell inverter was limited to a single frequency and therefore the performance of the compensation networks which were connected to the piezoelectric transducer could only be tested at that frequency with the multicell inverter. This controller generated the gate signals for the ten switches for the multicell inverter. The simulation model developed for the piezoelectric transducer was used in PSpice in order to be driven by a voltage source to obtain the response of the piezoelectric model with deferent compensation networks. This process was then repeated by driving the piezoelectric transducer with an audio amplifier and the different compensation network. This research did not consider the dynamic behaviour of the piezoelectric transducer when the applied power is varied; although effort was made to keep the power to the transducer constant.

1.6 Significance and contribution of the research

This study resulted in the design of a prototype, 5-cell multicell inverter that can drive a piezoelectric load at a mechanical resonant frequency of 22.1 kHz. This prototype also incorporated DirectFET's as switching devices and two bootstrap power supplies. Recommendations were made as to what

compensation network performed the best in terms of power transfer while driving a non-linear load. The compensation networks were also evaluated to see which one reduced the harmonic content produced by the multicell inverter the most. The piezoelectric transducer was driven by the multicell inverter without any compensation network successfully without any damage to the transducer. It was also shown that the cell voltages of the multicell inverter stayed balanced.

1.7 Structure of the thesis

The structure of the document is as follows:

- Chapter two starts with a brief history of the piezoelectric material, the properties of the material and an overview of how piezoelectric material behaves. The chapter continues with the background of the different types of models and how they played a role in developing the simplified BVD model which is an electrical model of the piezoelectric transducer. The BVD model was used and a model for the transducer was developed in order to simulate this non-linear material. This model will be used to evaluate the interaction of the multicell inverter with a piezoelectric transducer.
- Chapter three provides an overview of multilevel inverters. It covers in detail a description of the multicell inverter, “balance booster” circuit and bootstrap power supply. The multicell inverter will be used as a source to drive the piezoelectric load
- Chapter four describes how the three compensation networks work and how to design them. The objective of these compensation networks is to determine which compensation network is the most suited for this application.
- Chapter five states the specifications of the system and discusses the design procedure of the multicell inverter, the bootstrap power supply and the three compensation networks.
- Chapter six looks at the experimental setup and the result obtained.
- Chapter seven presents the conclusion and recommendation for future work.

CHAPTER TWO

Nonlinear piezoelectric loads

Driving a piezoelectric transducer with a multicell inverter can be challenging. It is therefore important to understand how this type of material functions and how it is used to produce a piezoelectric transducer. Using simulation software to determine how the piezoelectric transducer will react to the multicell inverter is important as this can reduce time wastage. Therefore research was done to determine how a model of a piezoelectric transducer can be produced. This information was implemented to obtain an electrical model of the transducer.

2.1 Background

The phenomenon of piezoelectric behaviour was first discovered in single crystals by J. and P. Curie in 1880. In 1946, scientists discovered that $BaTiO_3$ (Barium Titanate) ceramics could be altered to have piezoelectric properties by the application of an electric field. This new finding made the discovery of a number of piezoceramic materials, and the Lead Zirconate Titanate (PZT) family in 1956, possible. PZT soon replaced $BaTiO_3$, due to its increased sensitivity and higher operating temperature than single crystals. Ceramic materials have a higher sensitivity and are easier to fabricate into a variety of shapes and sizes. Single crystals must be cut along certain crystallographic directions, thus limiting the possible shapes and sizes produced by this material. (Ferroperm Piezoceramics, 2003)

Piezoelectric material is formed by the application of a poling process to ferroelectric ceramics. This process consists of heating the ferroelectric ceramic to its Curie temperature (T_C) while applying a poling voltage to the material. This will cause the randomly oriented dipole's direction to change according to the applied electrical field. The material is gradually cooled while the electrical field is applied. When the material is at room temperature, the applied electric field can be removed. After the poling process is completed, a voltage with the same polarity as the poling voltage will cause expansion along the poling axis and contract perpendicular to the poling axis. (Ferroperm Piezoceramics, 2003)

Piezoelectric material is used to produce ultrasonic transducers. The piezoelectric effect is when piezoelectric material generates a charge when pressure is applied to the material. The inverse piezoelectric effect occurs when an electrical field is applied to the material, namely the shape will change. This material can be used as a transducer for transforming electrical energy into mechanical energy and vice versa. When an AC voltage is applied to the material, it will cause the material to vibrate. The acoustical waves caused by the mechanical vibration of the material will have the same frequency as the applied electrical voltage. (Ferroperm Piezoceramics, 2003)

2.2 Piezoelectric modes of vibration

The modes of vibration depend on the geometry of the piezoelectric material. Pertaining to piezoelectric disc, they have mainly two different types of resonance modes:

- Radial-medium diameter or planar resonance mode is where the frequency matches a standing half-wave with a length equal to the diameter of the transducer material. At this frequency the primary vibration mode takes place in a planar direction with the oscillating change in diameter (See Figure 2.1) (Ferroperm, 2006).

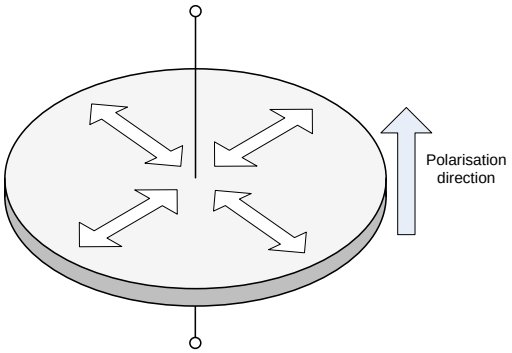

Figure 2.1: Radial-medium vibration mode of piezoelectric material. (Ferroperm, 2006)

- Thickness resonance mode is when the wavelength matches a standing half-wave in the thickness direction. At this frequency the primary vibration mode takes place in the thickness direction with the oscillating changes in thickness (See figure 2.2) (Ferroperm, 2006).

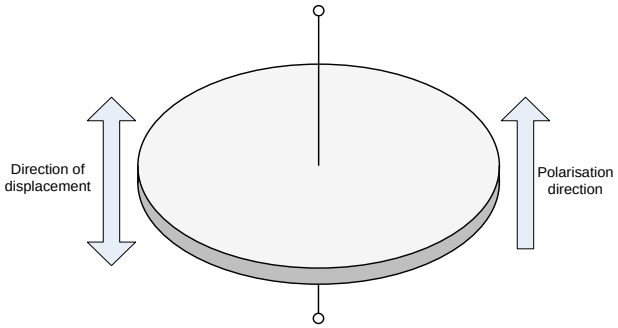

Figure 2.2: Thickness resonance mode of piezoelectric material. (Ferroperm, 2006)

If these two types of modes have fundamental resonances close to each other, there will be some interference between them which creates so-called spurious modes (e.g. bending vibration modes). Additionally each fundamental mode has several overtones which can also be located close to a higher fundamental mode. These overtones can also cause spurious modes when they interact with other fundamental modes (Ferroperm, 2006).

Care must be taken to excite the transducer correctly in order to avoid these spurious modes, as the effects of these spurious modes will cause the one resonance to either force the other resonance away from its natural position or to split it into several smaller sub-resonances. These situations could have serious implications for the operation of the piezoelectric load, and therefore preventative action needs to be taken. (Ferroperm, 2006).

2.3 Modelling a piezoelectric transducer

Warren Mason developed an electro-mechanical model based on network theory to describe the behaviour of a piezoelectric transducer (see Figure 2.3) (Mason, 1942, p. 205). The model has been widely used for free and mass loaded resonators, transient response, material constant determination, and other applications.

2.3.1 Mason's model

The model presents an equivalent circuit that separated the piezoelectric material into an electrical port and two acoustic ports linked through an electromechanical transformer. The transformer's ratio represents the coupling between the electrical and mechanical systems. One of the alleged problems with the model is that it required a negative capacitor at the electrical port. (Sherrit, et al., 1999, p. 921)

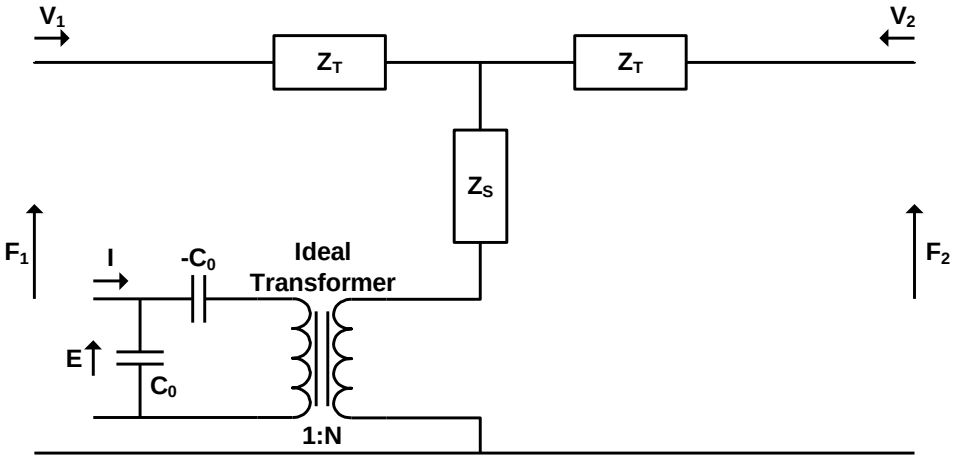

Figure 2.3: The Mason's model for equivalent electromechanical circuits that are used to represent the behaviour of a piezoelectric transducer. (Sherrit, et al., 1999, p. 921)

The electrical port conforms to standard electrical elements where the voltage, *E*, is defined by the product of the current, *I*, and the total impedance seen from the electrical port. The acoustical port is defined in terms of force, *F*, which is defined by the product of the velocity, *v*, and the characteristic acoustic impedance Z_O. The acoustic impedance is proportional to the product of the density, ρ, the area of the piezoelectric transducer, *A*, and the velocity of the piezoelectric material. (Sherrit, et al., 1999, p. 921)

The circuit parameters for Mason's equivalent electromechanical circuit are defined by the following equations (see Figure 2.3) (Mason, 1942, p. 205):

$$Z_T = jZ_O \cdot \tan\left(\frac{k \cdot t}{2}\right) \tag{2.1}$$

$$Z_S = j\frac{Z_O}{\sin(k \cdot t)} \tag{2.2}$$

where $k = \frac{2\pi}{\lambda} = \frac{\omega}{v}$; *k* is the wave number, *λ* is the wavelength, *ω* is the angular frequency, and *t* is the thickness of the transducer.

The electrical capacitance can be calculated by the following equation:

$$C_O = \frac{\varepsilon^S A}{t} \tag{2.3}$$

where ε^S is the clamped permittivity.

The transformer ratio can be calculated by the following equation:

$$N = h_x C_O \tag{2.4}$$

where h_x is the piezoelectric constant.

The capacitor, $-C_O$ illustrated in Figure 2.3, symbolises the excitation of the piezoelectric transducer when an electrical field, which is parallel to the wave propagation direction, is applied. When the applied electrical field is transverse to the wave propagation direction, the negative capacitor can be ignored.

2.3.2 Simplified Mason's model

If an acoustical load is only applied to the one port of the model, the model can be reduced as seen in Figure 2.4. The primary side of an ideal transformer is used to couple the electrical terminals to the mechanical motional arm on the secondary side. C_o represents the capacitance formed by the piezoelectric ceramic and the cable. The series motional arm consists of C_M (the compliance of the oscillating body), M (the motional inductance giving a measure of mass) and R_M (the mechanical impedance) (Smith, 2006, p. 11).

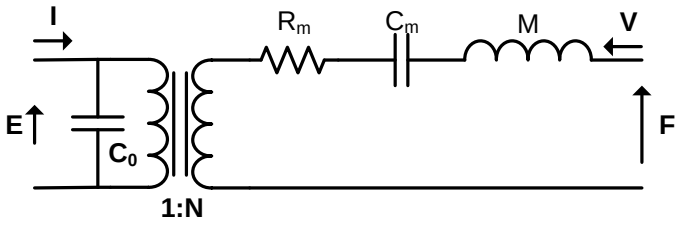

Figure 2.4: Simplified Mason's model where the oscillator is free at the one acoustical port and loaded on the other acoustical port. (Smith, 2006, p. 11)

2.3.3 The Butterworth-Van Dyke model

In order to deliver maximum ultrasonic power to a piezoelectric load, we need a simple and practical equivalent model which is expressed in electrical parameters. In such a model we should know which particular components represent the purely electrical and which components represent the mechanical or acoustical nature of the transducer, and how to represent the mechanical load. The best lumped parameter equivalent circuit for piezoelectric loads for an isolated vibration mode are shown to be the Butterworth-Van Dyke (Figure 2.5) which is derived by simplification of Mason's equivalent model. This equivalent circuit produces the least complex piezoelectric impedance model based on experimental results and electromechanical analogies. (Prokic, 2004, pp. 1-3)

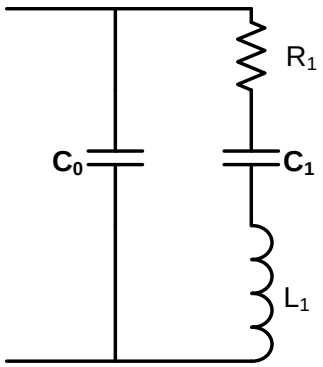

Figure 2.5: The Butterworth-Van Dyke (BVD) one port equivalent electromechanical circuit. (Prokic, 2004, pp. 1-3)

C_O is the clamped static capacitance of the piezoceramics, C_1 is the motional mass of the mechanical oscillating circuit, L_1 is the stiffness of the mechanical oscillating circuit and R_1 is the dissipative power losses. These dissipative power losses included losses from the joints, planar friction losses between piezoceramics and metal parts, mounting elements, material hysteresis-related losses and the load applied to the transducer. (Prokic, 2004, pp. 1-4)

2.3.3.1 Admittance curve and vector diagram

The Butterworth-Van Dyke (BVD) model requires an admittance plot (Figure 2.6) from the piezoelectric load as this enables us to produce an admittance vector diagram (Figure 2.7). The admittance vector diagram together with the admittance plot will provide all the information needed to calculate the different parameters for the BVD model.

The admittance plot in Figure 2.6 represents the different resonant modes of the transducer (model MPI-20kHz-3kW 502/932R Branson Converter). The admittance peak around 22.1 kHz represents the thickness resonant mode. In examining the admittance peaks, the dotted and solid line in Figure 2.6, around 22.1 kHz, it will be notice that the Q-factor, admittance and resonate frequency of the system changes as the transducer is loaded.

Admittance, Y, consists of a real part, conductance (G), plus an imaginary part, susceptance (B):

$$Y = G + jB \tag{2.5}$$

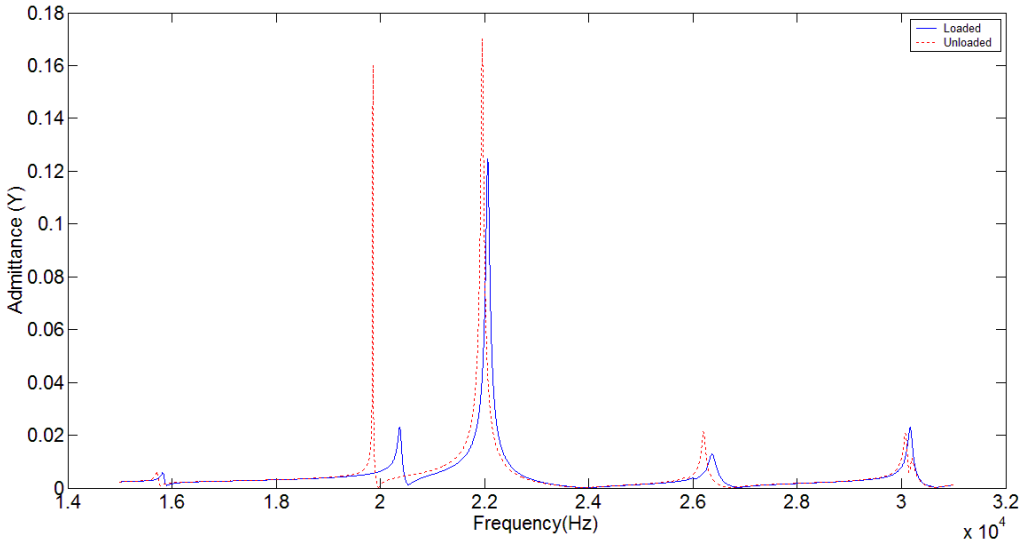

Figure 2.6: An admittance plot of a piezoelectric load (model MPI-20 kHz-3kW 502/932R Branson Converter) measured with a Hewlett Packard 4192A LF impedance analyser. The red line represents an admittance plot of the unloaded transducer and the blue line represents an admittance plot of a loaded transducer.

Figure 2.7 represents the admittance plot of an ideal transducer plotted as a vector on the susceptance-conduction plain and the frequency increases clockwise along the circle. The dotted line represents the "clamped" characteristics of the transducer (Stansfield, 1990, p. 78). The clamped conductance, G_C, is small compared to the conductance of the motional arm, G_{MAX}.

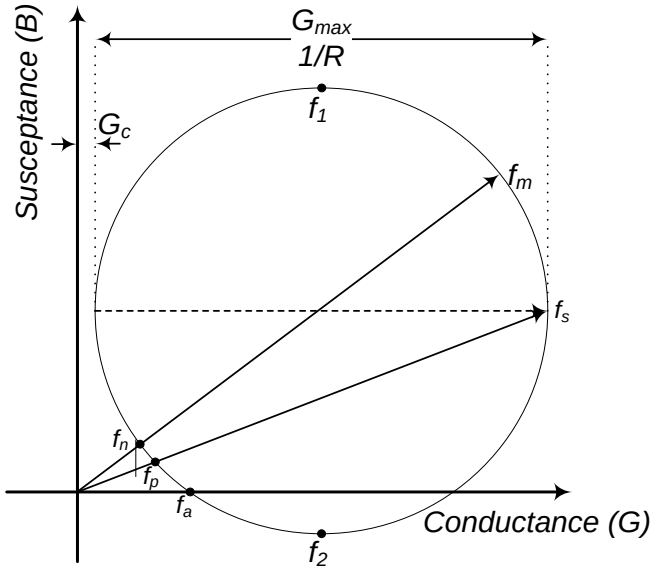

Figure 2.7: Admittance vector diagram. (Stansfield, 1990, p. 78)

The frequencies of interest to determine the circuit parameters are: f_s is the series resonance frequency of the motional arm where the conductance is a maximum, f_m is the frequency of maximum admittance, f_p is the parallel resonance frequency, f_n is the frequency where the admittance is a minimum and f_1 and f_2 are the points where the conductance is half the value of G_{MAX}.

2.3.3.2 The mechanical Q-factor

The series resonance frequency of the motional arm occurs when the conductance is at a maximum and therefore the motional power is a maximum for a constant voltage. Frequencies f_1 and f_2 are the point where the conductance is half the value of G_{MAX}. The mechanical Q-factor can be defined as:

$$Q_m = \frac{f_s}{f_2 - f_1} \tag{2.6}$$

The value of f_1 is always smaller than f_2.

The mechanical Q-factor can also be estimated with the absolute admittance curve:

$$Q_m \approx \frac{\omega_m}{2(\omega_n - \omega_m)} \cdot \left(\frac{\left|Y_{f_m}\right|}{\left|Y_{f_n}\right|} \right) \tag{2.7}$$

where ω_m is the angular frequency of maximum admittance, ω_n is the angular frequency where the admittance is a minimum, Y_{f_m} is the admittance at the frequency f_m and Y_{f_n} is the admittance at the frequency of f_n.

2.3.3.3 The electromechanical coupling coefficient

The electromechanical coupling coefficient plays an important role together with Q_m to control the size of the admittance vector diagram. The electromechanical coupling coefficient can be determined by the following equation:

$$k_{eff} = \sqrt{1 - \frac{f_s^2}{f_p^2}} \approx \sqrt{1 - \frac{f_m^2}{f_n^2}} \tag{2.8}$$

2.3.3.4 BVD modelling parameters

The BVD model contains four basic parameters to describe a piezoelectric load. These parameters are C_O, C_1, L_1 and R_1. These parameters are defined by the following equations:

$$R_1 = \frac{1}{\left|Y_{f_m} - Y_{f_n}\right|} \tag{2.9}$$

$$L_1 = \frac{Q_m \cdot R_1}{\omega_s} \tag{2.10}$$

$$C_1 = \frac{1}{\omega_s \cdot Q_m \cdot R_1} \tag{2.11}$$

The clamped static capacitance of the piezoceramics can be measured by using a capacitance bridge or a Q-Meter. The clamped static capacitance can also be determined by the following equation:

$$C_O = C_1 \left(\frac{1}{k_{eff}^2} - 1 \right) \tag{2.12}$$

2.3.3.5 Developing the model

The application of the BVD model to the admittance vs. frequency plot (Figure 2.6), obtained from the unloaded and loaded piezoelectric load, results in models with electrical components as tabled in Table 2-1. Figure 2.8 and Figure 2.9 represents a comparison of the response of the loaded and unloaded piezoelectric load to that of the model. The dotted line represents the original admittance plot of the load and the solid line represents the admittance plot of the model. These two figures show that the admittance plots of the models correlate closely to that of the measured plots of the real transducer.

Table 2-1: Electrical component values for the developed Butterworth-van Dyke model

	Unloaded	**Loaded**
Description	**Value**	**Value**
Q_m	473.69	353.77
k_{eff}	0.3955	0.3888
R_1	5.9544Ω	8.1607Ω
L_1	20.447mH	20.829mH
C_1	2.5703nF	2.4990nF
C_o	14.110nF	14.031nF

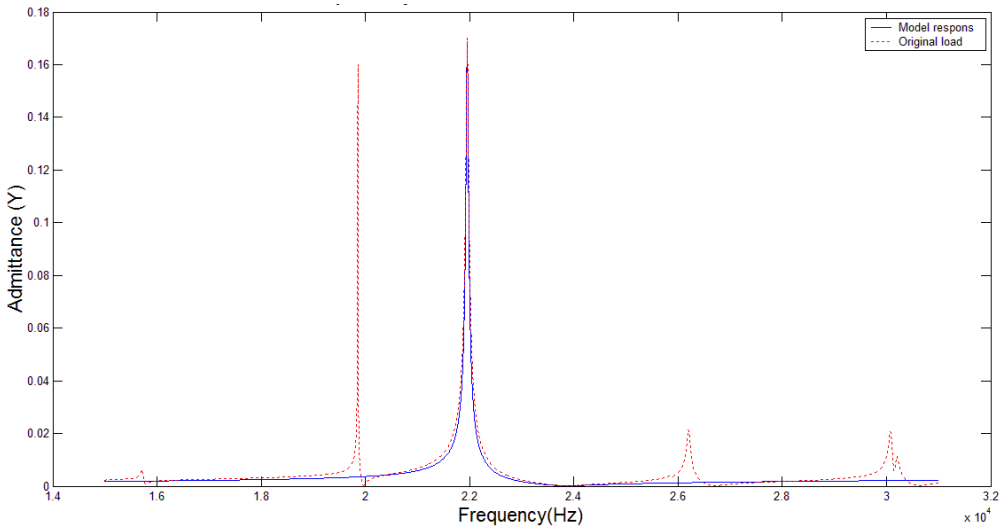

Figure 2.8: A comparison of the measured admittance plot of the unloaded piezoelectric transducer and the developed BVD model of the unloaded transducer.

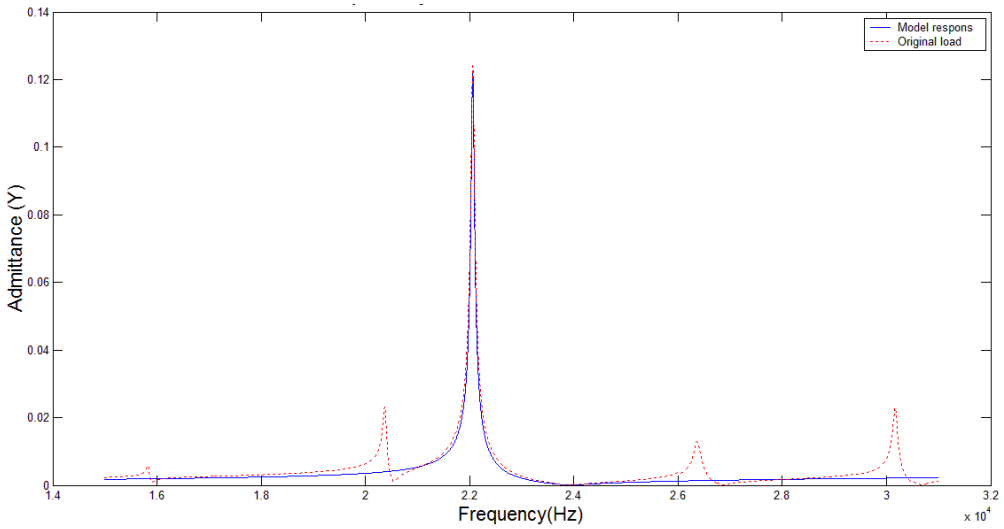

Figure 2.9: A comparison of the measured admittance plot of the loaded piezoelectric transducer and the developed BVD model of the loaded transducer.

Figure 2.10 and Figure 2.11 represents the admittance vector diagram of the unloaded and loaded piezoelectric load. The solid line represents the BVD model of the transducer and the dotted line represents the admittance vector plot of the original transducer. The large circle represents the thickness resonant mode and the smaller circles represent the radial resonant mode.

It is important to remember that the model only caters for a single resonance, as this is the only part of interest. The model holds true for the required application.

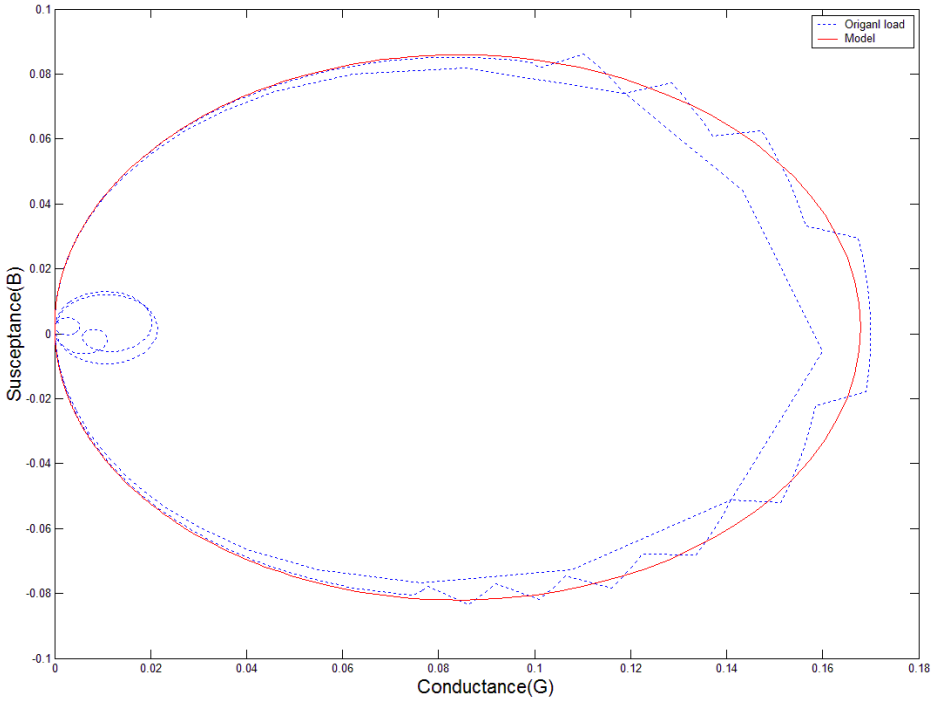

Figure 2.10: Susceptance vs. Conductance of the measured unloaded transducer and the devoloped model.

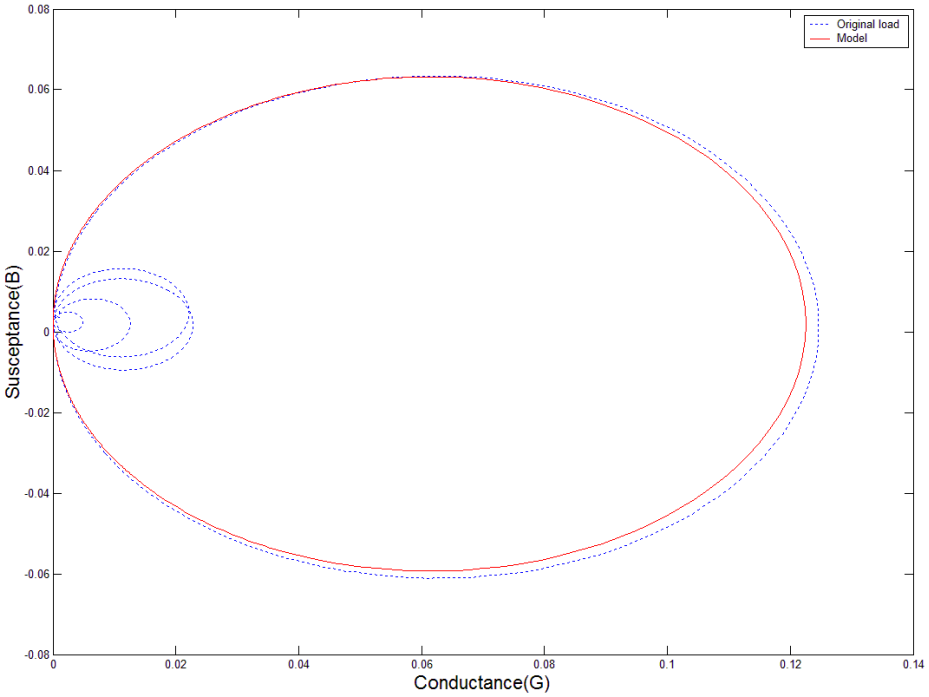

Figure 2.11: Susceptance vs. Conductance of the measured loaded transducer and the developed model.

2.4 Summary

Literature research was done on piezoelectric material and piezoelectric transducers in order to understand the different aspects to consider when driving a piezoelectric transducer. The literature was used to develop a theoretical model of the piezoelectric transducer which is needed for simulation purposes. The developed BVD models of the piezoelectric transducer was also validated and found to correlate with the measurements obtained from the piezoelectric transducer (model MPI-20kHz-3kW 502/932R Branson Converter).

High power piezoelectric transducers would need a power source that requires a high supply voltage. Switching devices for this application have disadvantages that can be resolved by using multilevel inverters, which is looked at in the next section.

CHAPTER THREE

MULTILEVEL INVERTER TOPOLOGIES

The multilevel inverter topologies were identified as a good option as a source to drive a piezoelectric transducer. This group of inverter topologies stacks its switching devices in series in order to achieve a high blocking voltage, and at the same time uses switching devices that have fast switching abilities, low conduction losses and a lower cost per switching device. The multicell inverter topology has an added advantage that the first harmonic is situated in the region of the apparent frequency. As the first harmonic is situated far away from any of the resonant modes of the piezoelectric transducer, it should be possible to drive the piezoelectric transducer without any filtering of the output signal and without exciting the transducer incorrectly. (Molepo, 2003, p. 17)

3.1 The plain series connected pseudo multilevel topology

The plain series connected pseudo multilevel topology (Figure 3.1) is the simplest form of solving the problem of an input voltage that is higher than the blocking-voltage of a single switch. This topology is described as a pseudo multilevel topology because the output voltage is only switched between two levels. The dc-bus voltage is shared between the devices. It is important to use switching devices from the same manufacturer, rating and batch number to prevent device mismatch. An extra protection precaution to be taken is to implement a snubber circuit connected across each switching device. The snubber circuit will clamp the voltage and the dv/dt across the device. The advantages of this topology are that it is not complex to implement and the control is simple compared to the other multilevel topologies. The disadvantage of this topology is the high dv/dt as the full dc-bus voltage is switched every time. (Wilkinson, 2004, p. 2)

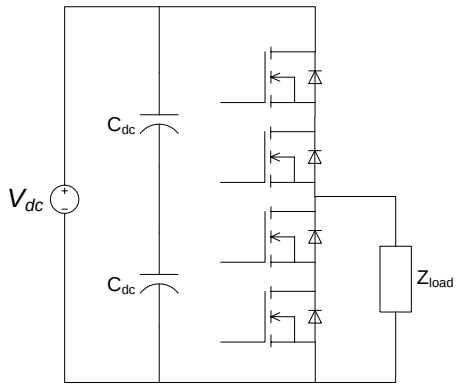

Figure 3.1: The plain series connected pseudo multilevel topology. (Wilkinson, 2004, p. 2)

3.2 The neutral-point-clamped multilevel topology.

This topology is also known as the diode-clamped multilevel topology (Figure 3.2). The switches in this topology share the same capacitor bus voltage. The capacitors in the capacitor bus form a voltage divider circuit so that the switches can be clamped at different voltages through the diodes. (Wilkinson, 2004, p. 3)

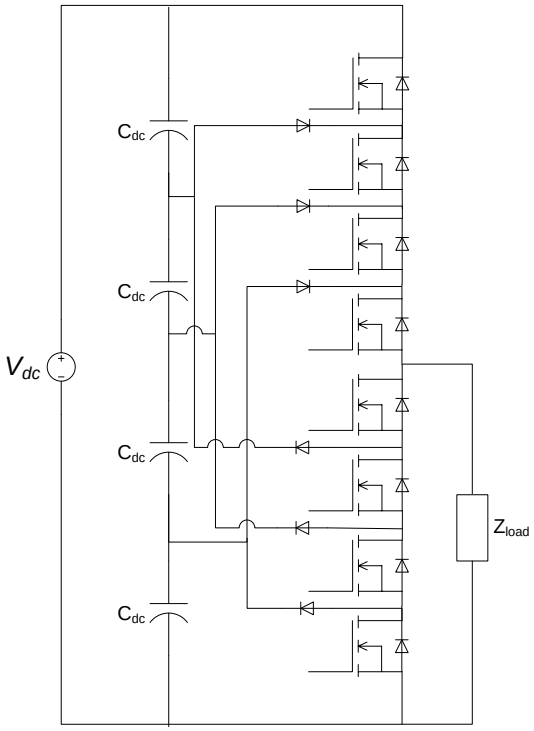

Figure 3.2: The neutral-point-clamped multilevel topology. (Wilkinson, 2004, p. 3)

3.3 The series-stacked multilevel topology.

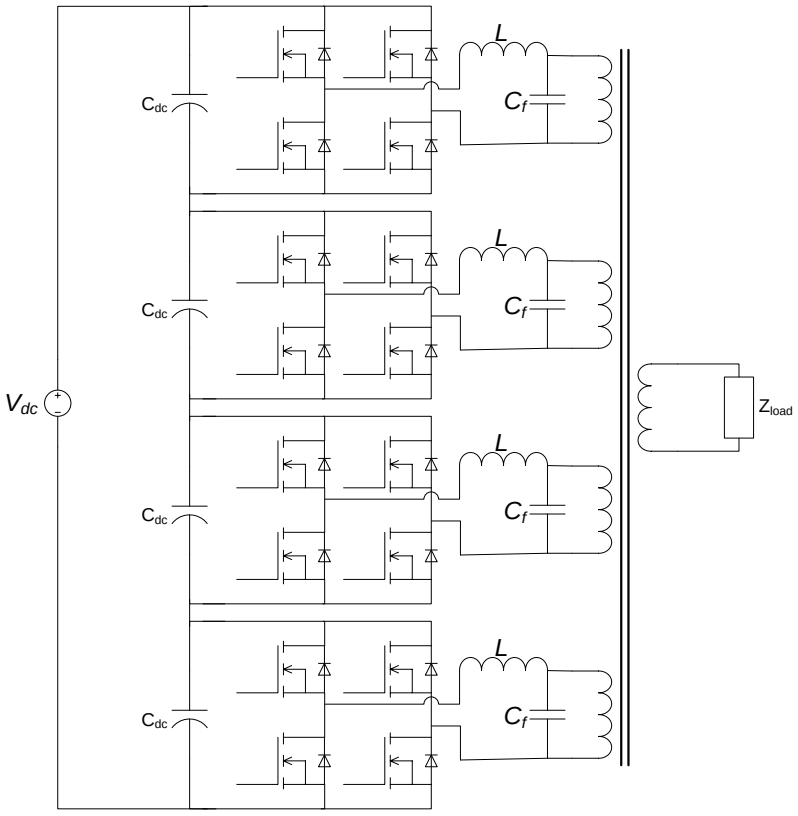

Figure 3.3: The series-stacked multilevel topology. (Wilkinson, 2004, p. 4)

This topology is formed by the connection of a number of dc-bus capacitors of individual full-bridge converters in series (Figure 3.3). Every full-bridge converter has its own output filter and is connected to its own matched primary winding of the output transformer. The transformer consists of the same number of primary windings corresponding to the number of connected full-bridge converters. The secondary side of the transformer usually consists of one winding. The advantage of this topology is that it has good steady-state balancing characteristics. The negative aspect of this topology is that it requires a specially designed transformer. (Wilkinson, 2004, p. 4)

3.4 The cascaded multilevel topology.

This topology is constructed by connection of the outputs of a number of full bridge converters in series with each other. Figure 3.4 shows the cascaded multilevel topology where every full-bridge converter has its own dc-supply. (Wilkinson, 2004, p. 5) This type of converter can generate near sinusoidal waveform voltage and currents, with a single switching per fundamental cycle, and will have a fast dynamic response. The disadvantage of this topology is that it requires a complex control to generate all the required control signals. (Wilkinson, 1997, p. 15)

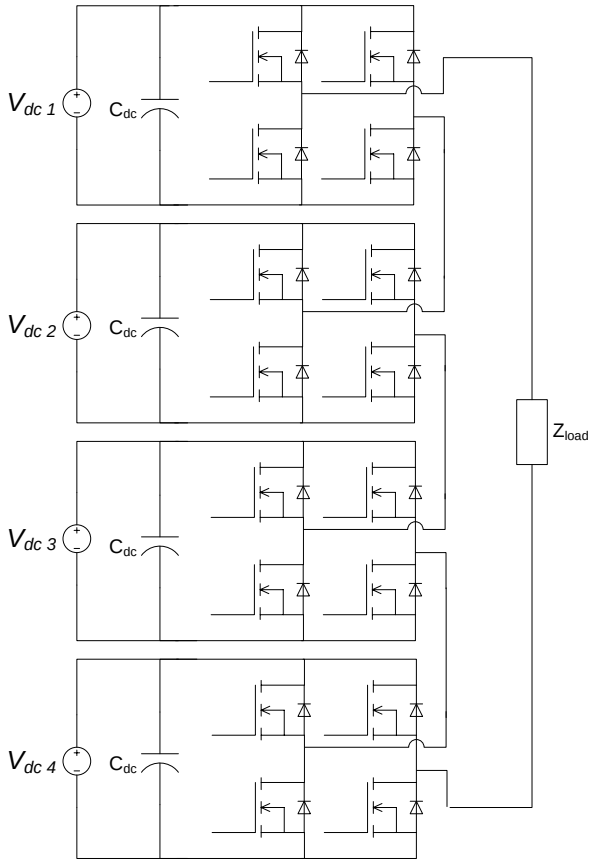

Figure 3.4: The cascaded multilevel topology. (Wilkinson, 2004, p. 5)

3.5 The multicell topology.

Each of the above-mentioned multilevel topologies has its own advantages and disadvantages. The multicell topology has an added advantage: The control signals applied to the switching devices can be phase-shifted to increase the apparent switching frequency (Meynard, 1997, p. 356). The apparent frequency is the product of the number of cells, contained in a multicell inverter, and switching frequency. This will result in less distortion being produced due to a reduction of the overlapping of the side-band harmonics. The high apparent switching frequency will also reduce the need for a large output filter (Wilkinson, et al., 1999, p. 1).

Sinusoidal pulse width modulation (SPWM) is used for the gate signals of the switching devices of the multicell inverter and is illustrated in Figure 3.5. This is a process where an applied reference signal, in the form of a sinusoidal wave, is compared with the carrier signal in the form of a triangle wave. When the applied reference signal has a voltage magnitude larger than the carrier signal, the output signal of the comparator will be just below the positive power supply voltage of the comparator. When the applied reference signal has a voltage magnitude smaller than the carrier signal, the output signal of the comparator will be just above the negative power supply voltage of the comparator. This process will result in a square wave of which the pulse width will vary according to the applied reference signal and the carrier signal. (Mohan, et al., 2003, p. 163)

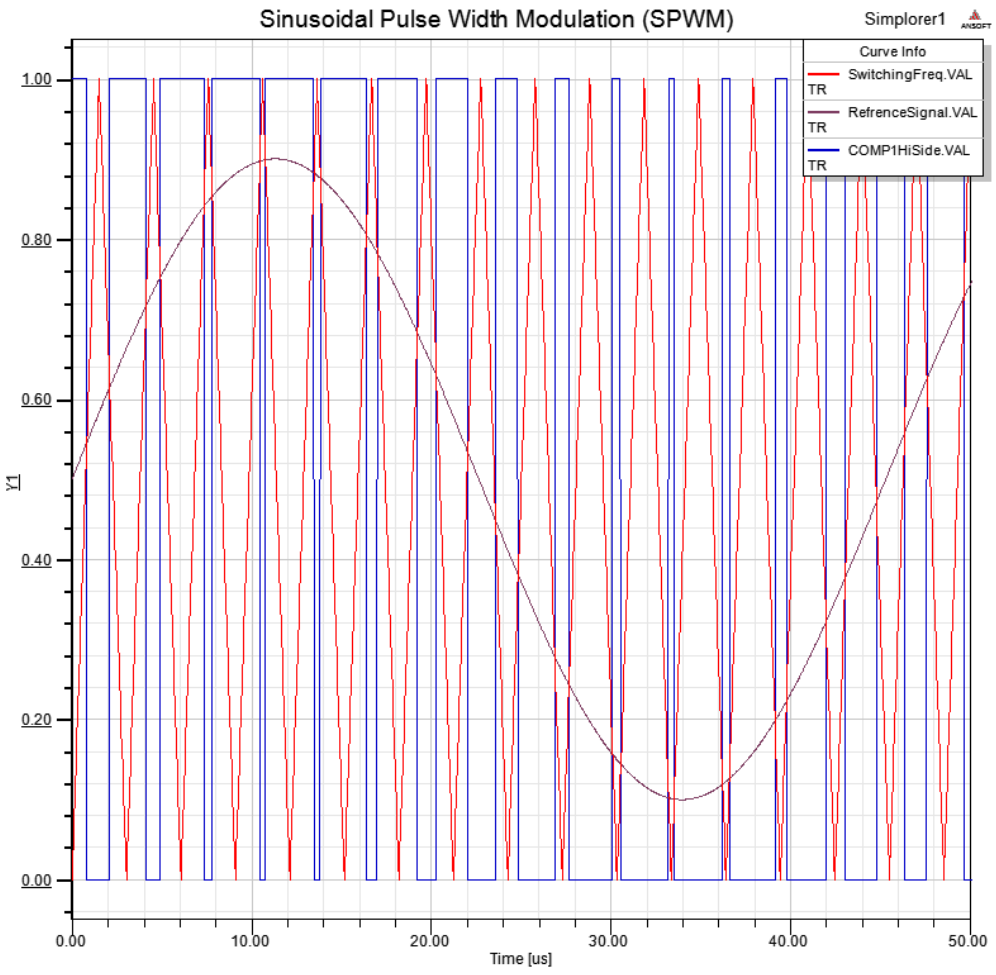

Figure 3.5: Sinusoidal Pulse Width Modulation (SPWM). (Wilkinson, 2004, p. 31)

The control signal for each cell is phase shifted according to the following equation:

$$\text{Phase-shift} = \frac{2 \cdot \pi}{p} \tag{3.1}$$

where *p* is the number of cells. When the control signal is phase-shifted, as illustrated in Figure 3.6, to the respective cells, it is known as interleaved pulse width modulation. When the phase-shift meets the requirements of equation 3.1, the apparent switching frequency will be equal to the product of the number of cells and the switching frequency.

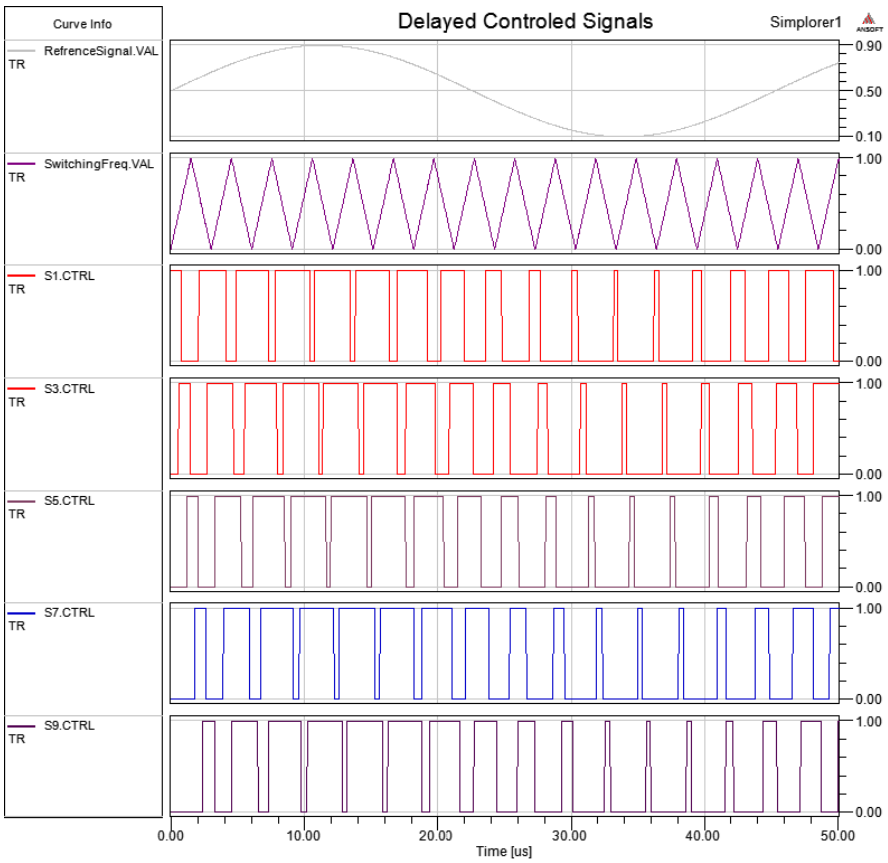

Figure 3.6: The simulated gate signals for the top switches of a five cell multicell inverter which is phase shifted according to equation 3.1. (Wilkinson, 1997, p. 21)

The switches of the multicell inverter shown in Figure 3.7 are arranged in pairs, called commutation cells, and must be in a complementary state with each other (Molepo, 2003, p. 16). A floating capacitor is placed between two commutation cells. Multicell inverters are composed of p-commutative cells connected with a set of p-1 floating capacitors (Molepo, 2003, p. 20).

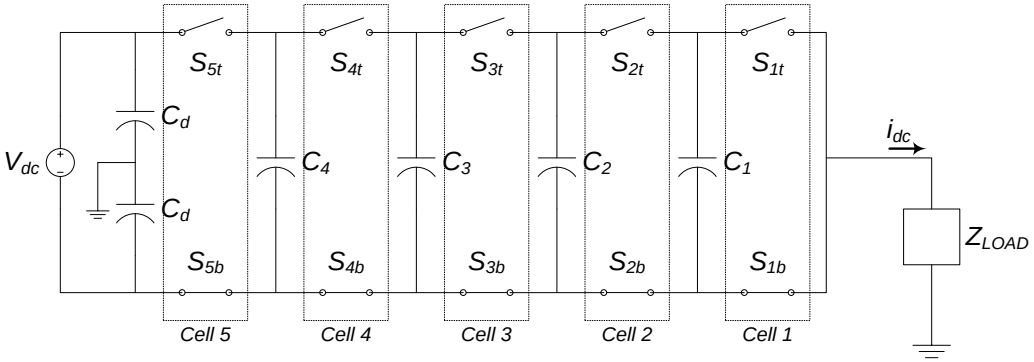

Figure 3.7: A basic representation of a five-cell multicell inverter. (Wilkinson, 1997, p. 18)

The voltage across each capacitor is defined by the following equation:

$$V_{C_k} = \frac{k \cdot V_{dc}}{p} \tag{3.2}$$

where $k = p\text{-}1$.

The value of the floating capacitor can be calculated by use of the following formula:

$$C_k > \frac{\phi \cdot I_{dc}}{2 \cdot \pi \cdot f_{sw} \cdot \Delta V_{C_k \max}} \tag{3.3}$$

where C_k is the cell capacitance, f_{sw} the switching frequency, Φ the phase-shift between the control signals, I_{dc} the output dc current and ΔV_{Ck} the capacitor ripple voltage (Wilkinson, 1997, p. 28). The voltage across each switching device is limited to $\frac{V_{dc}}{p}$ (Wilkinson, 2004, p. 6). The number of cells can be increased depending on the blocking voltage required and the blocking voltage of the device used (Wilkinson, et al., 2003, p. 1307).

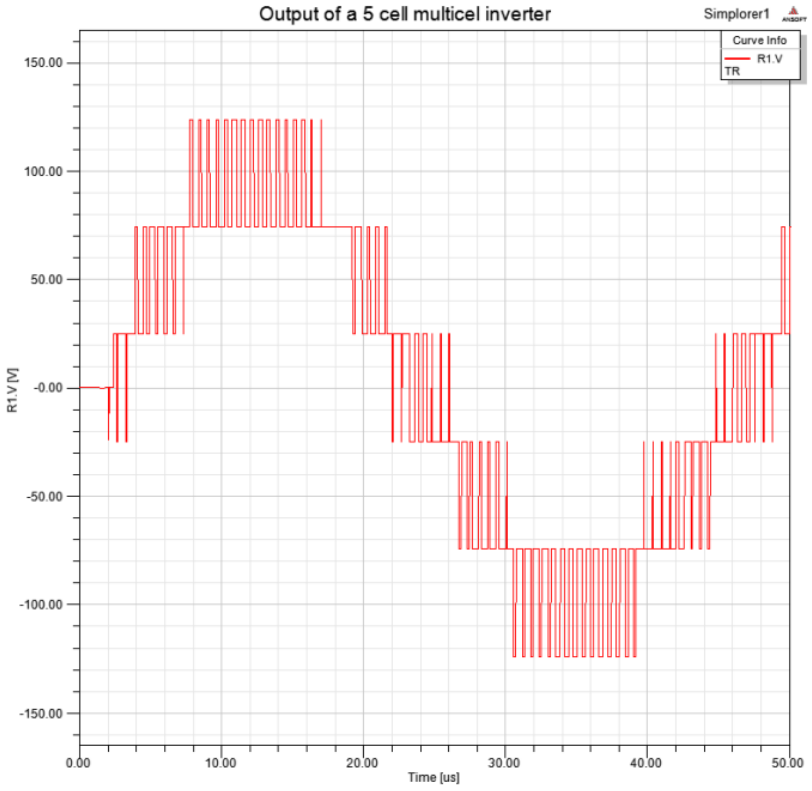

Figure 3.8: The output of a five-cell multicell inverter which was simulated with Simplorer. (Meynard & Foch, 1992, p. 402)

Figure 3.8 represents the output voltage of a five-cell multilevel inverter consisting of six levels. Each level consists of the sinusoidal pulse width modulation produced by each cell. The level steps are the same as the voltage across each switch.

3.5.1 Harmonic analysis

If the gate signal driving the multicell inverter in Figure 3.7 is not phase shifted, the resultant output voltage would look similar to that shown in Figure 3.5. The first harmonic at 22 kHz, representing the reference frequency which was applied to the multicell inverter, matches the frequency of the radial resonance mode of the piezoelectric load. The next group of harmonics is seen around 330 kHz, representing the switching frequency and is surrounded by deteriorating harmonics spaced 22 kHz apart. This occurrence is seen at multiples of the switching frequency.

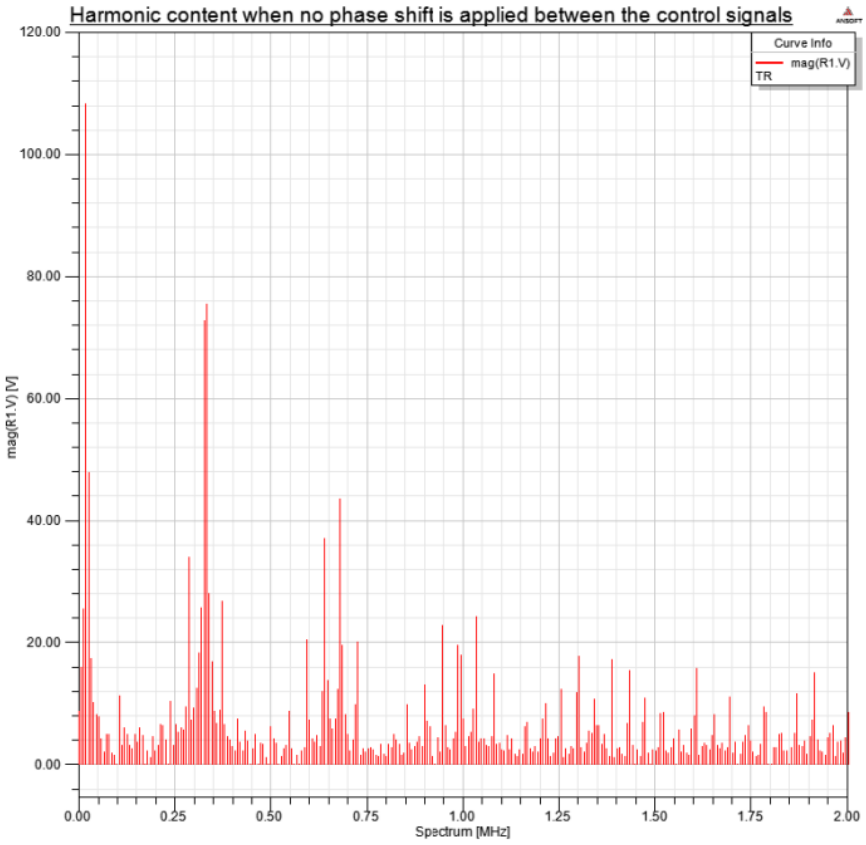

Figure 3.9: The simulated results of the harmonic content of a multicell inverter when there is no phase shift between the gate signals. (Meynard & Foch, 1992, p. 398)

Multicell inverters have the added advantage of a switching frequency multiplication property. This will only occur when the applied gate signals are phase shifted as described in Figure 3.6. This is called the apparent switching frequency and it will cause the next multiple of the switching frequency, for a five cell multicell inverter, to be at 1.650 MHz and not at 330 kHz, which will reduce the overlapping of side-band harmonics. This reduction in overlapping harmonics will help to assure that the piezoelectric load is excited in the right way and that it will reduce the occurrence of spurious modes. (Meynard & Foch, 1992, p. 401)

Figure 3.10 shows the harmonic content of the output of a multicell inverter. One can observe that the first harmonic is situated around 1.65 MHz and the magnitude of the first harmonic is considerably smaller than the fundamental harmonic of the reference signal.

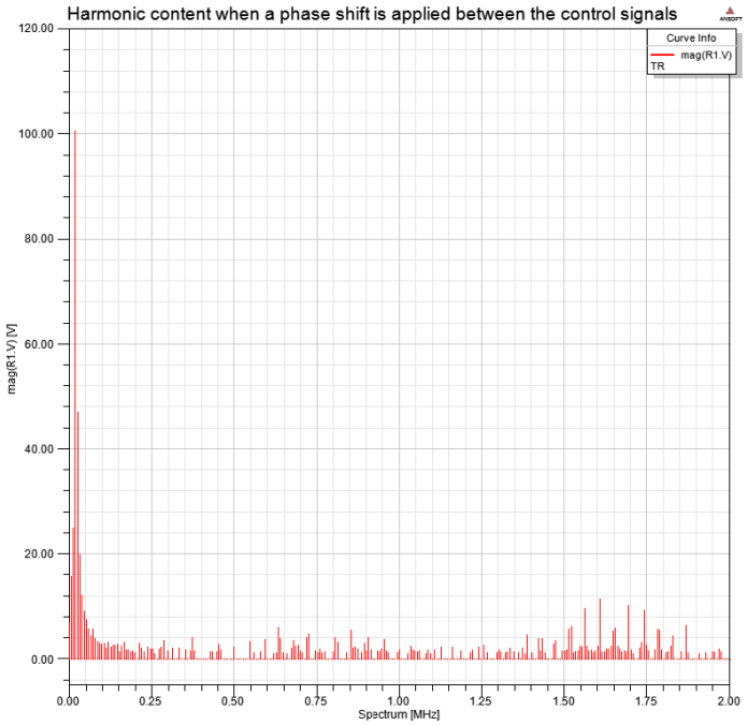

Figure 3.10: The simulated results of the harmonic content of a multicell inverter when there is a phase shift between the gate signals. (Meynard & Foch, 1992, p. 401)

3.5.2 Cell balancing

Natural balancing of the cells implies that the voltage across the floating capacitors will conform to equation 3.2. Before power is applied to the multicell inverter, the voltages across the cell capacitors will be 0V. If a $100V_{DC}$ power source and the correct gate signals are applied to the multicell inverter, the cell capacitors will start to charge to their natural voltage level. When the source is applied to a five cell multicell inverter with four cell capacitors, the cell capacitor closest to the power source will charge up to $80V_{DC}$, the second cell capacitor up to $60V_{DC}$, the third up to $40V_{DC}$ and the last cell capacitor will charge up to $20V_{DC}$. The dynamic response of the system is influenced by the size of the cell capacitors, and the speed at which cell balancing takes place also depends on the cell capacitors' size (Wilkinson, 1997, p. 34).

Natural balancing will only occur (Wilkinson, 2004, p. 86):

- When the switching frequency is sufficiently higher than the reference frequency.
- When the reference signal does not contain high frequency components.
- When sinusoidal modulation is used.
- Where fixed duty-cycle PWM is used.

3.5.3 Cell balancing with a “Balancing Booster” circuit

The “balance booster” circuit improves the time the cell capacitors of the multicell inverter take to achieve the voltage level determined by Equation 3.2. The circuit consists of a series connected $R_{booster}$, $L_{booster}$ and $C_{booster}$, and is connected between the multicell inverter and the load.

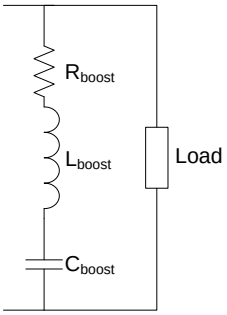

Figure 3.11: "Balance Booster” circuit with a load in parallel. (Wilkinson, 1997, p. 30)

The voltage unbalance of the multicell inverter is caused by current harmonics at the switching frequency of the cells. This series connected circuit is therefore tuned to the switching frequency of the multicell inverter in order to filter out these harmonics and achieve voltage balancing. (Wilkinson, 1997, p. 30)

3.5.4 Bootstrap power supply

A five-cell multicell inverter requires ten switching devices. Each switching device requires its own isolated power supply in order to supply power to the driving circuitry, to control the power device. With the implementation of bootstrap power supplies, only two power supplies are required instead of ten. A bootstrap power supply introduces a problem in that the voltage loss over every section of the power supply results in the last cell’s driving circuitry not having sufficient voltage to function properly. The problem was solved through the primary power supply (*E1*) voltage being increased and a voltage regulator being introduced to each cell (Molepo, 2003, p. 120).

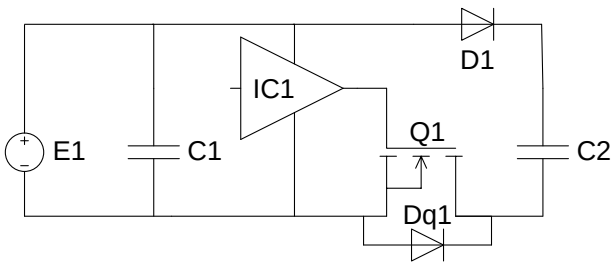

Figure 3.12: Section of a bootstrap power supply. (Molepo, 2003, p. 43)

According to the circuit in Figure 3.12, *E1* will charge *C1*. It must also be remembered that the bootstrap diodes must be able to handle twice the cell voltage and must be fast recovery diodes (Molepo, 2003, p. 43). This supplies the required energy to power *IC1* in order to control *Q1*. When

Q1 is switched on and connects the negative side of *C2* to the negative side of *C1*, *D1* becomes forward biased causing *C2* to charge. This is how the energy propagates from one cell to the next.

3.6 Summary

Five different types of multilevel inverter topologies were investigated to determine which one could be used to drive a piezoelectric transducer. The multicell inverter topology was used as it has an added advantage of apparent switching frequency. When a half-bridge inverter is used, there is a predominant harmonic at the switching frequency. A multicell inverter does not have a predominant harmonic at the switching frequency but has a predominant harmonic at the product of the number of cells and the switching frequency (apparent frequency). The operation of the multicell inverter was discussed. The balance circuit was also researched as this circuit helps the multicell inverter to achieve balance condition quicker. Bootstrap power supply was also researched as this type of power supply reduces the amount of isolated power supplies required.

We next consider compensation networks which are required to match the inverter to the non-linear load.

CHAPTER FOUR

Compensation Networks

For a piezoelectric load to be driven optimally, it must be driven at its mechanical resonance. At this frequency the piezoelectric load will reduce to the static capacitance, C_O, and the resistor of the motional arm, which are in parallel with each other. The static capacitance of the piezoelectric transducer can be eliminated by the introduction of compensation networks. To have the maximum transfer of energy, the source must have the same impedance as the load. Ultrasonic amplifiers constructed utilizing a half-bridge topology and with no output filters or compensation networks, normally have resistive output impedances (Bruyn, 2003, p. 45). Therefore the applied piezoelectric transducer must be resistive. This will ensure the energy applied to the piezoelectric transducer to be real power and will cause the energy to be transferred to the load of the piezoelectric transducer.

The parameters of piezoelectric transducers are known to change under high power conditions and these changes occur in the Q-factor, the impedance and the resonant frequency (Green, 2002, p. 110). This phenomenon makes it difficult to design matching circuits and filters for the purpose of driving nonlinear piezoelectric loads. It must be remembered that the piezoelectric load needs to be driven at the resonant frequency of the mechanical system in order to achieve the maximum power output (Kauczor & Fröhleke, 2004, p. 2739).

The output signal of an inverter contains unwanted harmonics due to the nature of switch-mode topologies. These harmonics need to be reduced as they might be situated close to other resonant modes of the piezoelectric transducer. Traditionally a low-pass filter will be used to filter out these unwanted harmonics and help to reduce distortion of the output signal. (Wilkinson, 1997, p. 4) These methods for designing filters do not work effectively in this situation as the impedance of the piezoelectric transducer changes with a change in load. This will cause a mismatch of impedances between the load and the source and will result in inefficient transfer of power to the load. Maximum power transfer will not occur and the efficiency of the total system will be poor (Horowitz, 2005, p. 5).

The multicell inverter, with its added advantage of apparent frequency, helps to reduce the harmonic content of the output signal as the first harmonic will be at the apparent frequency. This apparent frequency is much higher than the required output frequency. As different compensating systems are introduced, to characterize the transducer with a resistive impedance, a filter is not required as the compensating systems also function as a filter. (Boylestad, 1994, p. 1079)

There are numerous methods of impedance matching of which π- and T-matching networks are well known. These networks have high insertion losses and cannot be used in this application. An additional method of impedance matching is by implementation of a transformer.

4.1 Impedance matching with a transformer

Through the introduction of a transformer into a circuit, it is possible to reduce or increase the impedance of the load to the same value as the source. (Boylestad, 1994, p. 944)

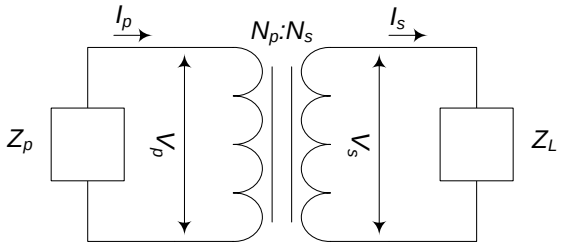

Figure 4.1: Transformer for impedance matching purpose. (Boylestad, 1994, p. 943)

The relationship between the circuit parameters (Figure 4.1) can be defined by this equation (Boylestad, 1994, p. 940):

$$\frac{V_p}{V_s} = \frac{N_p}{N_s} = \frac{I_s}{I_p} = a \qquad (4.1)$$

where V_p and V_s are the primary and secondary voltages respectively, N_p and N_s are the primary and secondary turns ratio respectively, I_p and I_s are the primary and secondary current respectively and a is the transformation ratio.

The impedance seen from the primary side of the transformer can be defined by this equation (Boylestad, 1994, p. 942):

$$Z_p = a^{2} \cdot Z_L \qquad (4.2)$$

As the load impedance and source impedance are known, this formula can be used to determine the transformer ratio and turns ratio respectively.

4.2 Transducer Compensation with a series tuning inductor

This method uses a series tuning inductor to “cancel” the reactance of the transducer, and a transformer can be used to match the magnitude of the impedances of the transducer and the source (Van Randeraat, J , 1968, p. 101). One disadvantage of this type of transducer compensation technique is that under certain conditions the series inductor can cause a high voltage across the transducer (Bruyn, 2003, p. 46).

In figure 4.2(a), L_s is the series inductor. In figure 4.2(b) the equivalent circuit for a piezoelectric transducer is converted into a parallel resonant circuit so that the series-tuned circuit, which includes $L_{s,}$ can be seen. As the impedance of a parallel resonant circuit is at a maximum at resonance, the admittance will be at the minimum. This point corresponds to the anti-resonant frequency, f_a, of a piezoelectric transducer. Therefore the series resonant circuit is tuned to f_a. (Van Randeraat, J , 1968, p. 101)

.

The following formula can be used to calculate the value of the series inductor:

$$L_s = \frac{1}{(2 \cdot \pi \cdot f_a)^2 \cdot C_o} \tag{4.3}$$

where f_a is the anti-resonance frequency.

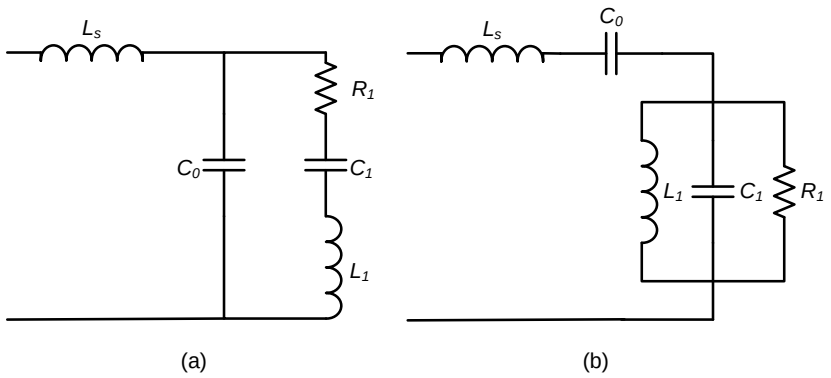

Figure 4.2: (a) The equivalent circuit for a piezoelectric transducer with compensation as a series inductor and (b) an alternative way of drawing the equivalent circuit for a piezoelectric transducer so that the series-tuned circuit can be seen. (Van Randeraat, J , 1968, p. 101)

4.3 Transducer Compensation with a parallel inductor

This method uses a tuning inductor connected in parallel with the transducer in order to "cancel" the blocked capacitance of the dielectric, C_O. A transformer can be used to modify the impedance of the load in order to match the impedance to the source (Van Randeraat, J , 1968, p. 101).

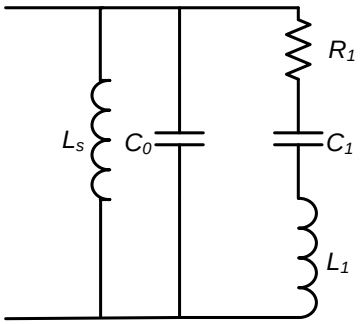

Figure 4.3: Transducer compensation with a parallel inductor (Van Randeraat, J , 1968, p. 101)

The value of the inductor is calculated so that the resonant frequency of the parallel resonant circuit, L_s and C_o, is the same as the resonant frequency, f_r, of the motional arm. The following formula can be used to calculate the value of the parallel inductor (Van Randeraat, J , 1968, p. 101):

$$L_p = \frac{1}{(2 \cdot \pi \cdot f_r)^2 \cdot C_o} \tag{4.4}$$

4.4 Q-Matching

At mechanical resonance the motional arm of the model of the piezoelectric transducer (Figure 4.4 (a)) reduces to only R_1 and C_O (Figure 4.4 (b)). Q-matching uses an additional capacitor, C_p, connected in parallel to the transducer in order to increase the electrical storage factor of the transducer. This capacitor reduces the impedance of the transducer to an impedance equal to that of the source. The addition of C_p has an added advantage namely that it would absorb energy generated by the piezoelectric material used in the load. At resonance the reactance of the transducer is "cancelled" by the addition of a series-connected network comprised of an inductor, L_s, and capacitors, C_s (Bruyn, 2003, p. 31).

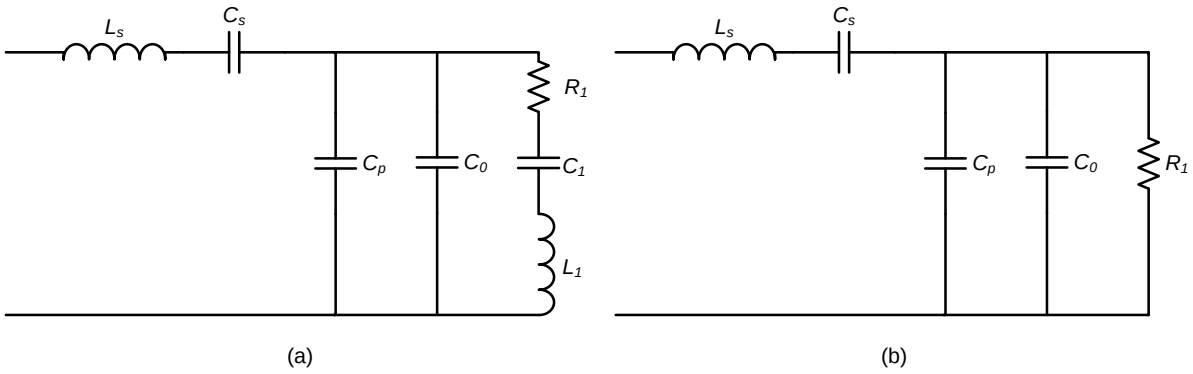

Figure 4.4:(a) Q-matching network connected to a model of a piezoelectric transducer and (b) Q-matching network connected to a model of a piezoelectric transducer at mechanical resonance. (Bruyn, 2003, p. 31)

The power to the load at the series resonant frequency is given by (De Vries, 1999, p. 16):

$$P = \frac{2V_S^2}{R_S \pi^2} \tag{4.5}$$

Rearranging for a certain power rating, the inverter will see an optimum resistance of:

$$R_S = \frac{2V_S^2}{P\pi^2} \tag{4.6}$$

The resistance, R_S, is determined by the power required, P, and the source voltage, V_S. When the resistance of the motional arm, R_1, is the same as the optimum resistance, R_S, maximum power transfer takes place and the power factor should be close to one. (Boylestad, 1994, p. 944)

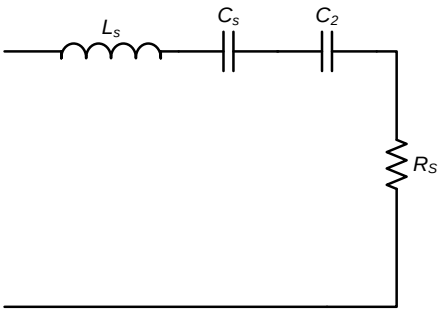

Figure 4.5: Series representation of the piezoelectric load at mechanical resonance and the Q-matching network.

To calculate the value of C_2, the sum of C_p and C_O, the series equivalent impedance of the network consisting of R_1, C_p and C_O must be determined (Figure 4.5). To determine the series equivalent impedance, the inverse of the admittance of the parallel network is used. The formula that defines the admittance is as follows:

$$\mathrm{Y} = \mathrm{G} + \mathrm{jB} \tag{4.7}$$

The admittance of the network is defined by the following equation:

$$Y = \frac{1}{R_P} + j\omega C_2 \tag{4.8}$$

where R_P represents the parallel resistor of the load which is equal to R_1.

The impedance of the series network can then be defined by:

$$Z = \frac{\frac{1}{R_p}}{\left(\frac{1}{R_p}\right)^2 + (\omega C_2)^2} - j\left[\frac{\omega C_2}{\left(\frac{1}{R_p}\right)^2 + (\omega C_2)^2}\right] \tag{4.9}$$

The value of the series resistor, R_S, will be the real part of equation 4.9:

$$R_S = \frac{\frac{1}{R_P}}{\left(\frac{1}{R_P}\right)^2 + (\omega C_2)^2} \tag{4.10}$$

When the subject of formula 4.10 is changed to C_2:

$$C_2 = \frac{1}{\omega}\sqrt{\frac{R_P - R_S}{R_P^2 R_S}} \tag{4.11}$$

the value of C_p can be determined by subtraction of the capacitance values of C_O from C_2. The imaginary part of equation 4.9 would represent the impedance of C_S.

$$C_S = \frac{1}{\omega\left(\frac{\omega C_S}{\left(\frac{1}{R_P}\right)^2 + (\omega C_2)^2}\right)} \tag{4.12}$$

By simplifying equation 4.12 the value of C_S can be determined by equation 4.13:

$$C_S = \frac{1}{\omega\sqrt{R_S R_P - R_S^2}} \tag{4.13}$$

At resonance the reactance of the inductor must be the same as the total capacitive reactance of the circuit. The capacitive reactance:

$$X_C = \frac{1}{\omega C_T} \tag{4.14}$$

can be obtained by calculation of the total capacitance:

$$\frac{1}{C_T} = \frac{1}{C_S} + \frac{1}{C_2} \tag{4.15}$$

The value of the inductor can be calculated by the following equation:

$$L_S = \frac{\sqrt{R_S}\left(2R_P + R_S\right)}{\omega\sqrt{R_P - R_S}} \tag{4.16}$$

The quality factor (Q factor) of the circuit can be calculated by the following equation:

$$Q = \frac{\sqrt{R_S}\left(2R_P - R_S\right)}{R_S\left(R_P - R_S\right)} \tag{4.17}$$

The full derivation of equation 4.11, 4.13, 4.16 and 4.17 can be found in Appendix D. The Q factor is determined by the values of R_S and R_P and cannot be specified. This type of compensation network would be applied directly between the output of an inverter and the load. This compensation network acts as a band-pass filter and one would require a high Q factor to reduce the harmonic content of the output of the inverter in order to achieve a pure sinusoidal output signal. The first harmonic of the output signal of the multicell inverter is very high and therefore a high Q factor is not required.

4.5 Summary

Different types of compensation networks available that can be used when a piezoelectric load is driven with a multicell inverter were researched. It was found that implementation of compensation networks with a series or parallel inductor requires an additional impedance matching transformer. This will increase the required magnetic components. Q-matching achieves the same functionality with only one inductor.

CHAPTER FIVE

System Overview and Design

This chapter contains an overview of the system and the design process that was used. The function for each block is outlined under the section, System Overview, and the design specifications and design process is discussed under the section, Design of System. The system is comprised of a multicell inverter, two auxiliary power supplies, a main power supply, a controller with an auxiliary power supply, three different types of compensation networks and two load options.

5.1 System overview

The Multicell inverter consists of five cells and each cell consists of two switches which form a half bridge. These five half bridge cells are stacked in a series fashion to form the Multicell inverter. The main power supply supplies a DC bus from which a virtual ground is created by introduction of two capacitors as depicted in Figure 5.1. This is done in order to produce a positive and negative supply rail which is required for the multicell inverter.

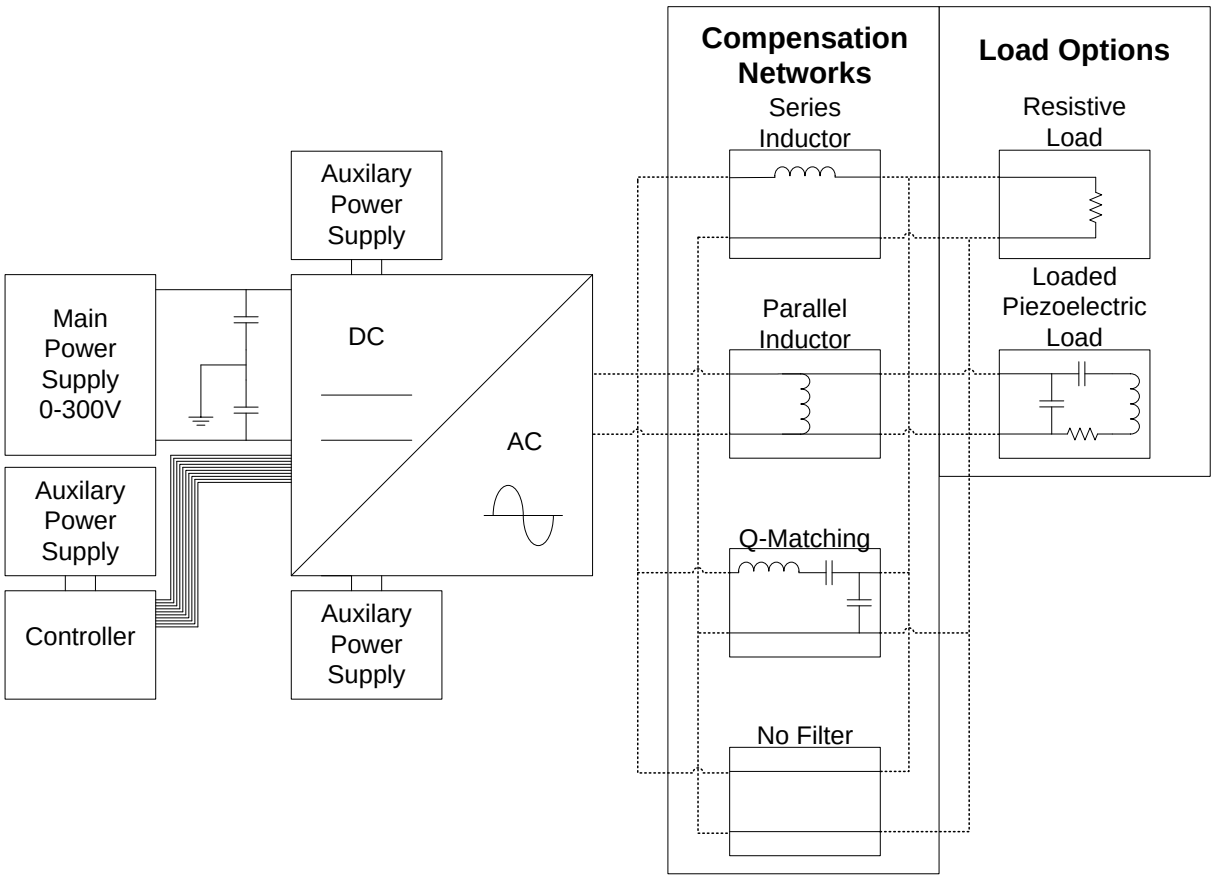

Figure 5.1: Block diagram of the system consisting of the multicell inverter, compensation options with impedance matching transformers where required, and load options

The two auxiliary supplies are used to produce energy to the bootstrap powers supplies, one for the high-side drivers and the other for the low-side drivers. A bootstrap power supply is required to supply power to five gate drivers which have different ground levels. The operation of this type of power supply is discussed in section 3.3.

The multicell inverter consists of five cells and each cell consists of two switches. These ten switches require ten gate signals which have different ground levels. The ten electrical gate signals from the controller are converted separately to light, and fibre optic cables are used to transmit the gate signal to an optic receiver. This receiver converts the control signal back to an electrical control signal which is then connected to the driver circuit of a switch.

The controller was designed by a Masters student, C.R.Jooste, at the Centre for Instrumentation Research (C.I.R.) of the Cape Peninsula University of Technology. The controller compares a 22.1kHz sinusoidal reference signal with a 300kHz triangular carrier signal. The result is inverted in order to provide a complementary state for the two switches within a cell. The incorporation of dead time ensures that the two switches within a cell are never on at the same time. The two signals are then phase shifted according to equation 3.1, which results in ten gate signals which are used for the ten switches. The control board is connected via fibre optic cables to ensure electrical isolation between the gate signals.

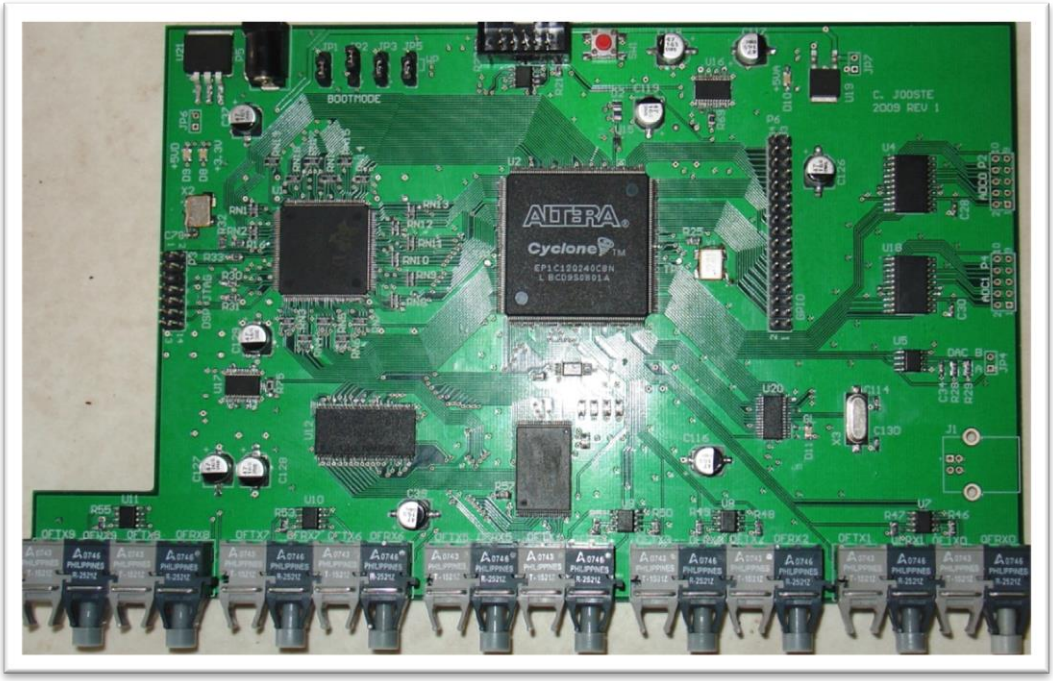

Figure 5.2: Photo of the control board

The three compensation networks need to be evaluated in order to determine which one transfers the most energy to the piezoelectric load. These networks consist of a series inductor, a parallel inductor, and a Q-matching compensation network. The common function of the compensation networks is to “cancel” the reactance of the clamped static capacitance of the piezoelectric transducer. This can be achieved in different ways. The first method is achieved by the introduction of an inductor in series with the transducer in order to form a series resonant circuit. The value of the inductor can be determined by equation 4.3. The second method introduces an inductor in parallel with the transducer. This will form a parallel resonant circuit that will “cancel” the capacitive reactance of the transducer. The value of the inductor can be determined by equation 4.4.

The third method introduces a capacitor in parallel to the transducer which will reduce the impedance of the transducer to that of the multicell inverter. A series resonant circuit is then added in series to the load to “cancel” the reactance of the capacitance of the piezoelectric load and the added capacitor. The last compensation option is included to show how the transducer is connected directly to the multicell inverter in order to test if the piezoelectric transducer can be excited by the multicell inverter without any compensation network.

The voltages across the cell capacitors of the multicell inverter will naturally balance, as discussed in Chapter 3. The research needs to determine if the multicell inverter will stay balanced when a non-linear load is connected to the multicell inverter and if it will stay in balance as the dynamics of the load changes. Therefore two different loads are connected to the multicell inverter. The first one is a resistive load to show that the cell voltages conform to the theory, and the second load is a piezoelectric transducer to show that the cell voltages still stay balanced.

5.2 Design of system

5.2.1 Multicell inverter

This section deals with the design process of the multicell inverter. This process will start with the selection of the switching device. The design process will also include the design of the gate drive circuit, flying capacitor, dc capacitors, bleeder resistors and heat sink. The specifications for the multicell inverter are summarised in Table 5-1: Multicell inverter specifications.

Table 5-1: Multicell inverter specifications

Parameter	**Symbol**	**Value**	**Unit**
Power rating	P	*800*	*W*
Input voltage	V_d	*100*	*V*
Output voltage (RMS)	V_o	*80*	*V*
Output current (RMS)	I_o	*10*	*A*
Output frequency	f_o	*22.164*	*kHz*
Switching frequency	f_{sw}	*300*	*kHz*

Figure 5.3 depicts a basic circuit diagram of a five cell multicell inverter with simplified bootstrap power supplies.

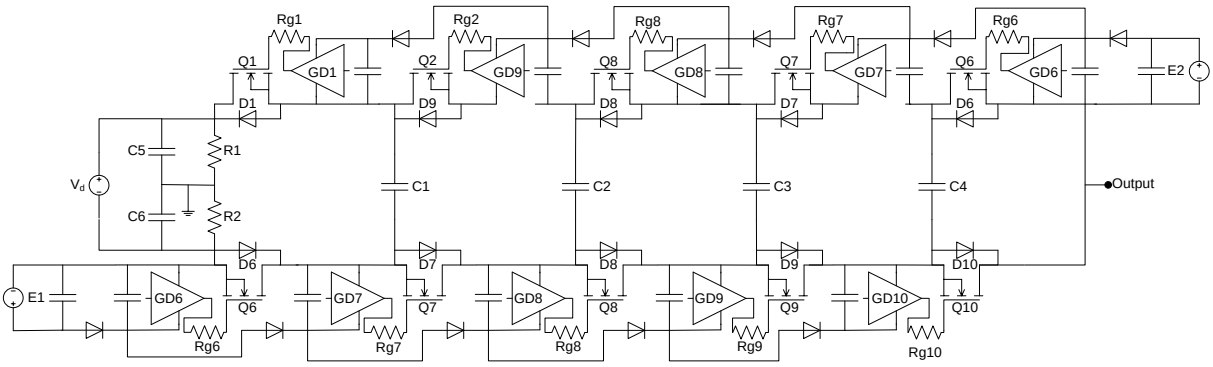

Figure 5.3: Circuit diagram of a basic five cell multicell inverter with a simplified bootstrap power supply.

5.2.1.1 MOSFET selection

Due to the high switching frequency it would be an advantage if the switching device had a low lead inductance and a small gate charge. The low lead inductance of the device will help to reduce any overshoots and the small gate charge will help to reduce the switching losses.

The DirectFET is a type of FET which is constructed by means of placing the substrate in a little can as depicted in Figure 5.4. The connection pads are directly connected to the substrate and therefore the lead inductances are reduced to a minimum.

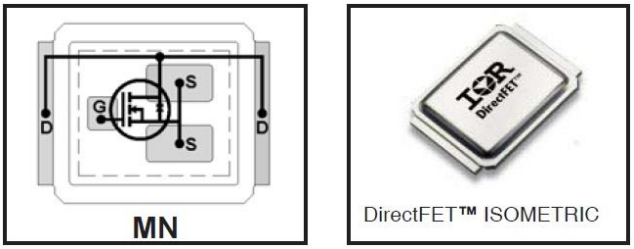

Figure 5.4: Example of a DirectFET (International Rectifier, 2012)

This device has a V_{DSS} of *100V*, a total gate charge of *35nC*, an $R_{DS(ON)}$ of *10.3mΩ*, a maximum pulsed drain current of *82A*, a footprint of an *SO-8* package and a profile of *0.7mm*.

5.2.1.2 Gate drives

The primary function of a gate drive circuit is to turn a switch on and off, according to a signal received from a controller, and the circuit requires its own isolated power supply to perform this task of amplifying the received controller signal. There are ten of these gate drive circuits required to drive the ten switches of the multicell inverter. Figure 5.5 is the circuit diagram of the gate drive circuit used, and the design process will be discussed to calculate the values of the different components.

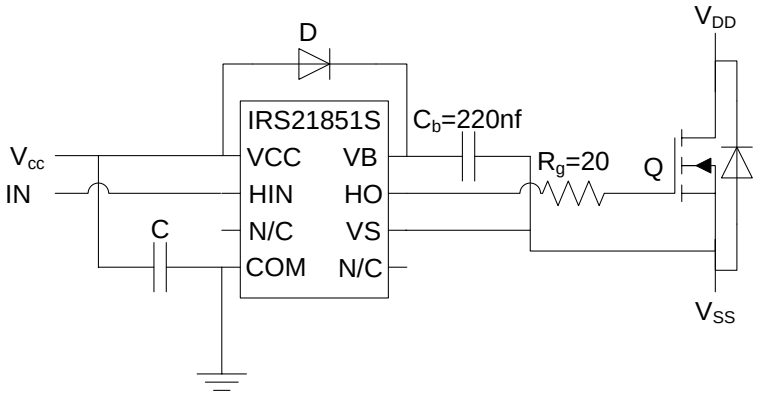

Figure 5.5: Circuit diagram of the gate drive circuit and a switch.

The IRS21851S single high-side driver IC was chosen because the output stage can sink and source *4A* with a propagation delay of *170ns.* A MOSFET is a voltage controlled device and is turned on by the application of a voltage between the gate and the source terminals. The function of R_g is to limit the charging rate of the gate capacitance in order to limit the slope *(dV/dt)* of the output voltage (Merello, A; Rugginenti, A; Grasso, A, 2012). This will help to reduce any overshoot voltage at the output.

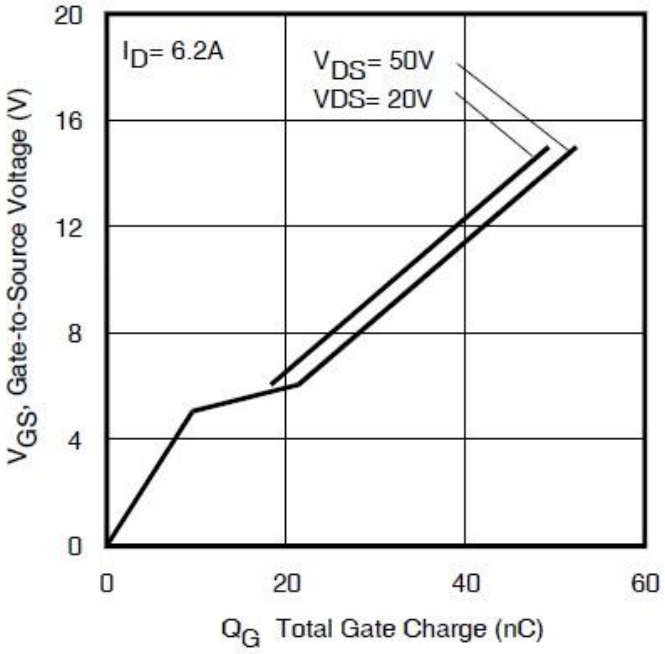

Figure 5.6: The total gate charge versus gate-to-source voltage graph of an IRF6644 DirectFET Power MOSFET (International Rectifier, 2012).

Figure 5.6 compares the gate-source voltage to the total gate charge when a constant current is applied to the gate. With the first rising slope, the gate-to-source capacitance is charged. When the slope becomes less positive, the gate-to-drain capacitance is charged. When the slope increases again, both capacitors will be charged and the switching device will conduct between drain and source.

The average current that will flow when the gate-to-source voltage is applied, is defined by the following equation (Merello, A; Rugginenti, A; Grasso, A, 2012):

$$\begin{aligned} I_{AVG} &= \frac{Q_{GS} + Q_{GD}}{t_{SW}} \\ I_{AVG} &= \frac{9.6nC + 11.5nC}{43ns} \\ I_{AVG} &= 490mA \end{aligned} \tag{5.1}$$

I_{AVG} is the average current that is required to charge Q_{GS} and Q_{GD} so that the gate-source voltage reaches a value, which is shown in Figure 5.6, at the point where the plateau ends. Q_{GS} is the charge of the gate-to-source capacitance, Q_{GD} is the charge of the gate-to-drain capacitance and t_{SW} is the minimum time to charge Q_{GS} and Q_{GD}. R_g can then be calculated by the following equation (Merello, A; Rugginenti, A; Grasso, A, 2012):

$$\begin{aligned} R_g &= \frac{V_{gate} - V_{GS(th)}}{I_{AVG}} \\ R_g &= \frac{15V - 4.8V}{0.490A} \\ R_g &= 20.8\Omega \end{aligned} \tag{5.2}$$

R_g is the gate resistor required in series with the gate of the FET. V_{gate} is the maximum voltage obtained from the gate drive IC's output. $V_{GS(th)}$ is the maximum gate-to-source threshold voltage required to turn on the MOSFET.

The energy consumed by the gate resistor during turn on can be determined by:

$$\begin{aligned} E_{(R_g)} &= I_{R_{gate}}^2 \cdot R_g \cdot t_{on} \\ E_{(R_g)} &= (0.490A)^2 \cdot 20\Omega \cdot 43ns \\ E_{(R_g)} &= 206.49nJ \end{aligned} \tag{5.3}$$

The bootstrap capacitor is used in conjunction with the bootstrap diode to store energy which is used to turn on the switching device when required. The value of the capacitor can be calculated with the following equation (International Rectifier, 2012):

$$\begin{aligned} C_b &\geq \frac{\left[2Q_g + \frac{I_{qbs(\max)}}{f_{sw}} + Q_{ls} + \frac{I_{cbs}}{f_{sw}}\right]}{V_{cc} - V_f - V_{ls} - V_{\min}} \\ C_b &\geq \frac{\left[2 \cdot 47nC + \frac{150\mu A}{330kHz} + 5nC + 0\right]}{15V - 1V - 0V - 13.5V} \\ C_b &\geq 198.9nF \end{aligned} \tag{5.4}$$

where V_{min} is the minimum voltage between pins V_B and V_S of the gate drive IC, V_{LS} is the volt drop across the low-side FET, V_f is the forward voltage drop across the bootstrap diode, V_{CC} is the supply voltage applied to the gate drive IC, Q_g is the total gate charge required by the MOSFET, I_{qbs} is the quiescent current for the high-side driver, f_{sw} is the switching frequency, Q_{ls} is the level shift charge required per cycle and I_{cbs} is the bootstrap capacitor leakage current.

The decoupling capacitor, *C*, in Figure 5.5 connected to V_{CC} is used to compensate for the inductance of the supply line (International Rectifier, 2012). This capacitor must be placed as close to the IC as possible. The bootstrap diode, *D*, must be able to block the full voltage across the DirectFET when the diode is reverse biased. In this application the maximum voltage across the switching device is *100V* divided by five cells, *20V*. The current rating of the diode is calculated by multiplication of the total gate charge of the gate capacitance by the switching frequency. The diode in this application must have a minimum current rating of *35nC* multiplied by *300 kHz* equals *10.5mA* (International Rectifier, 2012). The diode must also be an ultrafast recovery diode.

5.2.1.3 Flying capacitors

The flying capacitors are labelled *C1-C4* in Figure 5.3. The flying capacitors, also referred to as the floating capacitors, will naturally balance according to equation 3.2. The maximum voltage across each switching device will be *20V*. The capacitor voltage will decrease from *80V*, for *C1*, to *20V* across *C4* in steps of *20V*. The flying capacitors are used to clamp the voltages between the switches. Within a switching cycle the output current flows through the flying capacitors causing a ripple voltage. This ripple voltage is constrained to *5%* of the DC-Bus voltage (Molepo, 2003, p. 55). With a ripple voltage of *5V*, a phase shift of *1.26rad/s*, a switching frequency of *300 kHz* and an output current of *10A*, equation 5.5 can be used to calculate the value of the flying capacitors.

$$C_k > \frac{\phi \cdot I_{dc}}{2 \cdot \pi \cdot f \cdot \Delta V_{C_k \max}} \tag{5.5}$$

The minimum values for the flying capacitors are *1.34µF*. The voltage rating of the four flying capacitors must be *20V*, *40V*, *60V* and *80V*. The closet practical value found for the capacitor was a *1.5µF 400V* capacitor.

5.2.1.4 Heat sink design

The purpose of heat sink design is to determine the thermal resistance of the heat sink required to dissipate the heat generated by the switching device. The heat sink assists the switching device to get rid of excess heat energy by increasing the surface area of the transistor in order to have a larger contact area with the ambient temperature. The thermal resistance is defined by the following equation:

$$R_\theta = \frac{\Delta T}{P_D} \tag{5.6}$$

where R_θ is the thermal resistance, ΔT is the temperature difference and P_D is the power being dissipated. The maximum case temperature, T_c, can be obtained from the datasheet which is *150°C*. The power being dissipated by the switching device must be calculated, and the total power dissipation, P_T, consists of the switching losses (P_{sw}), conduction losses (P_{con}) and reverse recovery losses (P_{rr}) of the internal diode.

The losses can be calculated with the following equations (Molepo, 2003, p. 72):

$$\begin{aligned} P_{con} &= R_{DS(on)} I^2 D \\ P_{con} &= (10.3m\Omega)(10)^2(0.5) \\ P_{con} &= 0.515W \end{aligned} \qquad (5.7)$$

where $R_{DS(on)}$ is the resistance between drain and source when the FET is on, I is the current and D is the duty cycle.

$$\begin{aligned} P_{SW} &= \frac{f_{sw}}{2\pi} V_{cell} \beta (t_{on} + t_{off}) \\ P_{SW} &= \frac{300kHz}{2\pi} \cdot 20V \cdot 14.14A(43ns + 50ns) \\ P_{SW} &= 1.38W \end{aligned} \qquad (5.8)$$

where f_{sw} is the switching frequency, V_{cell} is the voltage across the switching device, β is the peak current ($I \times \sqrt{2}$), t_{on} is the turn on time and t_{off} is the turn off time.

$$\begin{aligned} P_{rr} &= 0.125 \cdot Q_{rr} \cdot V_{cell} \cdot f_{sw} \\ P_{rr} &= 0.125(100nC)(20V)(300kHz) \\ P_{rr} &= 82.5mW \end{aligned} \qquad (5.9)$$

where Q_{rr} is the reverse recovery charge.

The total power dissipation is:

$$\begin{aligned} P_T &= P_{con} + P_{SW} + P_{rr} \\ P_T &= 0.515W + 1.38W + 82.5mW \\ P_T &= 1.98W \end{aligned} \qquad (5.10)$$

The ambient temperature, T_a, is chosen to be *40°C*. The total thermal resistance, $R_{\theta(j-a)}$, of the thermal system can be calculated by making use of equation 5.6, with ΔT*=110°C* and P_D=P_T, which resulted in a thermal resistance of *55.56°C/W*.

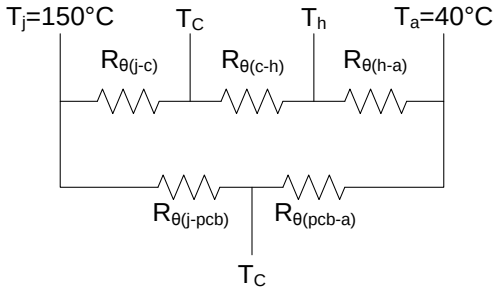

Figure 5.7: The thermal resistances of the thermal system.

In Figure 5.7 the top leg consisting of elements $R_{\theta(j-c)}$ (thermal resistance of junction-to-case), $R_{\theta(c-h)}$ (thermal resistance of case-to-heat sink) and $R_{\theta(h-a)}$ (thermal resistance of heat sink-to-ambient), is a train of elements normally found when dealing with heat sink design. The $R_{\theta(j-c)}$, *1.4°C/W*, can be obtained from the data sheet of the switching device used. The $R_{\theta(c-h)}$ is normally the thermal resistance of the material used to electrically isolate the switch from the heat sink. In this case it is the thermal resistance of special double sided tape with low thermal resistance of *0.9°C/W* to attach the heat sink to the DirectFET. Electrical isolation is not required as each switching device (DirectFET) has its own small heat sink.

The thermal resistance of the heat sink, $R_{\theta(h\text{-}a)}$, can be calculated by subtraction of the $R_{\theta(j\text{-}c)}$ and $R_{\theta(c\text{-}h)}$ from the total thermal resistance, which results in a thermal resistance of *53.26°C/W*. A heat sink with a profile suitable for the DirectFET was chosen. This heat sink had a thermal resistance of *28.5°C/W*, which is smaller than required. The temperature difference across the heat sink plus the ambient temperature resulted in a case temperature of *98°C*.

The DirectFET is a surface mount device (SMD), which means that the printed circuit board (PCB) can also be used as a heat sink.

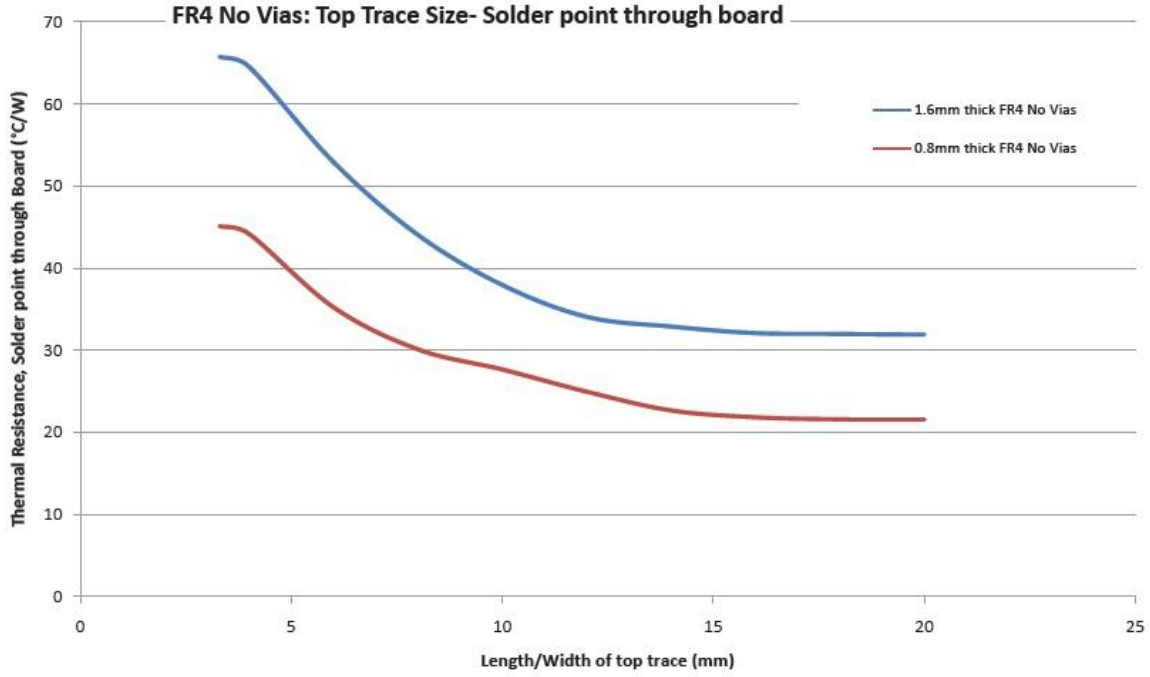

Figure 5.8: Thermal resistance versus length and width of FR4 double sided PCB material in thickness of 1.6mm and 0.8mm (Cree, 2012).

Figure 5.8 represents a graph which depicts the thermal resistance with respect to the area of FR4 double sided PCB material. The area of copper surrounding the DirectFET is $25mm^2$ which has a thermal resistance of *65°C/W*. The DirectFET has a thermal resistance from junction-to-PCB, $R_{\theta(j\text{-}pcb)}$ (see Figure 5.7), of *1°C/W*. This means that there is a thermal path in parallel to the other train of elements to ambient with a thermal resistance of *66°C/W*. The thermal resistance of the total system is recalculated as resisters in series and parallel with a value of *21.1°C/W*. The power dissipated through these two channels can be calculated as the power dissipation propagates through the elements in the same way as current circulates through a circuit.

The power dissipation propagating through the top leg of elements, P_{top}, in Figure 5.7 can be calculated as follows:

$$P_{top} = \frac{P_D\left(R_{\theta(j-pcb)} + R_{\theta(pcb-a)}\right)}{R_{\theta(j-pcb)} + R_{\theta(pcb-a)} + R_{\theta(j-c)} + R_{\theta(c-h)}R_{\theta(h-a)}}$$

$$P_{top} = \frac{1.98(1+65)}{(1+65+1.4+0.9+28.5)} \qquad (5.10)$$

$$P_{top} = 1.36W$$

The case temperature can then be calculated as follows:

$$T_C = T_a + (P_{top} \cdot R_{\theta(h-a)}) + (P_{top} \cdot R_{\theta(c-h)})$$
$$T_C = 40 + (1.36 \times 28.5) + (1.36 \times 0.9) \quad (5.11)$$
$$T_C = 80°C$$

Using the PCB as a heat sink improves the thermal system performance. If enough space is available, the PCB can perform the function as a heat sink. Incorporating vias into the PCB thermally connects the top and bottom layer of the PCB and this helps to reduce the space needed to dissipate heat.

5.2.1.5 DC capacitors and Bleeder resistors

The DC capacitors can be seen in Figure 5.3 and are labelled as *C5* and *C6*. The bleeder resistors are in parallel with the DC capacitors and are labelled *R1* and *R2*. The primary function of the DC capacitors is to create a virtual ground between the positive voltage and ground of the DC-Bus. This allows the output voltage of the Multicell inverter to swing around the virtual ground. The secondary function of these DC capacitors is to absorb any noise that might be on the DC-Bus. The following equation can be used to calculate the value of the DC capacitors (Molepo, 2003, p. 57):

$$C_{DC} = \frac{I_{peak}}{\omega \cdot V_{ripple}} \quad (5.7)$$

As only half of the current flows through the top and bottom at a time, I_{peak} is *14.14A*. The value of ω is determined by the frequency of the reference signal of *22.1 kHz*. A ripple voltage of *1%* is assumed. The value of C_{DC} is *101.8µF*. The bus voltage is *100V* and therefore the minimum voltage that the capacitor must withstand is *50V*. A *120µF*,*100V*, capacitor was used.

The function of the bleeder resistors is to discharge the DC capacitors when the inverter is switched off. This is done to prevent electrocution. The discharge time can be set to any time length. Making the discharge time very short will result in a physically large resistor as the resistor must dissipate the energy as heat. The power rating of the resistor in conjunction with the maximum voltage charge of the capacitor is used to determine the resistor value by equation 5.8.

$$R = \frac{V^2}{P} \quad (5.8)$$

When a *0.5W*, *P*, resistor is used with a voltage value of *50V*, *V*, the resistor value is *5kΩ*.

Using equation 5.9 (Molepo, 2003, p. 58) the time that it will take to discharge the capacitor to a safe value of *10V*, *v(t)*, will then be *1s*.

$$t = -RC\ln(\frac{v(t)}{V_O}) \quad (5.9)$$

Although the maximum voltage across the capacitor is relatively low and not a huge risk, the process can be used to determine the value of the resistor and how long it will take for the capacitor to discharge to a safe value.

5.2.2 Bootstrap power supplies

Figure 5.9 represents a simplified circuit diagram of a bootstrap power supply. C_1-C_5 represents the bootstrap capacitors and D_1-D_4 represents the bootstrap diodes. The *5V* and *15V* regulators have been left out to simplify the circuit diagram. The *5V* regulator is a KF05 IC which is used for the optical receiver and the MC7815 is used as a *15V* regulator for the single high-side driver IC.

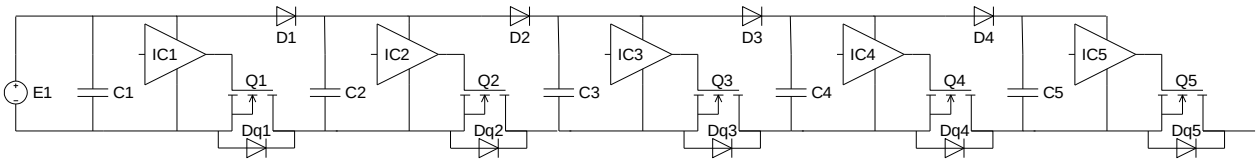

Figure 5.9: Circuit diagram of a bootstrap power supply.

Table 5-2 lists all the components that require energy from the bootstrap power supply for one cycle of the switching frequency. One must also remember that the first section of the bootstrap power supply must supply energy to the next section and so on. To make sure that there is enough energy stored in the capacitor, twice the current requirement was used for the calculations.

Table 5-2: The current consumption of each device connected to the bootstrap power supply for one cycle of the switching frequency per cell.

Component	**Current**
5V regulator (KF05)	*500µA*
Optic receiver (HFBR2521)	*8.2mA*
15V regulator (MC7815)	*8mA*
Gate drive (IRS21850S)	*240µA*
Current consumption of the gate of the DirectFET	*6.93mA*
Total current per cycle	*23.87mA*

The voltages and current requirements of the bootstrap power supply in Table 5-3 can be expected during normal operation. These requirements for the positive and negative bootstrap power supplies are the same.

Table 5-3: Design specifications for a bootstrap power supply.

Parameter	Value	Unit
Input voltage (E1)	*22*	*V*
Input current (E1)	*240*	*mA*
Output voltage cell 1 (C1)	*15*	*V*
Output current cell 1 (E1)	*240*	*mA*
Output voltage cell 2 (C2)	*15*	*V*
Output current cell 2 (D1)	*192*	*mA*
Output voltage cell 3 (C3)	*15*	*V*
Output current cell 3 (D2)	*144*	*mA*
Output voltage cell 4 (C4)	*15*	*V*
Output current cell 4 (D3)	*96*	*mA*
Output voltage cell 5 (C5)	*15*	*V*
Output current cell 5 (D4)	*48*	*mA*

The current requirements per section can be seen in Table 5-2. As the current requirements per cycle are known, the charge of the capacitor can be calculated with the following formula:

$$Q = \frac{I}{f_{sw}}$$
$$Q = \frac{48mA}{300kHz} \qquad (5.10)$$
$$Q = 145.45nC$$

Then the capacitor value can be calculated as follows:

$$C = \frac{Q}{V}$$
$$C = \frac{145.45nC}{15V} \qquad (5.11)$$
$$C = 9.7nF$$

The value for the bootstrap capacitor calculated above would be the minimum value for bootstrap capacitor C_5. The minimum capacitance value for C_4 must be *19.4nF*, C_3 must be *29.1nF*, C_2 must be *38.8nF* and C_1 must be *48.5nF*. The increase of the capacitance value is because the first section of the bootstrap power supply must supply energy to the next section and so on. To simplify the construction of the circuit, a *100nF*, *35*V_{DC}, tantalum capacitor was used for each section of the bootstrap power supply.

The bootstrap diode must be a fast recovery diode as it must function at the switching frequency of the multicell inverter. The diode must also be able to withstand the cell voltage. (Molepo, 2003, p. 43) An SK310A diode was used with a recovery time of *500ns*, a forward conduction current of *3A* and a peak reverse voltage of *100V*.

5.2.3 Compensation networks

5.2.3.1 Compensation with series inductor

In section 4.2 the purpose of the series inductor was discussed. The value of the series inductor can be calculated by making use of equation 4.3. The anti-resonance frequency, f_a, of the transducer is *23944Hz*(loaded) and the clamped capacitance of the transducer, C_O, is *14.031nF* (loaded). The value of the inductor for a loaded transducer can be calculated as follows:

$$\begin{aligned} L_S &= \frac{1}{(2 \cdot \pi \cdot f_a)^2 \cdot C_O} \\ L_S &= \frac{1}{(2 \cdot \pi \cdot 23944Hz)^2 \cdot 14.031nF} \\ L_S &= 3.1489mH \end{aligned} \tag{5.12}$$

The value of *3.15mH* is used for the inductor.

Table 5-4: Series compensation inductor's design parameters.

Parameter	Symbol	Value	Unit
Inductance	L_S	*3.15*	*mH*
Inductor peak current	I_S	*14.14*	*A*
Frequency of the applied signal	f_o	*22.1*	*kHz*

A PM 74/53 core made with N27 ferrite material was chosen for this inductor. The properties of this core is summarised in Table 5-5.

Table 5-5: Specifications of the core and material of the serial inductor

Parameter	Symbol	Value	Unit
Frequency range	*f*	*20-150*	*kHz*
Effective area	A_e	*790*	mm^2
Bobbin window area	A_w	*884*	mm^2
Saturation flux density	B_{max}	*500*	*mT*

By using Faraday's law, $v=N(d\varphi/dt)$, and the equation that defines the voltage across an inductor, $v=L_f(di/dt)$, one can calculate the number of turns required to achieve a certain inductance:

$$\begin{aligned} N &= \frac{L \cdot I_{peak}}{B_{\max} \cdot A_e} \\ N &= \frac{3.15mH \cdot 14.14A}{500mT \cdot 884 \times 10^{-6}} \\ N &= 101turns \end{aligned} \tag{5.13}$$

where L is the inductance of the inductor, I_{peak} is the peak current flow in the inductor, B_{max} is the maximum flux density and A_e is the effective area of the core.

The air gap of the inductor must be determined so that the maximum flux density of the core is reached when the current flowing through the inductor is at a peak. The air-gap can be calculated by the following equation (Molepo, 2003, p. 51):

$$\begin{aligned} l_g &= \frac{\mu_0 \cdot N \cdot \hat{I}}{B_{\max}} \\ l_g &= \frac{4 \cdot \pi \cdot 10^{-7} \cdot 101 \cdot 14.14A}{500mT} \\ l_g &= 3.6mm \end{aligned} \qquad (5.14)$$

where l_g is the length of the air gap and μ_0 is the permeability of free space. An E-type core was used having three limbs resulting in the air-gap being *3.6mm* divided by three. The area of the copper conductor (A_{con}) was then calculated next. A current density of $6A/mm^2$ was used to calculate the copper area when a current of $10A_{RMS}$ flows through the inductor, and this results in $A_{con} = 1.67mm^2$. The depth of the current penetration as a result of skin effect can be calculated as (Mohan, et al., 2003, p. 748):

$$\begin{aligned} \delta &= \sqrt{\frac{2}{\mu_i \cdot \sigma \cdot \omega}} \\ \delta &= \sqrt{\frac{2}{1.256x10^{-6} \cdot 59.52x10^{6} \cdot 2 \cdot \pi \cdot 22100}} \\ \delta &= 438.93\mu m \end{aligned} \qquad (5.15)$$

where δ is the skin depth, μ_i is the permeability of the copper and σ is the conductivity of copper. When the diameter of the conductor is selected to be $\leq 2\delta$, the effects of skin effect can be ignored. *0.8mm* diameter copper wire was used to wind the inductor. The area of wire with a diameter of *0.8mm* is equal to πr^2 or $0.502mm^2$. The number of conductors required is then A_{con} divided by $0.502mm^2$, which results in four conductors.

The number of windings that will fill the winding window of the core can be calculated through changing of the subject of the formula of the copper fill factor equation (Mohan, et al., 2003, p. 752):

$$\begin{aligned} N &= \frac{K_C \cdot A_W}{A_{con}} \\ N &= \frac{0.5 \cdot 884}{0.502} \\ N &= 880turns \end{aligned} \qquad (5.16)$$

where *Kc* is the copper fill factor and A_w is the winding window. The maximum number of windings that the core can accommodate is *880 turns*. The inductor requires *101* windings with *4* conductors each in parallel which equals *404* turns and is less than the maximum number of windings.

5.2.3.2 Compensation with parallel inductor

In section 4.4 the purpose of the parallel inductor was discussed. The value of the parallel inductor can be calculated by making use of equation 4.4. The resonance frequency, f_r, of the transducer is *23944Hz* (loaded), and the clamped capacitance of the transducer, C_O, is *14.031nF* (loaded).

The value of the inductor for a loaded transducer can be calculated as follows:

$$L_P = \frac{1}{(2 \cdot \pi \cdot f_r)^2 \cdot C_O}$$
$$L_P = \frac{1}{(2 \cdot \pi \cdot 22060Hz)^2 \cdot 14.031nF} \quad (5.17)$$
$$L_P = 3.70972mH$$

An inductor would be made with a value of *3.71mH*.

Table 5-6: Parallel compensation inductor's design parameters.

Parameter	Symbol	Value	Unit
Inductance	L_S	*3.71*	*mH*
Inductor peak current	I_S	*14.14*	*A*
Frequency of the applied signal	f_o	*22.1*	*kHz*

A PM 74/53 core made with N27 ferrite material was chosen for this inductor. The properties of this core is summarised in Table 5-5.

Table 5-7: Specifications of the core and material

Parameter	Symbol	Value	Unit
Frequency range	*f*	*20-150*	*kHz*
Effective area	A_e	*790*	mm^2
Bobbin window area	A_w	*884*	mm^2
Saturation flux density	B_{max}	*500*	*mT*

By using Faraday's law, $v=N(d\varphi/dt)$, and an equation that defines the voltage across an inductor, $v=L_f(di/dt)$, one can calculate the number of turns required to achieve a certain inductance:

$$N = \frac{L \cdot I_{peak}}{B_{\max} \cdot A_e}$$
$$N = \frac{3.71mH \cdot 14.14A}{500mT \cdot 884 \times 10^{-6}} \quad (5.18)$$
$$N = 119turns$$

where L is the inductance of the inductor, I_{peak} is the peak current flow in the inductor, B_{max} is the maximum flux density and A_e is the effective area of the core.

The air gap of the inductor must be determined so that the maximum flux density of the core is reached when the current flowing through the inductor is at a peak. The air-gap can be calculated by the following equation (Molepo, 2003, p. 51):

$$I_g = \frac{\mu_0 \cdot N \cdot \hat{I}}{B_{\max}}$$
$$I_g = \frac{(4 \cdot \pi \cdot 10^{-7}) \cdot 119 \cdot 14.14A}{500mT} \quad (5.19)$$
$$I_g = 4.23mm$$

An E-type core was used having three limbs, resulting in the air-gap being *4.23mm* divided by three. The area of the copper conductor (A_{con}) was calculated next. A current density of *6A/mm²* was used to calculate the copper area when a peak current *14.14A* flows through the inductor, and this results in A_{con} *=2.36mm²*. The depth of the current penetration is the same as in equation 5.15 with a value of 438.93*μm. An 0.8mm* diameter copper wire was used to wind the inductor. The area of wire with a diameter of *0.8mm* is equal to *πr²* or *0.502mm²*. The number of conductors required is then A_{con} divided by *0.502mm²* which results in four conductors.

The number of windings that will fill the winding window of the core is the same as in equation 5.16 with a value of 880 turns. The maximum number of windings that the core can accommodate is *880 turns*. The inductor requires *119* windings with *4* conductors each in parallel which equals *476* turns and which is less than the maximum number of windings.

5.2.3.3 Q-Matching

Q-Matching is discussed in section 4.4. This method places a capacitor, C_P, in parallel with the clamped capacitor, C_O, of the piezoelectric transducer in order to reduce the impedance of the transducer to that of the source. A series resonance circuit consisting of L_S and C_S is added to cancel the capacitive reactance of the load. This circuit can be seen in Figure 4.4. Equation 4.11 is used to calculate C_2 which is the combined value of C_O and C_P:

$$C_2 = \frac{1}{\omega}\sqrt{\frac{R_P - R_S}{R_P^2 R_S}}$$
$$C_2 = \frac{1}{2 \cdot \pi \cdot 22100}\sqrt{\frac{8.1607 - 1.64}{8.1607^2 \cdot 1.64}} \quad (5.20)$$
$$C_2 = 1.75964\mu f$$

The value of C_P can then be determined by subtraction of the clamped capacitance, C_O*=14.031nf*, from C_2 and this results in *1.74561μf*. The value of C_S is calculated making use of equation 4.13:

$$C_S = \frac{1}{\omega\sqrt{R_S R_P - R_S^2}}$$
$$C_S = \frac{1}{2 \cdot \pi \cdot 22100\sqrt{1.64 \cdot 8.1607 - 1.64^2}} \quad (5.23)$$
$$C_S = 2.2\mu f$$

The inductor placed in series with C_S forms a series resonant circuit to cancel the capacitive reactance of the load and can be calculated by making use of equation 4.16:

$$L_S = \frac{\sqrt{R_S}\left(2R_P + R_S\right)}{\omega\sqrt{R_P - R_S}}$$
$$L_S = \frac{\sqrt{1.64}\left(2 \cdot 8.1607 + 1.64\right)}{2 \cdot \pi \cdot 22100\sqrt{8.1607 - 1.64}} \qquad (5.21)$$
$$L_S = 64.82\mu H$$

Table 5-8 are the specifications for the inductor required for the Q-matching network.

Table 5-8: Inductor specifications for the inductor used to implement Q-matching.

Parameter	Symbol	Value	Unit
Inductance	L_S	*64.8*	μH
Inductor peak current	I_S	*14.14*	*A*
Frequency of the applied signal	f_o	*22.1*	*kHz*

A PM 50/39 core made with N27 ferrite material was chosen for this inductor. The properties of this core is summarised in Table 5-9.

Table 5-9: Specifications of the core and material of the serial inductor

Parameter	Symbol	Value	Unit
Frequency range	*f*	*20-150*	*kHz*
Effective area	A_e	*173*	mm^2
Bobbin window area	A_w	*420*	mm^2
Saturation flux density	B_{max}	*500*	*mT*

By using Faraday's law, $v=N(d\varphi/dt)$, and an equation that defines the voltage across an inductor, $v=L_f(di/dt)$, one can calculate the amount of turns required to achieve a certain inductance:

$$N = \frac{L \cdot I_{peak}}{B_{\max} \cdot A_e}$$
$$N = \frac{64.8\mu H \cdot 14.14A}{500mT \cdot 173 \times 10^{-6}} \qquad (5.22)$$
$$N = 11 turns$$

The air gap of the inductor must be determined so that the maximum flux density of the core is reached when the current flowing through the inductor is at a peak.

The air-gap can be calculated by the following equation (Molepo, 2003, p. 51):

$$l_g = \frac{\mu_0 \cdot N \cdot I_{peak}}{B_{\max}}$$
$$l_g = \frac{4 \cdot \pi \cdot 10^{-7} \cdot 6 \cdot 14.14A}{500mT} \quad (5.23)$$
$$l_g = 0.213mm$$

Where l_g is the length of the air gap and μ_0 is the permeability of free space. An E-type core was used having three limbs resulting in the air-gap being *0.213mm/3*. The area of the copper conductor *(A_{con})* must be calculated next. A current density of $6A/mm^2$ was used to calculate the copper area when a current $10A_{RMS}$ flows through the inductor, and this results in $A_{con} = 1.67mm^2$. The depth of the current penetration as a result of skin effect can be calculated as (Mohan, et al., 2003, p. 748):

$$\delta = \sqrt{\frac{2}{\mu_i \cdot \sigma \cdot \omega}}$$
$$\delta = \sqrt{\frac{2}{1.256x10^{-6} \cdot 59.52x10^{6} \cdot 2 \cdot \pi \cdot 22100}} \quad (5.24)$$
$$\delta = 438.93\mu m$$

When the diameter of the conductor is selected to be $\leq 2\delta$, the effects of skin effect can be ignored. *0.8mm* diameter copper wire was used to wind the inductor. The area of wire with a diameter of *0.8mm* is equal to πr^2 or $0.502mm^2$. The number of conductors required is then A_{con} divided by $0.502mm^2$ which results in four conductors.

The number of windings that will fill the winding window of the core can be calculated through change of the subject of the formula of the copper fill factor equation (Mohan, et al., 2003, p. 752) :

$$N = \frac{K_C \cdot A_W}{A_{con}}$$
$$N = \frac{0.5 \cdot 420}{0.502} \quad (5.25)$$
$$N = 418turns$$

where K_c is the copper fill factor and A_w is the winding window. The maximum number of windings that the core can accommodate is *418* turns. The inductor requires *11* windings with *4* conductors each in parallel which equals *44* turns and is less than the maximum number of windings.

5.3 Summary.

This chapter examined an overview of the system required to answer the research question. A full design followed on all the different aspects of the system and all the subsystems. Component values were calculated and components were chosen.

We next turn to the experiments in order to evaluate the performances of the different setups.

CHAPTER SIX

Experimental setup and results.

6.1 Introduction

This chapter presents the setup of all the experiments and results obtained from practical work. Experimental results were obtained of the bootstrap power supplies, the six-level multicell inverter (discussed in chapter three) and the compensation networks (discussed in chapter four). The multicell inverter was also compared with an industrial standard ultrasonic amplifier and a linear audio amplifier.

The following equipment was used to obtain the results for the experiments conducted:

- Hewlett Packard 4192A LF impedance analyser (5Hz-13MHz)
- PM100 single phase power analyser
- 2 x Tektronix TDS 2024B four channel digital oscilloscope
- Delta Elektronika DC power supply (SM 300-10D)
- 3 x power supply (based on the LM200 voltage regulator)
- 4 x Tektronix P5205 100MHz high voltage differential probe
- 2 X Tektronix 1103 Tekprobe power supply
- 1 x Tektronix TCP312 current probe
- 1 x Tektronix TCPA300 Amplifier, AC/DC current probe
- 2 x Fluke 77 IV Series Digital multi-meter
- Crest CA6 Audio amplifier
- Agilent 33210A 10MHz function / arbitrary waveform generator

The HP impedance analyser was connected to a PC and Lab View was used to obtain measurements in order to plot impedance curves of the transducers. USB flash drives were used to capture scope traces from the two Tektronix TDS 2024B, and information was recorded from the PM100 and fluke 77 by hand.

6.2 Bootstrap power supplies

The aim of this experimental work is to verify the operation of the bootstrap power supply. The bootstrap power supplies are required to supply power to the gate drive circuits and optical transducers of each cell. The bootstrap power supply and the multicell inverter were discussed in chapter three. The bootstrap power supply was implemented and used on a 5 cell multicell inverter.

6.2.1 Experimental setup of the bootstrap power supply

The bootstrap power supply functions are explained in section 3.3. Two DC power supplies were used to supply power to the top and bottom bootstrap power supplies as depicted in Figure 5.3 (see E1 and E2). The gate signals produced by the controller are as explained in section 5.1. The experimental setup is as shown in Figure 6.1.

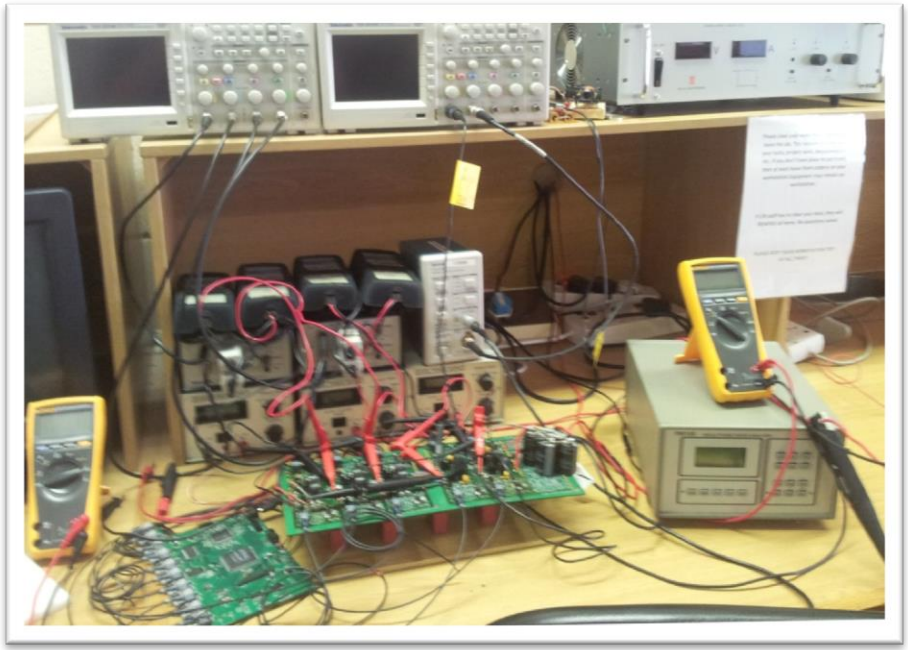

Figure 6.1: Experimental setup.

6.2.2 Experimental results of the Bootstrap Power Supply

The two DC power supplies were set to *24.97V*. From the results in Table 6-1 the volt drop across each diode can be observed and is very small. The total volt drop across the four diodes is *1.96V* and therefore the *15V* regulators could be left out as the maximum supply voltage to the bootstrap power supply could be set to *17V* without damaging the DirectFET or the driver of any of the cells.

Table 6-1: Experimental results obtained from the two bootstrap power supplies.

	Top				Bottom			
Switch no.	**Bootstrap capacitor voltage**	**Voltage drop across bootstrap diode**	**Voltage supplied to the gate drives**	**Voltage supplied to the optical interface**	**Bootstrap capacitor voltage**	**Voltage drop across bootstrap diode**	**Voltage supplied to the gate drives**	**Voltage supplied to the optical interface**
1	*23.01V*		*14.83V*	*5.00V*	*24.97V*		*15.00V*	*4.95V*
		0.41V				*0.53V*		
2	*23.42V*		*15.02V*	*4.95V*	*24.44V*		*14.97V*	*5.01V*
		0.46V				*0.51V*		
3	*23.88V*		*14.90V*	*4.94V*	*23.93V*		*14.93V*	*4.95V*
		0.51V				*0.48V*		
4	*24.39V*		*14.98V*	*4.97V*	*23.45V*		*15.06V*	*4.98V*
		0.58V				*0.44V*		
5	*24.97V*		*15.04V*	*4.92V*	*23.01V*		*15.03V*	*4.96V*

The maximum V_{GS} for the DirectFET is *20V* (International Rectifier, 2012, p. 2), and the gate driver can withstand a maximum input voltage of *25V* and has an internal voltage clamp of *20V* to make sure that the output of the gate drive never exceeds *20V* (International Rectifier, 2008, p. 2). The optic interface requires a *5V* supply and therefore it is required to reduce the supply voltage to *5V*. The unfiltered output voltage of the five cell multicell inverter can be seen in Figure 6.5, and this proves that the two bootstrap power supplies are supplying the required energy to the individual gate drive circuits.

6.3 Five cell multicell inverter

The aim of the experimental work is to verify the operation of the five cell multicell inverter. The circuit diagram of the experimental setup can be seen in Figure 5.3. The bootstrap power supplies are also used. Figure 6.2 shows the constructed circuit of a five cell multicell inverter using DirectFET's as switching devices.

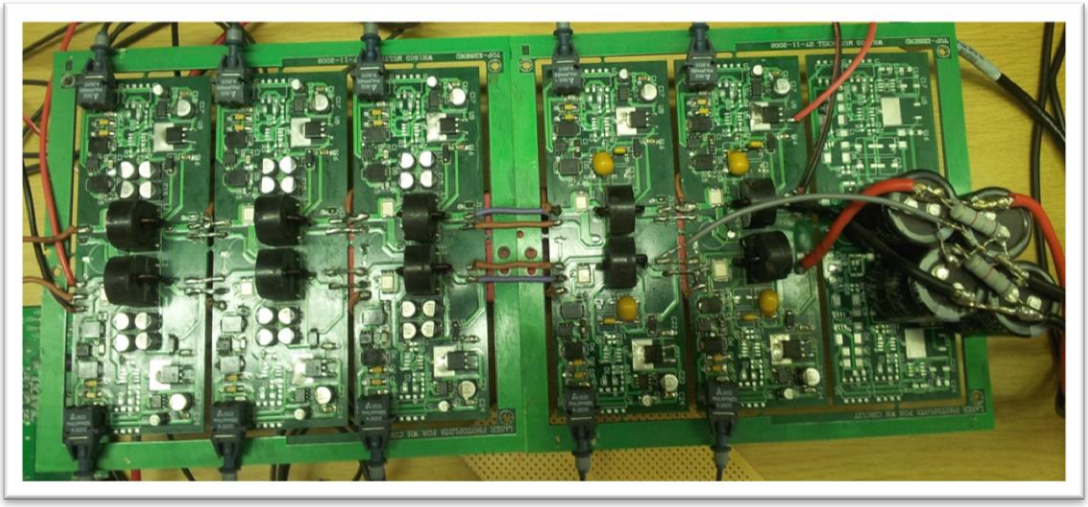

Figure 6.2: Five cell multicell inverter with bootstrap power supplies.

The cell capacitors are mounted underneath the PCB with very short conductors in order to have the cell capacitors as close to the switches as possible. Figure 6.3 shows this.

Figure 6.3: The cell capacitors mounted underneath the PCB.

6.3.1 Experimental setup of the five cell multicell inverter

Figure 6.4 shows the block diagram of the experimental setup. The Delta power supply is used as the main power supply and one L200 power supply is used to power the Controller which requires a 5V auxiliary power supply. The other two L200 power supplies are used as auxiliary power supplies to supply 25V to the top and bottom bootstrap power supplies individually. As illustrated in Figure 6.4, no filter or compensation network is connected between the multicell inverter and a resistive load of 2.47Ω. The main Delta supply is set to supply 100V DC to the DC capacitors and multicell inverter.

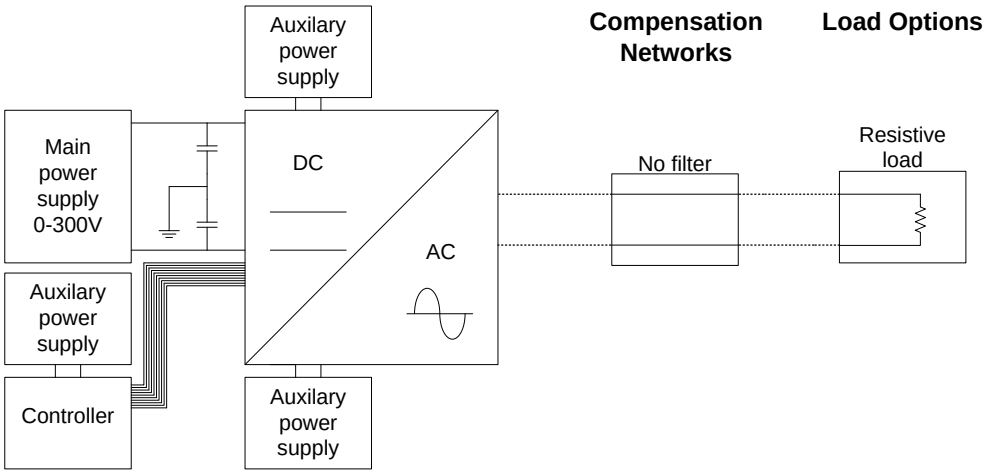

Figure 6.4: Block diagram of the experimental setup.

6.3.2 Experimental results of the five cell multicell inverter

Table 5-1 gives a list of the specifications for the multicell inverter. Figure 6.5 shows the output voltage of the five cell multicell inverter producing six voltage steps. The output frequency, *22085Hz*, is close to the required *22.1kHz* and the output peak to peak voltage is measured at *129V*. If the peaks of the noise on the voltage signal could be ignored, the output peak to peak voltage is measured to be *104V*.

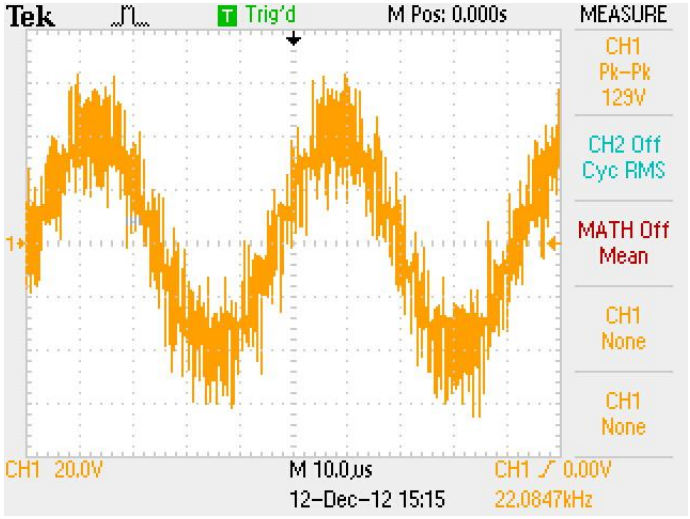

Figure 6.5: The output voltage of a five cell multicell inverter producing six voltage levels.

According to the theory (equation 3.2), the voltage across the cell capacitors with a supply voltage of *100V* should differ with *20V* per cell capacitor. With reference to Figure 5.3, Figure 6.6 shows the voltage of the cell capacitors with values of C_1=*79.5V*, C_2=*60.7V*, C_3=*40.7* and C_4=*20.7V*. The peaks that can be seen in Figure 6.6 represent the current flow between cells in order to stay balanced.

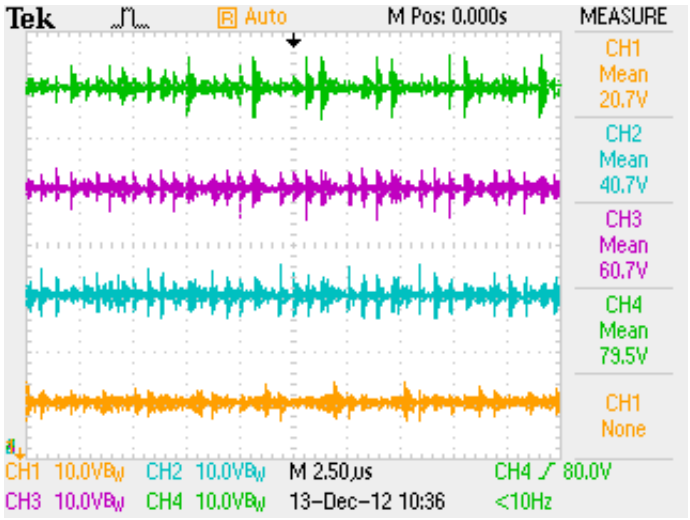

Figure 6.6: The voltage values of the four cell capacitors.

The design specification required a maximum current of $10A_{RMS}$. With a resistive load of *2.47Ω* and a supply voltage of $24.95V_{RMS}$, a current flow of $10.1A_{RMS}$ was achieved with a power of *252VA*. This is also the maximum supply current the Delta power supply could deliver.

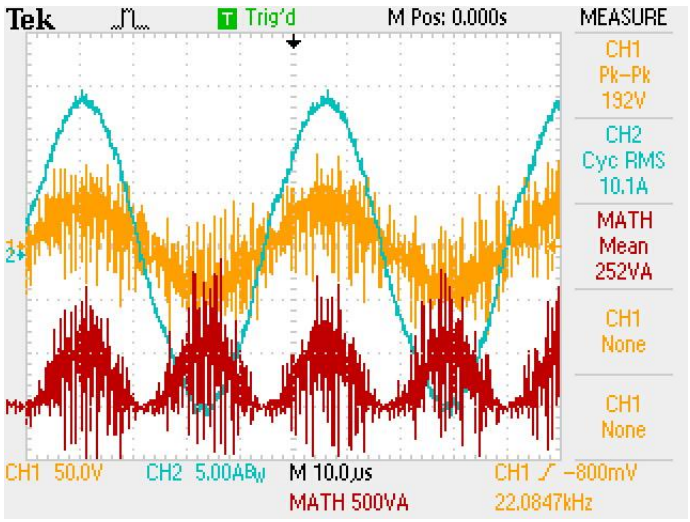

Figure 6.7: A screen capture from an oscilloscope of the output voltage, current and power of the output signal from the five cell multicell inverter.

To verify the theory of the harmonic content of a multicell inverter, the Fast Fourier Transfer (FFT) function of the oscilloscope was used to obtain the harmonic spectrum of the output voltage signal from the multicell inverter. This theory is discussed in section 3.5.1. With a switching frequency of *300kHz* and a reference frequency of *22.1kHz*, the first harmonic is expected to be situated around *1.5MHz* (*300kHz* multiplied by the number of cells of *5*) and the second harmonic situated around *3MHz* as shown in Figure 6.8 with cursor 1 and 2.

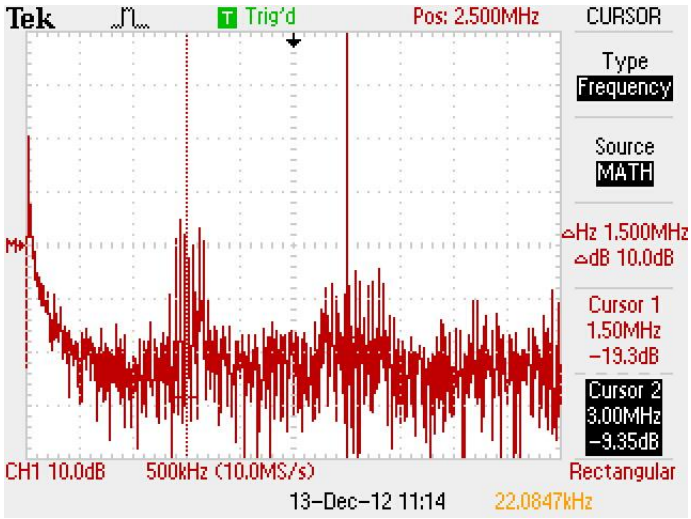

Figure 6.8: Frequency spectrum of the output voltage of a multicell inverter.

6.4 Compensation Networks

The purpose of these experiments is to determine if the compensation networks will "cancel" the capacitive reactance of the load in order to achieve a Power Factor (P.F.) of one which implies that the apparent power and the real power is the same. When this happens, the load reacts as a resistive load and all the applied power is dissipated by the load. The types of compensation networks that were examined were compensation with a series inductor (see section 4.3), compensation with a parallel inductor (see section 4.4) and compensation with Q-matching (see section 4.5).

The second reason for these experiments is to determine which one of the compensation networks will reduce the harmonic content the most from the multicell inverter and the third objective is to determine if the cell voltages of the multicell inverter stays naturally balanced.

6.4.1 Experimental setup with no compensation network.

A current response curve of a piezoelectric load mimics the admittance curve of a transducer. PSpice was first used to simulate the current response curve of the piezoelectric load in order to correlate the results with the measured values obtained from the experiment with the Crest amplifier. The model for the piezoelectric load used in PSpice was derived in chapter two and is explained in detail. The PSpice simulation model can be seen in Figure 12.1. PSpice was used to obtain the input and output apparent power and the real power dissipated in the piezoelectric load, and this was used to determine the P.F. Simplorer was also used to simulate the interaction of the multicell inverter with the piezoelectric transducer. The experiment with a Crest CA6 audio amplifier and an Agilent signal generator with no compensation, while connected to a MPI-20 kHz-3 kW (502/932R, Branson Converter) piezoelectric load, were performed next.

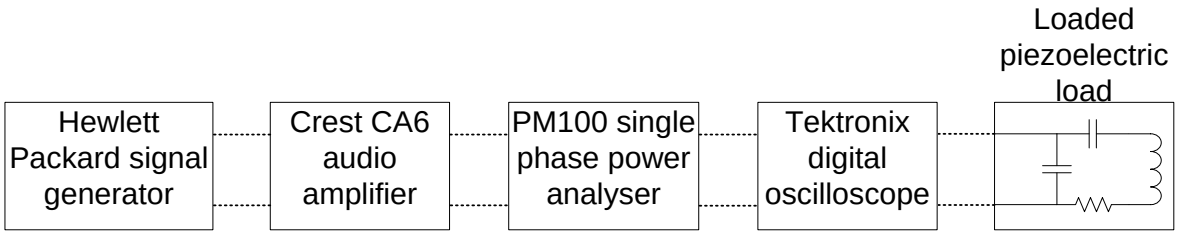

Figure 6.9: Experimental setup with Audio amplifier and piezoelectric load and no compensation network.

Figure 6.9 shows the block diagram of the experimental setup with no compensation network. The PM100 single phase power analyser was connected in series to measure current and in parallel to measure voltage. To ensure that the Tektronix oscilloscope measures the same values, the scope was also connected into the circuit with a current probe to measure the current and a 10:1 voltage probe to measure the voltage.

The frequency was increased from *10kHz* to *30kHz* and the magnitude of the current flowing through the load was recorded. The measurements were correlated between the oscilloscope and the power analyser. The real power, $V_{THD}(\%)$ and $I_{THD}(\%)$, was also recorded from the PM100 at the point of mechanical resonance.

The piezoelectric load, PM100 and Tektronix oscilloscope were then connected to the five cell multicell inverter as illustrated in Figure 6.10. The second Tektronix oscilloscope was used with four differential probes to capture the charging of the cell capacitors and how long it took until they reached their maximum voltage. The operating frequency of the multicell inverter was fixed at *22.163kHz* and was the same as the mechanical resonant frequency of the transducer. The voltage of the main Delta power supply was set to *68V* which would result in an output power in the region of *10W*.

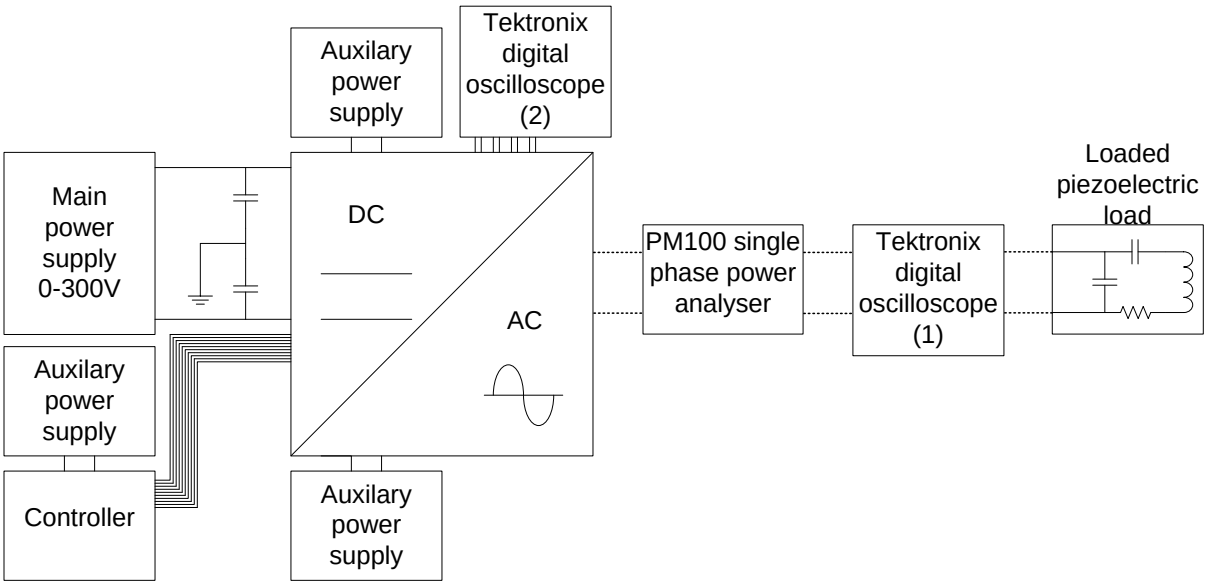

Figure 6.10: Experimental setup of multicell inverter and piezoelectric load with no compensation network.

When the Delta power supply was switched on, the second Tektronix scope was triggered, logging the information of the cell capacitors. The apparent power of the PM100 and Tektronix was recorded and the real power measured by the PM100 was also recorded.

A further experiment was performed to observe what filtering effect the conductors will have between the multicell inverter and the piezoelectric transducer. Two differential probes where removed across the cell capacitors, and one was connected directly across the output of the multicell inverter. The other differential probe was connected directly across the transducer. The main Delta power supply was switched on and the scope capture was recorded.

6.4.2 Experimental results with no compensation network

The simulated and measured current plot of the piezoelectric model and load can be seen in Figure 6.11. PSpice was used for the simulation and the experiment with the audio amplifier was used for the measured values. The model has a peak current flow of *1.18A* at *22,052kHz* and the transducer has a peak current flow of *1.05A* at *22,163kHz*. These peaks represent the thickness resonant mode of the model and the transducer. The small difference in frequency is due to the no-standard load conditions used when the transducer was applied to the load. The smaller peaks of the measured values situated at *22kHz* and *22.6kHz* shows the radial resonant point of the piezoelectric load.

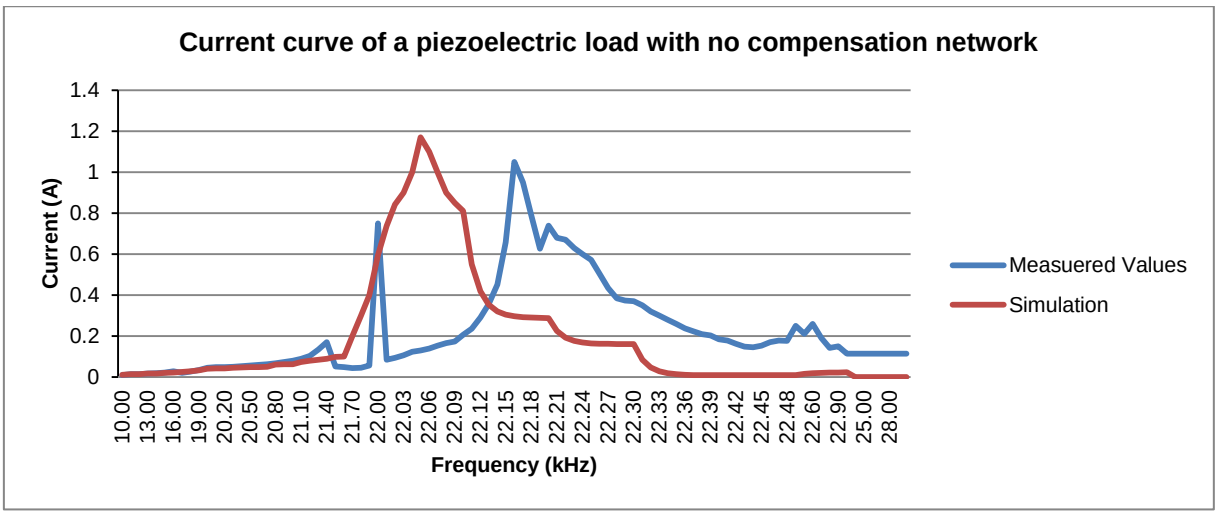

Figure 6.11: Experimental and simulated results of a current plot of the piezoelectric load and simulation model.

Table 6-2 summarises the experimental and simulated results obtained. The applied apparent power (*Pin(S)*) was measured with the PM100, and the apparent power (*Pout(S)*) was obtained through measuring of the applied voltage and current with the Tektronix oscilloscope. The efficiency of the compensation network was then determined by division of the output power by the input power. As there was no compensation network, the efficiency resulted in *100%*. The V_{THD}*(%)* represents the total harmonic distortion of the voltage produced by the source, and the I_{THD}*(%)* represents the total harmonic distortion of the current that the load creates. The multicell inverter produces a V_{THD} of *10.2%* where the crest amplifier produces a V_{THD} of only *0.3%.* As the 1st harmonic of the multicell inverter is situated at *1.5MHz*, it is still evident in the measurement (see Figure 6.12).

Table 6-2: Table with simulated and experimental results of piezoelectric load with no compensation network.

	Pin(S) PM100	Pout(S) scope	Efficiency of the network (%)	V_{THD} (%)	I_{THD} (%)	Pout (W)	P.F.	Rise time of cell capacitors
PSpice simulation	*13.9*	*13.9*	*100*			*11.6*	*0.83*	
Crest amplifier	*11.7*	*11.7*	*100*	*0.3*	*12.5*	*10.3*	*0.88*	
Simplorer simulation	*13.8*	*13.8*	*100*			*10.8*	*0.78*	*12.3ms*
Multicell inverter	*13.9*	*13.9*	*100*	*11.3*	*10.2*	*10.4*	*0.75*	*30ms*

The Power Factor (*P.F.*) in Table 6-2 shows clearly that the load has a reactive component and that maximum power transfer does not occur. This value of the *P.F.* was calculated by division of the real power (*Pout(W)*) by the output apparent power (*Pout(S)*). This was also evident in Figure 6.12, as the phase shift between the voltage and current waveforms can be observed.

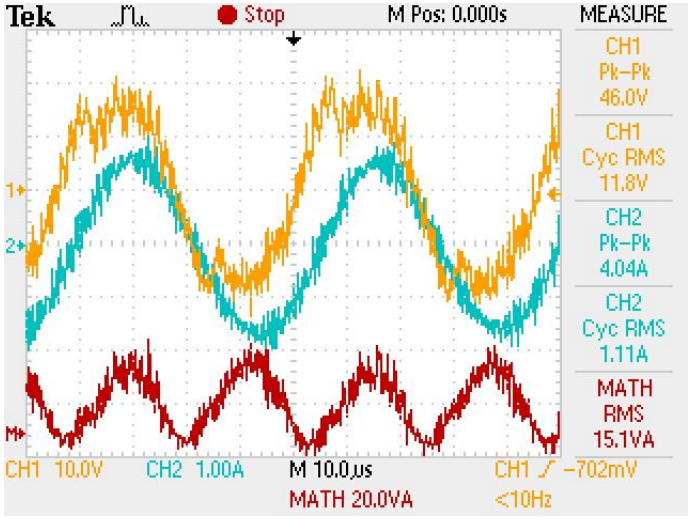

Figure 6.12: Capture of an oscilloscope of the output voltage, current and power of the multicell inverter which was connected to the piezoelectric load.

The rise time of the cell capacitors represents the time it took for all the cell capacitors to reach their maximum voltage as dictated by equation 3.2. The Simplorer simulation of the charging time of the cell capacitors is shown in Figure 6.13, where the last cell reaches a voltage of *9.3V* in *12.3ms*. According to equation 3.2 the cell capacitor voltages should be *54.4V, 40.8V, 27.2V* and *13.6V*. The simulated voltages correlate fairly closely to the expected values, as the simulated values are *52.3V, 38V, 23.2V* and *9.3V*. Figure 6.14 shows the practical result obtained from the multicell inverter. The cell capacitors took 30ms to charge to their respective values of *56.7V, 43.8V, 28.6V* and *16V*.

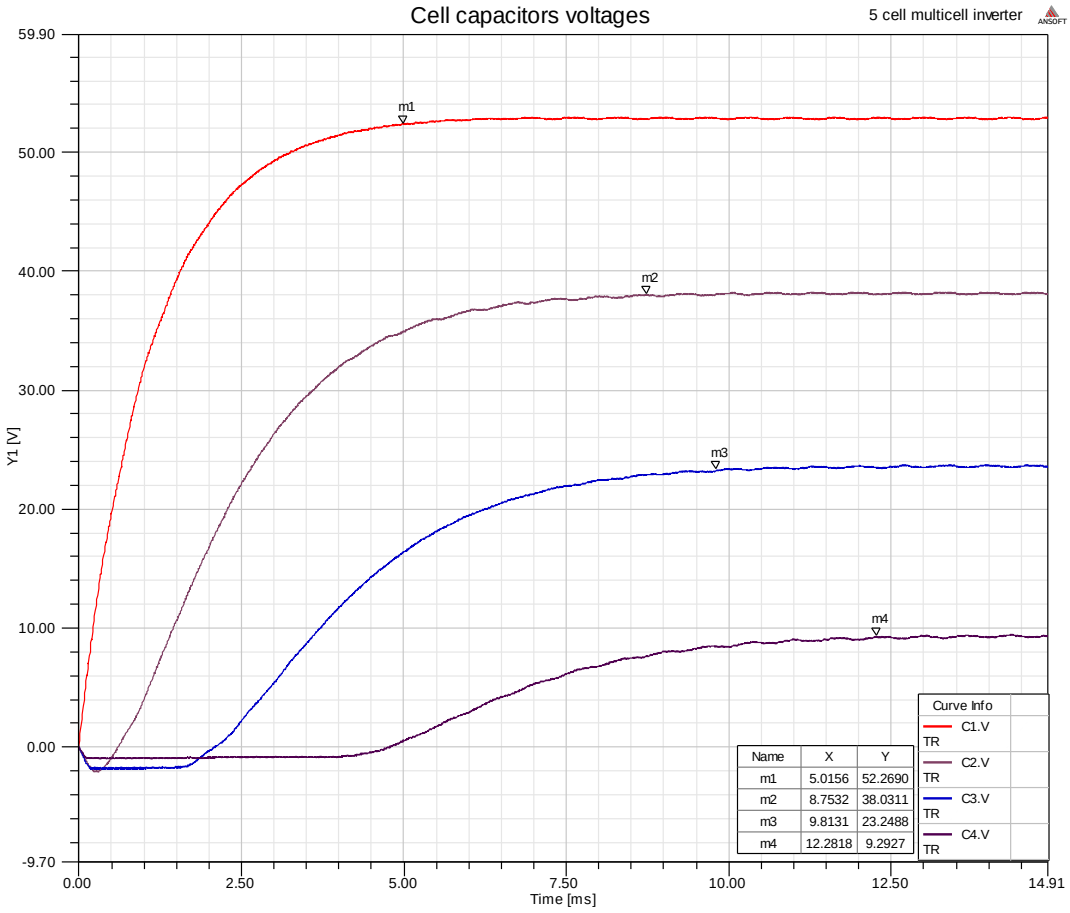

Figure 6.13: Simulation with Simplorer showing the charging times of the four cell capacitors.

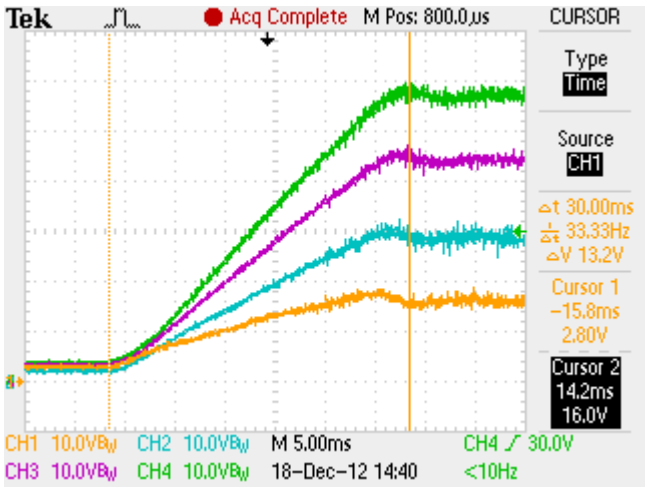

Figure 6.14: Oscilloscope trace of the charging curves of the cell capacitors of a five cell multicell inverter.

Figure 6.15 shows the output voltage (waveform in yellow) obtained from the differential probe connected directly across the multicell inverter and the input voltage (waveform in blue) obtained from the differential probe connected directly across the piezoelectric transducer. One can observe a great reduction in noise with the conclusion that the conductors also perform a filtering function of the noise presented to the load.

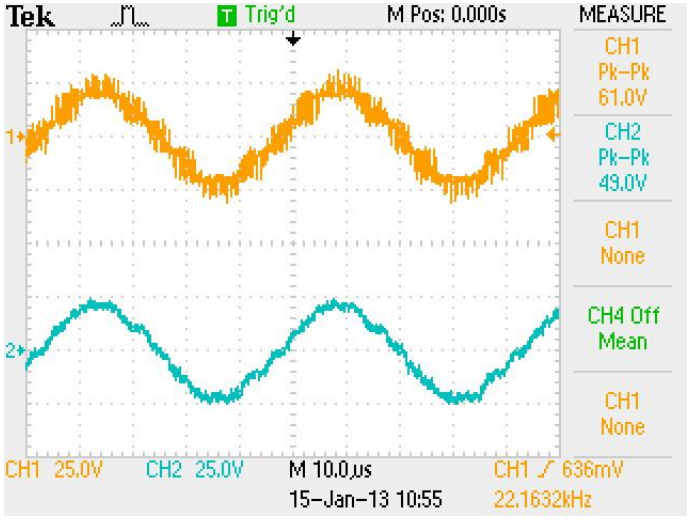

Figure 6.15: Oscilloscope trace of the voltage measured directly across the output of the multicell inverter and directly across the piezoelectric transducer with two differential probes.

6.4.3 Experimental setup with series inductor compensation network

The experimental setup in Figure 6.16 was used to obtain the required experimental result. The series inductor was connected between the PM100 analyser and the Tektronix scope. The frequency was increased from *10kHz* to *30kHz* to plot a current curve representing the response of the transducer with the series inductor. This experiment was also simulated using PSpice, and the simulation model can be seen in Figure 12.2.

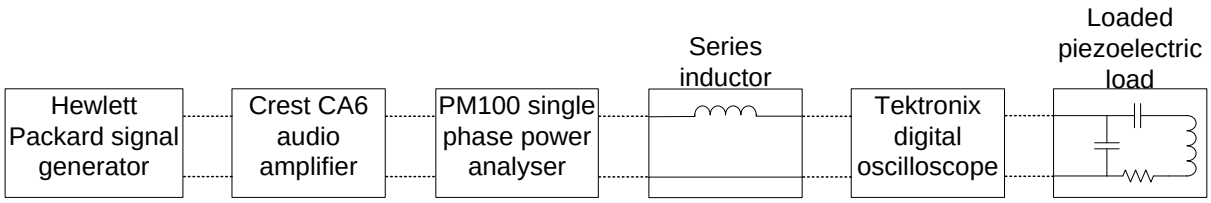

Figure 6.16: Experimental setup with audio amplifier, piezoelectric load and series inductor compensation network.

The experiment was performed again with the multicell inverter as seen in Figure 6.17. The voltage of the Delta main power supply was set to *68V* as this would result in an output power in the region of *10W*.

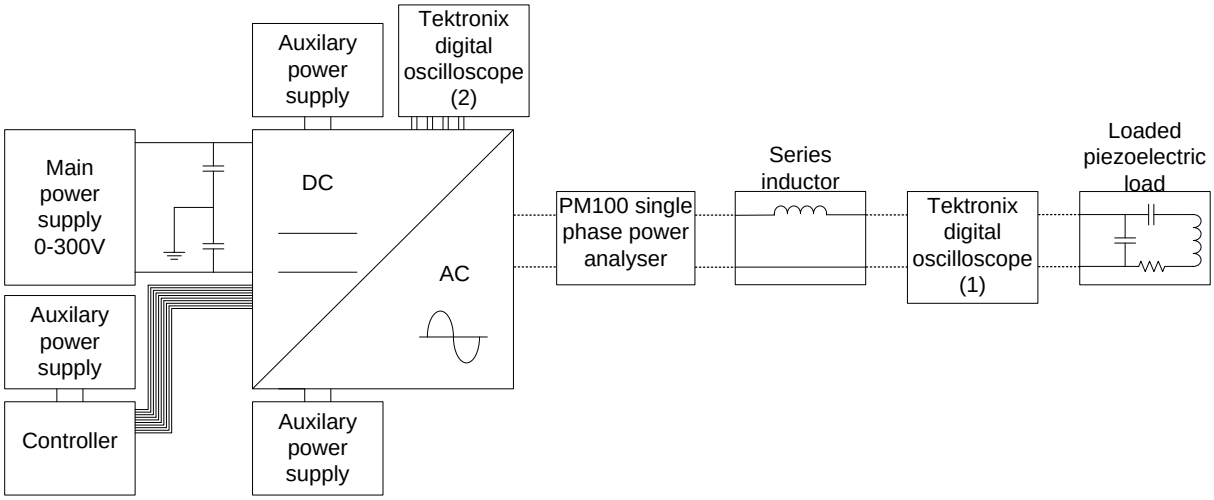

Figure 6.17: Experimental setup with a multicell inverter, piezoelectric load and series inductor compensation network.

6.4.4 Experimental results with series inductor compensation network

The current plot of the PSpice simulation and the current plot of the experiment with the audio amplifier can be seen in Figure 6.18. The theory on compensation networks with a series inductor in section 4.3 states that the value of the inductor must be determined at the anti-resonant frequency of the piezoelectric load which is *23,944kHz*, and that the network will resonate at that frequency. The PSpice simulation shows a peak at *17kHz* and another peak at *27kHz*. The anti-resonant frequency was higher than the resonant frequency of the transducer and therefore it is assumed that the peak at *27kHz* represents the new thickness resonant mode and that the peak situated at *17kHz* represents the new radial resonant mode. The experimental results showed similar results except that the first peak was situated at *18kHz* and the second peak was situated at *26kHz*.

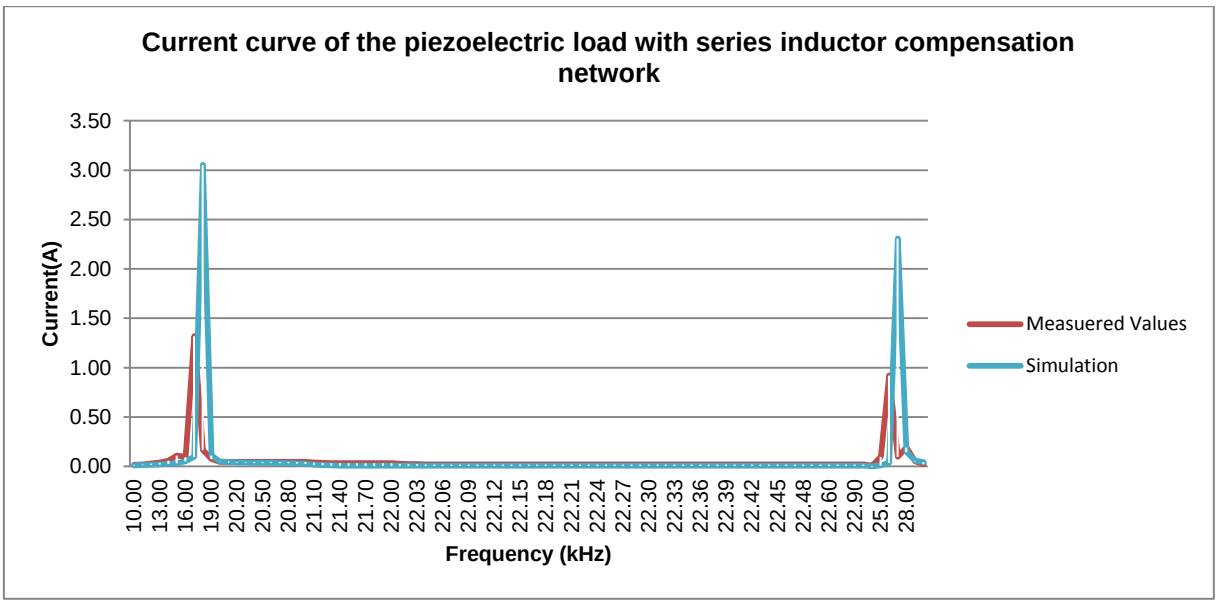

Figure 6.18: Experimental and simulated results of a current plot of the piezoelectric load and simulation model with a series inductor compensation network.

The result for the PCPICE simulation shows a *P.F.* of *0.99*, which is close to the *P.F.* of the audio amplifier of *0.97*. The frequency of the multicell inverter was fixed at *22.163kHz* and therefore the piezoelectric load could not be exited correctly and resulted in a *P.F.* of *0.31.*

Table 6-3: Table with simulated and experimental results of piezoelectric load with series inductor compensation network.

	Pin(S) PM100	Pout(S) scope	Efficiency of network (%)	V_{THD} (%)	I_{THD} (%)	Pout (W)	P.F.	Rise time of cell capacitors
PSpice simulation	*10.71*	*10.4*	*97*			*10.31*	*0.99*	
Crest amplifier	*11.16*	*10.26*	*92*	*0.6*	*0.2*	*10.26*	*0.97*	
Multicell inverter	*0.9*			*11.9*	*1.3*	*0.0284*	*0.31*	*222ms*

The output power after the inductor could not be measured as this point is in the centre of a series resonant circuit. The PSpice simulation resulted in a value of *1600V* and a current of *2.31A* after the inductor. The experiment with the audio amplifier had the same problem that the voltage after the inductor was too high and was stopped when a voltage value of *350V* was reached. A different approach was used by making use of a program called Magnetic Designer to determine the power losses in the inductor which resulted in a value of *0.3W*. This value was then used with the simulation of PSpice, and the efficiency of the compensation network was calculated to be 97%. The power losses of the inductor were then calculated by consideration of only the losses associated to the copper losses of the conductor, and this resulted in a value of *0.57W*. This value was used with the experiment with the audio amplifier and resulted in an efficiency value of *95%*. It was observed that the series inductor managed to block the total harmonics distortion of the current produced by the

load. The load produced a total harmonic distortion value of *12.5%* with the no compensation experiment, and this number was reduced to *0.2%* with the audio amplifier and *1.3%* with the multicell inverter.

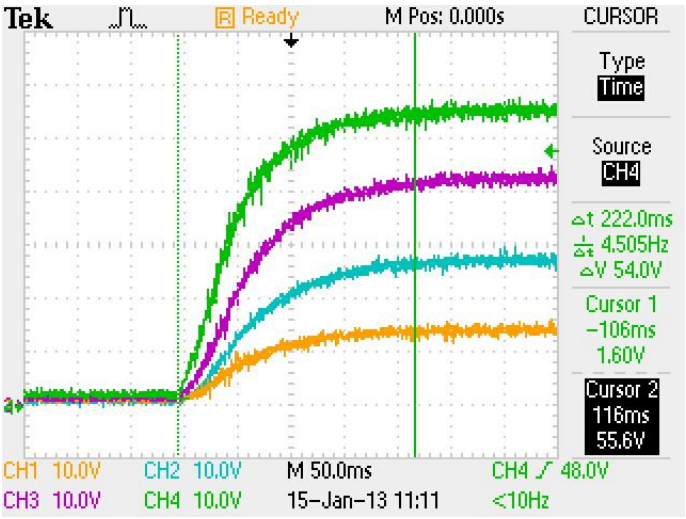

Figure 6.19: Oscilloscope trace of the charging curves of the cell capacitors of a five cell multicell inverter.

The cell capacitors took *222ms* to reach their natural points with voltages of *56.9V, 44.6V, 28.6V* and *15.6V*. This can be seen in Figure 6.19. The expected values were *54.4V, 40.8V, 27.2V* and *13.6V* with a *68V* supply voltage.

6.4.5 Experimental setup parallel inductor compensation network

A simulation model was created as in Figure 12.3 and a current plot was produced to obtain the response of the load with a parallel inductor. The parallel inductor was connected between the PM100 analyser and the Tektronix oscilloscope as shown in Figure 6.20. The frequency was incremented from *10kHz* to *30 kHz* and the current and voltage values was documented. The V_{THD}, I_{THD} and real power were also recorded at the point of resonance.

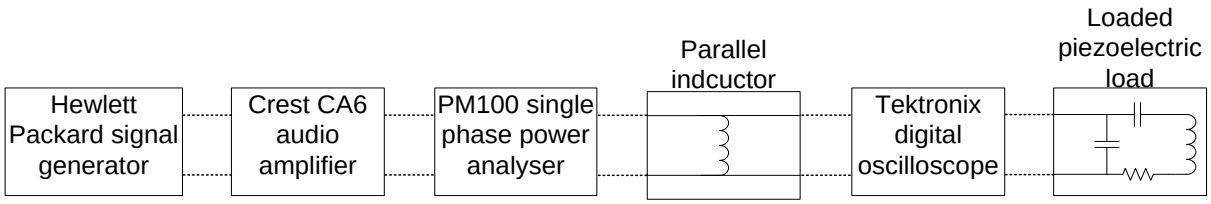

Figure 6.20: Experimental setup with audio amplifier, piezoelectric load and parallel inductor compensation network.

The Agilent signal generator and audio amplifier were replaced (as shown in Figure 6.21) with the multicell inverter and the test was repeated at a frequency of *22.163kHz*. A second Tektronix oscilloscope was connected across the four cell capacitors with differential probes in order to measure the charging time and voltages across these capacitors. The voltage of the Delta main power supply was set to *68V* as this would result in an output power in the region of *10W*. The V_{THD}, I_{THD} and real power were recorded at this frequency.

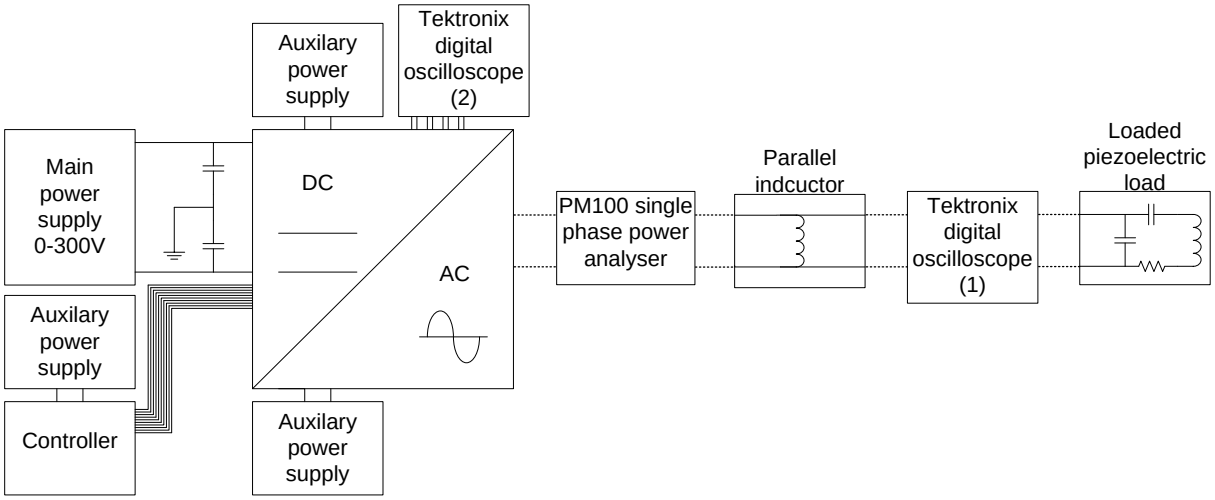

Figure 6.21: Experimental setup of multicell inverter, piezoelectric load and parallel inductor compensation network.

6.4.6 Experimental results with parallel inductor compensation network

Figure 6.22 shows a comparison of the simulated and experimental results obtained of the current curves. This shows that the transducer with the parallel inductor compensation network has a simulated resonant point at *22.052kHz* and has a measured current peak at *22.150kHz*. This small variation in the resonant points is most probably due to the inconsistent load condition to the piezoelectric transducer. This slight deviation will have the result that the multicell inverter will not be able to drive the piezoelectric load effectively at *22.163kHz*, and would explain the lower P.F. value of 0.93 in Table 6-4.

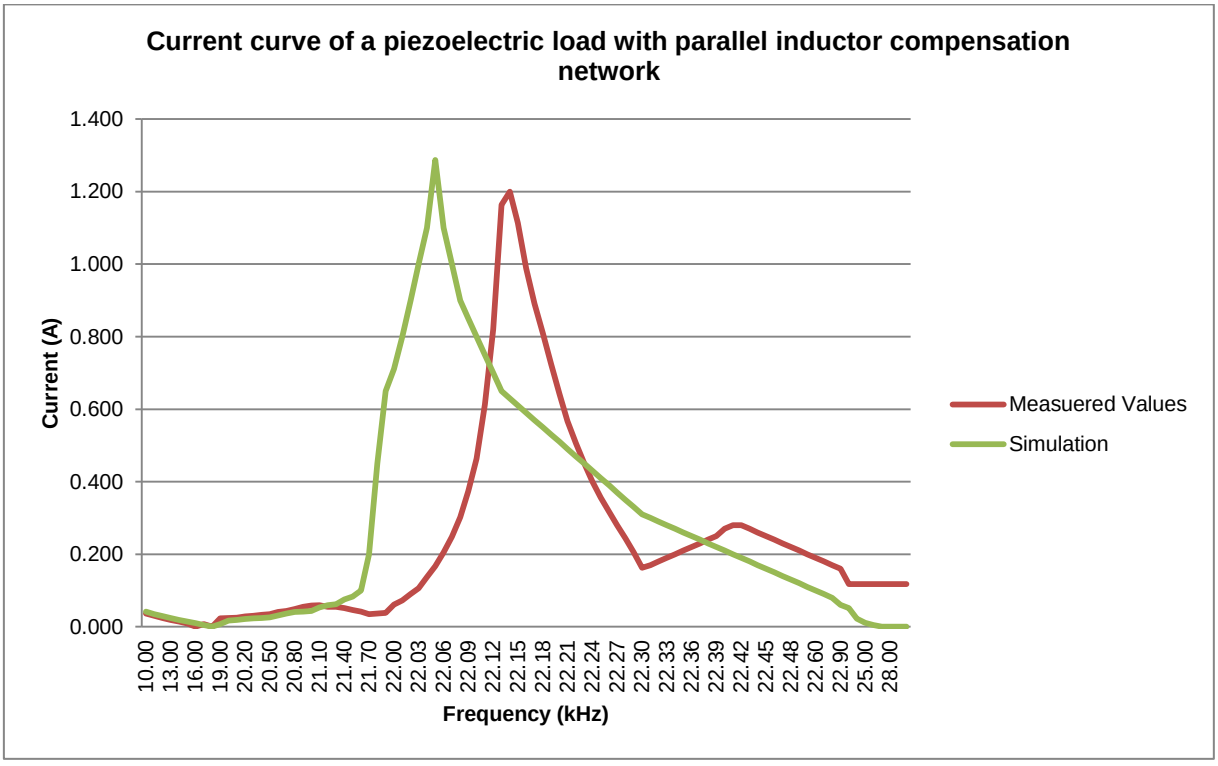

Figure 6.22: Experimental and simulated results of a current plot of the piezoelectric load, with parallel inductor compensation network, and simulation model.

The summarised results in Table 6-4 shows that the results obtained from the PSpice simulation and the experimental results correlate in terms of V_{THD}, I_{THD} and *P.F*. The total harmonic distortion values show that the parallel inductor compensation network only "cancels" the reactive component of the transducer and does not reduce the harmonic content of the voltage or current. This is also evident in the voltage and current capture in Figure 6.23 from the Tektronix oscilloscope.

Table 6-4: Table with simulated and experimental results of piezoelectric load with parallel inductor compensation network.

	Pin(S) PM100	Pout(S) scope	Efficiency of network (%)	V_{THD} (%)	I_{THD} (%)	Pout (W)	P.F.	Rise time of cell capacitors
PSpice simulation	*13.93*	*13.24*	*95*			*12.87*	*0.97*	
Crest amplifier	*11.61*	*10.9*	*94*	*0.3*	*11.6*	*10.6*	*0.97*	
Multicell inverter	*12.5*	*11.8*	*94*	*11.2*	*10.2*	*10.9*	*0.93*	*30ms*

The efficiency was calculated by *d*ivision of the value of the power after the compensation network by the value of the power before the compensation network. The efficiency of the compensation network was simulated to be *95%* and the experimental result produced a value of *94%*. The reason for the small peaks at the leading and lagging edges of the sinusoidal voltage signal (CH1) is unknown and still under investigation.

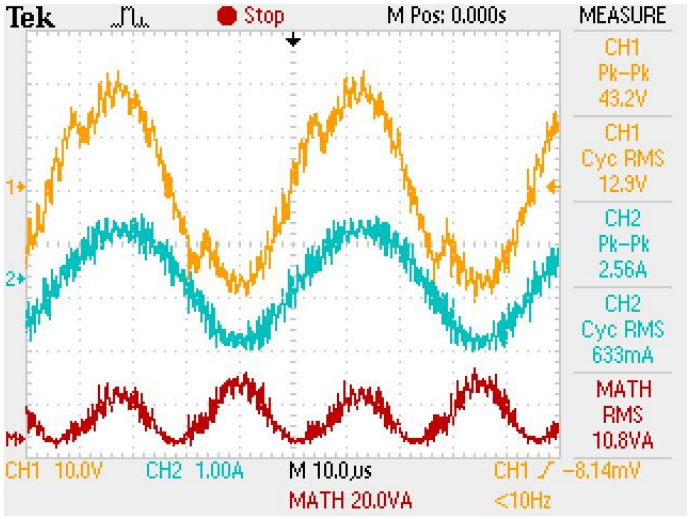

Figure 6.23: Capture of the output voltage, current and power of the multicell inverter which was connected to a parallel inductor compensation network and piezoelectric load.

The charging time of the cell capacitors can be seen in Figure 6.24 and they took *30ms* to charge to their natural values of *56.5V, 43.6V, 28.5V* and *15.9V*. The expected values were *54.4V, 40.8V, 27.2V* and *13.6V* with a *68V* supply voltage.

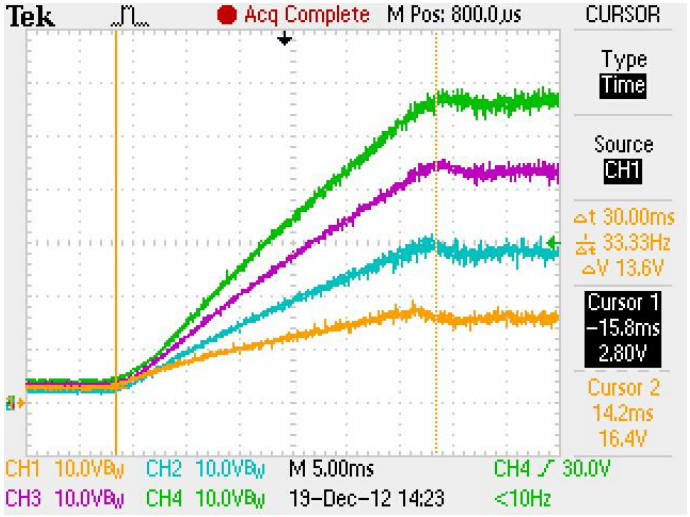

Figure 6.24: Oscilloscope trace of the charging curves of the cell capacitors of a five cell multicell inverter.

6.4.7 Experimental setup with Q-matching as compensation network.

The Q-matching compensation network was connected between the PM100 analyser and the Tektronix oscilloscope. The Q-matching compensation network comprises a series resonant circuit and a capacitor placed across the transducer. The frequency of the signal generator was increased from *10kHz* to *30kHz* and the voltage and current measurements were recorded. At the resonant point the V_{THD}, I_{THD} and real power were recorded. The experimental setup can be seen in Figure 6.25. The PSpice simulation used to simulate this compensation network can be seen in Figure 12.4.

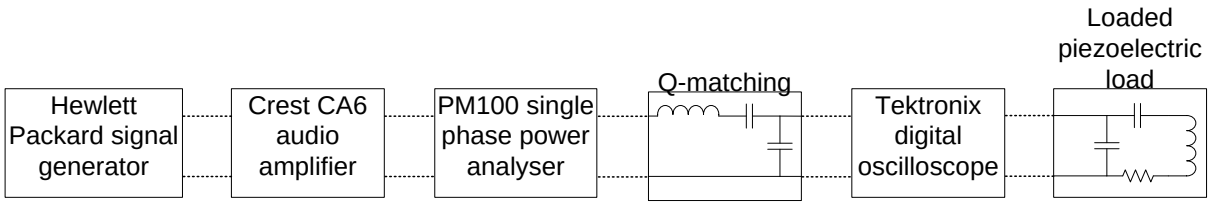

Figure 6.25: Experimental setup with audio amplifier, piezoelectric load and Q-matching as compensation network.

The audio amplifier and signal generator were removed and replaced by the multicell inverter. A second Tektronix oscilloscope was connected across the four cell capacitors with differential probes in order to measure the charging time and voltages across these capacitors. The voltage of the Delta main power supply was set to *30V* as this would result in an output power in the region of *10W*. The lowered supply voltage is due to the fact that Q-matching also incorporates impedance matching. The experiment was repeated at the fixed frequency of *22.163kHz*. The V_{THD}, I_{THD} and real power were recorded at this frequency.

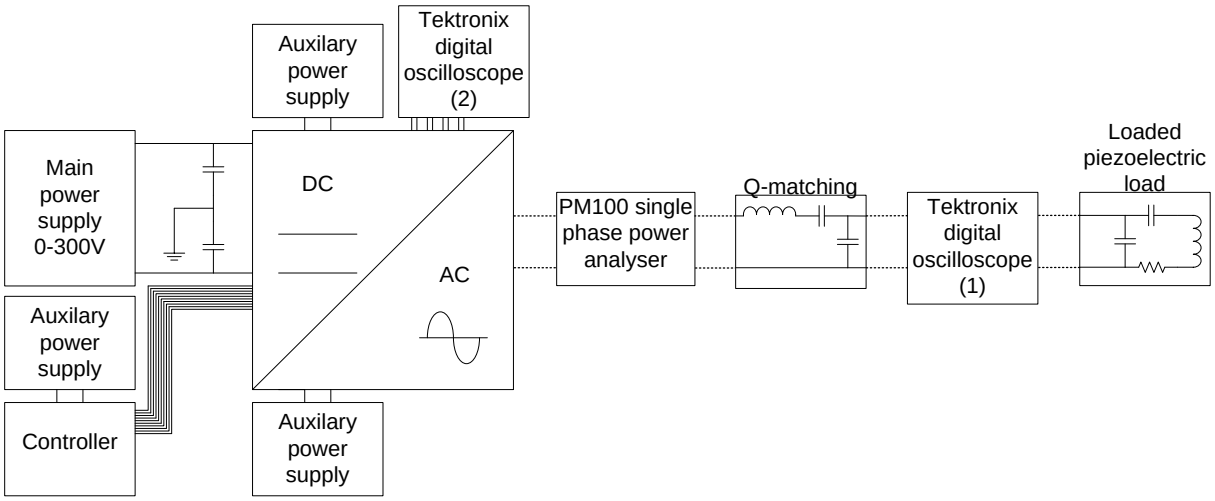

Figure 6.26: Experimental setup of multicell inverter, piezoelectric load and Q-matching as compensation network.

6.4.8 Experimental results with Q-matching as compensation network.

The simulated and measured current plot of the piezoelectric model and load can be seen in Figure 6.27. The model has a peak current flow of *1.145A* at *22,06kHz* and the transducer has a peak current flow of *1.13A* at *22,160kHz*. The smaller peak of the measured values situated at *21.9kHz* shows the radial resonant point of the piezoelectric load.

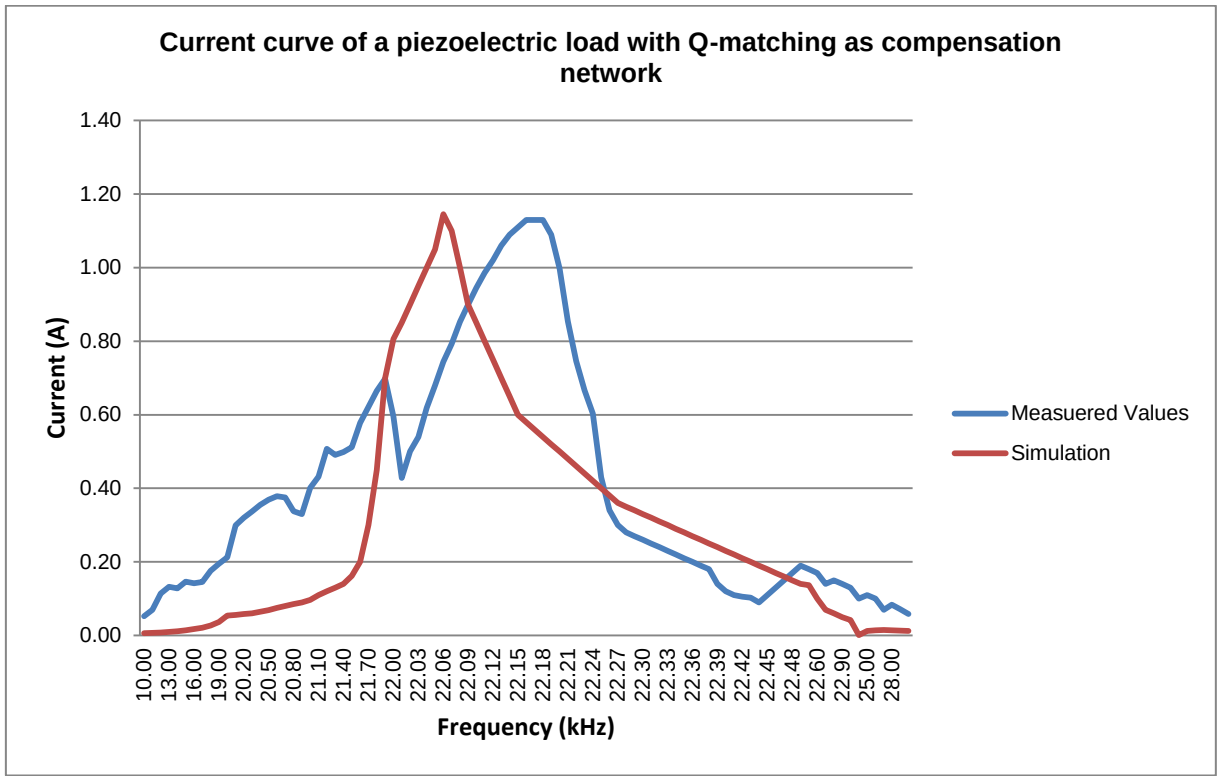

Figure 6.27: Experimental and simulated results of a current plot of the piezoelectric load and simulation model.

One of the advantages of Q-matching is that it reduces the impedance of the piezoelectric load to that of the source without introducing an impedance matching transformer. This advantage means that the

magnetic components can be reduced by just having an inductor instead of an impedance matching transformer and an inductor. This comes at a cost, namely that the compensation network is less efficient in comparison to the parallel inductor which had an efficiency of *94%* compared to that of *87%* of the Q-Matching network. The Q-matching compensation networks achieve a good P.F. of *0.98* with the experiment with the audio amplifier. Results of the experiment with the multicell inverter produced a slightly less desirable P.F. of 0.94. This might be due to the fact that the multicell inverter did not excite the piezoelectric load at the right frequency as this transducer has a high Q value. The compensation network also managed to reduce the total harmonic distortion produced by the multicell inverter and this is evident in Figure 6.29 and with the V_{THD} measurement of *0.75%.*

Table 6-5: Table with simulated and experimental results of piezoelectric load with Q-matching as compensation network.

	Pin (S) PM100	Pout (S) scope	Efficiency of network (%)	V_{THD} (%)	I_{THD} (%)	Pout (W)	P.F.	Rise time of cell capacitors
PSpice simulation	*12.3*	*10.96*	*89*			*10.86*	*0.99*	
Crest amplifier	*12.03*	*10.51*	*87*	*0.5*	*14.5*	*10.3*	*0.98*	
Multicell inverter	*13.5*	*11.4*	*85*	*0.75*	*14.6*	*10.7*	*0.94*	*18.2ms*

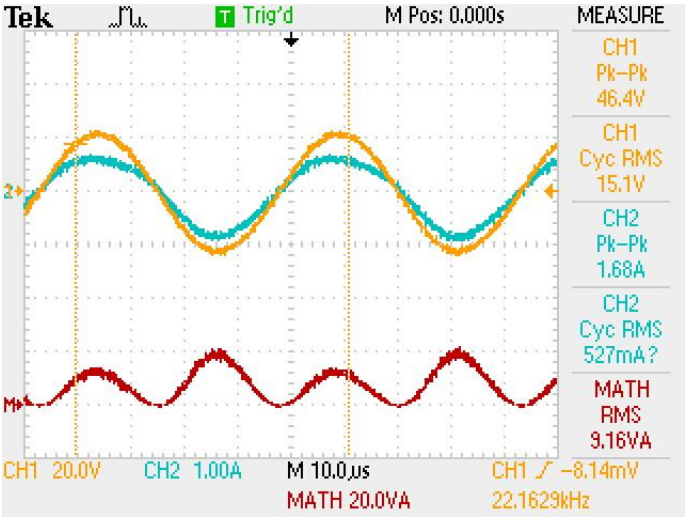

Figure 6.28: Capture of an oscilloscope of the output voltage, current and power of the multicell inverter which was connected to the piezoelectric load with Q-matching as compensation network.

The charging time of the cell capacitors can be seen in Figure 6.29, and they took *18.2ms* to charge to their natural values of *24.2V, 20.4V, 13V* and *9.49V*. The expected values were *24, 18V, 12V* and *6V* with a *30V* supply voltage. The increase of noise on the cell voltages are a combination of EMI and the increase of current flow between the cells, to achieve their natural voltage values, as the load impedance applied to the multicell inverter was in the region of *1.64Ω*.

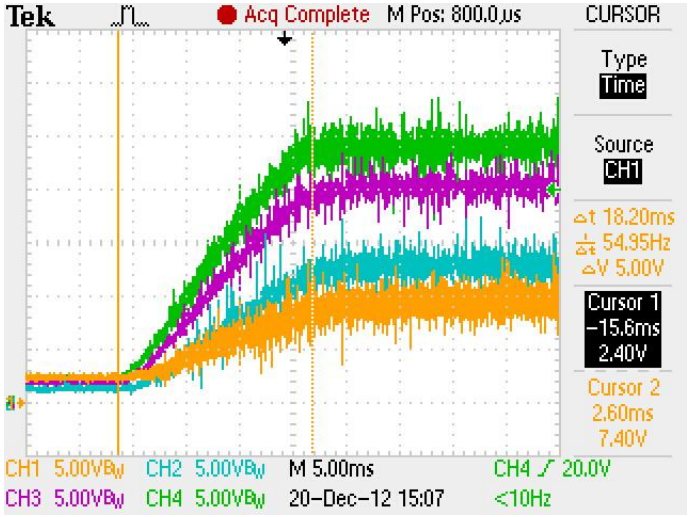

Figure 6.29: Oscilloscope trace of the charging curves of the cell capacitors of a five cell multicell inverter.

6.5 Sonics Vibra cell

An industry standard ultrasonic amplifier, Sonics Vibra cell model VCX 750, with its matched transducer was obtained in order to obtain measurements of the output voltage and current to compare it with the five cell multicell inverter as in the experiment in section 6.4.2. The Sonics Vibra cell amplifier utilises a full-bridge switch mode topology with their own PWM scheme. The output is then filtered with a low-pass filter and is then used to drive the transducer and has a maximum output power of *750W*. The Sonics Vibra cell works at a frequency of *20kHz* and has the ability to track the resonant frequency of the load as it changes under different conditions.

As this is a commercially available product, the load directly connects to the Vibra cell. The enclosure of the transducer had to be opened to gain access to the measuring points. Measurements of the voltage, current and power were obtained at the transducer and an oscilloscope trace of these measurements can be seen in Figure 6.30. The V_{THD}, I_{THD} and *P.F.* was also measured with the PM100 analyser and $V_{THD} = 11.5\%$, $I_{THD} = 23.31\%$ and $P.F. = 0.728$.

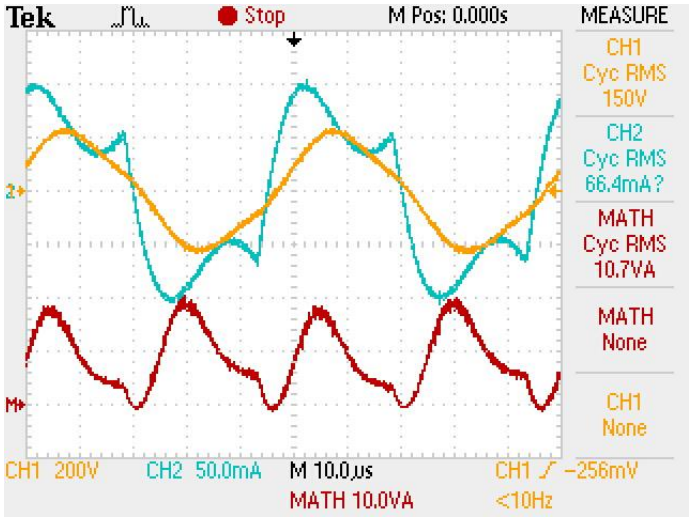

Figure 6.30: The voltage, current and power measurements obtained from a Sonics Vibra cell VCX750 ultrasonic amplifier and its matched transducer.

The multicell inverter produced a V_{THD} of *11.3%,* I_{THD} of *10.1%* and *P.F.* of *0.75.* Comparing the results of the two experiments it is found that the total harmonic distortion of the voltage signal and the P.F. are similar between the two systems. It is also noticeable that when Figure 6.30 is compared with Figure 6.12, the multicell inverter produces a purer sinusoidal shaped current output signal than that of the Sonics Vibra cell. This is also evident when the total harmonic distortion values of the output current signals are compared.

6.6 Summary

In this chapter it was shown that the bootstrap power supply and the five cell multicell inverter worked and performed as designed. The piezoelectric load was excited by the multicell inverter without any filtering of the output signal from the multicell inverter, and worked correctly, without damage to the transducer.

The three compensation networks, namely series inductor, parallel inductor and Q-matching, were evaluated and results were obtained. It was found that all three achieved reasonably with P.F. values ranging between 0.97 and 0.99. The series inductor compensation network was able to reduce the total harmonic distortion produced by the load, and the Q-matching compensation network was able to reduce the total harmonic distortion created by the multicell inverter.

The cell capacitors stayed fairly naturally balanced without external help. The cell capacitors did however deviate slightly from the expected theoretical values but did not hamper the performance of the multicell inverter. Table 14-2 summarises the cell voltages obtained from the simulation, measurements and expected cell voltages.

CHAPTER SEVEN

Conclusion

7.1 Multicell Inverter with Bootstrap power supplies

The Multicell inverter was identified as a candidate to drive a piezoelectric load as the first harmonic is situated at the product of the switching frequency and the number of cells. This would help as the multi cell inverter could be used to excite only the mechanical resonant frequency of the piezoelectric transducer. Chapter three was introduced by a background study of multilevel inverter and thereafter multicell inverters were discussed.

A five cell, six level, multicell inverter was constructed using DirectFETs as switching devices. Positive and negative bootstrap power supplies were also incorporated to supply energy to the five top and five bottom switches of the five cells. A controller, developed by another M-Tech student, was connected via optical links to the gate drive circuit of the switches. The Multicell inverter was tested to produce a current of *10.1A* and an output voltage of more than *80V* verifying the operation of the multicell inverter and the bootstrap power supplies. It was also shown that the first harmonic is situated at the product of the switching frequency and the number of cells.

7.2 Compensation Networks

Chapter two discusses the piezoelectric material and how it can be used as a transducer. The different resonate modes of the piezoelectric transducers was looked at and how piezoelectric transducers can be modelled. A model was developed using Butterworth-Van Dyke's theory to facilitate in simulating the different compensation networks with PSpice and Simplorer.

Three different types of compensation networks where researched and are reported on in chapter four. The piezoelectric transducer is a load that reacted in a dynamic way by changing its Q-factor, resonant frequency and impedance as the load and the power intensity to the piezoelectric transducer is changed.

The series inductor compensation network and the Q-Matching compensation network produced the highest simulated *P.F.* with a result of *0.99*. Experimentally the Q-Matching compensation network performed the best with a *P.F.* value of *0.98*; however, this came at a cost of only having an efficiency of *87%*. The *P.F.* value was high as the output apparent power after the compensation network was used to determine the *P.F.* It was important to differentiate between losses due to the compensation network and a lack of energy transfer due to the compensation network not "cancelling' the reactive component of the load effectively. The series inductor compensation network had an efficiency of *95%* which is one percent higher than the parallel inductor compensation network. It must be remembered that this efficiency was achieved in a theoretical manner. These two compensation networks obtained the same *P.F.* value of *0.97*. The series inductor compensation network produced a very high voltage across the transducer due to series resonance and resonated at the anti-resonant

frequency of the transducer. The parallel inductor compensation network was simple to implement and produced similar result as the series inductor compensation network and therefore this would be the first choice.

The harmonic content of the applied signal to the piezoelectric transducer can stimulate different resonant modes of the piezoelectric transducer. It is important to only stimulate the mechanical resonant frequency of the transducer. This makes it important to make sure that the applied signal does not have any harmonic peaks close to the other resonant modes of the piezoelectric load. The multicell inverter only produces its first harmonic at the apparent frequency of the multicell inverter which is at the product of the switching frequency and the number of cells. In this research the first harmonic was situated at *1.5MHz*. The Q-Matching compensation network was the only network that reduced the total harmonic distortion of *11.3%* that was produced by the multicell inverter to *0.75%*. The other compensation networks only "cancelled" the reactive component of the load. The series inductor compensation network managed to reduce the total harmonic distortion produced by the load from *12%* to *0.2%*. The piezoelectric load did not perform differently as a result of the total harmonic distortion produced by the multicell inverter. Although the Q-matching compensation network reduced the total harmonic distortion produced by the multicell inverter, this should not be a deciding factor when a multicell inverter is used to drive a piezoelectric load while the correct switching technique is used to control the multicell inverter. The apparent frequency of the multicell inverter is much higher than the frequency of the other resonant modes of the transducer. Appendix F
Summary of test results
Table 14-11, summarises the results.

7.3 Natural Balancing of the Cell Capacitors of the Multicell Inverter

The piezoelectric transducer is a dynamic load to any source and it is important that the multicell inverter's cell capacitors stay naturally balanced. The natural cell balancing conditions are discussed in section 3.5.2. The multicell inverter was simulated with Simplorer using a model of a piezoelectric transducer in order to correlate the results with the practical experiments.

Table 14-2, in Appendix F, summarises the voltage measurements obtained of the cell capacitors of the multicell inverter while driving the piezoelectric load with and without compensation networks. This table also correlates the measured cell capacitor voltages with the simulated and calculated cell capacitor voltage values. These values do slightly deviate from the expected values, but Figure 6.13 of the Simplorer simulation and Figure 6.14, Figure 6.24 and Figure 6.29, which shows the cell capacitor voltage values of the different cells over time, show that the cell capacitor voltages stay stable except for the increase of "noise" which represents the flow of current between cells in order to

stay balanced. This looks like noise as the time/division is set very slow in order to capture the charging of the cell capacitors.

7.4 Driving a Piezoelectric Load with a Multicell Inverter

Driving a piezoelectric load with a multicell inverter is possible. The frequency of the first harmonic produced by the multicell is much higher than the frequency of any resonant mode of the piezoelectric transducer. Therefore the transducers were excited only at the frequency of mechanical resonance. The results produced from the experiment where a piezoelectric load was driven with a multicell inverter shows that the *P.F.* value obtained was *0.75*. This indicates that the load had a reactive component but the transducer still produced enough acoustical energy to melt plastic when *10W* real power was produced. It is recommended to implement compensation with a parallel inductor as this improves the efficiency of the system significantly. It was also shown that the conductors used to connect the transducer to the multicell inverter performed some form of filtering as there was a great reduction of noise between the signal from the multicell inverter and the signal applied to the piezoelectric load.

Therefore combining the correct parallel inductor with a piezoelectric transducer as a unity, driving it with a multicell inverter which is designed to produce a range of frequencies by changing the reference frequency which would correspond to the frequency of the mechanical resonance of the transducer, will result in a product which could be used to drive a range of different transducer units with a single ultrasonic amplifier.

The multicell inverter was compared with an industrial standard ultrasonic amplifier, and in certain aspects the results were similar and in other aspects the multicell inverter outperformed the commercially obtained product.

7.5 Thesis Contributions

The main contributions of this thesis are:

A five cell multicell inverter using DirectFET's as switching devices was designed and constructed. This multicell inverter incorporated two bootstrap power supplies to supply energy to the switching drivers and optical interfaces. The inverter had a switching frequency of *300kHz*, an output signal with a frequency of *22.163kHz*, an output current of *10A* and an output voltage of *100V*.

Three compensation networks were designed and constructed. These compensation networks were compared with reference to efficiency and the ability to transfer energy. It was found that the series inductor compensation network performed similarly to that of the parallel inductor but the parallel inductor was easier to implement.

The output signal from the multicell inverter does not need to be filtered in order to drive a piezoelectric transducer, as the frequency of the harmonic content falls outside the range of the resonant modes of the piezoelectric load.

A multicell inverter can be used to drive a piezoelectric transducer while the cell capacitors of the multicell inverter stay balanced as defined by the theory.

A multicell inverter can be used to excite a piezoelectric transducer correctly only when the gate signals of the switches are phase shifted as defined by the theory.

7.6 Future Work

Future work should focus on the following:

Develop a controller for the multicell inverter with admittance locking as this will help the multicell inverter to change its reference frequency to stay in sync with the changing mechanical resonant frequency of the transducer.

Incorporate current limiting into the multicell inverter to protect itself from over current situations.

Develop two auxiliary supplies, to supply power to the bootstrap power supplies, which are powered from the main power supply supplying power to the multicell inverter.

Research the range in which the impedance of the piezoelectric transducer changes in order to investigate methods of impedance matching the multicell inverter with the piezoelectric load.

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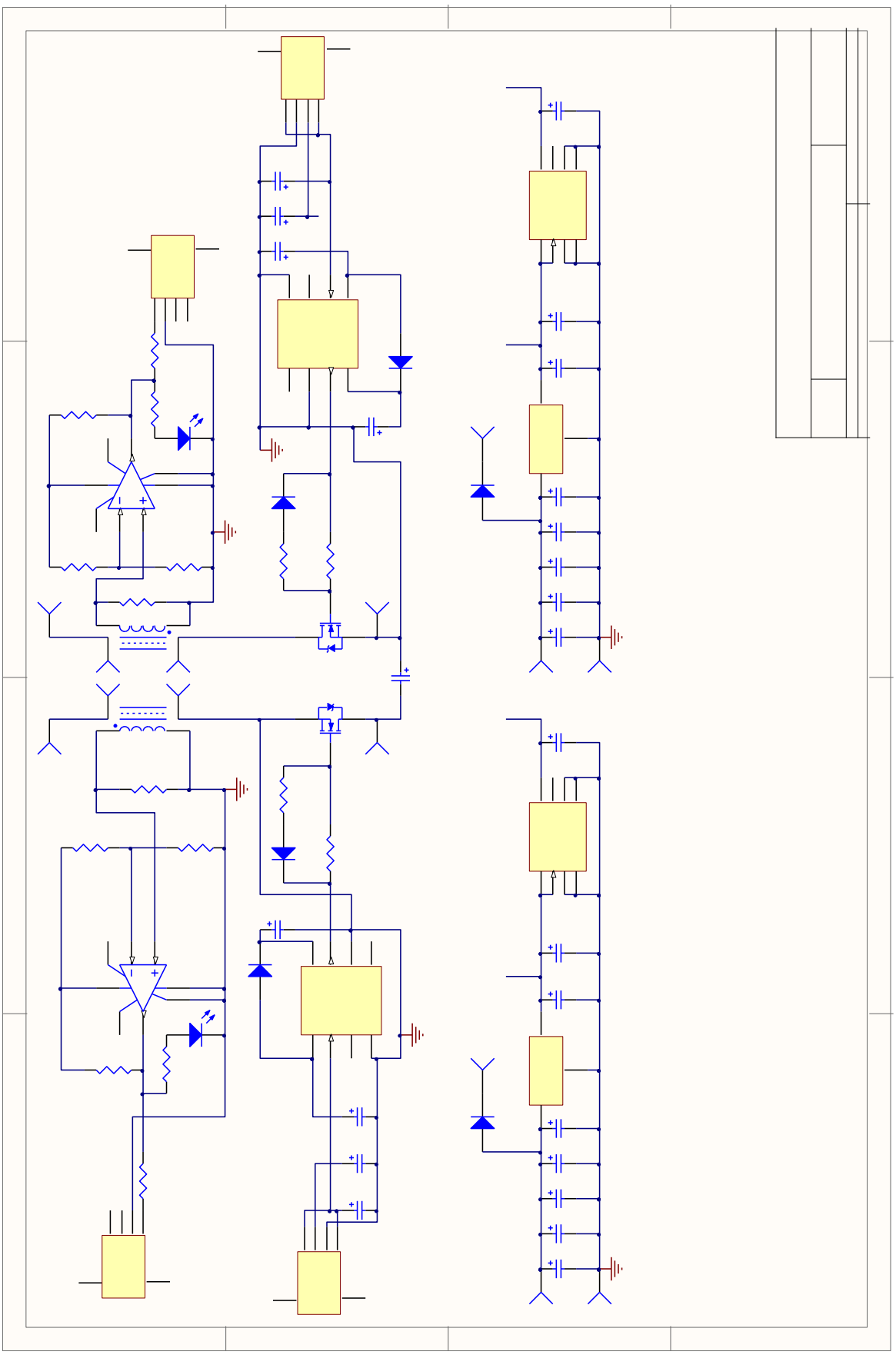
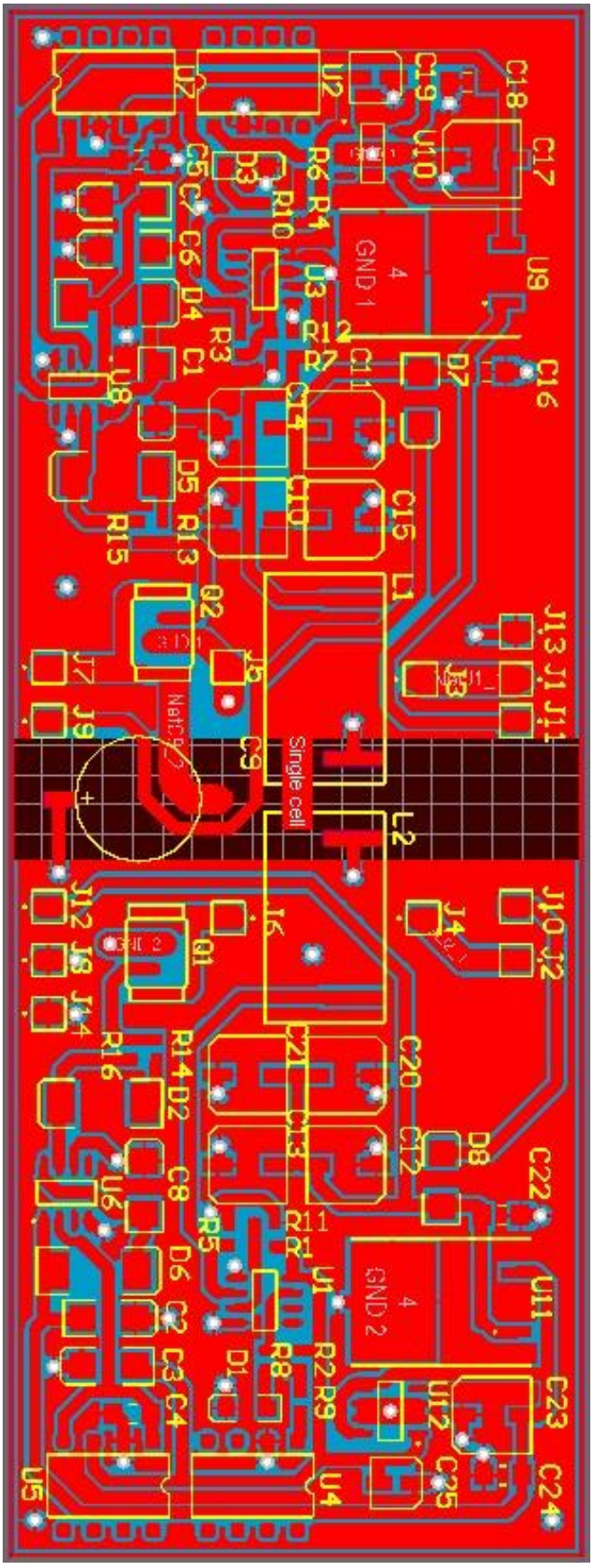
Appendix A

Circuit diagram and PCB artwork




C18
C17
C19
U10
U2
U7
C5
C7
C6
D3
R10
R6
R4
D4
C1
R3
U8
U3
C12
C11
C14
C10
D5
R13
R15
C15
L1
Q2
J5
J7
J9
Net 2
C9
Single cell
L2
J6
J12
J8
J14
Q1
R16
R14
D2
C21
C13
C8
U6
D6
C2
C3
C4
U5
U1
R5
C11
C22
C20
C12
D8
U11
R8
R2
R9
U12
C23
C24
C25
U4
J13
J1
J11
J3
J10
J2
J4
GND 1
GND 2

Appendix B

Matlab Programm

```
%Import the data file called load.txt

%Define contents of the data matrix:

Yloaded=Load(:,1);
PHloaded=Load(:,2);
f=Load(:,3);
Yunloaded=Load(:,4);
PHunloaded=Load(:,5);
w=2*pi;

%Plot Admittance vs frequency

figure(1);
subplot(2,1,1);
plot(f,Yloaded);
hold on
plot(f,Yunloaded,'r');
title('Admittance vs. frequency of the unloaded and loaded transducer')
xlabel('frequency(Hz)')
ylabel('Admittance (Y)')
hold on

%Calculating values for the BVD model for unloaded trancducer

fmunloaded=21954;
fnunloaded=23870;
Ymunloaded=0.17;
Ynunloaded=0.0020561;
Qmun=((w*fmunloaded)/(2*(w*fnunloaded-w*fmunloaded)))*(abs(Ymunloaded)/abs(Ynunloaded));
keffun=sqrt(1-(fmunloaded^2)/(fnunloaded^2));
R1un=1/(abs(Ymunloaded-Ynunloaded));
L1un=(Qmun*R1un)/(w*fmunloaded);
C1un=1/(w*fmunloaded*Qmun*R1un);
Coun=C1un*((1/keffun^2)-1);

%Calculating values for the BVD model for loaded trancducer

fmloaded=22060;
```

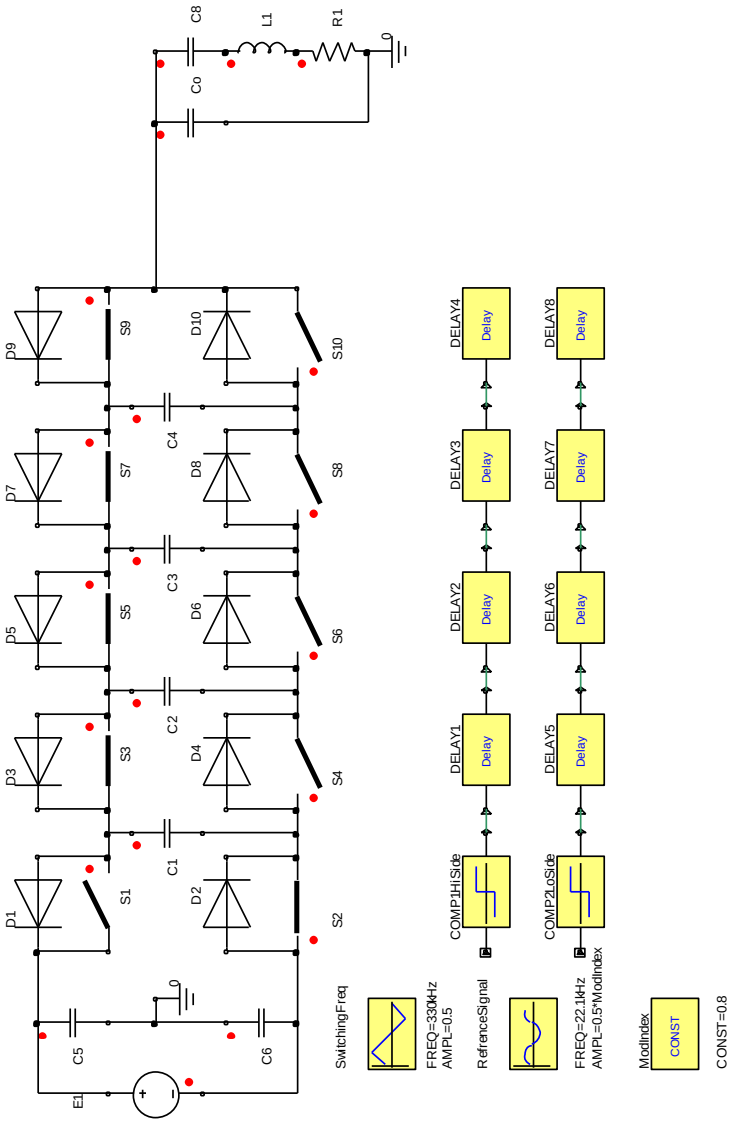
```
fnloaded=23944;
Ymloaded=0.1246;
Ynloaded=0.002062;
Qm=((w*fmloaded)/(2*(w*fnloaded-w*fmloaded)))*(abs(Ymloaded)/abs(Ynloaded));
keff=sqrt(1-(fmloaded^2)/(fnloaded^2));
R1=1/(abs(Ymloaded-Ynloaded));
L1=(Qm*R1)/(w*fmloaded);
C1=1/(w*fmloaded*Qm*R1);
Co=C1*((1/keff^2)-1);

%Display BVD model values for unloaded transducer

disp(['Qm(un)=',num2str(Qmun)])
disp(['keff(un)=',num2str(keffun)])
disp(['R1(un)=',num2str(R1un)])
disp(['L1(un)=',num2str(L1un)])
disp(['C1(un)=',num2str(C1un)])
disp(['Co(un)=',num2str(Coun)])

%Display BVD model values for loaded transducer

disp(['Qm=',num2str(Qm)])
disp(['keff=',num2str(keff)])
disp(['R1=',num2str(R1)])
disp(['L1=',num2str(L1)])
disp(['C1=',num2str(C1)])
disp(['Co=',num2str(Co)])

%Calculate plot values for the loaded and unloaded model

W=2*pi.*f;

%Unloaded Model

Zarmun=R1un+(j.*W.*L1un)-(j./(W.*C1un));
Zoun=-j./(W.*Coun);
Ztotun=(Zarmun.*Zoun)./(Zarmun+Zoun);
Ytotun=1./Ztotun;

%loaded Model

Zarm=R1+(j.*W.*L1)-(j./(W.*C1));
```

```
Zo=-j./(W.*Co);
Ztot=(Zarm.*Zo)./(Zarm+Zo);
Ytot=1./Ztot;

%Plot Measured data with model data

figure(2)
subplot(2,1,1);
plot(f,abs(Ytotun));
hold on
plot(f,abs(Yunloaded),'r');
title('Admittance vs. frequency of the unloaded transducer and the model')
xlabel('frequency(Hz)')
ylabel('Admittance (Y)')
hold on
subplot(2,1,2)
plot(f,abs(Ytot));
hold on
subplot(2,1,2)
plot(f,abs(Yloaded),'r');
title('Admittance vs. frequency of the loaded transducer and the model')
xlabel('frequency(Hz)')
ylabel('Admittance (Y)')
hold on

%Calculating G and B for the unloaded transducer and model

PHradun=PHunloaded.*(pi/180);
Gunloaded=Yunloaded.*cos(PHradun);
Bunloaded=Yunloaded.*sin(PHradun);
Gunloadedsim=real(Ytotun);
Bunloadedsim=imag(Ytotun);

%Calculating G and B for the loaded transducer

PHrad=PHloaded.*(pi/180);
Gloaded=Yloaded.*cos(PHrad);
Bloaded=Yloaded.*sin(PHrad);
Gloadedsim=real(Ytot);
Bloadedsim=imag(Ytot);

%plot circles
```

```
figure(3)
subplot(2,1,1);
plot(Gunloaded,Bunloaded);
hold on
plot(Gunloadedsim,Bunloadedsim,'r');
title('Susceptance vs. Conductance of the unloaded transducer and the model')
xlabel('Conductance(G)')
ylabel('Susceptance(B)')
hold on
subplot(2,1,2);
plot(Gloaded,Bloaded);
hold on
plot(Gloadedsim,Bloadedsim,'r');
title('Susceptance vs. Conductance of the loaded transducer and the model')
xlabel('Conductance(G)')
ylabel('Susceptance(B)')
hold on
```

Appendix C

Antsoft Simplorer Simulation Model



Appendix D

PSpice Simulation Models

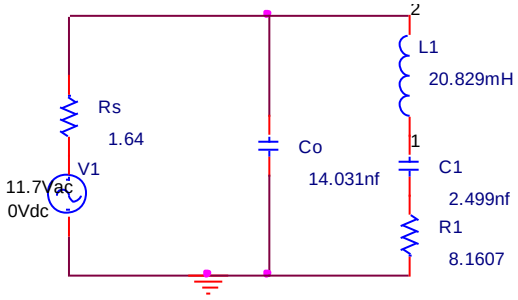


Figure 12.1: PSpice model used to simulate the interaction of a source and a model of a piezoelectric load with no compensation network.

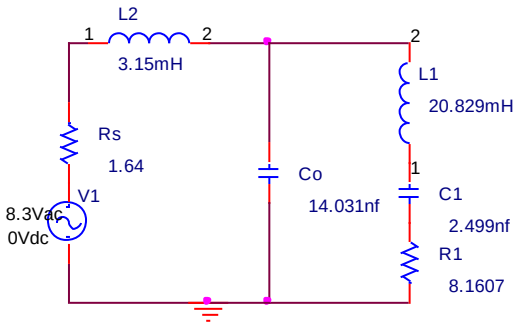


Figure 12.2: PSpice model used to simulate the interaction of the source and a model of a piezoelectric load with a series inductor compensation network.

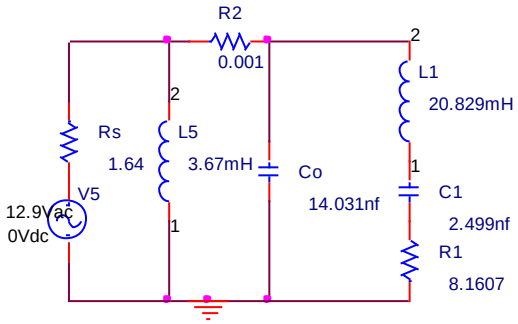


Figure 12.3: PSpice model used to simulate the interaction of the source and a model of a piezoelectric load with a parallel inductor compensation network.

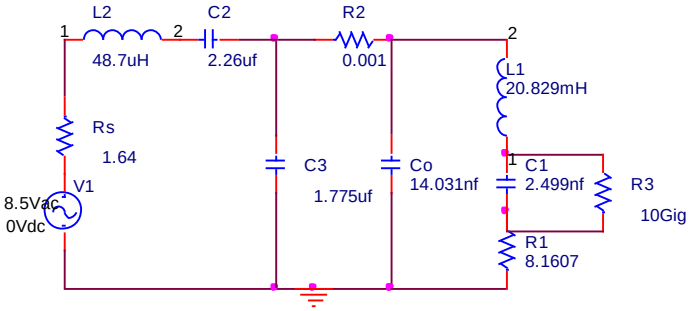


Figure 12.4: PSpice model used to simulate the interaction of the source and a model of a piezoelectric load with Q-Matching as compensation network.

Appendix E

Derivation of the formulae for Q-Matching

Deriving the formula (equation 4.11) to calculate the value of C_2.

$$Y = G + jB$$

$$Y = \frac{1}{R_P} + j\omega C$$

$$Z = \frac{1}{\frac{1}{R_P} + j\omega C} \times \frac{\frac{1}{R_P} - j\omega C}{\frac{1}{R_P} - j\omega C}$$

$$Z = \frac{\frac{1}{R_P} - j\omega C}{\left(\frac{1}{R_P}\right)^2 - j\frac{1}{R_P}\omega C + j\frac{1}{R_P}\omega C + (\omega C)^2}$$

$$Z = \frac{\frac{1}{R_P} - j\omega C}{\left(\frac{1}{R_P}\right)^2 + (\omega C)^2}$$

$$Z = \frac{\frac{1}{R_P}}{\left(\frac{1}{R_P}\right)^2 + (\omega C)^2} - j\frac{\omega C}{\left(\frac{1}{R_P}\right)^2 + (\omega C)^2}$$

R_S is the real part of the impedance

$$R_S = \frac{\frac{1}{R_P}}{\left(\frac{1}{R_P}\right)^2 + (\omega C)^2}$$

$$R_S\left(\frac{1}{R_P}\right)^2 + R_S(\omega C)^2 = \frac{1}{R_P}$$

$$R_S\left(\frac{1}{R_P}\right) + R_S R_P(\omega C)^2 = 1$$

$$R_S + R_S {R_P}^2(\omega C)^2 = R_P$$

$$R_S {R_P}^2(\omega C)^2 = R_P - R_S$$

$$(\omega C)^2 = \frac{R_P - R_S}{R_S {R_P}^2}$$

$$C = \frac{1}{\omega}\sqrt{\frac{R_P - R_S}{R_S {R_P}^2}} = C_2$$

Deriving the formula (equation 4.13) to calculate the value of C_s. The imaginary part of the impedance above would represent the impedance of C_S.

$$C_S = \frac{1}{\omega\left(\frac{\omega C_2}{\left(\frac{1}{R_P}\right)^2 + (\omega C_2)^2}\right)}$$

$$\omega C_S = \frac{1}{\frac{\omega C_2}{\left(\frac{1}{R_P}\right)^2 + (\omega C_2)^2}}$$

$$\omega C_S = \frac{\frac{1}{R_P^2} + (\omega C_2)^2}{\omega C_2}$$

$$\omega C_S = \frac{\frac{1}{R_P^2} + \left(\omega\left(\frac{1}{\omega}\right)\sqrt{\frac{R_P - R_S}{R_P^2 R_S}}\right)^2}{\left(\omega\left(\frac{1}{\omega}\right)\sqrt{\frac{R_P - R_S}{R_P^2 R_S}}\right)}$$

$$\omega C_S = \frac{\frac{1}{R_P^2} + \frac{R_P - R_S}{R_P^2 R_S}}{\left(\sqrt{\frac{R_P - R_S}{R_P^2 R_S}}\right)}$$

$$\omega C_S = \frac{\frac{R_S + R_P - R_S}{R_P^2 R_S}}{\left(\sqrt{\frac{R_P - R_S}{R_P^2 R_S}}\right)}$$

$$\omega C_S = \frac{\frac{R_P}{R_P^2 R_S}}{\left(\sqrt{\frac{R_P - R_S}{R_P^2 R_S}}\right)}$$

$$\omega C_S = \frac{\frac{1}{R_P R_S}}{\left(\sqrt{\frac{R_P - R_S}{R_P^2 R_S}}\right)} \times \frac{\sqrt{\frac{R_P - R_S}{R_P^2 R_S}}}{\sqrt{\frac{R_P - R_S}{R_P^2 R_S}}}$$

$$\omega C_S = \frac{\frac{1}{R_P R_S}\sqrt{\frac{R_P - R_S}{R_P^2 R_S}}}{\frac{R_P - R_S}{R_P^2 R_S}}$$

$$\omega C_S = \frac{1}{R_P R_S}\sqrt{\frac{R_P - R_S}{R_P^2 R_S}}\frac{R_P^2 R_S}{R_P - R_S}$$

$$\omega C_S = \frac{1}{R_P R_S}\frac{\sqrt{R_P - R_S}}{\sqrt{R_P^2 R_S}}\frac{R_P^2 R_S}{R_P - R_S}$$

$$\omega C_S = \frac{\sqrt{R_P - R_S}}{R_P R_S}\frac{\sqrt{R_P^2 R_S}}{R_P - R_S}$$

$$\omega C_S = \frac{1}{R_P R_S}\frac{\sqrt{R_P^2 R_S}}{\sqrt{R_P - R_S}}$$

$$(\omega C_S)^2 = \left(\frac{1}{R_P R_S}\right)^2 \frac{R_P^2 R_S}{R_P - R_S}$$

$$(\omega C_S)^2 = \frac{1}{R_S R_P - R_S^2}$$

$$C_S = \frac{1}{\omega\sqrt{R_S R_P - R_S^2}}$$

Deriving the formula (equation 4.16) to calculate the value of L_s.

At resonance $X_L = X_C$ or $\omega L = \frac{1}{\omega C_T}$

$$\frac{1}{C_T} = \frac{1}{C_S} + \frac{1}{C_2}$$

$$\frac{1}{C_T} = \frac{1}{\frac{1}{\omega\sqrt{R_S R_P - R_S^2}}} + \frac{1}{\frac{1}{\omega}\sqrt{\frac{R_P - R_S}{R_S {R_P}^2}}}$$

$$\frac{1}{C_T} = \omega\sqrt{R_S R_P - R_S^2} + \frac{1}{\frac{1}{\omega}\frac{\sqrt{R_P - R_S}}{\sqrt{R_S {R_P}^2}}}$$

$$\frac{1}{C_T} = \omega\sqrt{R_S}\sqrt{R_P - R_S} + \frac{\omega R_P\sqrt{R_S}}{\sqrt{R_P - R_S}}$$

$$\frac{1}{C_T} = \frac{\omega\sqrt{R_S}(R_P - R_S) + \omega R_P\sqrt{R_S}}{\sqrt{R_P - R_S}}$$

$$\frac{1}{C_T} = \frac{\omega\sqrt{R_S}(R_P - R_S + R_P)}{\sqrt{R_P - R_S}}$$

$$\frac{1}{\omega C_T} = \frac{\sqrt{R_S}(2R_P - R_S)}{\sqrt{R_P - R_S}} = X_L = \omega L_S$$

$$L_S = \frac{\sqrt{R_S}(2R_P - R_S)}{\omega\sqrt{R_P - R_S}}$$

Deriving the formula (equation 4.17) to calculate the value of the Q-factor.

$$Q = \frac{X_{L_S}}{R_S} = \frac{\sqrt{R_S}(2R_P - R_S)}{R_S\sqrt{R_P - R_S}}$$

Appendix F

Summary of test results

Table 14-1: Summary of the measured and simulated results obtained from the experiments performed of the compensation networks.

Crest amp							
Compensation type	**PM100 Pin(S)**	**scope Pout(S)**	**efficiency of network**	**Vthd (%)**	**Ithd(%)**	**Pout(W)**	**P.F.**
No compensation	*11.70*	*11.70*	*100%*	*0.30*	*12.50*	*10.30*	*0.88*
No compensation (PSpice)	*13.95*	*13.95*	*100%*			*11.60*	*0.83*
Series	*10.41*	*10.28*	*95%*	*0.60*	*0.20*	*10*	*0.97*
Series (PSpice)	*10.71*	*10.4*	*97%*			*10.31*	*0.99*
Parallel	*11.61*	*10.90*	*94%*	*0.30*	*11.60*	*10.60*	*0.97*
Parallel (PSpice)	*13.93*	*13.24*	*95%*			*12.87*	*0.97*
Q-matching	*12.03*	*10.51*	*87%*	*0.50*	*14.50*	*10.30*	*0.98*
Q-matching (PSpice)	*12.31*	*10.96*	*89%*			*10.86*	*0.99*
Multicell inverter							
No compensation (multicell inverter)	*13.92*	*13.92*	*100%*	*11.3*	*10.2*	*10.4*	*0.75*
No compensation (Simplorer)	*13.79*	*13.79*	*100%*			*10.8*	*0.78*
Series (multicell inverter)	*0.93*	*0.29*	*31%*	*11.9*	*0.7*	*0.28*	*0.31*
Parallel (multicell inverter)	*12.50*	*11.75*	*94%*	*11.2*	*10.2*	*10.9*	*0.93*
Q-matching (multicell inverter)	*13.46*	*11.44*	*85%*	*0.75*	*14.6*	*10.7*	*0.94*
Sonic Vibra cell model VCX 750							
As supplied from manufacturer				*11.5*	*23.31*		*0.73*

Table 14-2: Summary of the expected and measured cell voltages without and for the three different compensation networks.

	Power supply voltage	Cell1	Cell2	Cell3	Cell4
Expected cell voltages for supply voltage	*68*	*54.4*	*40.8*	*27.2*	*13.6*
No compensation (Multicell inverter)	*68*	*56.7*	*43.8*	*28.6*	*16*
No compensation (Simplorer)	*68*	*52.3*	*38.03*	*23.2*	*9.3*
Series inductor (Multicell inverter)	*68*	*56.9*	*44.6*	*28.6*	*15.6*
Parallel inductor (Multicell inverter)	*68*	*56.5*	*43.6*	*28.5*	*15.9*
Q-matching (Multicell inverter)	*30*	*24.2*	*20.4*	*13*	*9.49*
Expected cell voltages for supply voltage	*30*	*24*	*18*	*12*	*6*