Cape Peninsula University of Technology

IMPLEMENTATION OF AN ADAPTIVE PROTECTION SCHEME FOR A HYBRID MICROGRID SYSTEM WITH DISTRIBUTED GENERATIONS

By

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DECLARATION

I, Hendrik de Graaff Genis, declare that the contents of this thesis represent my own unaided work and that the thesis has not previously been submitted for academic examination towards any qualification. Furthermore, it represents my own opinions and necessarily those of the Cape Peninsula University of Technology.

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ABSTRACT

The global increase in the use of renewable energy sources and distributed generation is due to positive environmental impacts and the need to meet energy demand. The protection scheme for traditional radial power systems with unidirectional power flow are not suitable for bidirectional power flow caused by the addition of DGs. The integration of DGs may lead to a loss of coordination between overcurrent protection relays, which could lead to unnecessary disconnections and reduced reliability. Microgrids can operate in grid-connected or island modes. Fault currents are higher during grid-connected mode operation than during island mode operation. Different protection settings are required for relays depending on the mode of operation.

Modelling and simulation are conducted in DIgSILENT PowerFactory and RSCAD simulation environments. The modified IEEE 14-bus system is used as a case study, with a 50 MW wind farm as the distributed generation. A protection coordination study is completed for SEL-351 protection relays in grid-connected and islanded modes. Hardware-in-the-loop (HIL) testing of directional overcurrent protection is completed using RTDS and SEL-351A relays. IEC 61850 standard-based GOOSE messages between SEL-351 relays are demonstrated in a laboratory-scale test bench.

To address the challenges associated with traditional protection schemes, an adaptive protection scheme is implemented. The adaptive protection algorithm is based on the IEC 61850 GOOSE communication protocol. The adaptive scheme enables real-time monitoring of the network configuration and detects faults in both grid-connected and island modes to ensure MG system reliability.

The project focuses on addressing the challenges associated with the integration of distributed generation into the power grid, particularly in the case of microgrids. The emphasis on adaptive protection and real-time monitoring through advanced communication protocols based on IEC 61850 reflects a forward-looking approach to improving the reliability and efficiency of microgrid systems.

Keywords: Adaptive protection, DIgSILENT PowerFactory, distributed generation, GOOSE, IEC 61850, microgrid, PMSG, renewable energy sources, RTDS, wind turbine generator.

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LIST OF ABBREVIATIONS

BESS	Battery energy storage system
CID	Configured IED description
DER	Distributed energy resources
DFIG	Double-fed induction generator
DG	Distributed generation
EPS	Electric power system
FRT	Fault ride-through
GOOSE	Generic Object-Oriented System Event
GTAO	Gigabit transceiver analogue output card
GTFPI	Gigabit transceiver front panel interface card
GTNET	Gigabit transceiver network card
HIL	Hardware-in-the-loop

HVRT	High-voltage ride-through
IEC	International Electrotechnical Commission
IED	Intelligent electronic device
IEEE	Institute of Electrical and Electronics Engineers
LN	Logical node
LVRT	Low-voltage ride-through
MG	Microgrid
MGCC	Microgrid central controller
MW	Mega-watt
MVA	Mega-volt-ampere
MVAr	Mega volt ampere reactive
PCC	Point of common coupling
PMSG	Permanent magnet synchronous generator
POC	Point of connection
PTRC	Protection trip conditioning
PV	Photo-voltaic
RES	Renewable energy sources
RTDS	Real-time Digital Simulator
SCD	Substation configuration description file
SCL	Substation Configuration Language
SEL	Schweitzer Engineering Laboratories
TMS	Time multiplier setting
VRT	Voltage ride-through
WTG	Wind turbine generator

DEFINITIONS

AcSELerator Architect	Software that is used to configure the IEC 61850 GOOSE messages, controls, and reports for SEL devices.
AcSELerator Quickset	Software tool that can quickly and easily configure, commission, and manage SEL devices for power system protection, control, metering, and monitoring.
DIgSILENT PowerFactory	Power system analysis software package that is used in analyzing generation, transmission, distribution, and industrial systems.
Distributed Generation	Method of generating electricity from multiple renewable energy sources that are close to the load demands.
GOOSE	An IEC 61850 Ethernet control mechanism in which the status and value data are grouped into a data set and transmitted between IEDs.
IED	Any device that is equipped with one or more processors with the capability of receiving or sending data/ controls from or to an external source.
Interoperability	The capability of two or more networks, systems, devices, applications, or components to externally exchange and readily use information securely and effectively.
Overcurrent relay	A protection relay that initiates a trip once the measured current exceeds the pickup value.
Point of common coupling	The point of connection between the area EPS (grid) and the local EPS.
Power system	A network of electrical components that transfers electrical power from the point of generation to the point of consumption.
Protection relay	Electronic device that can detect a fault condition and initiate a trip signal to open a circuit breaker and isolate the faulty part of the installation from the rest of the network.

Protection scheme	The coordinated arrangement for the protection of one or more elements of a power system. A protection scheme may consist of several protection systems.
Ride-through	Ability to withstand voltage or frequency disturbances inside defined limits and to continue operating as specified.
RSCAD	Power system simulation software package that is used for interfacing with the RTDS hardware to perform real-time simulations.
Short-circuit	Electrical circuit with a low resistance that allows a current to flow through an unintended path

CHAPTER 1
INTRODUCTION

1.1 Introduction

Renewable energy sources (RESs) are becoming more significant sources of electrical energy because of the awareness of environmental problems such as increased global warming. Globally, the integration of distributed generation (DG) into the main grid is increasing in modern power systems because of its improved efficiency, dependability, and reduction of greenhouse gas emissions. The integration of DGs into the grid is based on RESs such as solar photovoltaics (PVs), wind turbine generators (WTGs), fuel cells, and battery storage systems (BSSs) (Basak et al., 2012). A microgrid (MG) comprises a collection of DG devices and controllable loads that can operate in either grid-connected or island modes (Gadanayak, 2021). By utilising available smart grid technologies, MGs can coordinate DGs with conventional power grids. Integrating RES, synchronous generators, and loads into MGs represents a significant advancement for smart grids (Murty and Kumar, 2020).

A hybrid MG consists of a combination of different RESs, such as wind, PV, and battery storage systems, that can be integrated into the grid. The combination of wind and PV can improve the overall reliability of the MG because of the intermittent nature of the available wind and solar energy. Additionally, this can reduce the size and cost of the BSS that is needed for the MG (Badwawi, Abusara, and Mallick, 2015).

MGs can operate in both grid-connected and island modes. It is essential that the protection scheme that is developed and implemented can provide protection against all fault types during both operation modes. An adaptive protection scheme is proposed to update the relay settings depending on the MG configuration. A communication-based protection scheme is proposed for isolated MGs. Adaptive protection schemes can be based on either a centralised or decentralised architecture (Hussain and Kim, 2016).

This thesis investigates the development and implementation of an IEC 61850 standard-based adaptive protection scheme based on a decentralised architecture. The implementation of IEC 61850 GOOSE communication between intelligent electronic devices (IEDs) improves the speed and reliability of the protection scheme compared with hardwired connections between the devices. In a decentralised

architecture, each local controller (bay-level IED) communicates with its adjacent local controllers to isolate the fault within its protection zone. The implementation of the adaptive protection scheme is based on the status of the circuit breakers located at the point of common coupling (PCC). The circuit breakers are in the closed position during the grid-connected mode of operation and in the open position during the island mode of operation. The implementation of the MG adaptive protection scheme for the SEL-351A relays is based on a hardwired connection from the 110 V DC auxiliary supply to the opto-isolated inputs, IN101. Finally, an algorithm is developed for the implementation of the MG adaptive protection scheme for the SEL-700G relay based on the IEC 61850 standard-based communication protocol.

This chapter describes the awareness of the research problem, its statement, its aim and objectives, and the research methodology used for the development and implementation of the MG adaptive protection scheme.

1.2 Awareness of the research problem

MGs are capable of functioning in both grid-connected and island modes of operation. The short-circuit current and protection setting requirements are different for the two modes of operation. The configuration of protection IEDs requires a thorough understanding of the two operational modes and manages the transitions that occur between them. The exchange of information between the protection IEDs and the microgrid controller also needs to be considered as part of the microgrid protection design (Vegunta et al., 2021).

Traditional power systems are radial, and the power flow is unidirectional, i.e., from generation to load. The addition of DGs to the network causes the power flow to become bidirectional, and conventional protection schemes cannot be applied. Other factors include the intermitted nature of the DGs, changes in the fault current, and different modes of operation (grid-connected or island mode), which can cause more complex fault current paths. The following challenges should be highlighted in protection schemes for MGs:

- Changes in fault currents,
- Blinding protection,
- False tripping and

- Unsynchronised and automatic reclosing (Barra, Coury and Fernandes, 2020).

The operation of protection relays may be adversely affected by the integration of DGs into the grid. In addition to the problems described above, the integration of DGs into the grid can also cause problems in the coordination between overcurrent protection relays. This loss of coordination between the overcurrent protection relays may result in disconnecting the DG from the grid and reduce the reliability of the MG system (Bisheh, Fani and Shahgholian, 2021).

The information that is transmitted between the microgrid controller and microprocessor-based relays should be evaluated for speed and dependability as part of the protection design philosophy. This can be achieved by implementing IEC 61850 GOOSE communication between IEDs (Vegunta et al., 2021).

An adaptive protection scheme requires communication between a central controller and local IEDs. Implementing communication protocols between the IEDs allows information regarding the status of the generators, loads, and battery storage devices to be transmitted or received. The precalculated protection settings can be deployed by a centralised or decentralised communication architecture. Centralised architecture is the most common communication scheme that is currently being implemented in MG. The MGCC will make decisions about the protection settings that need to be applied to the protection of IEDs based on the network status. Some of the common communication protocols that are frequently employed include Modbus, DNP3, and IEC 61850 (Hatziargyriou et al., 2014).

Coordination becomes a complex task when RESs are integrated into the network. Factors such as variable fault current contributions and various network topologies contribute to this. When considering overcurrent protection relays, the following two adjustable parameters should be considered: the plug setting (PS) and the time multiplier setting (TMS). The objective of the overcurrent coordination is to optimise the duration of the operating time by adjusting the PS and TMS parameters for the overcurrent protection relays (El-Naily et al., 2022).

Awareness of the research: To develop and implement an adaptive protection scheme based on the IEC 61850 standard-based GOOSE communication between the IEDs to overcome the problems associated with conventional protection schemes in MG systems.

1.3 Statement of the Research Problem

MGs can operate in both grid-connected and islanded modes, and it is therefore important that the protection scheme implemented ensures that the MG system is protected against all types of faults that may occur in both modes. When DGs are incorporated into a network, the power flow becomes bidirectional, rendering conventional overcurrent protection schemes insufficient for the MG (Hussain and Kim, 2016).

Problem statement: The MG can operate in both grid-connected and island modes. The fault currents measured in the island mode of operation are less than those measured in the grid-connected mode. The contribution of the fault current depends on the quantity, control type, and power rating of the DGs, as well as the mode of operation. As a result, conventional protection schemes are ineffective and can lead to a loss of coordination between protection relays. Therefore, it is necessary to implement an adaptive protection scheme in which the relay settings are dynamically updated in response to the status of the circuit breaker monitored by relays. This ensures that the MG is always protected against fault currents, regardless of the network configuration.

1.4 Research aim and objectives

1.4.1 Aim

This research aims to contribute to the field of microgrid protection by implementing an adaptive protection scheme using the IEC 61850 GOOSE communication protocol. This comprehensive approach aligns with the challenges posed by bidirectional power flow and the need for adaptive and standardised protection in modern microgrid systems.

1.4.2 Objectives

The objective of this research is to develop and implement a hardware-in-the-loop (HIL) protection simulation as follows:

i. Provide a literature review on the modelling and control of DGs and protection schemes implemented in MG systems.
ii. Investigate the load flow, fault, and protection coordination study of the MG system for both modes of operation in the DIgSILENT simulation environment.
iii. Modelling and simulation of the hybrid MG system in RSCAD software, a suite of RTDS.
iv. Develop and implement HIL testing for the directional overcurrent function of the SEL-351A relays and demonstrate the IEC 61850 GOOSE message transmitted via Ethernet to test the trip functionality of the backup relay.
v. Develop and implement a laboratory-scale test bench for the adaptive protection scheme based on the hardwired connection between the RTDS and SEL-351A relays.
vi. Develop and implement a laboratory-scale test bench for the IEC 61850 standard-based adaptive protection scheme using the SEL-700G relay.

1.5 Hypothesis

MGs are capable of functioning in both grid-connected and island modes. The mode of operation changes the fault current, which can result in blinding or false tripping of overcurrent relays. The loss of coordination between protection relays can be resolved by developing and implementing an IEC 61850 standard-based adaptive protection scheme. The IEC 61850 standard-based adaptive protection scheme is tested in a real-time simulation environment between the RTDS and the protective relays.

1.6 Delimitation of the research

The research project consists of the following:

i. The modelling and simulation of the modified IEEE 14-bus MG system in the DIgSILENT PowerFactory and RSCAD simulation environments, respectively.
ii. Implement HIL protection testing in the real-time simulation environment using the RTDS for the SEL-351A relays.
iii. Implementation of the IEC 61850 GOOSE message between the SEL-351A relays.

iv. Implementation of the adaptive protection scheme based on the hardwired connection and the IEC 61850 communication protocol between the RTDS and the SEL directional overcurrent relays.

1.7 Limitation of the research

The following limitations apply to the research project:

i. The fault ride-through (LVRT and HVRT) capability of the DG as per the IEEE 1547 standard is not considered for this research project as this requires the implementation of a suitable protection scheme at the POC.
ii. A centralised adaptive protection scheme whereby all the local controllers send their status information to the microgrid-central controller (MGCC) is not considered for this research project.
iii. Islanding detection methods such as rate of change of frequency (ROCOF) are not part of this research project.

1.8 Assumption

The implementation of this research project is based on the following assumptions:

i. The WT is connected to permanent magnet synchronous generators (PMSGs) i.e., Type 4 WTGs that are modelled in the MG system. The fault current from the WTGs is limited to 1.5 p.u. during the DIgSILENT simulations. The fault current is limited because of the power electronic converters that are used (Nelson, 2012), (Walling, Gursoy, and English, 2011).
ii. The implementation of the IEC 61850 standard-based GOOSE message between the IEDs provides faster communication when compared to hardwired connections.
iii. The results obtained during the HIL testing with the external IEDs are as close as possible to the real-world power system. This is because the simulation is performed using a real-time digital simulator (RTDS).
iv. Primary relay R1 and backup relay R14, as highlighted in Figure 1, are considered relay pairs due to the hardware limitations at the CSAEMS at the CPUT.
v. The GOOSE message published by the primary relay R1 only contains the protection trip conditioning (PTRC) logical node (LN). The output of all the protection LNs is connected to a common trip and is transmitted to the circuit breaker (XCBR) LN (IEC 61850-7-4, 2010).

vi. A gain parameter (K_p) of 200 is selected for the proportional controller of the WTG (RSCAD manual, 2022).

1.9 Research Methodology

This research aims to design and implement an adaptive protection scheme for the MG system. This research utilises the modified IEEE 14-bus distribution system with an added DG as a case study.

The data for the modified IEEE 14-bus distribution system are given in Tables 3.1 to 3.5 of this thesis. The IEC 61850 standard-based GOOSE message is utilised to implement the adaptive protection scheme between the IEDs and is tested in a real-time simulation environment via the RTDS.

Figure 1.1 displays the modified IEEE 14-bus system that is simulated in the DIgSILENT and RSCAD environments. The MG system comprises wind turbine generators (WTGs) and a synchronous generator. The WTGs are linked to the distribution system at the point of connection (POC) via the main transformer. The fault currents are investigated for both grid-connected and island modes of operation for the MG. The position of the circuit breakers at the point of common coupling (PCC) determines the mode of operation. Hardware-in-the-loop (HIL) protection testing is demonstrated at the CSAEMS lab at CPUT by utilising the RTDS, Omicron CMS 156 amplifiers, and SEL-351A directional overcurrent relays. A laboratory-scale test bench setup is used to demonstrate the IEC 61850 standard-based GOOSE communication between the IEDs. Finally, the adaptive protection scheme is implemented for hardwired connections by utilising the SEL-351A relays and the IEC 61850 standard for the SEL-700G relay.

The research methodology is divided into three sections. Section 1.9.1 gives details of the literature review, section 1.9.2 discusses the modelling and simulation of the modified IEEE 14-bus MG system in the DIgSILENT and RSCAD simulation environments, and section 1.9.3 discusses the implementation of the HIL protection testing.

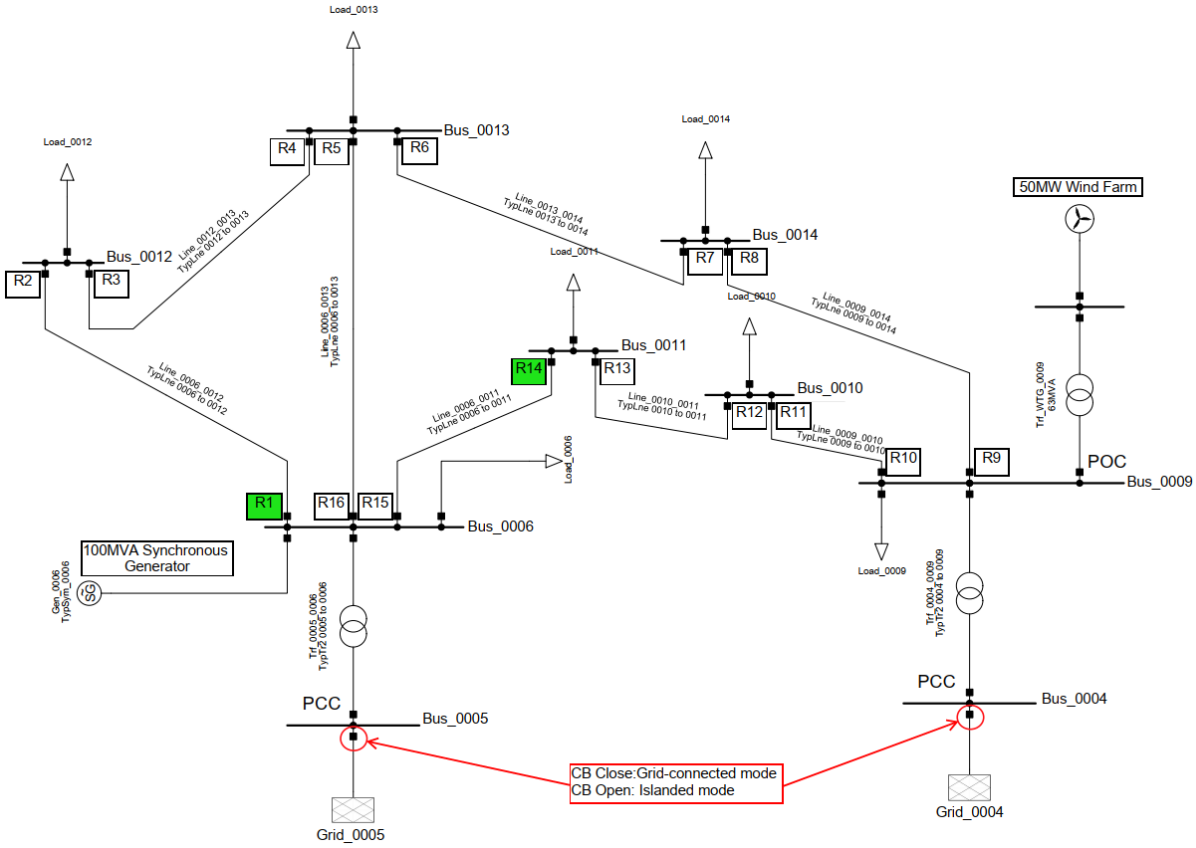

Figure 1.1: **Modified IEEE 14-bus system with added DG**

1.9.1 Literature review

The control of DGs utilised in MG systems is reviewed in the literature. The IEC 61850 standard about “communication networks and systems for power utility automation” is reviewed. Finally, the adaptive protection schemes implemented in MG systems are reviewed by reading open-access journal articles, published IEEE conference papers, and textbooks.

1.9.2 Modelling and Simulation

As a case study, the modified IEEE 14-bus distribution system is modelled and simulated in the DIgSILENT and RSCAD simulation environments. During the DIgSILENT simulation, load flow and fault analysis are examined for both grid-connected and islanded modes of operation. The DIgSILENT simulation examines a protection coordination study to determine the necessary overcurrent settings for both modes of operation.

The additional DG comprises a 50 MW wind farm equipped with a PMSG (Type 4 WTG) that is linked to the distribution network via a power electronics converter and step-up transformer at the POC. By utilising RSCAD, the PMSG's power electronics and controls are modelled in detail. An examination of the PMSG's performance is investigated in the RSCAD runtime simulations.

1.9.3 Hardware-in-the-loop simulation

CT and VT models are added to the modified IEEE 14-bus MG system. The output signals supplied by instrument transformers are connected to the input of the GTAO (analogue output) model. The low-level analogue output (±10 V) from the GTAO card is connected to the input of the Omicron CMS 156 amplifiers to increase the currents and voltages as needed by the SEL-351A relays. The trip outputs, OUT102 and OUT103 from the SEL-351A relays, are connected to the input of the GTFPI (front panel interface) card. The trip signal is used to operate the circuit breakers modelled in the RSCAD environment. The fault events measured during the RSCAD runtime simulation are investigated for the SEL-351A relays to verify that the external IEDs respond appropriately to the fault conditions. During the HIL simulations, the developed IEC 61850 GOOSE message is implemented between the SEL-351A IEDs and tested.

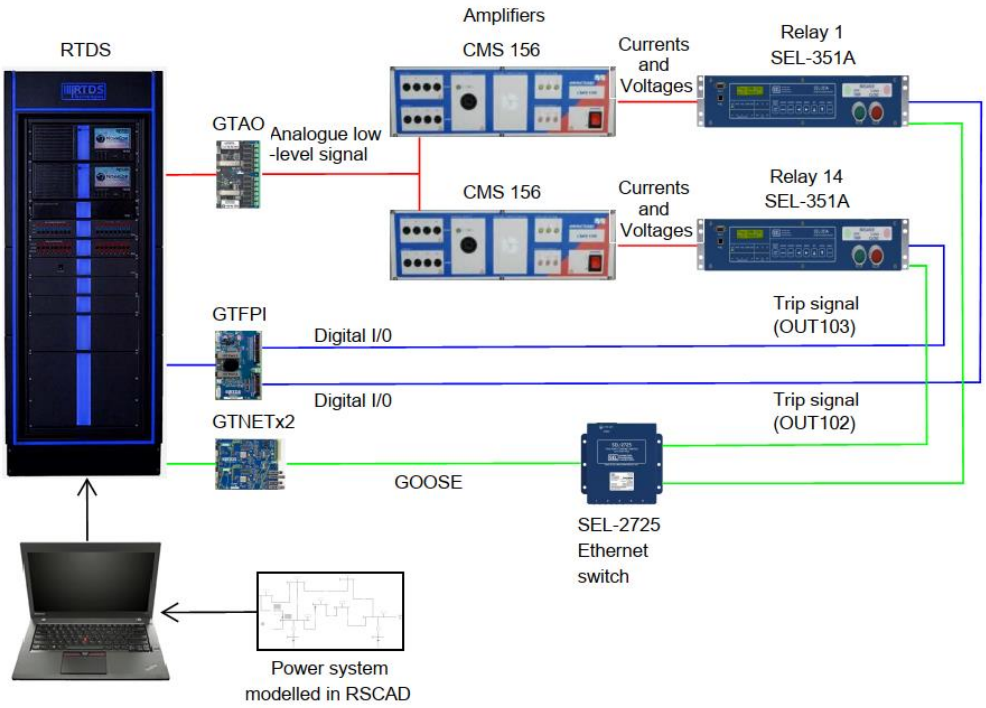

Figure 1.2: **Laboratory-scale test bench setup for HIL protection testing**

1.10 Thesis chapters

The thesis consists of eight chapters, and the description of each chapter is as follows:

1.10.1 Chapter one

This chapter presents the awareness of the research problem, problem statement, research aim and objectives, hypothesis, delimitations and limitations of the research, research methodology, and breakdown of the thesis chapters.

1.10.2 Chapter two

The literature review of the RESs utilised in MGs, control of DGs, the IEEE 1547 standard, the IEC 61850 communication protocol, and adaptive protection schemes are discussed in this chapter.

1.10.3 Chapter three

This chapter presents the load flow and fault analysis of the modified IEEE 14-bus MG system in the DIgSILENT simulation environment. The protection coordination study for the SEL-351A overcurrent relays is investigated.

1.10.4 Chapter four

The modelling of the modified IEEE 14-bus microgrid system with the additional WTGs in the RSCAD simulation environment is detailed in this chapter. The modelling of the permanent magnet synchronous generator (PMSG) (Type 4 WTG) is investigated in detail. The power output from the WTGs is examined at various wind speeds.

1.10.5 Chapter five

The implementation of hardware-in-the-loop (HIL) testing of directional overcurrent relays is detailed in this chapter. CT and VT models are incorporated into the RSCAD model of the modified IEEE 14-bus system. The GTAO (analogue output) and GTFPI (front panel interface) cards are configured.

1.10.6 Chapter six

The implementation of IEC 61850 GOOSE communication between IEDs is detailed in this chapter. Within the GTNET-GSE model in RSCAD, the IEC 61850 IED configuration tool (ICT) is configured for the IEC 61850 GOOSE, in which external IEDs subscribe to or publish via Ethernet.

1.10.7 Chapter seven

The implementation of an adaptive protection scheme for the MG system is detailed in this chapter. The protection scheme comprises the hardwired connection and the IEC 61850 standard-based GOOSE message between the IEDs. The RTDS and SEL relays are utilised to implement and test the adaptive protection scheme in a real-time simulation environment.

1.10.8 Chapter eight

The conclusion of the thesis is detailed in this chapter. Applications to academia and industry and recommendations for future research work are given.

1.11 Conclusion

This chapter gives a background on the development and implementation of the adaptive protection scheme for the MG system through the discussion of the research problem, the research aim and objectives, and the research methodology.

The literature review for the protection and control of MG systems is discussed in the following chapter.

CHAPTER 2
LITERATURE REVIEW

2.1 Introduction

The integration of renewable energy resources (RES) is increasing globally in the power generation, transmission, and distribution of electrical energy due to factors such as fossil fuels becoming scarcer, the deregulation of power utilities, and the impact that traditional power stations have on the environment (Basak et al., 2012).

The MG can operate in either grid-connected or island mode. The fault current contribution for the different modes is different. It is, therefore, necessary to ensure that the correct protection settings are loaded onto the protection IEDs in the network. This can be achieved by implementing an adaptive protection scheme for the microgrid that can be used to update the protection IEDs' settings depending on the system requirements (Vegunta et al., 2021).

Between 2010 and 2023, 377 papers were published using the keywords “microgrid adaptive protection.” The highest number of publications was in 2022, with 64 papers, as shown in Figure 2.1 (Scopus 2023). This increase in research reflects an increasing focus on adaptive protection for microgrids because it offers solutions to the problems faced by traditional protection systems. The structure diagram for the literature review is shown in Figure 2.2.

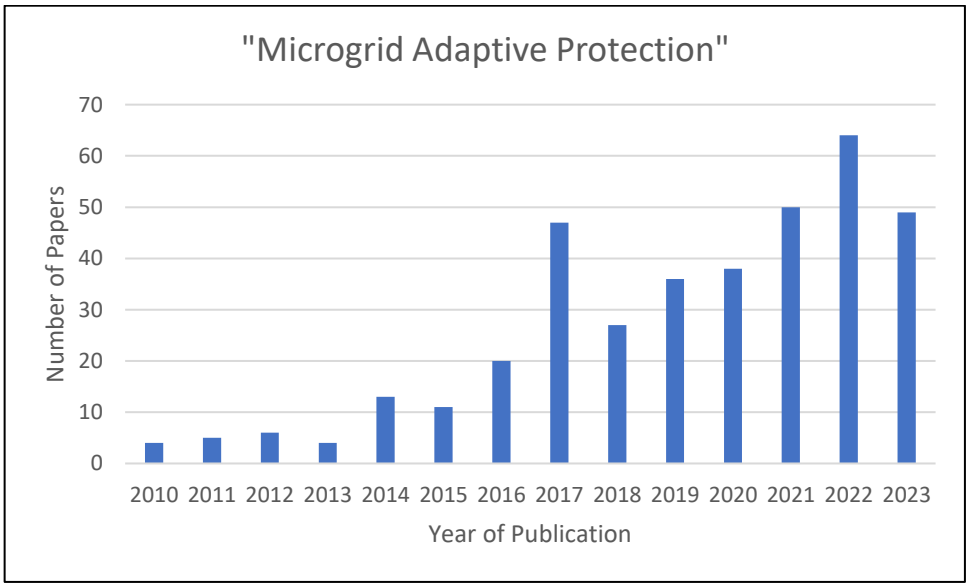

Figure 2.1: Number of papers published per year for microgrid adaptive protection (Scopus, 2023)

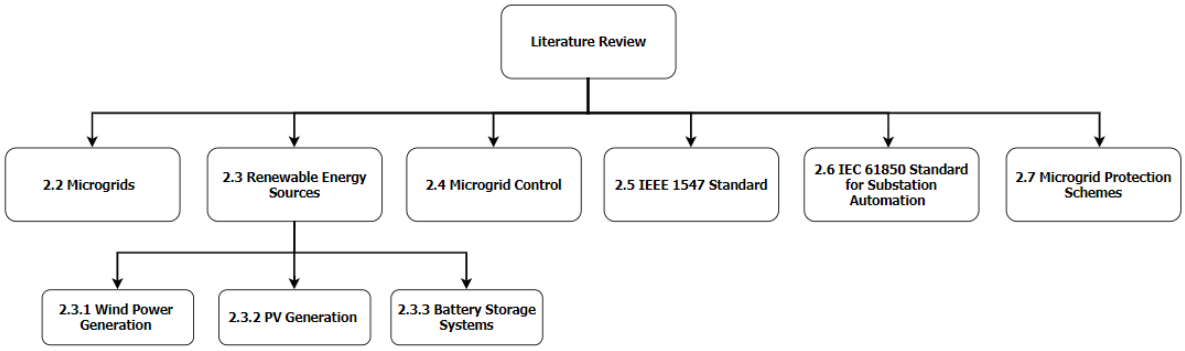

Figure 2.2: Structure diagram for literature review

2.2 Microgrids

Hybrid MGs can combine solar PV and wind generation to increase reliability because of the intermittent nature of available energy. This combination can also reduce the size and cost of battery storage systems required for continuous power supply to consumers (Badwawi, Abusara and Mallick, 2015).

MGs are distribution systems that comprises a group of interconnected loads and distributed energy resources (DERs) that act as a single control entity with respect to the grid. This also includes energy storage systems, control systems, and communication systems. Figure 2.3 illustrates a hybrid MG with solar PV, wind generation, and a battery storage system. Solar PV plants and wind turbine generators are connected to the AC collector bus through converters. To facilitate charging or discharging depending on the system requirements, the battery storage system connects to the AC collector bus through a bidirectional DC/AC converter (Coelho, Gomes and Moreira, 2018).

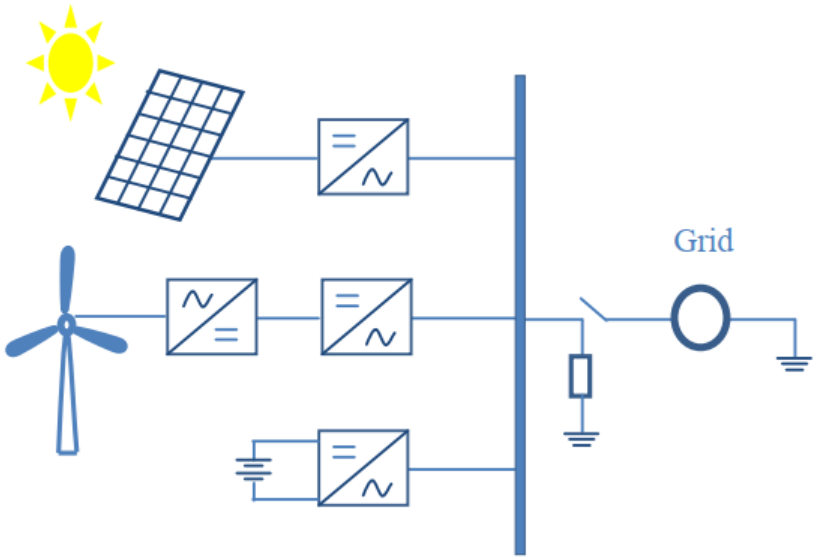

Figure 2.3: Hybrid system with AC microgrid (Badwawi, Abusara and Mallick, 2015)

As a result of changes in wind speeds and variations in solar energy throughout the year, the power output from either wind or solar energy cannot always meet the load demand. Hybrid MGs combine PV and wind RESs, improving system reliability and reducing battery storage size (Fathima et al., 2018).

A microgrid is a local power system that supplies energy to individual consumers. Figure 2.4 shows a typical MG network comprising distributed generators (e.g., WT, PV, and diesel generators) and energy storage systems (e.g., supercapacitors and battery energy storage systems (BESSs). The MG structure consists of a communication infrastructure between the IEDs and a microgrid central controller (MGCC), which manages the control and energy of the entire MG. MG provides a solution to control local generation and loads (Barra, Coury and Fernandes, 2020).

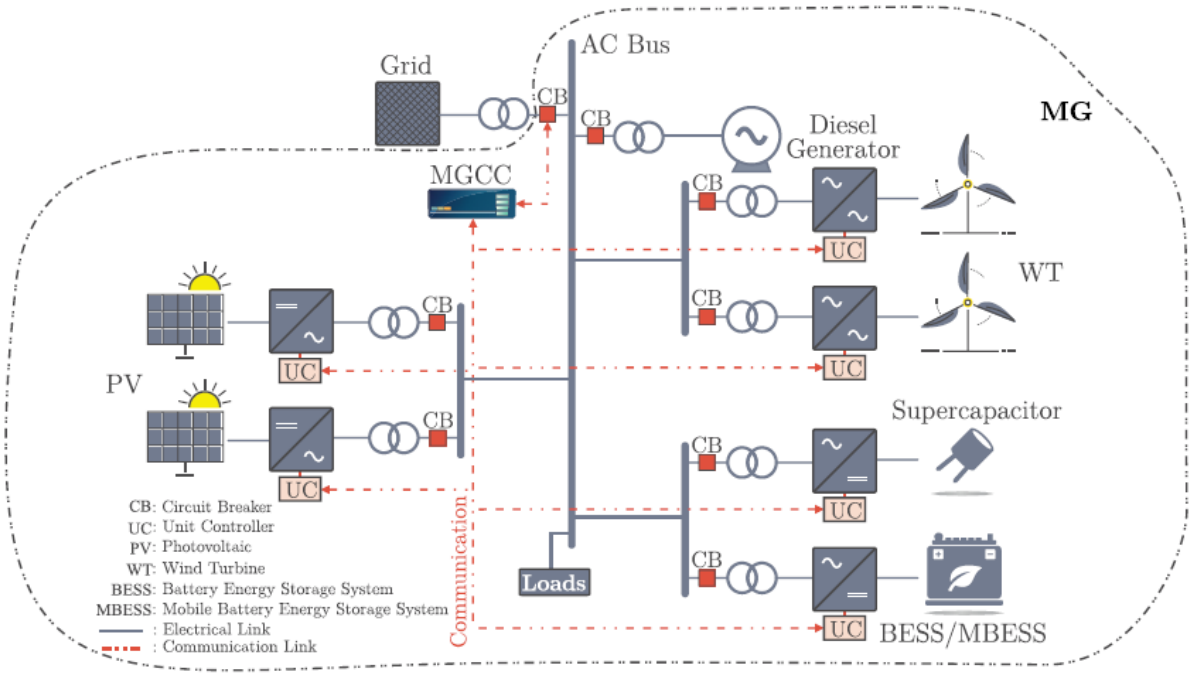

Figure 2.4: **Microgrid structure (Barra, Coury and Fernandes, 2020)**

2.3 Renewable energy sources for microgrids

2.3.1 Wind power generation

According to IRENA's latest data, for both onshore and offshore installations, the total global installed capacity from wind generation has increased from 216 GW in 2011 to more than 836 GW in 2022, as shown in Figure 2.5. In 2016, wind energy accounted for 6% of the electricity generated by RES (IRENA, 2023).

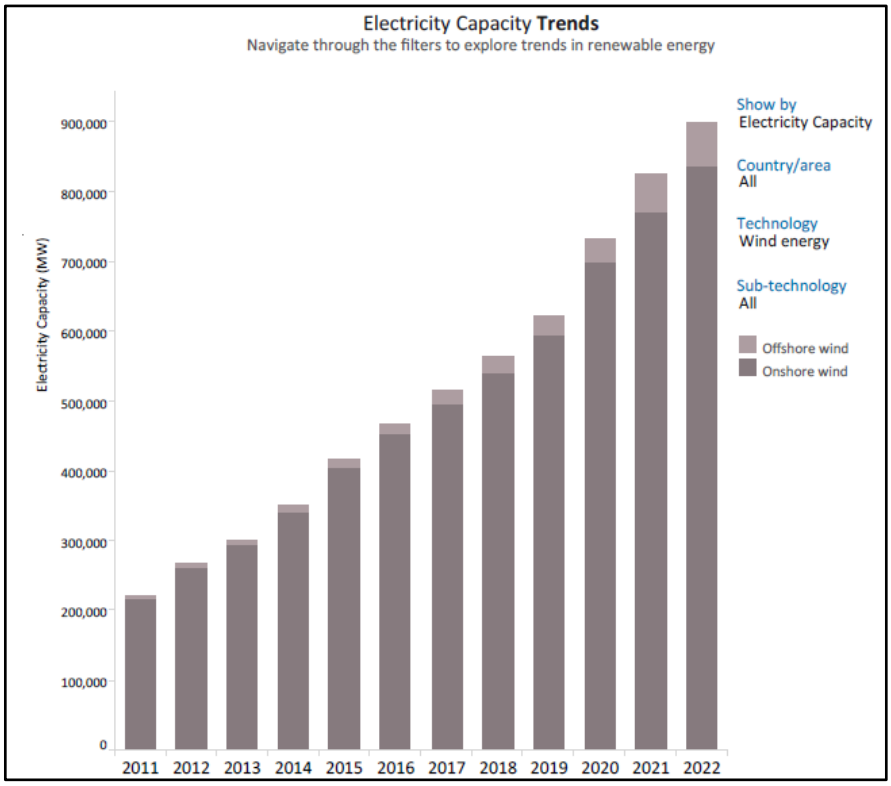

Figure 2.5: **Global installed capacity from wind generation (IRENA, 2023)**

A wind turbine consists of two or more blades that are mechanically coupled to an electrical generator to capture the wind's kinetic energy and convert it into electrical energy. As shown in Figure 2.6, the turbine is mounted on a large tower in a horizontal configuration (Patel and Beik, 2021).

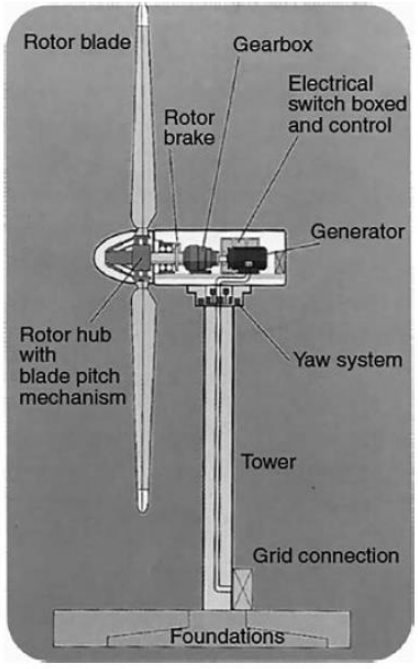

Figure 2.6: **Construction of a wind turbine showing the major components (Patel and Beik, 2021)**

WTGs consist of mechanical and electrical systems to convert wind energy into electrical energy. These components include the rotor, gearbox, generator, power electronics converter, and step-up transformer, as shown in Figure 2.7 (Blaabjerg and Ionel, 2017).

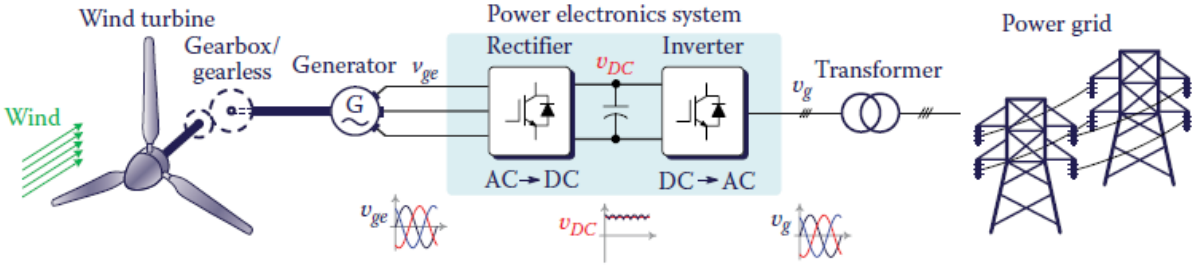

Figure 2.7: **Power electronic converters enabling wind energy conversion system (Blaabjerg and Ionel, 2017)**

Currently, four types of WTG's are being employed in the industry:

- Type I: Fixed speed turbine with squirrel-cage induction generator (SCIG)
- Type II: Variable speed turbine with a wound-rotor induction generator (WRIG)
- Type III: Variable speed turbine with a double-fed induction generator (DFIG)
- Type IV: Variable speed turbine with a permanent-magnet synchronous generator (PMSG)

The DFIG wind turbine technology is mostly adopted by manufacturers in recent wind power plants. The power ratings for WTGs ranges up to 6 MW for onshore installations and up to 14 MW for offshore installations. The output voltage from the WTG is normally rated at 690 V and is stepped up to the distribution voltage level (e.g., 33 kV) through a step-up transformer (Glover et al., 2017).

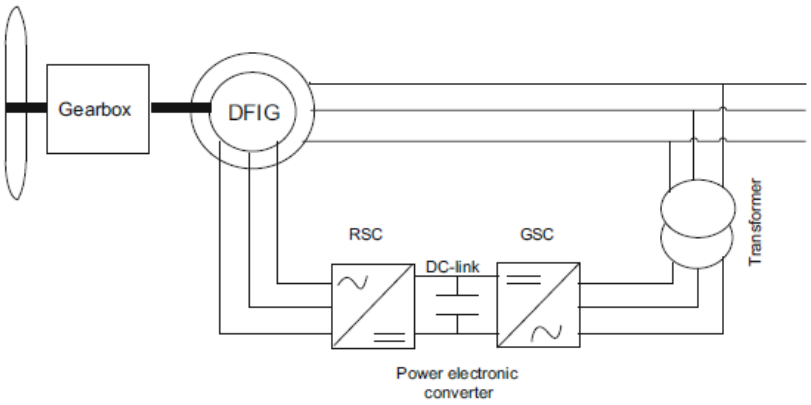

Figure 2.8: **Variable speed turbine with double-fed induction generator (Bansal et al., 2017)**

The three-phase rotor of the DFIG is supplied by a voltage source frequency converter that feeds slip frequency power to the rotor. The stator is supplied from the same source as the rotor, hence the name. The wind turbine is connected to the grid through back-to-back converters, as shown in Figure 2.8. Rotor speed and grid frequency are decoupled through the power electronic frequency converters. The per-phase equivalent circuit for the DFIG is shown in Figure 2.9. The DFIG has a second controlled source that is controlled by a DC/AC converter that supplies the controlled current to the rotor winding. The benefit of the DFIG is that only approximately 20%–30% of the power generated needs to pass through the frequency converter, which reduces the cost of the power electronics converter that is required. The disadvantage is that this causes stability problems because the IEEE 1547 standard requires the wind turbine to remain connected to the grid during a voltage dip (Patel and Beik, 2021).

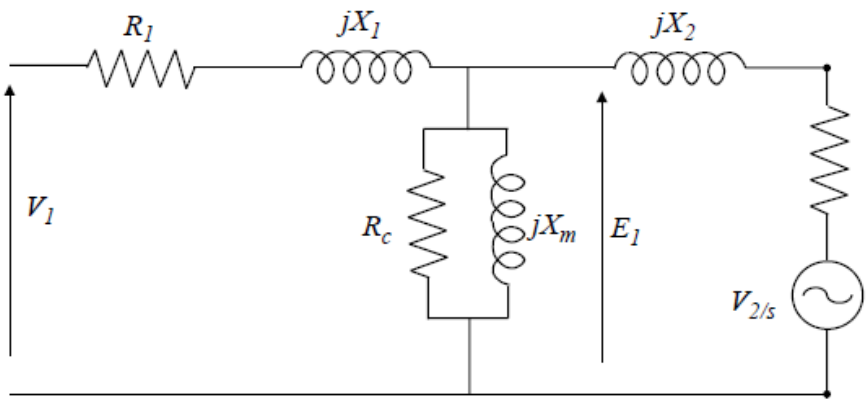

Figure 2.9: **DFIG equivalent circuit (Patel and Beik, 2021)**

The control of the WTG consists of controlling both the mechanical and electrical systems. The power flow within the system must be controlled. This means controlling the mechanical components on the input side of the converter and the electrical power on the output side, which is injected into the grid. Variable-speed wind turbine generators can change the current output by adjusting the power electronic converters, thereby adjusting the turbine speed to achieve maximum power output depending on the available wind speed as shown in Figure 2.10 (Blaabjerg and Ionel, 2017).

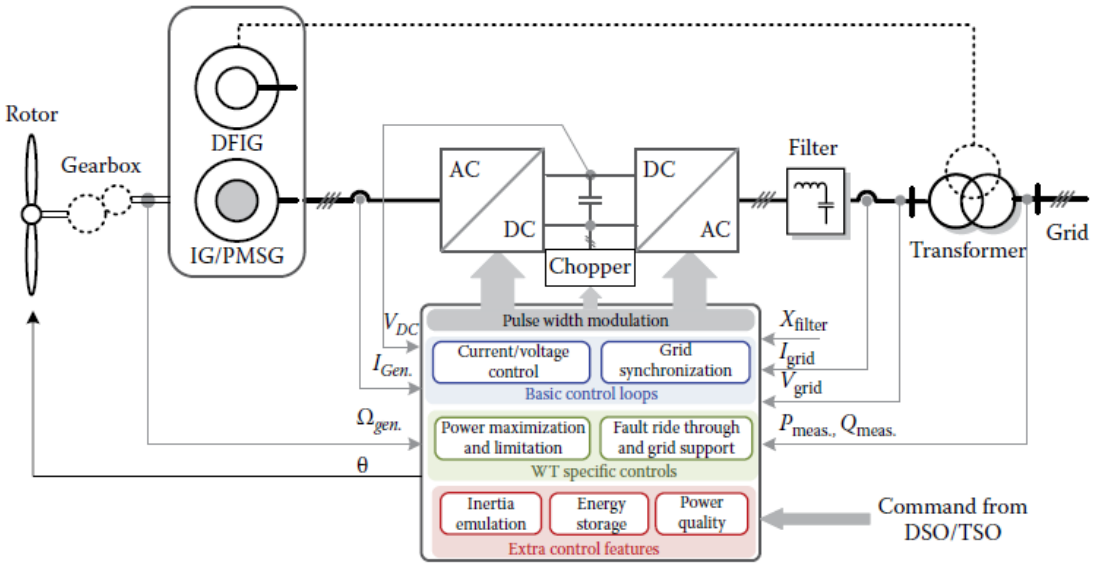

Figure 2.10: **Power electronics converter control for wind turbine generators (Blaabjerg and Ionel, 2017)**

The wind turbine power output represents a nonlinear characteristic curve of wind speed. The maximum power point tracking (MPPT) control continuously adjusts the WTG rotor speed to obtain the maximum power from the WTG at different wind speeds. In the MPPT control scheme, the wind speed is taken as the parameter, while the wind turbine rotor speed is the variable. Equation 2.1 gives the output power of the wind turbine. As shown in Figure 2.11, the maximum or optimal output power (P_{opt}) can be obtained from the wind resource at different wind speeds by varying the rotor speed of the generator (Bansal et al., 2017).

$$P_{WT} = \frac{1}{2}\rho A C_P \left(\frac{\omega_r R}{nv}\right) v^3 = \frac{1}{2}\rho A C_P \left(\frac{2\pi N_r R}{60nv}\right) v^3$$

Equation 2.1

Where:

ρ = air density

A = swept area of the turbine rotor

C_P = power coefficient of the turbine rotor

N_r = rotor speed

R = radius of the turbine rotor

n = gearbox ratio

v = velocity of the air

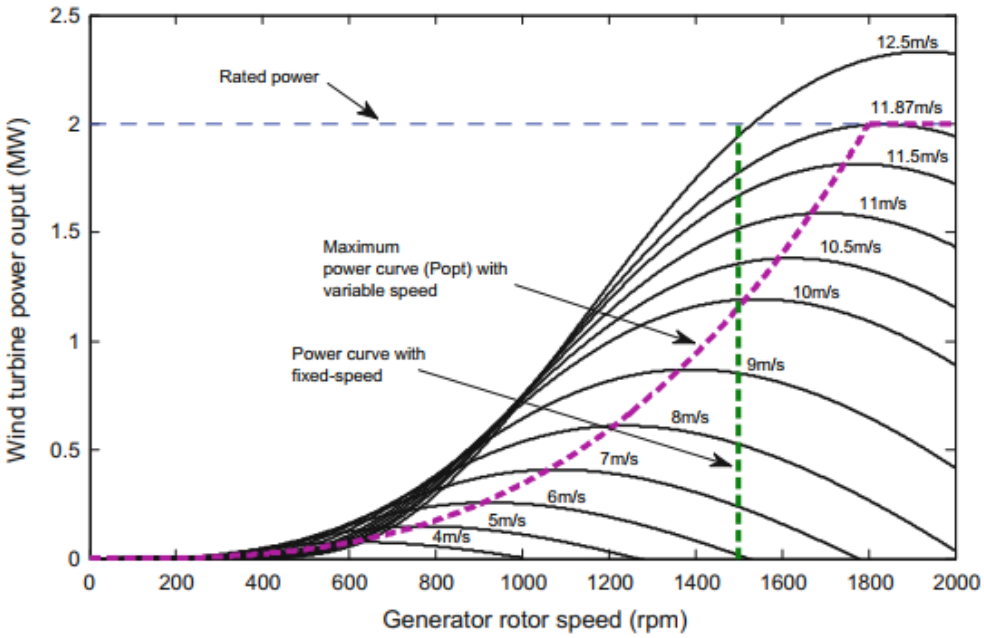

Figure 2.11: MPPT characteristic of a wind turbine based on variable wind speed (Bansal et al., 2017)

2.3.2 Photovoltaic Solar Generation

According to IRENA's latest data, the total global installed capacity from solar energy has increased from 72 GW in 2011 to more than 1055 GW in 2022 for both solar photovoltaic (PV) and solar thermal, as shown in Figure 2.12 (IRENA, 2023).

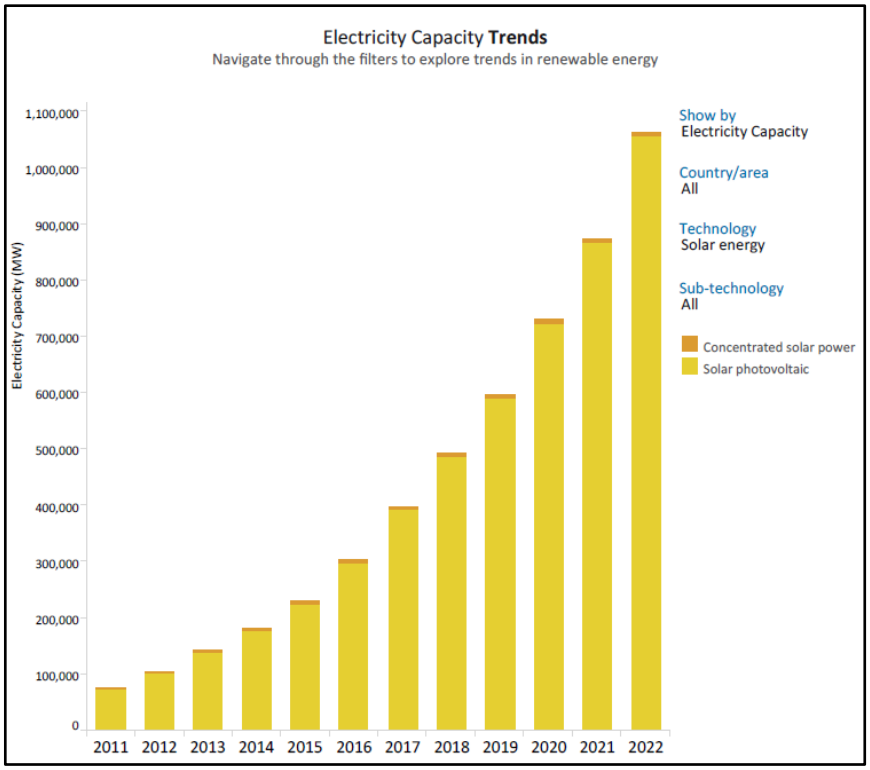

Figure 2.12: Global installed capacity of solar PV (IRENA, 2023)

As shown in Figure 2.13, the grid-connected PV system consists of DC/DC and DC/AC power electronic converters. The converters are connected through a step-up transformer to connect the PV system to the grid (Blaabjerg and Ionel, 2017).

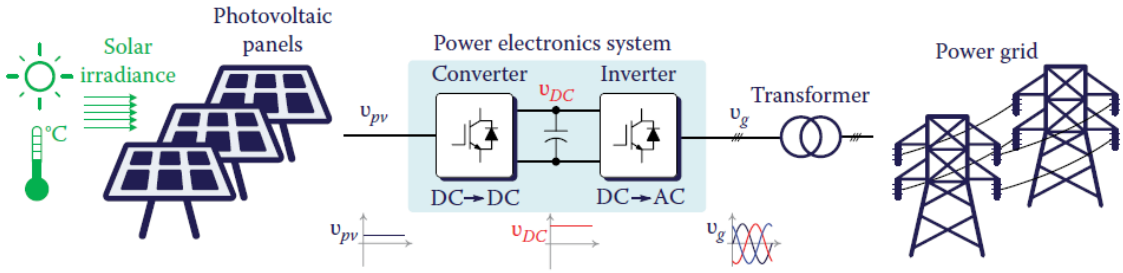

Figure 2.13: **Power electronic enabling PV energy conversion system with DC/DC and DC/AC converters (Blaabjerg and Ionel, 2017)**

The energy required by a photon to dislodge electrons from a semiconductor depends on the bandgap of the semiconductor element. To dislodge the electrons, the energy generated by the photons must be greater than the bandgap potential. Photon energy (Ep) is transferred to the semiconductor material of a solar cell to generate electric energy as shown in Figure 2.14 (Bansal et al., 2017).

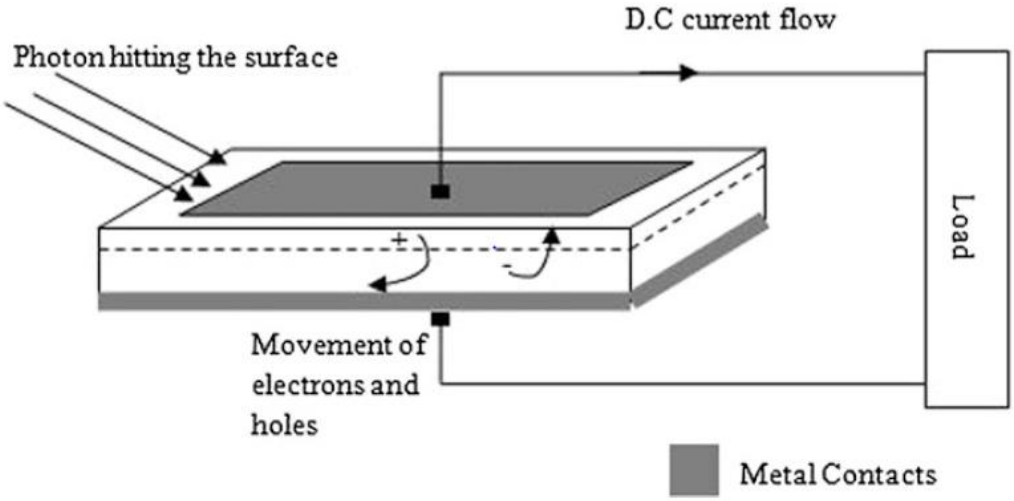

Figure 2.14: **Operation of a photovoltaic or solar cell (Bansal et al., 2017)**

The equivalent electrical circuit for a PV cell is shown in Figure 2.15. The energy, Ep, is converted into Iph (the current produced by the photon) in the semiconductor. The solar cell is represented by a current source (Iph). The current I that flows through the load is equal to Iph – Id (the diode current that flows when there is no solar radiation available). The voltage across the load resistance is the DC output voltage of the PV cell (Bansal et al., 2017).

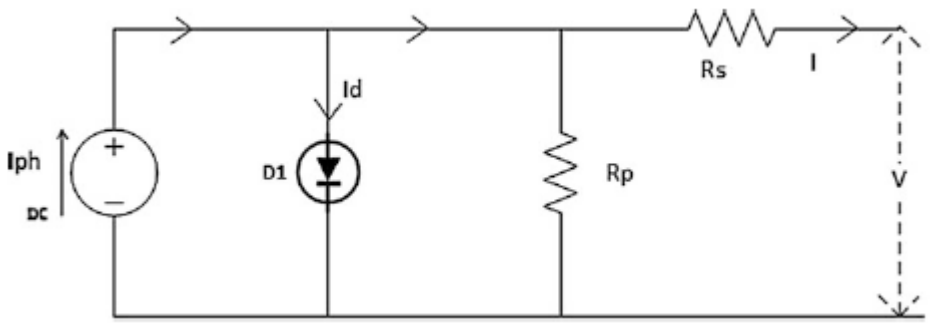

Figure 2.15: Equivalent circuit of a PV cell (Patel and Beik, 2021)

The current flowing through each PV cell can be expressed mathematically as shown in Equation 2.2.

$$I = I_{ph} - I_d = I_{ph} - I_o\left[\exp\left\{\frac{eV}{kT_c}\right\} - 1\right]$$

Equation 2.2

Where:

e = 1.6021765 x 10^{-19} C (electron charge)

V = Voltage across the cell (Volts)

K = 1.38064852 x 10^{-23} J/K

T_C = Absolute cell temperature (K)

I_O = Dark saturation current (A)

The knee point on the I-V curve represents the optimal operation point for the PV cell as shown in Figure 2.16. The output power of the PV cell is the product of the current and voltage (P = I x V). The values concerning V can be used to obtain the P-V curve (Bansal et al., 2017).

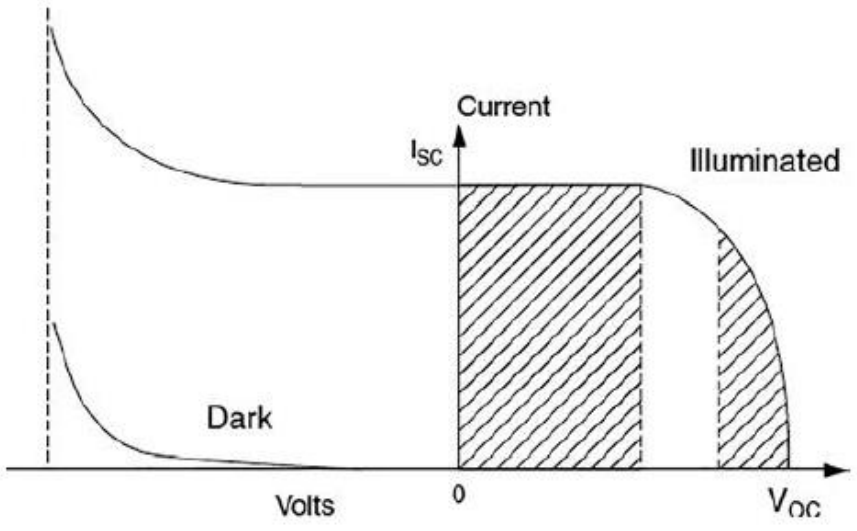

Figure 2.16: I-V characteristic curve for a PV module in the sunlight and the dark (Patel and Beik, 2021)

The knee point of the P-V curve represents the maximum output power of the PV cell as shown in Figure 2.17. Maximum power point trackers (MPPTs) are installed allowing the PV cells to operate at the point where they can produce the maximum output power at any given time (Bansal et al., 2017).

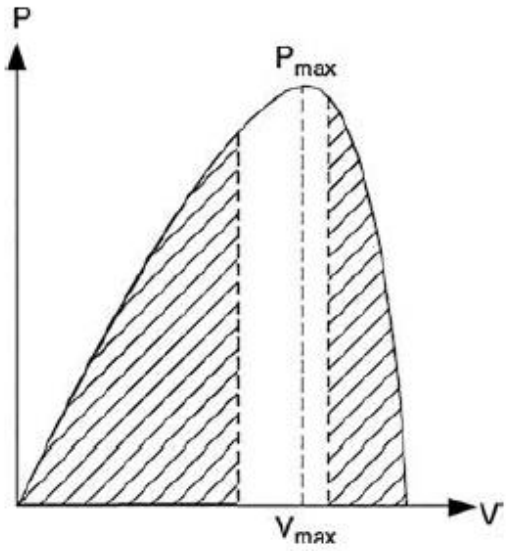

Figure 2.17: **P-V characteristic curve for a PV module in the sunlight (Patel and Beik, 2021)**

The maximum power point can be expressed mathematically as shown in Equation 2.3.

$$P_{\max} = I_{\mathrm{m}} \times V_{\mathrm{m}}$$

Equation 2.3

The efficiency of a PV cell is the output power divided by the input power from the solar energy and can be expressed mathematically as shown in Equation 2.4.

$$\eta = \frac{P_{\max}}{P_{\text{input}}} = \frac{I_{\max} V_{\max}}{A G_{\mathrm{T}}}$$

Equation 2.4

Where:

P_{input} = Input power from solar energy (W)

A = Area of the cell (m^2)

G_T = Solar irradiance (W/m^2)

η = Efficiency of a PV cell

2.3.3 Battery Storage Systems

With the development of smart grids, the demand for energy storage applications is increasing. These applications include the penetration of large-scale renewable energy sources, the improvement of power system efficiency, reducing the cost of power systems, and improving the quality of power delivery (Yao et al., 2016).

The following energy storage technologies are available for wind and PV power systems:

- Electrochemical battery
- Flywheel
- Compressed air
- Supercapacitor

The battery consists of electrochemical cells that are connected in series or parallel to ensure the required voltage and current. To increase the output voltage of the battery, the cells must be connected in series. The product of the voltage and ampere-hour gives the watt-hour (Wh) energy rating of the battery. Battery charge and discharge rates are given in Ah (Patel and Beik, 2021).

The following types of batteries are available on the market:

- Lead-acid (Pb-acid)
- Nickel-cadmium (NiCd)
- Nickel-metal hydride (NiMH)
- Lithium-ion (Li-ion)
- Lithium-polymer (Li-poly)
- Zinc-air

Table 2.1: Average cell voltage during discharge for batteries (Patel and Beik, 2021)

Electrochemistry	Cell Volts	Remark
Lead-acid	2.0	Most cost-effective
Nickel-cadmium	1.2	Exhibits memory effect
Nickel-metal hydride	1.2	Temperature-sensitive
Lithium-ion	3.6	Metallic lithium free
Lithium-polymer	3.0	Contains metallic lithium
Zinc-air	1.2	Requires good air management

The equivalent electrical circuit for a battery is represented in Figure 2.18. The battery is a constant voltage source with internal resistance. The output voltage E_i of the battery

decreases linearly as the battery Ah discharges (Q_d). The battery internal resistance R_i increases linearly with Q_d. The maximum power supplied to the load occurs when the source impedance is equal to the load impedance ($R_i = R_L$). This can be expressed mathematically as shown in Equation 2.5 (Patel and Beik, 2021).

$$P_{\max} = \frac{E_i^2}{4R_i}$$

Equation 2.5

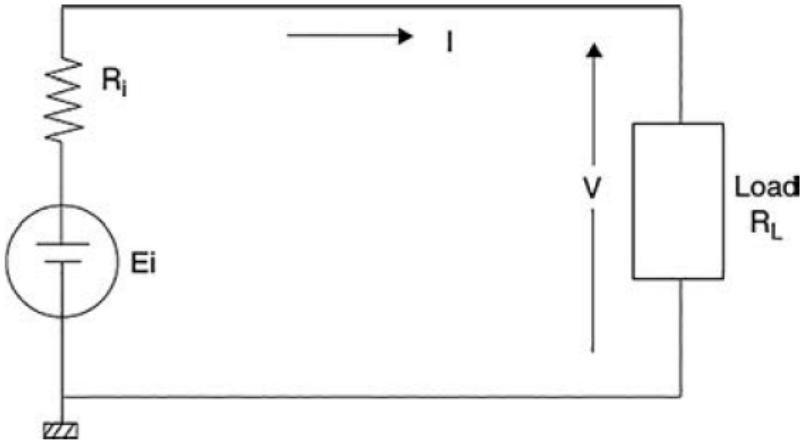

Figure 2.18: **Equivalent electrical circuit for a battery showing the internal voltage and resistance (Patel and Beik, 2021)**

$$\eta = \frac{R_L}{R_L + R_i}$$

Equation 2.6

The efficiency decreases with a decrease in the charge capacity of the battery (Patel and Beik, 2021).

2.4 Microgrid control

When the MG operates in grid-connected and island mode, the MGCC is the most essential piece of equipment employed in substation automation and control. The MGCC facilitates DER coordination by comparing the available generating capacity to load demand. The MGCC regulates the voltage and frequency output of the DERs to ensure system stability (Kaur, Kaushal and Basak, 2016).

There are several control strategies available for microgrid controls namely:

- Natural droop control

- Modified natural droop control
- Hierarchical droop control
- Virtual droop control

The resilient version of the modified natural droop controller is shown in Figure 2.19. The controller is composed of three layers. The first layer is an autonomous layer based on the concept of the Consortium for Electric Reliability Technology Solutions (CERTS). Grid-connected devices use the grid voltage as a reference, and the active and reactive power values are predefined. DGs connected to the grid use maximum power point tracking (MPPT) capabilities for active power and voltage droop control for reactive power support.

The second layer is the dispatch layer. The active and reactive power of the DG unit is adjusted to move from one source to another and to adjust the storage power depending on the SOC. The third layer is the optimization layer, which optimises based on the available generation capacity and load demand (Fu et al., 2015).

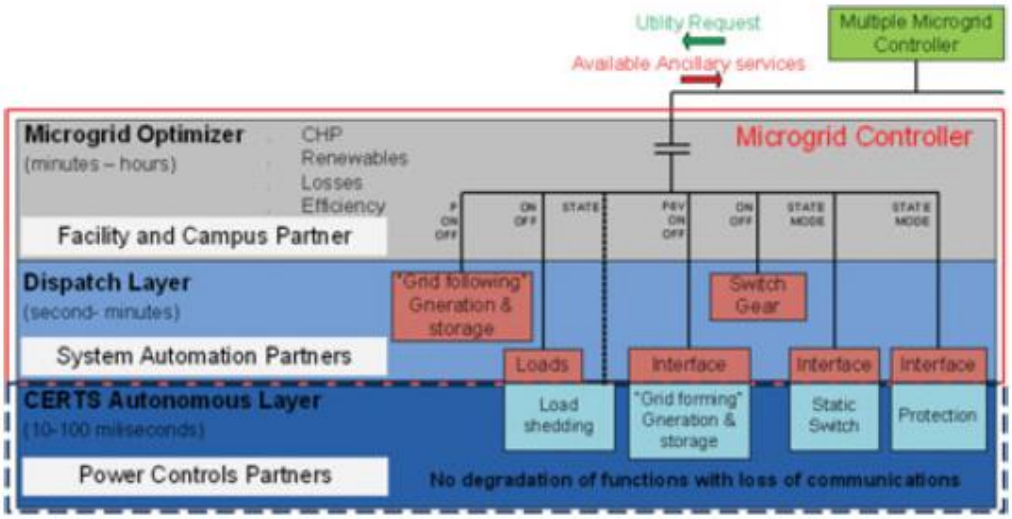

Figure 2.19: **Architecture for the control layers for a microgrid controller (Fu et al., 2015)**

MGs comprise DGs, energy storage systems (ESS), and loads. The ESS must store the excess power available from the DGs under light load conditions and can supply power to the load if the DGs are not available. MGs can operate in either grid-connected or island mode, and a well-developed power management and control strategy is important. The primary control level ensures the stability of the power system, and the secondary control level ensures that the MG operates within the permissible voltage and frequency range according to the IEEE 1547 standard. The tertiary level determines the exchange of power between the MG and the grid. The droop control

method is used for synchronous generators, in which the active and reactive power is varied according to the voltage magnitude and frequency. The active (P) and reactive (Q) power values are obtained from the voltage and current measurements. As shown in Figure 2.20, P/f and Q/V define the characteristic equations for the voltage magnitude and frequency of the DG units The power output of each DG unit is controlled by the control loop shown in Figure 2.21. (Abuhilaleh, Li and Hossain, 2020).

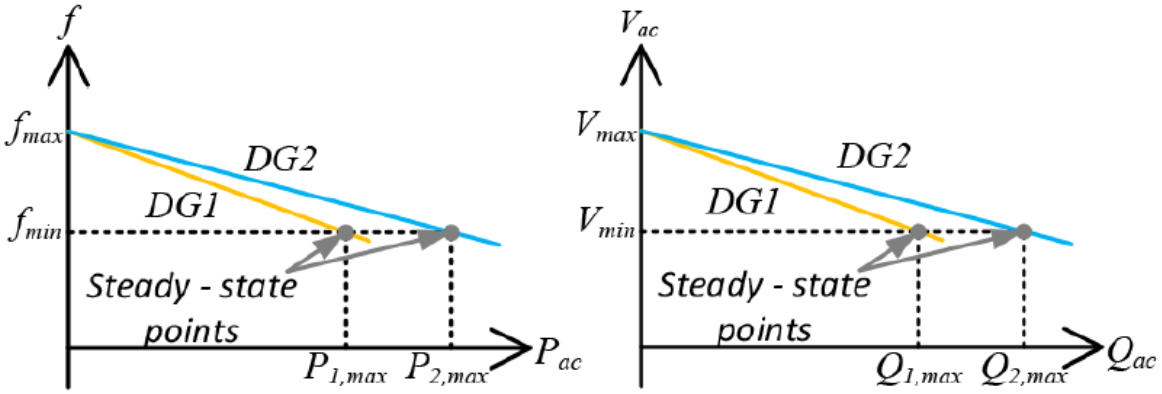

Figure 2.20: Active and reactive power droop characteristics of AC MGs (Abuhilaleh, Li and Hossain, 2020)

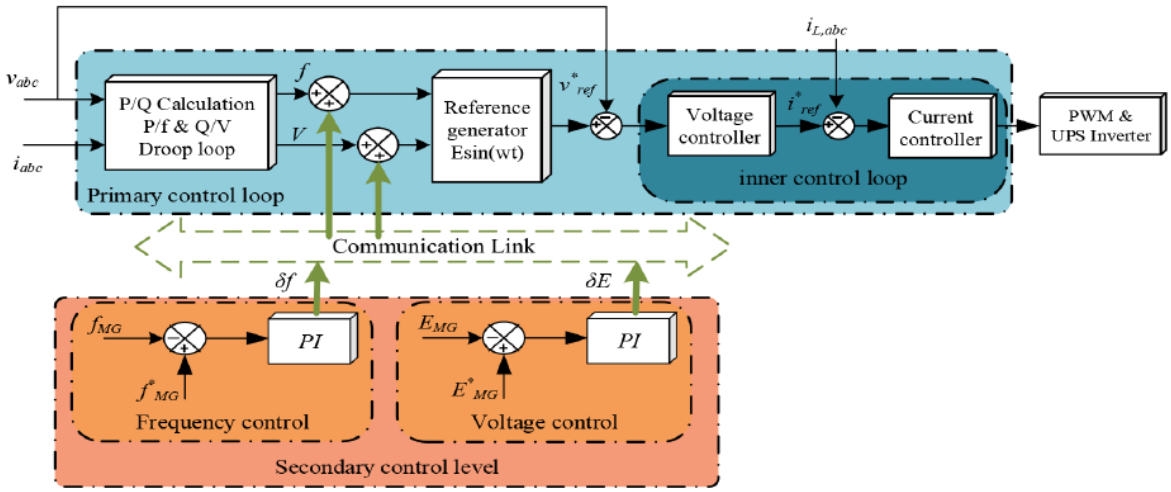

Figure 2.21: Primary and secondary control for AC MGs (Abuhilaleh, Li and Hossain, 2020)

2.5 IEEE 1547 Standard

The IEEE 1547 standard specifies the technical requirements for the interconnection of DG units during operation under abnormal fault conditions, power quality, and islanding. It also provides specifications and requirements for the interconnection and interoperability of distributed energy resources (DERs) with electric power systems (EPSs). The DER must be able to supply power with voltage and frequency levels within the limits provided by the regulating authority. The normal operating voltage ranges from 0.95 to 1.05 p.u. of the nominal voltage. If the operating voltage is below or higher than the voltage threshold, the DER must be disconnected from the grid within a specified clearing time, as shown in Table 2.2. As soon as the DER disconnects from the grid, it cannot reconnect until the voltage level is within the acceptable limits provided in the standard. The standard was divided into three categories related to the response of the EPS area to abnormal conditions. Category I is based on the essential bulk power system stability and reliability requirements that can be easily achieved by all available DER technologies (IEEE 1547, 2018).

Table 2.2: DER response (shall trip) to abnormal voltages for DER (IEEE 1547: 2018)

Shall trip—Category I				
Shall trip function	Default settings[a]		Ranges of allowable settings[b]	
	Voltage (p.u. of nominal voltage)	Clearing time (s)	Voltage (p.u. of nominal voltage)	Clearing time (s)
OV2	1.20	0.16	fixed at 1.20	fixed at 0.16
OV1	1.10	2.0	1.10–1.20	1.0–13.0
UV1	0.70	2.0	0.0–0.88	2.0–21.0
UV2	0.45	0.16	0.0–0.50	0.16–2.0

The DER must be able to handle the voltage ride-through capabilities listed below in Table 2.3 without exceeding its capabilities. If the DER does not provide the necessary ride-through capability as set out in Table 2.3, or if the DER prevents the start of a trip due to a voltage disturbance within the ride-through region, the DER constitutes noncompliance with IEEE 1547 standards. Once the frequency range is within the range set out in Table 2.4 and the frequency component of the voltage on any phase is greater than 30%, the DER must not be energised and trip within the specified clearing time. Under- and over-frequency elements must initiate a trip within the clearing times listed in Table 2.4 (IEEE 1547, 2018).

Table 2.3: Voltage ride-through requirements for DER (IEEE 1547:2018)

Voltage range (p.u.)	Operating mode/response	Minimum ride-through time (s) (design criteria)	Maximum response time (s) (design criteria)
$V > 1.20$	Cease to Energize[a]	N/A	0.16
$1.175 < V \leq 1.20$	Permissive Operation	0.2	N/A
$1.15 < V \leq 1.175$	Permissive Operation	0.5	N/A
$1.10 < V \leq 1.15$	Permissive Operation	1	N/A
$0.88 \leq V \leq 1.10$	Continuous Operation	Infinite	N/A
$0.70 \leq V < 0.88$	Mandatory Operation	Linear slope of 4 s/1 p.u. voltage starting at 0.7 s @ 0.7 p.u.: $T_{VRT} = 0.7\ \text{s} + \frac{4\ \text{s}}{1\ \text{p.u.}}(V - 0.7\ \text{p.u.})$	N/A
$0.50 \leq V < 0.70$	Permissive Operation	0.16	N/A
$V < 0.50$	Cease to Energize[a]	N/A	0.16

Table 2.4: DER response (shall trip) to abnormal frequencies for DER (IEEE 1547, 2018)

Shall trip function	Default settings[a]		Ranges of allowable settings[b]	
	Frequency[c] (Hz)	Clearing time (s)	Frequency (Hz)	Clearing time (s)
OF2	62.0	0.16	61.8–66.0	0.16–1 000.0
OF1	61.2	300.0	61.0–66.0	180.0–1 000.0
UF1	58.5	300.0[c]	50.0–59.0	180.0–1 000
UF2	56.5	0.16	50.0–57.0	0.16–1 000

Table 2.5: Frequency ride-through requirements of DER (IEEE 1547, 2018)

Frequency range (Hz)	Operating mode	Minimum time (s) (design criteria)
$f > 62.0$	No ride-through requirements apply to this range	
$61.2 < f \leq 61.8$	Mandatory Operation[a]	299
$58.8 \leq f \leq 61.2$	Continuous Operation[a,b]	Infinite[c]
$57.0 \leq f < 58.8$	Mandatory Operation[b]	299
$f < 57.0$	No ride-through requirements apply to this range	

Tripping large DGs from the grid because of voltage or frequency disturbances may result in power system stability problems. Tripping DGs may affect the voltage and frequency of the grid and lead to the tripping of nearby power generators. Fault ride-through capabilities for grid-connected DGs that can control active and reactive power during transient conditions have been proposed by utilities. During a grid disturbance, the voltage ride-through (VRT) and frequency ride-through (FRT) of the DGs can help stabilise the power system. Figure 2.22 shows the typical boundaries of the voltage ride-through (VRT). The green area indicates the region in which the DG is allowed to operate, where the high-voltage ride-through (HVRT) and low-voltage ride-through (LVRT) are the top and lower areas, respectively. To provide the necessary

reactive power to assist with voltage stability, the DG must remain connected to the grid for the recommended time during a fault (Bansal *et al.,* 2017).

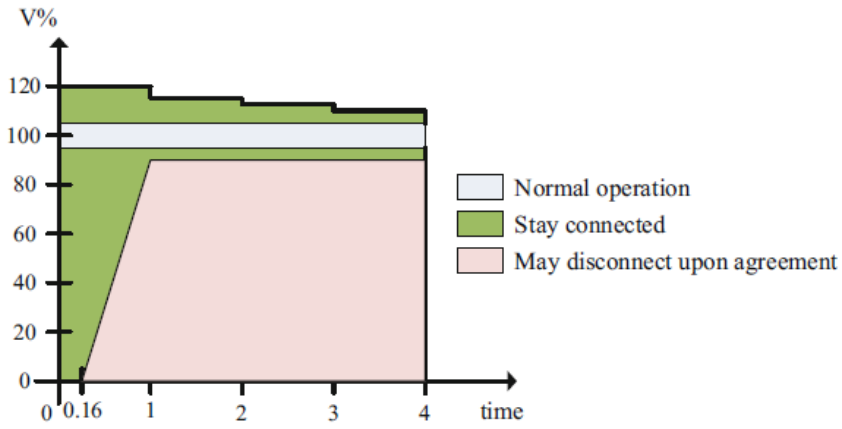

Figure 2.22: **Typical voltage ride-through requirements (Bansal et al., 2017)**

2.6 IEC 61850 Standard for substation automation

2.6.1 Introduction

The IEC 61850 standard is an international standard for Ethernet communication within substations. It establishes a communication protocol between IEDs and integrates all protection, control, measurement, and monitoring functions within the substation. This standard has been introduced into the industry to allow the interoperability of substation devices from different manufacturers (Alstom Grid, 2011). Generic Object-Oriented System Event (GOOSE) messages containing information such as trip signals and a change in status are used to communicate messages between IEDs. Sampled values (SVs) are used to send current and voltage sampled values between IEDs, while COMTRADE files record event data (Hussain and Kim, 2016).

Advanced protection schemes can be obtained through the exchange of data between the utility and the DG. To exchange data, communication equipment and channels are required. Fibre, pilot wire, or an internet-based network is the communication medium for the IEC GOOSE messages that are exchanged between IEDs. Communication-assisted protection schemes that are required for the integration of DG units into the grid occur between IEDs in multiple bays over the logical interface number 8, as shown in Figure 2.23. Communication between the IEDs at the process bus and bay levels is required through the logical interface shown by numbers 4 and 5 in Figure 2.23 (Bansal et al., 2017).

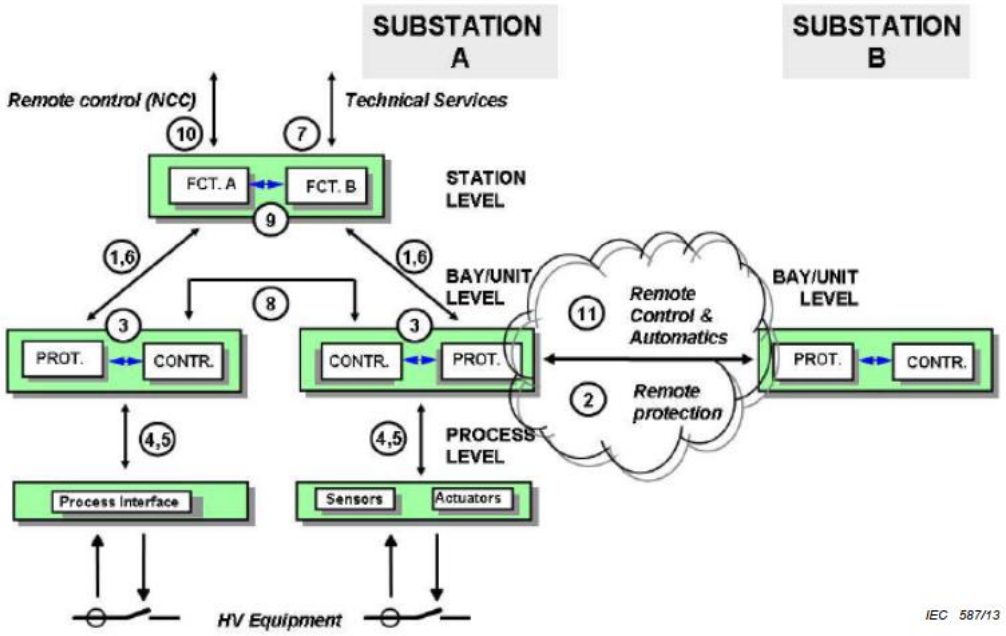

Figure 2.23: **Logical interface in substation automation systems (IEC 68150-1, 2013)**

The functions of the interfaces in Figure 2.23 are as follows:

1. Protection-data exchange between bay and station level.
2. Protection-data exchange between bay level and remote protection
3. Data exchange within the bay level
4. CT and VT instantaneous data exchange between process and bay level
5. Control-data exchange between process and bay level
6. Control-data exchange between bay and station level
7. Data exchange between the substation level and a remote engineer's workplace
8. Direct data exchange between the bays
9. Data exchange within the station level
10. Remote-controlled data exchange between substation devices and a remote network control centre

The IEC 61850 standard consists of 10 parts, as summarised in Table 2.6 below.

Table 2.6: **Different part numbers of the IEC 61850 standard (IEC 61850-1:2013)**

IEC 61850 standard part #	Title
1	Introduction and overview
2	Glossary

3	General requirements
4	System and project management
5	Communication requirements for functions and device models
6	Configuration description language for communication in electrical substations related to IEDs
7-1	Basic communication structure – Principles and models
7-2	Basic information and communication structure – Abstract communication service interface (ACSI)
7-3	Basic communication structure – Common data classes
7-4	Basic communication structure – Compatible logical node classes and data object classes
7-410	Hydroelectric power plants – Communication for monitoring and control
7-420	Basic communication structure – Distributed energy resources logical nodes
7-5	IEC 61850 – Modelling concepts
7-500	Use of logical nodes to model functions of a substation automation system
7-510	Basic communication structure – Hydroelectric power plants – Modelling concepts and guidelines
7-520	Use of logical nodes to model functions of distributed energy resources
8-1	Specific communication service mapping (SCSM) – Mappings to MMS (ISO 9506-1 and ISO 9506-2) and ISO/IEC 8802-3 Guidelines
80-1	Guideline to exchanging information from a CDC-based data model using IEC 60870-5-101 or IEC 60870-5-104
9-2	Specific communication service mapping (SCSM) – Sampled values over ISO/IEC 8802-3
90-1	Use of IEC 61850 for the communication between substations
90-2	Using IEC 61850 for the communication between substations and control centres
90-3	Using IEC 61850 for condition monitoring
90-4	Network Engineering Guidelines - Technical report
90-5	Using IEC 61850 to transmit synchrophasor information according to IEEE C37.118
10	Conformance testing

2.6.2 Benefits of the IEC61850 standard

Some of the major benefits of implementing the IEC 61850 standard into a power system include:

- IEC 61850 allows IEDs to exchange data using GOOSE through the station LAN without having separate wires going to each IED. This reduces the installation cost by reducing the wiring that is required.
- The digital measurements from a single merging unit can be published to several IEDs over the IEC 61850-based communication network.

- Reduced commissioning cost as IEC 61850 compatible devices do not require a lot of manual configurations. Most of the applications only require configuring the network address of the devices.
- Reduced cost of equipment migration due to the standardised naming of the device.
- Adding new IEDs to an existing IEC 61850-based network can be achieved with little impact on the existing equipment, which reduces the extension cost.
- IEC 61850 networks can send data without a separate communication front-end or reconfiguring device. This reduces the integration cost.
- IEC 61850 enables new and innovative applications that can be implemented due to all the data associated with a substation being available at the LAN in a standard format that can be accessed using standard protocols (Alstom Grid, 2011).

2.6.3 IEC 61850 Substation Configuration Language (SCL)

IEC 61850 describes an SCL to allow for the exchange of the device description and system parameters between IEDs from different manufacturers. The language allows:

- System functional specification
- IED capability description
- Power utility automation system description (IEC 61850-1, 2013).

The IEC 61850-6-1 specifies an XML-based SCL to define the configuration of IEC 61850 standard-based IEDs. The SCL defines a hierarchy of configuration files that allows for the description of the following different levels:

- System specification description (SSD)
- IED capability description (ICD)
- Substation configuration description (SCD)
- Configured IED Description (CID)
- System exchange description (SED)
- Instantiated IED description (IID)

Some of the benefits of having an off-line description language other than IEC 61850 applications for the configuration of an IED are:

- SCL allows for the offline development of the files that are required for the IED configuration from the power system design phase and reduces the cost of the IED configuration.
- SCL allows for the sharing of the IED configuration files between users and manufacturers. Users can use their own SCL configuration for the IEDs based on their requirements.

- SCL allows for the offline configuration of the IEC 61850 applications that are required for the IED.

Figure 2.24 shows the workflow for the SCL configuration files in an IEC 61850 application (Alstom Grid, 2011).

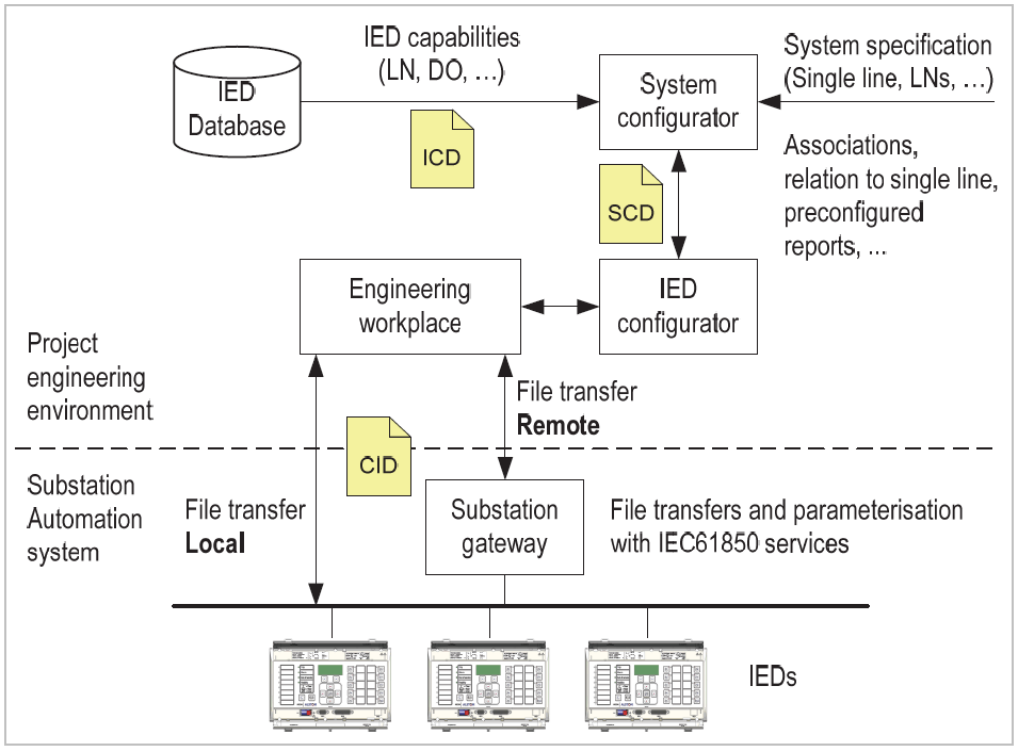

Figure 2.24: IEC61850 Project configuration (Alstom Grid, 2011)

2.6.4 IEC 61850 standard-based Generic Object-Oriented System Event (GOOSE) messages

The use of the IEC 61850 GOOSE message enables high-speed communication between IEDs. This makes it possible to implement substation protection, interlocking control systems, and distributed control systems. The GOOSE message provides a fast and reliable exchange of data between IEDs. The IEDs at the remote end require a mechanism to manage the received GOOSE messages. The GOOSE message contains data and additional information, such as the status number and sequence number parameters. The use of these parameters allows IEDs at the remote end to determine whether the message received contains new data. This allows IEDs to filter the GOOSE messages, thereby saving time. GOOSE messages are exchanged on a publisher/subscriber mechanism using multicast. GOOSE messages are repeated until there is a change in state (Cigre 540, 2013).

2.6.5 IEC 61850 logical nodes

The IEC 61850 information model is divided into physical and logical devices. As shown in Figure 2.25, a physical device can be broken down into logical devices, and a logical device can be broken down into logical nodes, data objects, and attributes. The logical device is the first functional level supported by the physical device. A logical device cannot be used in more than one IED and must only be used by a single IED. As shown in Table 2.7, a logical device consists of a group of logical nodes that contain automation, protection, and other functions (IEC 61850-1, 2013).

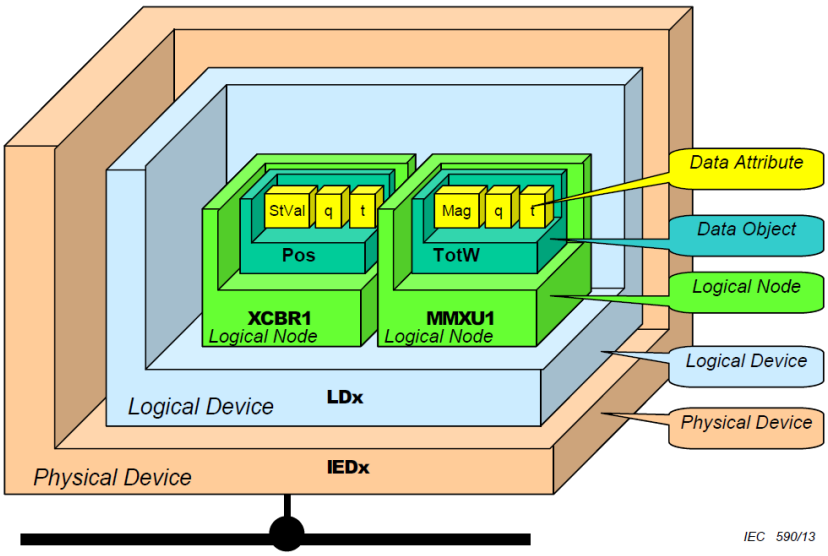

Figure 2.25: IEC 61850 data modelling (IEC 61850-1, 2013)

Table 2.7: LN Groups (IEC 61850-7-4, 2010)

Group indicator	Logical node groups
A	Automatic control
B	Reserved
C	Supervisory control
D	Distributed energy resources
E	Reserved
F	Functional blocks
G	Genetic functions references
H	Hydropower
I	Interfacing and archiving
J	Reserved
K[a]	Mechanical and non-electrical primary equipment
L	System logical nodes
M	Metering and measurement
N	Reserved
O	Reserved
P	Protection functions
Q	Power quality events detection related

R	Protection related functions
S[a]	Supervision and monitoring
T[a]	Instrument transformer and sensors
U	Reserved
V	Reserved
W	Wind power
X[a]	Switchgear
Y[a]	Power transformer and related functions
Z[a]	Further (power system) equipment
An LN of this group exists in dedicated IEDs if a process bus is used. Without a process bus, LNs of this group are the I/O in the hardwired IED one level higher (for example in a bay unit).	

The IEC 61850 standard is used to read data, write data, control devices, report events, and record events. A hierarchical data model for the circuit breaker is shown in Figure 2.26. The IEC 61850 standard contains basic objects known as logical nodes (LN). The group to which the LNs belong depends on the function of the data objects (DOs) belonging to the LN. DOs consist of attributes that contain detailed information about the data objects. The names of LNs, DOs, and attributes are standardized in the IEC 61850 standard, whereas the names of LDs and IEDs are not (Hussain and Kim 2016).

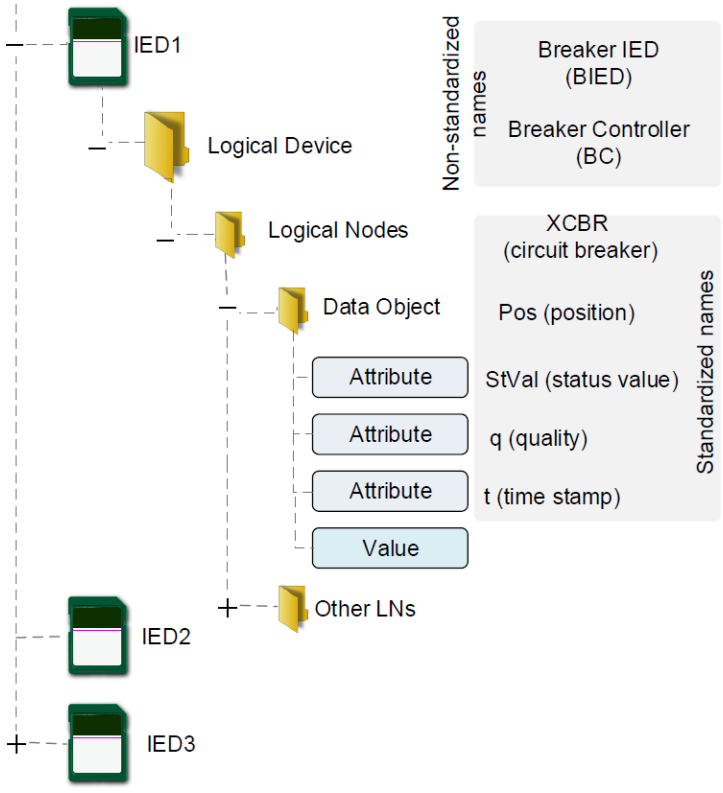

Figure 2.26: IEC 61850 data model (Hussain and Kim, 2016)

2.6.6 IEC 61850 standard-based protection schemes

Conventional overcurrent protection schemes used in radial distribution networks cannot be used for MG protection schemes. As a result of the addition of DGs, the power flow becomes bidirectional and may lead to a loss of coordination when using conventional overcurrent protection schemes. In the case of MG protection schemes, directional overcurrent protection relays must be implemented.

The IEC 61850 standard is implemented in the MG protection scheme to improve fault clearing times. GOOSE messages containing information on the fault direction and breaker status are transmitted between the protection IEDs. This reduces the complexity of protection coordination between IEDs, reduces the time needed to isolate a fault, and helps solve problems related to MG protection schemes. The IEC 61850 GOOSE message enables fast transmission of object changes between substation IEDs. The transmitted GOOSE messages are short, allowing fast encoding and decoding. In addition to this message, a publisher/subscriber mechanism is embedded. The publisher/subscriber mechanism is implemented using an Ethernet connection between the IEDs. High-speed peer-to-peer GOOSE messages can be exchanged directly between the IEDs, allowing the IEDs to perform logic operations and transmit commands directly without the need for a SCADA platform. This configuration can reduce the installation cost (Gu et al., 2019).

The application of IEC 61850 GOOSE in distribution protection schemes improves the performance of distribution protection schemes and reduces the time required to clear the fault. It is possible to reduce the impact of short-circuit faults by combining all available protection functions of the protection IED with the exchange of GOOSE messages between the protection IEDs. When a feeder fault (F1 in Figure 2.27) occurs in a selective backup tripping protection scheme, the feeder protection IED detects the fault. This feeder fault can also be detected by an IED located at the transformer. The feeder IED publishes a GOOSE message to the transformer protection IED, indicating a feeder fault. As soon as the transformer protection IED receives the GOOSE message, the overcurrent element protecting the bus will be blocked from operating.

The feeder IEDs do not detect a fault current on the bus (F2 in Figure 2.27). In such a case, the transformer protection IED does not receive a GOOSE message from any feeder IED. It will indicate to the transformer protection IED that there is a fault on the bus, and it will send a signal to the circuit breaker located at the transformer protection IED.

In the Sympathetic Trip scheme, IEDs located in adjacent feeders are prevented from operating during a feeder fault. As soon as a feeder IED detects a feeder fault, it sends a GOOSE signal to the feeder IEDs located adjacent to the feeders and informs them of the inrush current. These IEDs are blocked from operating after receiving the GOOSE message for the expected period of the inrush current (Apostolov & Vandiver 2011).

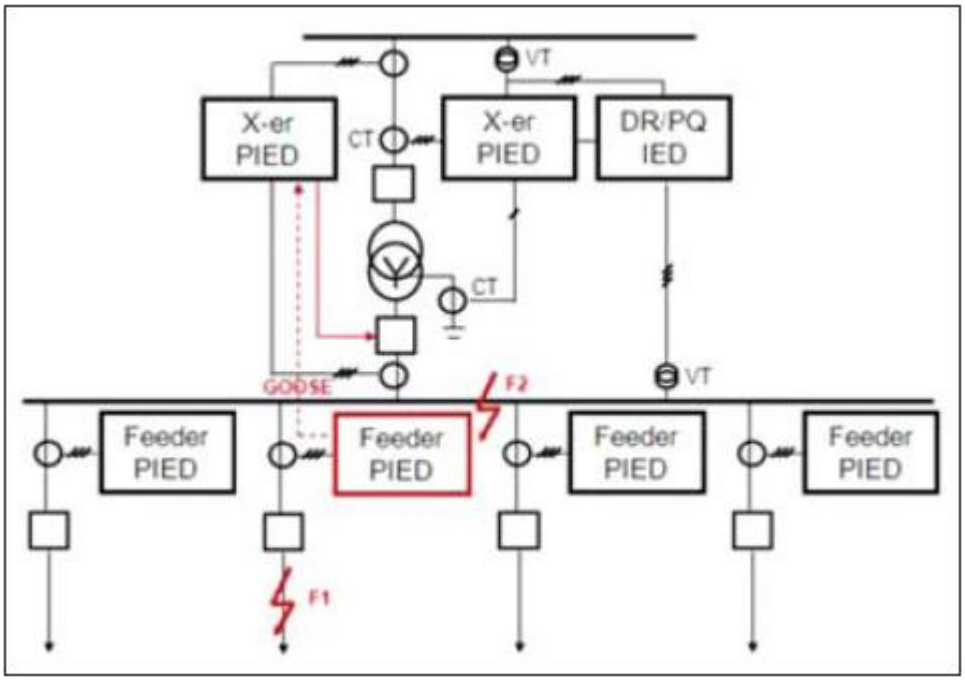

Figure 2.27: **Peer-to-peer communication-based distributed bus protection (Apostolov & Vandiver, 2011)**

According to Hussain and Kim (2016), an IEC 61850 framework is required to implement a hybrid adaptive protection scheme, as shown in Figure 2.28. This will allow interoperability between the developed DERs. A gateway is used for the exchange of information between the IEC 61850 standard-based IEDs. The MGCC is located at the station level, and the process-level IEDs function as local controllers. Local controllers can communicate with devices at other levels through the relevant gateway. IEC 61850-7-420 is used to define the LNs for the MG. The IEC 61850 standard-based IEDs from the gateway and the process bus exchange a message containing trip commands, lock instructions, and other data (sampled current and voltage values). Bay-level IEDs perform the functions defined for merging units and input/output units. The IEDs connected to the bus are configured to subscribe to the published IEC 61850 standard-based GOOSE message (Hussain and Kim, 2016)

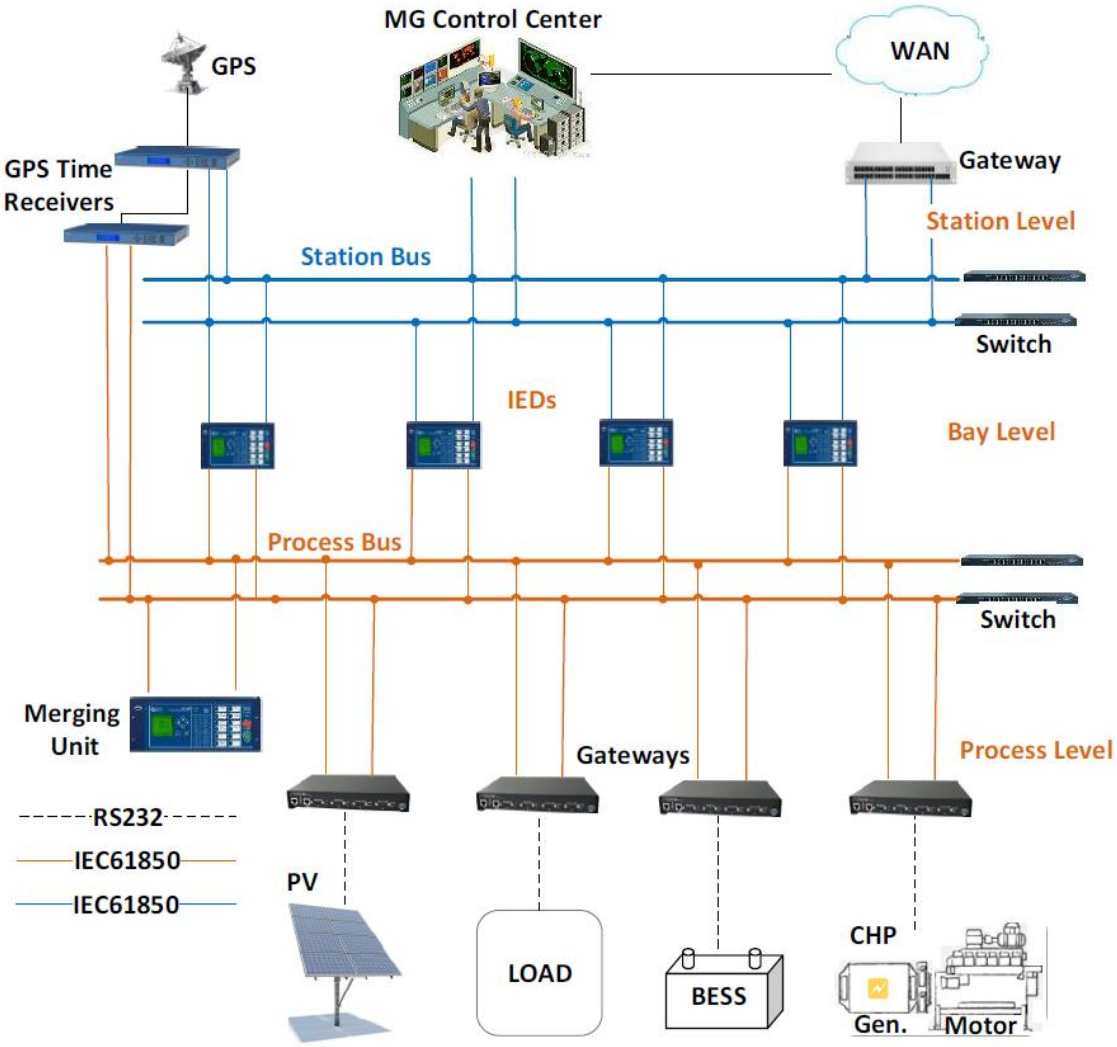

Figure 2.28: Architecture for the implementation of the hybrid adaptive protection scheme through the IEC 61850 standard-based IEDs (Hussain and Kim, 2016)

Table 2.8: Summary of IEC 61850 standard-based protection schemes

Paper	Aim	Method used	Communication and Protocol	Simulation/ hardware implementation	Benefits
Gu et al., 2019	Implementation of the IEC 61850 standard-based GOOSE message for the MG protection scheme.	Real-time SCADA platform based on the IEC 61850.	IEC 61850-7-4 GOOSE message	ETAP power system simulation software and SCADA platform.	Implementation of the IEC 61850 GOOSE message between IEDs improves the fault clearing times.
Apostolov & Vandiver, 2011	IEC 61850 GOOSE applications to distribution protection schemes	Distribution bus protection, Sympathetic trip logic and selective backup tripping.	IEC 61850-7-4 GOOSE message	Software tool for configuration of IEC 61850 GOOSE message between IEDs	IEC 61850 communication-based distribution bus protection provides fast fault clearing times for distribution bus faults.
Hussain and Kim, 2016	Implementation of a hybrid adaptive protection scheme through the IEC 61850	Adaptive protection scheme	IEC 61850-7-4 GOOSE message	Modelling and fault analysis of the network in a power system simulation software package.	Allows for the interoperability and exchange of information between IEC 61850 compliant devices from different manufacturers.
Ge et al. (2021)	To address the need for feeder topology information exchange the distribution network.	Development of a feeder model as a container of the equipment along the distribution line. This method involves	IEC 61850 GOOSE message	IEEE 13-bus system used as an experimental environment to verify the effectiveness of the proposed method.	Enables exchange of topology information between the IEDs. The method is adaptable to different network topologies.

		adding new logical nodes to describe the physical and logical connection between the devices.			
Penthong et al., 2023	Propose an IEC 61850 standard-based protection scheme to enhance network reliability, service quality and availability.	GOOSE message for exchange of information between IEDs.	IEC 61850 GOOSE message	The developed IEC 61850 standard-based protection scheme is tested in hardware-in-the-loop (HIL) protection testing using RTDS and multi-vendor IEDs.	The scheme enhances the reliability and selectivity of the protection system. The developed HIL platform allows for testing interoperability between multi-vendor IEDs.

2.7 Protection schemes for microgrids

An adaptive protection scheme is a protection philosophy that seeks to adjust the protection functions of the relays based on the power system conditions. The fault current depends on the available sources in the network. Therefore, when the MG operates in island mode, the fault currents measured by the protection relays are lower than those measured in grid-connected mode. Traditional distribution networks have a radial topology with a unidirectional power flow. The addition of DGs to the network causes the power flow to be bidirectional. In addition to other factors, such as the intermittent nature of DGs and the change in fault current contribution between grid-connected and island modes of operation, a complex fault current path results. This means that traditional protection schemes are ineffective and cannot therefore be applied to networks containing DGs.

Some of the following issues can occur for MG protection schemes:

i. Change in fault current: MGs can operate in either grid-connected or island mode, and the fault current measured by the protection relays is less during island mode when compared to the grid-connected mode of operation.
ii. Blinding of protection: The fault current measured by a protection relay changes due to the presence of DGs, causing the misoperation of the protection relay.
iii. False tripping: This will occur when a feeder protection relay initiates a trip for a fault occurring in an adjacent feeder due to the presence of DGs. This will cause the healthy feeder circuit to be disconnected from the rest of the MG.
iv. Unsynchronized and automatic reclosing: When an MG is connected to the grid through a recloser, synchronisation between the MG and the grid needs to be considered. Reconnection of a faulted section without synchronisation can cause damage to the DGs connected. The issue of the failed reclosing can be addressed by disconnecting the faulted DG sources from the feeder circuits before the reclosure operation occurs. The DGs must be disconnected based on the voltage and frequency requirements as per the IEEE 1547:2018 standard (Barra, Coury and Fernandes, 2020).

The addition of DGs to the MG may cause some challenges when considering the design of the protection system. The DGs cause the power flow to be bidirectional, which may result in a loss of coordination between the overcurrent protection relays. Conventionally, islanding detection methods are used to disconnect the entire

DG from the grid based on the IEEE 1547 standard requirements. The fault current contribution is higher in the grid-connected mode than in the island mode. Conventional overcurrent protection relays will only detect higher fault currents in the grid-connected mode and not in the island mode. An adaptive overcurrent protection scheme has been proposed in which the microgrid controller can monitor the change in generation and load and automatically adjust the relay characteristics based on the network conditions (Bansal et al., 2017).

Some of the proposed protection system-based strategies include the application of fault current limiters (FCLs) to improve the fault ride-through capabilities (FRT) of the DG and the application of protection schemes such as distance, differential, and directional overcurrent. To improve the performance of the protection system, another strategy is to apply communication systems based on the IEC 61850 standard. An adaptive coordination-protection scheme has been proposed in which the operation conditions are based on an impedance matrix along with a limited number of predefined group settings configured on the protection relays (Bisheh, Fani and Shahgholian, 2021).

Protection relays located at the DG sources are used to protect against internal short-circuit faults and abnormal fault conditions such as reverse power flow. Table 2.9 lists the protective elements required to protect IEDs located at the DG source. Interconnection protection is located at the PCC and the main step-up transformer. To prevent unintentional islanding of the DG units, interconnection protection is necessary once the circuit breaker located at the PCC has disconnected the DG due to a fault. This prevents the DG sources from continuing to supply the fault current. Table 2.10 lists the protection elements used for the protection of IEDs located at the PCC (Bansal et al., 2017).

Table 2.9: Protection elements used for the protection relays located at the DG sources (Bansal et al., 2017)

Functionality	Protection device
Fault backfeed protection	Voltage-constrained inverse time overcurrent (51 V)
Abnormal flow of power	Directional power (32)
System restoration	Synchronism check (25)
Unbalanced current and phase reversal conditions	Negative sequence current/voltage (46/47)
Overcurrent condition	Differential (87)
Loss of field protection	Offset mho impedance (40) relay
Field faults	Generator field ground (64 F) relay

Table 2.10: **Protection elements used for the protection relays located at the PCC (Bansal et al., 2017)**

Functionality	Protection device(s)
Loss of parallel operation (loss of mains)	Over/under voltage (59/27), Over/under frequency (81 O/U), ROCOF (81R), Loss of Mains (LOM)
Fault backfeed protection	Voltage-constrained inverse time overcurrent (51 V), directional overcurrent (67), distance (21)
Abnormal power flow protection	Directional power (32)
System restoration	Synchronism check (25)
Preventing the reconnection of the DG to a de-energised utility	Voltage check (27)
Unbalanced current/phase reversal conditions	Negative sequence current/voltage (46/47)

Considering the network shown in Figure 2.29, if a fault occurs on the feeder circuit, the feeder protection IED and transformer IED will detect a fault (F1). To ensure coordination within the network, the feeder protection IED must initiate a trip and isolate the faulty circuit from the rest of the MG before the transformer IED initiates a trip. In the event that the transformer IED initiates a trip first, the entire MG will be disconnected from the grid. If a fault occurs on the bus, both the feeder protection IED and the transformer IED will detect the fault current (F2). In such an event, only the transformer protection IED must operate (Bansal et al., 2017).

Directional comparison protection schemes based on communication infrastructures allow the exchange of signals between protection IEDs, which improves the time required to clear faults compared with transformer backup protection schemes. The transformer protection IED is configured such that it subscribes to the GOOSE message published by the feeder directional overcurrent protection IED located at one of the feeder circuits. The feeder-protection IED detects the fault current (F1) in the forward direction, whereas the other feeder-protection IEDs detect the fault current in the reverse direction. The feeder protection IED is configured to publish a GOOSE message, whereas the transformer protection IED is configured to subscribe to a GOOSE message indicating a feeder fault (external fault to the bus). The transformer protection IED should be blocked from operating, and time coordination between the protection IEDs should be ensured before initiating a trip and disconnecting the entire DG from the grid. In the case of a fault (F2) occurring on the bus, the feeder protection IED will detect a reverse fault current. In this case, the transformer protection IED will not receive a GOOSE message from any of the feeder protection IEDs, indicating that the fault is occurring on the bus, and is configured to publish a GOOSE message to

all feeder protection IEDs to initiate a trip signal and disconnect all circuit breakers connected to the bus (Bansal et al., 2017).

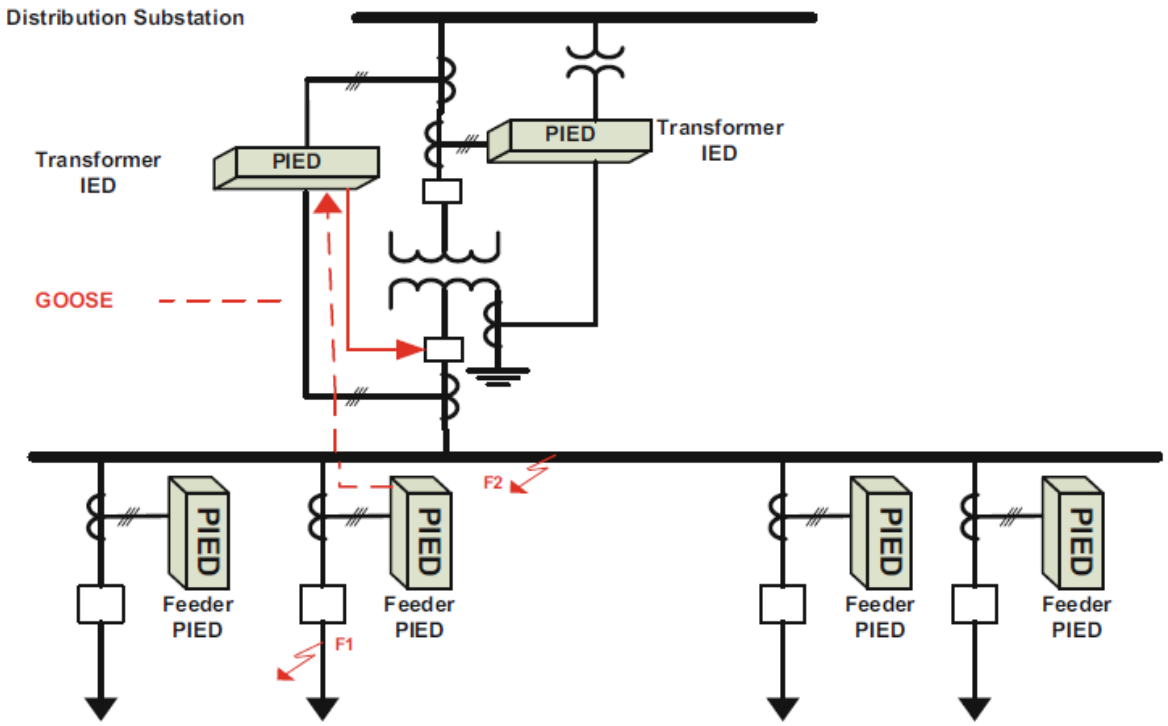

Figure 2.29: **Directional comparison distribution bus protection scheme (Bansal et al., 2017)**

Most adaptive protection schemes implemented in the industry use the setting groups that are available for protection IEDs. The MGCC monitors the status of each circuit breaker to identify the network topology and update the setting groups of each protection IED according to the mode of operation. To determine the protection settings to be applied for the protection of IEDs, it is necessary to conduct offline fault and coordination studies. The IEC 61850 GOOSE message may be transmitted from the MGCC to the protection IEDs to update the setting group, depending on the mode of operation. (Bansal et al., 2017).

The adaptive protection scheme can respond to MG fault conditions by changing the protection settings of the protection IEDs. This can be achieved through a communication infrastructure between the protection relays. The protection relays require several group settings along with directional overcurrent protection. Adaptive protection schemes can be either centralised or decentralised. A centralised adaptive protection scheme, as shown in Figure 2.30, consists of local controllers that send GOOSE messages to the central controller. If a change in network configuration

or device status is detected, the central controller calculates the new protection settings required for all protection relays and informs the local controllers.

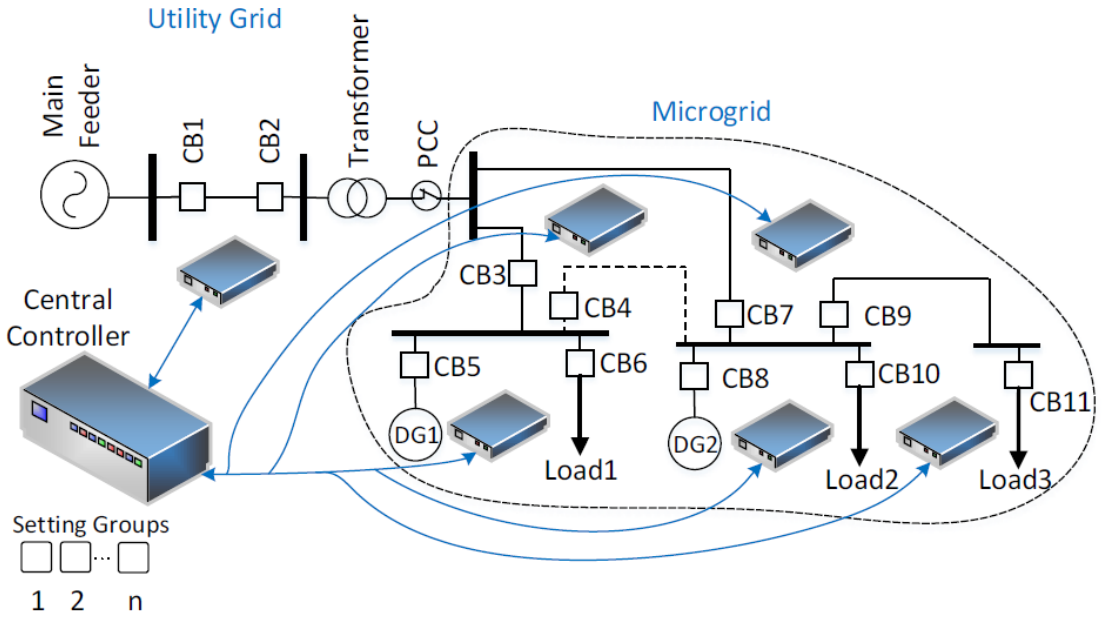

Figure 2.30: **Centralized adaptive protection scheme for an MG system (Hussain and Kim, 2016)**

As shown in Figure 2.31, a decentralised adaptive protection scheme consists of local controllers that send GOOSE messages to adjacent controllers. Each local controller is configured to respond to the received GOOSE messages. The local controller communication structure is implemented over the bus of an Ethernet network (Hussain and Kim, 2016).

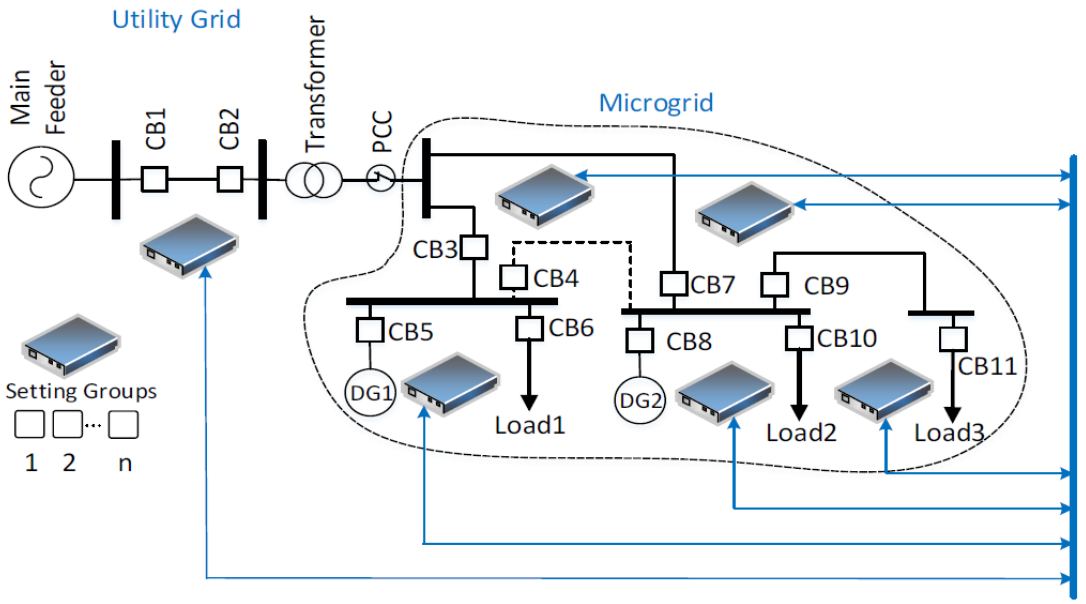

Figure 2.31: **Decentralized adaptive protection scheme for an MG system (Hussain and Kim, 2016)**

The communication-based protection scheme implemented between numerical protection relays consists of two stages: topology sensing and the calculation of protection settings. The topology-sensing-stage analysis of the network configuration is based on the information received from the devices within the network, such as the breaker status, penetration level of DG units, and other grid parameters. The trip signal from the relay located at the fault is published to the MGCC during the fault condition. In the next stage, the MGCC analyses the data, reviews the protection settings for each protection relay, and adapts if selectivity is no longer available. If the boundary conditions are successfully met, the tripping characteristics of each of the protection relays are updated. The application of the IEC 61850 GOOSE messages between protection IEDs allows real-time communication. Once a change in the state occurs, the GOOSE message is published or received at a high repetition rate within a few milliseconds. The MGCC continuously monitors the network topology of the MG using the information it receives about the status of the circuit breakers. The protection relays will update the MGCC in the event of a measured fault current contribution. The operating fault current for any of the protection relays is calculated using the following equation:

$$I_{relay} = (I_{fault(Grid)} \times OM) + \Sigma(k_i \times I_{fault(DG)} \times SB)$$

Equation 2.7

where:

N = Total number of DGs

OM = Operating mode

SB = Status of circuit breaker

k_i = Impact factor of the n^{th} distributed generator on the fault current that is measured by the relay

The contribution of the fault current that is supplied by the grid is calculated using Thevenin's equivalent circuit of the network (Shah, Goli and Shireen, 2018).

Table 2.11: Summary of MG protection schemes

Paper	Aim	Method used	Protection	Simulation/ hardware implementation	Benefits/ disadvantages
Bansal *et. al,* 2017	Implementation of a directional comparison protection scheme.	IEC 61850 standard-based GOOSE message.	Directional overcurrent protection (67).	Application of the IEC 61850 GOOSE message between the feeder protection IEDs and the transformer protection IED.	Only the faulted feeder is disconnected from the MG during a feeder fault. Allows for time coordination between the feeder protection IED and transformer protection IED.
Hussain and Kim, 2016	Implementation of an adaptive protection scheme.	Centralized adaptive protection scheme.	Directional overcurrent protection (67).	IEC 61850 GOOSE message application between the central controller and local controllers.	Can be implemented using any type of communication structure (i.e., serial communication, Ethernet network etc.).
Hussain and Kim, 2016	Implementation of an adaptive protection scheme.	Decentralized adaptive protection scheme.	Directional overcurrent protection (67).	IEC 61850 GOOSE message application between local controllers.	The communication structure is required to be implemented over a bus of an Ethernet network.
Shah, Goli and Shireen, 2018	A novel adaptive protection scheme using numerical relays that are compatible with the IEC 61850 standard.	IEC 61850 standard-based GOOSE message.	Directional overcurrent protection (67).	The IEEE 13-bus system is modelled in ETAP software to perform the protection coordination study with and without PV or wind power sources. A laboratory-based MG test bed is modelled with LNs based on the IEC 61850 communication protocols to	The adaptive protection scheme changes the relay settings in real-time under varying DG penetration levels, ensuring effective protection coordination between the protection relays. The adaptive protection scheme uses numerical relays compatible with the IEC 61850 standard,

				implement the proposed adaptive protection scheme.	allowing easier integration with other IEDs.
Abbaspour, Fani and Karami-Horestani, 2021,	Adaptive protection scheme for protecting renewable-dominated MGs against changes in the network topology.	Protection algorithm that employes overcurrent relays with the capabilities of IEC 61850 protocol. The algorithm is applied within a peer-mode multiagent system (MAS) structure.	Overcurrent protection (50 and 51)	The protection scheme is simulated using the ETAP software environment. ETAP is used for offline simulations, whereas the MATLAB environment plots the relays' current waveform generated from ETAP simulations.	The proposed protection scheme is designed to adapt independently to possible network topology changes, allowing it to respond to dynamic conditions with renewable-dominated MGs effectively. The protection scheme improves the reliability of the MG protection with the implementation of the IEC 61850 protocol and MAS structure.
Vaithilingam *et al.*, 2018	The MG adaptive protection scheme proposes an Arduino-based adaptive protection using wireless communication for MGs with RESs.	The Arduino processor is programmed using calculated fault current for different operating conditions.	Overcurrent protection (50 and 51)	The hardware setup includes a three-way regulated power supply module representing three sources. An Arduino Uno microcontroller is used to measure the voltage values from the three sources and formulate current values to check for fault current conditions. The fault current status is communicated between microcontrollers via Bluetooth modules.	The proposed protection scheme responds rapidly to the dynamic current conditions. The proposed protection scheme provides selective and fast protection through the use of wireless communication protocols and dynamically changing the relay settings based on the operating conditions.

Adewole *et al.*, 2023	The protection scheme for the MG with DERs proposes a centralised protection and control (CPC) architecture.	The CPC architecture for MGs is implemented by interfacing the process-level instrument transformers and Intelligent Merging Units (IMUs) at the MGs directly to the station-level CPC (CISP) over a communication network. The CISP approach utilises an adaptive protection algorithm to dynamically determine protection zones and select appropriate protection settings based on the network topology and operating conditions.	Supervised current differential (SCD), Rate-of-Change of Current (ROCOC), and Voltage-controlled ROCOC (V-ROCOC) algorithms.	The CISP is demonstrated through real-time simulations using the Real-Time Digital Simulator (RTDS) testbed. The real-time simulations using the RTDS testbed enables the validation of the centralised protection algorithm under various system configurations.	The CISP platform eliminates the need for several local relays and provides a reliable adaptive protection algorithm that is centrally coordinated. The proposed CISP platform utilises communication protocols such as IEC 61850 GOOSE and Sampled Values (SVs) in MGs to improve the overall efficiency, security, and dependability of the protection scheme.
Ataee-Kachoee, Hashemi-Dezaki and Ketabi (2022)	The optimised adaptive protection scheme proposes using high set relays and a genetic algorithm to reduce the coordination constraints.	The genetic algorithm (GA) is used to find the optimal solution for the adaptive protection scheme.	Directional overcurrent relays (DOCRs) with high-set relays.	Power system analysis is conducted in DIgSILENT and exported to MATLAB for further analysis.	Simultaneous optimisation of time and current settings of the DOCR relays. Different operation modes and network configurations considered. Proposed protection scheme validated during DIgSILENT simulations.

	A coordinated adaptive protection scheme for protecting AC MGs during grid-connected and islanded modes.	To develop and offline and online algorithm for the adaptive setting and coordination of the protection relays.	Various relays such as DOCRs, direction UVR, directional negative sequence current OCRs.	Adaptive protection algorithm is developed to switch the protection relay's automatically.	Online adaptive protection algorithm ensures fast and reliable operation for various network topologies, while providing selective coordination between the protection relays.
Srivastave and Parida, 2020	Adaptive relaying scheme for online update of relay setting using smart sensing devices and communication links in MGs.	Use of a processor-based computer system for online update of relays settings based on the operating mode and network topology.	Numerical directional overcurrent relays (NDOCRs)	No specific software Formation of the relay coordination problem as a non-linear optimisation function.	The scheme enables the dynamic update of the relay settings based on the operating mode and network topology. The use of inclusive mode settings provides a novel measure to maintain relay coordination.

CHAPTER 3
MODELLING, LOAD FLOW ANALYSIS, FAULT AND PROTECTION STUDY OF THE MICROGRID SYSTEM

3.1 Introduction

DIgSILENT, short for "**DIg**ital **SI**mu**L**ation of **E**lectrical **N**e**T**works", is a computer-aided engineering tool for analysing transmission, distribution, and industrial electrical power systems. Power system engineers and researchers widely use it to model and simulate complex electrical networks. The programme offers a range of features, including load flow analysis, short circuit analysis, and dynamic stability analysis. Additionally, the software allows users to investigate the impact of renewable energy sources (RESs) that are integrated into the grid (DIgSILENT, 2022).

The 33 kV distribution network of the modified IEEE 14-bus system comprises a synchronous generator with a capacity of 100 MVA, two transformers with a capacity of 100 MVA each, eight transmission lines, and seven loads, as shown in Figure 3.1. The grid is a voltage source with the parameters provided in Table 3.1. The parameters for the two 100 MVA transformers are provided in Table 3.2. The parameters for the 100 MVA synchronous generator, Gen_0006, are presented in Table 3.3. The active and reactive power for the seven loads is provided in Table 3.4, and the parameters for the eight transmission lines are provided in Table 3.5. The integration of the 50 MW wind farm at the point of coupling (POC) in addition to the existing 100 MW synchronous generator, Gen_0006, enhances the overall reliability of the modified IEEE 14-bus system.

The objective of this chapter is to model and simulate the modified IEEE 14-bus system in the DIgSILENT software environment. This simulation includes the load flow analysis, short-circuit analysis and a coordination study for both grid-connected and islanded modes of operation. The grid-connected mode of operation occurs when the circuit breakers at the point of common coupling (PCC) are closed, while the islanded mode of operation occurs when the circuit breakers are open, as shown in Figure 3.1. The load flow and short circuit analysis results are used to calculate the pickup values for the phase time-overcurrent (51) and instantaneous overcurrent (50) settings for the SEL-351A relays. A coordination study is also investigated to ensure a sufficient grading margin between the primary and backup relays.

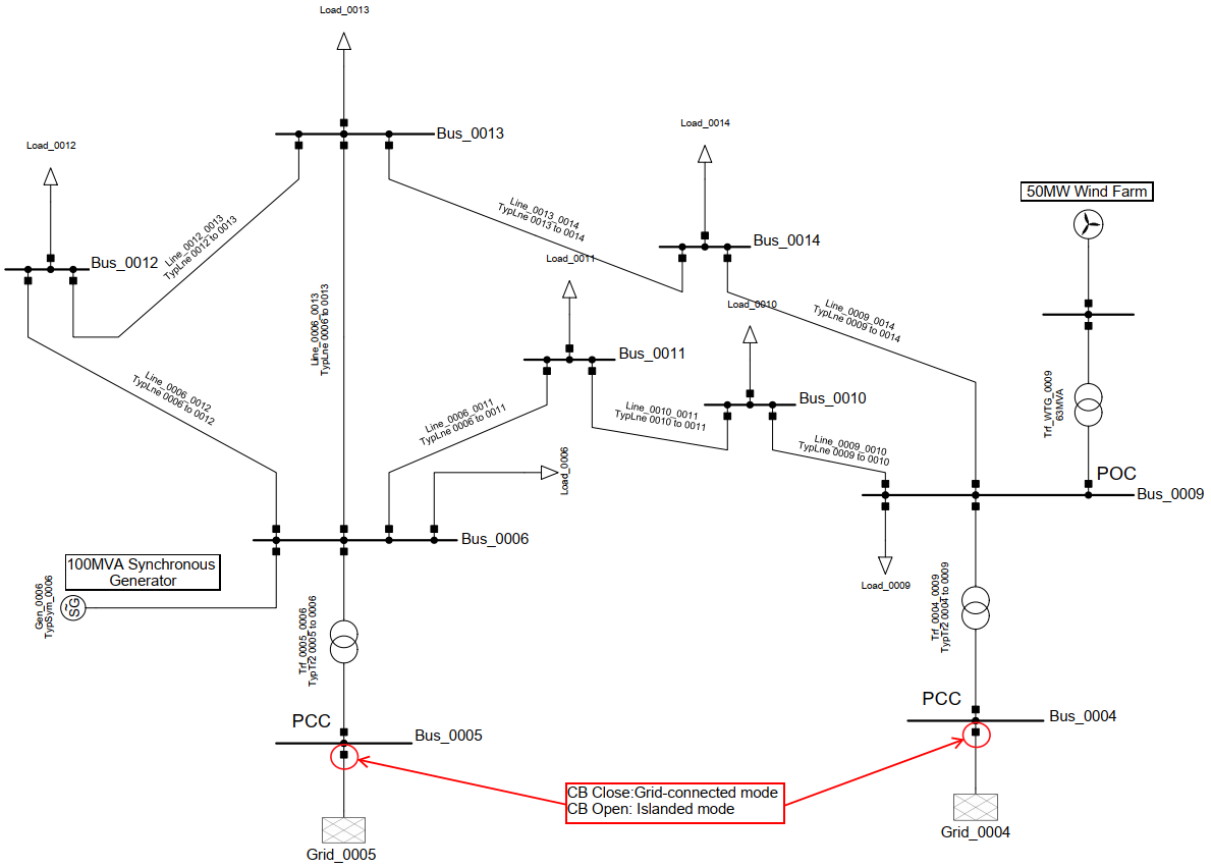

Figure 3.1: 33 kV distribution network of the IEEE 14 bus system

Table 3.1: Voltage source parameters

Description	Bus type	Voltage (kV)	Resistance (Ω)	Reactance (Ω)	X/R ratio
Grid_0004, Grid_0005	PV	132	0.173376	1.733753	10

Table 3.2: Transformer parameters

Description	Size (MVA)	Voltage (kV)	Vector Group	Impedance (p.u.)
Trf_0005_0006	100	132/33	YNyn0	0.25202
Trf_0004_0009	100	132/33	YNyn0	0.55618

Table 3.3: Generator parameters

Description	Bus type	Size (MVA)	Voltage (kV)	Power factor	Xd'' (p.u.)
Gen_0006	PV	100	33	0.9	0.2

Table 3.4: Load parameters

Description	Active Power (MW)	Reactive Power (Mvar)
Load_0006	11.2	7.5
Load_0009	29.5	16.6
Load_0010	9	5.8
Load_0011	3.5	1.8
Load_0012	6.1	1.6
Load_0013	13.5	5.8
Load_0014	14.9	5

Table 3.5: Transmission line parameters

Description	Rated Voltage (kV)	Impedance in polar form $Z\angle\delta$		Impedance in rectangular form $Z = R + jX$	
		Z1 (Ω)	δ (deg)	R1 (Ω)	X1 (Ω)
Line_0006_0011	33	2.400311	64.4743	1.034332	2.166021
Line_0006_0012	33	3.090643	64.3369	1.338490	2.785771
Line_0006_0013	33	1.591062	63.0789	0.720373	1.418640
Line_0009_0010	33	0.983249	69.3712	0.346410	0.920205
Line_0009_0014	33	3.253583	64.821	1.384228	2.944439
Line_0010_0011	33	2.274501	66.8684	0.893524	2.091643
Line_0012_0013	33	3.244373	42.1376	2.405819	2.176693
Line_0013_0014	33	4.222386	63.842	1.861428	3.789938

3.2 Load flow analysis of the modified IEEE 14-bus system without added RESs

The load flow results are used to ensure that the voltage at each bus is within the ±10% tolerance that is allowed in the IEEE 141 standard. The load flow results can be used to ensure that the equipment, such as the transformers and cables in the network, is not overloaded.

Load flow analysis is a method used to determine the voltage magnitude and phase angle at each bus in a balanced three-phase power system during steady-state conditions. Real and reactive power flows are also calculated for the equipment within the power system. The variables, such as voltage magnitude (V_k), phase angle (δ_k), real power (P_k), and reactive power (Q_k), are computed for each bus k, as shown in Figure 3.2.

Additionally, the delivered power to bus k is divided into generator and load components (Glover et al., 2017).

$$P_k = P_{Gk} - P_{Lk} \quad \textbf{Equation 3.1}$$

$$Q_k = Q_{Gk} - Q_{Lk} \quad \textbf{Equation 3.2}$$

where P_{Gk} and Q_{Gk} are the generator's real and reactive power, and P_{Lk} and Q_{Lk} are the real and reactive power of the loads.

Each bus can be divided into the following bus types:

- Swing bus (or slack bus) – There is only one swing bus in a power system. The swing bus is the reference bus where $V\angle\delta° = 1.0\angle 0°$ per unit. The power flow computes P_k and Q_k.
- Load (PQ) bus – P_k and Q_k are used as the input data for this bus type. The power flow computes V_k and δ_k. Most buses in a power flow are load buses.
- Voltage-controlled (PV) bus – P_k and V_k are the input data for this bus type. The power flow computes Q_k and δ_k. These can be buses to which generators, shunt capacitors or static var systems are connected.

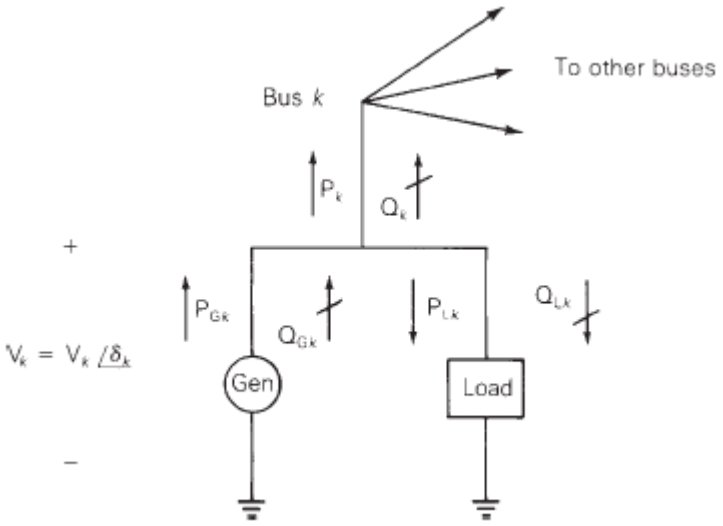

Figure 3.2: Bus variables V_k, δ_k, P_k and Q_k (Glover et al., 2017)

The Newton-Raphson method is used to solve the power flow problem in DIgSILENT PowerFactory. The x, y and f vectors for the power flow problem are defined in equations 3.3 to 3.5.

$$\mathbf{x} = \begin{bmatrix} \boldsymbol{\delta} \\ \mathbf{V} \end{bmatrix} = \begin{bmatrix} \delta_2 \\ \vdots \\ \delta_N \\ \mathrm{V}_2 \\ \vdots \\ \mathrm{V}_N \end{bmatrix}$$

Equation 3.3

$$\mathbf{y} = \begin{bmatrix} \mathbf{P} \\ \mathbf{Q} \end{bmatrix} = \begin{bmatrix} \mathrm{P}_2 \\ \vdots \\ \mathrm{P}_N \\ \mathrm{Q}_2 \\ \vdots \\ \mathrm{Q}_N \end{bmatrix}$$

Equation 3.4

$$\mathbf{f}(\mathbf{x}) = \begin{bmatrix} \mathbf{P}(\mathbf{x}) \\ \mathbf{Q}(\mathbf{x}) \end{bmatrix} = \begin{bmatrix} \mathrm{P}_2(\mathbf{x}) \\ \vdots \\ \mathrm{P}_N(\mathbf{x}) \\ \mathrm{Q}_2(\mathbf{x}) \\ \vdots \\ \mathrm{Q}_N(\mathbf{x}) \end{bmatrix}$$

Equation 3.5

All the V, P and Q terms are given in per unit, and the δ terms are given in radians. The V and δ variables for the swing bus are omitted from equations 3.3 to 3.5, because it is known, that $V\angle\delta° = 1.0\angle 0°$ per unit. The power balance equations are written as,

$$y_k = \mathrm{P}_k = \mathrm{P}_k(\mathrm{x}) = \mathrm{V}_k \sum_{n=1}^{N} \mathrm{Y}_{kn} \mathrm{V}_n \cos(\delta_k - \delta_n - \theta_{kn})$$

Equation 3.6

$$y_{k+N} = \mathrm{Q}_\mathrm{k} = \mathrm{Q}_k(\mathrm{x}) = \mathrm{V}_\mathrm{k} \sum_{n=1}^{N} \mathrm{Y}_\mathrm{kn} \mathrm{V}_n \sin(\delta_k - \delta_n - \theta_{kn})$$

Equation 3.7

k = 2, 3, …, N

The Jacobian matrix is given in equation 3.8. Equation 3.8 is partitioned into four blocks. The partial derivatives in each block are derived from equations 3.6 and 3.7. The Newton-Raphson method for the load flow analysis starts with equation 3.9 at the *i*th iteration.

$$\mathbf{J} = \left[\begin{array}{ccc|ccc} & \mathbf{J1} & & & \mathbf{J2} & \\ \frac{\partial P_2}{\partial \delta_2} & \cdots & \frac{\partial P_2}{\partial \delta_N} & \frac{\partial P_2}{\partial V_2} & \cdots & \frac{\partial P_2}{\partial V_N} \\ \vdots & & & \vdots & & \\ \frac{\partial P_N}{\partial \delta_2} & \cdots & \frac{\partial P_N}{\partial \delta_N} & \frac{\partial P_N}{\partial V_2} & \cdots & \frac{\partial P_N}{\partial V_N} \\ \hline \frac{\partial Q_2}{\partial \delta_2} & \cdots & \frac{\partial Q_2}{\partial \delta_N} & \frac{\partial Q_2}{\partial V_2} & \cdots & \frac{\partial Q_2}{\partial V_N} \\ \vdots & & & \vdots & & \\ \frac{\partial Q_N}{\partial \delta_2} & \cdots & \frac{\partial Q_N}{\partial \delta_N} & \frac{\partial Q_N}{\partial V_2} & \cdots & \frac{\partial Q_N}{\partial V_N} \\ & \mathbf{J3} & & & \mathbf{J4} & \end{array}\right]$$

Equation 3.8

$$\mathbf{x}(i) = \begin{bmatrix} \boldsymbol{\delta}(i) \\ \mathbf{V}(i) \end{bmatrix}$$

Equation 3.9

Equations 3.6 and 3.7 are used to solve equation 3.10:

$$\Delta \mathbf{y}(i) = \begin{bmatrix} \Delta \mathbf{P}(i) \\ \Delta \mathbf{Q}(i) \end{bmatrix} = \begin{bmatrix} \mathbf{P} - \mathbf{P}[\mathbf{x}(i)] \\ \mathbf{Q} - \mathbf{Q}[\mathbf{x}(i)] \end{bmatrix}$$

Equation 3.10

After solving the Jacobian matrix, the Gauss elimination and back substation are used to solve equation 3.11,

$$\left[\begin{array}{c|c} \mathbf{J1}(i) & \mathbf{J2}(i) \\ \hline \mathbf{J3}(i) & \mathbf{J4}(i) \end{array}\right] \begin{bmatrix} \Delta \boldsymbol{\delta}(i) \\ \Delta \mathbf{V}(i) \end{bmatrix} = \begin{bmatrix} \Delta \mathbf{P}(i) \\ \Delta \mathbf{Q}(i) \end{bmatrix}$$

Equation 3.11

After solving equation 3.11, equation 3.12 must be computed:

$$\mathbf{x}(i+1) = \begin{bmatrix} \boldsymbol{\delta}(i+1) \\ \mathbf{V}(i+1) \end{bmatrix} = \begin{bmatrix} \boldsymbol{\delta}(i) \\ \mathbf{V}(i) \end{bmatrix} + \begin{bmatrix} \Delta \boldsymbol{\delta}(i) \\ \Delta \mathbf{V}(i) \end{bmatrix}$$

Equation 3.12

Starting with the initial value x(0), the procedures continue until convergence is obtained for the load flow problem or until the set maximum number of iterations is reached. For each voltage-controlled bus, the magnitude of V_k is known. In this instance, the function $Q_k(x)$ is not needed. V_k can be omitted from the x-axis, and Q_k can be omitted from the y-axis of the vector. The column corresponding to the partial derivatives of V_k and the rows corresponding to the partial derivatives of Qk(x) can be omitted. Alternatively, the rows and columns corresponding to the voltage-controlled buses can remain in the Jacobian matrix. After each iteration, the voltage magnitude,

$V_k(i + 1)$, of each voltage-controlled bus is reset to V_k, which is used as the input data for that bus. At the end of each iteration, $Q_k(x)$ is computed (Glover et al., 2017).

The load flow analysis for both grid-connected and islanded modes of operation for the modified IEEE 14-bus system is computed during the DIgSILENT simulation.

3.2.1 Grid-connected mode of operation

This section examines the balanced load flow results of the modified IEEE 14-bus system without renewable energy sources (RESs) during the grid-connected mode with the circuit breakers at the PCC in the close position, as shown in Figure 3.3. The DG consists of a 100 MVA synchronous generator, Gen_0006.

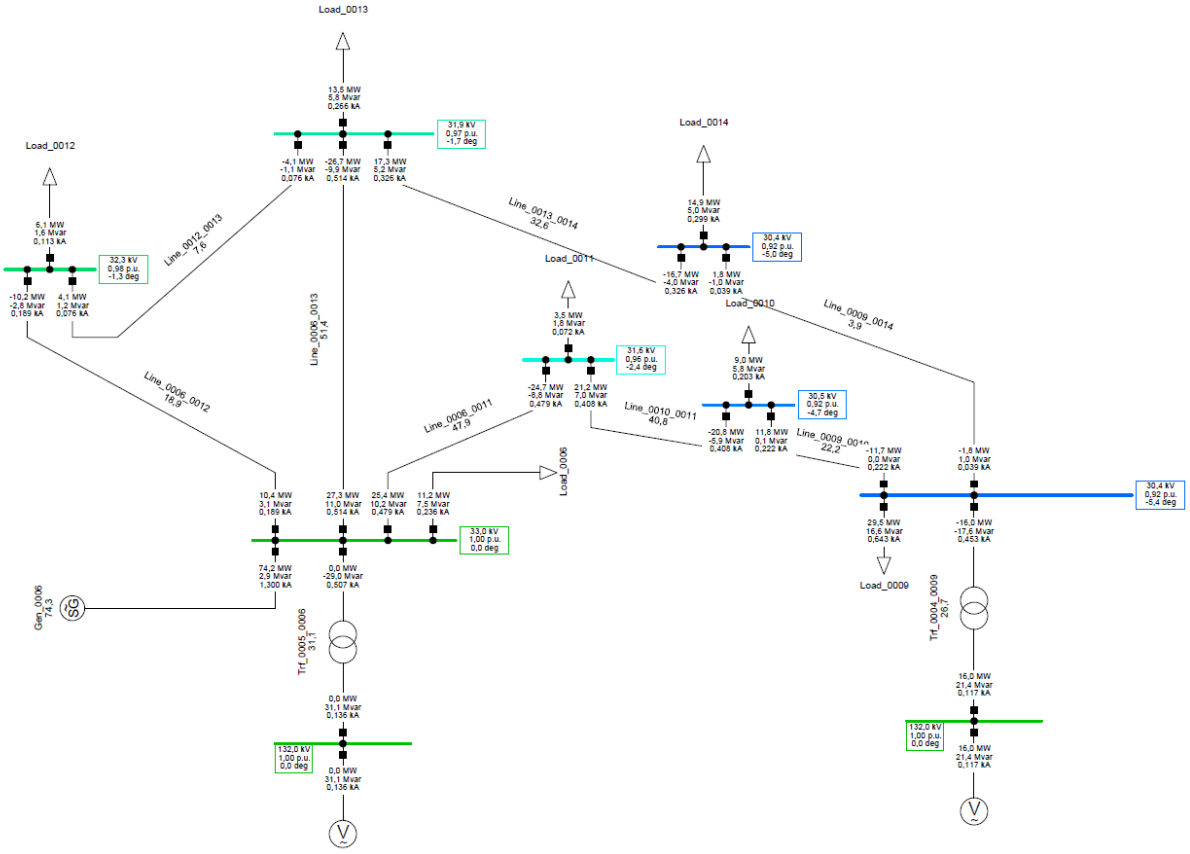

Figure 3.3: **Load flow results of the modified IEEE 14-bus system without RESs during grid-connected mode**

The voltage profile of the modified IEEE 14-bus system is provided in Table 3.6. The voltage deviation from the load flow results is within the ±10% tolerance according to

the voltage limit given in the IEEE 141 standard (IEEE 141, 1993). The voltage at Bus_0009 is $\frac{V_{actual}}{V_{base}} = \frac{30.39}{33} = \mathbf{0.921}\ \boldsymbol{p.u.}$

Table 3.6: Bus voltage results of the modified IEEE 14-bus system without DERs during grid-connected mode

Grid: Grid	System Stage: Grid			Study Case: 01 - Load Flow Case Origin	Annex: / 4
	nom.V [kV]	Bus - voltage [p.u.]	[kV]	[deg]	Voltage - Deviation [%] -10 -5 0 +5 +10
Bus_0004	132,00	1,000	132,00	0,00	
Bus_0005	132,00	1,000	132,00	0,00	
Bus_0006	33,00	1,000	33,00	0,00	
Bus_0009	33,00	0,921	30,39	-5,38	
Bus_0010	33,00	0,925	30,52	-4,71	
Bus_0011	33,00	0,956	31,56	-2,45	
Bus_0012	33,00	0,980	32,33	-1,33	
Bus_0013	33,00	0,968	31,95	-1,67	
Bus_0014	33,00	0,920	30,37	-4,97	

From Table 3.7, the load flow results are as follows:

Gen_0006 supplies 74.25 MW + 2.86 Mvar (74.31 MVA) at a power factor of 0.9992 lagging. The grid supplies the additional power of 16.02 MW + 52.44 Mvar (54.83 MVA) required by the load.

Table 3.7: Load flow results of the modified IEEE 14-bus system without RESs during grid-connected mode

Bus no.	Bus results						
	V (p.u.)	V (kV)	δ (deg)	P_G (MW)	Q_G (Mvar)	P_L (MW)	Q_L (Mvar)
4	1,000	132,00	0,00	16.02	21.37	-	-
5	1,000	132,00	0,00	-	31.06	-	-
6	1,000	33,00	0,00	74.25	2.86	11.2	7.5
9	0.921	30.39	-5.38	-	-	29.5	16.6
10	0.925	30.52	-4.71	-	-	9.0	5.8
11	0.956	31.56	-2.45	-	-	3.5	1.8
12	0.980	32.33	-1.33	-	-	6.1	1.6
13	0.968	31.95	-1.67	-	-	13.5	5.8
14	0.920	30.37	-4.97	-	-	14.9	5.0

From the grid summary of the modified IEEE 14-bus system during the grid-connected mode, it is observed that the total generation is 90.27 MW + 55.3 Mvar (105.86 MVA) as given in Table 3.8. The load demand is 87.7 MW + 44.1Mvar (98.16 MVA) and the transmission lines losses are 2.57 MW + 11.2 Mvar (11.49 MVA). The sum of the active

power are $\sum P_G = P_L + P_{losses} = 87.7 + 2.57 = 90.27\ MW$, and reactive power are $\sum Q_G = Q_L + Q_{losses} = 44.1 + 11.2 = 55.3\ Mvar$.

Table 3.8: Grid summary of the modified IEEE 14-bus system without RESs during grid-connected mode

Description	Active power (MW)	Reactive power (Mvar)
Generation	90.27	55.3
Load	87.7	44.1
Line losses	2.57	11.2

3.2.2 Islanded mode of operation

This section examines the balanced load flow results of the modified IEEE 14-bus system without RESs during the islanded mode with the circuit breakers at the PCC in the open position, as shown in Figure 3.4. The DG consists of a 100 MVA synchronous generator, Gen_0006.

The voltage profile of the modified IEEE 14-bus system is provided in Table 3.9. The voltage deviation from the load flow results exceeds the ±10% tolerance allowed according to the voltage limit given in the IEEE 141 standard (IEEE 141, 1993). The voltage at Bus_0009 is $\frac{V_{actual}}{V_{base}} = \frac{27.2}{33} = 0.824\ p.u.$

Table 3.9: Bus voltage results of the modified IEEE 14-bus system without RESs during islanded mode

Grid: Grid	System Stage: Grid			Study Case: 01 - Load Flow Case Origin	Annex: / 4
	nom.V [kV]	Bus - voltage [p.u.]	[kV]	[deg]	Voltage - Deviation [%] -10 -5 0 +5 +10
Bus_0004	132,00	0,000	0,00	0,00	
Bus_0005	132,00	0,000	0,00	0,00	
Bus_0006	33,00	1,000	33,00	0,00	
Bus_0009	33,00	0,824	27,20	-7,52	
Bus_0010	33,00	0,843	27,83	-6,34	
Bus_0011	33,00	0,914	30,15	-3,06	
Bus_0012	33,00	0,972	32,09	-1,51	
Bus_0013	33,00	0,953	31,44	-1,86	
Bus_0014	33,00	0,857	28,28	-6,27	

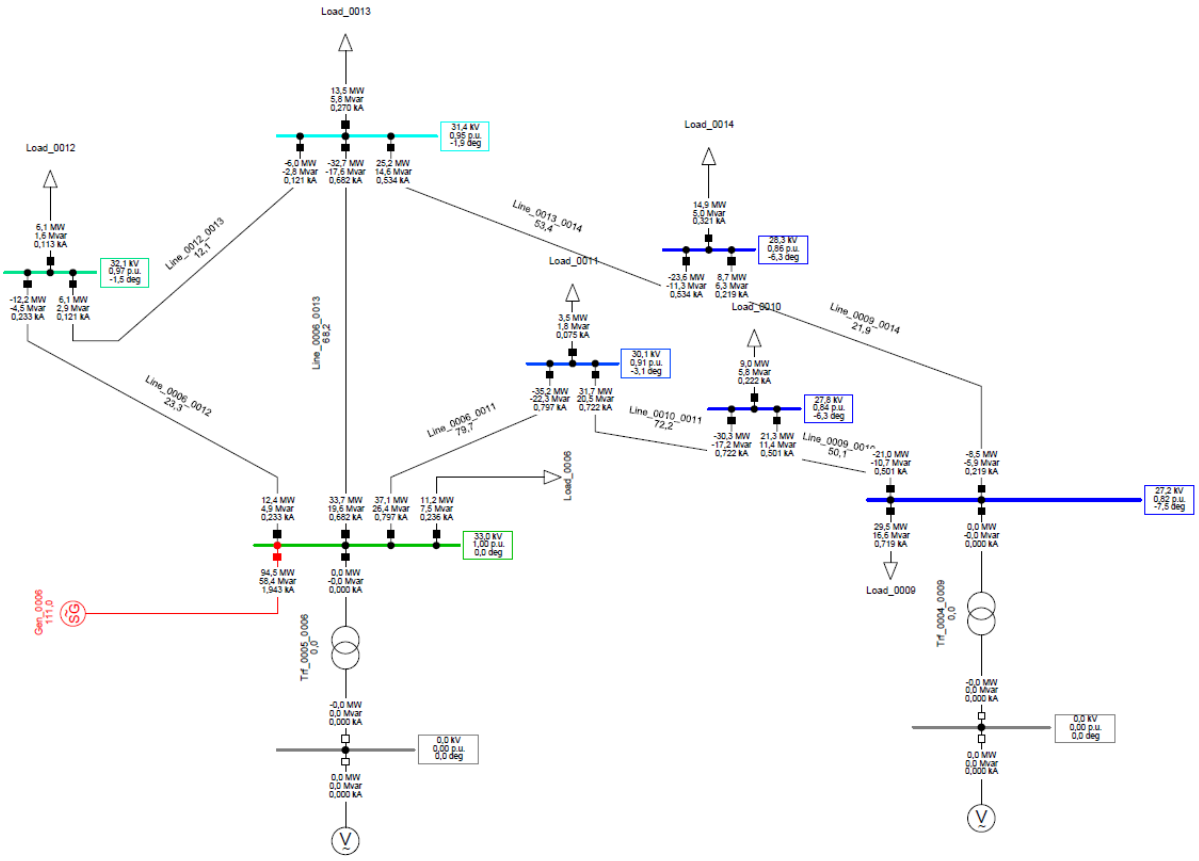

Figure 3.4: Load flow results of the IEEE 14 bus system without RESs during islanded mode

From Table 3.10, the load flow results are as follows:

Gen_0006 supplies 94.45 MW + 58.39 Mvar (111.04 MVA) at a power factor of 0.8506 lagging.

Table 3.10: Load flow results of the modified IEEE 14-bus system without RESs during islanded mode

Bus no.	Bus results						
	V (p.u.)	V (kV)	δ (deg)	P_G (MW)	Q_G (Mvar)	P_L (MW)	Q_L (Mvar)
4	-	-	-	-	-	-	-
5	-	-	-	-	-	-	-
6	1,000	33,00	0,00	94.45	58.39	11.2	7.5
9	0.824	27.20	-7.52	-	-	29.5	16.6
10	0.843	27.83	-6.34	-	-	9.0	5.8
11	0.914	30.15	-3.06	-	-	3.5	1.8
12	0.972	32.09	-1.51	-	-	6.1	1.6
13	0.953	31.44	-1.86	-	-	13.5	5.8
14	0.857	28.28	-6.27	-	-	14.9	5.0

From the grid summary of the modified IEEE 14-bus system during the islanded mode, it is observed that the total generation is 94.45 MW + 58.39 Mvar (105.86 MVA) as given in Table 3.11. The load demand is 87.7 MW + 44.1Mvar (98.16 MVA) and the transmission lines losses are 6.75 MW + 14.29 Mvar (15.8 MVA). The sum of the active power are $\sum \boldsymbol{P_G} = \boldsymbol{P_L} + \boldsymbol{P_{losses}} = \boldsymbol{87.7 + 6.75 = 94.45\ MW}$, and reactive power are $\sum \boldsymbol{Q_G} = \boldsymbol{Q_L} + \boldsymbol{Q_{losses}} = \boldsymbol{44.1 + 14.29 = 58.39\ Mvar}$.

Table 3.11: Grid summary of the modified IEEE 14-bus system without RESs during islanded mode

Description	Active power (MW)	Reactive power (Mvar)
Generation	94.45	58.39
Load	87.7	44.1
Line losses	6.75	14.29

Gen_0006 is voltage controlled, and the voltage at Bus_0006 is $1.00\angle 0.00\ p.u.$ for both grid-connected and islanded modes of operation. Gen_0006 is overloaded (111.0 %) during the islanded mode. Additionally, the voltages at Bus_0009, Bus_0010, and Bus_0014 are less than 0.90 p.u. and do not comply with the requirements as provided in the IEEE 141 standard.

3.3 Load flow analysis of modified IEEE 14-bus system with an additional DG

An additional DG is added to the existing 100 MVA synchronous generator, Gen_0006, to assist with the load demand during the islanded mode. The DG consists of 20 x 2.5 MVA type 4 (full converter) wind turbine generators (WTGs) to give a total installed capacity of 50 MW for the wind farm. The WTG is connected to the modified IEEE 14-bus system at the point of coupling (POC) at Bus_0009, as depicted in Figure 3.5. The parameters for the WTGs and step-up transformers are provided in Tables 3.12 and 3.13, respectively.

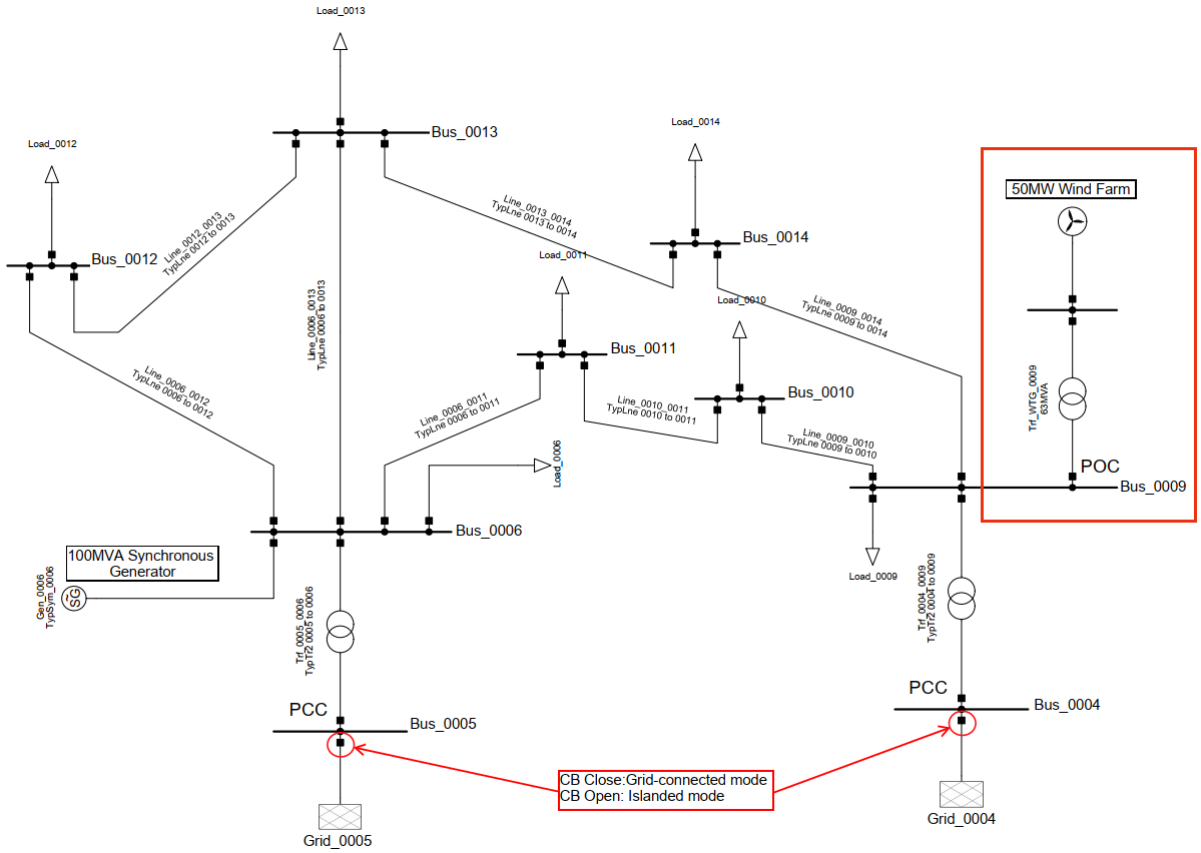

Figure 3.5: 33 kV distribution network of the modified IEEE 14-bus system with an additional DG

Table 3.12: Data for the 50 MW wind farm

Description	No. of units in parallel	Unit size (MVA)	Voltage (kV)	Power factor	Short-circuit model	Fault current contribution per unit (kA)
50MW WTG	20	2.5	0.69	0.9	Type 4 – Full-size converter	3.1378

Table 3.13: Data for the 63 MVA transformer

Description	Size (MVA)	Voltage (kV)	Vector Group	Impedance (p.u.)
Trf_WTG_0009	63	0.69/33	Dyn11	0.125

3.3.1 Grid-connected mode of operation

This section examines the balanced load flow results of the modified IEEE 14-bus system with the additional DG during the grid-connected mode with the circuit breakers at the PCC in the close position, as shown in Figure 3.6. The loading of Gen_0006 decreased from 74.3% to 40.2% with the added DG during the grid-connected mode.

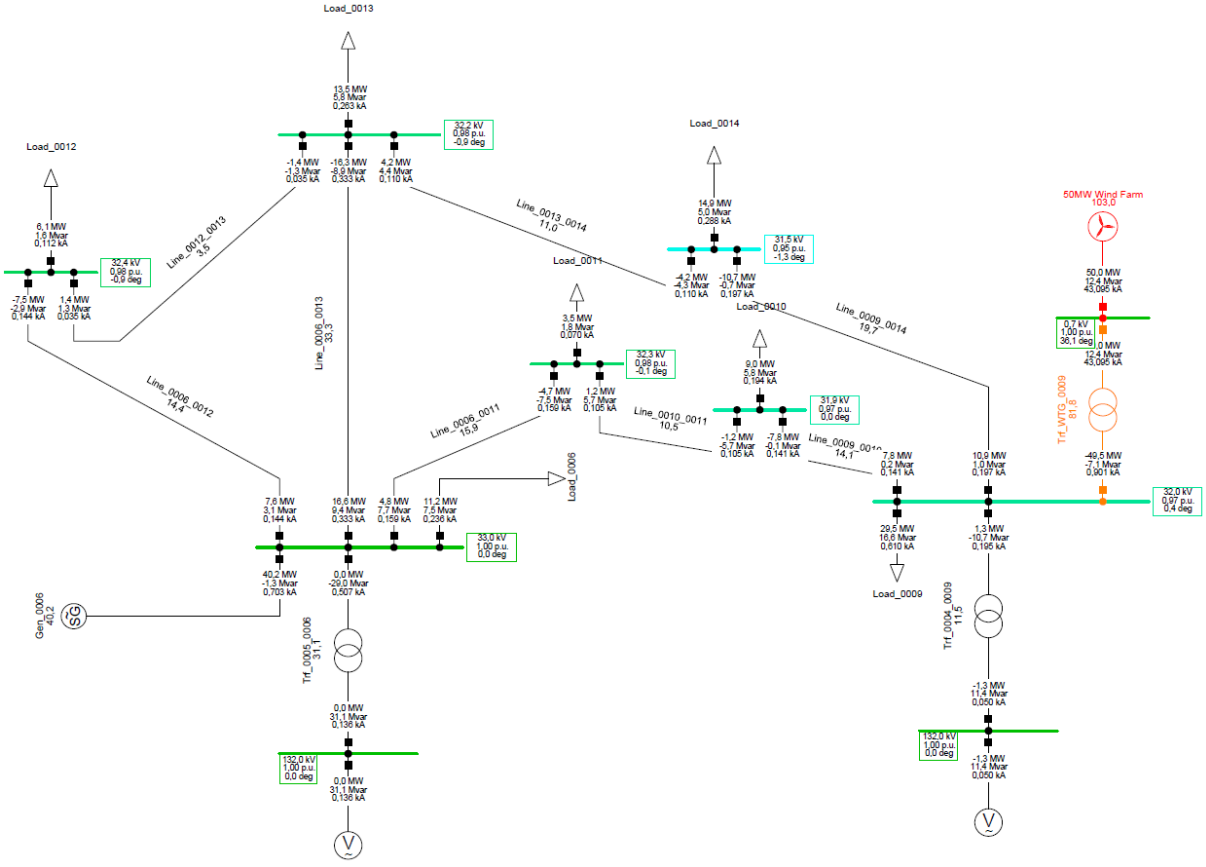

Figure 3.6: **Load flow results of the modified IEEE 14-bus system with an additional DG during grid-connected mode**

The voltage profile of the modified IEEE 14-bus system is provided in Table 3.14. The voltage deviation from the load flow results is within the ±10% tolerance according to the voltage limit given in the IEEE 141 standard (IEEE 141, 1993). The voltage at Bus_0009 is $\frac{V_{actual}}{V_{base}} = \frac{32.03}{33} = \mathbf{0.971\ p.u.}$

Table 3.14: Bus voltage results of the modified IEEE 14-bus system with an additional DG during grid-connected mode

Grid: Grid	System Stage: Grid	Study Case: 01 - Load Flow Case Origin	Annex: / 4

	nom.V [kV]	Bus - voltage [p.u.]	[kV]	[deg]	Voltage - Deviation [%] -10 -5 0 +5 +10
Bus_0004	132,00	1,000	132,00	0,00	
Bus_0005	132,00	1,000	132,00	0,00	
Bus_0006	33,00	1,000	33,00	0,00	
Bus_0009	33,00	0,971	32,03	0,40	
Bus_0010	33,00	0,968	31,94	0,01	
Bus_0011	33,00	0,980	32,34	-0,13	
Bus_0012	33,00	0,983	32,43	-0,91	
Bus_0013	33,00	0,977	32,24	-0,90	
Bus_0014	33,00	0,954	31,47	-1,34	
Bus_WTG	0,69	1,000	0,69	36,10	

From Table 3.15, the load flow results are as follows:

Gen_0006 supplies 40.18 MW + -1.26 Mvar (40.2 MVA) at a power factor of 0.9995 leading. The grid supplies the additional power of -1.27 MW + 42.47 Mvar (54.83 MVA) required by the load. The real power of 1.27 MW is exported into the main grid.

Table 3.15: Load flow results of the modified IEEE 14-bus system with an additional DG during grid-connected mode

Bus no.	Bus results						
	V (p.u.)	V (kV)	δ (deg)	P_G (MW)	Q_G (Mvar)	P_L (MW)	Q_L (Mvar)
4	1,000	132,00	0,00	-1.27	11.41	-	-
5	1,000	132,00	0,00	-	31.06	-	-
6	1,000	33,00	0,00	40.18	-1.26	11.2	7.5
9	0.971	32.03	0.40	-	-	29.5	16.6
10	0.968	31.94	0.01	-	-	9.0	5.8
11	0.980	32.34	-0.13	-	-	3.5	1.8
12	0.983	32.43	-0.91	-	-	6.1	1.6
13	0.977	32.24	-0.90	-	-	13.5	5.8
14	0.954	31.47	-1.34	-	-	14.9	5.0
WTG	1.000	0.69	36.1	50.0	12.35	-	-

From the grid summary of the modified IEEE 14-bus system during the grid-connected mode, it is observed that the total generation is 88.91 MW + 53.56 Mvar (103.8 MVA) as given in Table 3.16. The load demand is 87.7 MW + 44.1Mvar (98.16 MVA), and the transmission line losses are 1.21 MW + 9.46 Mvar (9.54 MVA). The sum of the active power are $\sum \boldsymbol{P_G} = \boldsymbol{P_L} + \boldsymbol{P_{losses}} = \boldsymbol{87.7 + 1.21 = 88.91\ MW}$, and reactive power are $\sum \boldsymbol{Q_G} = \boldsymbol{Q_L} + \boldsymbol{Q_{losses}} = \boldsymbol{44.1 + 9.46 = 53.56\ Mvar}$.

Table 3.16: Grid summary of the modified IEEE 14-bus system with an additional DG during grid-connected mode

Description	Active power (MW)	Reactive power (Mvar)
Generation	88.91	53.56
Load	87.7	44.1
Line losses	1.21	9.46

3.3.2 Islanded mode of operation

This section examines the balanced load flow results of the modified IEEE 14-bus system with an additional DG during the islanded mode with the circuit breakers at the PCC in the open position, as shown in Figure 3.7. The loading of Gen_0006 decreased from 111.0% to 51.0% with the added DG during the islanded mode.

The voltage profile of the modified IEEE 14-bus system is provided in Table 3.17. The voltage deviation from the load flow results is within the ±10% tolerance according to the voltage limit given in the IEEE 141 standard (IEEE 141, 1993). The voltage at Bus_0009 is $\frac{V_{actual}}{V_{base}} = \frac{31.61}{33} = \mathbf{0.958}\ \boldsymbol{p.u.}$

Table 3.17: Bus voltage results of the modified IEEE 14-bus system with an additional DG during islanded mode

Grid: Grid	System Stage: Grid	Study Case: 01 - Load Flow Case Origin	Annex: / 4

	nom.V [kV]	Bus - voltage [p.u.]	[kV]	[deg]	Voltage - Deviation [%] -10 -5 0 +5 +10
Bus_0004	132,00	0,000	0,00	0,00	
Bus_0005	132,00	0,000	0,00	0,00	
Bus_0006	33,00	1,000	33,00	0,00	
Bus_0009	33,00	0,958	31,61	1,02	
Bus_0010	33,00	0,957	31,59	0,51	
Bus_0011	33,00	0,975	32,17	0,12	
Bus_0012	33,00	0,982	32,40	-0,88	
Bus_0013	33,00	0,975	32,18	-0,82	
Bus_0014	33,00	0,946	31,20	-0,98	
Bus_WTG	0,69	1,000	0,69	36,71	

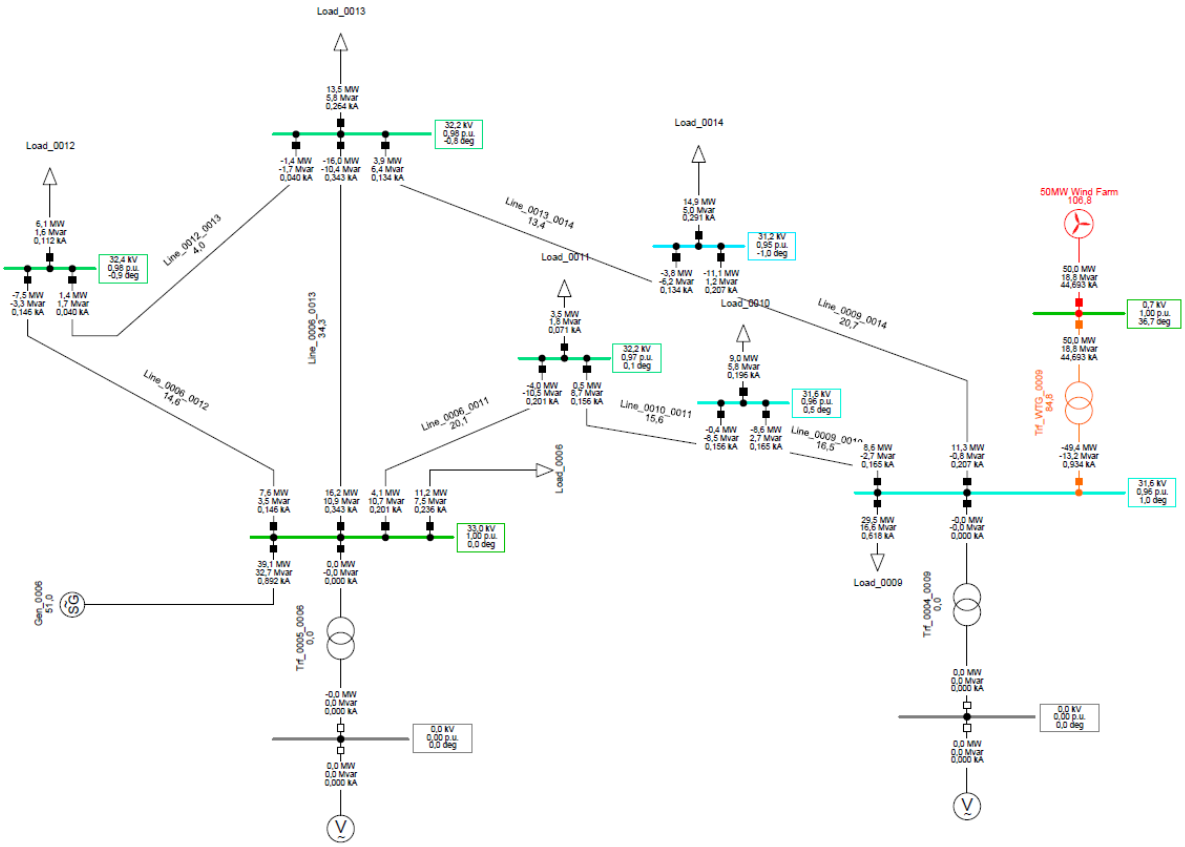

Figure 3.7: **Load flow results of the modified IEEE 14-bus system with an additional DG during islanded mode**

From Table 3.18, the load flow results are as follows:

Gen_0006 supplies a power of 39.11 MW + 32.71 Mvar (50.99 MVA) at a power factor of 0.767 lagging. The WTG supplies a power of 50.00 MW + 18.78 Mvar (53.41) at a power factor of 0.9362 lagging.

Table 3.18: **Load flow results of the modified IEEE 14-bus system with an additional DG during islanded mode**

Bus no.	Bus results						
	V (p.u.)	V (kV)	δ (deg)	P_G (MW)	Q_G (Mvar)	P_L (MW)	Q_L (Mvar)
4	-	-	-	-	-	-	-
5	-	-	-	-	-	-	-
6	1,000	33,00	0,00	39.11	32.71	11.2	7.5
9	0.958	31.61	1.02	-	-	29.5	16.6
10	0.957	31.59	0.51	-	-	9.0	5.8
11	0.975	32.17	0.12	-	-	3.5	1.8
12	0.982	32.40	-0.88	-	-	6.1	1.6
13	0.975	32.18	-0.82	-	-	13.5	5.8
14	0.946	31.20	-0.98	-	-	14.9	5.0
WTG	1.000	0.69	36.71	50.0	18.79	-	-

From the grid summary of the modified IEEE 14-bus system during the grid-connected mode, it is observed that the total generation is 89.11 MW + 51.49 Mvar (102.92 MVA) as given in Table 3.19. The load demand is 87.7 MW + 44.1Mvar (98.16 MVA), and the transmission line losses are 1.41 MW +7.39 Mvar (7.52 MVA). The sum of the active power are $\sum \boldsymbol{P_G} = \boldsymbol{P_L} + \boldsymbol{P_{losses}} = \boldsymbol{87.7 + 1.41 = 89.11\ MW}$, and reactive power are $\sum \boldsymbol{Q_G} = \boldsymbol{Q_L} + \boldsymbol{Q_{losses}} = \boldsymbol{44.1 + 7.39 = 51.49\ Mvar}$.

Table 3.19: Grid summary of the modified IEEE 14-bus system with an additional DG during islanded mode

Description	Active power (MW)	Reactive power (Mvar)
Generation	89.11	51.49
Load	87.7	44.1
Line losses	1.41	7.39

Gen_0006 is voltage controlled, ensuring that the voltage at Bus_0006 remains at $1.00\angle 0.00\ p.u.$ for both grid-connected and islanded modes of operation. The added DG improved to overall reliability of the modified IEEE 14-bus system. The loading for the 100 MVA synchronous generator decreased from 74.3 to 40.2% during the grid-connected mode, and from 111.0 to 51.0% during islanded mode. The voltage at Bus_0009 increased from 0.921 to 0.971 during the grid-connected mode, and from 0.824 to 0.958 during islanded mode and is within the allowed tolerance of ±10% as per the IEEE 141 standard.

3.4 Short-circuit study of the modified IEEE 14-bus network

A fault current in a power system is caused by insulation failure disrupting the normal flow of current. Different types of faults can be divided into symmetrical and asymmetrical faults as shown in Figure 3.8.

Three-phase faults are known as symmetrical faults. Symmetrical faults are fault currents that are equal in magnitude and are phased-displaced 120° apart from each other. These types of faults are the most severe but rarely occur in power systems (2-3% of faults). Most faults that occur in power systems are single line-to-ground faults (Blackburn and Domin, 2014)

The following types of faults can be classified as asymmetrical faults:

- Single line-to-ground: 70-80% of faults

- Line-to-line: 8-10% of faults
- Double line-to-ground: 10-17% of faults (Blackburn and Domin, 2014).

The method of symmetrical components is used to analyse three-phase systems during power-unbalanced conditions such as phase-to-ground faults. Symmetrical components are divided into the following sequence components:

- Positive-sequence components
- Negative-sequence components
- Zero-sequence components

Only three-phase faults are considered for the study of the modified IEEE 14-bus system during the DIgSILENT simulations. The single phase-to-ground fault are simulated during the hardware-in-the-loop (HIL) protection testing in Chapter 5. The fault currents are calculated according to the IEC 60909 standard.

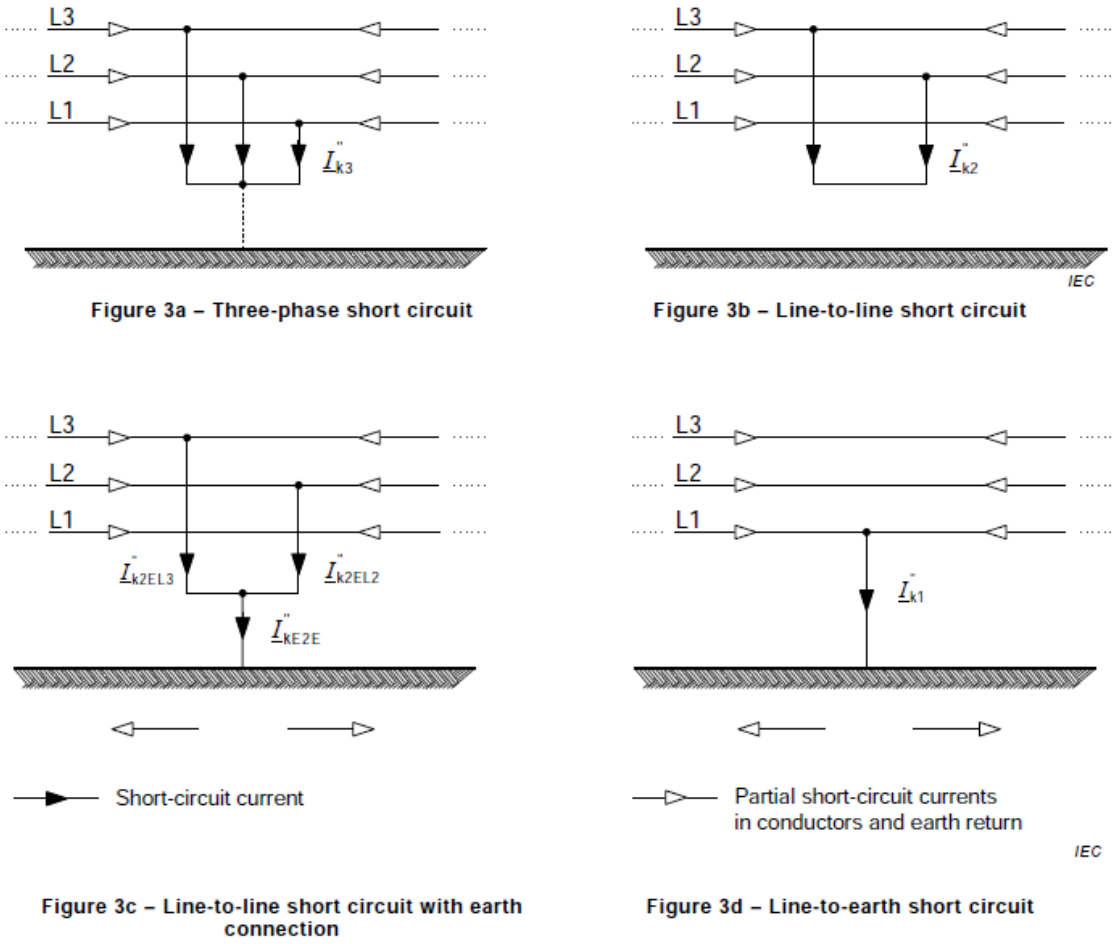

Figure 3a – Three-phase short circuit

Figure 3b – Line-to-line short circuit

Figure 3c – Line-to-line short circuit with earth connection

Figure 3d – Line-to-earth short circuit

Figure 3.8: Different types of short-circuit currents in power systems (IEC 60909-0, 2016)

Three-phase, short-circuit currents are calculated for the following two network topologies:

- Grid-connected mode of operation

- Islanded mode of operation

Three-phase, short-circuit currents are calculated for close-in faults at each circuit breaker. This is calculated at 1% and 99% of the line length. The maximum fault current contribution from each 2.5 MW, Type 4 WTG is limited to 1.5 x I_{rated} (3.1378 kA per WTG at 0.69 kV) due to the power electronics converter (Nelson, 2012), (Walling, Gursoy, and English, 2011). The short-circuit MVA for the grid is 10000 MVA at the 132 kV bus (IEC 60076-5, 2005), while the c-factor is 1.10 p.u. at 132 kV (IEC 60909, 2016).

3.4.1 Short-circuit study for the modified IEEE 14-bus system during grid-connected mode

Figure 3.9 and Table 3.20 shows the three-phase short-circuit currents at each bus. The installed circuit breakers must be designed to withstand the three-phase short-circuit currents at each bus. The three-phase short-circuit currents measured at 1% and 99% of the line length are provided in Table 3.21. The fault currents are applied on the line as close as possible to the CTs (1% and 99% of line length) to represent the close-in and far bus fault currents. The far bus fault currents (three-phase fault at 99% of line length) measured for each circuit breaker from Table 3.21 are used to calculate the instantaneous overcurrent settings (ANSI 50) for each relay during the grid-connected mode of operation.

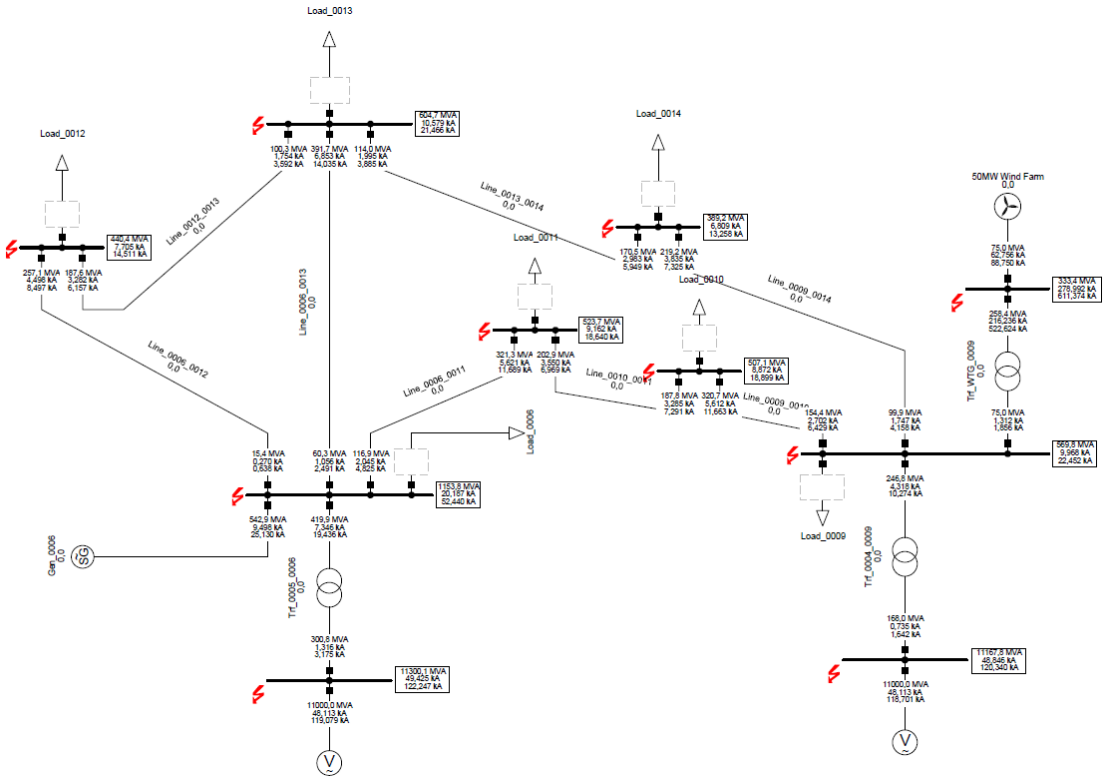

Figure 3.9: Results of short-circuit currents for 3ph faults at all busbars

Table 3.20: Summary of short-circuit currents for 3ph faults at all busbars

Bus no.	Sk" (MVA)	Ik" (kA)	δ (deg)
4	11167.79	48.85	-84.25
5	11300.12	49.43	-84.39
6	1153.84	20.19	-87.15
9	569.75	9.97	-80.66
10	507.1	8.87	-77.81
11	523.71	9.16	-75.4
12	440.41	7.71	-68.75
13	604.65	10.58	-74.86
14	389.21	6.81	-72.57
WTG	333.43	278.99	-82.3

Table 3.21: Summary of three-phase fault currents at 1% and 99% of line length

Location	3ph fault current at 1% of line length (kA)	3ph fault current at 99% of line length (kA)
Line_0006_0012	18.392	7.718
Line_0012_0013	7.698	10.492
Line_0006_0013	10.603	18.622
Line_0013_0014	10.445	6.803
Line_0009_0014	6.815	9.890
Line_0009_0010	9.952	8.879
Line_0010_0011	8.857	9.140
Line_0006_0011	9.187	18.548

From Table 3.20, it can be observed that the maximum three-phase fault in the 33 kV distribution network occurs at bus no. 6. With a three-phase fault current of 20.19 kA, the equipment needs to be designed to withstand a three-phase fault current of at least 21 kA for a duration of 1 s. The measured fault current at the far bus is used to calculate the instantaneous overcurrent settings for the SEL-351 directional overcurrent relays during the grid-connected mode.

3.4.2 Short-circuit study for the modified IEEE 14-bus system during islanded mode

Figure 3.10 and Table 3.22 show the three-phase short-circuit currents at each bus. The three-phase short-circuit currents measured at 1% and 99% of the line length are provided in Table 3.23. The fault currents are applied on the line as close as possible to the CTs (1% and 99% of line length) to represent the close-in and far bus fault

currents. The far bus fault currents (three-phase fault at 99% of line length) measured for each circuit breaker from Table 3.23 are used to calculate the instantaneous overcurrent settings (ANSI 50) for each relay during the islanded mode of operation. The fault current contribution is less than that of the grid-connected mode of operation.

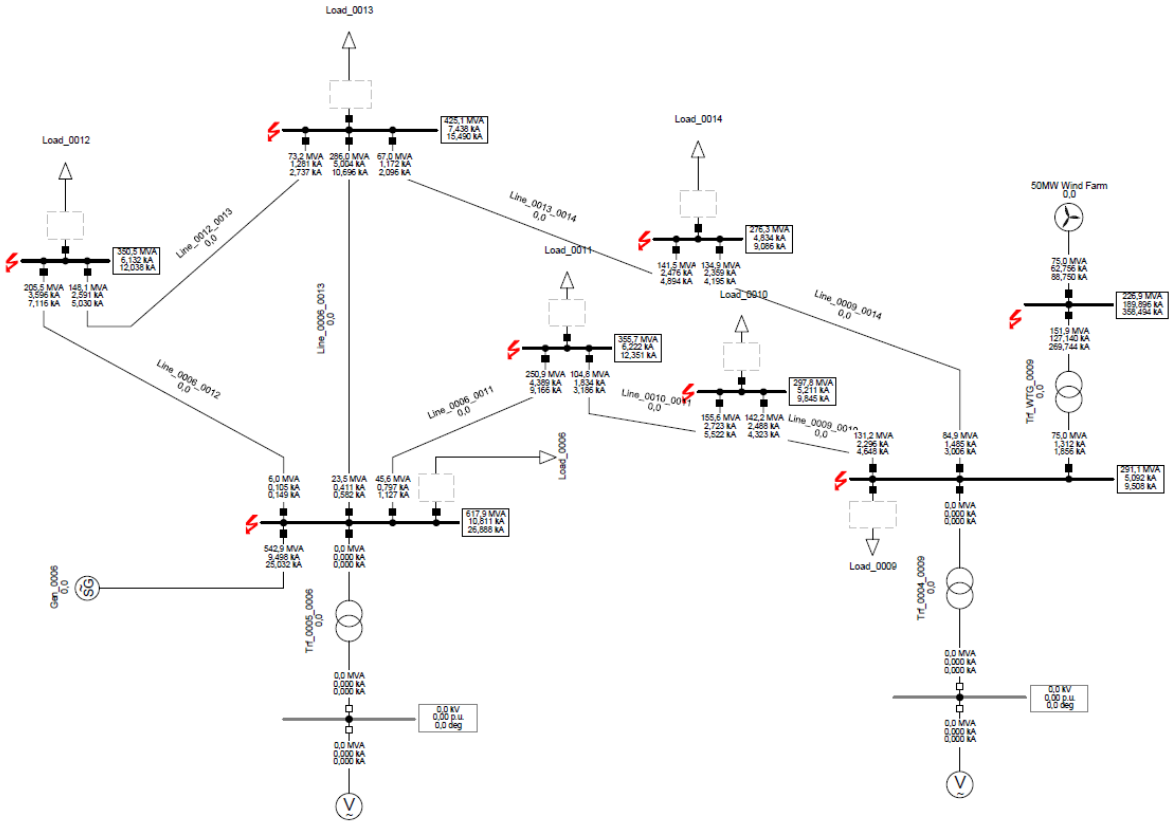

Figure 3.10: Results of short-circuit currents for 3ph faults at all busbars

Table 3.22: Summary of short-circuit currents for 3ph faults at all busbars

Bus no.	Sk" (MVA)	Ik" (kA)	δ (deg)
4	-	-	-
5	-	-	-
6	617.91	10.81	-87.14
9	291.06	5.09	-73.82
10	297.84	5.21	-74.22
11	355.66	6.22	-76.4
12	350.52	6.13	-73.81
13	425.14	7.44	-78.33
14	276.3	4.83	-73.18
WTG	226.95	189.9	-76.6

Table 3.23: Summary of three-phase fault currents at 1% and 99% of line length

Location	3ph fault current at 1% of line length (kA)	3ph fault current at 99% of line length (kA)
Line_0006_0012	10.675	6.140
Line_0012_0013	6.128	7.402
Line_0006_0013	7.452	10.743
Line_0013_0014	7.369	4.839
Line_0009_0014	4.830	5.083
Line_0009_0010	5.093	5.209
Line_0010_0011	5.215	6.204
Line_0006_0011	6.242	10.711

From Table 3.23, it can be observed that the maximum three-phase fault current is less than compared to the results obtained during the grid-connected mode. The measured fault current at the far bus is used to calculate the instantaneous overcurrent settings for the SEL-351 directional overcurrent relays during the islanded mode.

3.5 Overcurrent coordination

3.5.1 Introduction

There are 16 SEL-351A directional overcurrent relays (DOCRs), one at each end of the 8 transmission lines as shown in Figure 3.11. Because the fault current can flow in either direction into the line, DOCRs are needed. The trip direction is normally into the line where it is protected. The trip direction for all the protection relays is set in the forward direction. The relay pairs will be considered by identifying the relays in the clockwise and anti-clockwise loops as shown in Table 3.24. The modified IEEE 14-bus system consists of 3 loops (Senarathna and Hemapala, 2020).

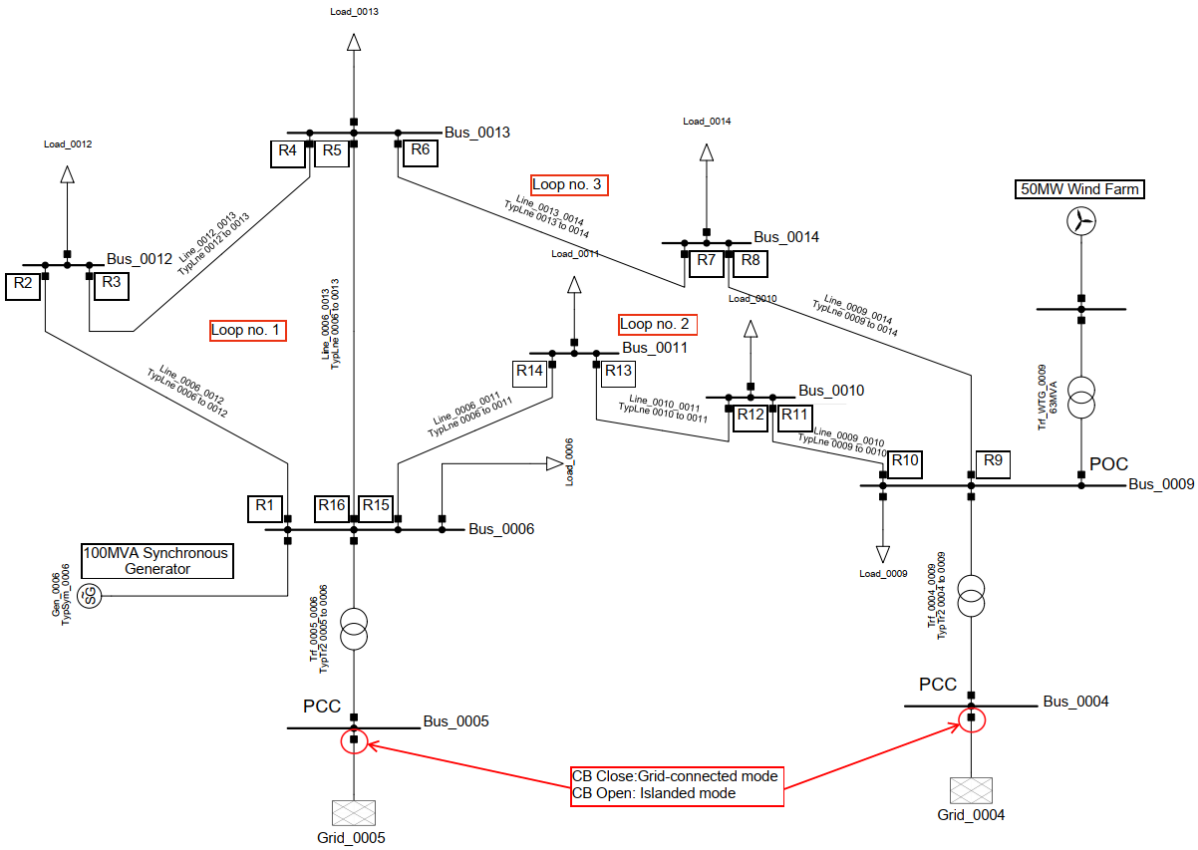

Figure 3.11: Location of relays in the modified IEEE 14-bus system with DGs

Table 3.24: Identification of the relay pairs for the modified IEEE 14-bus system (Senarathna and Hemapala, 2020)

Direction of loops	Loop no.	Primary relay	Backup relay
Clockwise	1	R1	R5
		R3	R1
		R5	R3
	2	R6	R16
		R8	R6
		R10	R8
		R12	R10
		R14	R12
		R16	R14
	3	R6	R3
		R1	R14
		All other relay pairs for loop no. 3 have already been identified.	
Anti-clockwise	1	R2	R4
		R16	R2
		R4	R16
	2	R5	R7
		R15	R5
		R13	R15
		R11	R13
		R9	R11
		R7	R9
	3	R15	R2
		R4	R7
		All other relay pairs for loop no. 3 have already been identified.	

Faults that occur within the transmission line should be cleared as fast as possible to enhance the transient stability of the system and minimise voltage disturbances. The overcurrent settings of the protection relays should ensure selective coordination. The objective would be to ensure that the protection settings allow the relays to operate as fast as possible for a fault that occurs in the primary zone and allow a sufficient time delay for faults that occur in backup zones. Where coordination is not possible, either a compromise must be made, or a pilot protection scheme must be implemented. The pickup current setting (51P) should be set to approximately 125 to 150% of the short-time maximum load (I_{STM}) to avoid unnecessary operation during short-time transients with inverse characteristic curves. The I_{STM} is the current that the circuit is required to carry during emergencies or unusual operating conditions, such as an adjacent circuit that is disconnected from the network. The instantaneous overcurrent setting (50P) must be set between 110 and 130% of the maximum far bus fault current (I_{FB}) and should operate with no intentional time delay in the order of 0.02 to 0.05 s. A coordination time interval (CTI) of 0.2 to 0.5 s is frequently used (Blackburn and Domin, 2014). The recommended minimum CTI allowed between the primary and backup protection relays is 0.20 s as shown in Table 3.25 (IEEE 242, 2001).

Table 3.25: Recommended minimum CTI for protection relays (IEEE 242, 2001)

Components	Electromechanical	Numerical
Circuit breaker opening time	0.08s	0.08s
Relay overtravel	0.10s	0.00s
Relay tolerance and CT error	0.12s	0.12s
Total CTI	0.30s	0.20s

The operating time for the relay characteristics curves can be calculated by using the following expression:

$$\boldsymbol{t = \frac{k\beta}{\left(\frac{I}{I_s}\right)^{\alpha} - 1} + L}$$ **Equation 3.13**

where:

t = relay operating times (s)

k = time dial or time multiplier setting

I = fault current (A)

I_s = pickup current setting (A)

L = constant

The constants α and β determine the slope of the relay characteristics. The values of α, β and L for the various standard relay overcurrent types are given in Table 3.26 according to the IEEE C37.112 and IEC 60255-151 standards.

Table 3.26: IEEE and IEC constant for standard overcurrent relays (IEC 60255-151, 2009), (IEEE C37.112, 2018)

Curve description	Standard	α	β	L
Moderately inverse	IEEE	0.02	0.0515	0.114
Very inverse	IEEE	2.0	19.61	0.491
Extremely inverse	IEEE	2.0	28.2	0.1217
Standard inverse	IEC	0.02	0.14	0
Very inverse	IEC	1.0	13.5	0
Extremely inverse	IEC	2.0	80.0	0

A combination of an inverse definite minimum time (IDMT) and instantaneous overcurrent relays is considered for all relays where possible. Using the high set instantaneous overcurrent element reduces the tripping time at high fault currents. It also improves the overall system grading by allowing the discrimination curves behind the high set instantaneous elements to be lowered (Alstom, 2011).

The IEC standard inverse characteristics curve will be used for the phase time-overcurrent setting. The instantaneous overcurrent is a definite time that is set at 0.05 s. A ratio of 1000/1 A is considered for all the current transformers (CTs). The coordination study of the primary relay, R1 and its backup relays, as well as the primary relay, R14 with its backup relay, is considered for case studies 1 and 2.

3.5.2 Case Study 1: Overcurrent coordination for the grid-connected mode of operation

Relay R1 measures a current of 144 A during normal operation, and the I_{STM} is 363 A. A pickup current of 550 A (approximately 1.5 x I_{STM}) is selected for the phase overcurrent (51P) setting. Relay R1 measures a far bus fault current of 4536 A. A pickup current of 5670 A (1.25 x I_{FB}) is selected for the instantaneous overcurrent setting (50P). During a close-in fault at Bus_0006 and Line_0006_0012, the primary relay R1 measures a 3-ph fault current of 18062 A. The 67P1 element initiates a trip at a time of 0.05 s. The backup relay, R5, measures a 3-ph fault current of 971 A and initiates a trip at a time of 9999.999 s (no trip). There is a loss of coordination between

relay R1 and relay R5. The backup relay, R14, measures a 3-ph fault current of 2001 A and initiates a trip at a time of 0.257 s. This gives a CTI of 0.257 – 0.05 = 0.207 s. Figure 3.12 and Table 3.27 show the measured fault currents and tripping times for relays R1, R5 and R14.

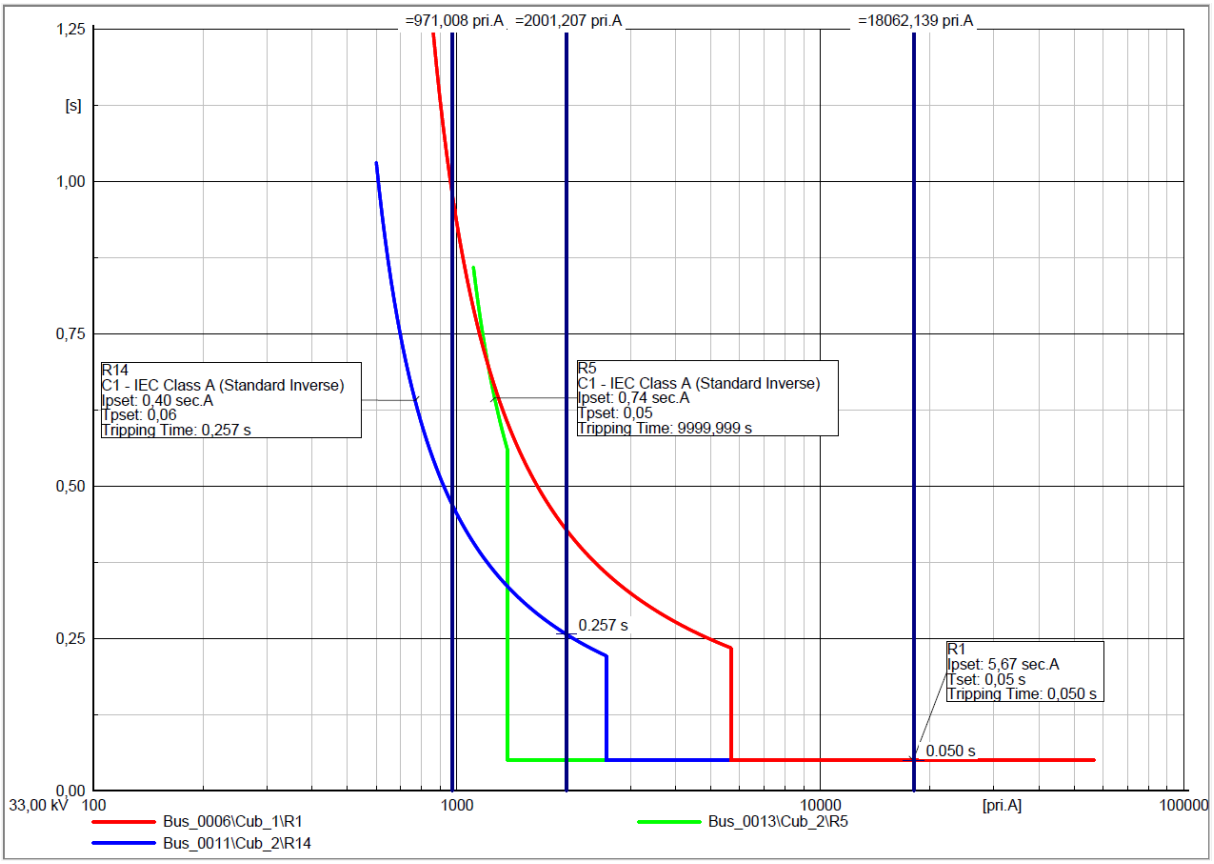

Figure 3.12: TCC for the primary relay R1 and backup relays R5 and R14

Table 3.27: Summary of tripping times during a close-in fault at Bus_0006 and Line_0006_0012

Relay	Protection element	Fault current (A)	Tripping time (s)
R1	51P	18062.14	0.159
	67P1	18062.14	0.050
R5	51P	971.01	9999.999
	67P1	971.01	9999.999
R14	51P	2001.21	0.257
	67P1	2001.21	9999.999

Relay R14 measures a current of 159 A during normal operation, and the I_{STM} is 267 A. A pickup current of 400 A (approximately 1.5 x I_{STM}) is selected for the phase overcurrent (51P) setting. Relay R14 measures a far bus fault current of 2067 A. A

pickup current of 2580 A (approximately 1.25 x I_{FB}) is selected for the instantaneous overcurrent setting (50P). During a close-in fault at Bus_0011 and Line_0006_0011, the primary relay R14 measures a 3-ph fault current of 3535 A. The 67P1 element initiates a trip at a time of 0.05 s. The backup relay R12 measures the same 3-ph fault current of 3535 A and initiates a trip at a time of 0.277 s. This gives a CTI of 0.277 – 0.05 = 0.227 s. Figure 3.13 and Table 3.28 show the measured fault currents and tripping times for relays R14 and R12. The summary of the protection settings for all the identified relay pairs are shown in Table 3.29, whereas Table 3.30 provides the summary of all the measured fault currents and tripping times during the grid-connected mode.

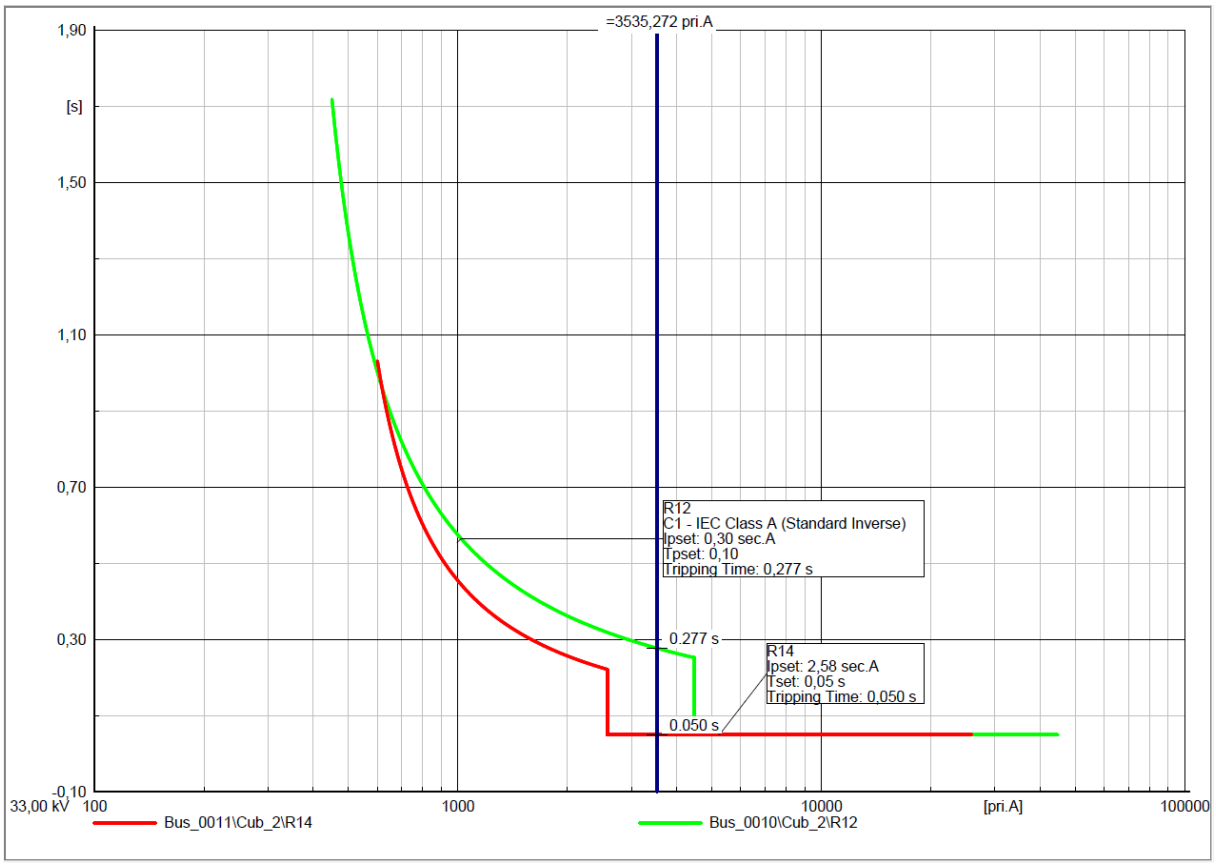

Figure 3.13: TCC for the primary relay R14 and backup relay R12

Table 3.28: Summary of tripping times during a close-in fault at Bus_0011 and Line_0006_0011

Relay	Protection element	Fault current (A)	Tripping time (s)
R14	51P	3535.27	0.189
	67P1	3535.27	0.050
R12	51P	3535.27	0.277
	67P1	3535.27	9999.999

Table 3.29: Summary of protection settings during grid-connected mode

Relay	Stage	PS (sec. A)	TD	Characteristic curve	Directional
R1	51P	0.55	0.08	IEC Std Inverse	Forward
	67P1	5.67	0.05	Definite time	Forward
R2	51P	0.55	0.05	IEC Std Inverse	Forward
	67P1	OFF	OFF	OFF	OFF
R3	51P	0.37	0.06	IEC Std Inverse	Forward
	67P1	2.23	0.05	Definite time	Forward
R4	51P	0.37	0.13	IEC Std Inverse	Forward
	67P1	4.14	0.05	Definite time	Forward
R5	51P	0.74	0.05	IEC Std Inverse	Forward
	67P1	1.38	0.05	Definite time	Forward
R6	51P	0.45	0.07	IEC Std Inverse	Forward
	67P1	3.76	0.05	Definite time	Forward
R7	51P	0.45	0.06	IEC Std Inverse	Forward
	67P1	2.51	0.05	Definite time	Forward
R8	51P	0.50	0.05	IEC Std Inverse	Forward
	67P1	2.20	0.05	Definite time	Forward
R9	51P	0.50	0.08	IEC Std Inverse	Forward
	67P1	4.82	0.05	Definite time	Forward
R10	51P	0.41	0.10	IEC Std Inverse	Forward
	67P1	7.03	0.05	Definite time	Forward
R11	51P	0.41	0.07	IEC Std Inverse	Forward
	67P1	OFF	OFF	OFF	OFF
R12	51P	0.30	0.10	IEC Std Inverse	Forward
	67P1	4.46	0.05	Definite time	Forward
R13	51P	0.30	0.16	IEC Std Inverse	Forward
	67P1	4.13	0.05	Definite time	Forward
R14	51P	0.40	0.06	IEC Std Inverse	Forward
	67P1	2.58	0.05	Off	Off
R15	51P	0.40	0.10	IEC Std Inverse	Forward
	67P1	7.08	0.05	Definite time	Forward
R16	51P	0.74	0.09	IEC Std Inverse	Forward
	67P1	8.63	0.05	Definite time	Forward

Table 3.30: Summary of relay tripping times during grid-connected mode

Primary relay	Backup relay	Fault current measured by the primary relay (kA)	Fault current measured by the backup relay (kA)	Tripping time for primary relay (s)	Tripping time for backup relay (s)	CTI (s)
R1	R5	18.062	0.971	0.05	9999.999	No trip
R1	R14	18.062	2.001	0.05	0.257	0.207
R2	R4	3.256	3.256	0.193	0.409	0.216
R3	R1	4.461	4.461	0.05	0.262	0.212
R4	R7	8.732	1.975	0.05	0.280	0.230
R4	R16	8.732	6.757	0.05	0.279	0.229
R5	R3	3.712	1.739	0.05	0.267	0.217
R5	R7	3.712	1.987	0.05	0.279	0.229
R6	R3	8.436	1.723	0.05	0.269	0.219
R6	R16	8.436	6.734	0.05	0.279	0.229
R7	R9	3.807	3.807	0.05	0.270	0.220
R8	R6	2.967	2.967	0.05	0.255	0.205
R9	R11	8.166	2.663	0.05	0.257	0.207
R10	R8	7.280	1.740	0.05	0.277	0.227
R11	R13	3.279	3.279	0.231	0.457	0.226
R12	R10	5.581	5.581	0.05	0.261	0.211
R13	R15	5.584	5.584	0.05	0.259	0.209
R14	R12	3.535	3.535	0.05	0.277	0.227
R15	R2	16.487	0.263	0.05	9999.999	No trip
R15	R5	16.487	1.027	0.05	9999.999	No trip
R16	R2	17.526	0.234	0.05	9999.999	No trip
R16	R14	17.526	2.016	0.05	0.256	0.206

3.5.3 Case study 2: Overcurrent coordination study for the islanded mode of operation

Both the 100 MVA synchronous generator and 50 MW wind farm are in operation during the islanded mode of operation. The output from the DGs is provided in Table 3.18. Relay R1 measures a current of 146 A during normal operation, and the I_{STM} is 384 A. A pickup current of 580 A (approximately 1.5 x I_{STM}) is selected for the phase overcurrent (51P) setting. Relay R1 measures a far bus fault current of 3624 A. A pickup current of 4530 A (1.25 x I_{FB}) is selected for the instantaneous overcurrent

setting (50P). During a close-in fault at Bus_0006 and Line_0006_0012, the primary relay R1 measures a 3-ph fault current of 10528 A. The 67P1 element initiates a trip at a time of 0.05 s. The backup relay R5 measures a 3-ph fault current of 374 A and initiates a trip at a time of 9999.999 s. There is a loss of coordination between relay R5 and relay R1. The backup relay R14 measures a 3-ph fault current of 792 A and initiates a trip at a time of 0.569 s. This gives a CTI of 0.569 – 0.05 = 0.519 s. Figure 3.14 and Table 3.31 show the measured fault currents and tripping times for relays R1, R5 and R14.

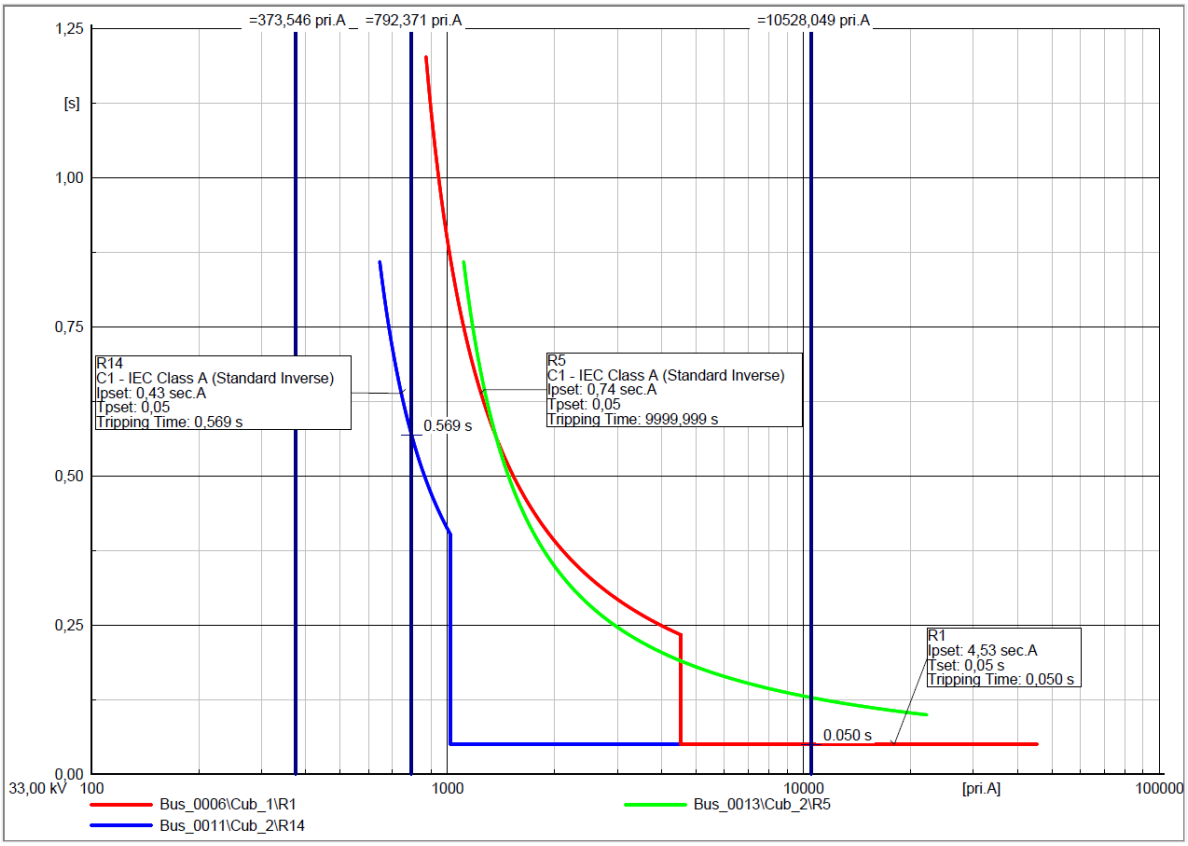

Figure 3.14: TCC for the primary relay R1 and backup relays R5 and R14

Table 3.31: Summary of tripping times during a close-in fault at Bus_0006 and Line_0006_0012

Relay	Protection element	Fault current (A)	Tripping time (s)
R1	51P	10528.05	0.164
	67P1	10528.05	0.050
R5	51P	373.55	9999.999
	67P1	373.55	9999.999
R14	51P	792.37	0.569
	67P1	792.37	9999.999

Relay R14 measures a current of 201 A during normal operation, and the I_{STM} is 288 A. A pickup current of 430 A is selected for the phase overcurrent (51P) setting. Relay R14 measures a far bus fault current of 815 A. A pickup current of 1020 A (approximately 1.25 x I_{FB}) is selected for the instantaneous overcurrent setting (50P). During a close-in fault at Bus_0006 and Line_0006_0011, the primary relay R14 measures a 3-ph fault current of 1827 A. The 67P1 element initiates a trip at a time of 0.05 s. The backup relay R12 measures the same 3-ph fault current of 1827 A and initiates a trip at a time of 0.291 s. This gives a CTI of 0.291 – 0.05 = 0.241 s. Figure 3.15 and Table 3.32 show the measured fault currents and tripping times for relays R14 and R12. The summary of the protection settings for all the identified relay pairs are shown in Table 3.33, whereas Table 3.34 provides the summary of all the measured fault currents and tripping times during the islanded mode.

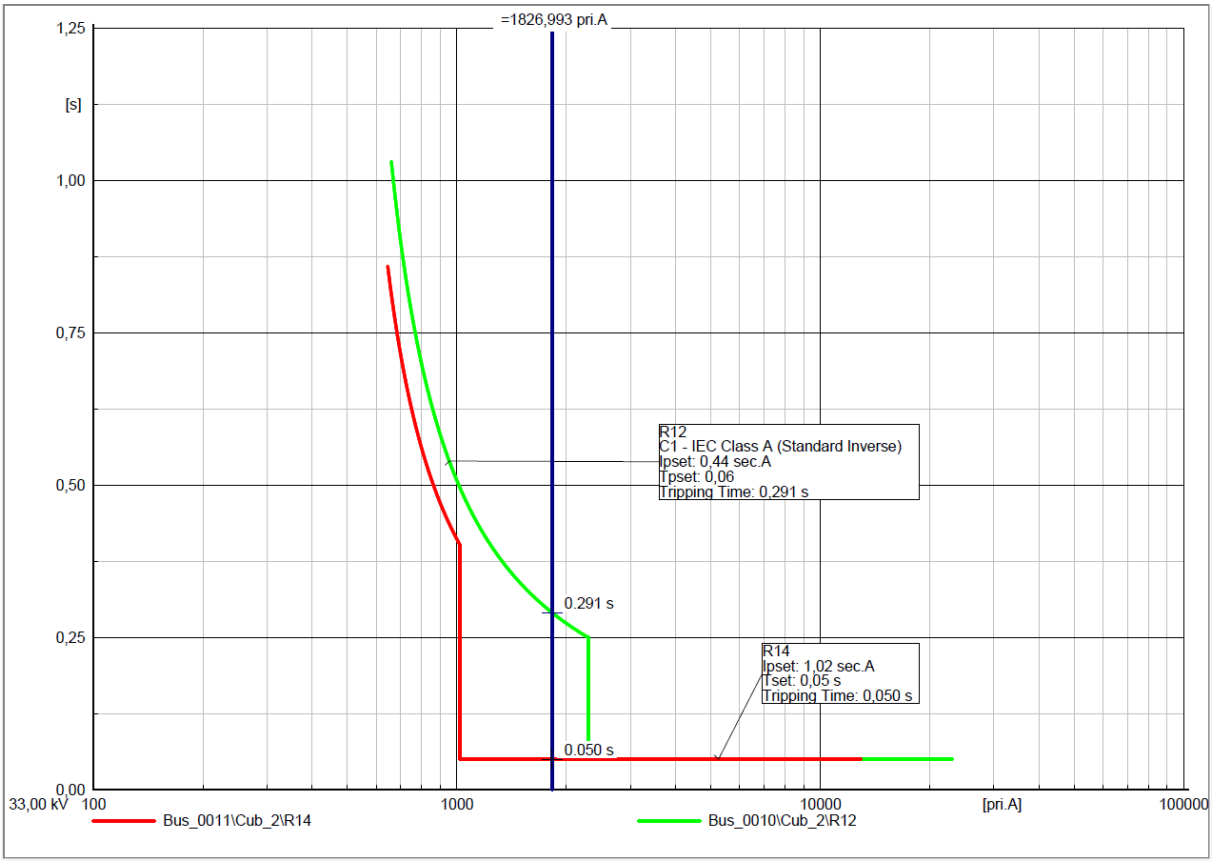

Figure 3.15: TCC curves for the primary relay R14 and backup relay R12

Table 3.32: Summary of tripping times during a close-in fault at Bus_0011 and Line_0006_0011

Relay	Protection element	Fault current (A)	Tripping time (s)
R14	51P	1826.99	0.238
	67P1	1826.99	0.050
R12	51P	1826.99	0.291

	67P1	1826.99	9999.999

Table 3.33: Summary of protection settings during islanded mode

Relay	Stage	PS (sec. A)	TD	Characteristic curve	Directional
R1	51P	0.58	0.07	IEC Std Inverse	Forward
	67P1	4.53	0.05	Definite time	Forward
R2	51P	0.58	0.05	IEC Std Inverse	Forward
	67P1	OFF	OFF	OFF	OFF
R3	51P	0.41	0.09	IEC Std Inverse	Forward
	67P1	1.63	0.05	Definite time	Forward
R4	51P	0.41	0.12	IEC Std Inverse	Forward
	67P1	3.27	0.05	Definite time	Forward
R5	51P	0.74	0.05	IEC Std Inverse	Forward
	67P1	OFF	OFF	OFF	OFF
R6	51P	0.45	0.07	IEC Std Inverse	Forward
	67P1	3.12	0.05	Definite time	Forward
R7	51P	0.45	0.07	IEC Std Inverse	Forward
	67P1	1.48	0.05	Definite time	Forward
R8	51P	0.56	0.07	IEC Std Inverse	Forward
	67P1	1.87	0.05	Definite time	Forward
R9	51P	0.56	0.06	IEC Std Inverse	Forward
	67P1	2.96	0.05	Definite time	Forward
R10	51P	0.57	0.06	IEC Std Inverse	Forward
	67P1	OFF	OFF	OFF	OFF
R11	51P	0.57	0.06	IEC Std Inverse	Forward
	67P1	OFF	OFF	OFF	OFF
R12	51P	0.44	0.06	IEC Std Inverse	Forward
	67P1	2.30	0.05	Definite time	Forward
R13	51P	0.44	0.13	IEC Std Inverse	Forward
	67P1	3.42	0.05	Definite time	Forward
R14	51P	0.43	0.05	IEC Std Inverse	Forward
	67P1	1.02	0.05	Definite time	Forward
R15	51P	0.43	0.09	IEC Std Inverse	Forward
	67P1	5.52	0.05	Definite time	Forward
R16	51P	0.74	0.07	IEC Std Inverse	Forward
	67P1	6.29	0.05	Definite time	Forward

Table 3.34: Summary of tripping times for relays during islanded mode

Primary relay	Backup relay	Fault current measured by the primary relay (kA)	Fault current measured by the backup relay (kA)	Tripping time for primary relay (s)	Tripping time for backup relay (s)	CTI (s)
R1	R5	10.528	0.374	0.05	9999.999	No trip
R1	R14	10.528	0.792	0.05	0.569	0.519
R2	R4	2.570	2.570	0.232	0.449	0.217
R3	R1	3.567	3.567	0.05	0.265	0.215
R4	R7	6.115	1.165	0.05	0.510	0.460
R4	R16	6.115	4.950	0.05	0.253	0.203
R5	R3	2.422	1.269	0.292	0.551	0.259
R5	R7	2.422	1.166	0.292	0.510	0.218
R6	R3	6.184	1.263	0.05	0.554	0.504
R6	R16	6.184	4.936	0.05	0.253	0.203
R7	R9	2.347	2.347	0.05	0.289	0.239
R8	R6	2.463	2.463	0.05	0.283	0.233
R9	R11	3.591	2.279	0.05	0.299	0.249
R10	R8	2.794	1.482	0.260	0.499	0.239
R11	R13	2.718	2.718	0.265	0.491	0.226
R12	R10	2.482	2.482	0.05	0.281	0.231
R13	R15	4.364	4.364	0.05	0.266	0.216
R14	R12	1.827	1.827	0.05	0.291	0.241
R15	R2	9.896	0.102	0.05	9999.999	No trip
R15	R5	9.896	0.397	0.05	9999.999	No trip
R16	R2	10.302	0.085	0.05	9999.999	No trip
R16	R14	10.302	0.788	0.05	0.575	0.525

3.6 Conclusion

This chapter focused on the modelling and simulation of the microgrid system in the DIgSILENT simulation environment. The 33 kV distribution part of the modified IEEE 14-bus system is considered a case study, with an additional DG added to improve the reliability of the system during the islanded mode of operation.

DIgSILENT was used for the load flow analysis, calculating short-circuit currents and protection coordination study of the IEEE 14 bus system. Because the fault current can

flow in either direction through the line, DOCRs are needed. The trip direction of the DOCRs is into the line that is protected. There are 16 SEL-351 DOCRs added to the network to protect each end of the 8 transmission lines. The calculated settings ensure sufficient coordination between the primary and backup relays.

The change in the network topology from a grid-connected mode to an islanded mode of operation causes miscoordination between the primary and backup relays without the implementation of adaptive protection. Both grid-connected and islanded modes of operation were considered for the coordination study. A CTI of at least 0.20 s was achieved between most primary and backup relay pairs for both network topologies. The loss of coordination between the primary and backup relays occured when the backup relay's measured fault current was below the relay's pickup current setting.

CHAPTER 4
MODELLING OF THE MICROGRID SYSTEM IN RSCAD SIMULATION ENVIRONMENT

4.1 Introduction

The Real-Time Digital Simulator (RTDS) utilises hardware and software components to simulate the power system in real-time. Engineers can configure the power system using the Real-Time Simulator Computer-Aided Design (RSCAD) software. RSCAD allows for detailed modelling of generators, transformers, transmission lines, and renewable energy sources. The performance of a power system can be evaluated using RSCAD under various operating conditions and disturbances. Engineers can connect actual equipment to the simulator and test protection, control, and power system components using the hardware-in-the-loop (HIL) feature of RSCAD, providing an accurate representation of the power system (RTDS manual, 2022). This chapter aims to demonstrate the real-time simulation of the modified IEEE 14-bus system by incorporating distributed generators (DGs). The analysis contributes to a better understanding of how DGs can be integrated into power systems to provide improved overall reliability.

Section 4.2 of this chapter focuses on the detailed modelling of the modified IEEE 14-bus network in the RSCAD software. The configuration of the power system components in the RSCAD draft is as follows:

4.2.1 Synchronous generator
4.2.2 Voltage source
4.2.3 Wind turbine
4.2.4 Permanent magnet synchronous generator (PMSG)
4.2.5 Power electronics converter circuit
4.2.6 Transformers
4.2.7 Transmission lines

Section 4.3 of this chapter focuses on the simulation of the modified IEEE 14-bus network in theRSCAD runtime. The real-time simulation investigates the wind turbine generators (WTG) response to steady-state and transient conditions during a three-phase fault. Additionally, the output power of the WTG is evaluated at various wind speed conditions.

4.2 Modelling of the modified IEEE 14-bus system in RSCAD

The network is divided into two subsystems, as shown in Figure 4.1. This is due to the network's scale and processing cards' capabilities. Subsystem 1 (Rack 1) represents the 33 kV distribution network of the modified IEEE 14-bus system and Subsystem 2 (Rack 2) represents the 50 MW wind farm.

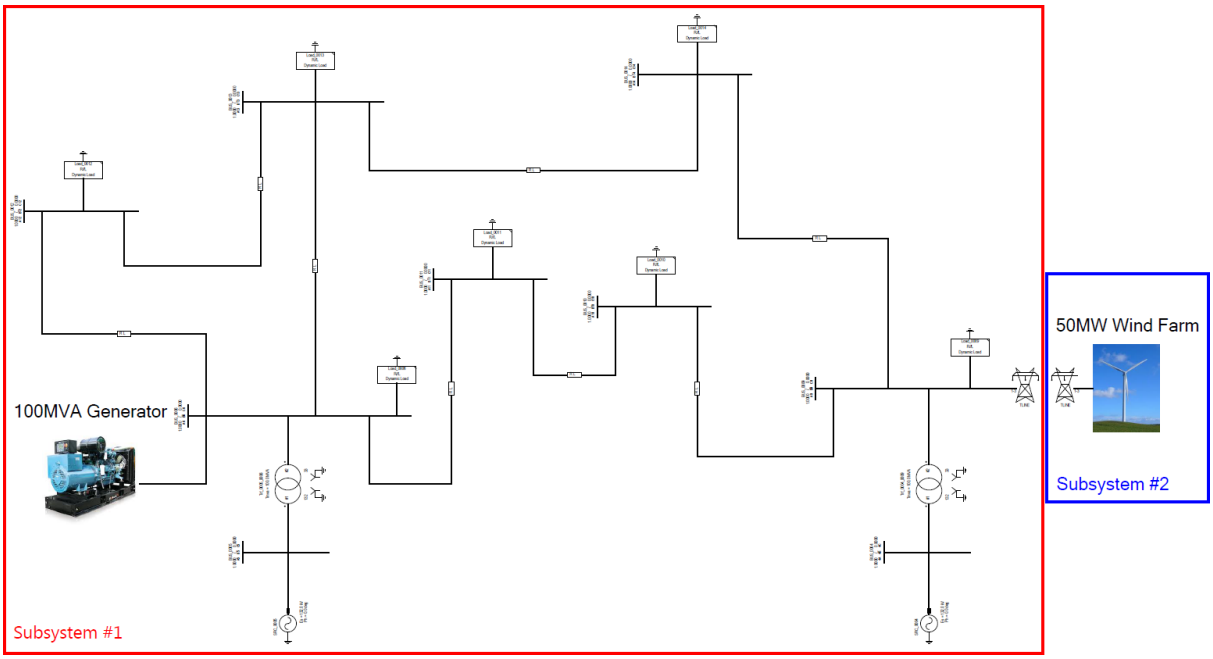

Figure 4.1: Modified IEEE 14-bus system modelled in RSCAD

The additional DG consists of a 50 MW wind farm. The draft components for the 50 MW wind farm are shown in Figure 4.2. This includes the wind turbine, PMSG, AC-DC- AC converter, step-up transformer, and all the controls associated with these components.

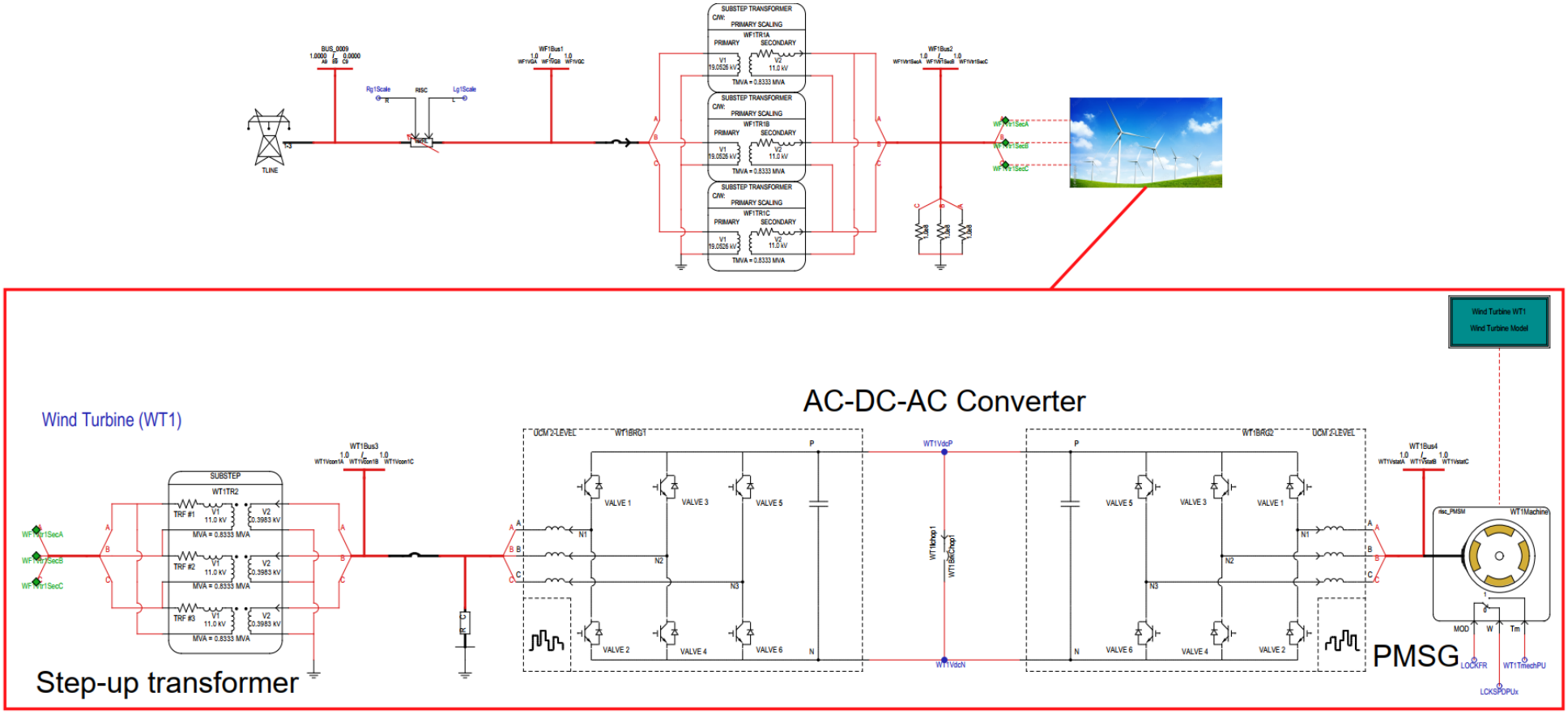

Figure 4.2: 50 MW wind farm model in RSCAD

The parameters for the modified IEEE 14-bus system are given in Tables 4.1 to 4.4.

Table 4.1: Transformer parameters

Description	Size (MVA)	Voltage (kV)	Vector Group	Leakage inductance (p.u.)
Trf_0005_0006	100	132/33	YNyn0	0.25202
Trf_0004_0009	100	132/33	YNyn0	0.55618

Table 4.2: Load parameters

Description	Active Power (MW)	Reactive Power (Mvar)
Load_0006	11.2	7.5
Load_0009	29.5	16.6
Load_0010	9	5.8
Load_0011	3.5	1.8
Load_0012	6.1	1.6
Load_0013	13.5	5.8
Load_0014	14.9	5

Table 4.3: Transmission line parameters

Description	Rated Voltage (kV)	Positive Sequence Resistance (Ohms/km)	Series inductance (H)
Line_0006_0011	33	1.0343322	0.0068947
Line_0006_0012	33	1.3384899	0.0088674
Line_0006_0013	33	0.7203735	0.0045157
Line_0009_0010	33	0.3464109	0.0029291
Line_0009_0014	33	1.3842279	0.0093724
Line_0010_0011	33	0.8935245	0.0066579
Line_0012_0013	33	2.4058188	0.0069286
Line_0013_0014	33	1.8614277	0.0120638

The reactance for the transmission lines in the modified IEEE 14-bus system is given in per-unitvalues. Series inductance values are required for the configuration of RLC models in RSCAD. The series inductance is calculated using equations 4.1 to 4.3.

$$X_b = \frac{kV^2}{MVA_b} = \frac{(33)^2}{100} = 10.89\ \Omega \qquad \textbf{Equation 4.1}$$

$$X_{actual} = X_{pu} \times X_b \qquad \textbf{Equation 4.2}$$

$$L = \frac{X}{2\pi f} \qquad \textbf{Equation 4.3}$$

4.2.1 Modelling of the source

The parameters for the voltage source are given in Table 4 . 4 . The short-circuit MVA rating is 10000 MVA at 132 kV (IEC 60076-5: 2006). The X/R ratio is 10.

Table 4.4: Voltage source parameters

Description	Source Impedance Type	Voltage (kV)	Frequency (Hz)	Pos. seq. impedance (Ω)	Pos. seq. impedance phase angle (deg)
SRC_0004, SRC_0005	R-R//L	132	50	1.7424	84.2894

The following formula calculates the positive sequence impedance and phase angle:

$$\boldsymbol{Z_1 = \frac{kV^2}{MVA_{SC}} = \frac{(132)^2}{10000} = 1.7424\ \Omega}$$

$$\boldsymbol{\delta = tan^{-1}(10) = 84.2894°}$$

4.2.2 Modelling of the synchronous generator

The synchronous generator operates at synchronous speed and is controlled by the grid's frequency. The speed of the synchronous generator is determined by the frequency of the rotating field and the number of pole pairs of the rotor. The 100 MVA synchronous generator model is depicted in Figure 4.3. This includes a IEEE Type 1 excitation system and TGOV1 governor. The parameters for the general model configuration are shown in Table 4.5, while the configuration for the generator d-axis and q-axis reactance values are given in Table 4.6. The rotor has two axes of mechanical rectangular symmetry called the q-axis and the d-axis. The d-axis is the axis from the axial center point in the pole direction, while the q-axis is the axis from the axial center point in the direction 90° leading the d-axis (Hase, Khandelwal and Kameda, 2019). The configuration of the excitation system and governor draft component are shown in Appendix A.

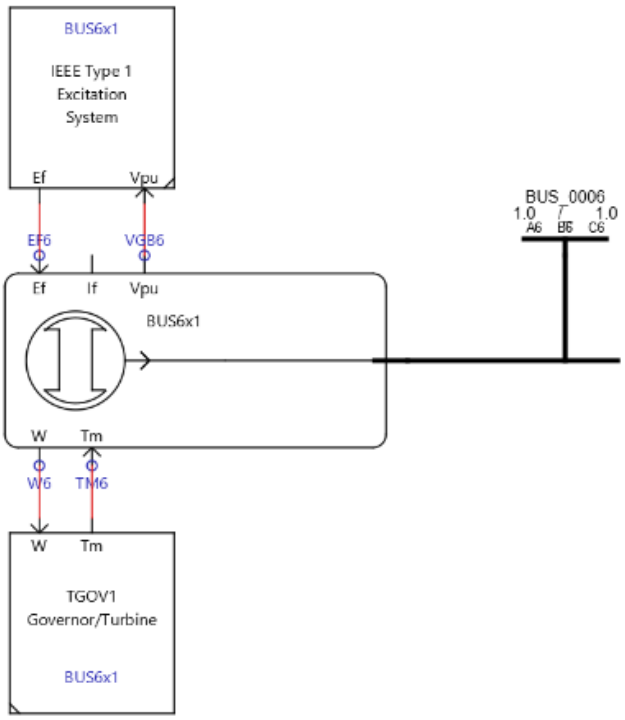

Figure 4.3: Modelling of 100 MVA synchronous generator in RSCAD

Table 4.5: Generator parameters

Description	Size (MVA)	Voltage (kV)	Frequency (Hz)
Gen006	100	33	50

Table 4.6: Configuration of the electrical parameters for the generator model

Name	Description	Value	Unit
Xa	Stator leakage reactance	0.15	p.u.
Xd	D-axis: Unsaturated reactance	1.50	p.u.
Xd’	D-axis: Unsaturated transient reactance	0.30	p.u.
Xd’’	D-axis: Unsaturated sub-transient reactance	0.20	p.u.
Xq	Q-axis: Unsaturated reactance	1.00	p.u.
Xq’	Q-axis: Unsaturated transient reactance	0.30	p.u.
Xq’’	Q-axis: Unsaturated sub-transient reactance	0.20	p.u.
Ra	Stator resistance	0.01	p.u.
Td0’	D-axis: Unsaturated transient open T constant	6.5	s
Td0’’	D-axis: Unsaturated sub-transient open T constant	0.05	s
Tq0’	Q-axis: Unsaturated transient open T constant	0.50	s
Tq0’’	Q-axis: Unsaturated sub-transient open T constant	0.05	s

4.2.3 Modelling of the wind turbine

The wind turbine and the pitch angle control in RSCAD is shown in Figure 4.4. If the power generated is less than the nominal value, the ideal pitch angle is set to zero to optimise turbine power generation. The blades are pitched to limit the rotor speed and the power extracted from the wind when the wind speed exceeds the nominal value. A proportional controller is used to allow for a slight overspeed above the nominal value of the turbine.

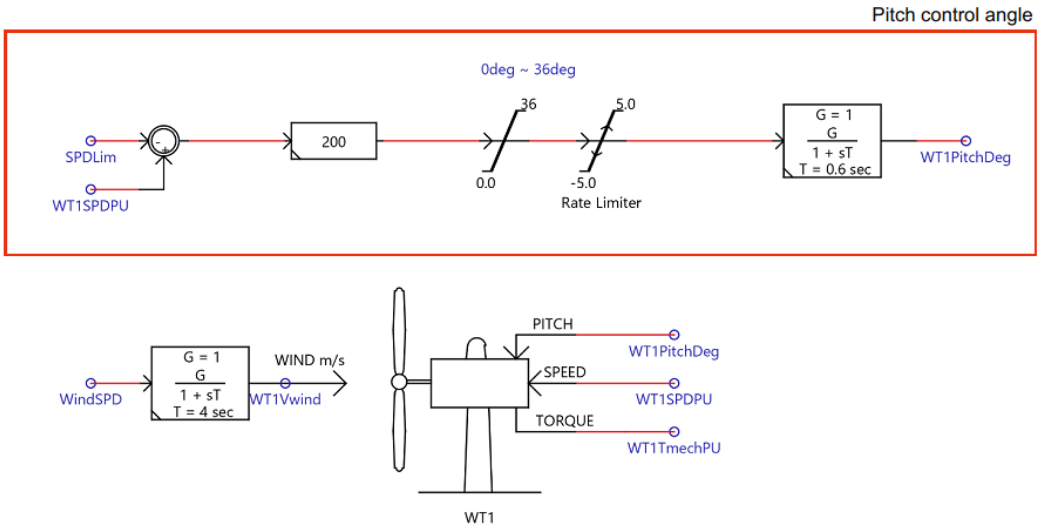

Figure 4.4: Modelling of the wind turbine in RSCAD

The 2.5 MW wind turbine data are configured as shown in Table 4.7. The power rating are set to 2.5 MVA for the generator (GR) and 2.5 MW for the wind turbine (TR). The generator speed, WR, is set at 1.0 p.u. Therefore, the rotor speed is the same as the synchronous speed of the machine. The wind turbine modelin RSCAD uses the per-unit value for torque calculation. The coefficient data for the wind turbine is shown in Table 4.8.

Table 4.7: Configuration of the wind turbine

Name	Description	Value	Unit
GR	Rated generator power	2.5	MVA
TR	Rated turbine power	2.5	MW
WR	PU generator speed @ rated turbine speed	1.0	p.u.
WSR	Rated wind speed	12	m/s
WSCI	Cut-in wind speed	6	m/s

Table 4.8: Configuration of coefficient data for the wind turbine (Youness et al., 2019)

Name	Description	Value	Unit
c1	Cp (lmda, Beta)	0.5176	
c2	c1(c2 * Imdai – c3 * Beta - c4)	116	
c3	Exp(-c5 * Imdai) + c6 * Imda	0.4	
c4		5	
c5	Imdai = (1/(lmda + 0.08*Beta))	21	
c6	(0.035/(Beta*3 + 1)	0.0068	

4.2.4 Modelling of the permanent magnet synchronous generator

The permanent magnet synchronous generator (PMSG) has a wound stator while the rotor is provided with a permanent magnet pole system. The use of a permanent magnet excitation system requires the use of a full-scale power electronics converter to adjust the generators voltage and frequency to match the voltage at the point of coupling (POC) (Letcher et al., 2023). The PMSG model in RSCAD is shown in Figure 4.5. The digital input "*MOD"* specifies the operation mode of the machine. If MOD = 0, then the machine operates in lock mode, and the speed of the machine is controlled by the input control signal *"W"*. If MOD = 1, then the machine operates in free mode, and the mechanical torque is controlled by the input signal *"Tm"*. The PMSG is integrated with a conventional three-phase full-bridge active rectifier or VSC.

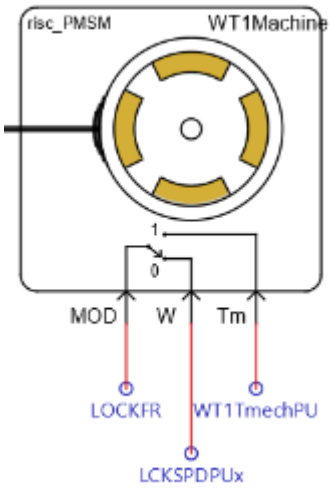

Figure 4.5: PMSG model in RSCAD

The time-domain modelling of the PMSG is based on the dq0 theory. The d-q model for the PMSG is shown in Figure 4.6. The dynamic equations for the operation of the PMSG are presented in a synchronous rotating reference frame (d-q) as follows:

- Stator voltages:

$$\boldsymbol{V_{sd} = R_s \cdot i_{sd} + \frac{d\psi_d}{dt} - \omega_r \cdot \psi_q} \qquad \textbf{Equation 4.4}$$

$$\boldsymbol{V_{sq} = R_s \cdot i_{sq} + \frac{d\psi_q}{dt} - \omega_r \cdot \psi_d} \qquad \textbf{Equation 4.5}$$

- Stator fluxes:

$$\boldsymbol{\psi_d = L_d \cdot i_{sd} + \Phi_f} \qquad \textbf{Equation 4.6}$$

$$\boldsymbol{\psi_q = L_q \cdot i_{sq}} \qquad \textbf{Equation 4.7}$$

Where:

ψ_q, ψ_d is the d-q axis flux in Wb,

i_{sd}, i_{sq} is the d-q stator current in A,

$L_{d,}\, L_q$ is the d-q inductance in H.

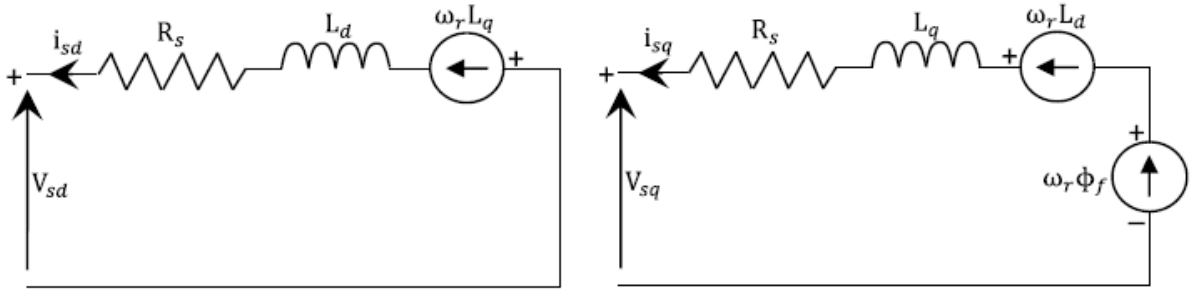

Figure 4.6: **d-q equivalent circuit of the PMSG in the synchronous reference frame (Youness et al., 2019)**

The PMSG model in RSCAD is configured as shown in Table 4.9. These parameters describe the electrical transient behaviour of the machine. The rating of the generator is 2.5 MVA. The mechanical parameters describe the mechanical dynamics of the machine. The constant for the rotational inertia expressed in megawatt seconds of stored energy at the rated speed per MVA of generator rating is set at 3.5 MW/MVA.

Table 4.9: Configuration of the PMSG electrical and mechanical parameters

Name	Description	Value	Unit
Vll_rms	Rated RMS line-to-line voltage	0.69	kV
Srated	Rated MVA of the machine	2.5	MVA
Fb	Rated frequency of the machine	12	Hz
Xlspu	Stator leakage reactance	0.1	p.u.
Xmdpu	D-axis unsaturated magnetic reactance	0.35	p.u.
XIDpu	D-axis damper leakage reactance	0.05	p.u.
Xmqpu	Q-axis magnetising reactance	0.4	p.u.
XIQpu	Q-axis damper leakage reactance	0.045	p.u.
Rspu	Stator resistance	0.01	p.u.
RDpu	D-axis damper resistance	0.035	p.u.
RQpu	Q-axis damper resistance	0.028	p.u.
PsiMpu	Magnetic strength	1.0	Norm
H	Inertia constant	3.5	MWs/MVA
D	Frictional damping	0.0	pu/pu

4.2.5 Modelling of the converter circuits

The converters in the PMSG WTG are used to transmit full-scale power from the generators to the AC grid. The PMSG is integrated into the AC grid with a pulse with amodulation-voltage source consisting of a two-level output voltage (2 L-PWM-VSC). The 2 L-PWM-VSC is configured as a back-to-back converter with a DC link between the 2 L-VSC, as shown in Figure 4.7 (Blaabjerg and Ionel, 2017).

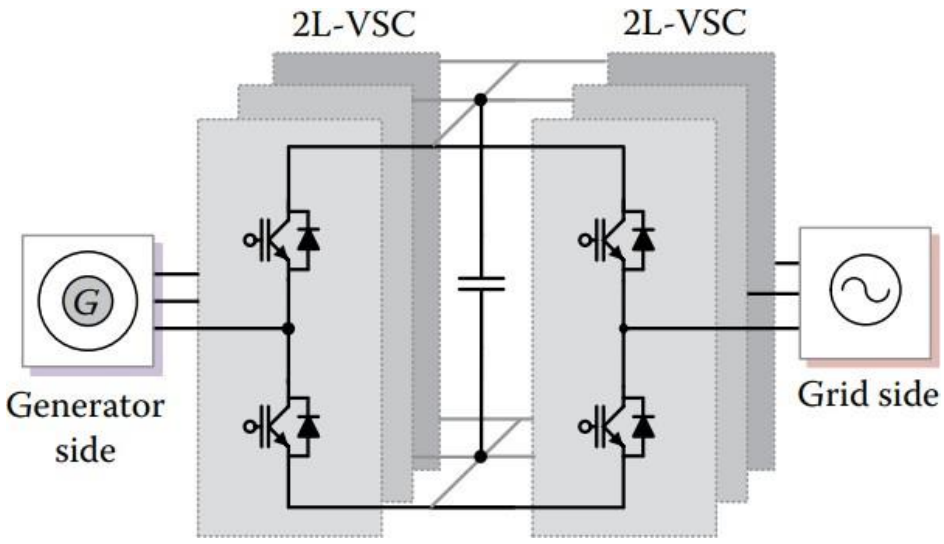

Figure 4.7: Two-level voltage source converter in a back-to-back configuration (Blaabjerg and Ionel, 2017)

The generated current references are compared to the measured current in the d-q frame at the generator-side controls. The signals are fed through PI controllers to generate a voltage reference for the generator model. The grid-side converter is controlled by a d-q reference frame that rotates with the grid voltage. The current measured by the controller regulates the real power transferred to the grid by maintaining the DC-link voltage (Blaabjerg and Ionel, 2017).

The active rectifier controls the voltage, current, and frequency signal outputs from the PMSG.The control for the VSC is implemented in the direct-quadrature (d-q) reference frame to simplify the control scheme needed. The time-varying inductances of the AC source are converted to a DC command. This allows the use of a simple linear compensator such as the proportional-integral (PI) or proportional-integral-derivative (PID) (Bansal et al., 2017).

The grid-side converter comprises an AC inductor, an AC capacitor, and a DC capacitor. The AC inductor suppresses the AC ripple and filters out switching harmonics along with the AC capacitor. The grid-side controller regulates the AC voltage at the 0.69 kV bus connected to the machine-side converter. The VSC converter controls both reactive power (or AC voltage) and active power (or DC voltage). By controlling the VSC terminal voltages at the AC grid, a current controller can regulate the VSC output currents.

In the d-q frame control of a grid-connected VSC system, it is feasible to achieve instantaneous independent regulation of the active and reactive power transferred between the VSC system and the AC system. The power control block diagram in the d-q frame for a grid-connected two-level voltage source converter demonstrates how the d-axis current control enables grid active power control, while the q-axis current control facilitates grid reactive power control.

In addition, the control variables are DC quantities during steady-state conditions. The control of real and reactive power in a grid-imposed VSC system can be achieved through voltage mode control or current-mode control. In a voltage-controlled VSC system, the phase angle and amplitude of the VSC AC-side terminal voltage relative to the PCC voltage govern real and reactive power respectively. The voltage mode control is less complicated because of a lower number of control loops. Current-mode control involves regulating the VSC line current with a dedicated current control scheme through the VSC AC-side terminal voltage; thereafter, real and reactive power is managed by adjusting its phase angle and amplitude of the VSC line current concerning

the PCC's voltage. Thus, due to the current regulation scheme, the VSC system is protected against overcurrent conditions (Yazdani and Iravani, 2010).

The parameters for the grid-side and machine-side converters are configured as shown in Table 4.10. The logic that is modelled in RSCAD for the inner and outer control loops is shown in Appendix B.

Table 4.10: Configuration of the power electronics converter (Yazdani and Iravani, 2010) (RSCAD manual, 2022)

Name	Description	Value	Unit
Indac	The inductance of AC reactor	$120x10^{-6}$	H
Resac	Resistance of AC reactor	$1.0x10^{-6}$	ohms
Capufd	The capacitance of each DC capacitor	35000.0	μF
Capres	Resistance in series with each DC capacitor	0.0	ohms
Rvlon	Valve ON resistance	0.0001	ohms
Rvlof	Valve OFF resistance (block mode)	$100x10^{-6}$	ohms
Snbc	Snubber series capacitance (block mode)	0.01	μF
snbr	Snubber series resistance (block mode)	$1.0x10^{-4}$	ohms

4.2.6 Modelling of transformers

The transformers are connected back-to-back to step up the voltage level from the WTG to the grid. The transformers between the grid-side converter and the scaling transformer at the PCC are used to increase the voltage from 690 to 11000 V. The parameters for the transformer are configured as shown in Table 4.11. The scaling transformer at the PCC is used to increase the voltage from 11 to 33 kV. The parameters for the transformer are configured as shown in Table 4.12.

Table 4.11: Configuration of the parameters for the transformer between the grid-side converter and the scaling transformer at the PCC

Name	Description	Value	Unit
vw1t	Rated winding 1 RMS voltage	11	kV
vw2t	Rated winding 2 RMS voltage	0.398372	kV
MVA	Rated 1-phase transformer MVA	0.83333	MVA
frqt	Transformer base frequency	50	Hz
rput	Total winding resistances	0.001	p.u.
xput	Total winding reactances	0.1	p.u.
mgls1	Winding 1 magnetising losses	0.00001	p.u.
mgls2	Winding 2 magnetising losses	0.00001	p.u.

Table 4.12: Configuration of the parameters for the scaling transformer at the PCC

Name	Description	Value	Unit
vtpri	Rated primary RMS voltage	19.0526	kV
vtsec	Rated secondary RMS voltage	11	kV
TMVA	Rated transformer MVA	0.83333	MVA
freqb	Base frequency	50	Hz
trpos	Leakage resistance	0.001	p.u.
txpos	Leakage reactance	0.1	p.u.

4.2.7 Modelling of the transmission line

The transmission line model is used to connect subsystems 1 and 2. Travelling-wave models represent the transmission lines in RSCAD. RSCAD supports two types of travelling-wave models: Bergeron and frequency-dependent phase. The Bergeron model is selected, as shown in Figure 4.8, considering a line length of 15 km. The Bergeron model is a lossless line with resistances lumped together at terminals and the centre of the line. The line length of 15 km is classified as a short transmission line. The configuration of the transmission line parameters in Tline is shown in Appendix C.

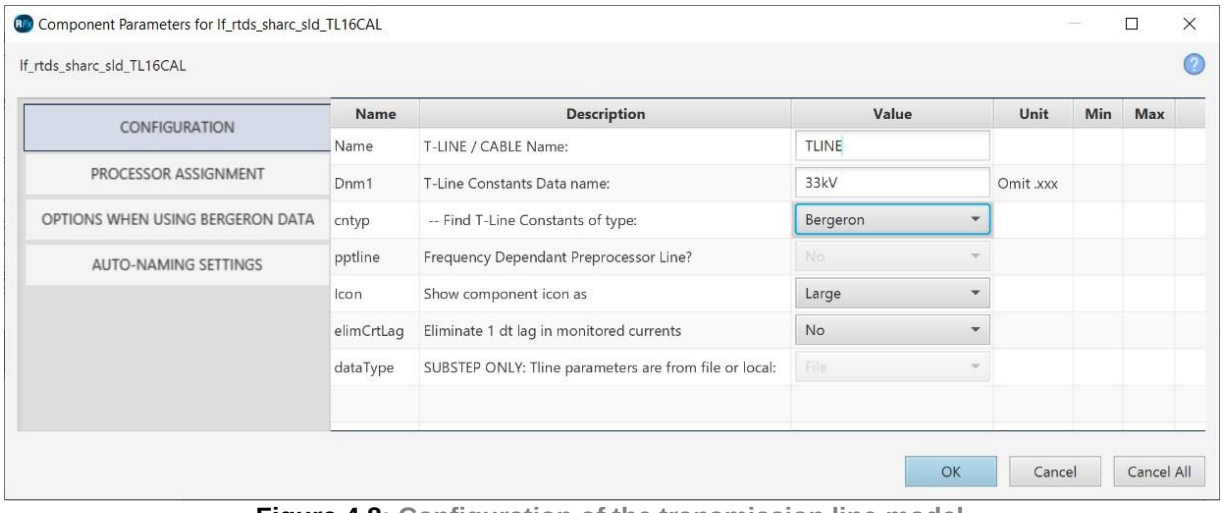

Figure 4.8: Configuration of the transmission line model

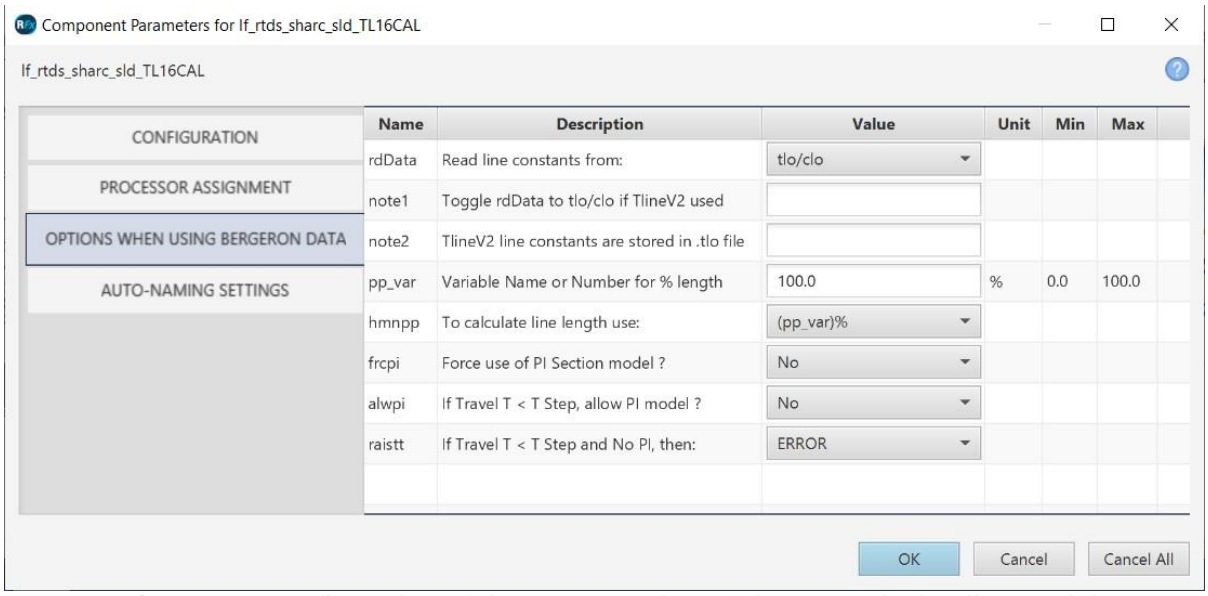

Figure 4.9: **Configuration of the Bergeron data of the transmission line model**

4.3 50 MW type 4 wind turbine simulation results

This section presents the type 4 PMSG wind turbine simulation results in RSCAD runtime and describes the scaling factors to increase the output power of the wind turbine. Transformer scaling can increase the output power from the transformer at the PCC by the scaling factor. The scaling factor can be dynamically adjusted in RSCAD Runtime using the scale slider, as shown in Figure 4.10. The scaling factor is adjusted to 20. The active output power of the wind turbine is increased 20 times the actual rating, i.e. 2.5 MW x 20 = 50 MW.

Only a single WTG's controls is needed when using the transformer scaling feature. This simplifies the network when compared with aggregation models. The WTG can be easily scaled and integrated into the AC network.

The scaling factor will change the parameters needed while ensuring the following criteria (RTDS manual, 2022):

- Maintain the AC grid strength,
- Maintain the per-unit impedance for the AC-side filter,
- Maintain the holding-up time for the DC capacitance.

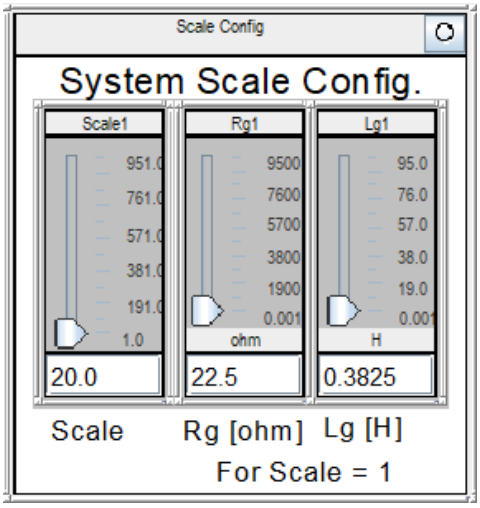

Figure 4.10: Sliders for configuration of the WTG scale in RSCAD Runtime

The control preferences and wind speed must be set before running the simulation. The wind speed is initially set to 12 m/s. After the simulation runs, the *Start* and *DBlk* push buttons, as shown in Figure 4.11, need to be pressed. The *DBlk* push-button is used to deblock the converters, while the *Blk* push-button blocks the converters.

Figure 4.11: Push buttons in RSCAD Runtime

4.3.1 Case Study 1: PMSG wind turbine simulation at a wind speed of 12 m/s

The WTG's active and reactive power, as well as AC and DC voltages, are shown in Figure 4.12. The wind turbine's active is 2.500 MW at a speed of 720.0 rpm (1.000 p.u.). The PMSG supplies an active power of 2.500 MW. The measured DC voltage at the AC-DC-AC converter is 1.199 kV. The active and reactive power at the grid side of the converter is 2.46 MW, and 0.6788 Mvar, respectively. This gives a power factor of 0.964 lagging. The loss through the back-to-back converter is 0.04 MW (1.60%). The active power supplied from the step-up transformer is 2.457 MW. After applying the scaling factor of 20, the wind farm supplies a total active power of 49.02 MW.

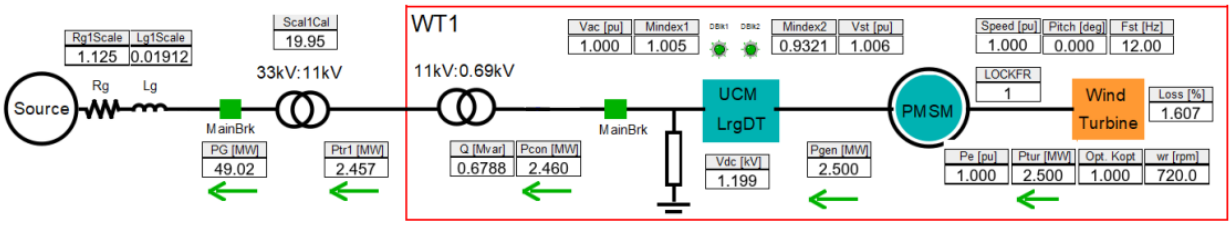

Figure 4.12: **Power output from WTG during the runtime simulation at a wind speed of 12 m/s**

The measured voltages and currents at the grid side of the converter are shown in Figure 4.13. WF1VGA, WF1VGB, and WF1VGC represent the measured three-phase voltages at WF1Bus1 on the HV side of the scaling transformer at the PCC. The measured voltages are 18.3847 kV. The per-unit voltage is calculated as follows:

$$\boldsymbol{V_{base\ (rms)} = \frac{33}{\sqrt{3}} = 19.0526\ kV}$$

$$\boldsymbol{V_{pu} = \frac{V_{actual}}{V_{base}} = \frac{18.3847}{19.0526} = 0.9649\ p.u.}$$

WF1IGA, WF1IGB, and WF1IGC represent the measured three-phase currents from the output of the scaling transformer at the PCC. The measured current is 0.8944 kA. The apparent power is calculated as follows:

$$\boldsymbol{S = 3 \cdot V_{ph} \cdot I_{ph} = 3 \cdot (18.3847)(0.8944) = 49.3298\ MVA}$$

WF1Vtr1SecA, WF1Vtr1SecB, and WF1Vtr1SecC represent the measured three-phase voltages at WF1Bus2 between the step-up transformer at the grid-side converter and the scaling transformer at the PCC. The measured voltage is 6.21 kV. The per-unit voltage is calculated as follows:

$$\boldsymbol{V_{base\ (rms)} = \frac{11}{\sqrt{3}} = 6.3509\ kV}$$

$$\boldsymbol{V_{pu} = \frac{V_{actual}}{V_{base}} = \frac{6.21}{6.3509} = 0.9778\ p.u}$$

WF1Vcon1A, WF1Vcon1B, and WF1Vcon1C represent the measured three-phase voltages at WF1Bus3 between the grid-side converter and the step-up transformer. The measured voltage is 0.3987 kV. The per-unit voltage is calculated as follows:

$$V_{base\,(rms)} = \frac{0.69}{\sqrt{3}} = 0.3984\ kV$$

$$V_{pu} = \frac{V_{actual}}{V_{base}} = \frac{0.3987}{0.3984} = 1.0008\ p.u$$

WF1Icon1A, WF1Icon1B, and WF1con1C represent the measured three-phase currents measured through the step-up transformer. The measured currents are 2.1383 kA. WF1Icon1TA, WF1Icon1TB, and WF1con1TC represent the measured three-phasecurrents measured through the converter. The measured currents are 2.1267 kA. The apparent power and power factor at the step-up transformer is calculated as follows:

$$S = \sqrt{(P^2 + Q^2)} = \sqrt{(2.46^2 + 0.6788^2)} = 2.5519\ MVA$$

$$pf = \frac{P_{con}}{S} = \frac{2.46}{2.5519} = 0.964\ lagging$$

The measured voltages and currents on the machine side of the converter are shown in Figure 4.14. WT1VdcBus1 is the measured DC voltage between the AC-DC-AC converter.The measured value is approximately 1.2 kV. WT1Icon2TA, WT1Icon2TB, and WT1Icon2TC represent the measured three-phase currents going into the machine side of the converter. The measured current is 2.1568 kA. WT1IstatA, WT1IstatB, and WT1StatC represent the stator current of 2.157 kA. WT1VstatTAB, WT1statTBC, and WT1statTCA represent the line-to-line stator voltage of 0.8306 kV. The per-unit voltage is calculated as follows:

$$V_{pu} = \frac{V_{actual}}{V_{base}} = \frac{0.8306}{0.69} = 1.2037\ p.u$$

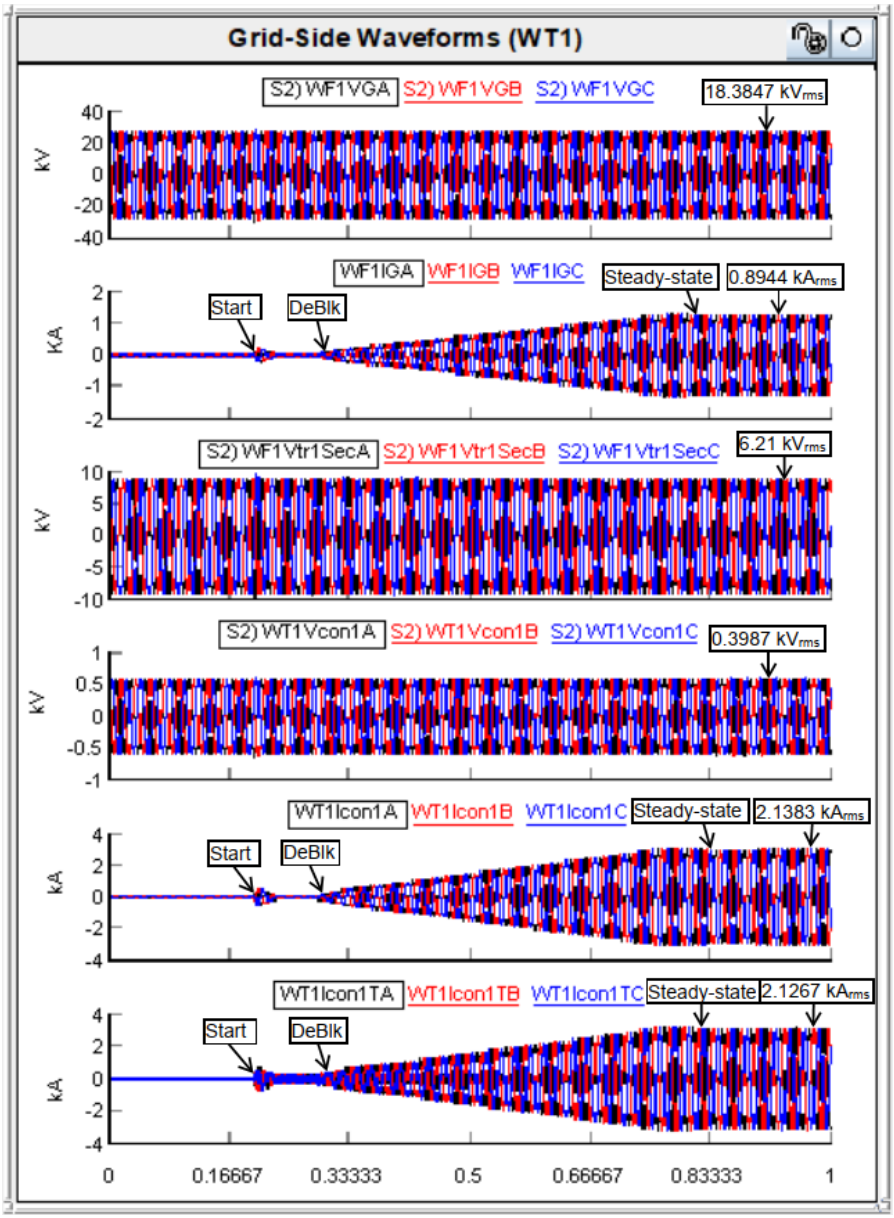

Figure 4.13: Measured voltages and currents at the grid side of the converter during start-up and steady-state conditions at a wind speed of 12 m/s

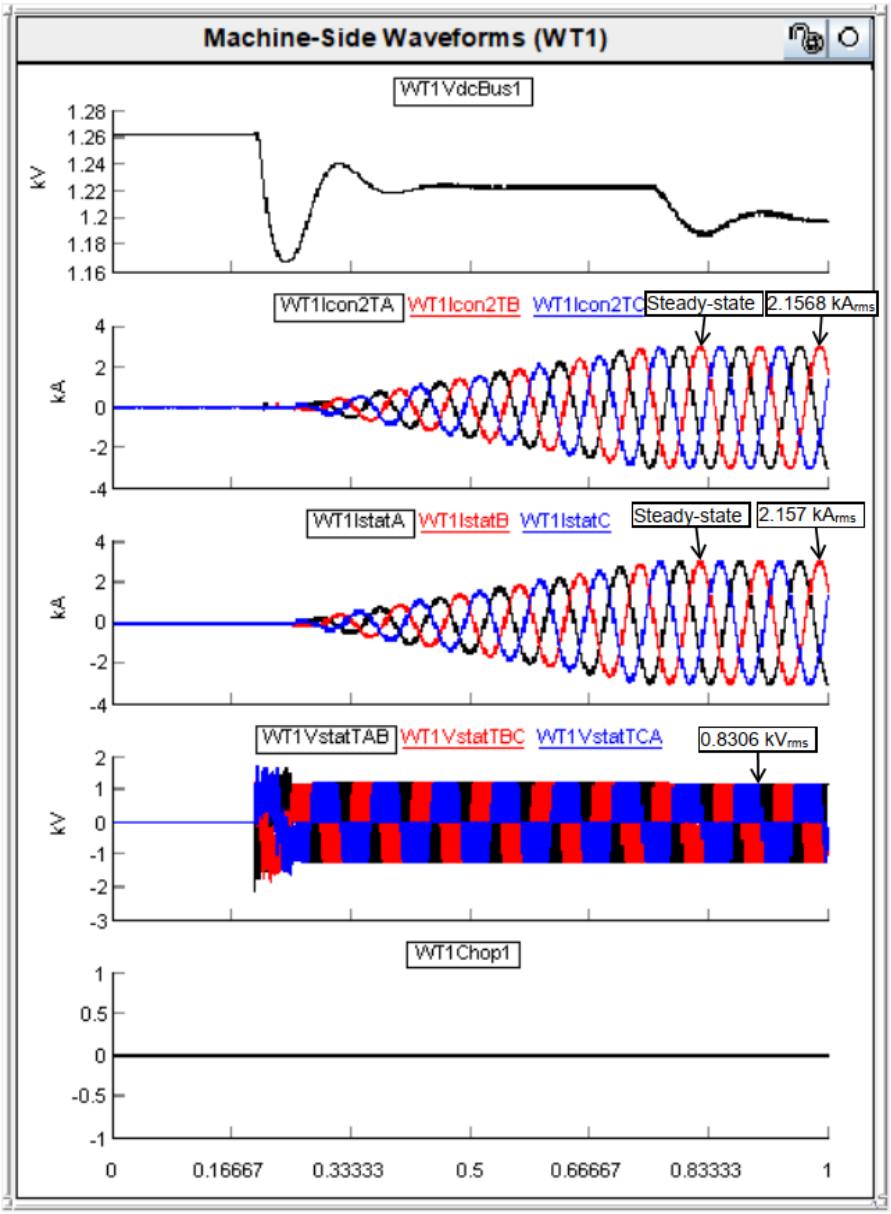

Figure 4.14: **Measured voltages and currents at the machine side of the converter during start-up and steady-state conditions at a wind speed of 12 m/s**

4.3.2 Case Study 2: PMSG wind turbine simulation at a wind speed of 9 m/s:

The WTG's active and reactive power, as well as AC and DC voltages, are shown in Figure 4.15. The wind turbine's active is 1.055 MW at a speed of 540.0 rpm (0.750 p.u.). The PMSG supplies an active power of 1.055 MW. The measured DC voltage at the AC-DC-AC converter is 1.199 kV. The active and reactive power at the grid side of the converter is 1.036 MW, and 0.1495 Mvar, respectively. This gives a power factor of 0.9898 lagging. The loss through the back-to-back converter is 0.019 MW (1.80%). The active power supplied from the step-up transformer is 1.036 MW. After applying the scaling factor of 20, the wind farm supplies a total active power of 20.68 MW.

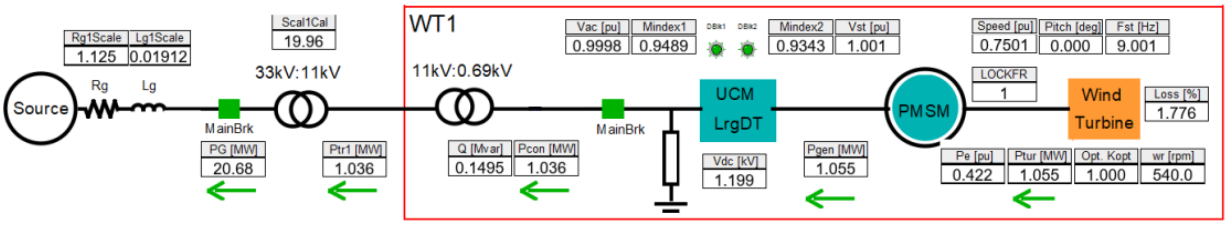

Figure 4.15: Output power from WTG during the runtime simulation at a wind speed of 9 m/s

The measured voltages and currents at the grid side of the converter are shown in Figure 4.16. The measured voltages for WF1VGA, WF1VGB, and WF1VGC are 18.8829 kV. The per-unit voltage is calculated as follows:

$$\boldsymbol{V_{base\,(rms)} = \frac{33}{\sqrt{3}} = 19.0526\ kV}$$

$$\boldsymbol{V_{pu} = \frac{V_{actual}}{V_{base}} = \frac{18.8829}{19.0526} = 0.9911\ p.u.}$$

The measured currents for WF1IGA, WF1IGB, and WF1IGC are 0.3668 kA. The apparent power is calculated as follows:

$$\boldsymbol{S = 3 \cdot V_{ph} \cdot I_{ph} = 3 \cdot (18.8829)(0.3668) = 20.7787\ MVA}$$

The measured voltages for WF1Vtr1SecA, WF1Vtr1SecB, and WF1Vtr1SecC are 6.3212 kV. The per-unit voltage is calculated as follows:

$$\boldsymbol{V_{pu} = \frac{V_{actual}}{V_{base}} = \frac{6.3212}{6.3509} = 0.9953\ p.u}$$

The measured voltages for WF1Vcon1A, WF1Vcon1B, and WF1Vcon1C are 0.3984 kV. The per-unit voltage is calculated as follows:

$$\boldsymbol{V_{pu} = \frac{V_{actual}}{V_{base}} = \frac{0.3984}{0.3984} = 1.0000\ p.u}$$

The measured currents for WF1Icon1A, WF1Icon1B, and WF1con1C are 0.8767 kA, while the currents for WF1Icon1TA, WF1Icon1TB, and WF1con1TC are 0.8779 kA. The apparent power and power factor at the step-up transformer is calculated as follows:

$$S = \sqrt{(P^2 + Q^2)} = \sqrt{(1.036^2 + 0.1495^2)} = 1.0467\ MVA$$

$$pf = \frac{P_{con}}{S} = \frac{1.036}{1.0467} = 0.9898\ lagging$$

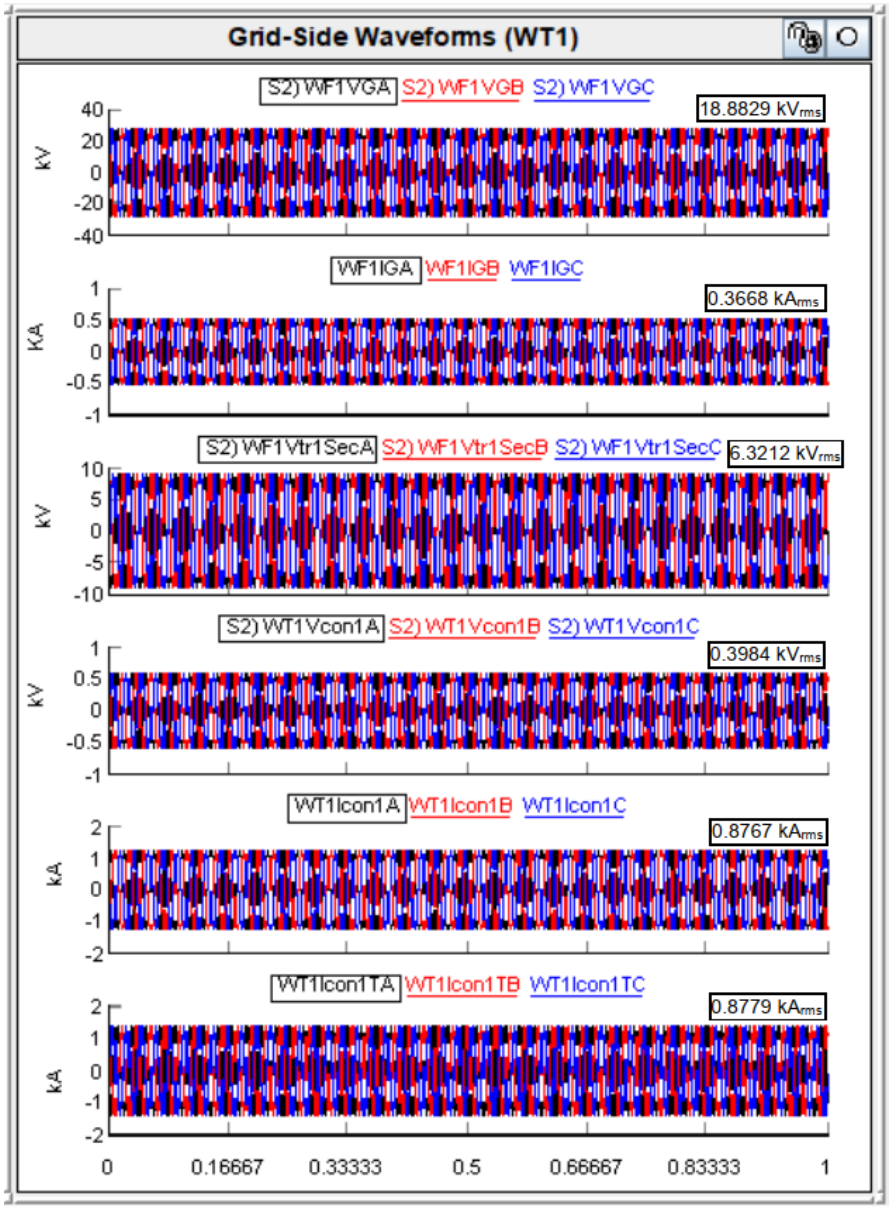

Figure 4.16: Measured voltages and currents at the grid side of the converter for a wind speed of 9 m/s

4.3.3 Case Study 3: PMSG wind turbine simulation at a wind speed of 6 m/s:

The WTG's active and reactive power, as well as AC and DC voltages, are shown in Figure 4.17. The wind turbine's active power is 0.3125 MW at a speed of 360.0 rpm (0.500 p.u.). The PMSG supplies an active power of 0.3121 MW. The measured DC voltage at the AC-DC-AC converter is 1.200 kV. The active and

reactive power at the grid side of the converter is 0.2552 MW, and 0.1078 Mvar, respectively. This gives a power factor of 0.964 lagging. The loss through the back-to-back converter is 0.057 MW (18.23%). The active power supplied from the step-up transformer is 0.2551 MW. After applying the scaling factor of 20, the wind farm supplies a total active power of 5.061 MW.

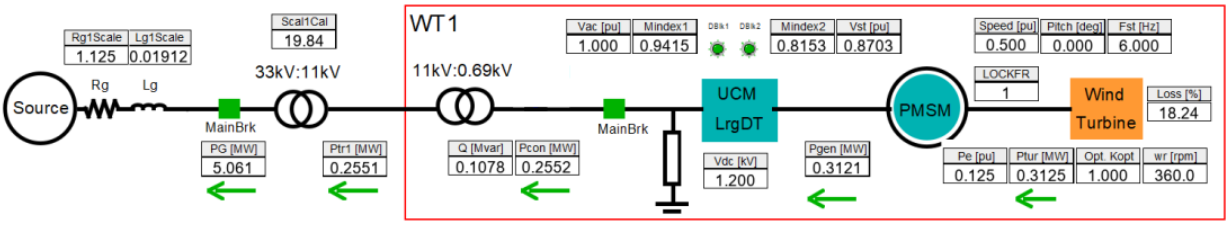

Figure 4.17: **Power output from the WTG during the runtime simulation at a wind speed of 6 m/s**

The measured voltages and currents at the grid side of the converter are shown in Figure 4.18. The measured voltages for WF1VGA, WF1VGB, and WF1VGC are 18.8983 kV. The per-unit voltage is calculated as follows:

$$V_{pu} = \frac{V_{actual}}{V_{base}} = \frac{18.8983}{19.0526} = 0.9919\ p.u.$$

The measured currents for WF1IGA, WF1IGB, and WF1IGC are 0.0978 kA. The apparent power is calculated as follows:

$$S = 3 \cdot V_{ph} \cdot I_{ph} = 3 \cdot (18.8983)(0.0978) = 5.5448\ MVA$$

The measured voltages for WF1Vtr1SecA, WF1Vtr1SecB, and WF1Vtr1SecC are 6.3238 kV. The per-unit voltage is calculated as follows:

$$V_{pu} = \frac{V_{actual}}{V_{base}} = \frac{6.3238}{6.3509} = 0.9957\ p.u$$

The measured voltages for WF1Vcon1A, WF1Vcon1B, and WF1Vcon1C are 0.3985 kV. The per-unit voltage is calculated as follows:

$$V_{pu} = \frac{V_{actual}}{V_{base}} = \frac{0.3985}{0.3984} = 1.0003\ p.u$$

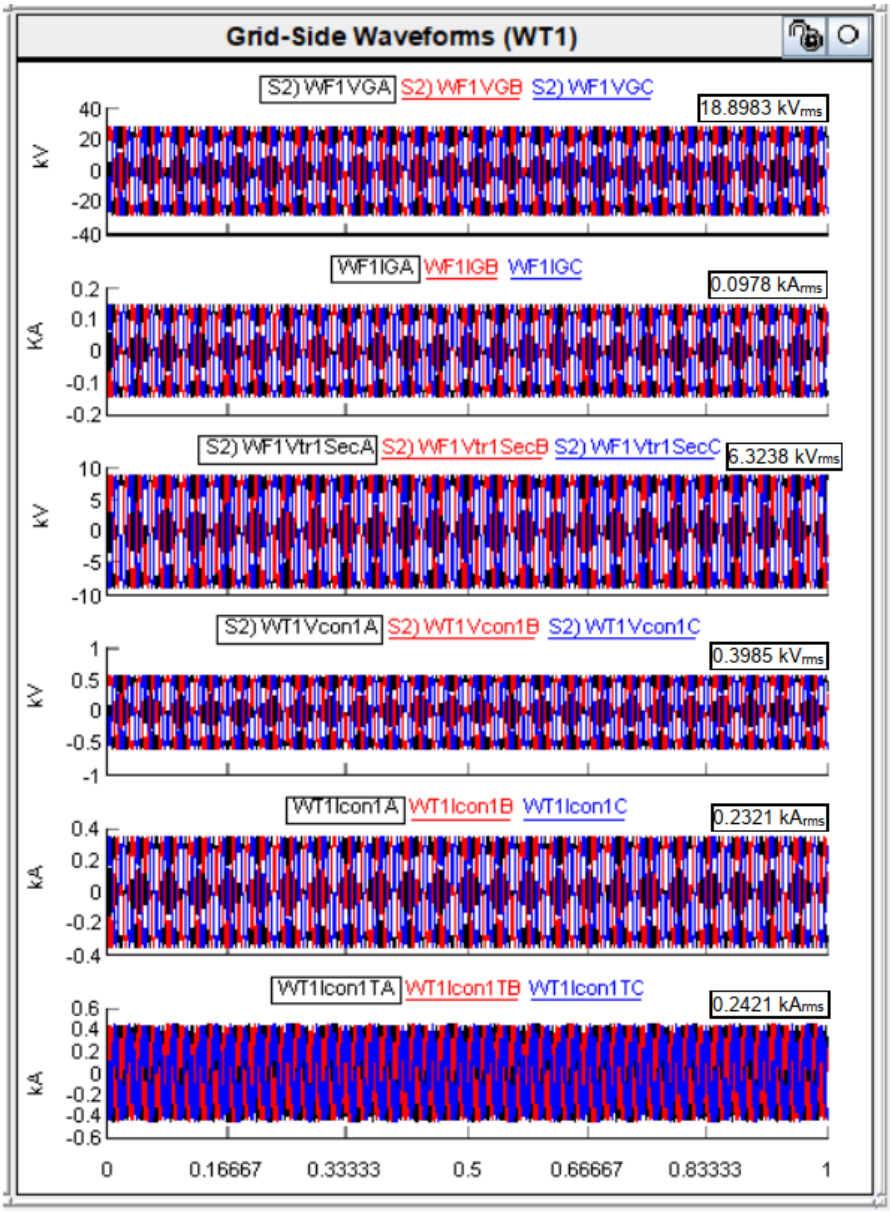

Figure 4.18: **Measured voltages and currents at the grid side of the converter for a wind speed of 6 m/s**

The measured currents for WF1Icon1A, WF1Icon1B, and WF1con1C are 0.2321 kA, while the currents for WF1Icon1TA, WF1Icon1TB, and WF1con1TC are 0.2421 kA. The apparent power and power factor at the step-up transformer is calculated as follows:

$$\boldsymbol{S = \sqrt{(P^2 + Q^2)} = \sqrt{(0.2552^2 + 0.1078^2)} = 0.277\ MVA}$$

$$\boldsymbol{pf = \frac{P_{con}}{S} = \frac{0.2552}{0.277} = 0.9213\ lagging}$$

4.3.4 Power output from WTG at various wind speeds

The real and reactive power output from the WTG for a wind speed ranging from 3 m/s to 25 m/s is shown inf Table 4.13. The real and reactive power at a wind speed of 12 m/s are 2.460 MW and 0.6788 Mvar, respectively.

Table 4.13: Power output from WTG at various wind speeds

Windspeed (m/s)	Pgen (MW)	Pcon (MW)	Q (Mvar)	PG (MW)
3	0	0	0	0
4	0.0923	0.0293	0.1257	0.5374
5	0.1813	0.1209	0.1168	2.373
6	0.3121	0.2552	0.1078	5.061
7	0.4939	0.4439	0.1031	8.837
8	0.7417	0.7126	0.1126	14.21
9	1.055	1.036	0.1495	20.68
10	1.445	1.428	0.2323	28.50
11	1.927	1.900	0.3916	37.90
12	2.500	2.460	0.6788	49.02
13	2.632	2.586	0.7604	51.54
14	2.724	2.676	0.8234	53.31
15 - 25	2.750	2.702	0.8421	53.82

From Figure 4.19, the following can be observed from the power curve at various wind speeds:

- The cut-in wind speed is at approximately 4 m/s. This is the minimum wind speed at which the wind turbine can deliver useful power.
- The rated wind speed is at 12 m/s. This is the wind speed at which the rated power from the wind turbine is obtained.
- The cut-out wind speed is at 25 m/s. This is the maximum wind speed at which the wind turbine is allowed to deliver mechanical power.

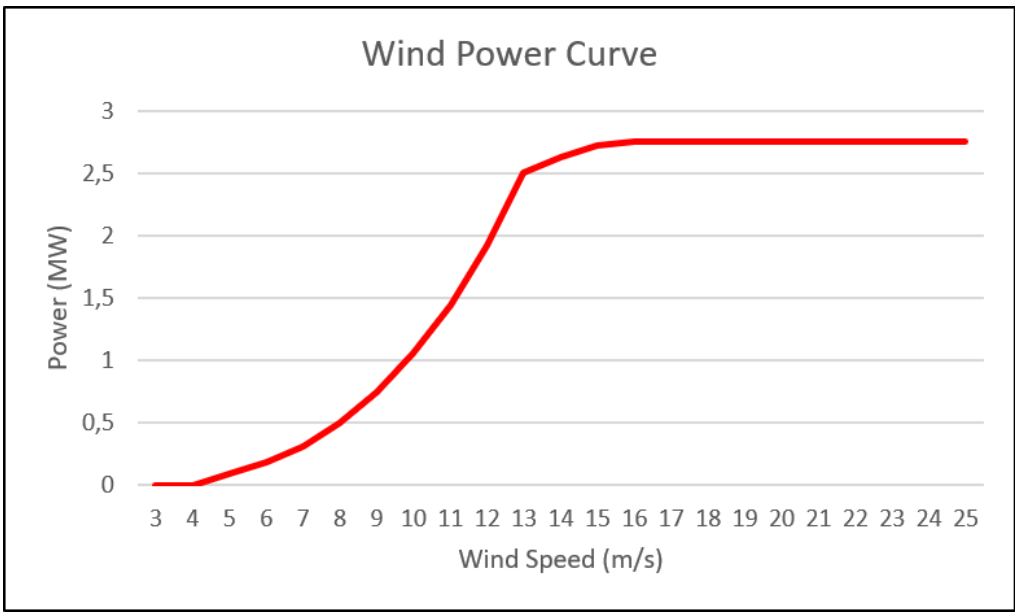

Figure 4.19: Wind turbine power curve for the 2.5 MW WTG

4.3.5 Short-circuit analysis of the WTG in RSCAD runtime

The voltages and currents at the grid side of the converter for a three-phase fault at the point of connection (POC) are shown in Figure 4.20. The measured currents for WF1VGA, WF1VGB, and WF1VGC are 1.2809 kA. The measured voltages at WF1GA, WF1GB, and WF1GC decreases from 18.3847 kV to 0.6025 kV for the duration of the fault. The per-unit fault current is calculated as follows:

$$I_{pu} = \frac{I_{Fault}}{I_{steady-state}} = \frac{1.2809}{0.8944} = 1.4321\ p.u.$$

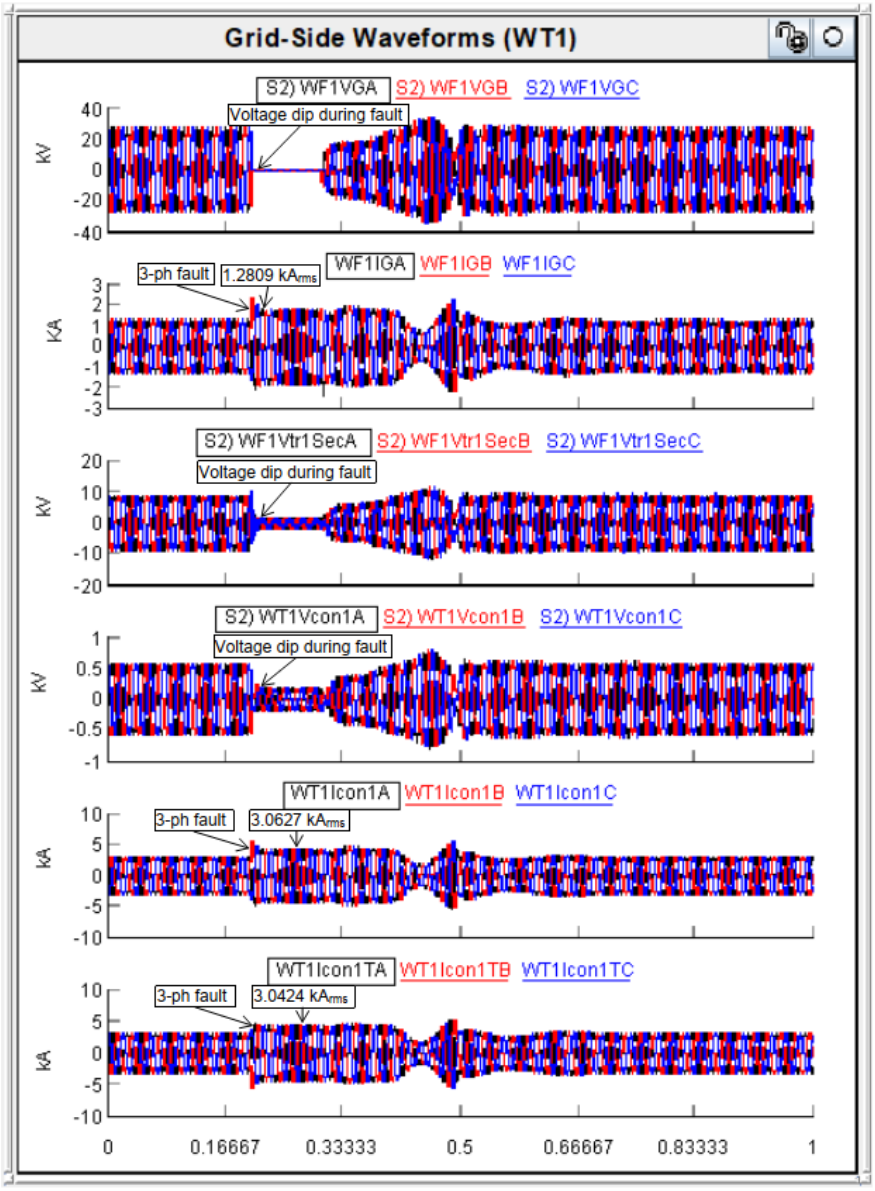

Figure 4.20: **Output voltages and currents at the grid side of the converter during a three-phase fault at the POC**

4.4 Conclusion

This chapter focused on the modelling and simulation of the modified IEEE 14-bus system in real-time using RSCAD software, a suite of RTDS. The network is divided into two subsystems. Subsystem 1 represents the modified IEEE 14-bus system, while subsystem 2 represents the 50 MW wind farm. The two subsystems are linked together through a transmission line model.

The 50 MW wind farm comprises of 20 x 2.5 MW type 4 WTGs. The type 4 WTG comprises a PMSG with a full-scale back-to-back converter. For simplicity, only one

2.5 MW WTG was modelled in RSCAD and increased to 50 MW output using the scaling functionality.

The voltages and currents were investigated for steady-state conditions at various wind speeds. Additionally, the short-circuit current during a three-phase fault was also investigated during the RSCAD runtime simulation.

The hardware-in-the-loop (HIL) platform is developed in the next chapter to by interfacing the external SEL-351A directional overcurrent relays with the modified IEEE 14-bus system modelled in RSCAD.

CHAPTER 5
HARDWARE-IN-THE-LOOP SIMULATION OF PROTECTION FUNCTIONAL TESTING FOR GRID-CONNECTED AND ISLANDED MODES OF OPERATION

5.1 Introduction

Real-time simulators utilise dedicated parallel processing hardware to perform simulations in real-time, which allows external equipment to be connected to the simulated network in the form of hardware-in-the-loop (HIL) testing. Advancements in real-time simulation technology have significantly enhanced the efficiency and reliability of HIL testing, establishing it as an essential tool for verifying complex systems and equipment (Sidwall and Forsyth, 2020). A HIL platform is developed to evaluate the proposed protection scheme, thus ensuring validation of protection and control functionality before field implementation (Penthong et al., 2023).

A laboratory-scale test bench is developed for HIL protection testing using a real-time digital simulator (RTDS) and SEL-351A directional overcurrent relays, as depicted in Figure 5.1. The power amplifiers increase the voltages and currents from the RSCAD simulation to an appropriate level for the SEL-351A relays. The trip signals from the SEL-351A relays are sent back to the RTDS through the digital interface front panel to open the circuit breaker models in the RSCAD simulation. This configuration allows a closed-loop interface between the RTDS simulator and the external SEL relays, known as HIL testing.

This chapter investigates the fault events obtained during HIL testing for both grid-connected and islanded modes of operation. The development and implementation of HIL protection testing are divided into the following sections:

5.2 Configuration of SEL-351A directional overcurrent relays

5.3 Modelling of RSCAD components

5.4 Hardware-in-the-loop simulation

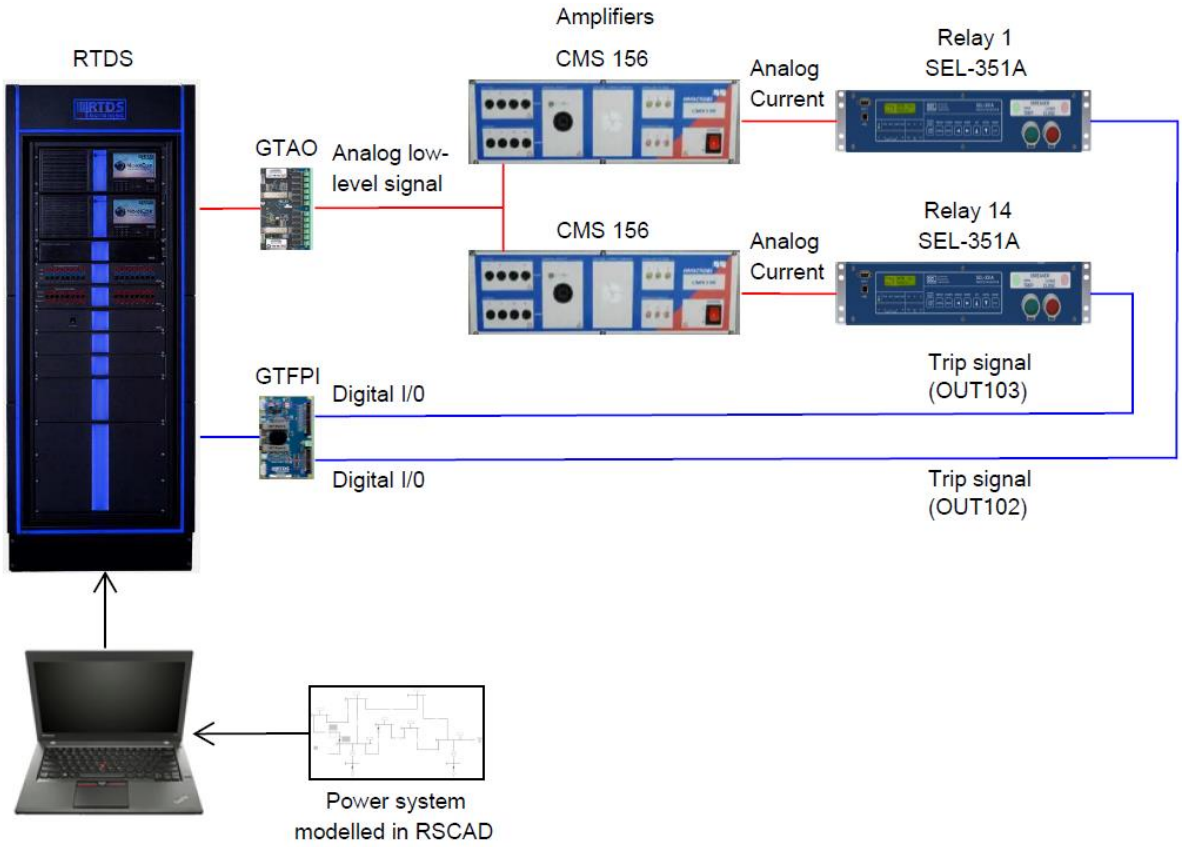

Figure 5.1: Lab-scale test bench setup to demonstrate HIL testing

5.2 Configuration of the SEL-351A direction overcurrent relays with AcSELerator Quickset

The relay settings calculated during the DIgSILENT PowerFactory simulations are the phase overcurrent (50P) and phase time overcurrent (51P) settings for the SEL-351A relays. These settings are used for the configuration of the relays during HIL testing. The primary relay, R1, and the backup relay, R14, are considered for the relay pair, as highlighted in Figure 5.2. The neutral overcurrent (50N) settings were calculated from the measured single-phase-to-ground fault during the RSCAD runtime simulation. Tables 5.1 and 5.2 show the settings for relays R1 and R14 in the grid-connected and islanded modes of operation, respectively.

The SEL-351A relays are configured using the AcSELerator Quickset software. The first step is to establish communication between the host computer and the SEL-351A relays. All IEDs are connected to the network via the SEL-2725 Ethernet switch. The Windows command prompt can ping the IP addresses of the IEDs connected to the network and verify the communication, as shown in Figure 5.3.

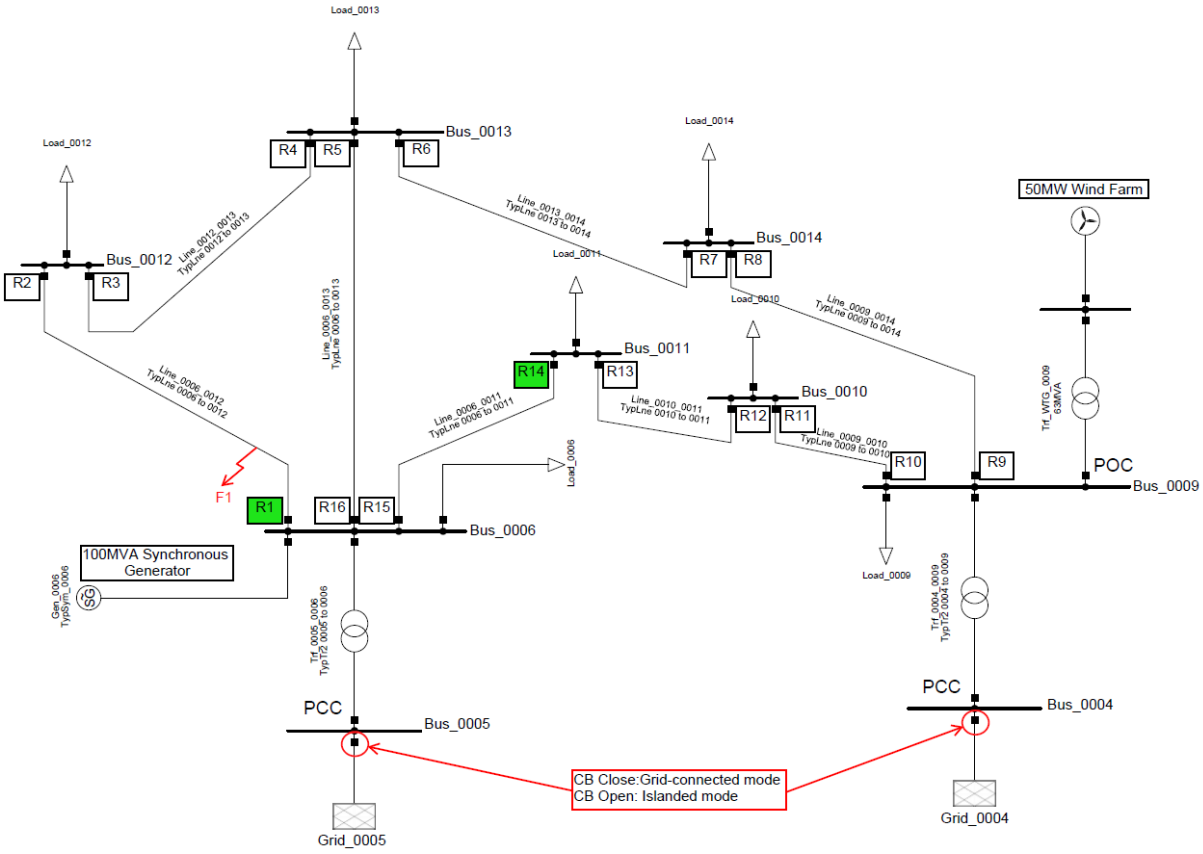

Figure 5.2: Modified IEEE 14-bus system with SEL-351A relays

Command Prompt

```
Microsoft Windows [Version 10.0.19045.3208]
(c) Microsoft Corporation. All rights reserved.

C:\Users\henni>ping 192.168.1.3

Pinging 192.168.1.3 with 32 bytes of data:
Reply from 192.168.1.3: bytes=32 time<1ms TTL=255
Reply from 192.168.1.3: bytes=32 time=1ms TTL=255
Reply from 192.168.1.3: bytes=32 time<1ms TTL=255
Reply from 192.168.1.3: bytes=32 time<1ms TTL=255

Ping statistics for 192.168.1.3:
    Packets: Sent = 4, Received = 4, Lost = 0 (0% loss),
Approximate round trip times in milli-seconds:
    Minimum = 0ms, Maximum = 1ms, Average = 0ms

C:\Users\henni>ping 192.168.1.6

Pinging 192.168.1.6 with 32 bytes of data:
Reply from 192.168.1.6: bytes=32 time<1ms TTL=255
Reply from 192.168.1.6: bytes=32 time<1ms TTL=255
Reply from 192.168.1.6: bytes=32 time=1ms TTL=255
Reply from 192.168.1.6: bytes=32 time<1ms TTL=255

Ping statistics for 192.168.1.6:
    Packets: Sent = 4, Received = 4, Lost = 0 (0% loss),
Approximate round trip times in milli-seconds:
    Minimum = 0ms, Maximum = 1ms, Average = 0ms
```

Figure 5.3: Command prompt ping results via the SEL-2725 Ethernet switch

According to Gers and Holmes (2022), the neutral time-overcurrent (51N) is typically set at 20% of the phase time-overcurrent (51P) pickup setting. For R1, the 51N setting is 110 A for the grid-connected mode and 116 A for the islanded mode. During the grid-connected mode, R1 measures a far bus fault current (I_{FB}) of 3749 A, and during the islanded mode, the fault current decreases to 2008 A. The instantaneous neutral overcurrent (50N) is set at 125% of the I_{FB}. For R1, the 50N setting is 4690 A for the grid-connected mode and 2510 A for the islanded mode. For R14, the 51N setting is 80 A for the grid-connected mode and 86 A for the islanded mode. During the grid-connected mode, R14 measures a far bus fault current (I_{FB}) of 1522 A, whereas during the islanded mode, the fault current decreases to 806 A. For R14, the 50N setting is 1900 A for the grid-connected mode and 1010 A for the islanded mode. The selected time multiplier setting (TMS) for R14 allows a coordination time interval (CTI) of 0.207 s and 0.229 s for the grid-connected and islanded modes, respectively.

Table 5.1: **Relay settings for the grid-connected mode (setting group 1)**

Relay	Element	PS (sec. A)	TD	Characteristic curve	Directional
R1	51P	0.55	0.08	C1 (Standard inverse)	Forward
	50P1	5.67	0.05	Definite time	Forward
	51N	0.11	0.05	C1 (Standard inverse)	Forward
	50N1	4.69	0.05	Definite time	Forward
R14	51P	0.40	0.06	C1 (Standard inverse)	Forward
	50P1	2.58	0.05	Definite time	Forward
	51N	0.08	0.11	C1 (Standard inverse)	Forward
	50N1	1.900	0.05	Definite time	Forward

Table 5.2: **Relay settings for the islanded mode (setting group 2)**

Relay	Element	PS (sec. A)	TD	Characteristic curve	Directional
R1	51P	0.58	0.07	C1 (Standard inverse)	Forward
	50P1	4.53	0.05	Definite time	Forward
	51N	0.116	0.05	C1 (Standard inverse)	Forward
	50N1	2.510	0.05	Definite time	Forward
R14	51P	0.43	0.05	C1 (Standard inverse)	Forward
	50P1	1.02	0.05	Definite time	Forward
	51N	0.086	0.09	C1 (Standard inverse)	Forward
	50N1	1.010	0.05	Definite time	Forward

Table 5.3: Equations for IEC curves (IEC 60255-151, 2009), (SEL-351A Instruction Manual, 2022)

Curve type	Operating time
C1 (Standard inverse)	$t = TD \cdot \left(\frac{0.14}{M^{0.02} - 1}\right)$
C2 (Very inverse)	$t = TD \cdot \left(\frac{13.5}{M - 1}\right)$
C3 (Extremely inverse)	$t = TD \cdot \left(\frac{80}{M^2 - 1}\right)$
C4 (Long-time inverse)	$t = TD \cdot \left(\frac{120}{M - 1}\right)$
C5 (Short-time inverse)	$t = TD \cdot \left(\frac{0.05}{M^{0.05} - 1}\right)$

The AcSELerator QuickSet is used to configure the programmable logic functions of the SEL-351A relays using the Relay Word Bits and SELOGIC control equations. The phase and neutral ground overcurrent pickup elements are mapped to the output contact equation OUT101. The trip logic equation from OUT102 is assigned to relay 1, whereas the trip logic equation from OUT103 is assigned to relay 14. The output contact equations for OUT102 and OUT103 are as follows:

51PT + 67P1T + 51NT + 67N1T **Equation 5.1**

The logic diagram for the output contact equation for OUT102 is shown in Figure 5.4.

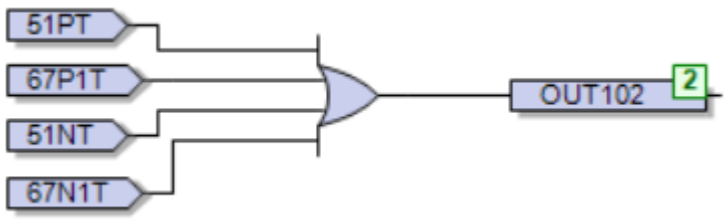

Figure 5.4: Logic diagram for the OUT102 trip logic equation

The description for the relays Word Bits from Equation 5.1 is given in Table 5.4.

Table 5.4: Description of relay Word Bits

Logic output	Description
51PT	Phase time-overcurrent element timed out
67P1T	Level 1 phase definite-time overcurrent element timed out
51NT	Neutral ground time-overcurrent element timed out
67N1T	Level 1 neutral ground definite-time overcurrent element timed out

5.3 Configuration of the circuit breaker control and fault logic in RSCAD

The secondary currents from CT1 are measured by relay 1, and the secondary currents from CT2 are measured by relay 14, as shown in Figure 5.5. The trip signal from relay 1 controls circuit breaker BRK1, and the trip signal from relay 14 controls circuit breaker BRK2.

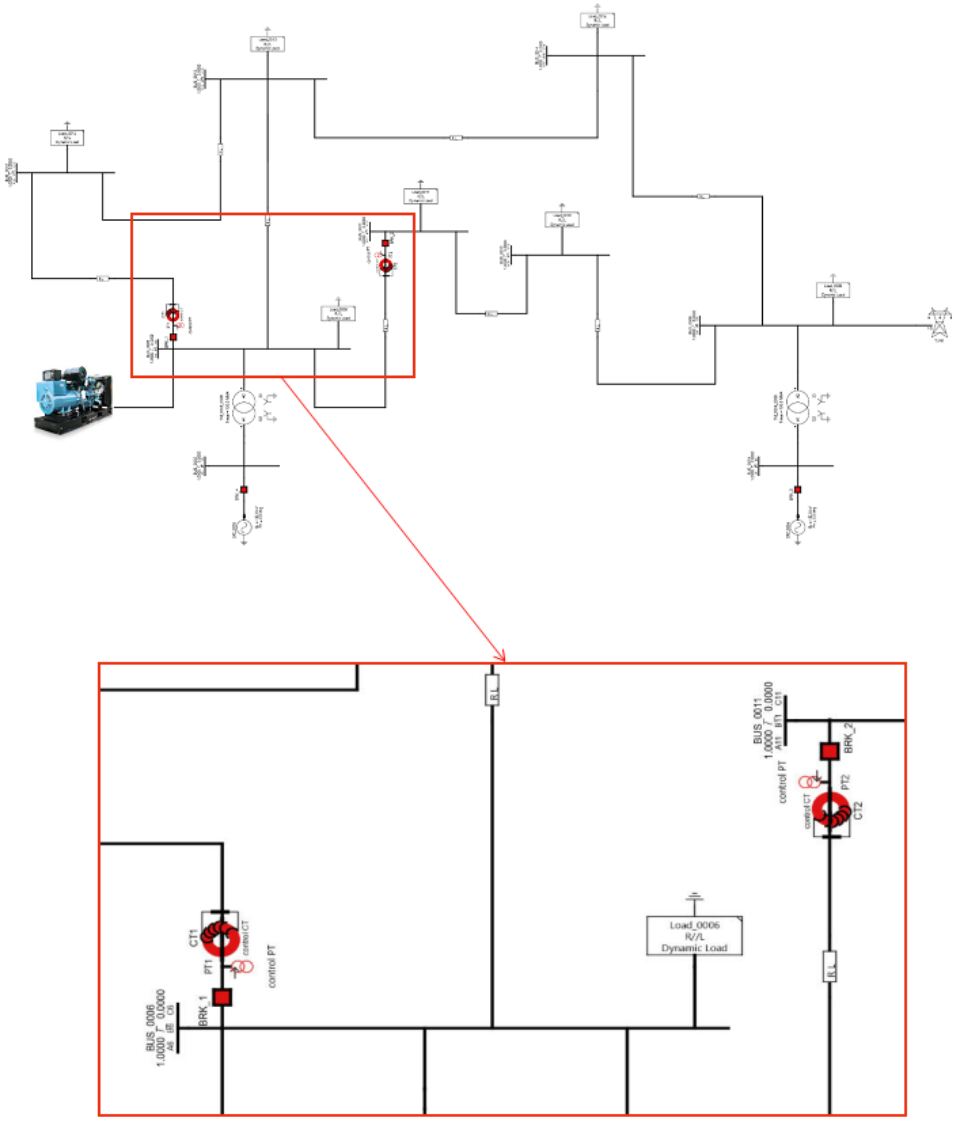

Figure 5.5: CTs, PTs, and circuit breakers in the RSCAD

5.3.1 Configuration of the GTAO card

The secondary currents from CT1 are connected to Inputs 1, 2, and 3 on the Gigabit Transceiver Analogue Output Card (GTAO), and the secondary currents from CT2 are connected to Inputs 7, 8, and 9 on the GTAO card, as shown in Figure 5.6. The

secondary voltages from PT1 are connected to Inputs 4, 5, and 6 on the GTAO card, and the secondary voltages from PT2 are connected to Inputs 10, 11, and 12 on the GTAO card, as shown in Figure 5.6. The GTAO card's digital-to-analogue (D/A) output channels are configured as shown in Figure 5.7. The analogue output from the GTAO card is connected to the Omicron CMS 156 amplifiers and has an output range of ±10 V. The scale factor determines the GTAO channel's output for a given floating-point input. The scaling factor entered corresponds to a maximum 5 V output from the GTAO card (i.e., half scale). The GTAO card's scaling factor is configured as shown in Figure 5.8. The scaling factor for the current channels is calculated as follows:

$$\frac{5}{Sx} \cdot \left(\frac{Volts}{Amps}\right) \times 5 \left(\frac{Amps}{Volts}\right) \equiv 1 \qquad \textbf{Equation 5.2}$$

$$\therefore S_x = 25$$

The scaling factor for the voltage channels is calculated as follows:

$$\frac{5}{Sx} \cdot \left(\frac{Volts}{Volts}\right) \times 50 \left(\frac{Volts}{Volts}\right) \equiv 1 \qquad \textbf{Equation 5.3}$$

$$\therefore S_x = 250$$

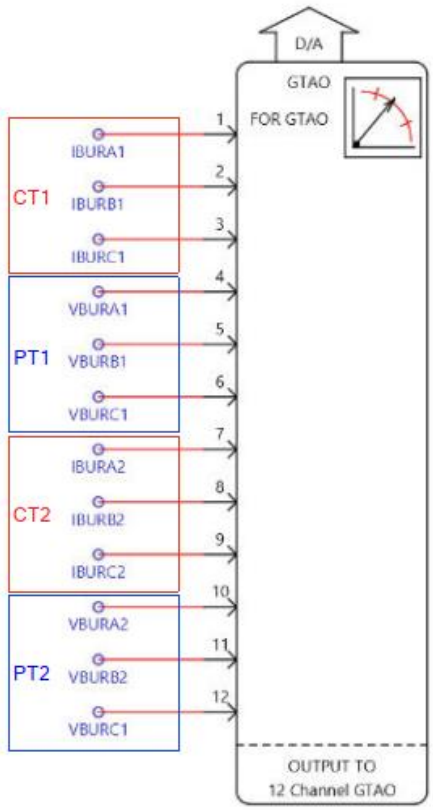

Figure 5.6: GTAO card for CT and PT input signals

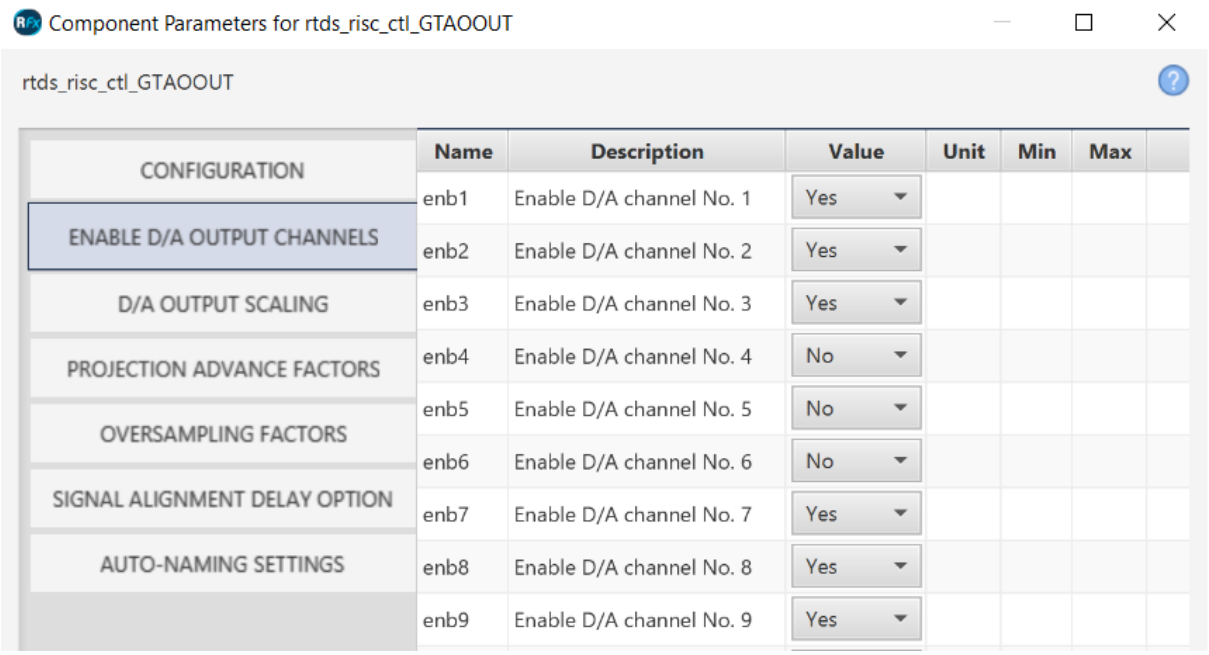

Figure 5.7: Configuration of the GTAO card digital to analogue output channels

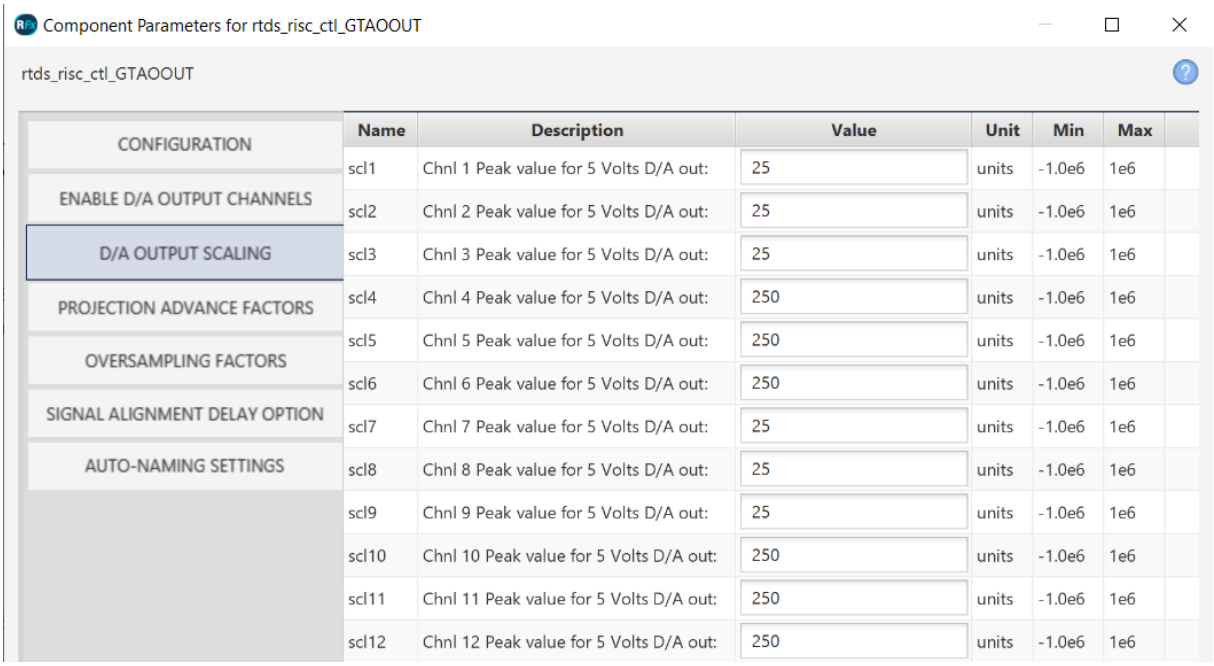

Figure 5.8: Configuration of the GTAO card digital to analogue scaling factors

5.3.2 Configuration of the GTFPI card

The Gigabit Transceiver Front Panel Interface Card (GTFPI) in RSCAD is shown in Figure 5.9. The output from the GTFPI card is connected to a word-to-bit converter. The word-to-bit converter is used to convert integer words to multiple logical signals. The GTFPI card is configured as shown in Figure 5.10. The digital I/O panel signals

are input-only, and the digital I/O panel input signals (16-bit words) are not inverted. The HV panel signals are not included in the HIL testing.

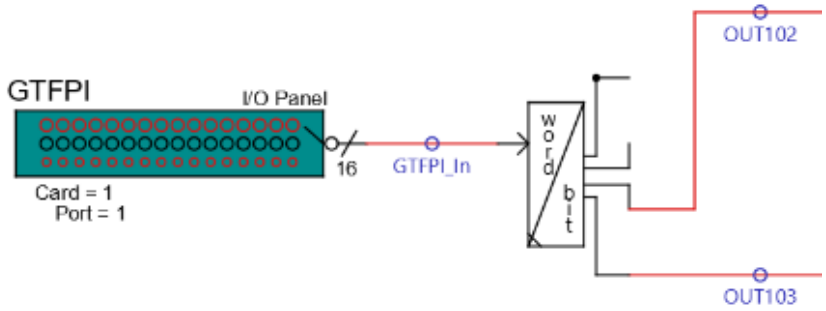

Figure 5.9: GTFPI output logic in RSCAD

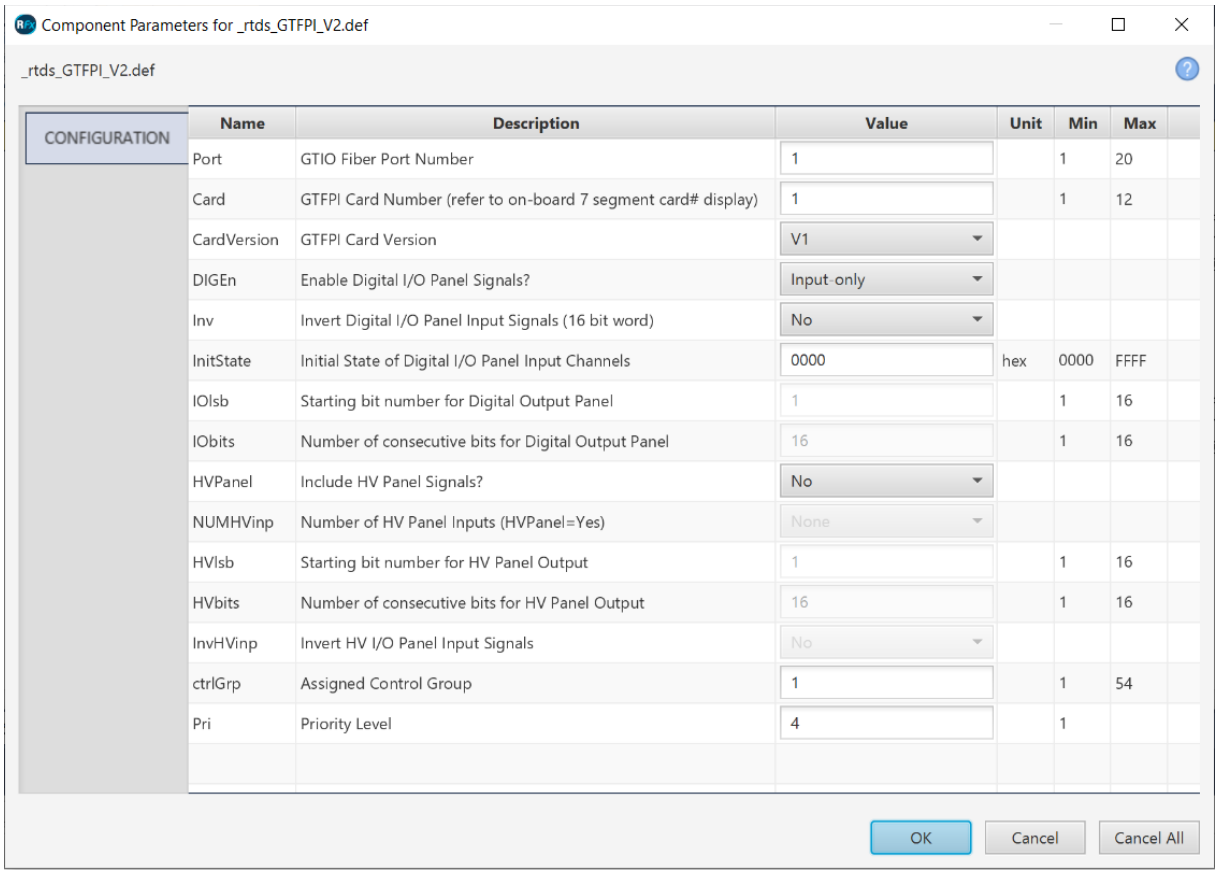

Figure 5.10: GTFPI configuration in RSCAD

5.3.3 Circuit breaker control logic

The logic for circuit breakers 1 and 2 is developed in RSCAD, as shown in Figure 5.11. Circuit breaker 1 is controlled by the signal name BRK1, and circuit breaker 2 by the signal name BRK2. Circuit breaker 1 is closed by pressing the BRK1CL push

button, and circuit breaker 2 is closed by pressing the BRK2CL push button. Circuit breaker 1 is opened by either the OUT102 signal from relay 1 or by pressing the BRK1Op button. Both of these signals are connected to an OR gate. Circuit breaker 2 is opened by either the OUT103 signal from relay 14 or by pressing the BRK2Op button. Both of these signals are connected to an OR gate. When the input changes from logical 0 to logical 1, the edge detectors give a single time-step pulse on the output.

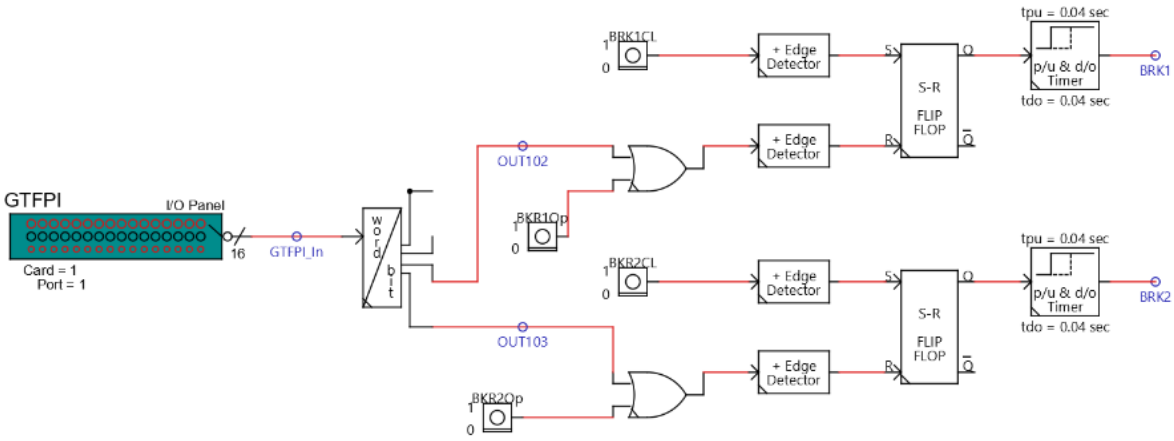

Figure 5.11: Circuit breaker logic in RSCAD

The SR flip-flop logic needs to be configured as shown in Figure 5.12. The active input signal is set high. Table 5.5 shows the truth table for the S-R flip-flop logic. The circuit breaker logic uses a 40 ms time delay. The time delay corresponds to the operation time of the circuit breaker at the moment of receiving the opening or closing signal.

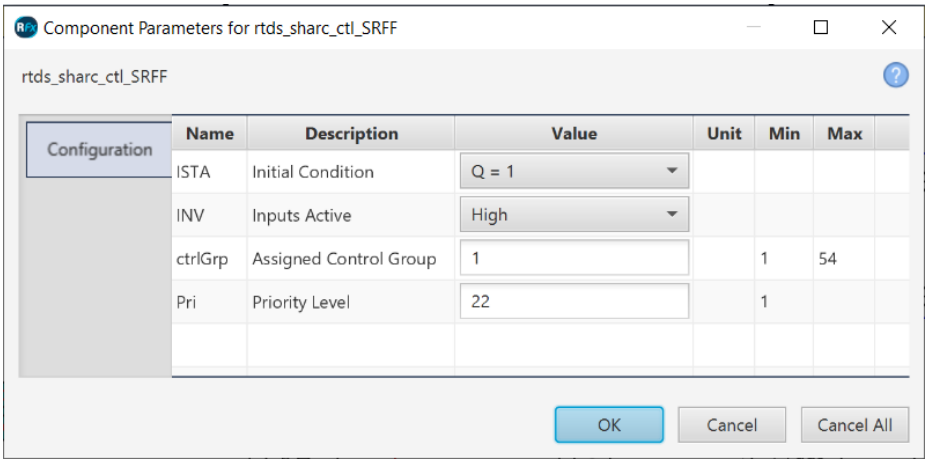

Figure 5.12: Configuration of the S-R Flip Flop logic

Table 5.5: Truth table for Flip-Flop logic (Floyd, 2015)

Input active = High, Q = 1			
S	**R**	**Q**	$\overline{Q}$
0	0	Keep state	Keep state
0	1	0	1
1	0	1	0
1	1	Keep state	Keep state

5.3.4 Fault control logic

The fault control logic in RSCAD operates using the 8421 logic, as shown in Table 5.6. The FltType component is a seven-segment dial switch that selects the individual line-ground fault during the RSCAD runtime. When the ApplyFlt button is pressed, the output transitions from logical 0 to logical 1, triggering a fault event during the RSCAD runtime. The fault duration during RSCAD runtime is determined by the FltDur slider.

Table 5.6: Truth table for 8421 BCD code (Floyd, 2015)

Decimal	Binary value			Status of an individual line-ground fault		
	Bit 3 $2^2 = 4$	**Bit 2** $2^1 = 2$	**Bit 1** $2^0 = 1$	**A**	**B**	**C**
0	0	0	0	OFF	OFF	OFF
1	0	0	1	ON	OFF	OFF
2	0	1	0	OFF	ON	OFF
3	0	1	1	ON	ON	OFF
4	1	0	0	OFF	OFF	ON
5	1	0	1	ON	OFF	ON
6	1	1	0	OFF	ON	ON
7	1	1	1	ON	ON	ON

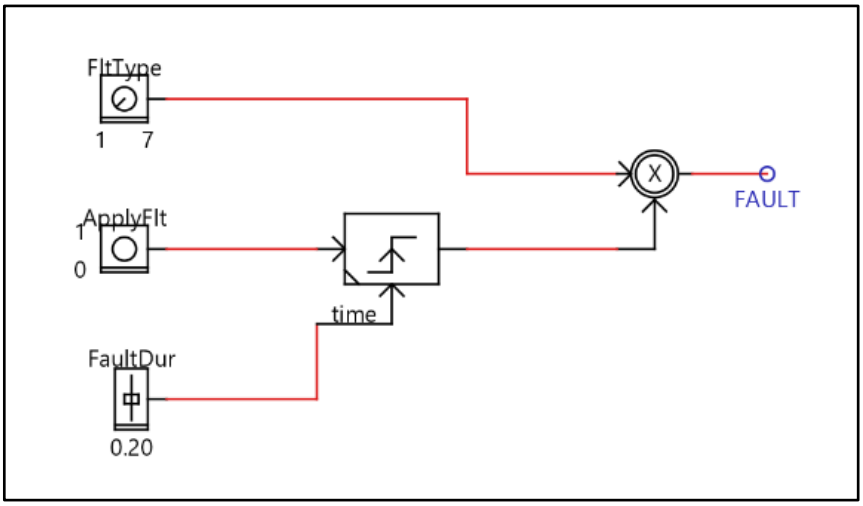

Figure 5.13: Fault logic in RSCAD

Figure 5.14 shows the RSCAD runtime fault controls. This includes a dial switch, a push button, and a slider. The dial switch, FltType, is set to position 1 for a single-phase-to-ground fault and position 7 for a three-phase-to-ground fault. The FaultDur slider is set to 0.2 s. The ApplyFlt push button initiates the fault during the RSCAD runtime simulation.

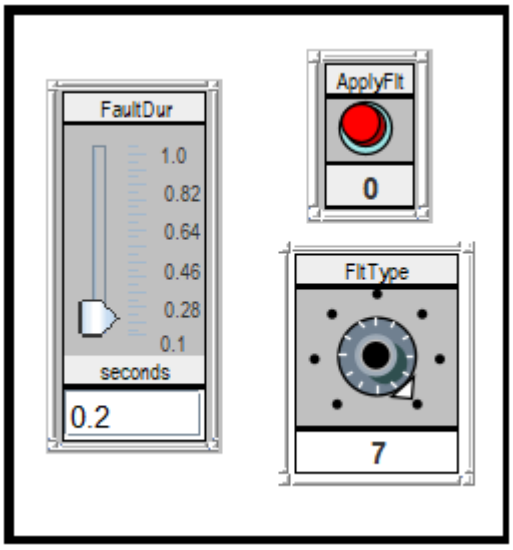

Figure 5.14: Fault controls in RSCAD Runtime

5.4 Hardware-in-the-loop (HIL) simulation

5.4.1 HIL testing for a three-phase fault during grid-connected mode

The ApplyFlt push button displayed in Figure 5.14 initiates a fault during the RSCAD runtime simulation. Figure 5.15 displays the three-phase fault current measured by CT1 and the circuit breaker control signals for relay 1. When the OUT102 output from relay 1 is asserted, the BRK1 signal changes from logical 1 to logical 0 after a 40 ms time delay. The steady-state measured current is 154.11 A. When circuit breaker 1 is opened, the fault current is cleared. The RMS fault current is 16.563 kA, whereas the peak fault current is:

$$\boldsymbol{I_p = \sqrt{2} \cdot I_{rms} = \sqrt{2} \cdot (16.563) = 23.424\ kA}$$

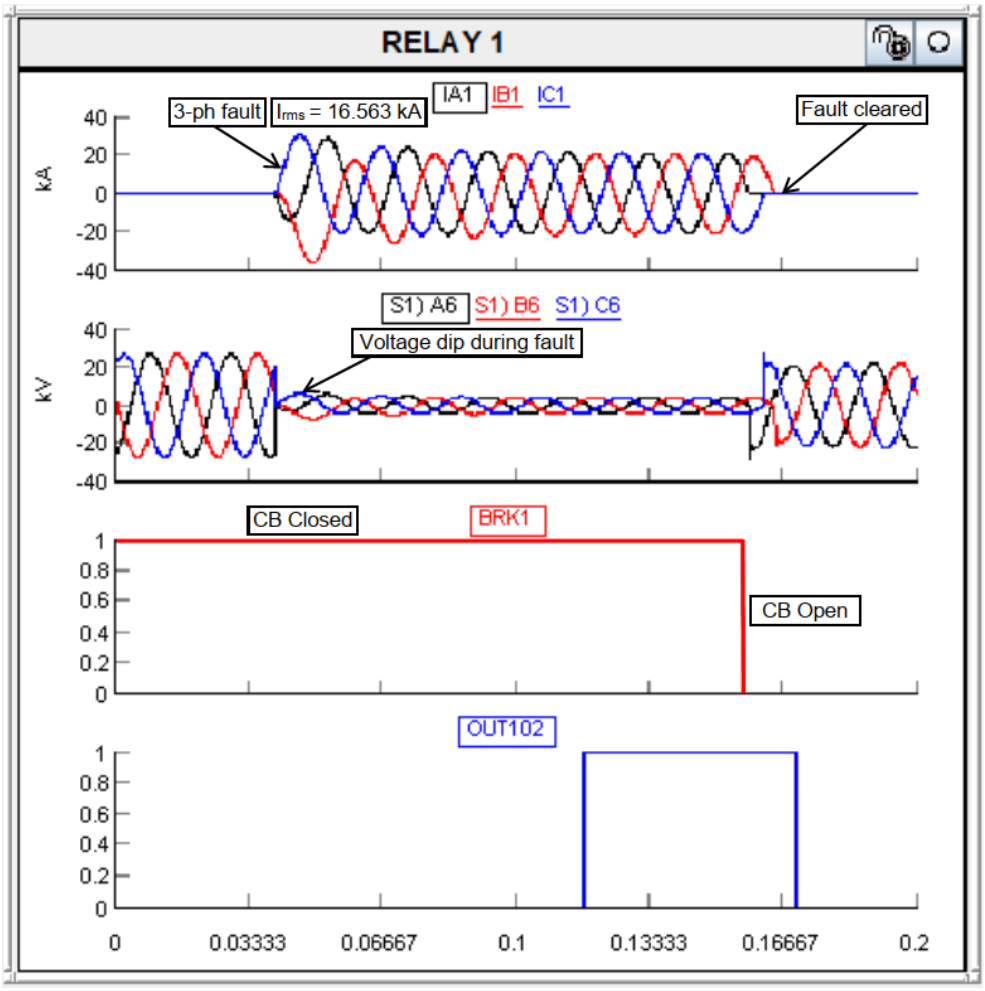

Figure 5.15: Three-phase fault and circuit breaker control for relay 1 during grid-connected mode

The data from the sequential event recorder (SER) presented in Table 5.7 indicates that the 50P1 element and OUT101 output of relay 1 are asserted at 629 ms, whereas the 51P element is asserted at 634 ms. The 67P1T element and OUT102 output are asserted at 694 ms. This gives a tripping time of 65 ms. The 67P1T element and OUT102 output are de-asserted at 749 ms, whereas the 50P1 element is de-asserted at 764 ms. The 51P element and OUT101 output are de-asserted at 774 ms.

Table 5.7: SER for relay 1 during a three-phase fault in grid-connected mode

Time (ms)	Function	State
629	50P1	Asserted
629	OUT101	Asserted
634	51P	Asserted
694	67P1T	Asserted
694	OUT102	Asserted
749	67P1T	De-asserted
749	OUT102	De-asserted
764	50P1	De-asserted
774	51P	De-asserted
774	OUT101	De-asserted

The event for relay 1 is shown in Figure 5.16. The measured three-phase fault currents are as follows:

I_A = 16563 A, I_B = 17224 A, I_C = 16948 A

The 50P1 element is asserted at 629 ms based on the recorded event. The 67P1T element and the TRIP signal are asserted at 694.016 ms. The tripping time is 694.016 - 629 = 65.016 ms. The fault current is cleared at 774 ms, while the TRIP signal is maintained until the relay is reset through the HMI.

Figure 5.21 illustrates the measured three-phase fault current through CT2 and the circuit breaker control signals for relay 14. The steady-state measured current is 272.63 A. Circuit breaker 2 does not trip during the fault event and continues to supply the reduced load after relay 1 has cleared the fault. No event is recorded for relay 14 in the grid-connected mode.

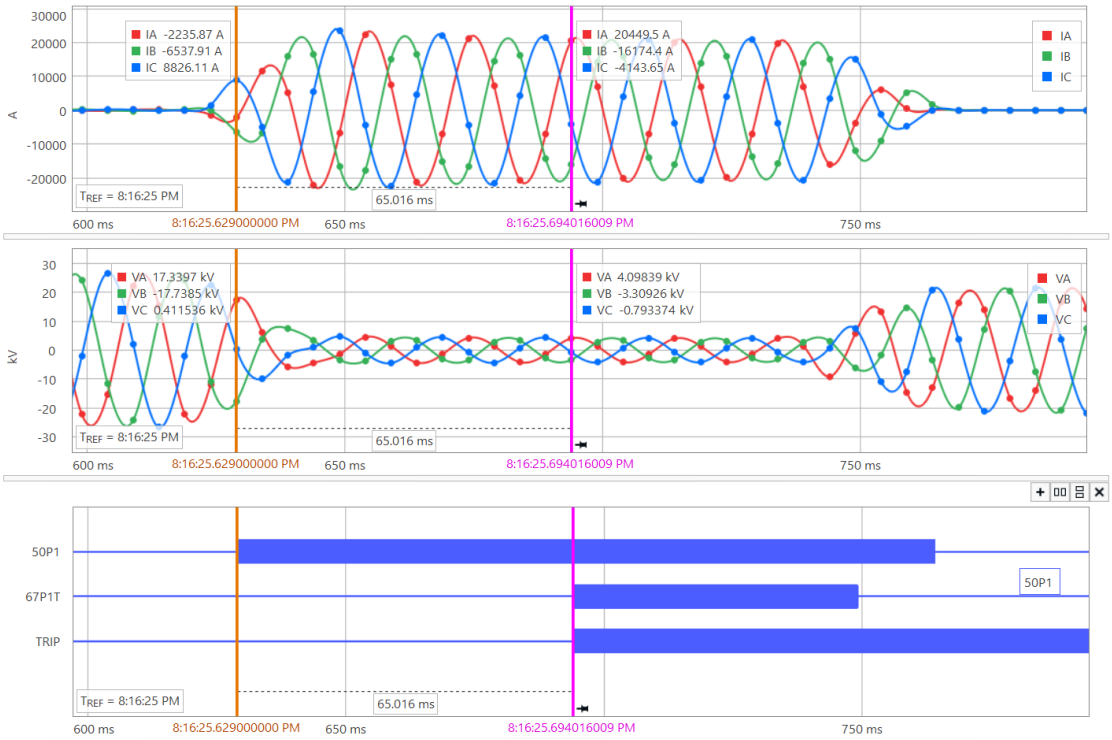

Figure 5.16: Event for relay 1 during a three-phase fault in grid-connected mode

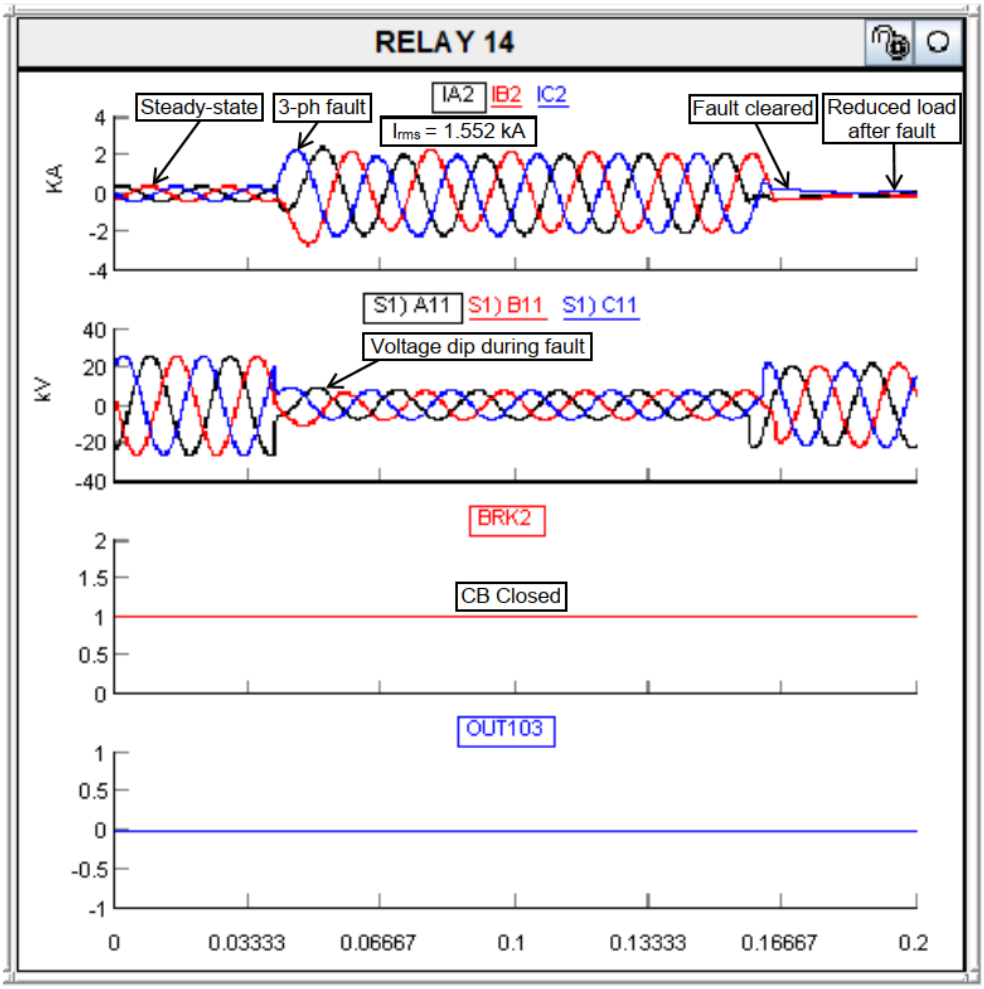

Figure 5.17: Three-phase fault and circuit breaker control for relay 14 during grid-connected mode

Table 5.8 presents data indicating that the 51P element and OUT101 output of relay 14 are asserted at 797 ms and then de-asserted at 937 ms after the fault current is cleared by relay 1.

Table 5.8: **SER for relay 14 during a three-phase fault in grid-connected mode**

Time (ms)	Function	State
797	51P	Asserted
797	OUT101	Asserted
907	51P	De-asserted
907	OUT101	De-asserted
917	51P	Asserted
917	OUT101	Asserted
937	51P	De-asserted
937	OUT101	De-asserted

5.4.2 HIL testing for a three-phase fault during grid-connected mode and maloperation of the primary relay

When the primary relay fails to operate, the backup relay should detect the fault and isolate the faulted section from the rest of the network. To address this issue, it is important to consider the coordination and operation of the protective relays and circuit breakers. The time coordination between the relays controlling the circuit breakers is crucial to ensuring that the circuit breaker closest to the fault location opens first. This requires an adequate time interval between the relays that control the circuit breakers, known as the coordination time interval (CTI) (Azizi, A., Vahidi, B., and Nematollahi, F., A., 2023). Furthermore, the primary and backup relays should be well coordinated to ensure that only the primary relay trips first to isolate the faulted section of the system, and the backup relay only operates if the primary relay fails to trip within the CTI (Park, W. et al., 2011). By carefully coordinating the operation of the protective relays and circuit breakers, the risk of miscoordination can be minimised.

When relay 1 fails to initiate a trip and open circuit breaker 1, relay 14 should detect the fault, and circuit breaker 2 should be opened to isolate the fault. Figure 5.18 displays the three-phase fault current measured by CT2 and the circuit breaker control signals for relay 14. Once the OUT103 output is asserted and the 40 ms time delay has elapsed, the BRK2 signal changes from closed to open. The RMS fault current is 1.552 kA, whereas the peak fault current is:

$$\boldsymbol{I_p = \sqrt{2} \cdot I_{rms} = \sqrt{2} \cdot (1.552) = 2.195\ kA}$$

The tripping time for relay 14 is calculated as follows:

$$t = \frac{0.14}{\left(\frac{1552}{400}\right)^{0.02} - 1} \cdot (0.06) = 0.306\ s$$

The data from the SER presented in Table 5.9 indicates that the 51P element and OUT101 output of relay 14 are asserted at 860 ms. The OUT103 and TRIP outputs are asserted at 1180 ms. This gives a tripping time of 320 ms. The 51P element and OUT101 output are de-asserted at 1260 ms, whereas the OUT103 output is de-asserted at 1280 ms.

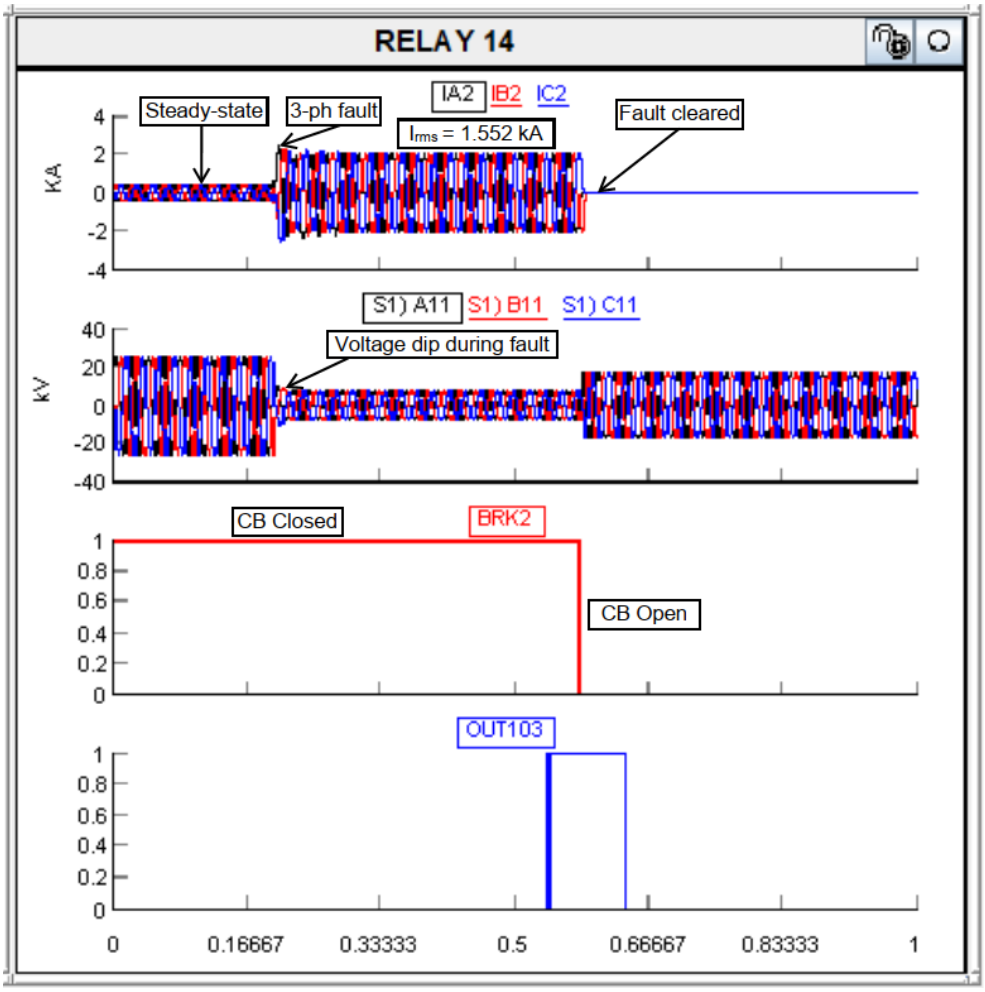

Figure 5.18: Three-phase fault and circuit breaker control for relay 14 during grid-connected mode and maloperation of relay 1

Table 5.9: SER for relay 14 during a three-phase fault in grid-connected mode and maloperation of relay 1

Time (ms)	Function	State
860	51P	Asserted
860	OUT101	Asserted

870	51P	De-asserted
870	OUT101	De-asserted
880	51P	Asserted
880	OUT101	Asserted
1180	OUT103	Asserted
1180	TRIP	Asserted
1260	51P	De-asserted
1260	OUT101	De-asserted
1280	OUT103	De-asserted

The event for relay 14 is shown in Figure 5.19. The measured three-phase fault currents are as follows:

I_A = 1552 A, I_B = 1488 A, I_C = 1590 A

The 51P1 element is asserted at 860.011 ms based on the recorded event. The 51PT element and the TRIP signal are asserted at 1180 ms. The tripping time is 1180 – 860.011 = 319.989 ms. The fault current is cleared at 1260 ms. The TRIP signal is maintained until the relay is reset through the HMI.

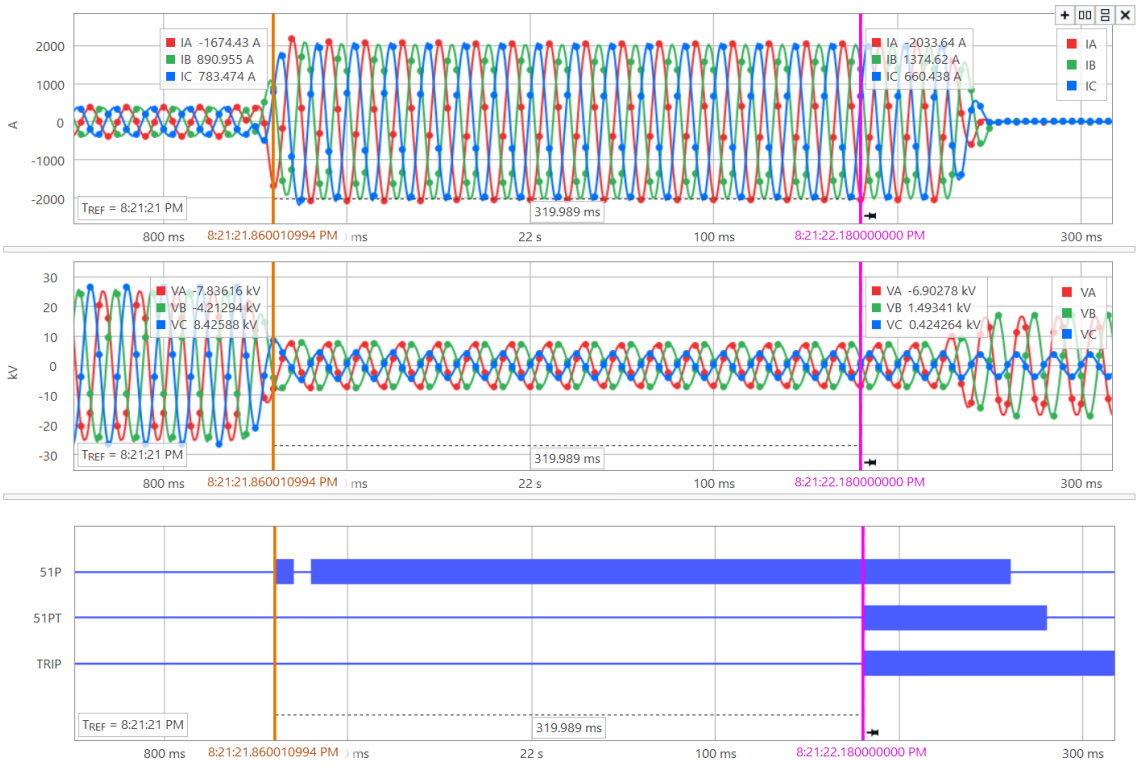

Figure 5.19: Event for relay 14 during a three-phase fault in grid-connected mode and maloperation of relay 1

5.4.3 HIL testing for a single-phase-to-ground fault during grid-connected mode

The single-phase-to-ground fault current measured through CT1 and the circuit breaker control signals for relay 1 are shown in Figure 5.20. When the OUT102 output from relay 1 is asserted, the BRK1 signal changes from logical 1 to logical 0 after a 40-ms time delay. The fault current will be cleared once circuit breaker 1 is opened. The RMS fault current is 13.619 kA, whereas the peak fault current is:

$$\boldsymbol{I_p = \sqrt{2} \cdot I_{rms} = \sqrt{2} \cdot (13.619) = 19.26\ kA}$$

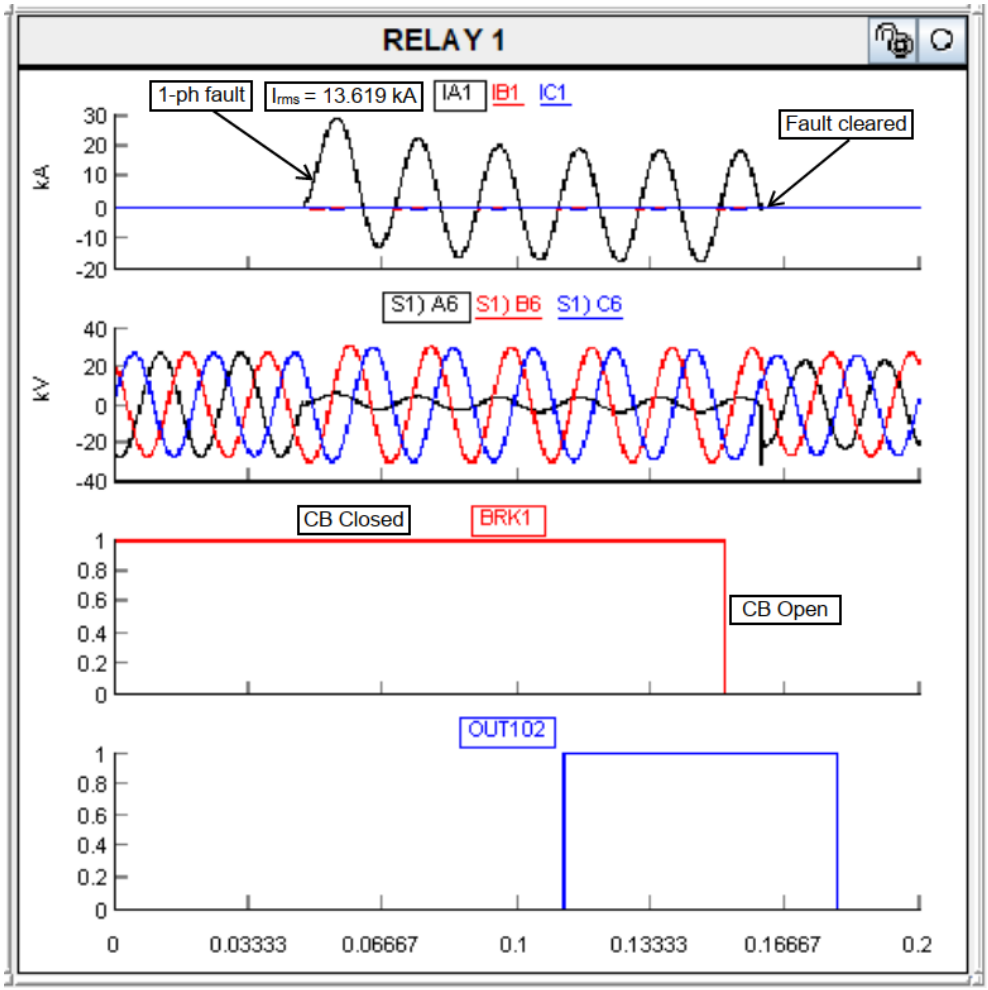

Figure 5.20: Single-phase-to-ground fault and circuit breaker control for relay 1 during grid-connected mode

The SER data presented in Table 5.10 indicate that relay 1's 50N1 element and OUT101 output are asserted at 140 ms. The 51N element is asserted at 145 ms. The 67N1T element and the OUT102 output are asserted at 190 ms. The tripping time is 50

ms. The 50N1, 67N1T, and OUT102 outputs are deasserted at 260 ms, whereas the 51N element and OUT101 output are deasserted at 275 ms.

Table 5.10: SER for relay 1 during single-phase to ground fault in grid-connected mode

Time (ms)	Function	State
140	50N1	Asserted
140	OUT101	Asserted
145	51N	Asserted
190	67N1T	Asserted
190	OUT102	Asserted
260	50N1	De-asserted
260	67N1T	De-asserted
260	OUT102	De-asserted
270	51N	De-asserted
275	OUT101	De-asserted

The 50N1 element is asserted at 140 ms based on the recorded event. The 67N1T element and OUT102 output are asserted at 190.141 ms. The tripping time is 190.141 – 140 = 50.141 ms. The fault current is cleared at 270.192 ms.

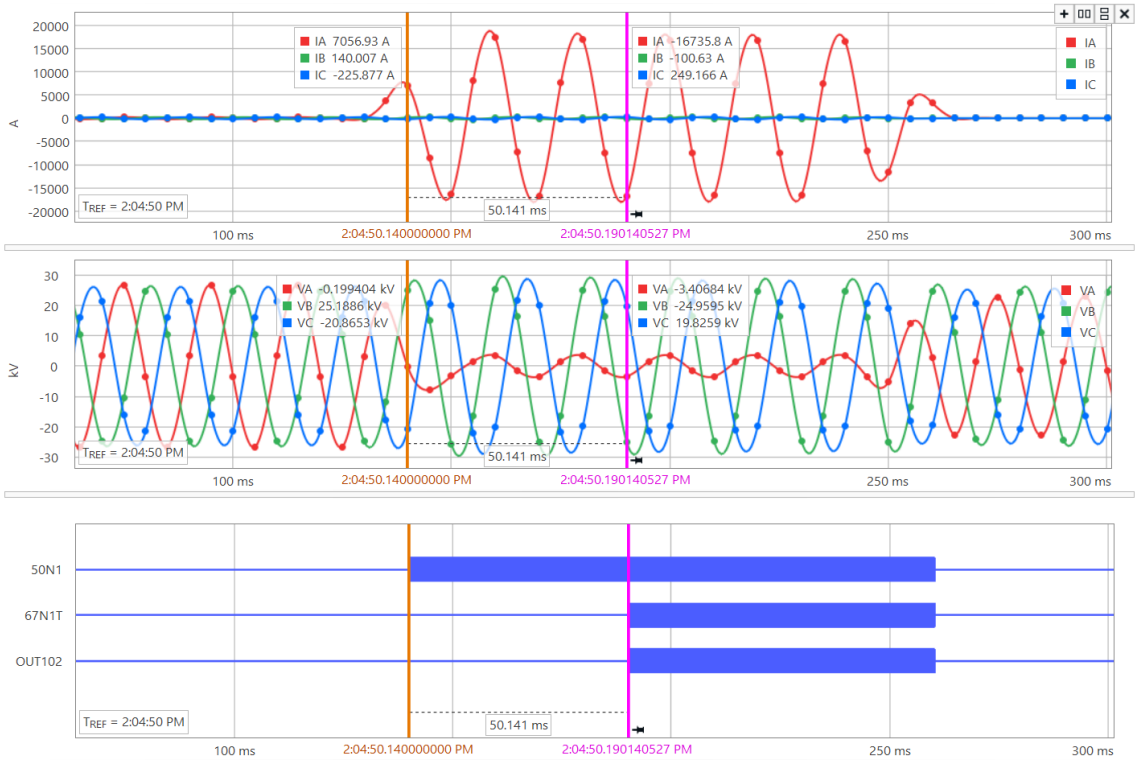

Figure 5.21: Event for relay 1 during a single-phase-to-ground fault in grid-connected mode

The measured single-phase-to-ground fault current through CT2 and the circuit breaker control signals for relay 14 are shown in Figure 5.22. The BRK2 signal remains unchanged at logical 1. Circuit breaker 2 does not trip during the fault event and continues to supply the reduced load after relay 1 has cleared the fault. No event is recorded for relay 14. The RMS fault current is 1.474 kA, whereas the peak fault current is:

$$\boldsymbol{I_p = \sqrt{2} \cdot I_{rms} = \sqrt{2} \cdot (1.474) = 2.085\ kA}$$

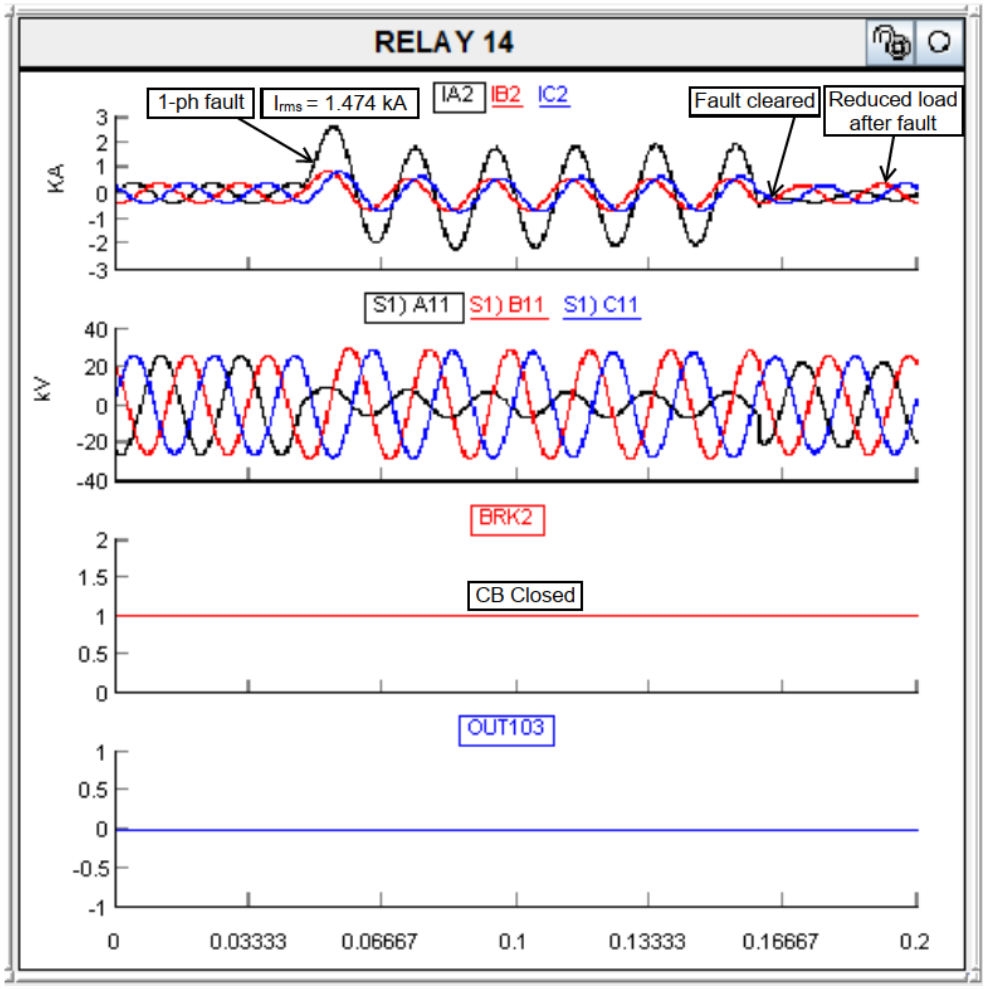

Figure 5.22: **Event for relay 14 during a single-phase to ground fault in grid-connected mode**

The information from the SER shown in Table 5.11, indicates that relay 14's 51N element and OUT101 output are asserted at 138 ms and then de-asserted at 258 ms.

Table 5.11: SER for relay 14 during a single-phase-to-ground fault in grid-connected mode

Time (ms)	Function	State
138	51N	Asserted
138	OUT101	Asserted
258	51N	De-asserted
258	OUT101	De-asserted

5.4.4 HIL testing for a three-phase fault during islanded mode

The measured three-phase fault current through CT1 and the circuit breaker control output for relay 1 are depicted in Figure 5.23. The BRK1 signal changes from logical 1 to logical 0 once the OUT102 output is asserted and the 40 ms time delay has elapsed. The steady-state measured current is 163.13 A. The fault current is cleared once circuit breaker 1 is opened. The RMS fault current is 9.450 kA, whereas the peak fault current is:

$$\boldsymbol{I_p = \sqrt{2} \cdot I_{rms} = \sqrt{2} \cdot (9.45) = 13.364\ kA}$$

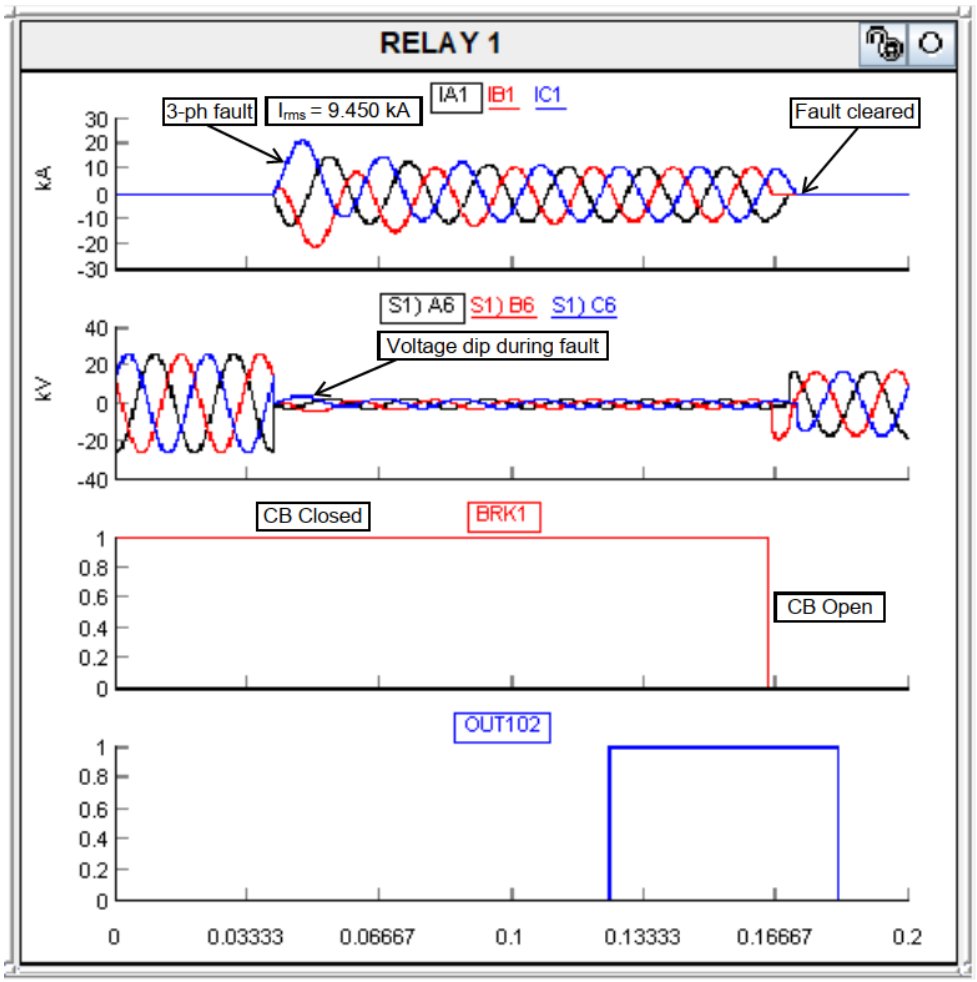

Figure 5.23: Three-phase fault and circuit breaker control for relay 1 during islanded mode

The information from the SER for relay 1 is shown in Table 5.12. The 50P1, 51P, and OUT101 outputs are asserted at 172 ms. The 67P1T element and OUT102 output are asserted at 237 ms. The tripping time is 65 ms. The 67P1T element and OUT102 output are de-asserted at 297 ms, whereas the 51P element and OUT101 output are de-asserted at 312 ms.

Table 5.12: **SER for relay 1 during a three-phase fault in islanded mode**

Time (ms)	Function	State
172	50P1	Asserted
172	51P	Asserted
172	OUT101	Asserted
182	51P	De-asserted
182	OUT101	De-asserted
187	OUT101	Asserted
192	51P	Asserted
237	67P1T	Asserted
237	OUT102	Asserted
297	67P1T	De-asserted
297	OUT102	De-asserted
302	50P1	De-asserted
312	51P	De-asserted
312	OUT101	De-asserted

The event for relay 1 is shown in Figure 5.24. The measured three-phase fault currents are as follows:

I_A = 9450 A, I_B = 9260 A, I_C = 9651 A

The 50P1 element is asserted at 172 ms based on the recorded event. The 67P1T element and OUT102 output are asserted at 237 ms. The tripping time is 237 – 172 = 65 ms. The fault current is cleared at 312 ms. The TRIP signal remains asserted until the relay is reset through the HMI.

Figure 5.24 illustrates the measured three-phase fault current through CT2 and the circuit breaker control signals for relay 14. The steady-state measured current is 353.45 A. Circuit breaker 2 does not trip during the fault event and continues to supply the reduced load after relay 1 has cleared the fault. No event is recorded for relay 14 in the islanded mode.

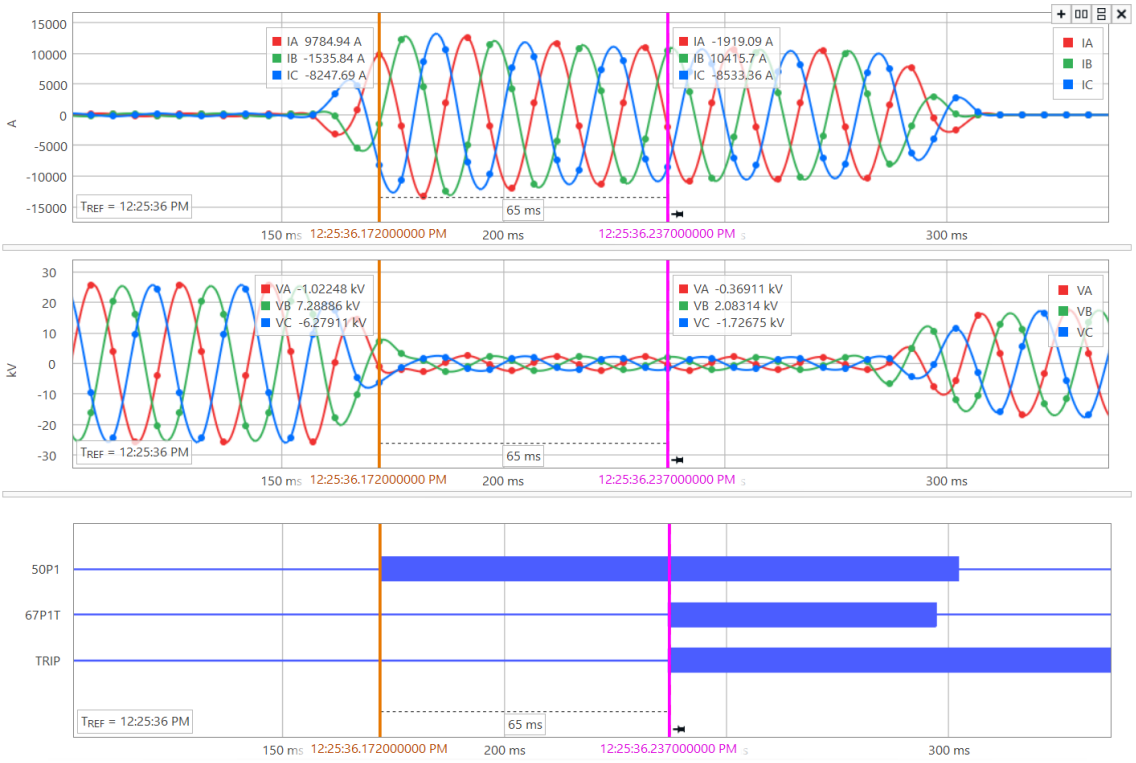

Figure 5.24: Event for relay 1 during a three-phase fault in islanded mode

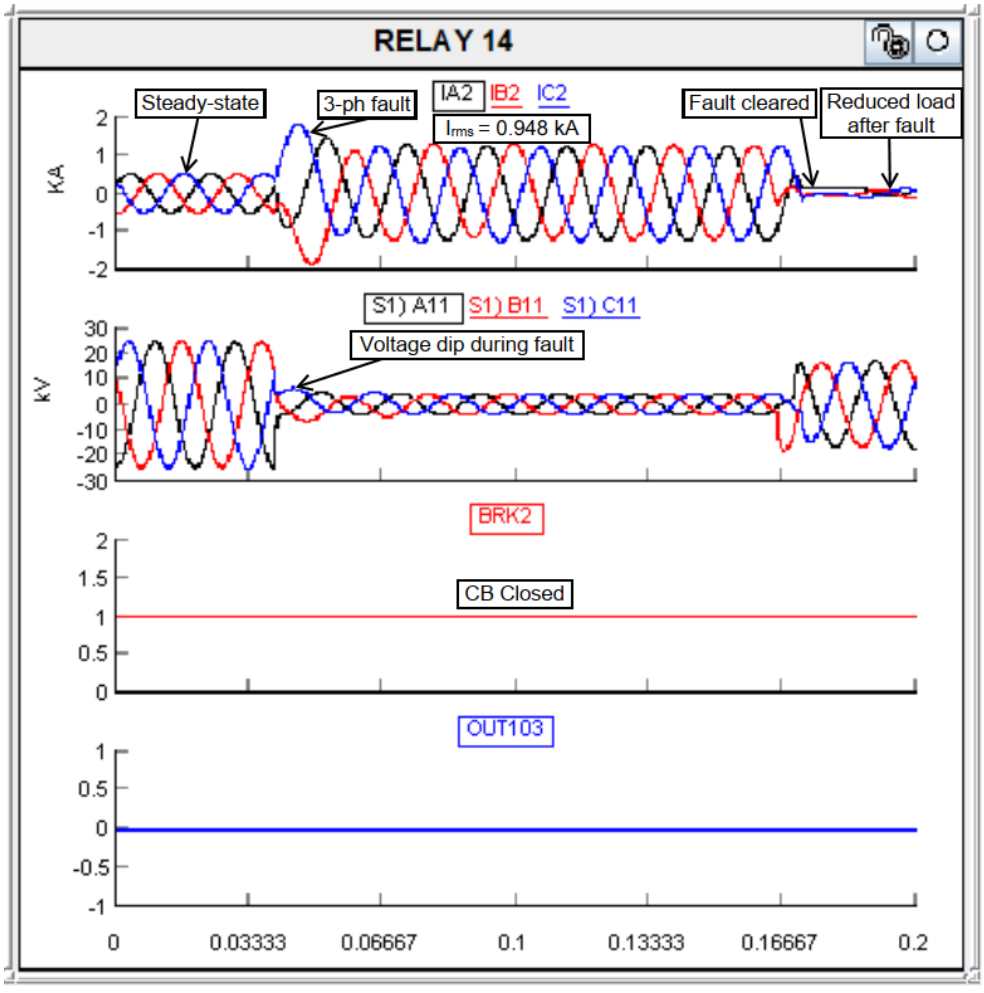

Figure 5.25: Three-phase fault current and circuit breaker control for relay 14 during islanded mode

The information from the SER presented in Table 5.13 indicates that relay 14's 51P element and OUT101 output are asserted at 165 ms and then de-asserted at 305 ms.

Table 5.13: **SER for relay 14 during a three-phase fault in islanded mode**

Time (ms)	Function	State
165	51P	Asserted
165	OUT101	Asserted
175	51P	De-asserted
175	OUT101	De-asserted
185	51P	Asserted
185	OUT101	Asserted
305	51P	De-asserted
305	OUT101	De-asserted

5.4.5 HIL testing for a three-phase fault during islanded mode and maloperation of the primary relay

When relay 1 fails to initiate a trip and open circuit breaker 1, relay 14 should detect the fault, and circuit breaker 2 should be opened to isolate the fault. Figure 5.26 displays the three-phase fault current measured by CT2 and the circuit breaker control signals for relay 14. Once the OUT103 output is asserted and the 40 ms time delay has elapsed, the BRK2 signal changes from closed to open. The RMS fault current is 0.948 kA, whereas the peak fault current is:

$$\boldsymbol{I_p = \sqrt{2} \cdot I_{rms} = \sqrt{2} \cdot (0.948) = 1.341\ kA}$$

The tripping time for relay 14 is calculated as follows:

$$\boldsymbol{t = \frac{0.14}{\left(\frac{948}{430}\right)^{0.02} - 1} \cdot (0.05) = 0.439\ s}$$

The information from the SER is shown in Table 5.14. The 51P element and OUT101 output are asserted at 913 ms. The OUT103 and TRIP outputs are asserted at 1393 ms. The tripping time is 480 ms. The 51P element and OUT101 output are de-asserted at 1453 ms, whereas the OUT103 output is de-asserted at 1473.

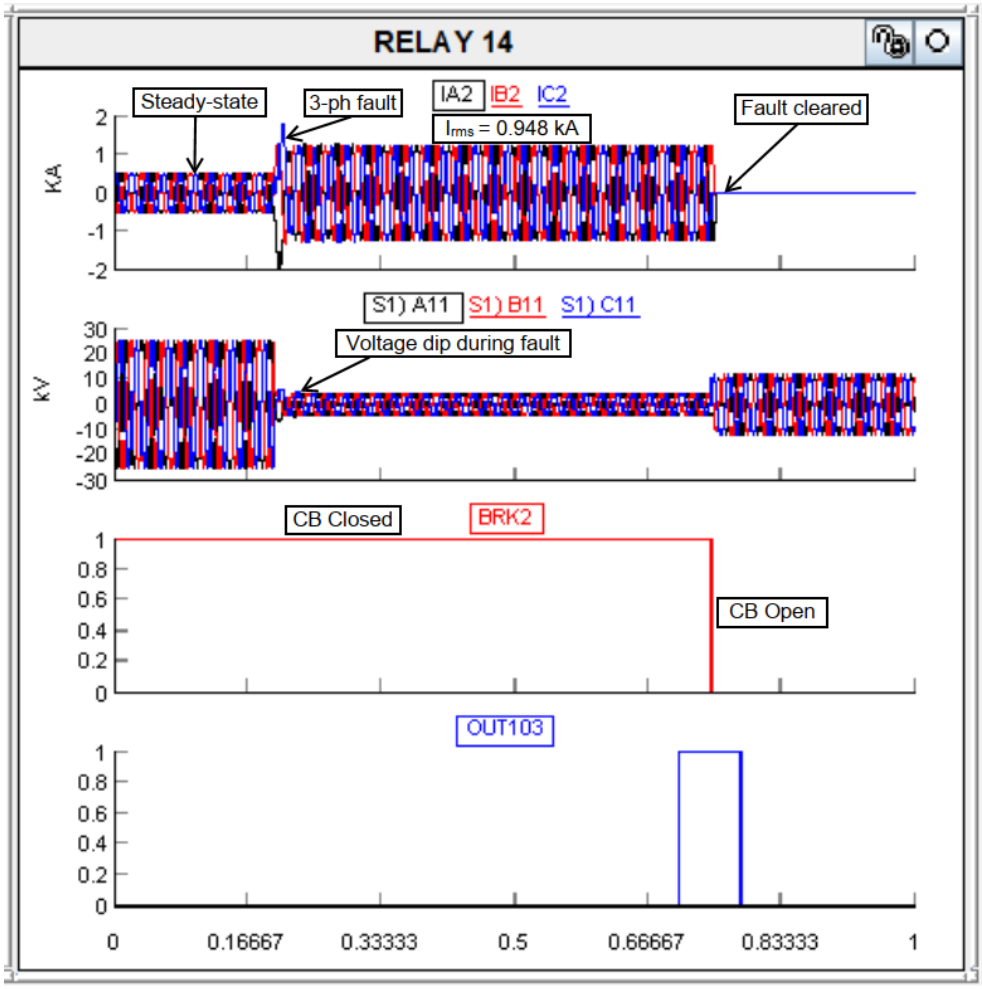

Figure 5.26: Three-phase fault and circuit breaker control for relay 14 during islanded mode and maloperation of relay 1

Table 5.14: SER for relay 14 during a three-phase fault in islanded mode and with maloperation of relay 1

Time (ms)	Function	State
913	51P	Asserted
913	OUT101	Asserted
1393	OUT103	Asserted
1393	TRIP	Asserted
1453	51P	De-asserted
1453	OUT101	De-asserted
1473	OUT103	De-asserted

The event for relay 14 is shown in Figure 5.27. The measured three-phase fault currents are as follows:

I_A = 948 A, I_B = 893 A, I_C = 918 A

The 51P element is asserted at 913.405 ms based on the recorded event. The 51PT element and OUT103 output are asserted at 1393 ms. The tripping time is 1393 – 913.405 = 479.595 ms. The fault current is cleared at 1472.976 ms.

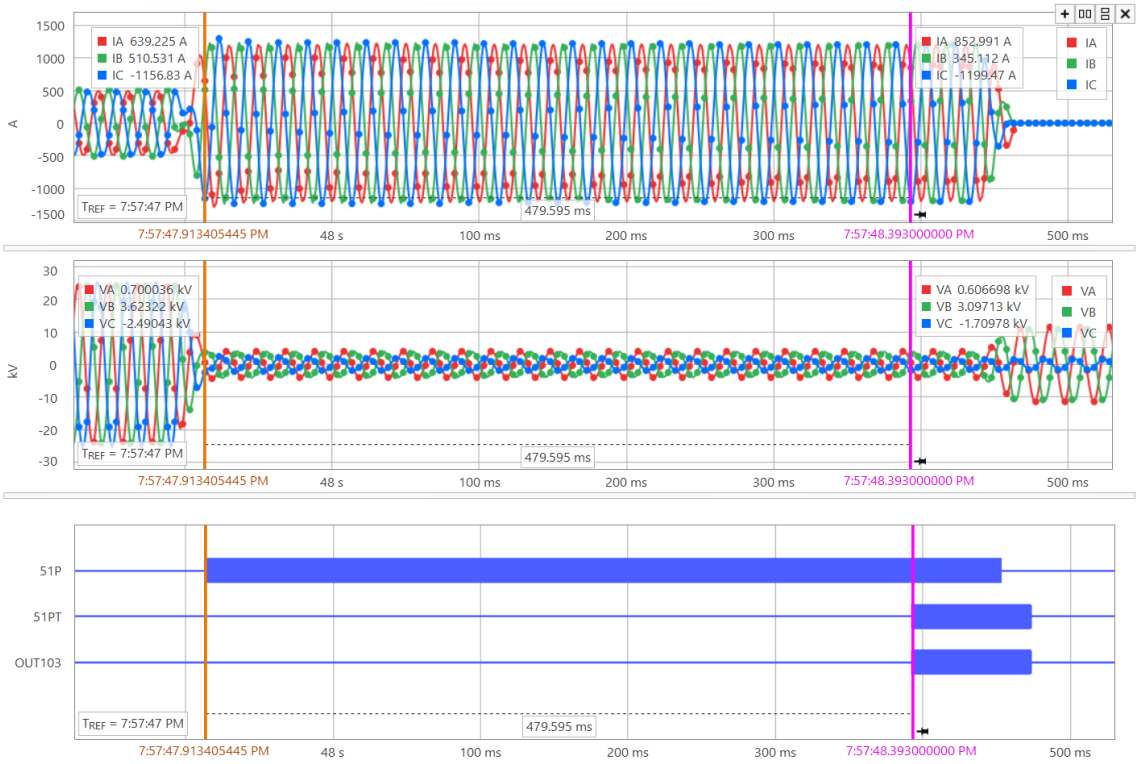

Figure 5.27: **Event for relay 14 during a three-phase fault in grid-connected mode and with maloperation of relay 1**

5.5 Conclusion

This chapter focused on the implementation of a laboratory-scale test bench to demonstrate hardware-in-the-loop (HIL) testing by interfacing the SEL-351A directional overcurrent relays with the RTDS. The SEL-351A relays were configured using AcSELerator Quickset. The relay settings obtained during the DIgSILENT PowerFactory simulations were used for the phase overcurrent and phase time-overcurrent settings. The neutral ground overcurrent and neutral ground time-overcurrent settings were calculated from the single-line-to-ground faults measured during the runtime simulations. The circuit breaker control and fault logic were developed in RSCAD. Three-phase and single-line-to-ground faults were investigated for both grid-connected and islanded modes during the real-time simulation in the RSCAD Runtime. The event files were downloaded from the SEL-351A relays and analysed using SEL SynchroWAVE.

The next chapter focuses on the implementation of the IEC 61850 GOOSE communication protocol during HIL testing.

CHAPTER 6
IMPLEMENTATION OF THE IEC 61850 STANDARD-BASED COMMUNICATION

6.1 Introduction

The IEC 61850 standard "communication networks and systems for power utility automation" was developed to standardise the communication requirements for information sharing and interoperability between intelligent electronic devices (IEDs) from various vendors. The IEC 61850 is used for protection, automation, and control within the substation. Within the IEC 61850 network, each physical device can contain several logical devices, and each logical device can contain several logical nodes (LNs). The GOOSE is used for transmitting critical events in real-time between two or more IEDs using an Ethernet multicast (Bishop and Nair, 2022).

Implementation of the IEC 61850 GOOSE message for overcurrent protection schemes in MGs has the following benefits:

- Fast fault detection and isolation
- Reduced complexity of protection coordination
- Decrease in fault-clearing times
- Ability to adapt to dynamic changes in network configuration and DER operation status.

GOOSE messages enable fast peer-to-peer communication between IEDs without the need for a SCADA platform because they are directly transmitted to the Ethernet link layer (Gu et al., 2019). This chapter aims to develop and implement the IEC 61850 GOOSE application in real-time simulation by interfacing the RTDS with external IEDs.

6.2 Laboratory-scale test bench for overcurrent functional testing using IEC 61850 GOOSE application

The laboratory-scale test bench for hardware-in-the-loop (HIL) testing is implemented using the RTDS and SEL-351A relays, as shown in Figure 6.1. The GTNETx2 card is used to connect the RTDS to the external IED through an Ethernet connection.

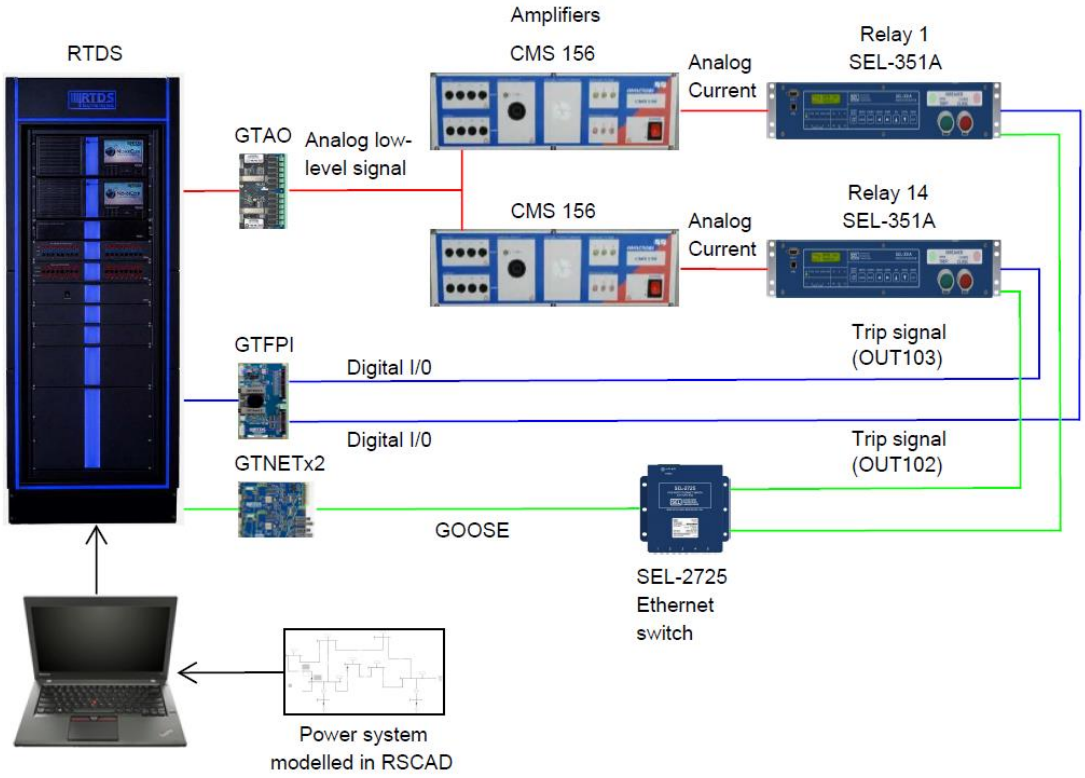

Figure 6.1: **Laboratory-scale test bench setup to demonstrate the GOOSE communication for overcurrent functional testing**

6.2.1 Configuration of the IEC 61850 GOOSE using AcSELerator Architect

The application functions are divided into smaller entities that exchange information between the IEDs. These entities are called logical nodes. A logical node contains a list of data objects with dedicated data attributes. The data is defined in IEC 61850-7-4. The information provided by the logical nodes can be divided into the following categories:

- Common logical node information
- Status information
- Settings
- Measured values
- Controls (IEC 61850-1, 2013)

The logical node information for each category is shown in Figure 6.2.

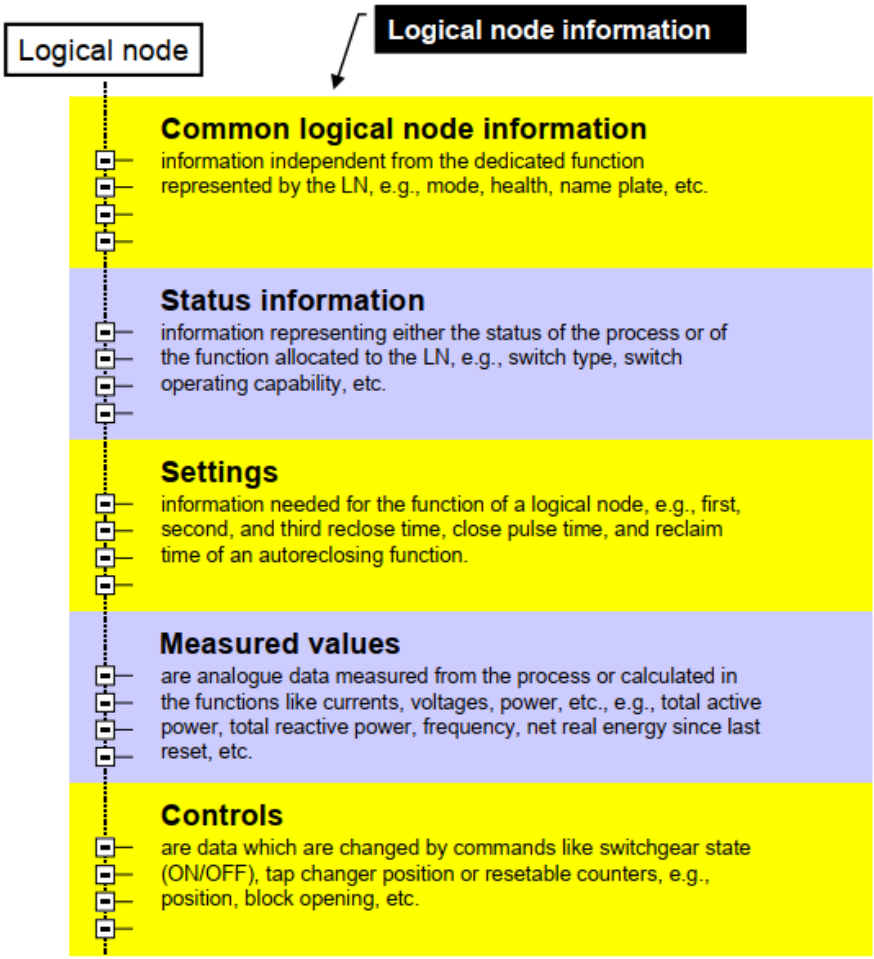

Figure 6.2: Logical node information categories (IEC 61850-7-1, 2011)

When adding IEDs to the project in Architect, the correct relay firmware must be selected, as shown in Figure 6.3. Relay firmware R510 and earlier is selected for the SEL-351A relays that are available at the CSAEMS at CPUT.

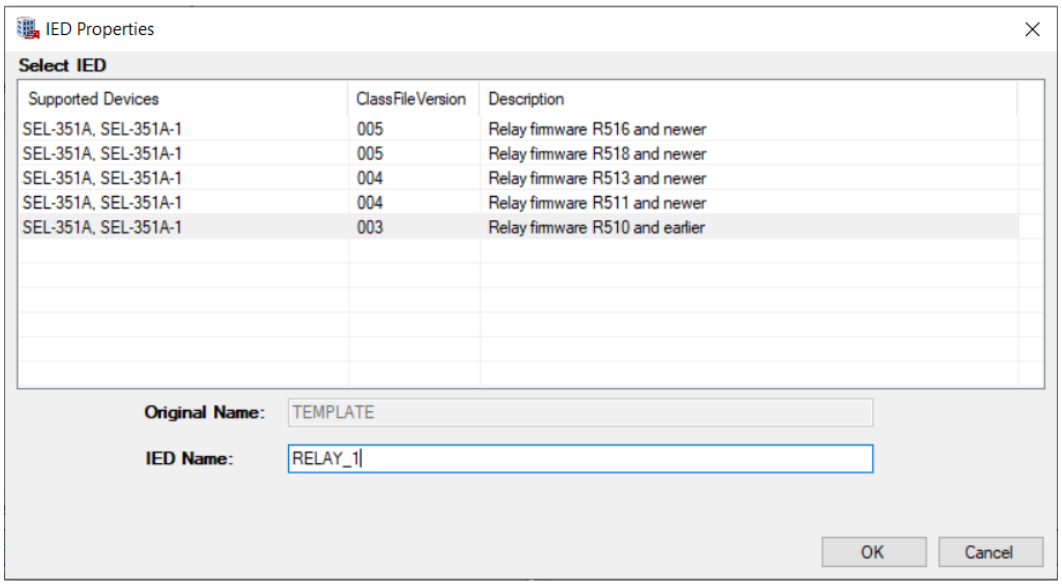

Figure 6.3: Selection of relay firmware for the SEL-351A IEDs

Both relays 1 and 14 are added to the project in Architect as shown in Figure 6.4. The IED properties such as the IP address are in the tap on the right.

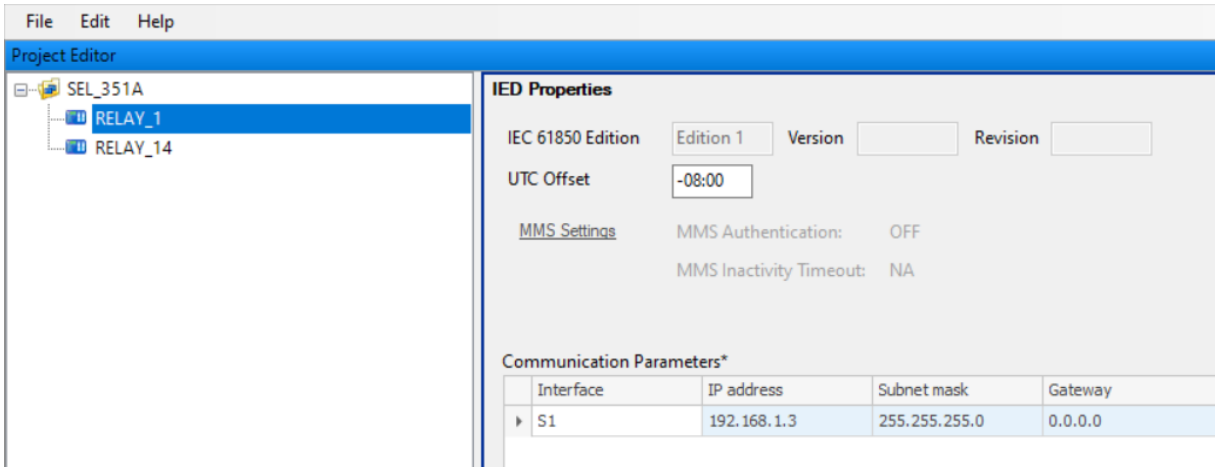

Figure 6.4: IEDs added to the project in Architect

An IED can be configured to subscribe to a specific set of GOOSE messages published by other IEDs on the LAN. The incoming and outgoing GOOSE messages from the IED are configured using AcSELerator Architect. The protection trip conditioning (PTRC) LN connects the output of one or more protection functions to a common trip transmitted to the XCBR. The logic diagram for the protection functions that operate the trip conditioning TRIPPTRC1 LN is shown in Figure 6.5. The dataset configuration containing the trip conditioning TRIPPTRC1 LN is shown in Figure 6.6. The LNs from the IED data items tab on the left are dragged to the dataset tab on the right, as shown in Figure 6.6. The TRIPPTRC1.Tr dataset contains the following data attributes:

- General
- Quality (q)
- Time stamp (t)

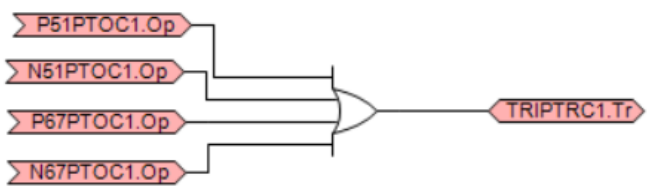

Figure 6.5: Logic diagram for the trip conditioning TRIPPTRC1 LN

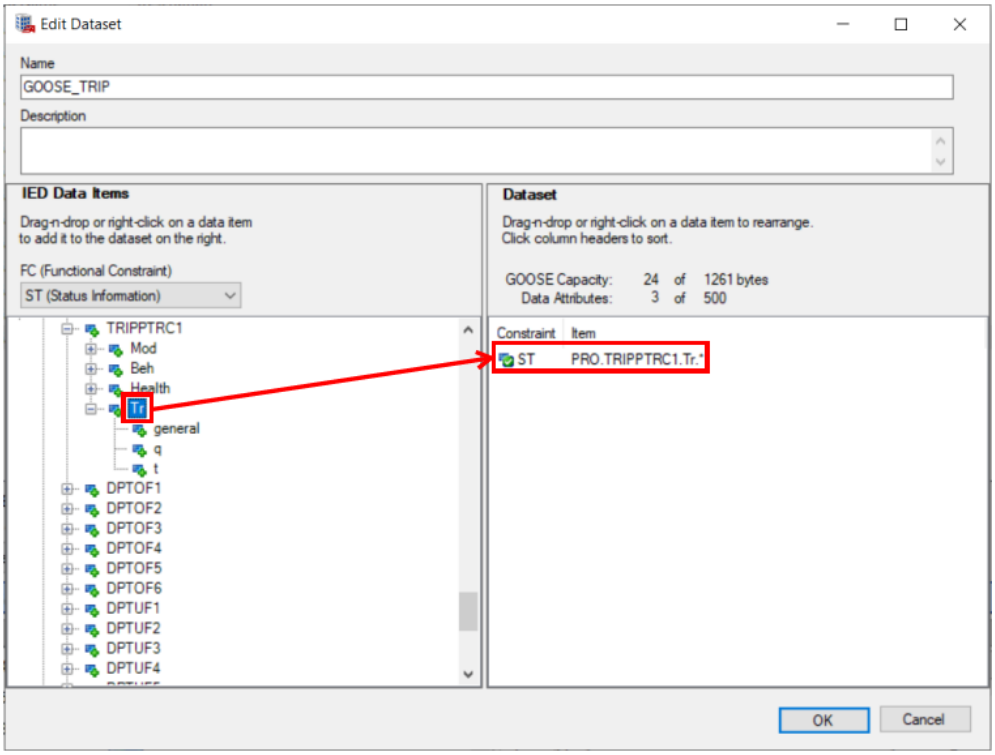

Figure 6.6: Configuration of the dataset in AcSELerator Architect

The GOOSE transmit message configuration is shown in Figure 6.7. The name of the GOOSE message published by relay 1 is GOOSE_TRIP. GOOSE messages use a multicast layer and are identified by MAC addresses and identifiers in the message body. The multicast MAC address of the GOOSE message is 01-0C-CD-01-00-04.

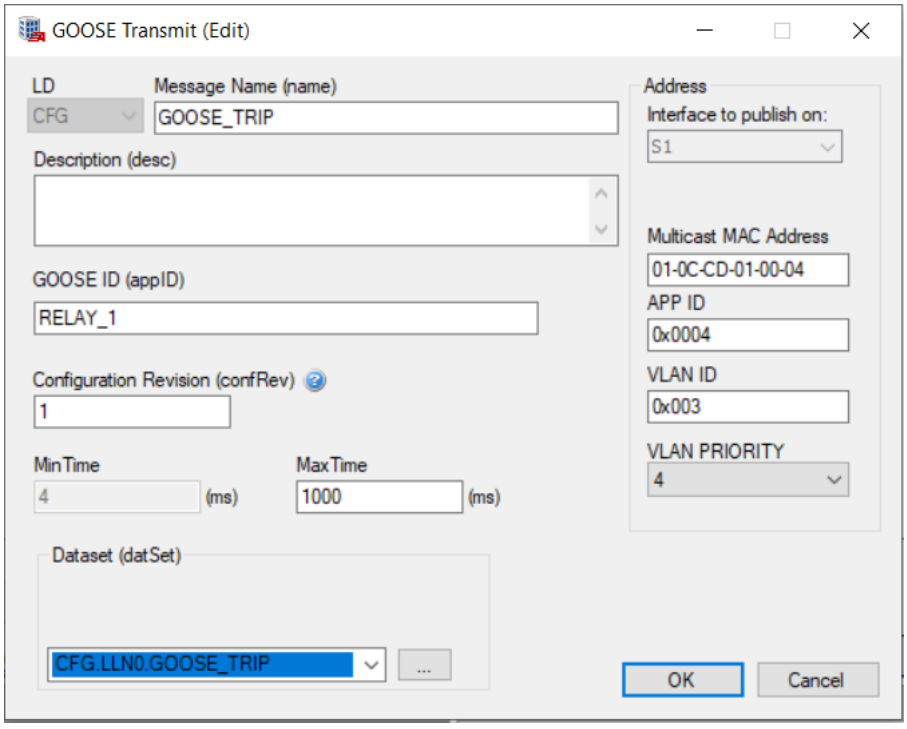

Figure 6.7: Configuration of GOOSE transmit

As shown in Figure 6.8, the GOOSE receive message for relay 14 is configured. The GOOSE_TRIP message published by relay 1 is shown in the left column. The GOOSE message is moved from the left column to the virtual bit VB001 in the right column.

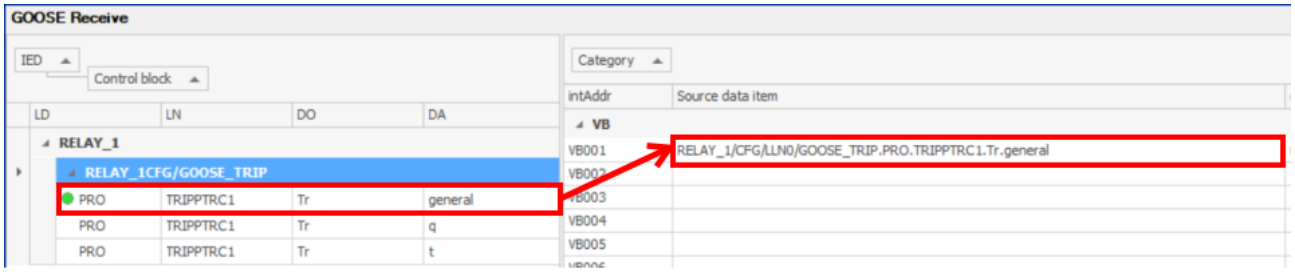

Figure 6.8: Configuration of GOOSE receive

The GOOSE configuration is sent to the SEL IEDs, as shown in Figure 6.9. The IP address of the SEL IED is entered in the FTP address. The username is FTPUSER, and the password is TAIL. The CID file is then ready to be sent to the SEL IED.

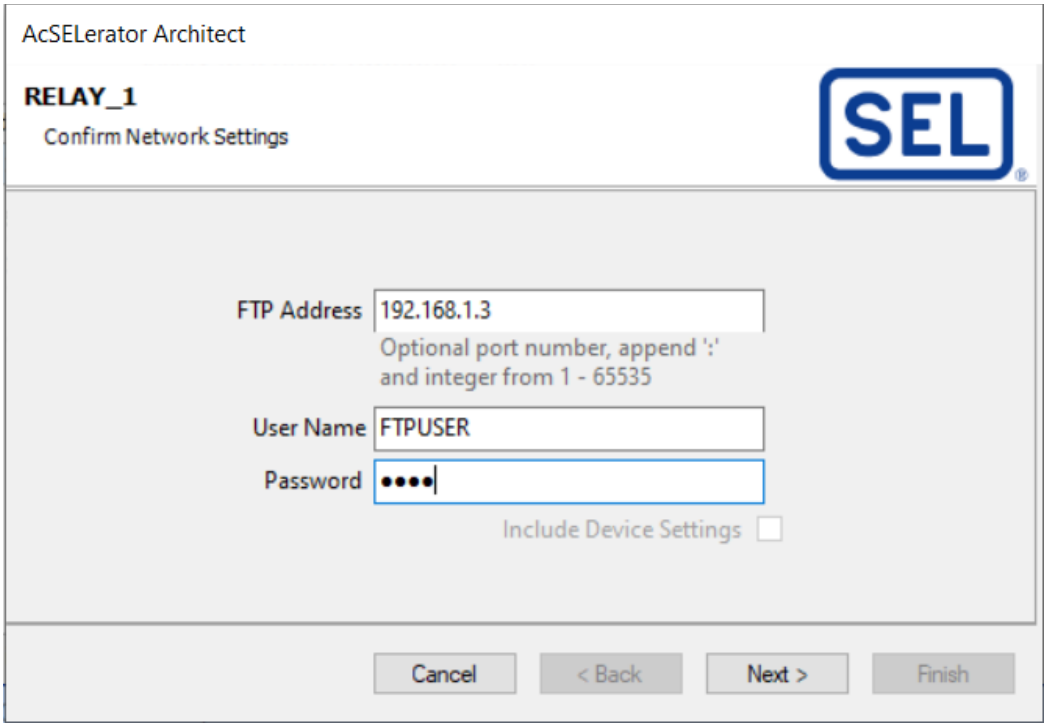

Figure 6.9: FTP address for sending the GOOSE dataset to the IED

6.3 Configuration of the GTNET-GSE in RSCAD

The GTNET card is used to connect the RTDS to the external IED. The circuit breaker control logic in RSCAD is shown in Figure 6.10. The second OR gate is configured for an additional input signal, GOOSE_Trip. The OUT103 output from relay 14 or the GOOSE_Trip signal from relay 1 is sent to the input of the OR gate. The input signal that arrives at the OR gate sends the trip command to the circuit breaker BRK2.

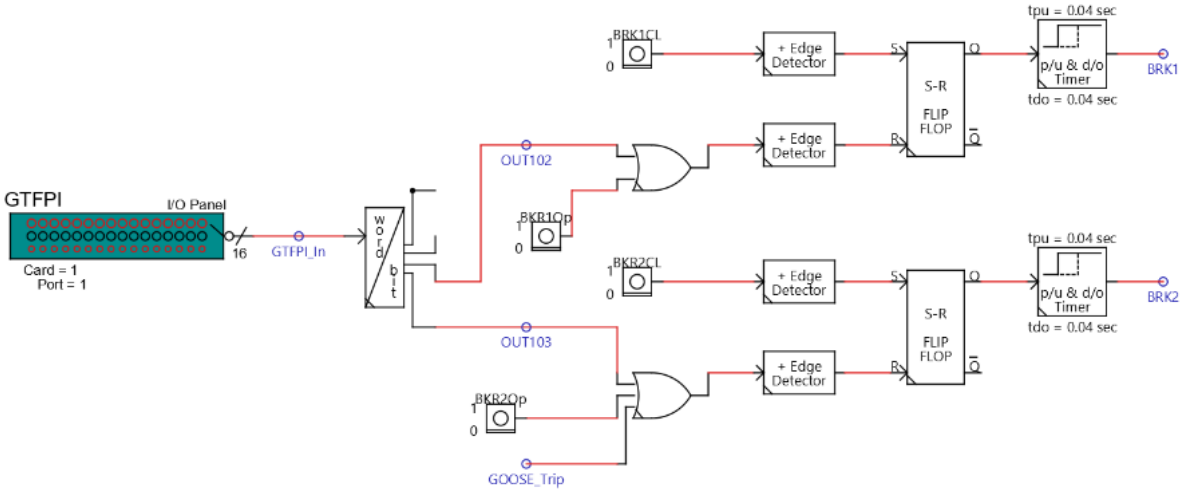

Figure 6.10: Circuit breaker logic in RSCAD

The GTNET-GSE component in RSCAD is used for the IEC 61850 GOOSE communication between the GTNETx2 card installed in the RTDS simulator and the external IED. Figure 6.11 illustrates the GTNET-GSE model in RSCAD. The GTNET-GSE component is configured as shown in Figure 6.12. The GTIO Fiber port number is set to 3. GTNETx2 is selected for GTNET, and GSE version 6 is also selected. The GOOSE_IN and GOOSE_Trip signals are connected to the input and output of the word-to-bit converter, respectively.

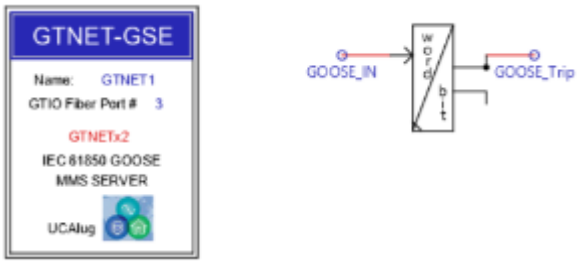

Figure 6.11: GTNET-GSE model in RSCAD

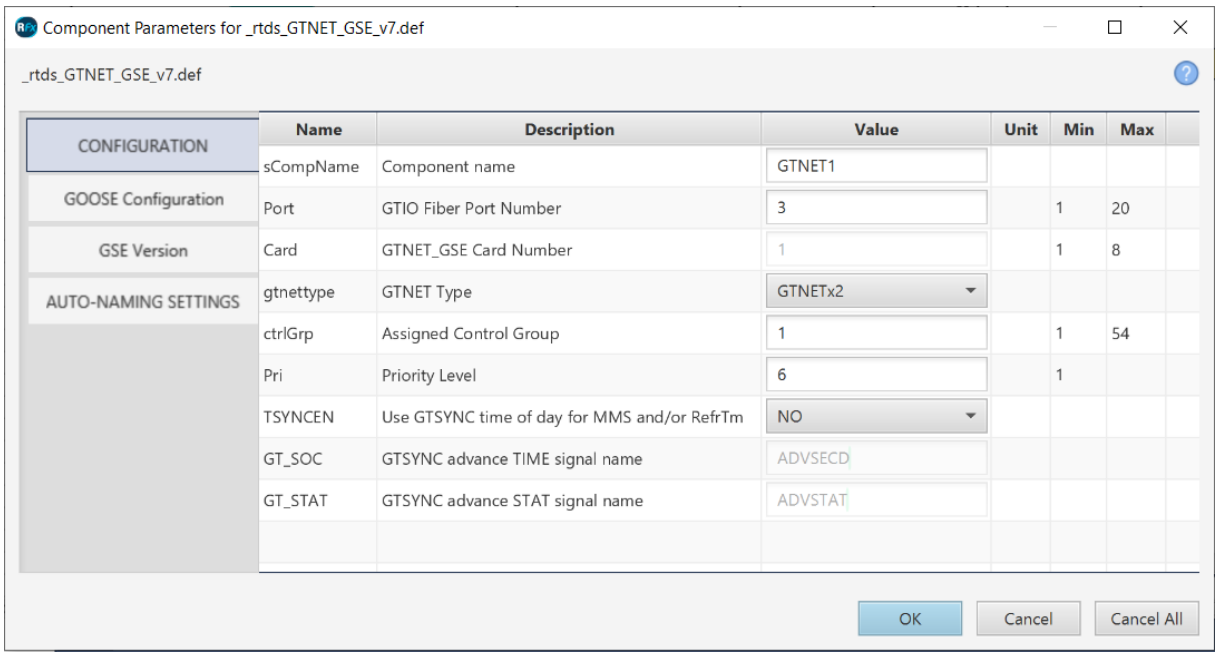

Figure 6.12: Configuration of the GTNET-GSE component

6.3.1 Configuration of the IEC 61850 GOOSE application in RSCAD IEC 61850 ICT tool

The RSCAD IEC 61850 ICT is used to configure the GTNET-GSE component, where the IEC 61850 GOOSE data sets can also be configured. As shown in Figure 6.13, IEC 61850 defines object-oriented data models. The physical device is defined by its IP address. Each physical device contains an access point and a server that contains several logical devices (LDs). Each LD can contain many LNs that represent physical elements or functions (such as protection functions). Each LN contains a group of data objects (DOs) associated with a function. Each DO includes several data attributes (DAs) representing information related to the LN (such as status, settings, etc.).

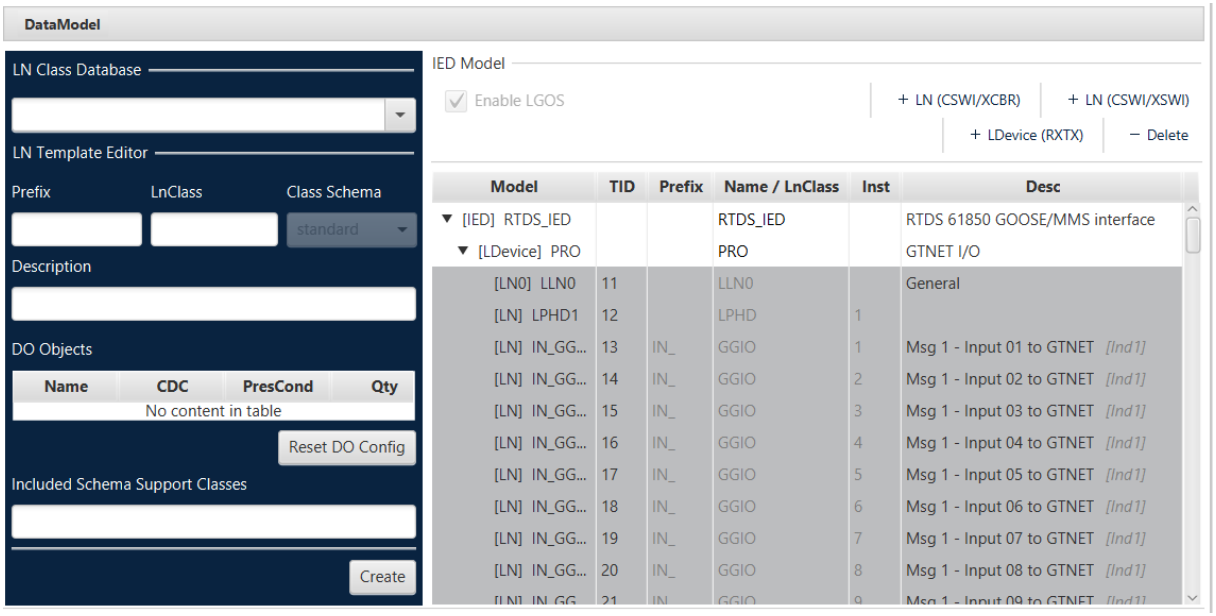

Figure 6.13: Configuration of the data model in the IEC 61850 ICT project

The GTNET-GSE is configured to subscribe to the GOOSE message published by relay 1, as shown in Figure 6.14. The GOOSE message contains the conditional trip TRIPPTRC1 LN. The "Tr" in the DO tab represents trip status information. The "general" in the DA tab represents the operation of the trip status information, and the "q" in the DA tab represents the quality of the trip status information.

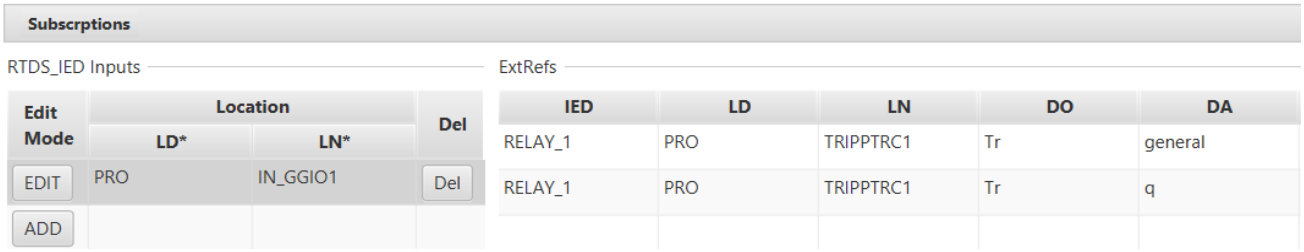

Figure 6.14: Configuration of GOOSE subscriptions

The GTNET-GSE is configured to publish the GOOSE message, as shown in Figure 6.15. The GOOSE message contains the generic process I/O (GGIO) LN. The "Ind1" in the DO tab represents the general indication (binary input). The "stVAL" in the DA tab represents the status value of the Ind1 LN, and the "q" in the DA tab represents the quality of the Ind1 LN.

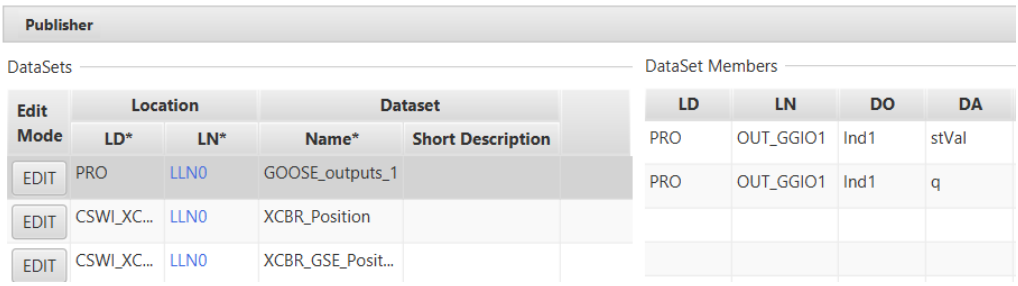

Figure 6.15: Configuration of GOOSE publications

6.4 Hardware-in-the-loop protection functional testing with the GOOSE communication

6.4.1 HIL testing for a three-phase fault during grid-connected mode with GOOSE message

The three-phase fault current measured by CT1 and the circuit breaker control signals for relay 1 are shown in Figure 6.16. Figure 6.17 shows the GOOSE trip signal published by relay 1, which changes from logical 0 to logical 1 with no intentional time delay after the OUT102 output is asserted. When the OUT102 output from relay 1 is asserted after a time delay of 40 ms, the BRK1 signal changes from logical 1 to logical 0. The measured current is 152.89 A under steady-state conditions. The fault current is cleared once circuit breaker 1 is opened. The RMS fault current is 16.842 kA, whereas the peak fault current is:

$$\boldsymbol{I_p = \sqrt{2} \cdot I_{rms} = \sqrt{2} \cdot (16.842) = 23.818\ kA}$$

The information from the SER for relay 1 in Table 6.1 indicates that the 50P1, 51P OUT101 outputs are asserted at 332 ms. The 67P1T element and OUT102 output are asserted at 402 ms. The time delay is 402 - 332 = 70 ms. All the elements are de-asserted at 462 ms. GOOSE message is published by relay 1 at 402.594 ms based on the information from the captured GOOSE message.

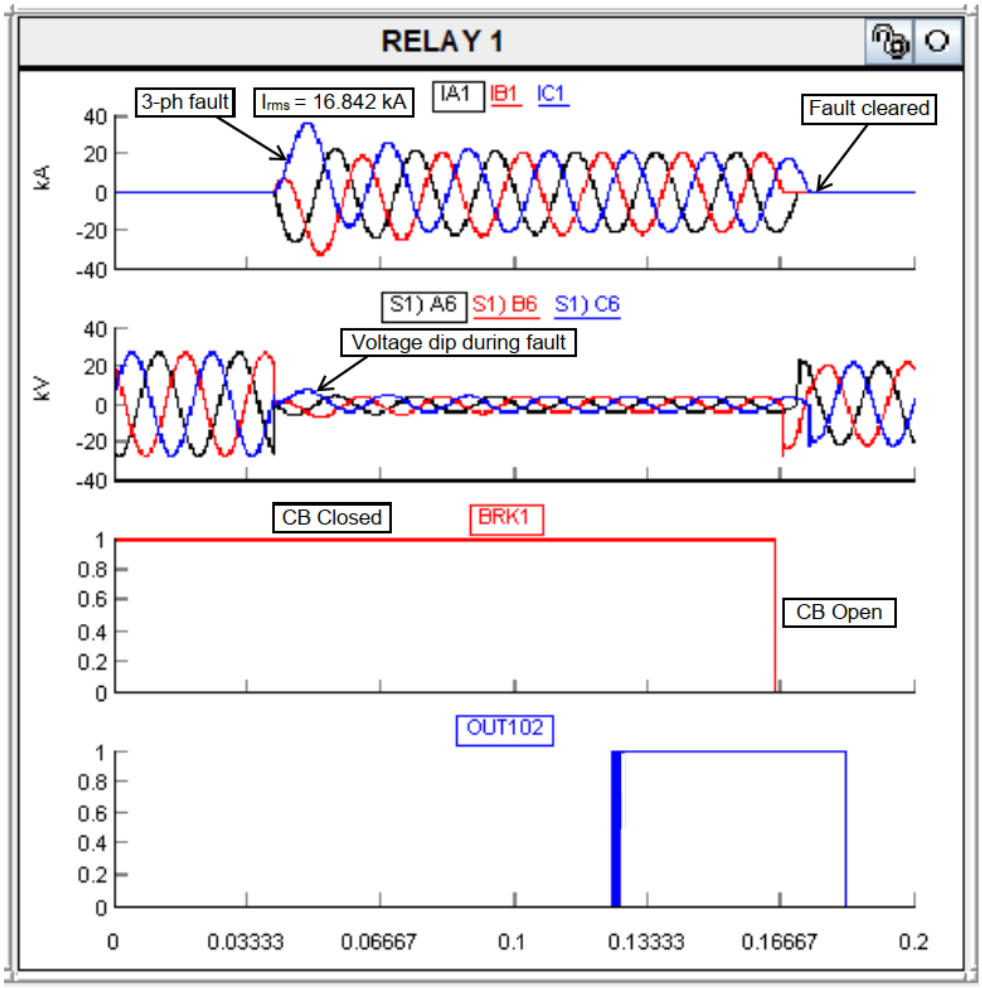

Figure 6.16: Three-phase fault and circuit breaker control for relay 1 during grid-connected mode

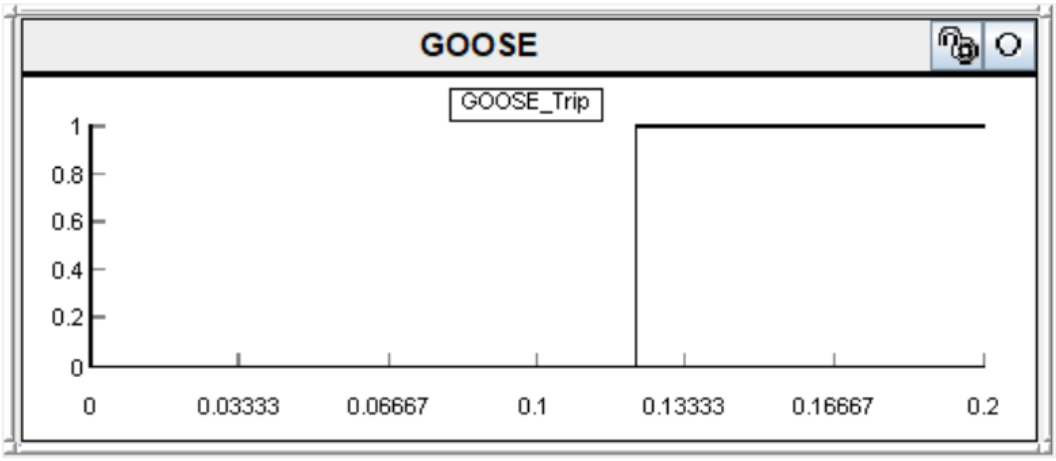

Figure 6.17: GOOSE message published by relay 1 during a three-phase fault in grid-connected mode

Table 6.1: SER for relay 1 during a three-phase fault in grid-connected mode

Time (ms)	Function	State
332	50P1	Asserted
332	51P	Asserted
332	OUT101	Asserted
402	67P1T	Asserted
402	OUT102	Asserted
462	51P	De-asserted
462	67P1T	De-asserted
462	OUT101	De-asserted
462	OUT102	De-asserted

The event for relay 1 is shown in Figure 6.18. The measured three-phase fault currents are as follows:

I_A = 16842 A, I_B = 16621 A, I_C = 17322 A

The 50P1 element is asserted at 332 ms based on the recorded event. The 67P1T element and OUT102 output are asserted at 402.026 ms. The tripping time is 402.026 – 332 = 70.026 ms. The fault current is cleared at 482.062 ms. The TRIP signal remains asserted until the relay is reset through the HMI.

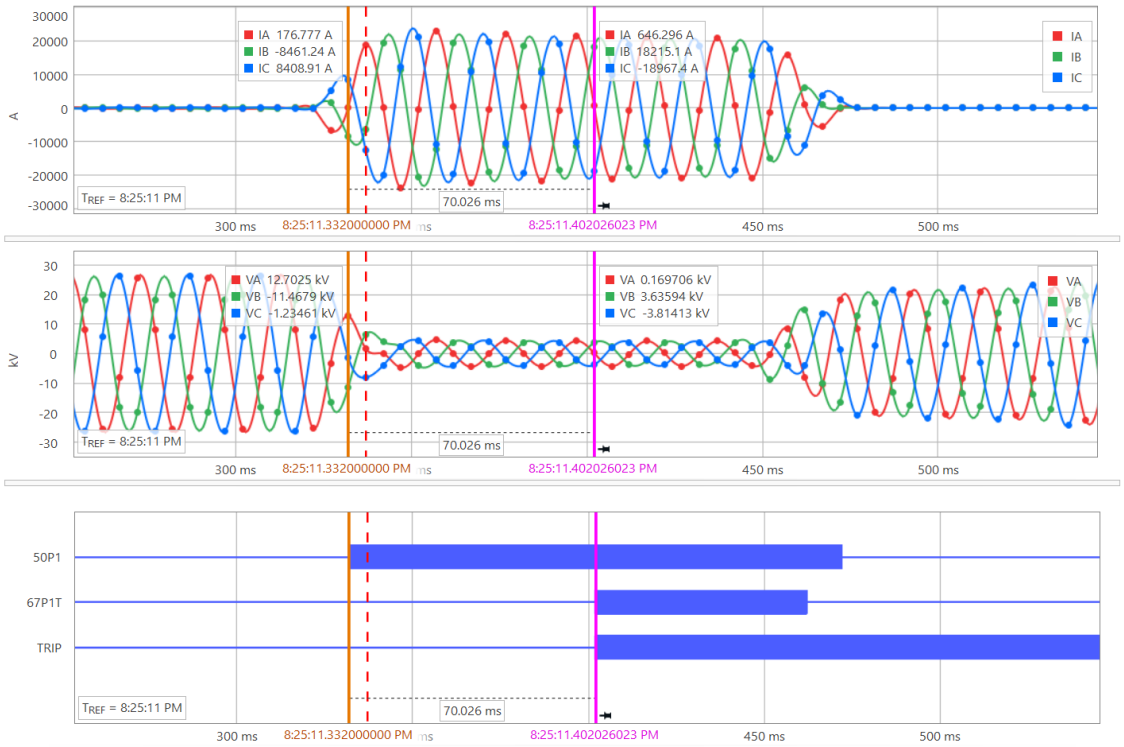

Figure 6.18: Event for relay 1 during a three-phase fault in grid-connected mode

The measured fault current from CT2 and the relay 14 circuit breaker control output are shown in Figure 6.19. The BRK2 signal changes from logical 1 to logical 0 once relay 14 subscribes to the GOOSE message. The fault current is cleared once circuit breaker 2 is opened.

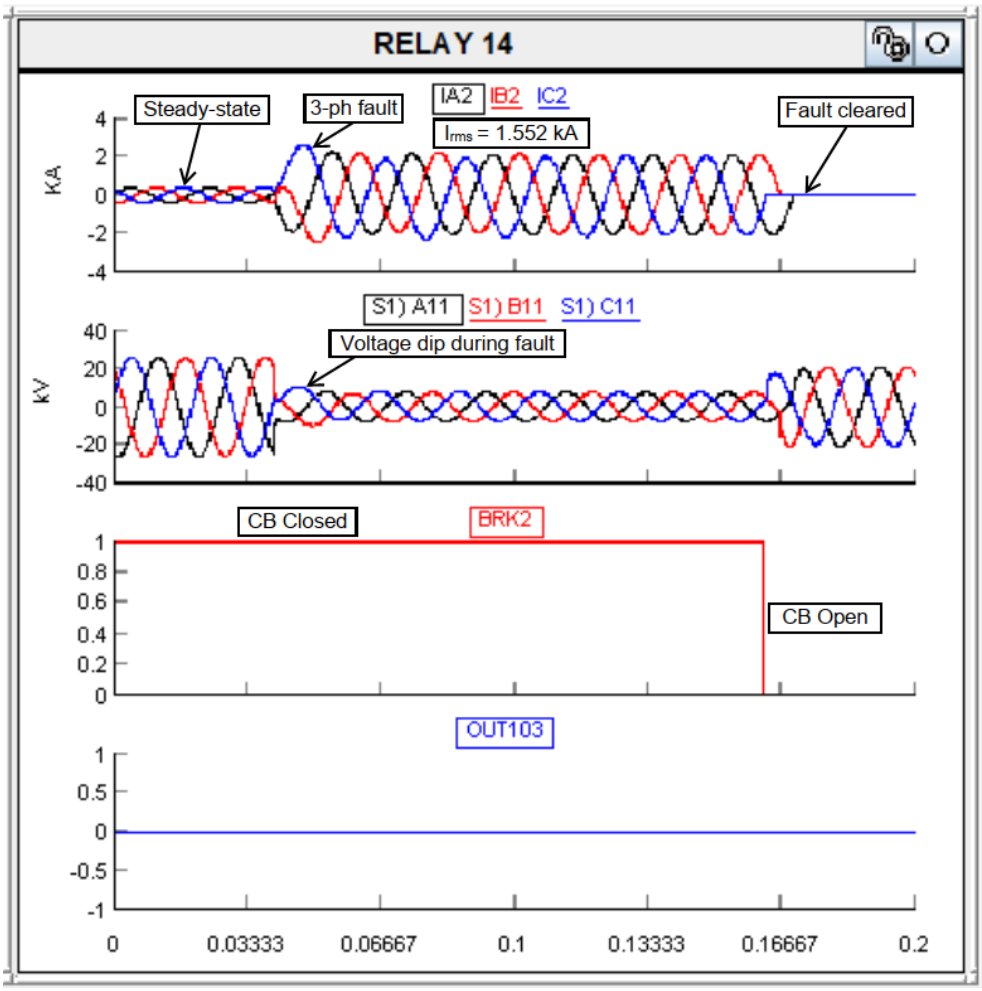

Figure 6.19: **Three-phase fault and circuit breaker control for relay 14 during grid-connected mode**

The SER data for relay 14 represented in Table 6.2, indicates that the 51P element and OUT101 output are asserted at 752 ms and then de-asserted at 882 ms after VB001 is asserted at 817 ms. The virtual bit VB001 is asserted once relay 14 subscribes to the GOOSE message transmitted through the Ethernet with the dataset containing the protection trip conditioning (TRIPPTRC1) LN. The 51P element and OUT101 output are de-asserted at 882 ms.

Table 6.2: SER for relay 14 during a three-phase fault in grid-connected mode

Time (ms)	Function	State
752	51P	Asserted
752	OUT101	Asserted
762	51P	De-asserted
762	OUT101	De-asserted
772	51P	Asserted
772	OUT101	Asserted
817	VB001	Asserted
882	51P	De-asserted
882	OUT101	De-asserted

6.4.2 HIL testing for a single-phase-to-ground fault during grid-connected mode with GOOSE message

The single-phase-to-ground fault current measured by CT1 and the circuit breaker control signals for relay 1 are shown in Figure 6.20. Figure 6.21 shows the GOOSE trip signal published by relay 1, which changes from logical 0 to logical 1 once the OUT102 output is asserted. When the OUT102 output from relay 1 is asserted after a time delay of 40 ms, the BRK1 signal changes from logical 1 to logical 0. The measured current is 158.012 A under steady-state conditions. When circuit breaker 1 is opened, the fault current is cleared. The RMS fault current is 13.642 kA, whereas the peak fault current is:

$$\boldsymbol{I_p = \sqrt{2} \cdot I_{rms} = \sqrt{2} \cdot (13.642) = 19.293\ kA}$$

The SER data for relay 1 in Table 6.3, indicates that the 51N element is asserted at 523 ms. The 50N1 element and OUT101 output are asserted at 528 ms, whereas the 67N1T element and OUT102 output are asserted at 578 ms,. Tripping time is 55 ms. The 50N1, 67N1T, and OUT102 outputs are de-asserted at 648 ms, whereas the 51N element and OUT101 output are de-asserted at 658 ms.

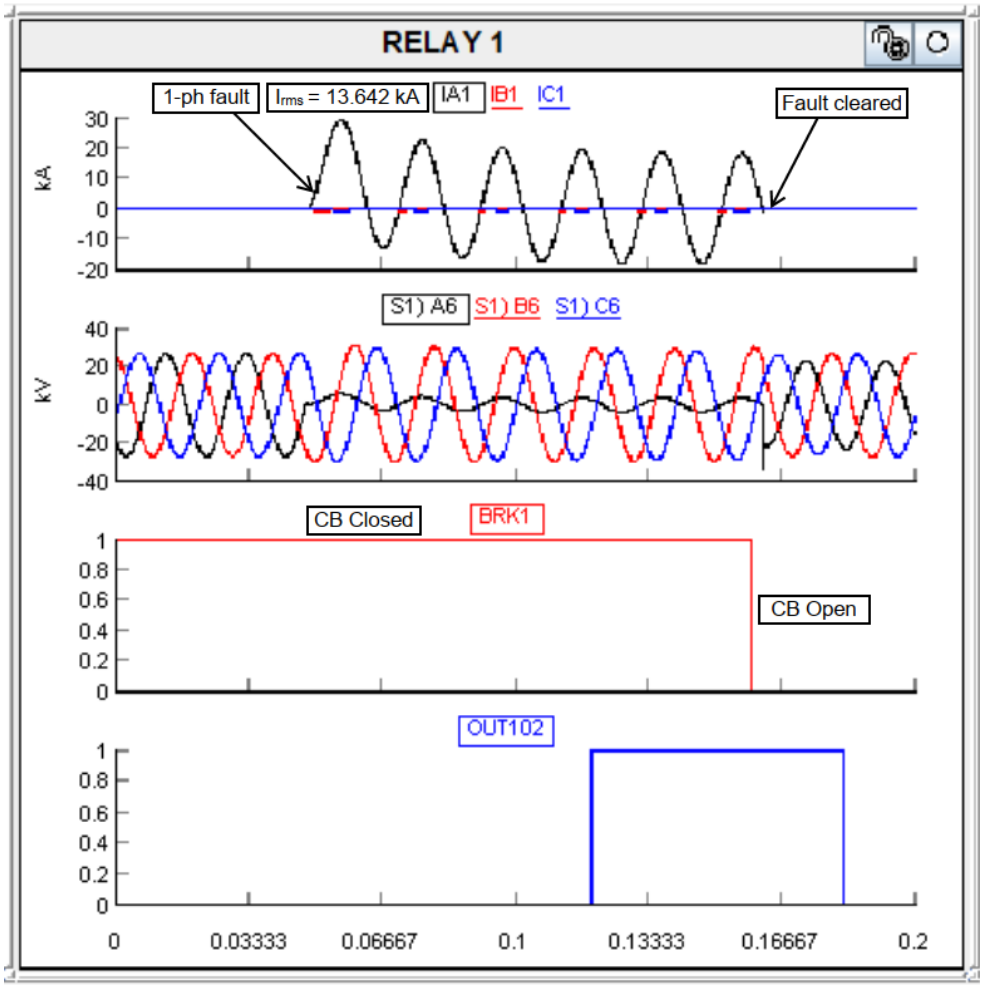

Figure 6.20: Single-phase-to-ground fault and circuit breaker control for relay 1 during grid-connected mode

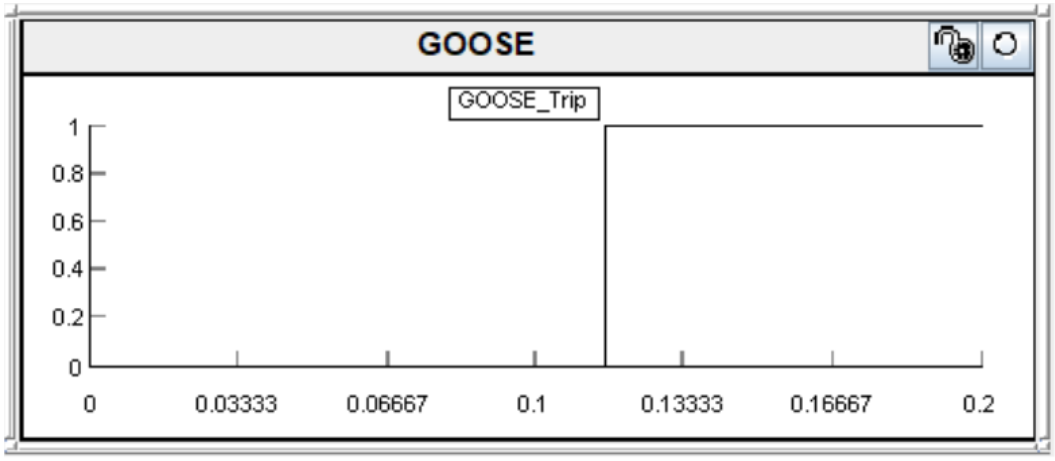

Figure 6.21: GOOSE message published by relay 1 during a single-phase fault in grid-connected mode

Table 6.3: SER for relay 1 during a single-phase to ground fault in grid-connected mode

Time (ms)	Function	State
523	51N	Asserted
528	OUT101	Asserted
528	50N1	Asserted
578	67N1T	Asserted
578	OUT102	Asserted
648	50N1	De-asserted
648	67N1T	De-asserted
648	OUT102	De-asserted
658	51N	De-asserted
658	OUT101	De-asserted

Figure 6.22 shows the fault event for relay 1. Based on the recorded event, the 50P1 element is asserted at 528 ms. The 67N1T element and OUT102 output are asserted at 402.026 ms. The tripping time is 578.114 – 528 = 50.114 ms, whereas the fault current is cleared at 663.151 ms.

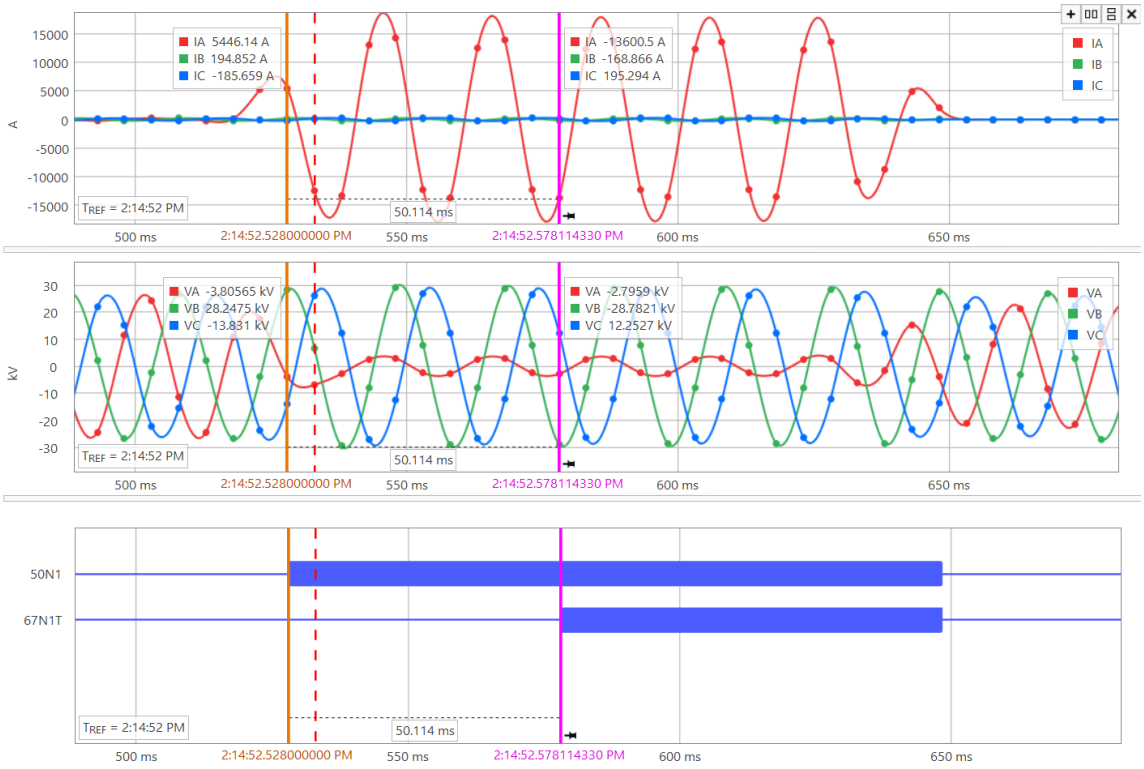

Figure 6.22: Event for relay 1 during a single-phase-to ground-fault in grid-connected mode

Figure 6.23 shows the single-phase-to-ground fault current measured by CT2 and the circuit breaker control signals for relay 14. When the OUT103 output from relay 14 is asserted after a time delay of 40 ms, the BRK2 signal changes from logical 1 to logical 0. The measured current is 158.012 A under steady-state conditions. When circuit breaker 2 is opened, the fault current is cleared. The RMS fault current is 1.474 kA, whereas the peak fault current is:

$$\boldsymbol{I_p = \sqrt{2} \cdot I_{rms} = \sqrt{2} \cdot (1.474) = 2.085\ kA}$$

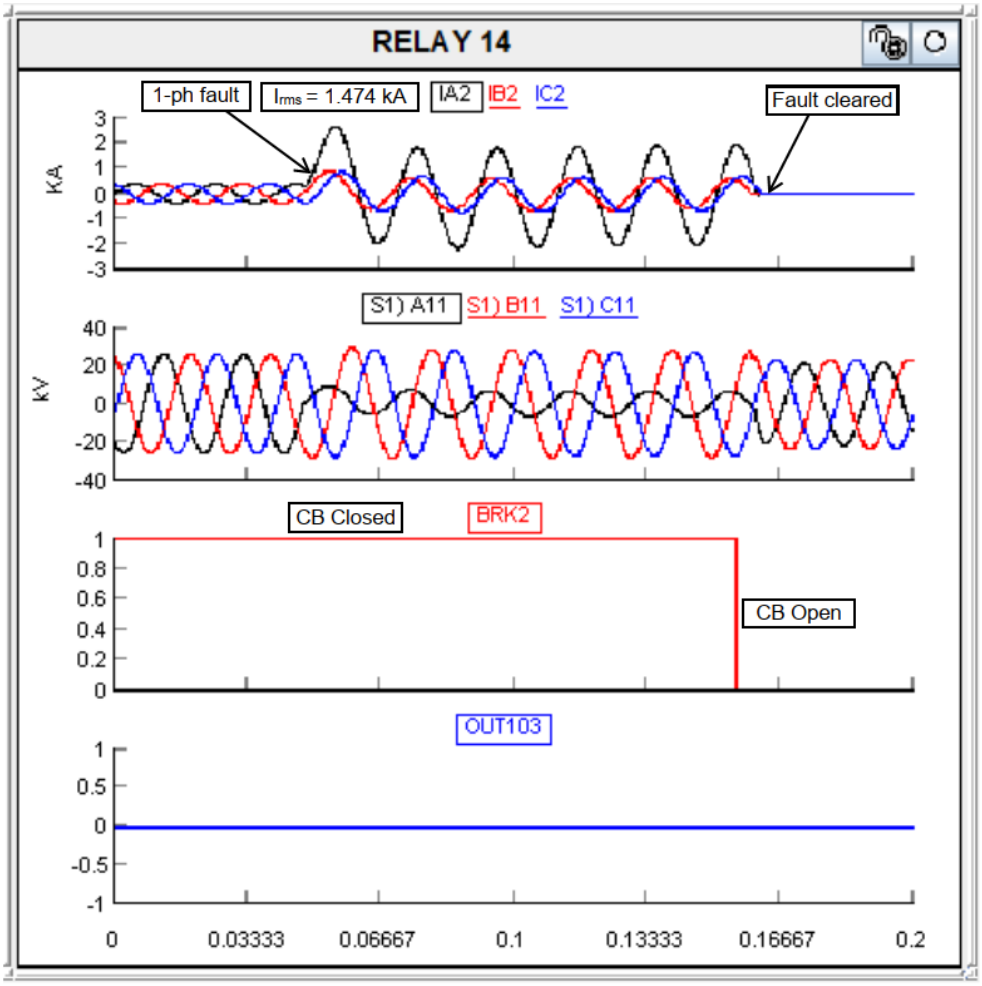

Figure 6.23: **Single-phase-to-ground fault and circuit breaker control for relay 14 during grid-connected mode**

The SER data for relay 14 from Table 6.4, indicates that the 51N element and OUT101 output from relay 14 are asserted at 659 ms and then de-asserted at 779 ms after VB001 is asserted at 714 ms. The virtual bit VB001 is asserted once relay 14

subscribes to the GOOSE message transmitted through the Ethernet with the dataset containing the protection trip conditioning (TRIPPTRC1) LN.

Table 6.4: SER for relay 14 during a single-phase-to-ground fault in grid-connected mode

Time (ms)	Function	State
659	51N	Asserted
659	OUT101	Asserted
714	VB001	Asserted
779	51N	De-asserted
779	OUT101	De-asserted

6.4.3 HIL testing for a three-phase fault during islanded mode with GOOSE message

The three-phase fault current measured by CT1 and the circuit breaker control signals for relay 1 are shown in Figure 6.24. Figure 6.25 shows the GOOSE trip signal published by relay 1, which changes from logical 0 to logical 1 once the OUT102 output is asserted. The BRK1 signal changes from logical 1 to logical 0 when the OUT102 output from relay 1 is asserted after a time delay of 40 ms. The measured current is 161.5 A under steady-state conditions. The fault current is cleared after circuit breaker 1 is opened. The RMS fault current is 9.49 kA, whereas the peak fault current is:

$$\boldsymbol{I_p = \sqrt{2} \cdot I_{rms} = \sqrt{2} \cdot (9.49) = 13.421\ kA}$$

The SER data for relay 1 in Table 6.5, indicates that the 51P element and OUT101 output are asserted at 754 ms. The 50P1 element is asserted at 759 ms, whereas the 67P1T element and OUT102 output are asserted at 824 ms. The tripping time is 65 ms. The 51P, 67P1T, OUT101, and OUT102 outputs are de-asserted at 884 ms, whereas the 50P1 element is de-asserted at 889 ms.

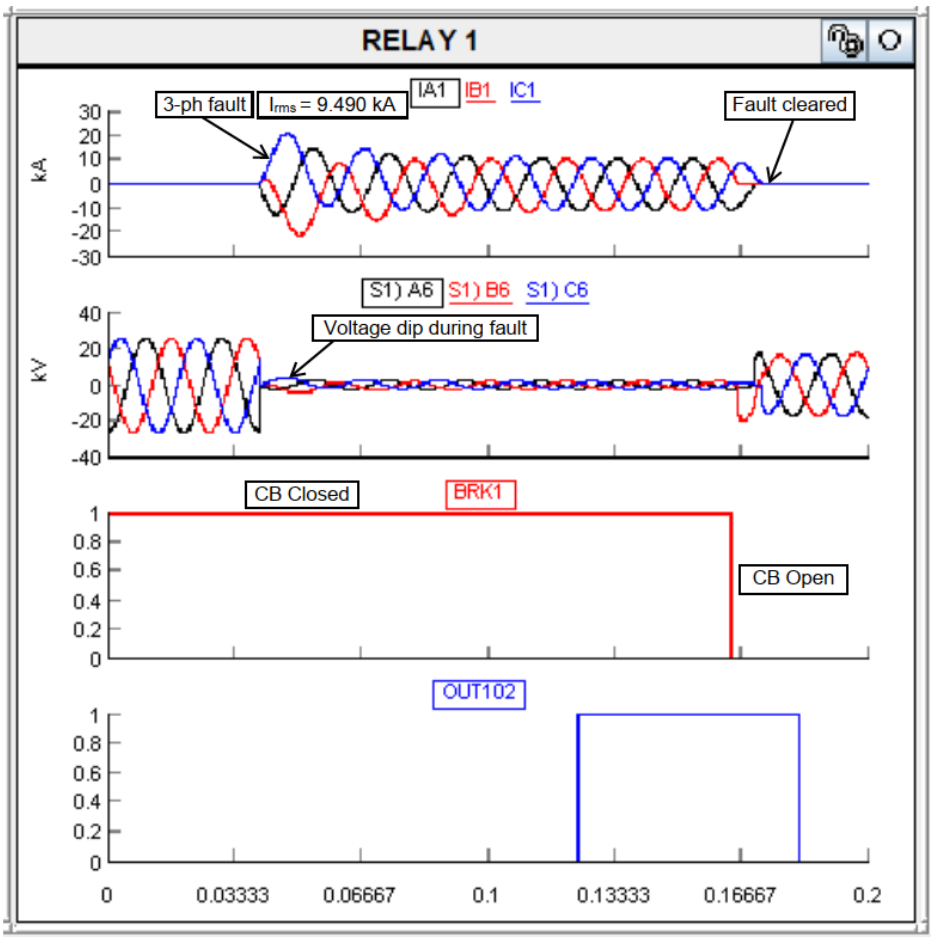

Figure 6.24: Three-phase fault and circuit breaker control for relay 1 during islanded mode

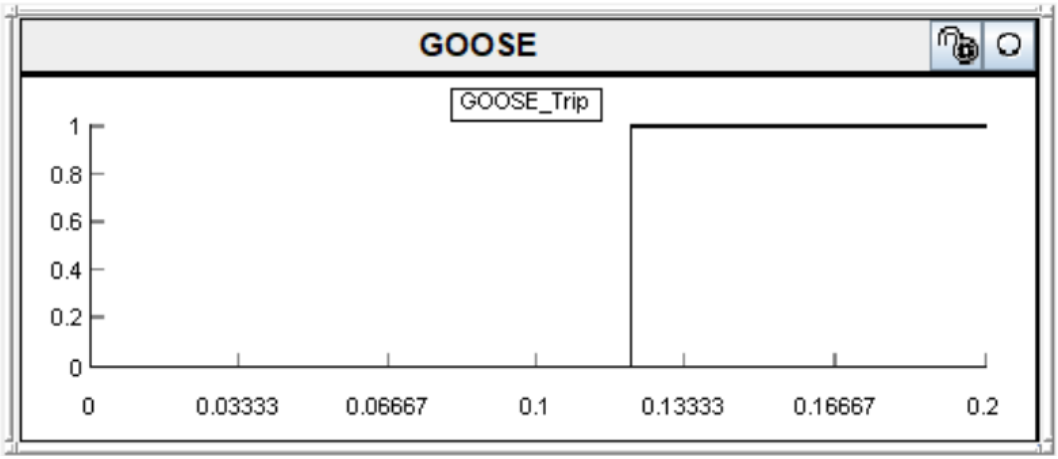

Figure 6.25: GOOSE message published by relay 1 during a three-phase fault in islanded mode

Table 6.5: SER for relay 1 during a three-phase fault in islanded mode

Time (ms)	Function	State
754	51P	Asserted
754	OUT101	Asserted
759	50P1	Asserted
824	67P1T	Asserted

824	OUT102	Asserted
884	51P	De-asserted
884	67P1T	De-asserted
884	OUT101	De-asserted
884	OUT102	De-asserted
889	50P1	De-asserted

The event for relay 1 is shown in Figure 6.26. The measured three-phase fault currents are as follows:

I_A = 9490 A, I_B = 9399 A, I_C = 9621 A

The 50P1 element is asserted at 759 ms based on the recorded event. The 67P1T element and OUT102 output are asserted at 824 ms. The tripping time is 824 – 759 = 65 ms. The fault current is cleared at 904 ms. The TRIP signal remains asserted until the relay is reset through the HMI.

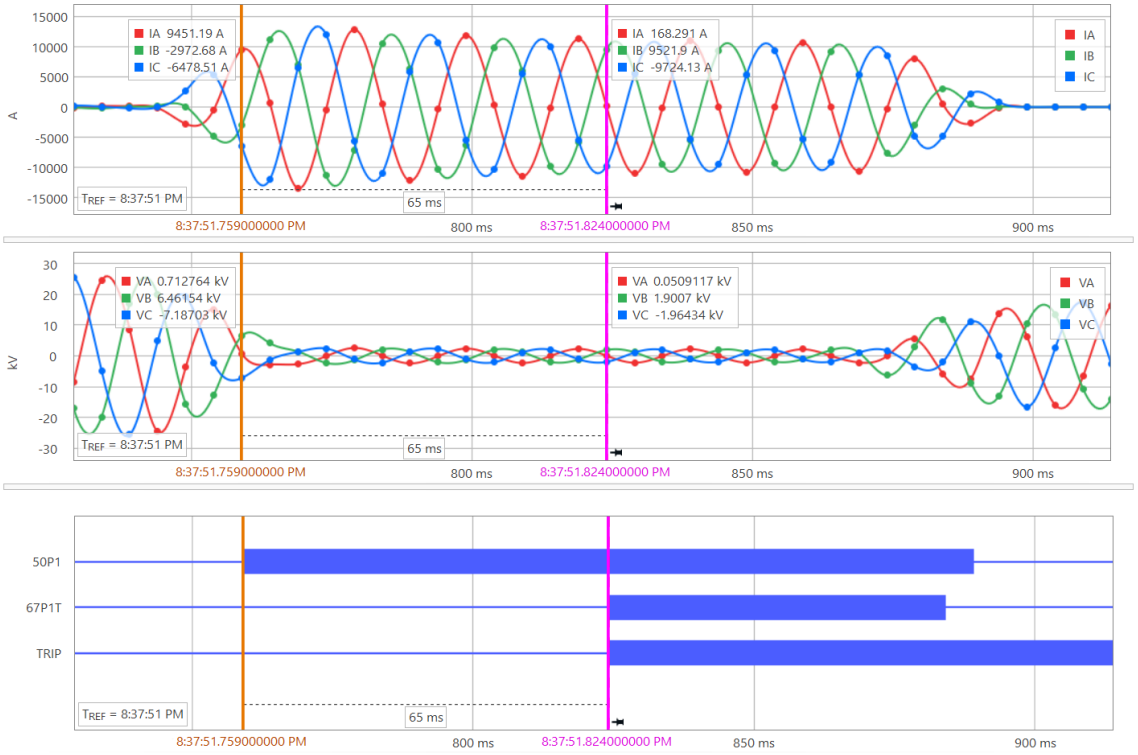

Figure 6.26: Event for relay 1 during a three-phase fault in grid-connected mode

The three-phase fault current measured by CT2 and the circuit breaker control signals for relay 14 are shown in Figure 6.27. The BRK2 signal changes from logical 1 to logical

0 once relay 14 subscribes to the GOOSE message. The fault current is cleared once circuit breaker 2 is opened. The RMS fault current is 0.948 kA, whereas the peak fault current is:

$$I_p = \sqrt{2} \cdot I_{rms} = \sqrt{2} \cdot (0.948) = 1.341\ kA$$

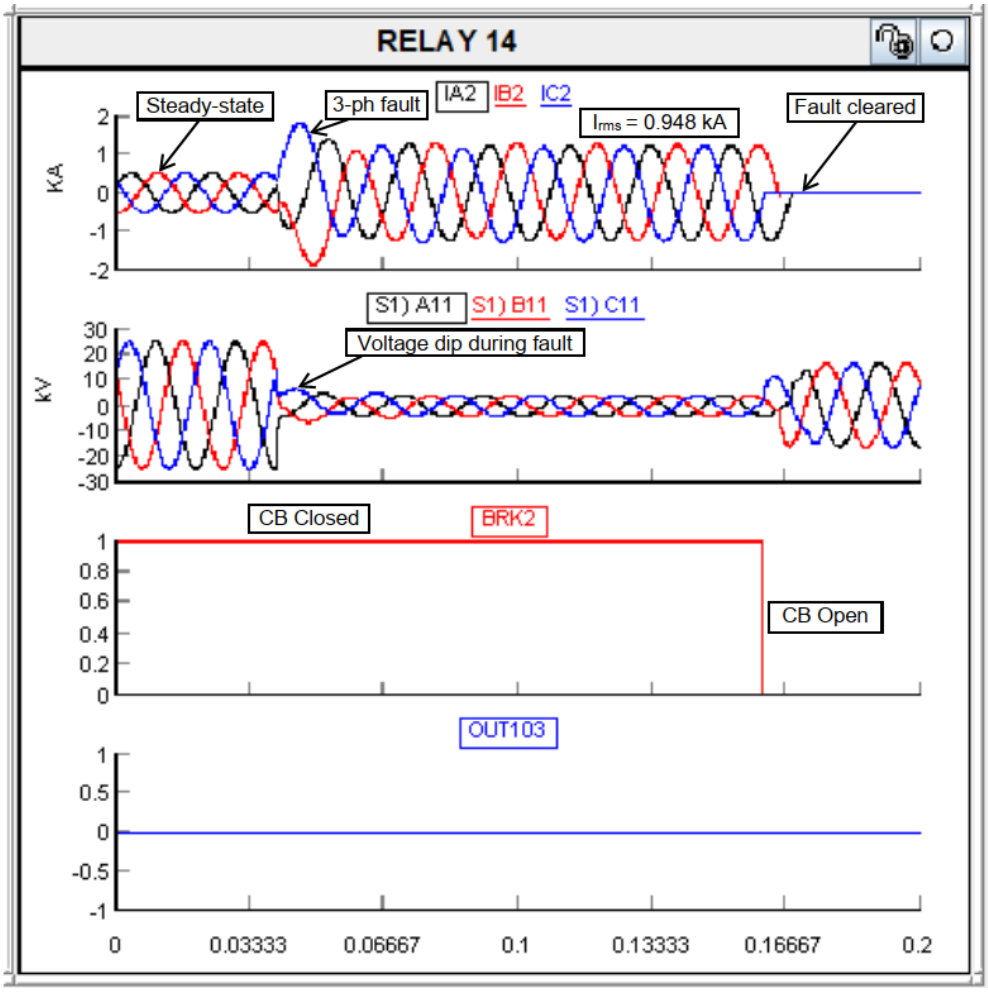

Figure 6.27: **Three-phase fault and circuit breaker control for relay 14 during islanded mode**

The data for relay'14 SER in Table 6.6, indicates that the 51P element and OUT101 output from relay 14 are asserted at 778 ms and then de-asserted at 898 ms after VB001 is asserted at 838 ms. The virtual bit VB001 is asserted once relay 14 subscribes to the GOOSE message transmitted through the Ethernet with the dataset containing the protection trip conditioning (TRIPPTRC1) LN.

Table 6.6: SER for relay 14 during a three-phase fault in islanded mode

Time (ms)	Function	State
778	51P	Asserted
778	OUT101	Asserted
838	VB001	Asserted
898	51P	De-asserted
898	OUT101	De-asserted

6.4.4 GOOSE message monitoring

The published GOOSE message may contain multiple data objects or attributes. The time interval between the GOOSE messages that are published is relatively long if there is no change in the attribute value. When the value contained in the data set changes, the updated GOOSE message is published with no intentional time delay. The subscriber requires a mechanism to handle the GOOSE message. Other than the data content contained in the GOOSE message, it also contains additional information such as the parameters of state number (StNum) and sequence number (SqNum). These two parameters assist the subscriber in identifying if the GOOSE message contains new data or not. This helps with the filtering of the GOOSE message, saving time and processing resources for the subscriber (Cigre 540, 2013).

GOOSE messaging is based on a multicast publisher/subscriber mechanism and contains information such as status along with the associated quality. The subscriber does not acknowledge receipt of a GOOSE message, and therefore the messages are published and repeated in a predefined pattern to achieve the reliability that is required. The GOOSE retransmission process is shown in Figure 6.28. The status number is incremented by one after each event, and the sequence number is set to zero. The sequence number is incremented on each retransmission until the next event (RTDS manual, 2022).

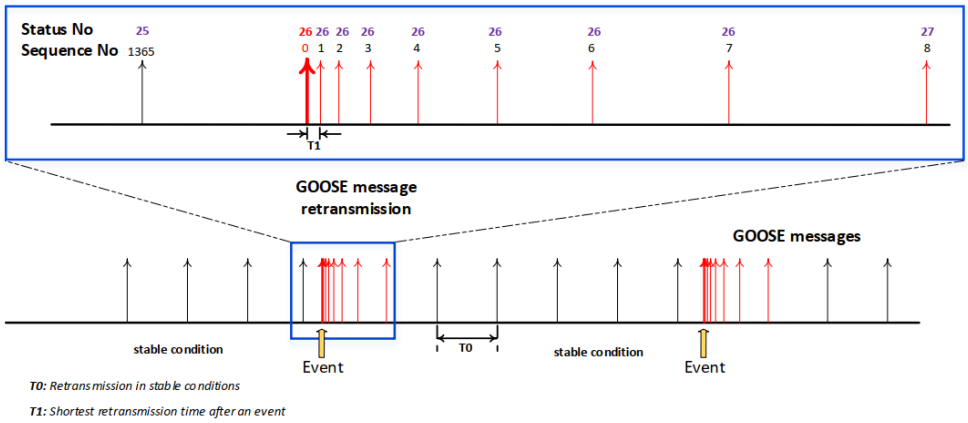

Figure 6.28: GOOSE retransmission process (RTDS manual, 2022)

When the GOOSE message is published, the attributes can be monitored using programs such as Wireshark, which can monitor the IEC 61850 GOOSE messages via the Ethernet. The source address for the sending IED is Schweitz_03:54:90 (00:30: a7:03:54:90). The MAC address (1:0C: CD: 01:00:04) for the sending IED is shown in Figure 6.29.

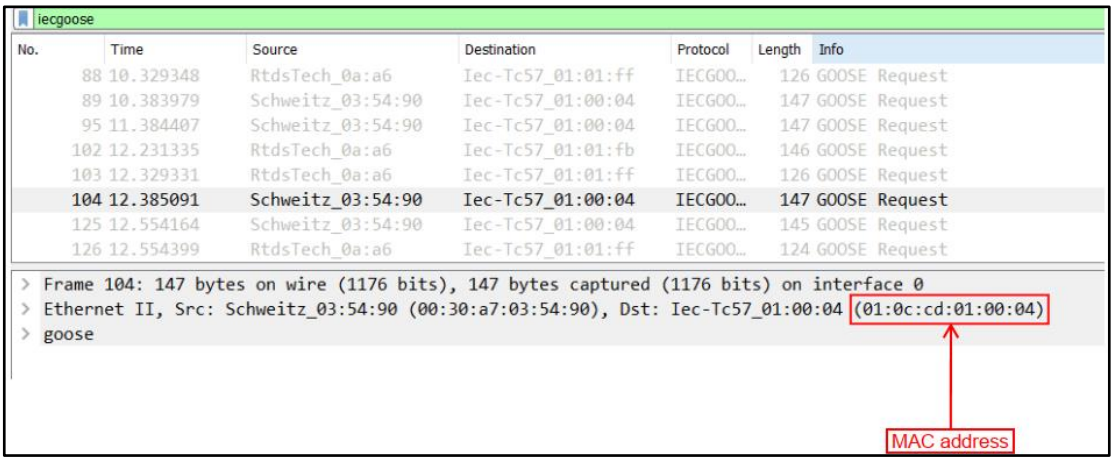

Figure 6.29: MAC address for IED

The GOOSE message published by relay 1 containing the data set "GOOSE_TRIP" is shown in Figures 6.21 and 6.22. Figure 6.30 shows the captured GOOSE message before the trip command is transmitted via the Ethernet. The packet number for the GOOSE message is 104, and the time stamp is 13:24:48,511690 (Hrs: min: sec). The initial state number is 1, and the state sequence is 331. The Boolean status is “False”.

Figure 6.31 shows the captured GOOSE message after the trip command is transmitted via the Ethernet. The packet number for the GOOSE message is 125, and

the time stamp is 13:24:48,681701(Hrs: min: sec). The state number changes to 2, and the state sequence resets to 0. The Boolean status changes to “True”.

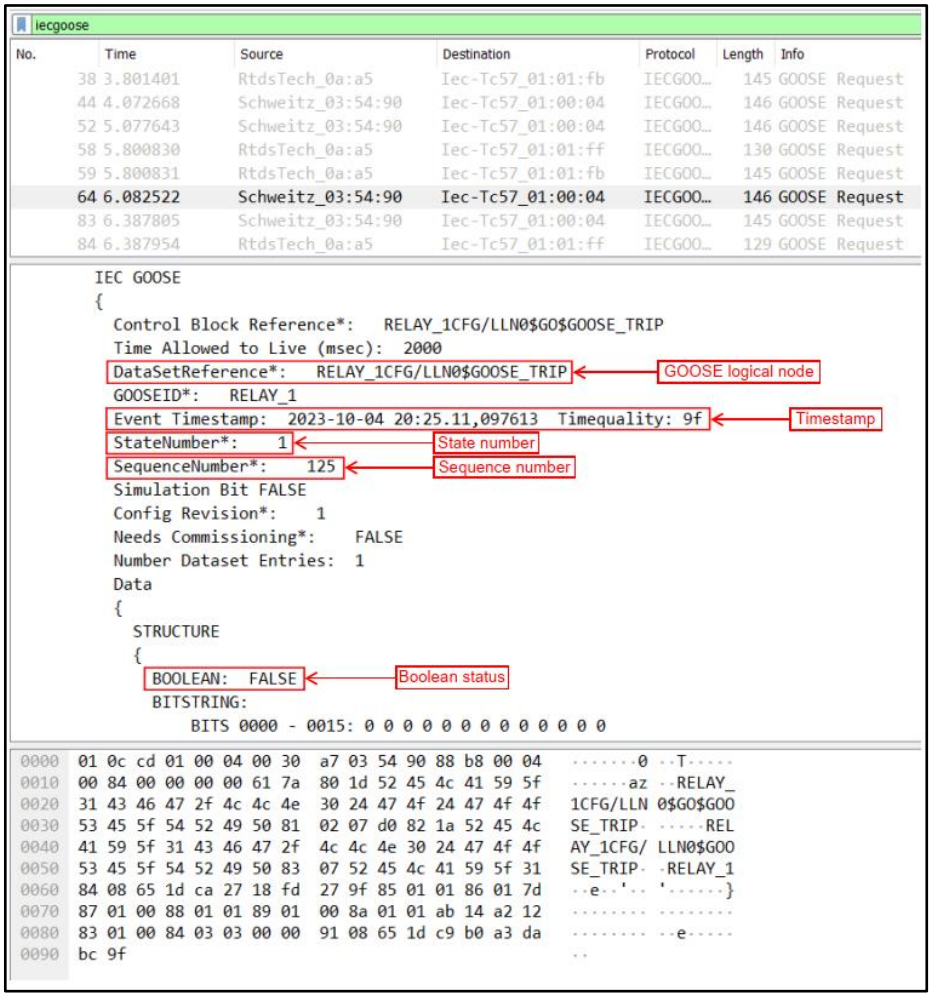

Figure 6.30: GOOSE message published by relay 1 captured with Wireshark

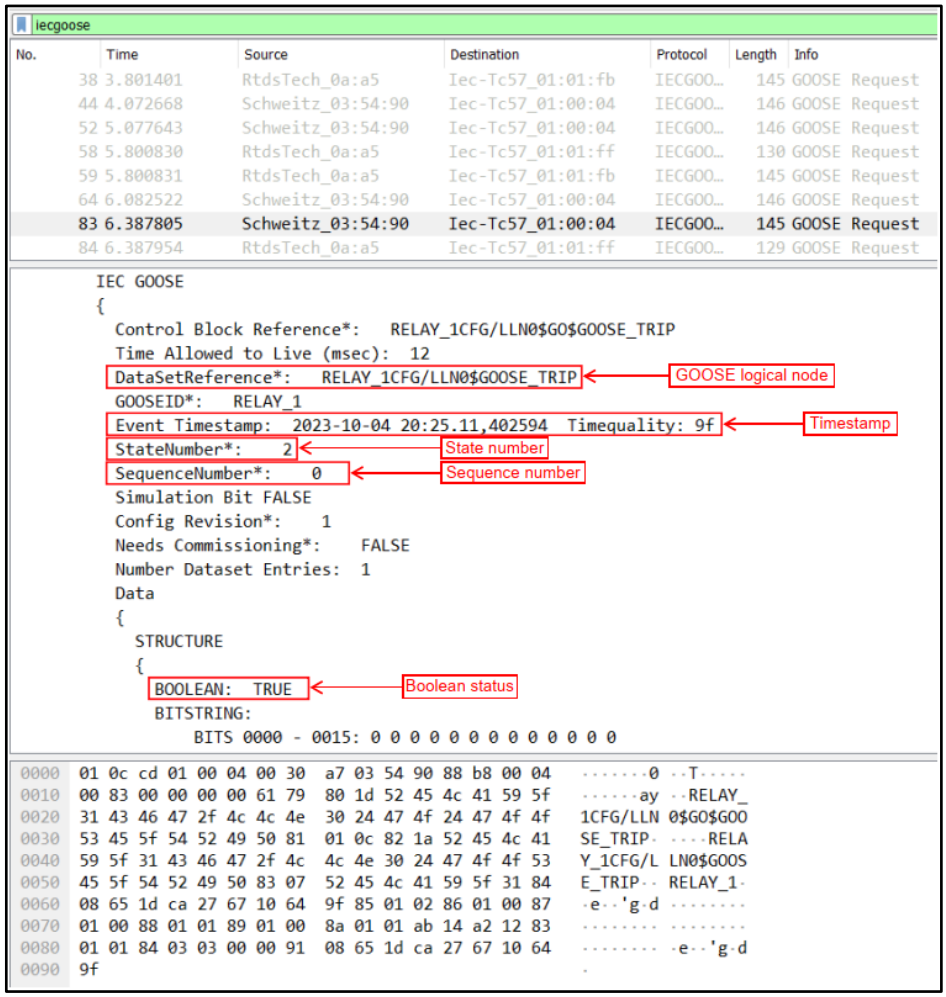

Figure 6.31: **Change in state of the GOOSE message published by relay 1 captured with Wireshark**

The tripping times for hardwired compared to the IEC 61850 GOOSE message for relay 14 are shown in Table 6.7. There are no tripping times for the backup relay R14 during the hardwired connection as shown in Table 6.7. This is because the primary relay R1 should be allowed to clear the fault within its primary protection zone and allow a coordination time before the backup relay operates.

Table 6.7: **Tripping times for hardwired compared to the IEC 61850 GOOSE for relay 14**

Type of fault	Tripping times for hardwired connection (ms)	Tripping times for IEC 61850 GOOSE message (ms)
Three-phase during grid-connected mode	No trip	65
Single-phase-to-ground during grid-connected mode	No trip	55
Three-phase during islanded mode	No trip	60

6.5 Conclusion

This chapter focuses on the implementation of GOOSE communication between the IEDs. The lab-scale test bench setup consists of the RTDS and SEL-351A relays. The GTNETx2 card allows for a connection between the RTDS and the SEL-351A relays over the Ethernet network. In RSCAD, the GTNET-GSE component is set up to subscribe to the GOOSE message that is published by the primary relay (relay 1). The GOOSE message contains the TRIPPTRC LN. The backup relay (relay 14) sends a trip signal back to the RTDS to open the circuit breaker in RSCAD when it subscribes to the GOOSE message published by relay 1.

The next chapter focuses on the implementation of the adaptive protection scheme. This allows for the settings group of the relays to change when there is a change in the network topology.

CHAPTER 7
IMPLEMENTATION OF THE ADAPTIVE PROTECTION SCHEME FOR THE MICROGRID SYSTEM

7.1 Introduction

The introduction of DGs into MGs results in a dynamic fault current magnitude, which is influenced by the network topology and the number of DGs connected at the time of the fault event. Traditional protection schemes are inadequate because of the dynamic nature of fault current, sympathetic tripping, and blinding protection. The implementation of adaptive protection enables the protection scheme to address these dynamic changes in the microgrid by dynamically adjusting the relay settings based on the microgrid configuration. (Kannaian et al., 2023).

Implementing an adaptive protection scheme offers the advantage of enabling two settings groups for the protection relays to detect and isolate fault currents in both grid-connected and islanded operation modes. Notably, the magnitude of the fault current during the islanded mode is generally lower due to the absence of the grid, which could lead to the blinding of the overcurrent relays. The adaptive protection scheme can be implemented using either a centralised or decentralised communication architecture within the microgrid, utilising the IEC 61850 communication protocol, which supports GOOSE and sampled values (SVs) transmitted over an Ethernet network. (Memon & Kauhaniemi, 2021).

This chapter aims to develop and implement an adaptive protection scheme for the MG system in real-time. This chapter is divided into two sections: Section 7.2 focuses on the configuration and modelling of the adaptive protection scheme for SEL-351A relays using a hardwired connection, and Section 7.3 focuses on the configuration and modelling of the adaptive protection scheme for the SEL-700G relay achieved through the IEC 61850 GOOSE communication protocol.

7.2 Implementation of the hardware-in-the-loop adaptive protection scheme

The adaptive protection scheme is based on the hardwired connection between the RTDS and SEL-351A protection relays. The setting group for the SEL-351A relays is configured using AcSELerator Quickset. The circuit breaker control logic is developed in RSCAD. Finally, the adaptive protection scheme is tested during HIL simulations.

During the RSCAD runtime, the circuit breakers BRK3 and BRK4 at the PCC are closed for grid-connected mode and opened for islanded mode, as shown in Figure 7.1. Relay R1 and R14 are configured to change from one setting group to another, depending on the network configuration.

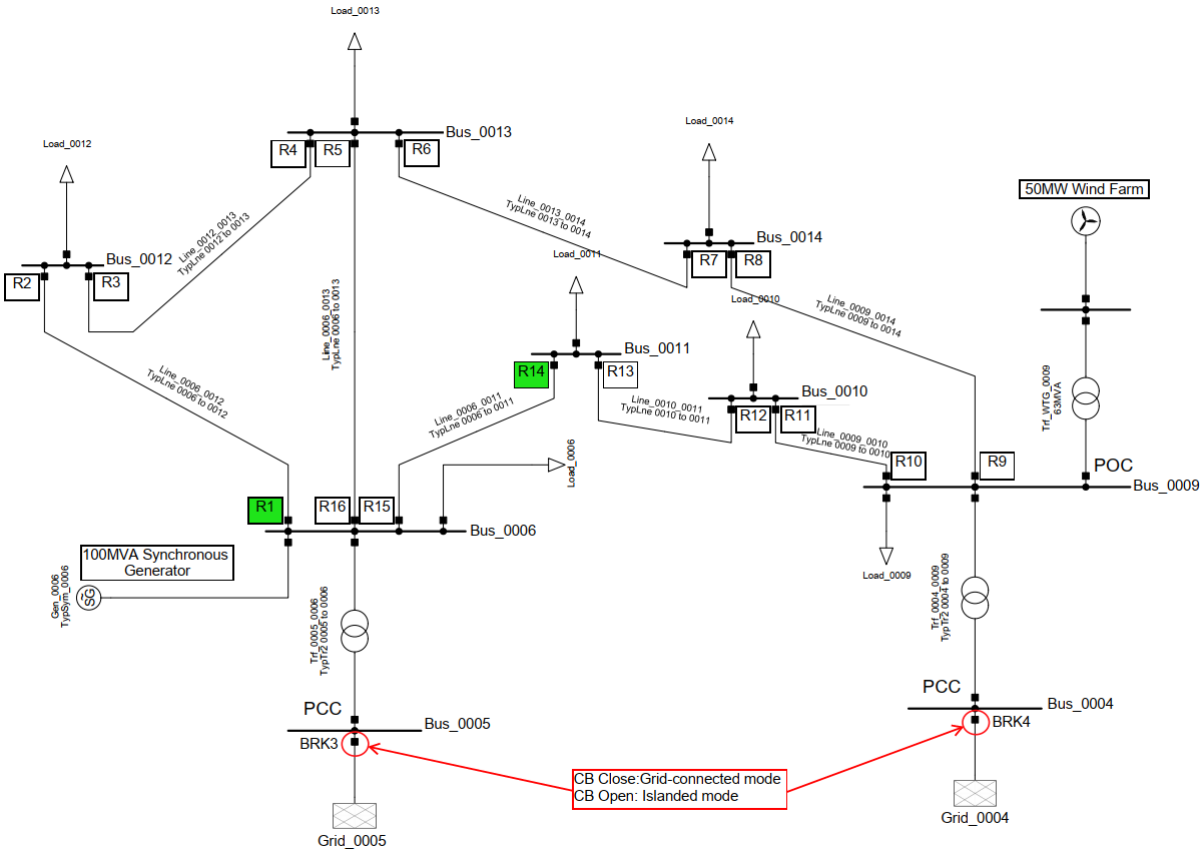

Figure 7.1: **Modified IEEE 14-bus system showing the circuit breakers at the PCC**

Figure 7.2 shows the laboratory-scale test bench for the adaptive protection scheme based on a hardwired connection. The output from the RTDS HV panel is connected to the opto-isolated input (IN101) of the SEL-351A relay, and the Omicron CMC 356 test set is used to supply the 110 V DC needed by the relay to indicate the status of the circuit breaker.

The flow diagram for the developed adaptive protection algorithm is shown in Figure 7.3. The position of the circuit breakers at the PCC is used to determine whether the MG is operating in grid-connected or islanded mode. Setting group 1 (SG1) is configured for the grid-connected mode, and setting group 2 (SG2) is configured for the islanded mode.

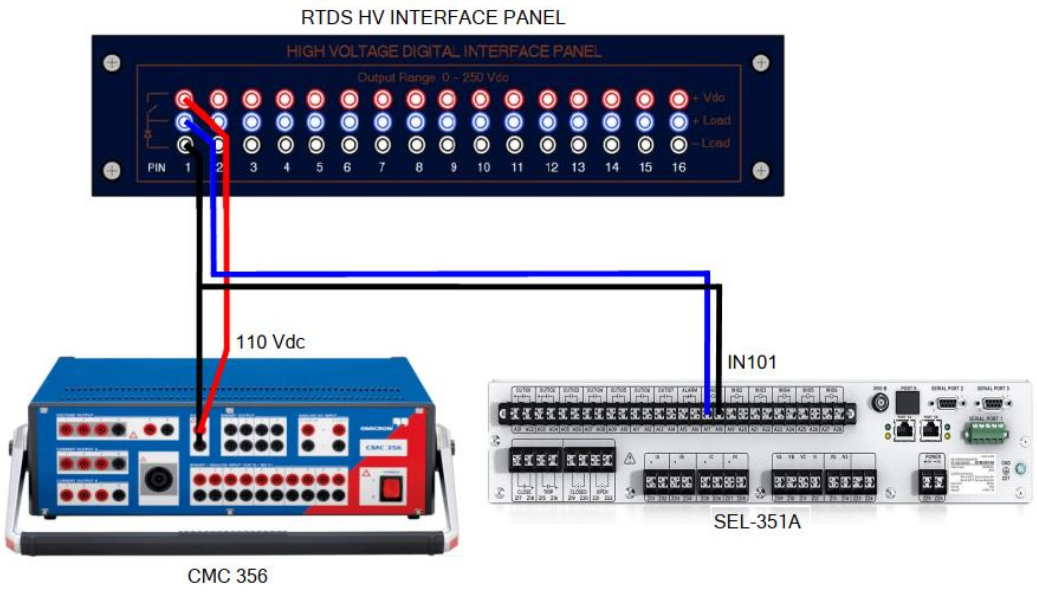

Figure 7.2: HV panel connection for breaker status signals using an external power supply

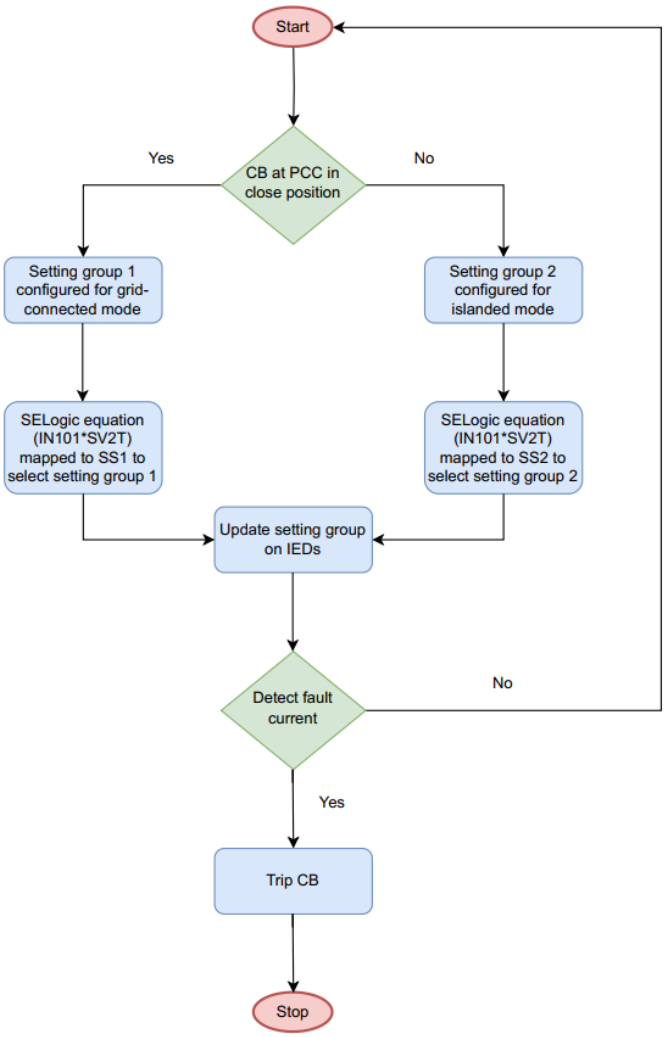

Figure 7.3: Flow diagram of the developed adaptive protection algorithm

7.2.1 Configuration of the SEL-351A relays to change the group settings using AcSELerator Quickset

The SEL-351A relay has six independent setting groups. Each setting group has overcurrent and SELOGIC control equation settings. Only one setting group can be active at a time. Relay Word Bits SG1–SG6 indicate the active setting group. The relay is disabled while changing the setting group. The output contact does not change state until the relay enables the new settings group (SEL-351A manual, 2022). Each pulse from the RTDS HV panel changes the setting group. The SELOGIC variable (SV2) timer pickup is set to 7.5 cycles (150 ms), and the SV2 timer dropout is set to 0 cycles, as shown in Figure 7.4. The SV2PU time delay is set to be longer than the pulse width of the output contacts from the RTDS. The SV2 SELOGIC control equation is set to SG1 for group 1 logic and SG2 for group 2 logic.

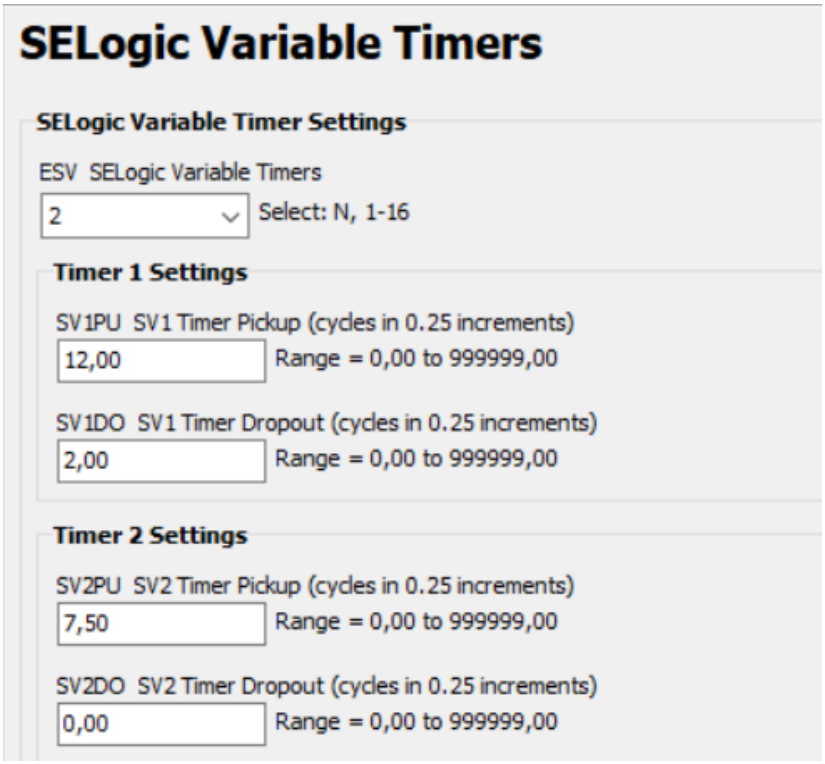

Figure 7.4: SELogic variable timer settings

The TRIP Relay Word Bit is assigned to the SV1 timer for the breaker failure scheme. The timer pickup setting SV1PU is set to the breaker failure time (12 cycles, or 240 ms). The timer dropout setting is set to 2 cycles (40 ms). The output of the timer (SV1T) operates an output contact, e.g. OUT103.

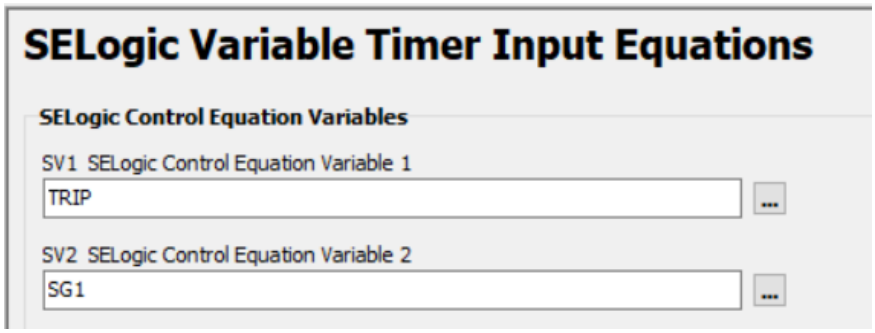

Figure 7.5: SELogic variable timer input equations

The SEL$_{OGIC}$ control equation timer SV2 has a logic output, SV2T. The SV2T timer is used for both setting groups. Relay starts by setting group 1. When the timer logic output, SV2T, is asserted, it enables the SEL$_{OGIC}$ control equation to be set to SS2 when the input, IN101, is asserted. When the output contacts from the RTDS pulse input IN101, the active setting group changes to group 2. When the relay is in group 2 and the timer logic output, SV2T, is asserted, the SEL$_{OGIC}$ control equation is set to SS1 when the input, IN101, is asserted. When the output contacts from the RTDS pulse input IN101, the active setting group changes to group 1. Figures 7.6 and 7.7 depict the SEL$_{OGIC}$ control equations for SS2 and SS1, respectively.

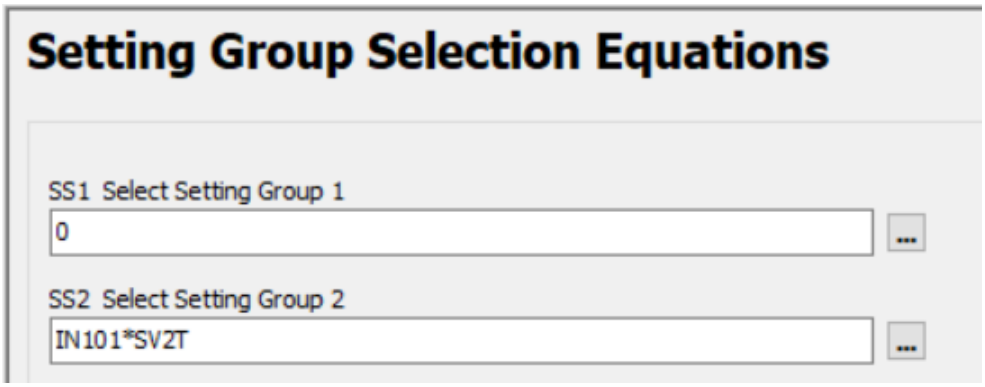

Figure 7.6: Setting group selection equation for logic group 1

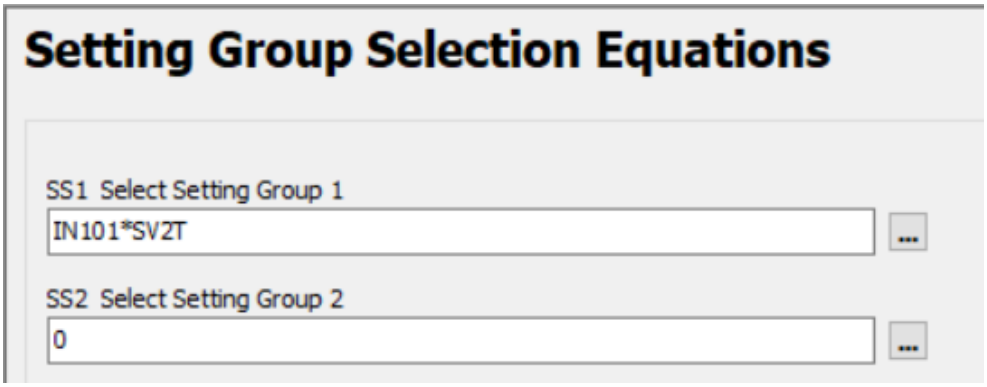

Figure 7.7: Setting group selection equation for logic group 2

The logic diagrams for selecting setting groups 1 and 2 are shown in Figures 7.8 and 7.9, respectively.

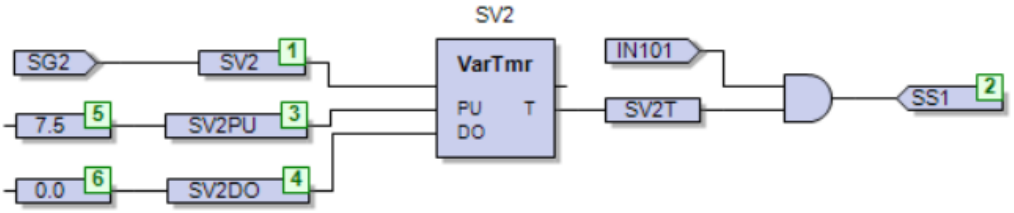

Figure 7.8: Logic diagram for setting group 1

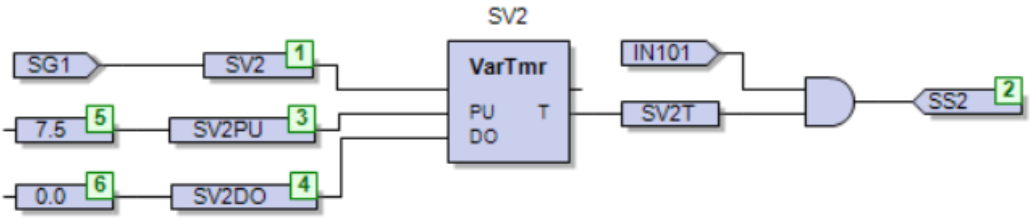

Figure 7.9: Logic diagram for setting group 2

7.2.2 Configuration of the RSCAD

The control logic for the circuit breaker status from BRK3 and BRK4 is shown in Figure 7.10. The circuit breaker status signals, BRK3ST and BRK4ST, are connected to an AND gate. These signals are also connected to an OR gate, followed by another AND gate. The output from the AND gate changes from logical 0 to logical 1 when the state of the signals BRK3 and BRK4 changes to either logical 0 or logical 1. The output from the AND gate is then connected to a bit-to-word converter that converts the binary output to an integer word. The outputs from the bit-to-word converters are linked to a timer set at 0.1 s. This causes the output from the bit-to-word converter to pulse for a duration of 0.1 s. Finally, the output from the timer is connected to the GTFPI card, which must be configured as shown in Figure 7.11 and include the HV panel signals.

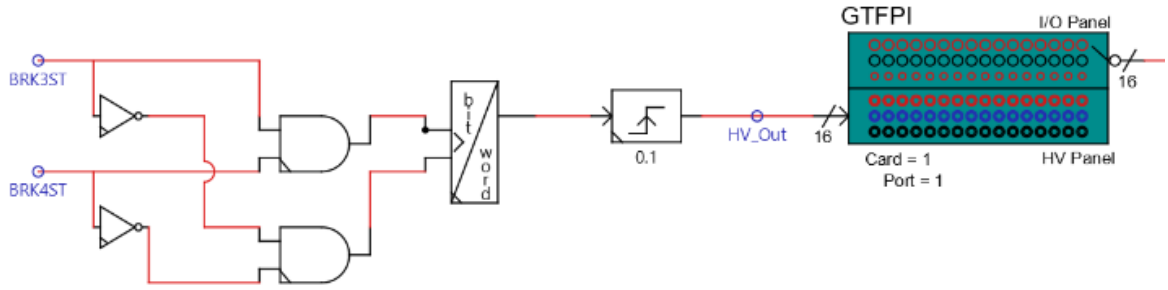

Figure 7.10: Logic for circuit breaker status in RSCAD

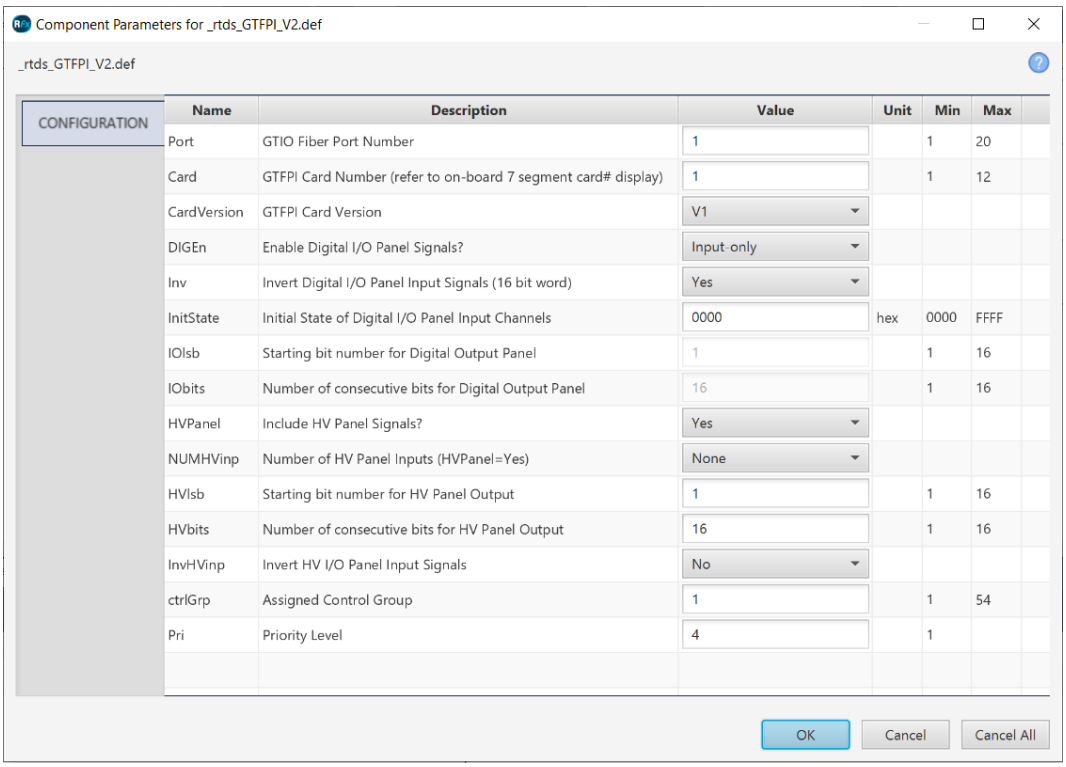

Figure 7.11: Configuration of GTFPI

7.2.3 Hardware-in-the-loop testing of the adaptive protection scheme

The circuit breakers BRK3 and BRK4 at the PCC are closed during grid-connected mode and open during islanded mode. The relay settings are changed from one setting group to another depending on the status of the circuit breakers. The pushbuttons BRK34Op and BRK34Cls are used to open and close BRK3 and BRK4 simultaneously during the runtime, as shown in Figure 7.12.

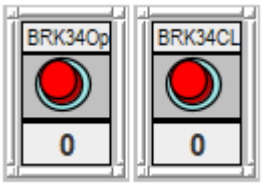

Figure 7.12: Pushbuttons used to open and close circuit breakers during runtime

Figure 7.13 shows the position of the circuit breakers BRK3 and BRK4 during the runtime. A decimal value of 1 represents the close position, while a decimal value of 0 indicates the open position. Initially, during the start of the runtime simulation, circuit breakers BRK3 and BRK4 are in a close position, with the circuit breaker position indicating a decimal value of 1. The measured currents through BRK3 and BRK4 under steady-state conditions are shown in Figure 7.14.

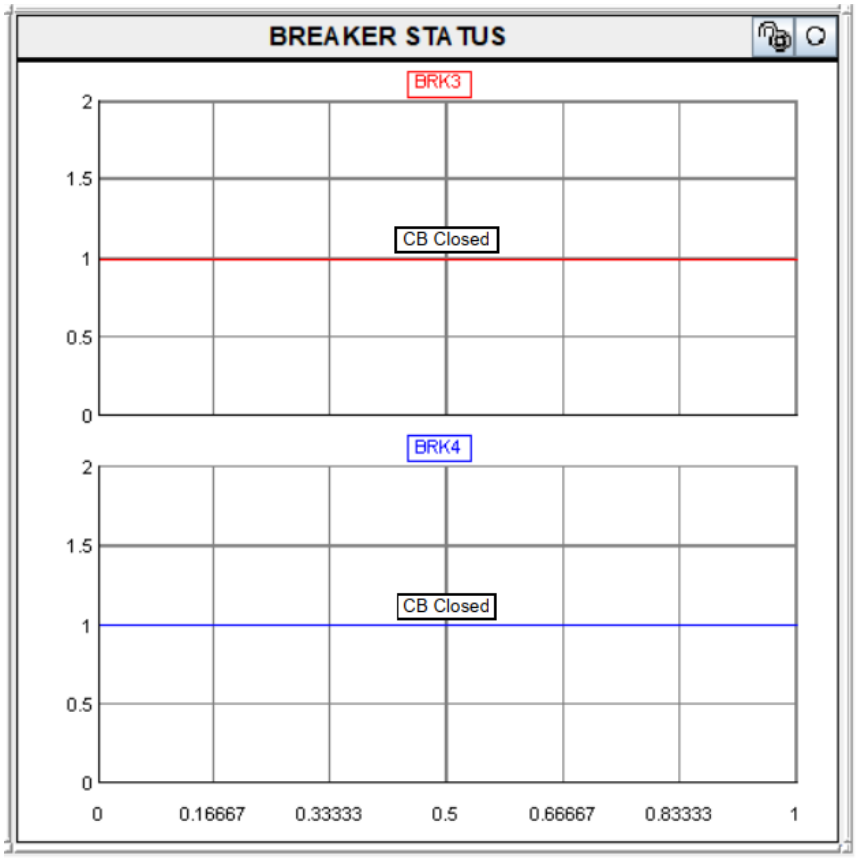

Figure 7.13: Circuit breakers BRK3 and BRK4 in the close position

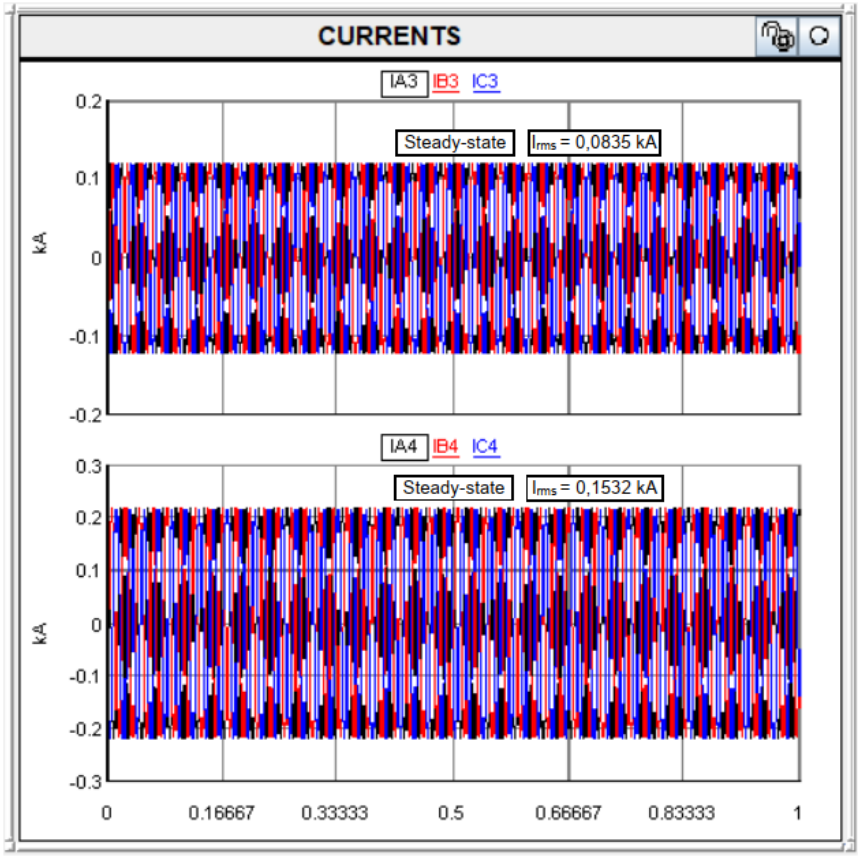

Figure 7.14: Measured currents through circuit breakers BRK3 and BRK4 during grid-connected mode

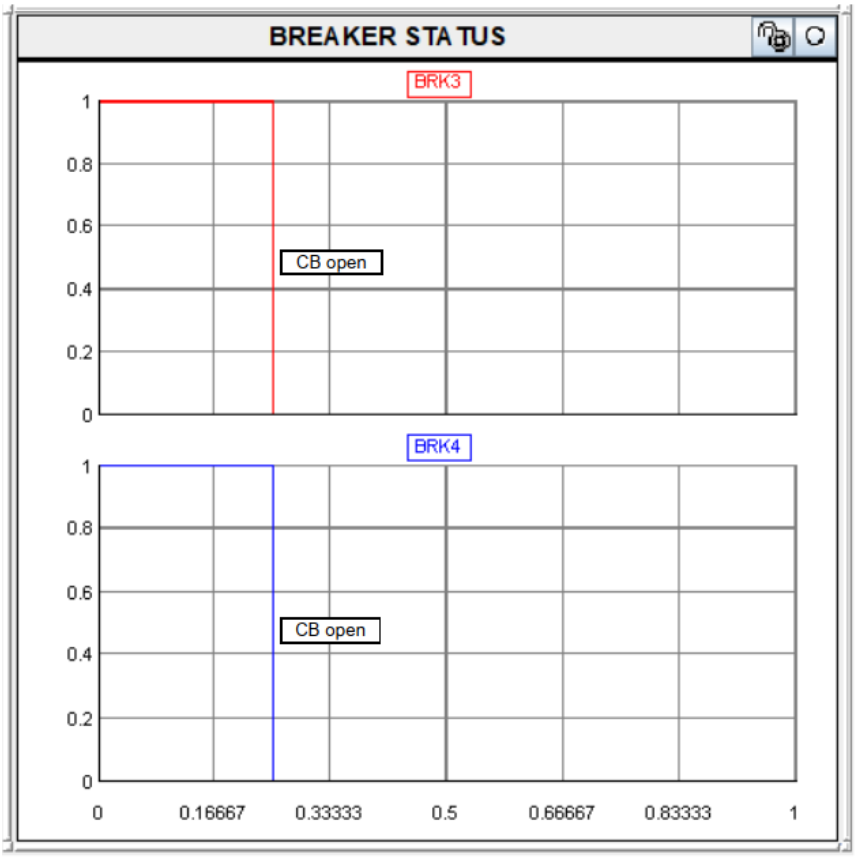

Figure 7.15: Circuit breakers BRK3 and BRK4 in the open position

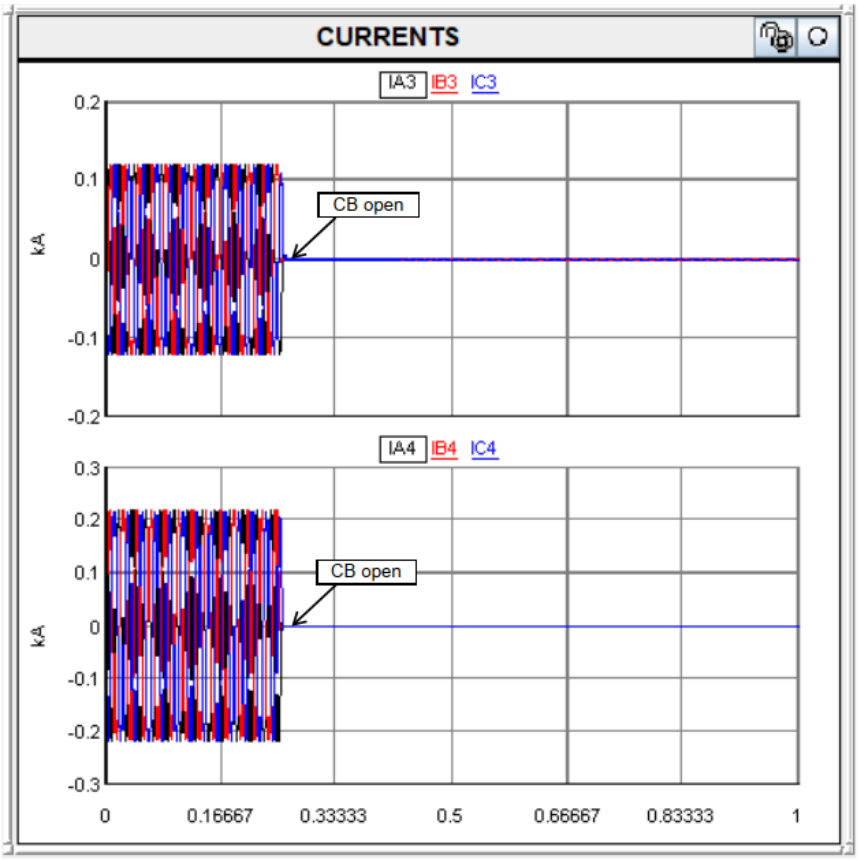

Figure 7.16: Measured currents through circuit breakers BRK3 and BRK4 during grid-connected mode

The circuit breakers BRK3 and BRK4 change from the close to open position after pressing the pushbutton, BRK34Op, and the circuit breaker status changes from a decimal value of 1 to 0, as shown in Figure 7.15. The measured currents through circuit breakers BRK3 and BRK4 decrease to 0 A once the circuit breakers are opened, as shown in Figure 7.16.

The HMI in AcSELerator Quickset can be used to confirm the setting group of the relay. When the circuit breakers BRK3 and BRK4 are in close positions, the relay is set to setting group 1, as shown in Figure 7.1. After applying the pushbutton BRK34Op, the circuit breaker changes to the open position, and the relay settings change from setting group 1 to setting group 2, as shown in Figure 7.18. When the pushbuttons BRK34Op and BRK34Cls are pressed during the runtime to open or close the circuit breakers, the solid-state switch on the HV panel is used to switch an external power supply that is needed by the SEL-351A relay to indicate the breaker status. The 110 V DC supply voltage is connected to the optoisolated input, IN101, on the SEL-351A relay. The SER for relay 1 can also be used to confirm the setting group change, as shown in Figure 7.19. The data from the SER indicates that the IN101 is asserted at 202 ms, and the relay settings are changed from setting group 1 to setting group 2 at 398 ms.

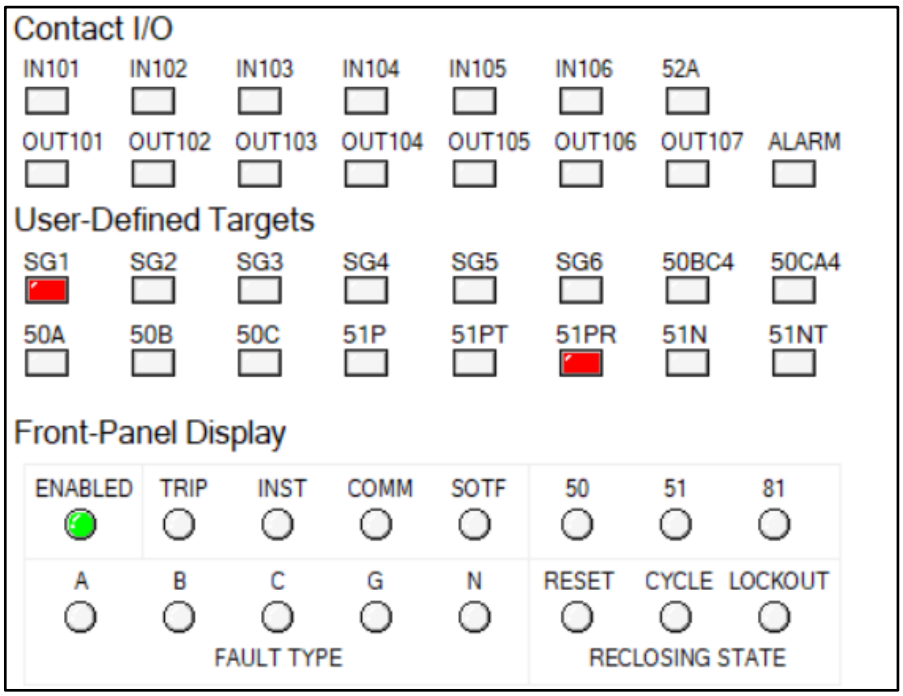

Figure 7.17: Relay HMI showing setting group 1 selected

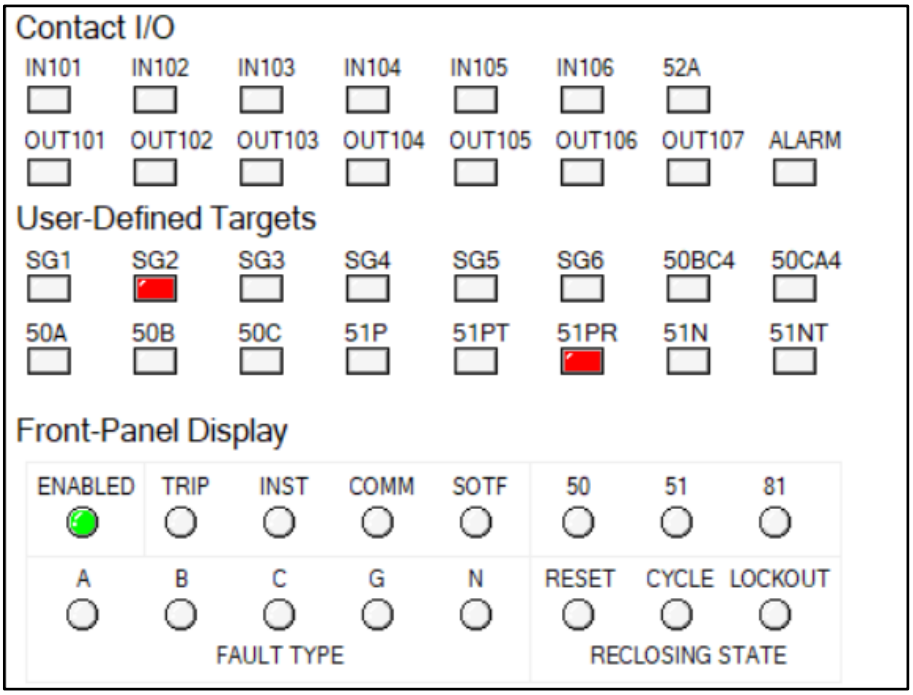

Figure 7.18: Relay HMI showing setting group 2 selected

#	DATE	TIME	ELEMENT	STATE
2	07/13/23	15:44:26.202	IN101	Asserted
1	07/13/23	15:44:26.398	Relay settings changed	

Figure 7.19: SER for relay 1 to confirm setting group change

7.3 Implementation of the IEC 61850 standard-based adaptive protection scheme

The functionality and reliability of the IEC 61850 standard-based adaptive protection scheme are verified in real-time during the HIL testing of the relays. The active setting group is determined by the circuit breaker status during grid-connected and islanded modes. The developed adaptive protection algorithm based on the IEC 61850 GOOSE communication between the IEDs is shown in Figure 7.20. The position of the circuit breakers at the PCC is used to determine whether the MG is operating in grid-connected or islanded mode. Setting group 1 (SG1) is configured for the grid-connected mode, and setting group 2 (SG2) is configured for the islanded mode.

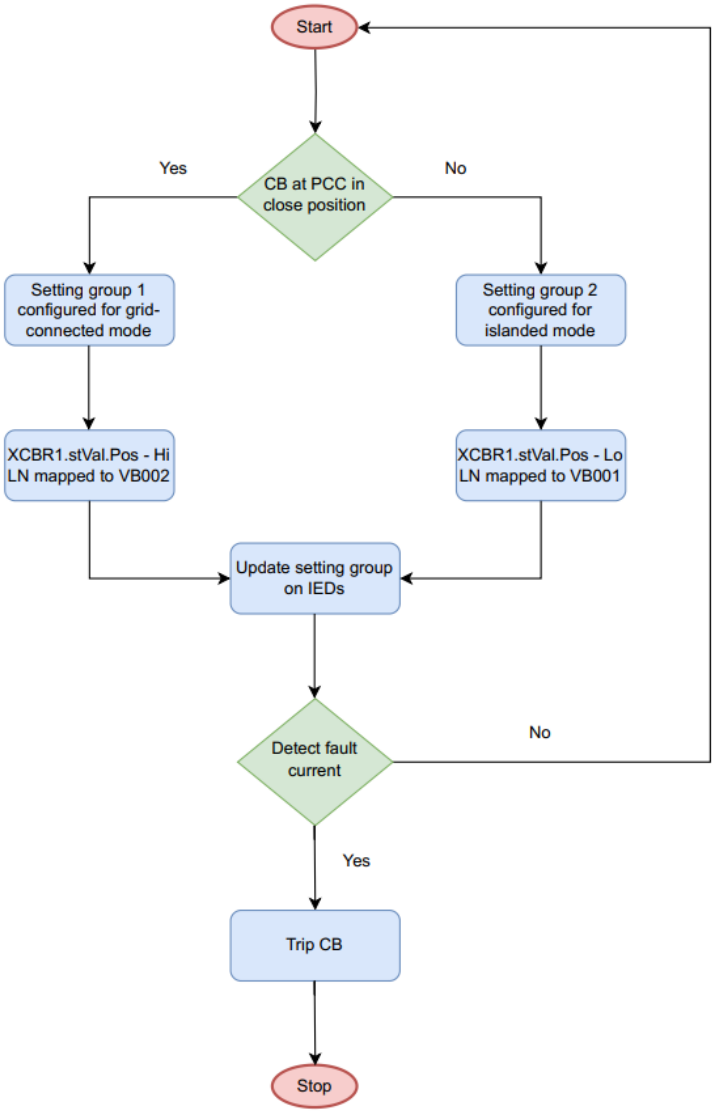

Figure 7.20: **Flow diagram of the developed IEC 61850 standard-based adaptive protection algorithm**

The laboratory-scale test bench for the implementation of the adaptive protection scheme based on the IEC 61850 standard is shown in Figure 7.21. The XCBR1 LN is configured in the GTNET-GSE component based on the status of the circuit breaker, BRK3, at the PCC, as shown in Figure 7.1. The IEC 61850 GOOSE message containing the XCBR1 LN is transmitted via Ethernet. The SEL-700G IED is configured to change the settings group based on the status of the XCBR1 LN. During the grid-connected mode, the circuit breaker BRK3 is closed, and group 1 is selected. In the islanded mode, the circuit breaker BRK3 is open, and group 2 is selected.

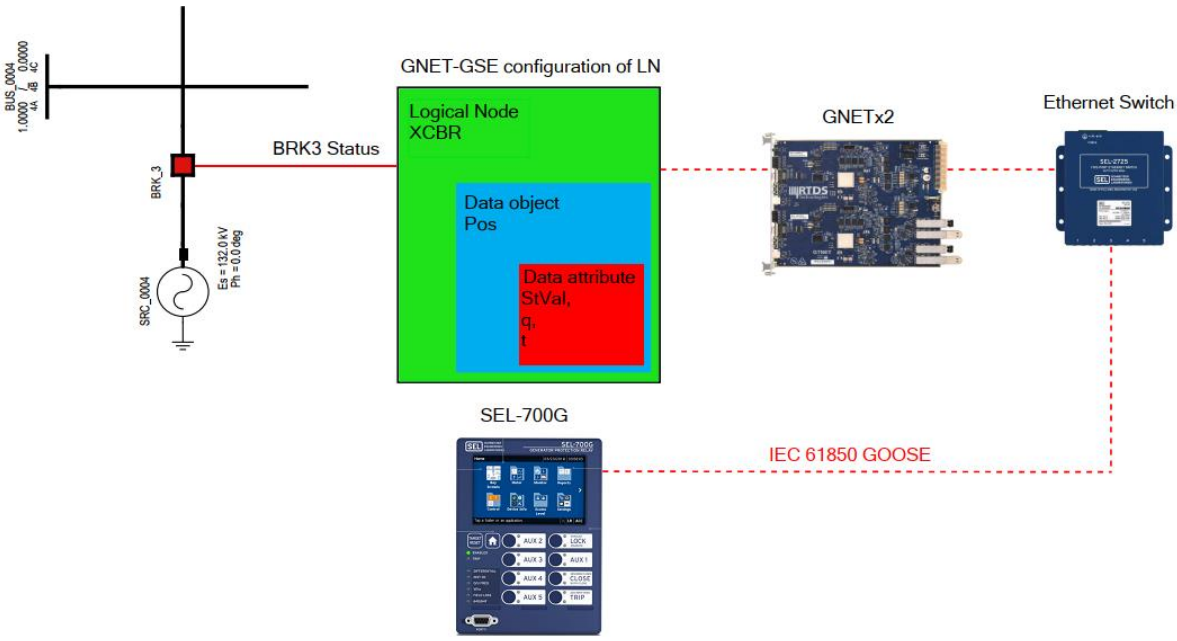

Figure 7.21: **Test bench for the adaptive protection scheme based on the IEC 61850 GOOSE communication**

The SEL-700GT IED is used for the implementation of the adaptive protection based on IEC 61850 GOOSE communication, as the SEL-351A IEDs do not support IEC 61850 Ed. 2 of the standard. The GTNET-GSE component and logic needed for adaptive protection are shown in Figure 7.22. The status signal BRK3STS is connected to the input of the word-to-bit converter, and BRK3Pos is at the output of the converter. The BRK3Pos signal is then connected to the input of a bit-to-word converter, with the PosA1 signal at the output of the converter. The PosA1 signal is the data object from the GTNET-GSE for the control of circuit breaker BRK3.

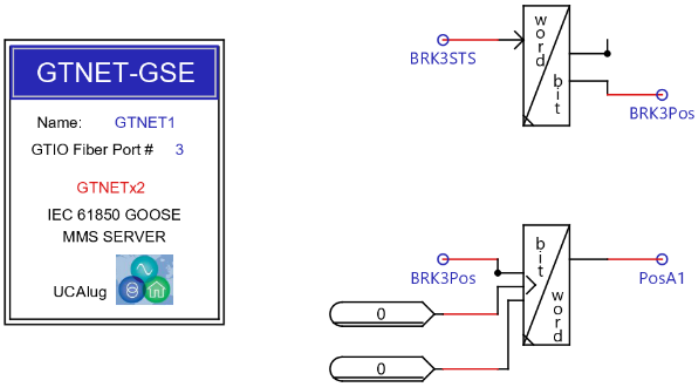

Figure 7.22: **Logic for circuit breaker status using GOOSE communication**

To configure the IEC 61850 GOOSE message that is published by the RTDS, right-click on the GTNET-GSE component and scroll down to the edit tap to access the IEC 61850 ICT Project, as shown in Figure 7.23. The IEC 61850 ICT is used to configure the GOOSE messages that are published by the RTDS or what the RTDS subscribes to from other IEDs connected to the LAN.

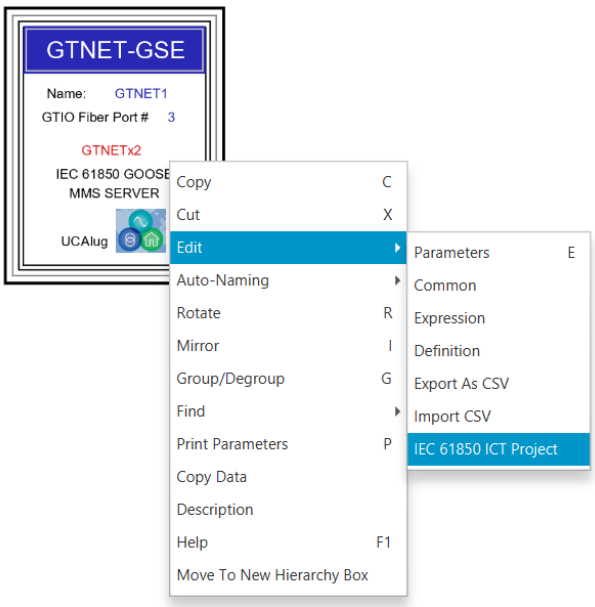

Figure 7.23: Access to the IEC 61850 ICT

The dataset XCBR_GSE_Position contains the logical device (LD) CSWI_XCBR, as shown in Figure 7.24. The LD contains the logical node (LN) Obj1XCBR1 (XCBR) with the data object (DO) for the position (named "Pos"). The DO "Pos" indicates the position of the circuit breaker. The common data class (CDC) describes the type and structure of the data within the LN. The CDC for the data object, Pos, is a double point controllable (DPC) type. The DO "Pos" contains the status value (stVal) and quality (q) data attributes (DAs) (IEC 61850-7-4, 2010). The hierarchical data model of the XCBR LN is shown in Figure 7.25.

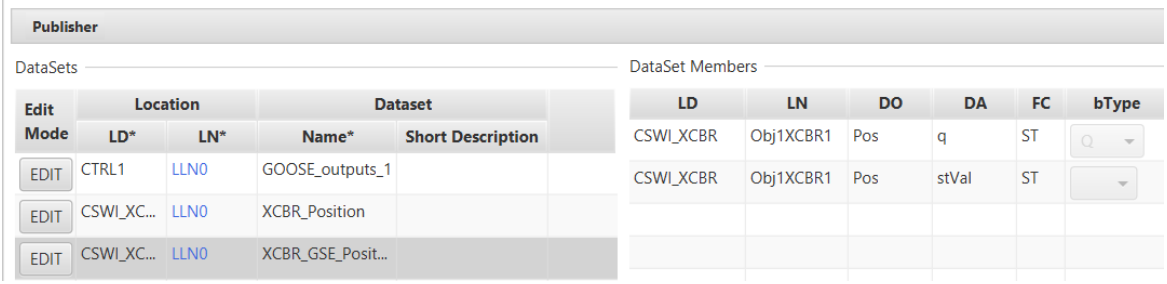

Figure 7.24: Configuration of the CSWI_XCBR dataset

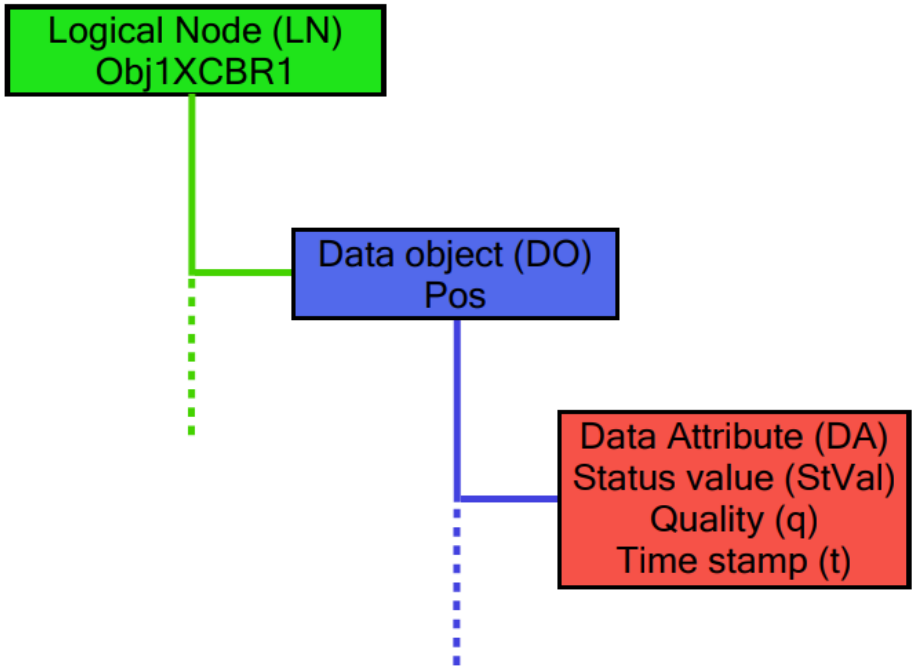

Figure 7.25: Hierarchical data model

The GOOSE receive message is configured in the AcSELerator Architect, as shown in Figure 7.26. The GOOSE message containing the CSWI_XCBR LD that is published by the RTDS is in the column on the left. The LD is mapped to VB001 and VB002 in the column on the right. VB001 indicates that the circuit breaker is in the open position (islanded mode). VB002 indicates that the circuit breaker is in the closed position (grid-connected mode). The FTP address is the IP address of the SEL-700G IED. The username is FTPUSER, and the password is TAIL. The CID file is ready to be sent to the IED, as shown in Figure 7.27.

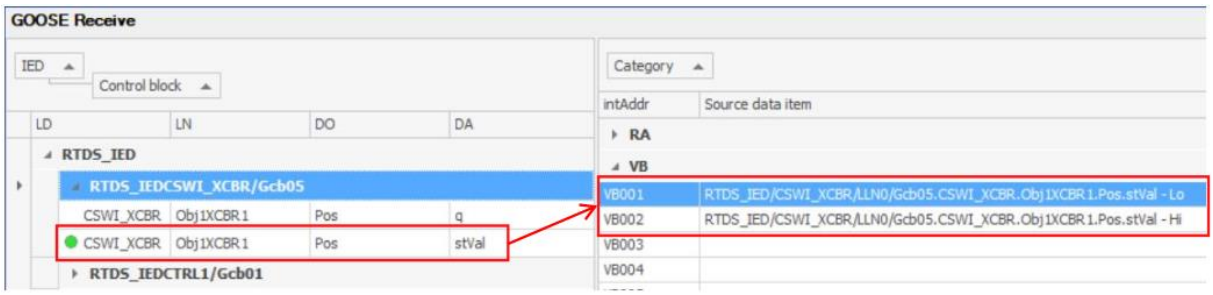

Figure 7.26: Configuration of the GOOSE receive

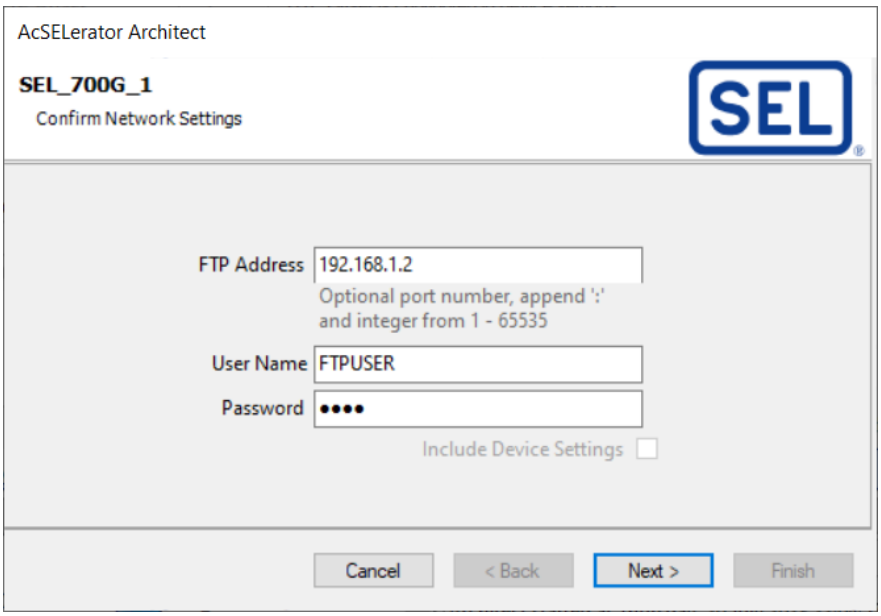

Figure 7.27: FTP address for sending the GOOSE configuration

The configuration of the SELogic control equation for setting group selection is shown in Figure 7.28. The SELogic equation for select settings group 1 (SS1) is VB002. The SELogic equation for select settings group 2 (SS2) is VB001. Group 1 is set for the grid-connected mode of operation, and Group 2 is set for the islanded mode of operation.

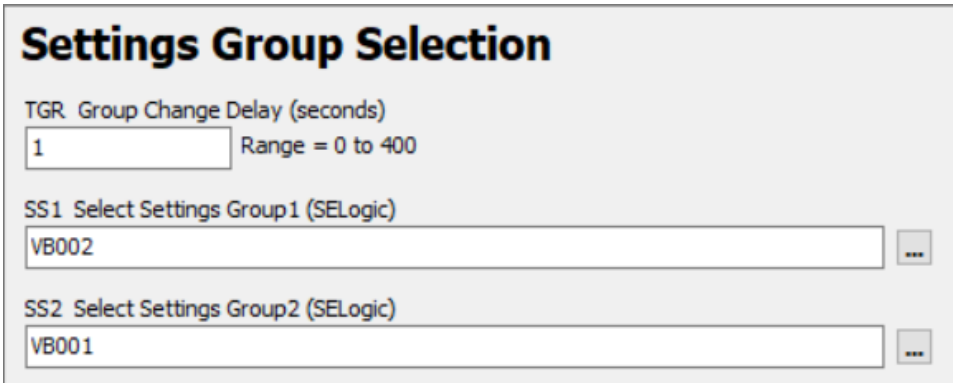

Figure 7.28: SELogic for setting group selection

7.4 Hardware-in-the-loop testing of the IEC 61850 standard-based adaptive protection scheme

The controls in the RSCAD runtime for testing the adaptive protection scheme are shown in Figure 7.29. The circuit breaker 3 status (BRK3) and circuit breaker 3 position (BRK3pos) are shown in Figures 7.30 and 7.31. Circuit breaker 3 is initially in the closed position, as shown in Figure 7.30. The BRK3 and BRK3pos signals are logical 1.

Pressing the BRK3Op push button changes the circuit breaker 3 status (BRK3) from a logical 1 to 0, while the circuit breaker position (BRK3Pos) changes from a logical 1 to 0, as shown in Figure 7.31.

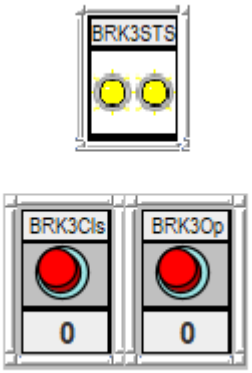

Figure 7.29: Push buttons in RSCAD runtime

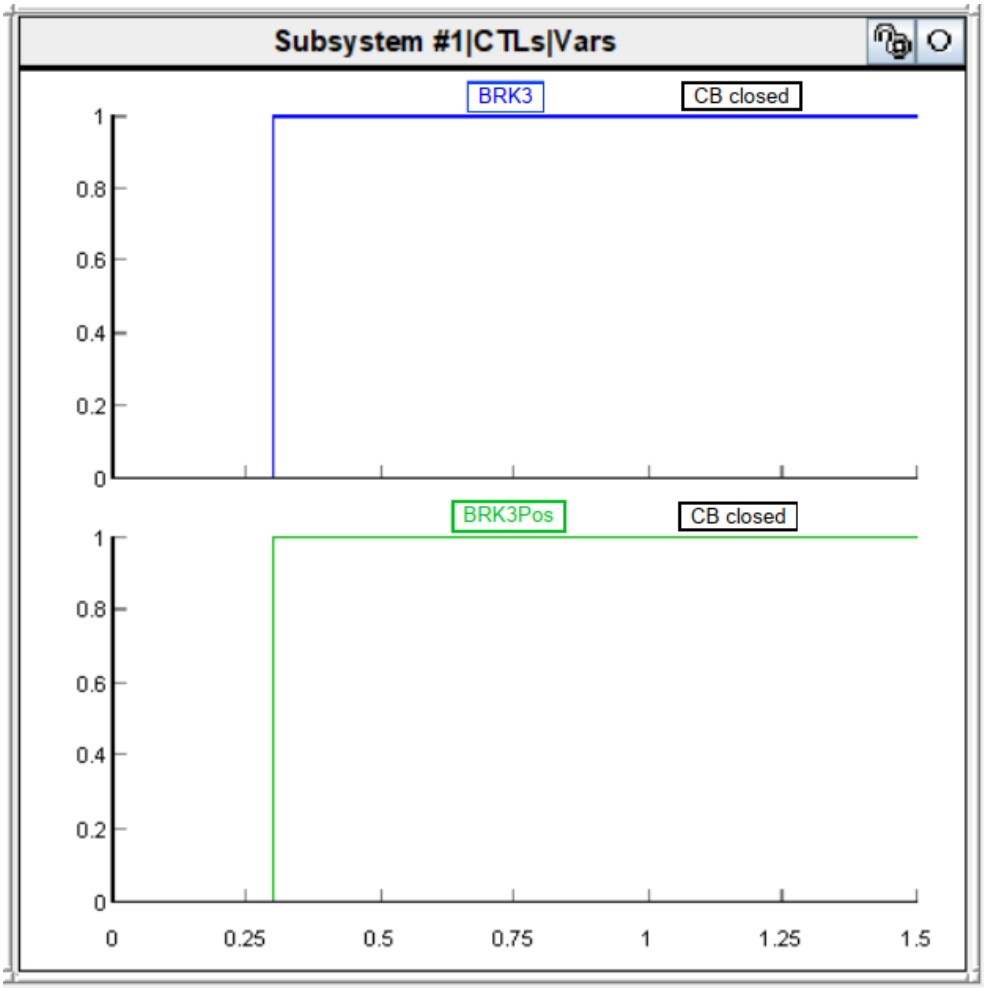

Figure 7.30: Circuit breaker BRK3 in the close position

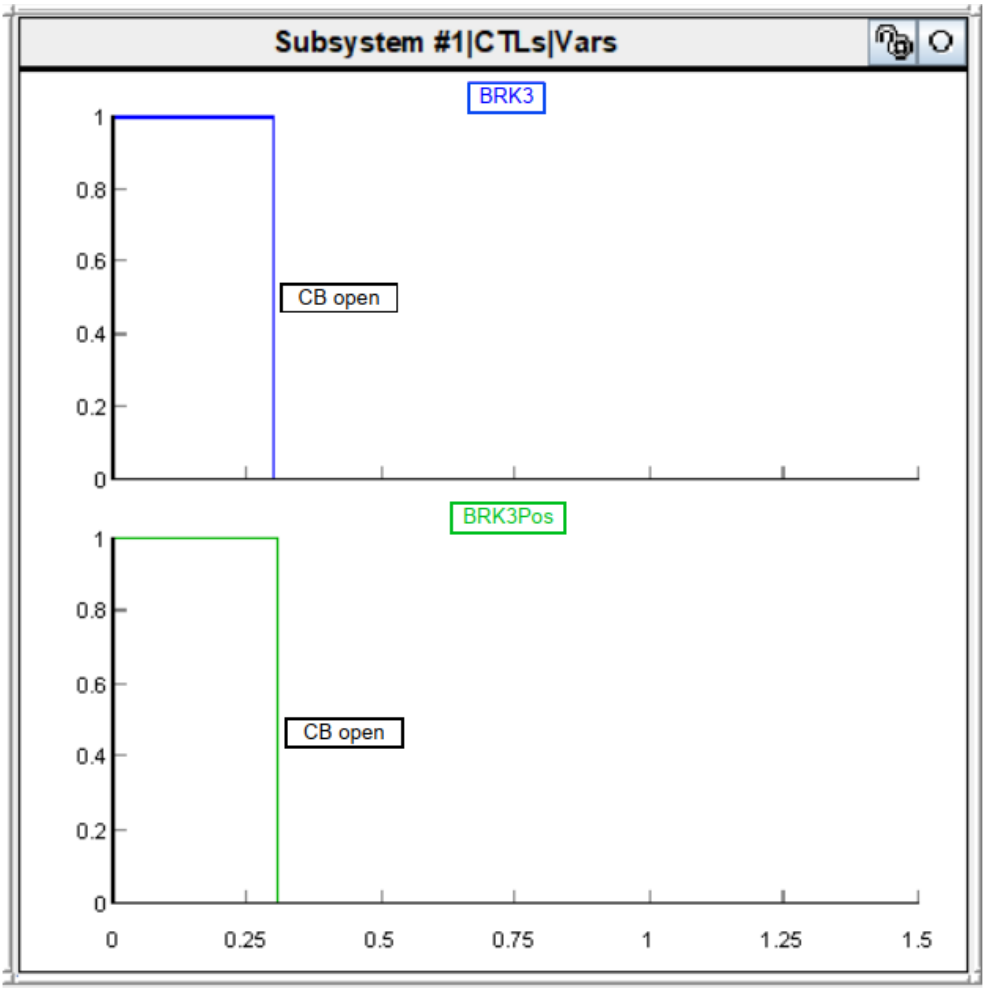

Figure 7.31: Circuit breaker BRK3 in the open position

From the sequential event reports (SER) in Figure 7.32, the following information is observed:

The relay group changed after pressing the pushbutton BRK3Op to open the circuit breaker BRK3 at a timestamp of 13:58:50.709. The relay group changed again after pressing the pushbutton BRK3Cls to close the circuit breaker BRK3 at a timestamp of 13:58:57.174.

Sequential Event Reports

SEL-700GT Date: 07/20/2023 Time: 13:59:56.195
INTERTIE RELAY Time Source: Internal

Serial No = 3191080066 FID = SEL-700G-R200-V0-Z006003-D20180629
CID = 59A0

#	DATE	TIME	ELEMENT	STATE
1	07/20/2023	13:58:58.141	SALARM	Deasserted
2	07/20/2023	13:58:57.174	SALARM	Asserted
3	07/20/2023	13:58:57.174	Relay Group Changed	
4	07/20/2023	13:58:51.676	SALARM	Deasserted
5	07/20/2023	13:58:50.709	SALARM	Asserted
6	07/20/2023	13:58:50.709	Relay Group Changed	

Figure 7.32: SER for setting group change

The GOOSE message published by the RTDS IED containing the dataset CSWI_XCBR is shown in Figures 7.33 and 7.34. Figure 7.33 shows the captured GOOSE message indicating that circuit breaker 3 is in the closed position. The packet number for the GOOSE message is 17, and the time stamp is 13:58:12,377603 (Hrs:min:sec). The initial state number is 2, and the state sequence is 29. The Boolean status is “False”.

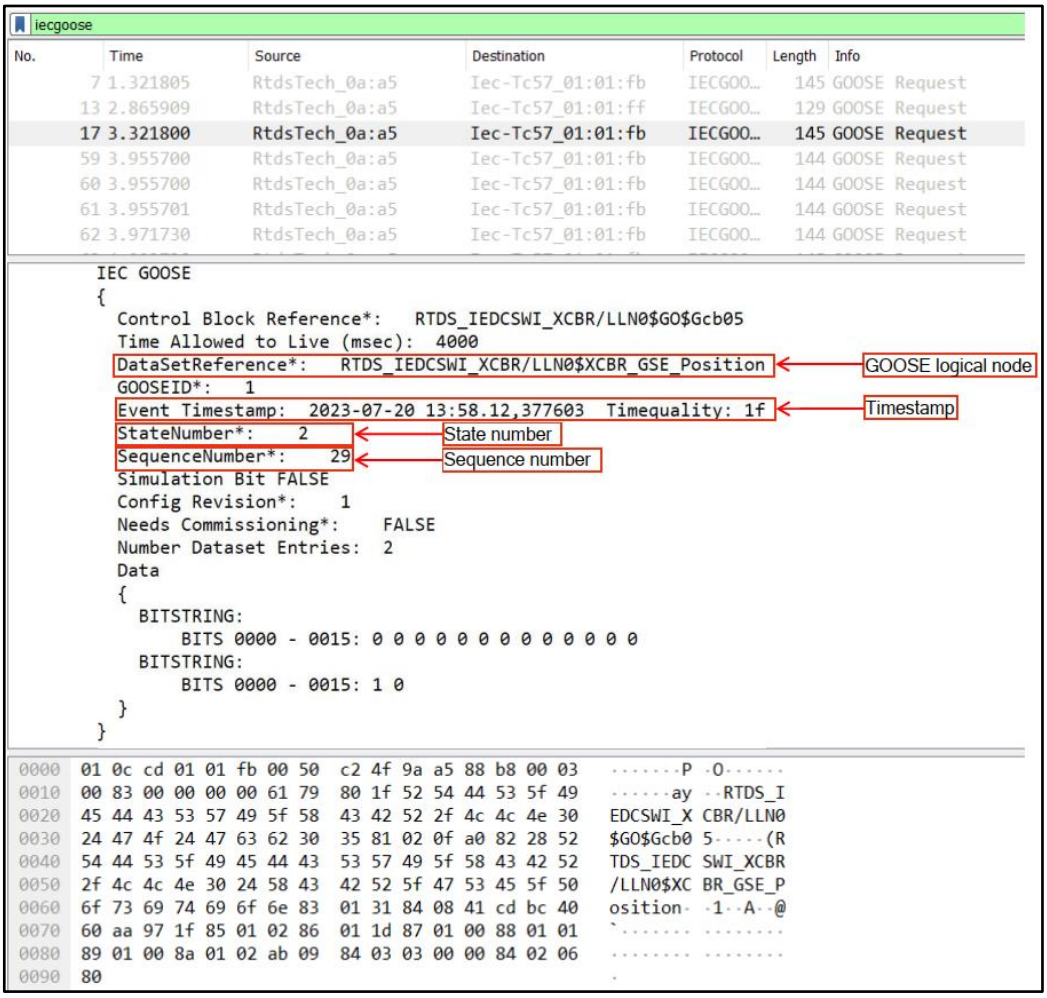

Figure 7.33: **GOOSE message published by RTDS indicating the XCBR status**

Figure 7.34 shows the captured GOOSE message, indicating that circuit breaker 3 changed to the close position. The packet number for the GOOSE message is 59, and the time stamp is 13:58:18,842192 (Hrs:min:sec). The initial state number is 3, and the state sequence is reset to 0. The change in the state number indicates that the Boolean status changed from “False” to “True”.

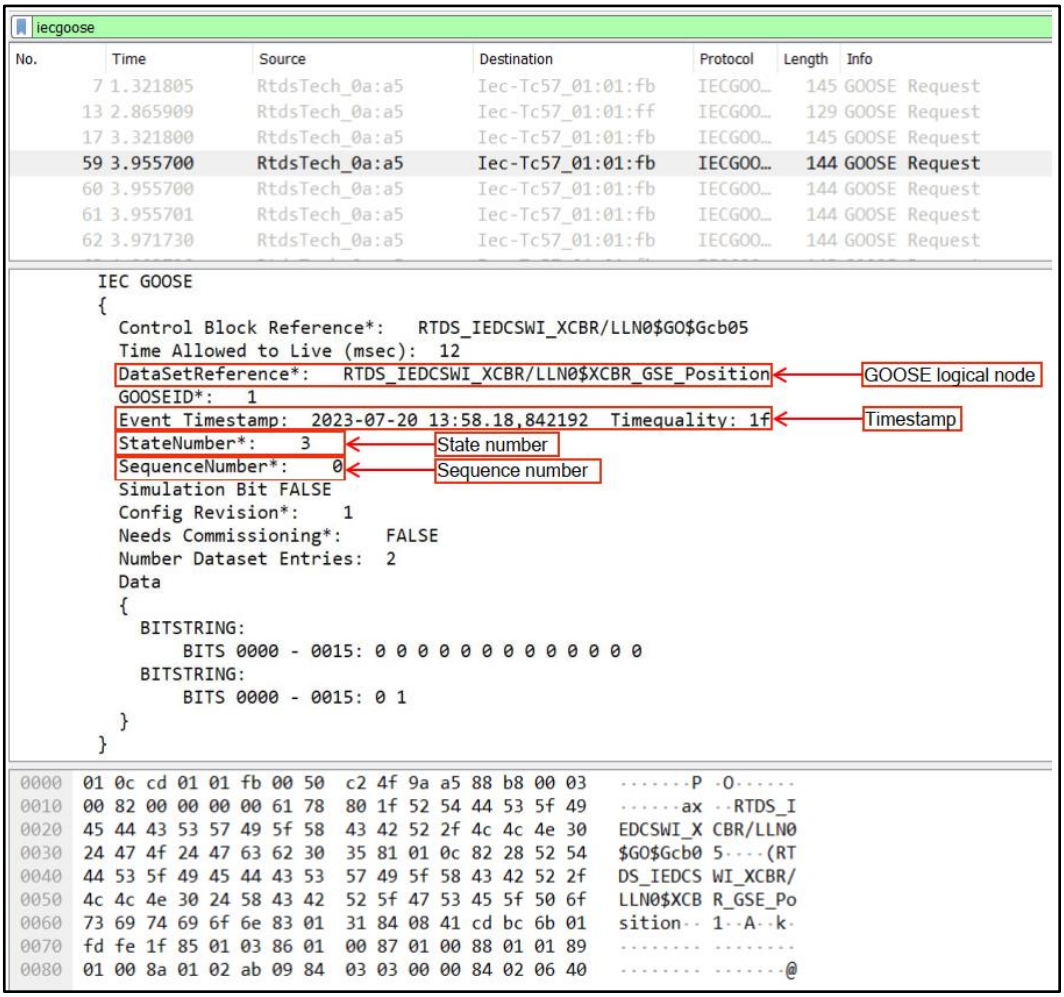

Figure 7.34: **Change in state of the GOOSE message published by RTDS indicating the XCBR status**

7.5 Conclusion

The developed adaptive protection algorithm was implemented, and HIL testing was conducted to validate the algorithm in a real-time simulation environment using RTDS and SEL protection relays in the CSAEMS laboratory at CPUT.

Hardwired connection between the RTDS and the SEL-351A IEDs was successfully implemented for the adaptive protection scheme. As a result, the setting group changed according to the position of the circuit breakers at the PCC. Similarly, adaptive protection for the SEL-700G IED based on the implementation of the IEC 61850 GOOSE communication allowed the setting group to change depending on the status of the XCBR logical node. The setting group is changed to SG1 during the grid-connected mode and to SG2 during the islanded mode.

The next chapter gives the conclusion for the entire scope of the thesis and discusses possible future research.

CHAPTER 8
CONCLUSION

8.1 Introduction

The integration of distributed generation (DG) into the microgrid (MG) system can have a negative impact on the overcurrent relay performance. The MG operates in both grid-connected and islanded modes, and the fault currents measured in the islanded mode are lower than those measured in the grid-connected mode. This may result in a loss of coordination between the overcurrent relays.

The aim of this research project is to develop and implement an adaptive protection scheme for the MG system to overcome the challenges associated with traditional protection schemes. The modified IEEE 14-bus system with an additional DG was used as a case study. The MG system was modelled and simulated in the DIgSILENT and RSCAD simulation environments. A hardware-in-the-loop (HIL) simulation was executed to validate the performance of the directional overcurrent relays during grid-connected and islanded modes for a fault event. The developed IEC 61850 GOOSE message was also implemented and tested during the HIL simulation by interfacing the external IEDs with a real-time digital simulator (RTDS).

This chapter summarises the research results and deliverables, which are presented in Section 8.2. Section 8.3 discusses the application of this research in academia and industry, and Section 8.4 provides recommendations for future research on adaptive protection schemes for MG systems.

8.2 Thesis deliverables

The IEC 61850 standard-based adaptive protection scheme was developed and implemented in real-time. The status of the circuit breakers' position (XCBR) was mapped to the virtual bits VB001 and VB002 on the SEL-700G IED. The settings group (SG) was updated to SG1 for grid-connected and SG2 for islanded modes.

The detailed thesis deliverables are given in sections 8.2.1 to 8.2.6 as follows:

8.2.1 Literature review

The literature review presented in Chapter 2 provides details on the protection and control measures in MG systems. A review has been conducted on the operation and control of wind turbine generators (WTGs) and other renewable energy sources. The IEC 61850 standard and its application to protection schemes were reviewed, and several adaptive protection algorithms were evaluated.

8.2.2 Modelling and Simulation in DIgSILENT PowerFactory

The modified IEEE 14-bus system was simulated within the DIgSILENT environment as a case study. We investigated the load flow and short circuit analysis of the MG system for both grid-connected and island modes of operation. The modified IEEE 14-bus distribution system comprises eight transmission lines with a directional overcurrent relay (SEL-351A) at both ends. A protection coordination study was conducted for the SEL-351A relays during both modes of operation. The coordination time interval (CTI) was sufficient for most of the identified relay pairs.

8.2.3 Modelling and simulation in RSCAD

The modified IEEE 14-bus system was modelled and simulated in the RSCAD software environment, which is a suite of RTDS. The 50-MW wind farm comprising the DG is linked to the distribution system at the POC. A permanent magnet synchronous generator (PMSG) is connected to the output of the type 4 wind turbine. Subsequently, the PMSG output is connected to an AC-DC-AC power electronics converter. The output of the power electronics converter circuit is linked to a step-up transformer, and the output from the step-up transformer is linked to a scaling transformer at the POC. To investigate the performance of the WTG at different wind speeds during the RSCAD runtime simulations, four case studies were considered.

8.2.4 Implementation of the hardware-in-the-loop simulation of the microgrid protection scheme

HIL protection testing was implemented to evaluate the proposed protection scheme, thus ensuring validation of the protection and control functionality before field commissioning. The modified IEEE 14-bus system was modelled in the RSCAD software environment. The CT and VT models required by the primary and backup relays were added to the RSCAD draft. The output signals from these instrument transformer models were connected to the analogue output (GTAO) model. The front panel interface (GTFPI) model was added and configured to receive the binary output signals for the trip from the external IEDs that interfaced with the RTDS. The output signals from the GTFPI model were connected to the circuit breaker logic. A three-phase fault was applied during the RSCAD runtime simulation, and the performance of the protection relays was investigated.

SEL Quickset software was used to configure the overcurrent settings and relay logic of the SEL-351A relay. The SEL SynchroWAVe event software was used to analyse the COMTRADE event file downloaded from the SEL-351 relay. From the simulation results, it can be concluded that the SEL-351A relays responded appropriately to the fault conditions.

8.2.5 Implementation of the hardware-in-the-loop simulation for testing the IEC 61850 GOOSE

To test the protection functionality of the directional overcurrent relays, a laboratory-scale test bench for the demonstration of the IEC 61850 GOOSE communication was implemented at the CSAEMS laboratory at CPUT. The AcSELerator Architect software was used to configure the IEC 61850 GOOSE messages published or subscribed to by IEDs. The data set contains a protection trip conditioning (PTRC) LN. The IEC 61850 IED Configuration Tool (ICT) within the GTNET-GSE model in RSCAD was used to configure the IEC 61850 GOOSE messages published or subscribed to by external IEDs through Ethernet.

The IED tripping times improved compared with the hardwired connection. The WireShark tool was used to analyse the GOOSE messages published through Ethernet. From the captured results, we can conclude that the IEC 61850 GOOSE message was successfully transmitted through Ethernet.

8.2.6 Implementation of the Adaptive Protection Scheme for the microgrid system

The MG can be operated in both grid-connected and island modes. The fault currents measured in the island mode of operation are less than those measured in the grid-connected mode. Consequently, conventional protection schemes are ineffective and may lead to a loss of coordination between the protection relays. Therefore, it is necessary to implement an adaptive protection scheme in which the relay settings are dynamically updated according to the status of the circuit breaker monitored by the relays. This ensures that the MG is always protected against fault currents, regardless of the network configuration. The adaptive protection scheme has been implemented for both hardwired connections and standard IEC 61850 communication between IEDs. The status of the circuit breakers' position at the PCC was used to identify the network topology (e.g., grid-connected or islanded). The circuit breakers were in the closed position during the grid-connected mode and in the open position during the islanded mode of operation.

To implement the adaptive protection scheme for the SEL-351A relays, a 110 V DC auxiliary supply was hardwired between the CMC 356 secondary-injection test set and the opto-isolated input IN101.

Adaptive protection based on the IEC 61850 standard was implemented for the SEL-700G IED. The GTNET-GSE model was used to configure the IEC 61850 GOOSE message published by RTDS. The logical node representing the position status of the circuit breaker was mapped to the virtual bits VB001 and VB002 of the SEL-700G IED. Circuit breaker control was used to open and close the circuit breakers during the RSCAD runtime.

The SEL351A and SEL-700G IEDs were changed to group 1 for the grid-connected mode (circuit breaker closed) and to group 2 for the islanded mode (circuit breaker open).

8.3 Academic and Industrial Applications

The DIgSILENT and RSCAD simulation results can assist both undergraduate and postgraduate students in modelling and simulating power system networks, understanding load flow and short-circuit simulation studies, and understanding how integrated DGs can affect the performance of the protection scheme implemented in MGs.

It is recommended that power utilities develop and implement the IEC 61850 standard-based adaptive protection scheme for MG systems to overcome the loss of coordination associated with traditional protection schemes. This may lead to the blinding of overcurrent relays or false tripping, leading to the disconnection of the DG and reducing the reliability of the supply to the customer.

8.4 Future research

This research project only focused on developing a decentralised adaptive protection algorithm whereby the IEC 61850 GOOSE communication was implemented between the local IEDs. Future research could consider the development of a centralised adaptive protection scheme whereby the IEC 61850 GOOSE communication is implemented between the local IEDs and a microgrid-centralised controller (MGCC). The SEL Real-time Automation Controller (RTAC) can be used as an MGCC. The SEL-700G IEDs and SEL RTAC can be interfaced with the RTDS to enable real-time simulations. Each SEL-700G IED has six setting groups available to allow for several network topologies within the modified IEEE 14-bus system to be tested. In addition to the operation of circuit breakers at the PCC, the circuit breakers at the POC can also be operated for the connection and disconnection of the DG. The MGCC can be configured to publish an IEC 61580 GOOSE message via Ethernet to update the setting group for the protection IEDs, depending on the network topology.

8.5 Publications

1. H. de Graaff Genis and S. Krishnamurthy, "Microgrid Protection Simulation and Testing using a Relay-Secondary Injection Device Testbed," *2024 32nd Southern African Universities Power Engineering Conference (SAUPEC)*, Stellenbosch, South Africa, 2024, pp. 1-6, doi: 10.1109/SAUPEC60914.2024.10445048

2. H.D.G. Genis and S. Krishnamurthy, 2024. Real-time hardware-in-the-loop testing of an adaptive protection scheme for a microgrid system. Manuscript drafted and will submit to the International Journal of Electrical Power and Energy Systems, Elsevier.

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Abuhilaleh, M., Li, L., & Hossain, M. J. (2020). Power management and control coordination strategy for autonomous hybrid microgrids. *IET Generation, Transmission and Distribution*, *14*(1), 119–130. https://doi.org/10.1049/iet-gtd.2018.5708.

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APPENDICES

APPENDIX A
CONFIGURATION OF RSCAD POWER SYSTEM COMPONENTS

A.1 Synchronous generator

The synchronous generator along with its exciter and governor controls is shown in Figure A.1. The speed of the prime mover is maintained through an electronically controlled rectifier known as the governor. The parameters of the governor are shown in Figure A.2. The exciter is used to supply a DC to the rotor winding to produce the rotor magnetic field. The parameter for the exciter is shown in Figure A.3.

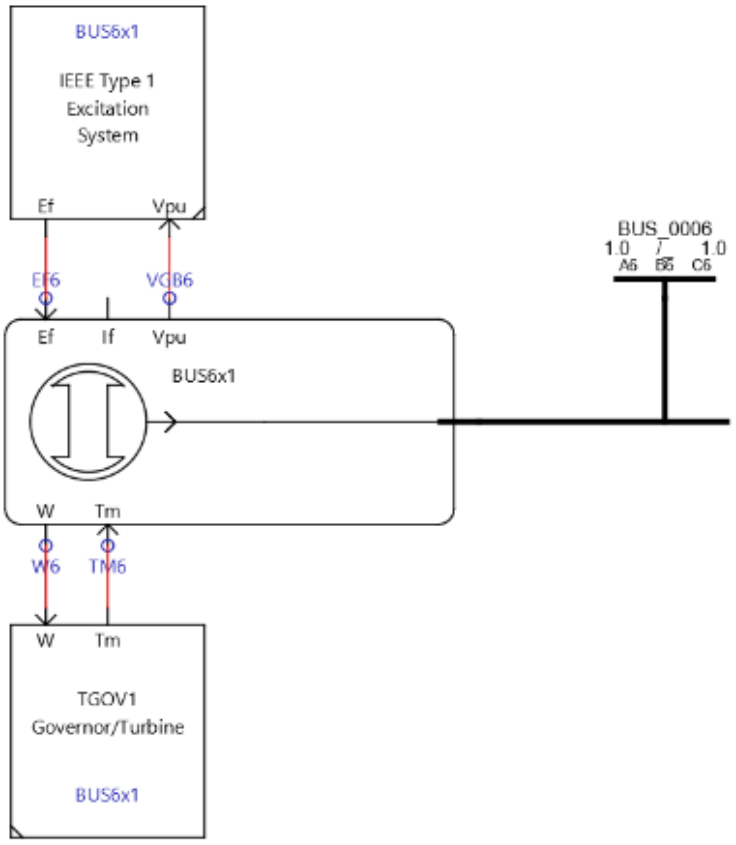

Figure A.1: Modelling of synchronous generator in RSCAD

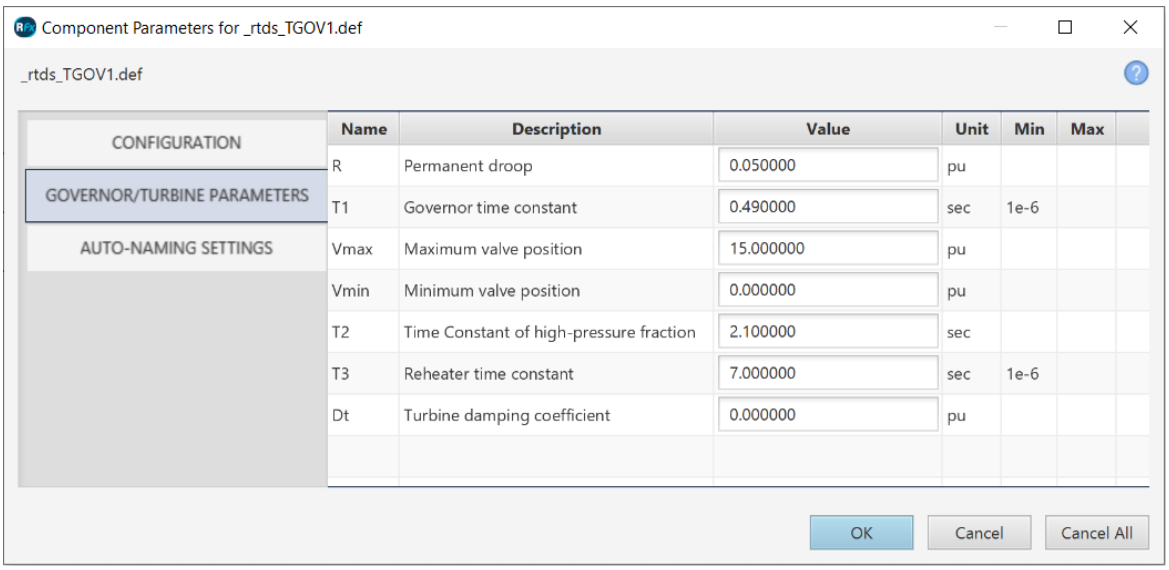

Figure A.2: Parameters of the governor

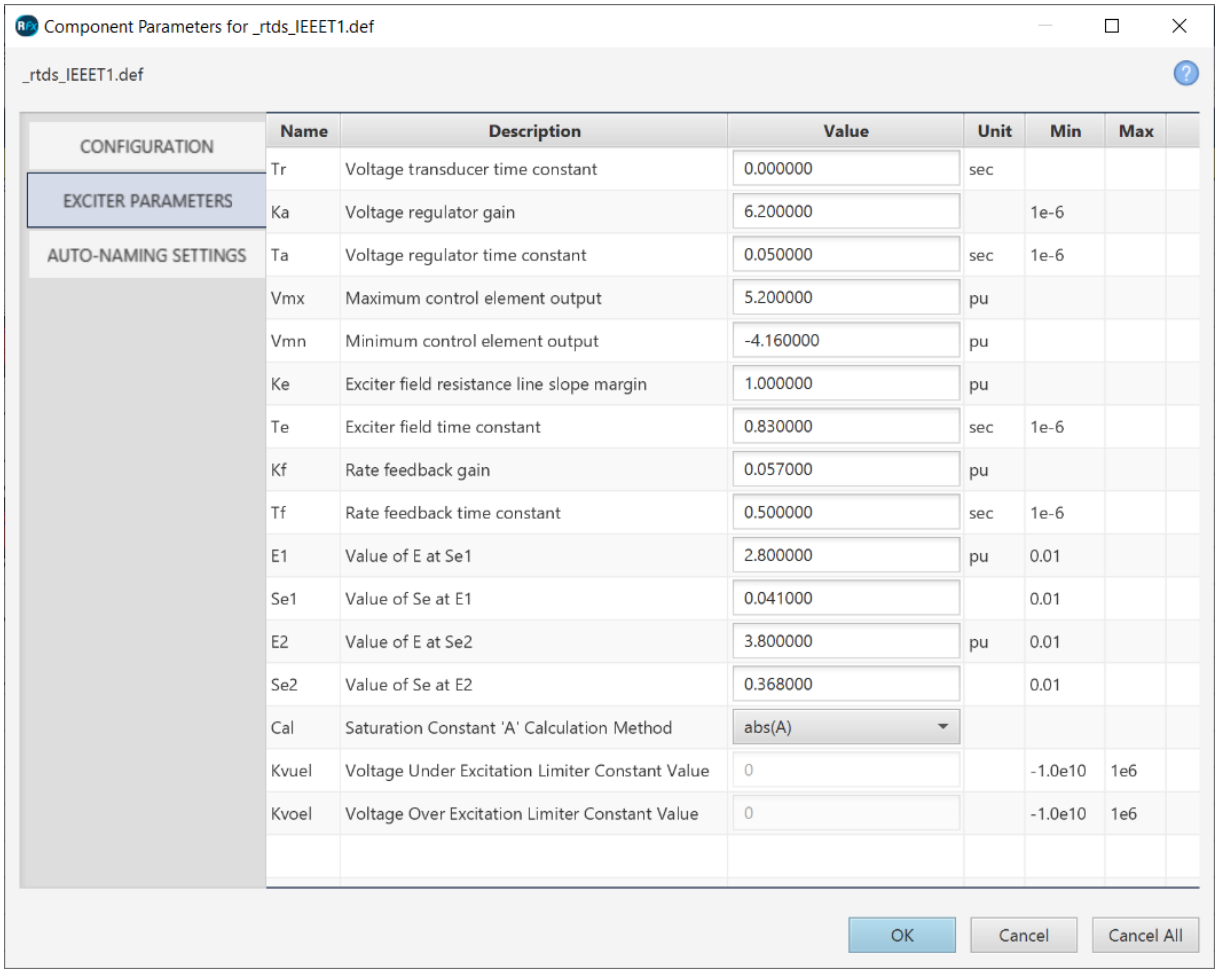

Figure A.3: Parameters of the exciter

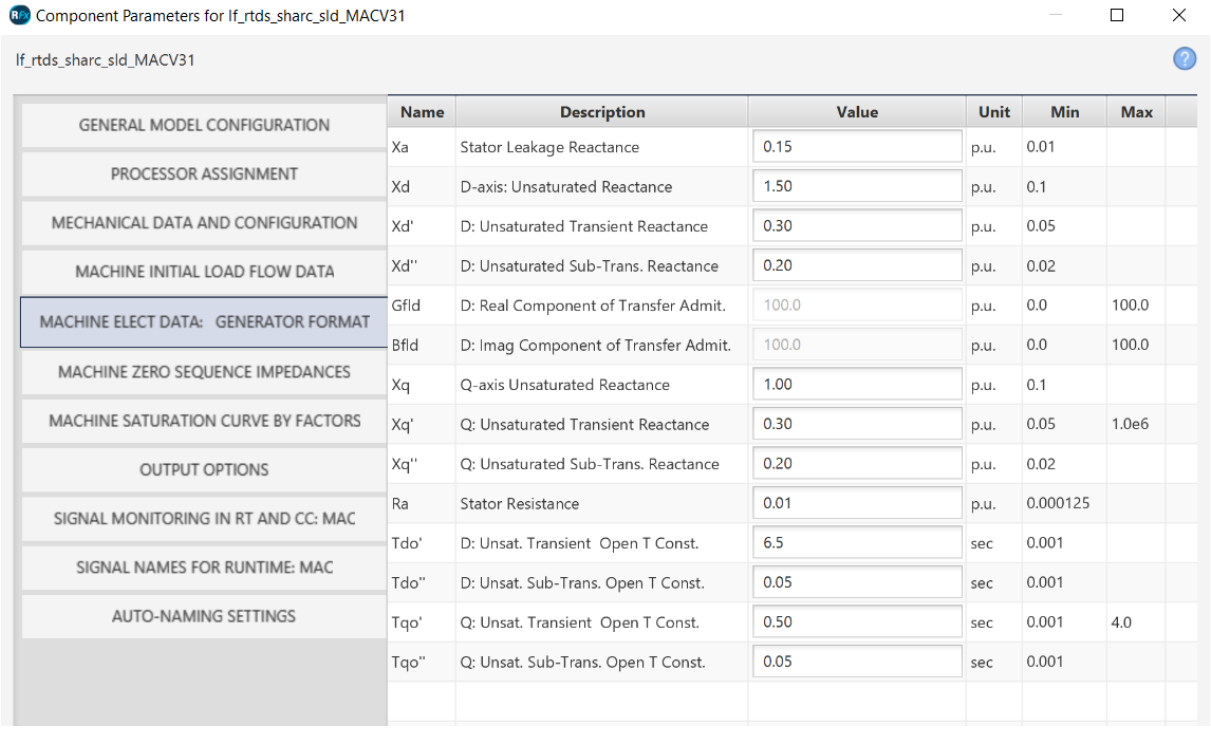

Figure A.4: Configuration of the electrical parameters for the generator

A.2 Voltage source

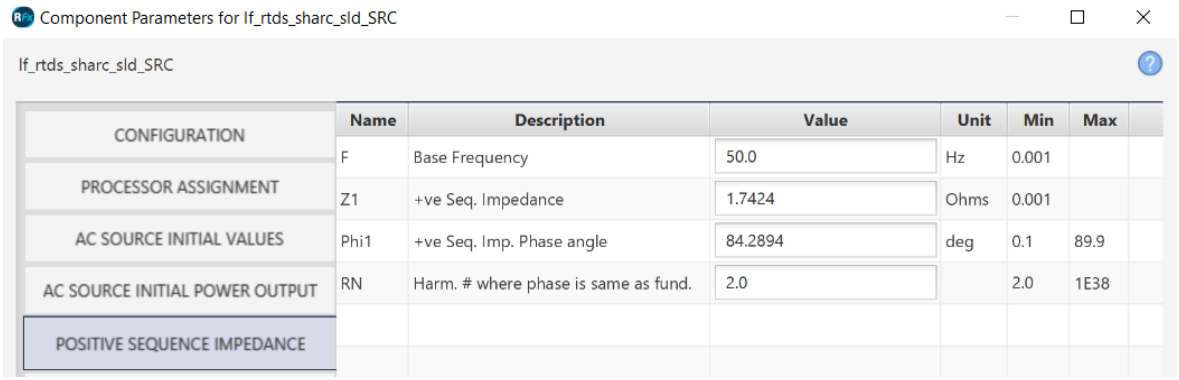

Figure A.5: Configuration of the voltage source

A.3 Wind turbine generator

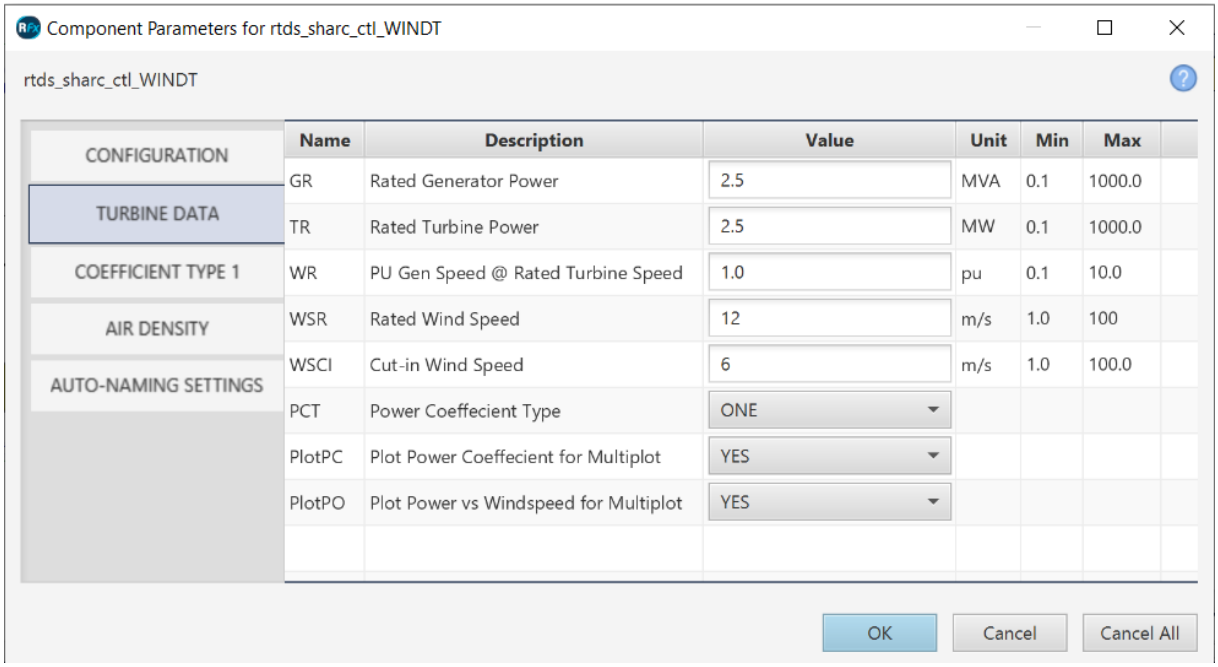

Figure A.6: Configuration of the wind turbine

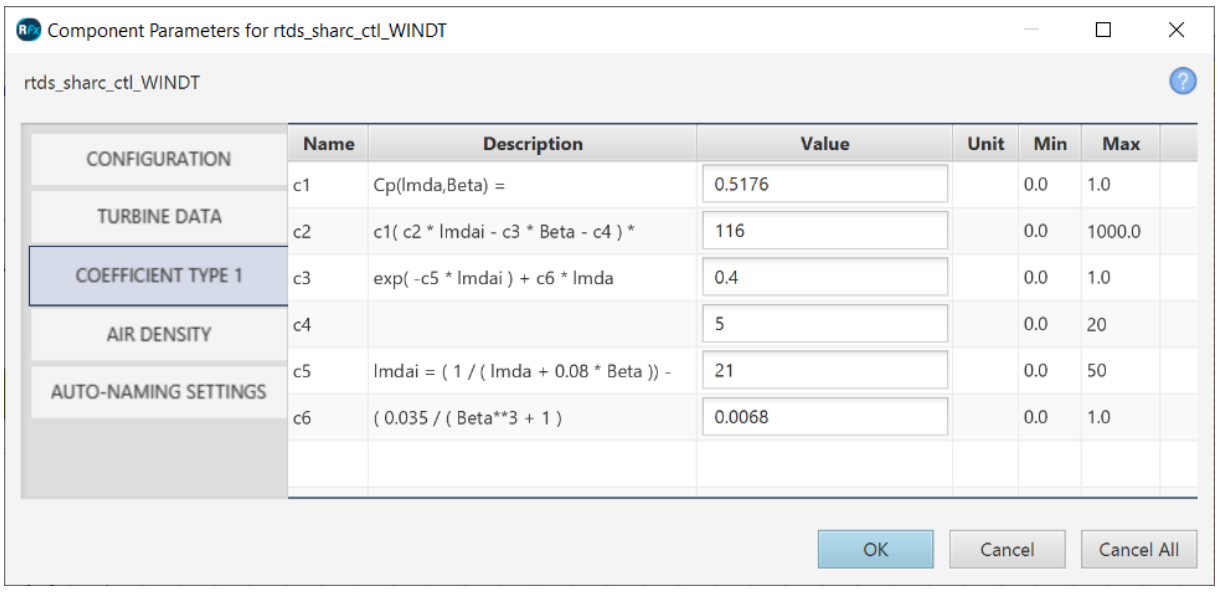

Figure A.7: Configuration of coefficient data for the wind turbine

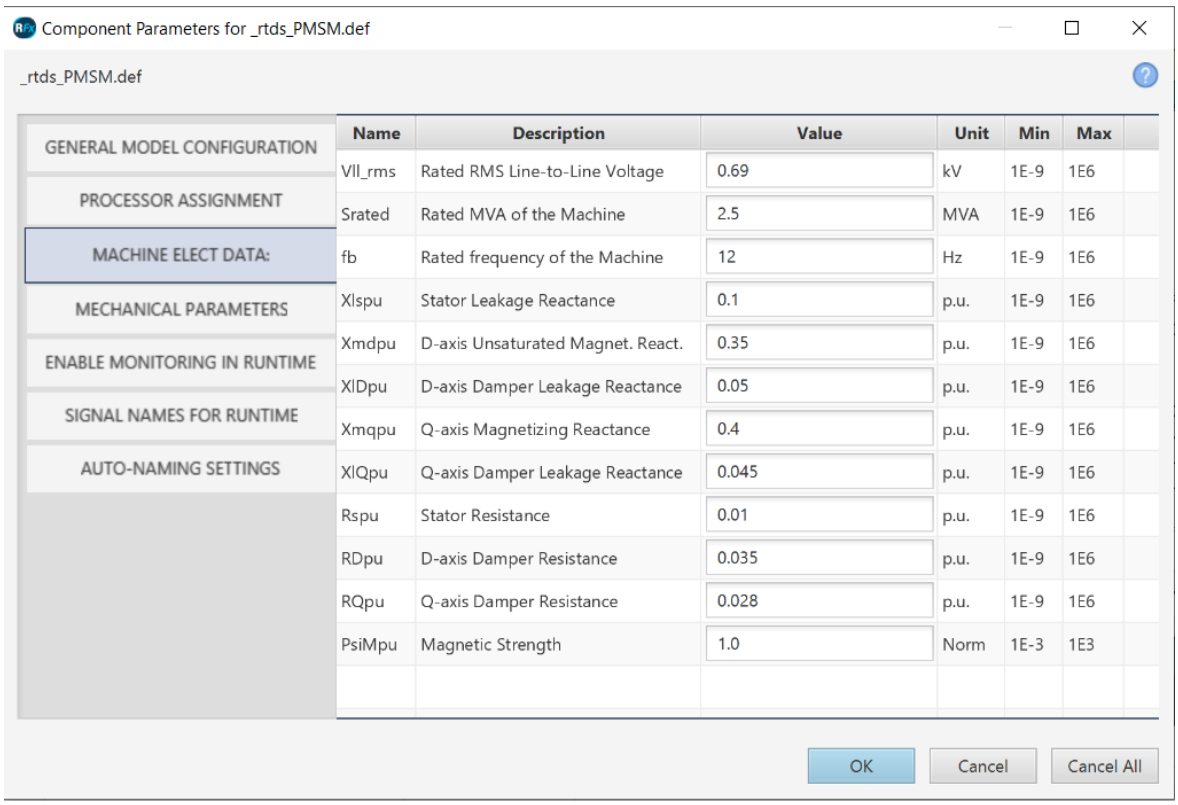

Figure A.8: Configuration of the PMSG electrical parameters

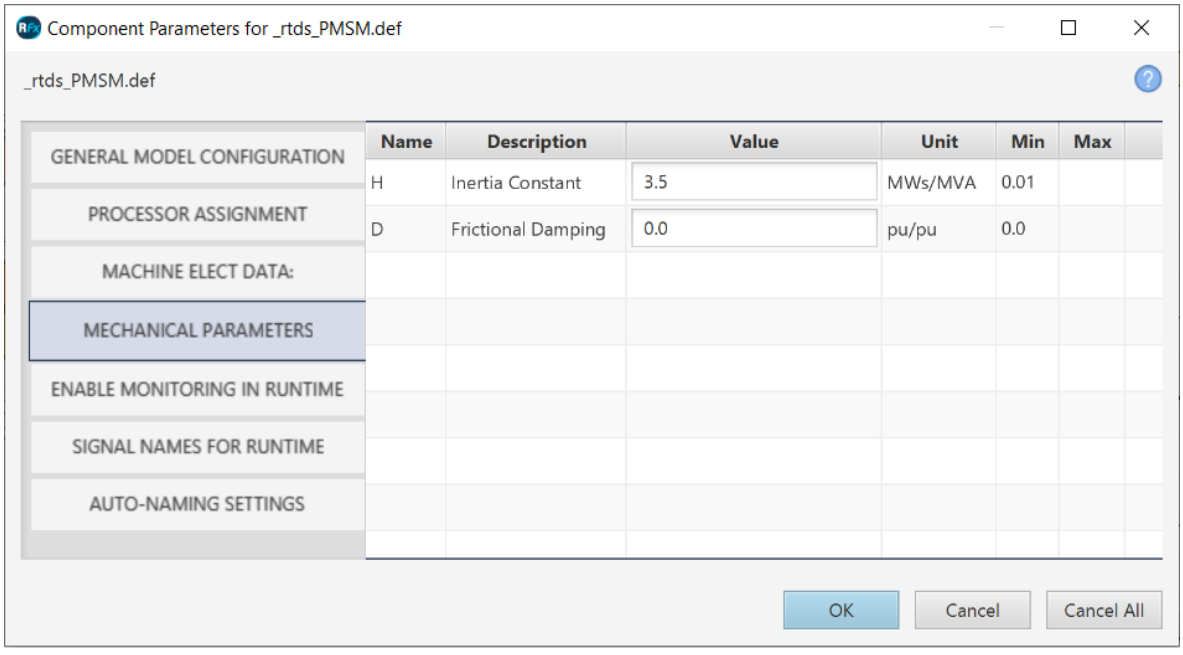

Figure A.9: Configuration of the PMSG mechanical parameters

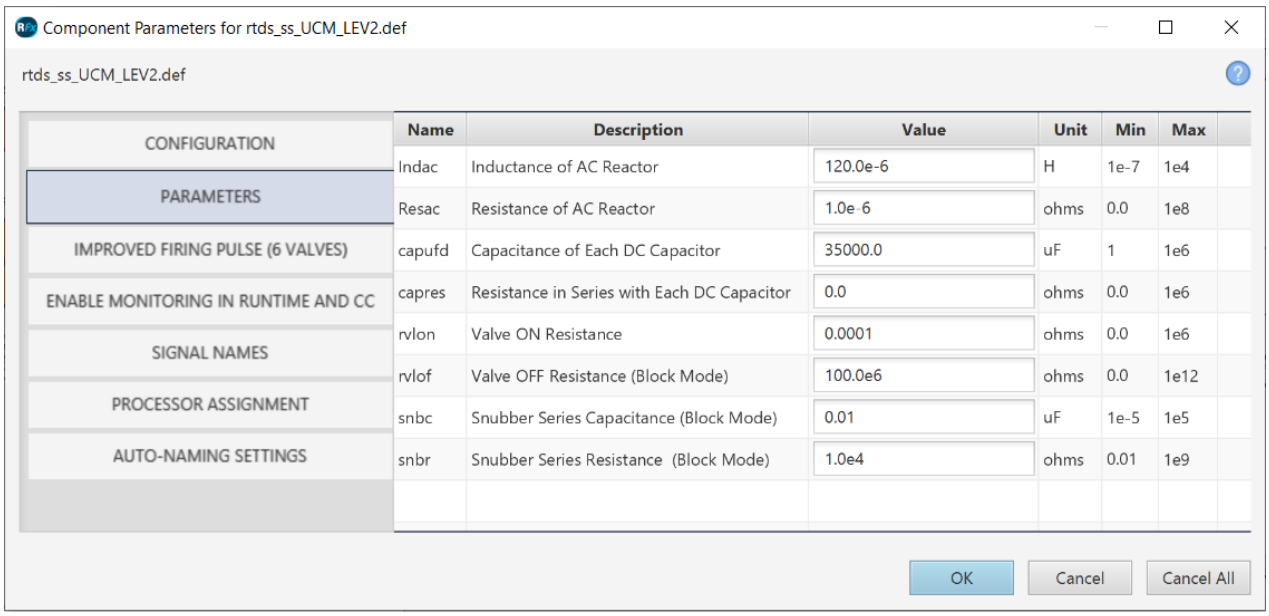

Figure A.10: Configuration of the power electronics converter

A.4 Power transformers

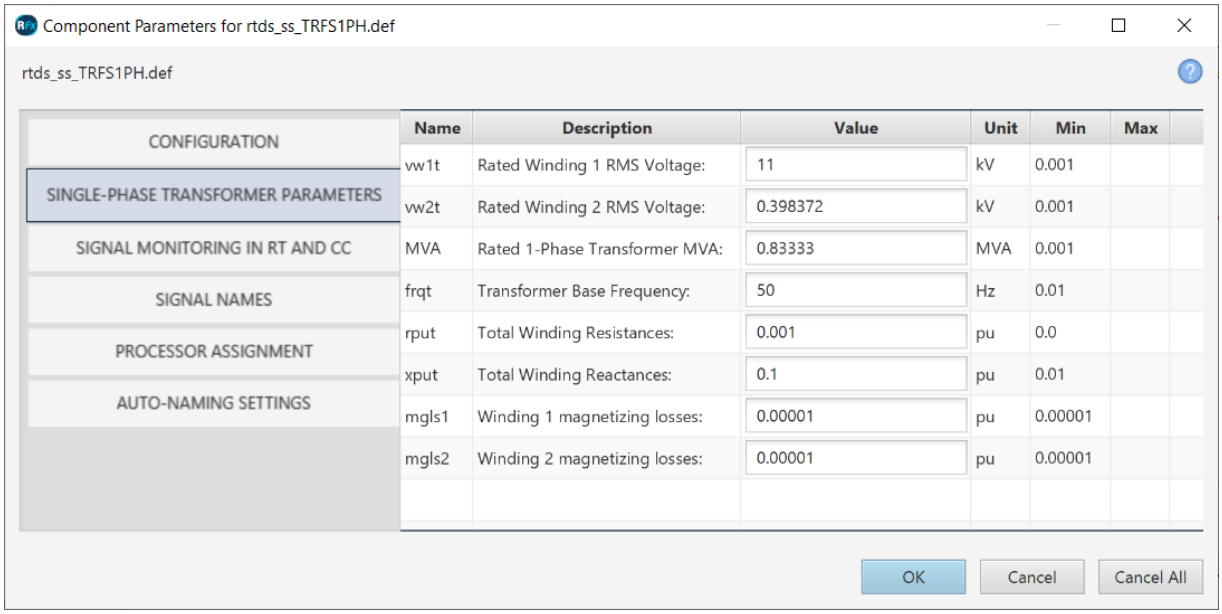

Figure A.11: Configuration of the parameters for the transformer between the grid-side converter and the scaling transformer at the PCC

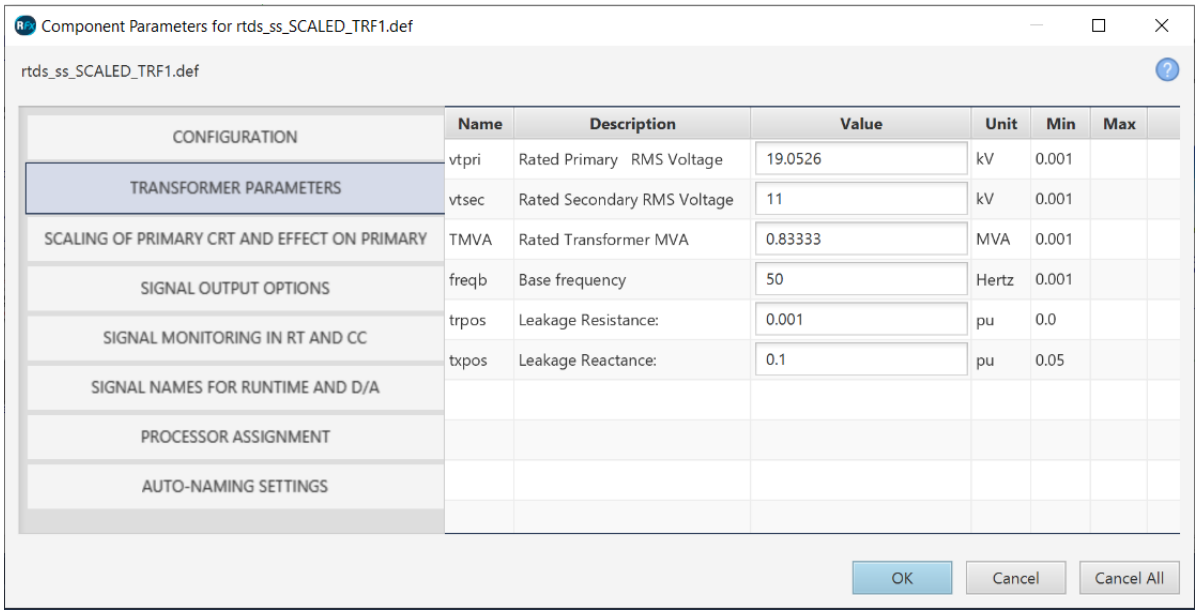

Figure A.12: Configuration of the parameters for the scaling transformer at the PCC

APPENDIX B
WIND TURBINE CONTROLS

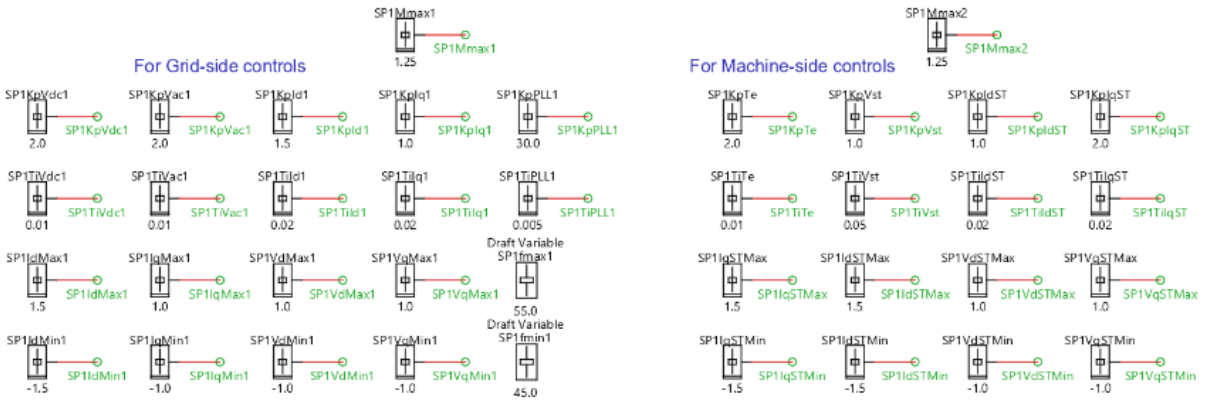

Figure B.1: PI parameters for control loops

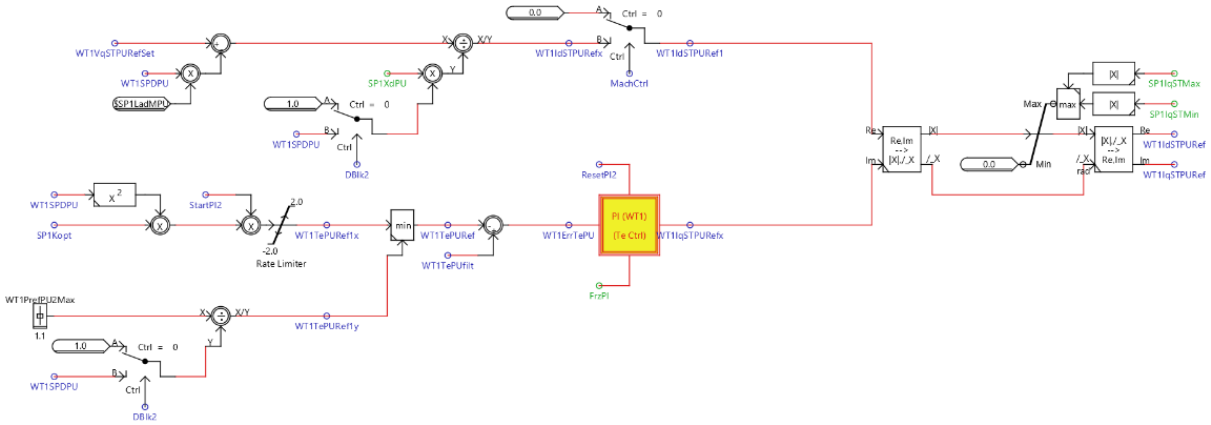

Figure B.2: Torque and Q control loops at the machine side

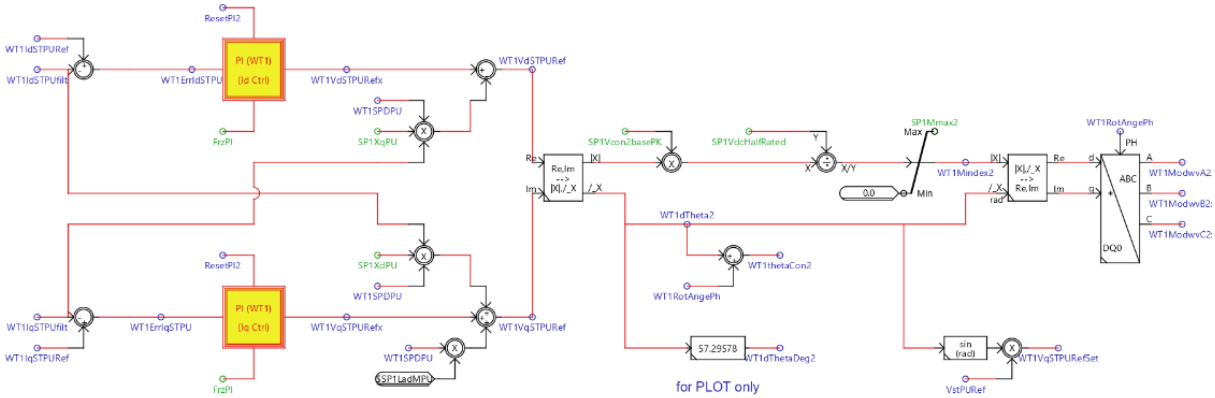

Figure B.3: Decoupled controls for I_d and I_q at the machine side

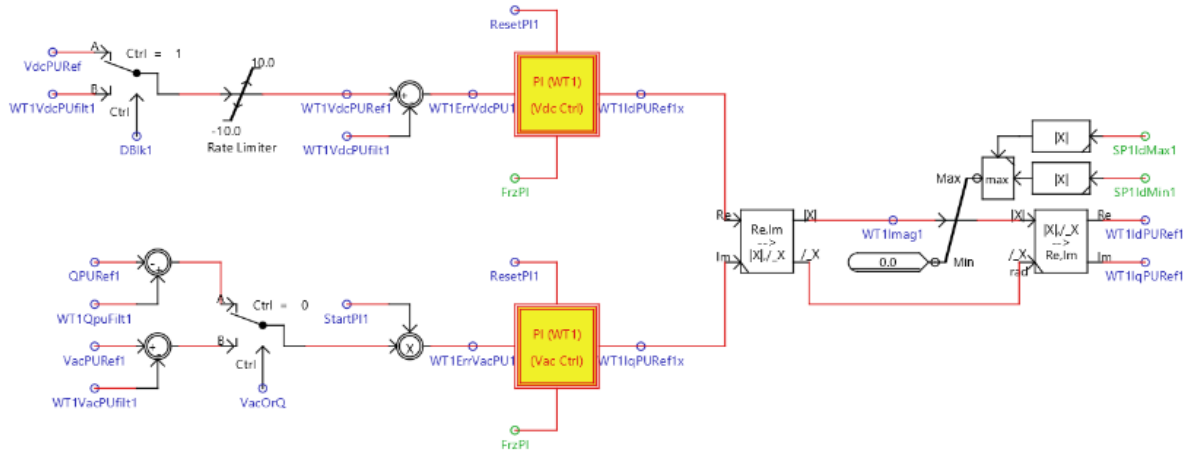

Figure B.4: V_{DC} voltage control loop at the grid side

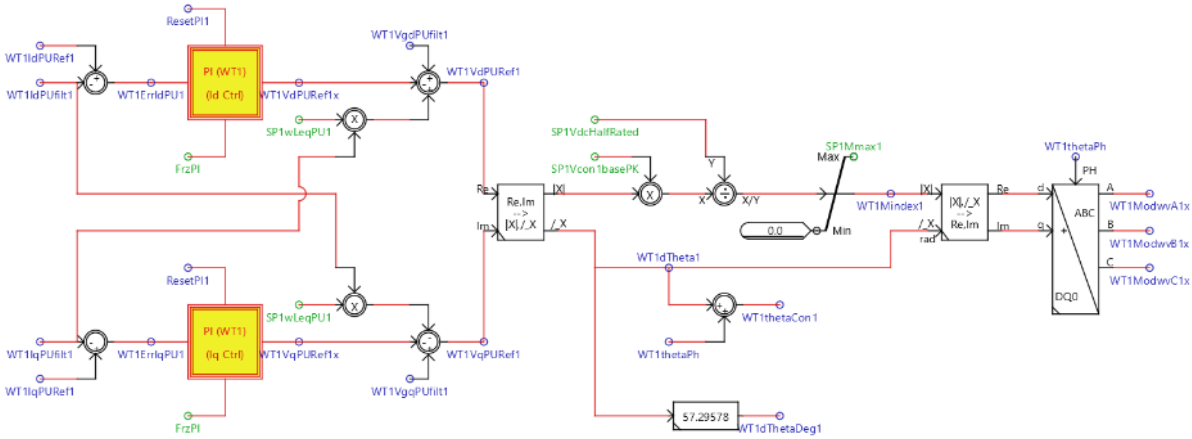

Figure B.5: Decoupled controls for I_d and I_q at the grid side

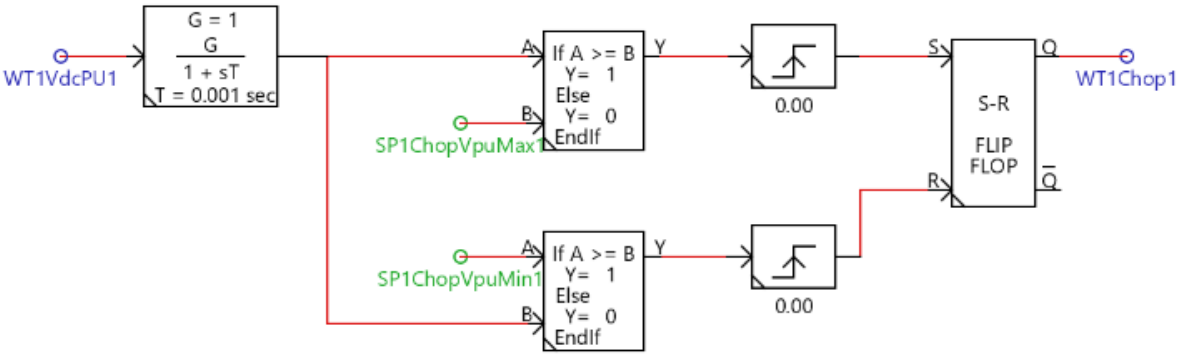

Figure B.6: Logic for DC chopper control

APPENDIX C
TRANSMISSION LINE DATA

The modelling of the transmission line is completed using the TLine editor in the RSCAD software. A line length of 15km is chosen for the 33kV line as shown in Figure C.1. This represents a short transmission line. The frequency is set to 50Hz. The Aluminium Cable Steel Reinforced (ACSR) conductor with code name “Parrot” is selected as shown in Figure C.2. The current rating for this conductor is 1315A at 75°C.

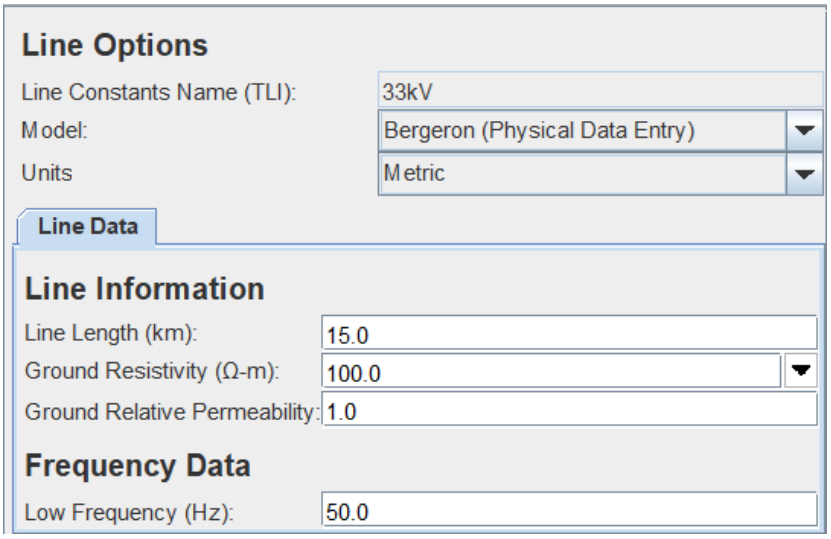

Figure C.1: Transmission line information

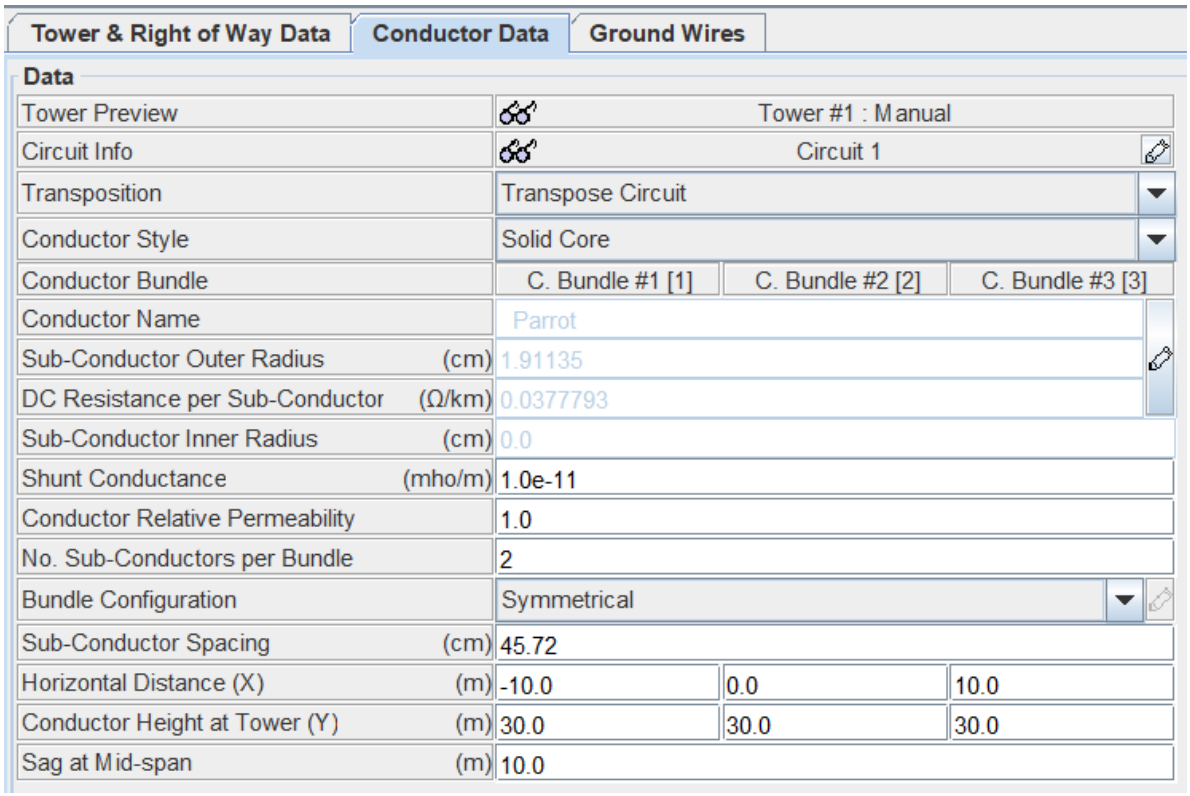

Figure C.2: Parameters for the phase conductor

The spacing between the sub-conductors is 45.72cm. This gives a geometric mean radius (GMR) of 9.348 Cm. The parameters for the ground wire are shown in Figure C.3. The overall dimensions for the transmission line are given in Figure C.4.

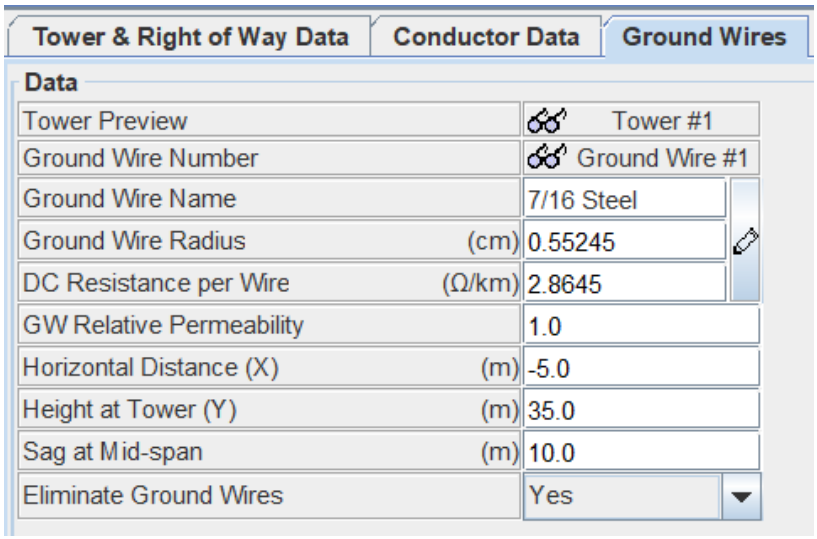

Figure C.3: Parameters for the ground wire

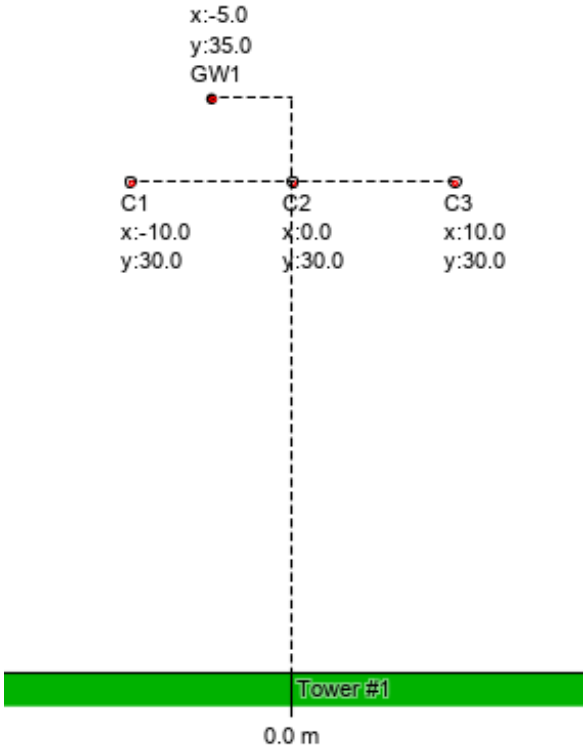

Figure C.4: Overall dimensions of the transmission line

APPENDIX D
CONFIGURATION OF SEL-351A RELAYS

The CT ratio and PT ratio are configured under the general settings tab, as shown in Figure D.1. The CT ratio is 1000/1 A, and the PT ratio is 33000/110 V.

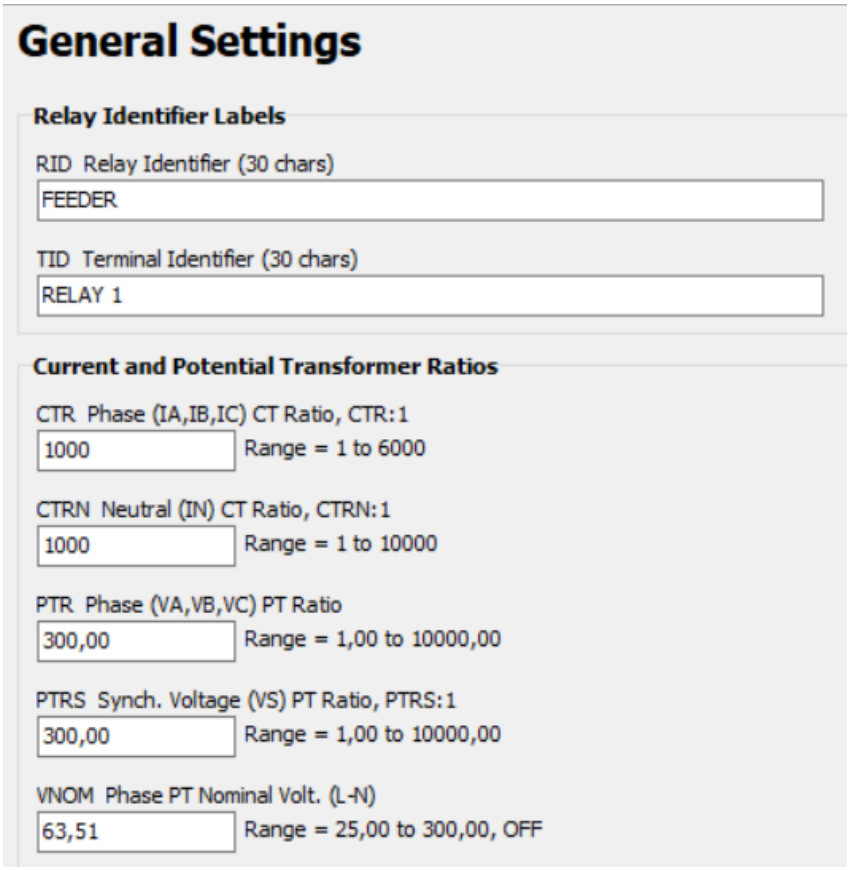

Figure D.1: Configuration of the general settings

The current pickup and time delay for the phase overcurrent (50P) element are configured as shown in Figure D.2.

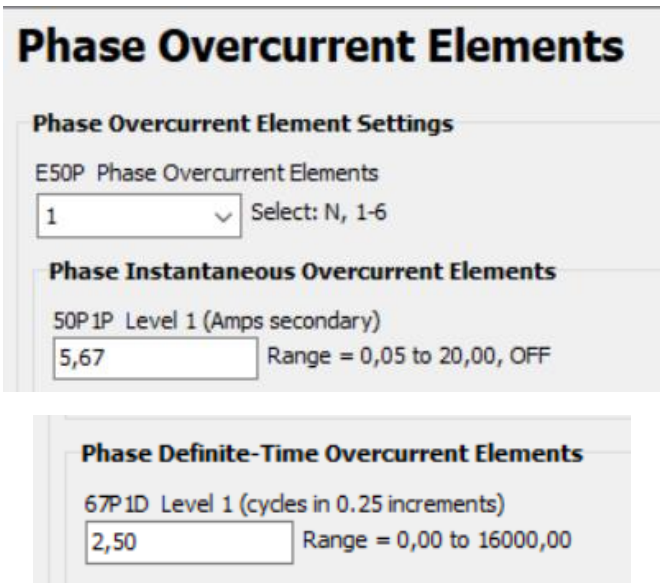

Figure D.2: **Configuration of the phase overcurrent settings**

The phase time-overcurrent (51P) element is configured as shown in Figure D.3. This includes the current pickup, characteristic curve, and time multiplier setting. The C1 (IEC Standard Inverse) curve type is selected.

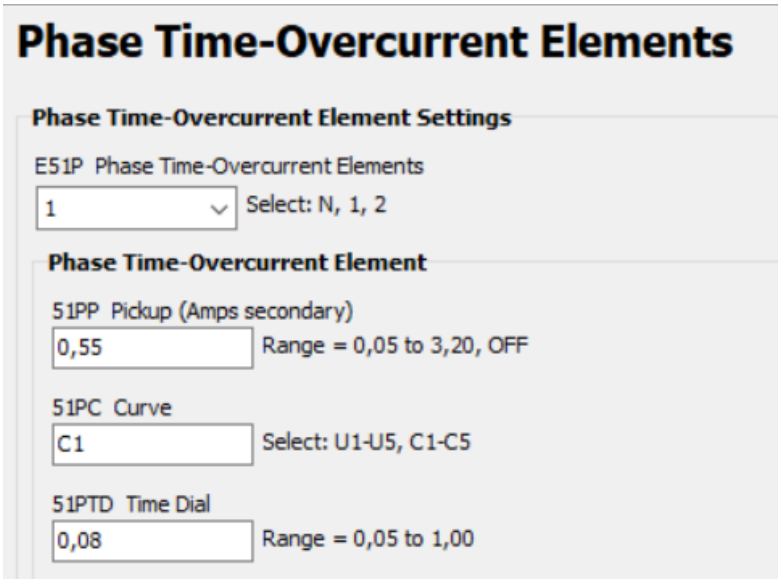

Figure D.3: **Configuration of the phase time-overcurrent settings**

The current pickup setting and time delay for the neutral ground overcurrent (50N) element are configured as shown in Figure D.4.

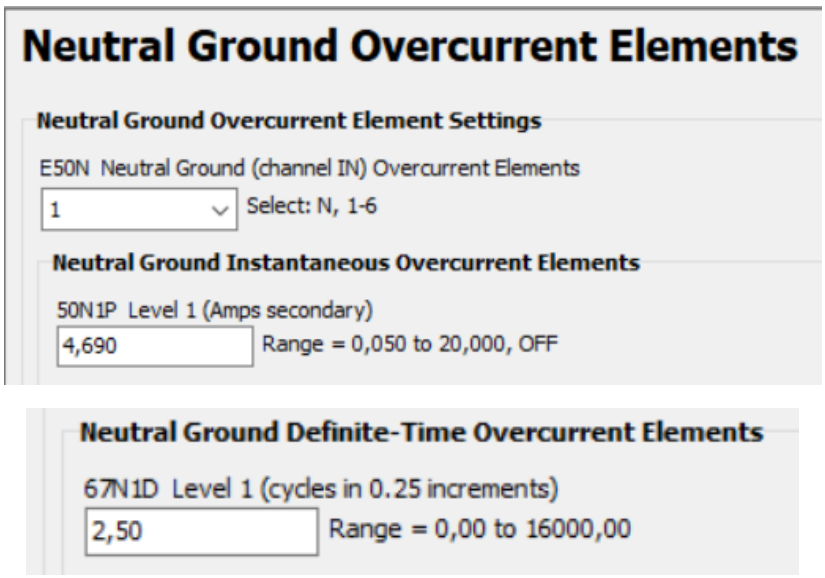

Figure D.4: Neutral ground overcurrent settings

The neutral ground time-overcurrent (51P) element is configured as shown in Figure D.5. This includes the current pickup, characteristic curve, and time multiplier setting. The C1 (IEC standard inverse) curve type is selected.

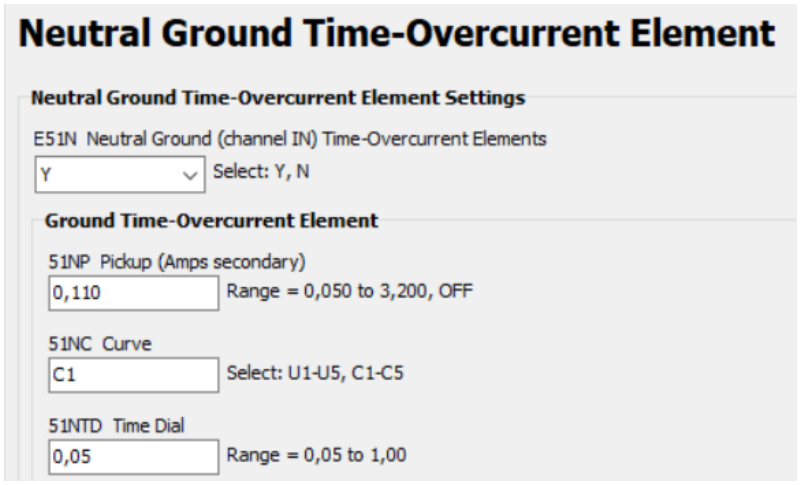

Figure D.5: Neutral ground time-overcurrent settings

The equations for the trip conditions and output contacts are configured as shown in Figures D.6 and D.7, respectively.

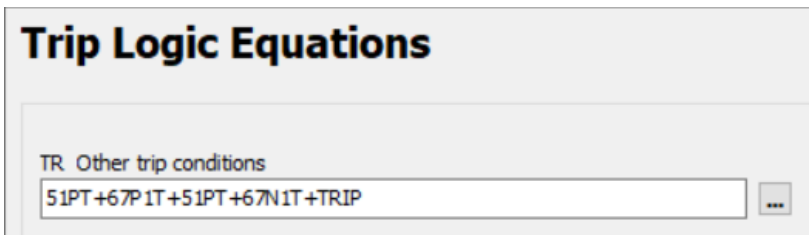

Figure D.6: Trip logic equations

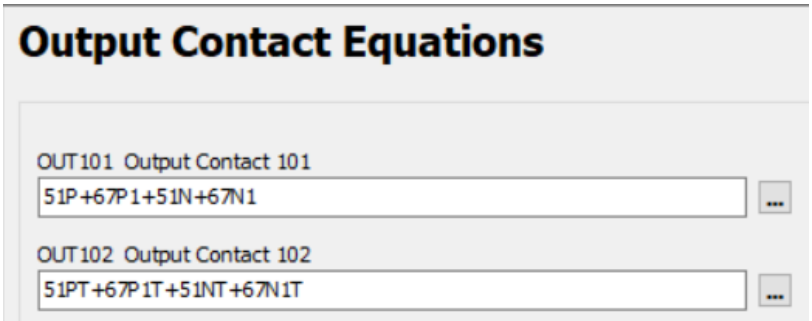

Figure D.7: Output contact equations